ACT88327

Advanced PMIC with 3 Bucks, 2 LDOs, and Load Bypass Switches

BENEFITS and FEATURES

- **Wide input voltage range**
  - Vin = 2.7V to 5.5V
- **Complete integrated power solution**
  - One 2A avg / 3A peak DC/DC Step-Down (Buck) Regulator with Bypass Function
  - One 2A avg / 3A peak DC/DC Step-Down (Buck) Regulator
  - One 1A avg / 1.5A peak DC/DC Step-Down (Buck)
    Regulator2
  - Two 300mA LDOs
- **Space Savings**
  - Fully integrated
  - High Fsw =2.25MHz or 1.125MHz
  - Works with 0.47µH Inductor
  - Integrated sequencing
- **Easy system level design**
  - Configurable sequencing
  - Multiple Wake up Triggers with GPIOs
  - Seven Programmable GPIOs
- **Buck 1 Bypass Mode for 3.3V system level compliance**
- **Highly configurable**
  - uP interface for status reporting and controllability
  - Programmable Reset and Power Good GPIO's
  - Flexible Sequencing Options
  - Multiple Sleep Modes
- **I^2C Interface – 1MHz**

APPLICATIONS

- Solid-State Drives (SSD)
- FPGA
- Computer Vision
- Portable Audio / Video

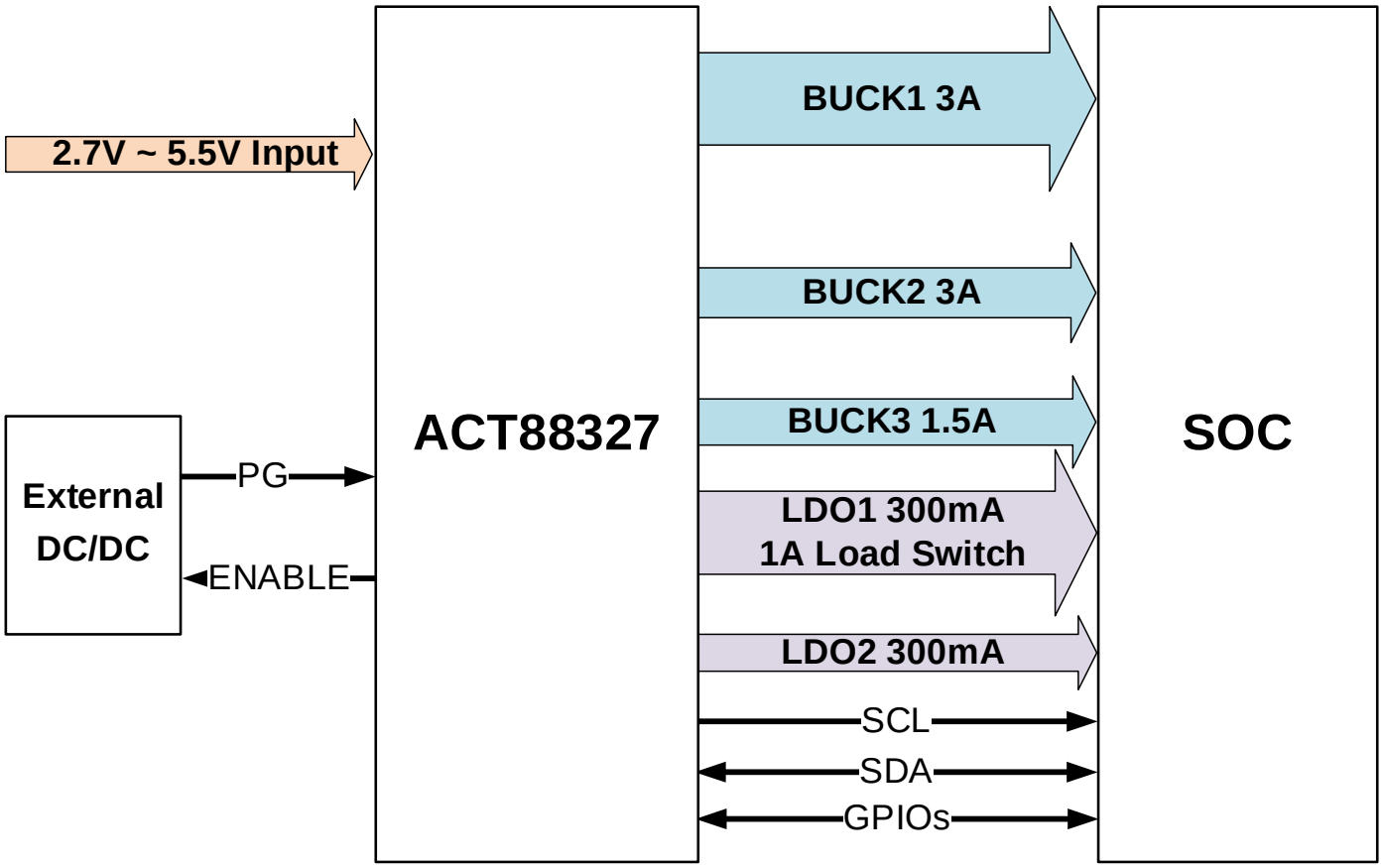
GENERAL DESCRIPTION

The ACT88327 PMIC is an integrated ActiveCiPS™ power management integrated circuit. It powers a wide range of processors, including solid-state drive applications, video processors, FPGA's, wearables, peripherals, and microcontrollers. The ACT88327 is optimized for SSD and FPGA applications. It is highly flexible and can be reconfigured via I^2C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc. ACT88327 is programmed at the factory with a default configuration. These settings can be optimized for a specific design through the I^2C interface. The ACT88327 is available in several default configuration. Contact the factory for specific default configurations.

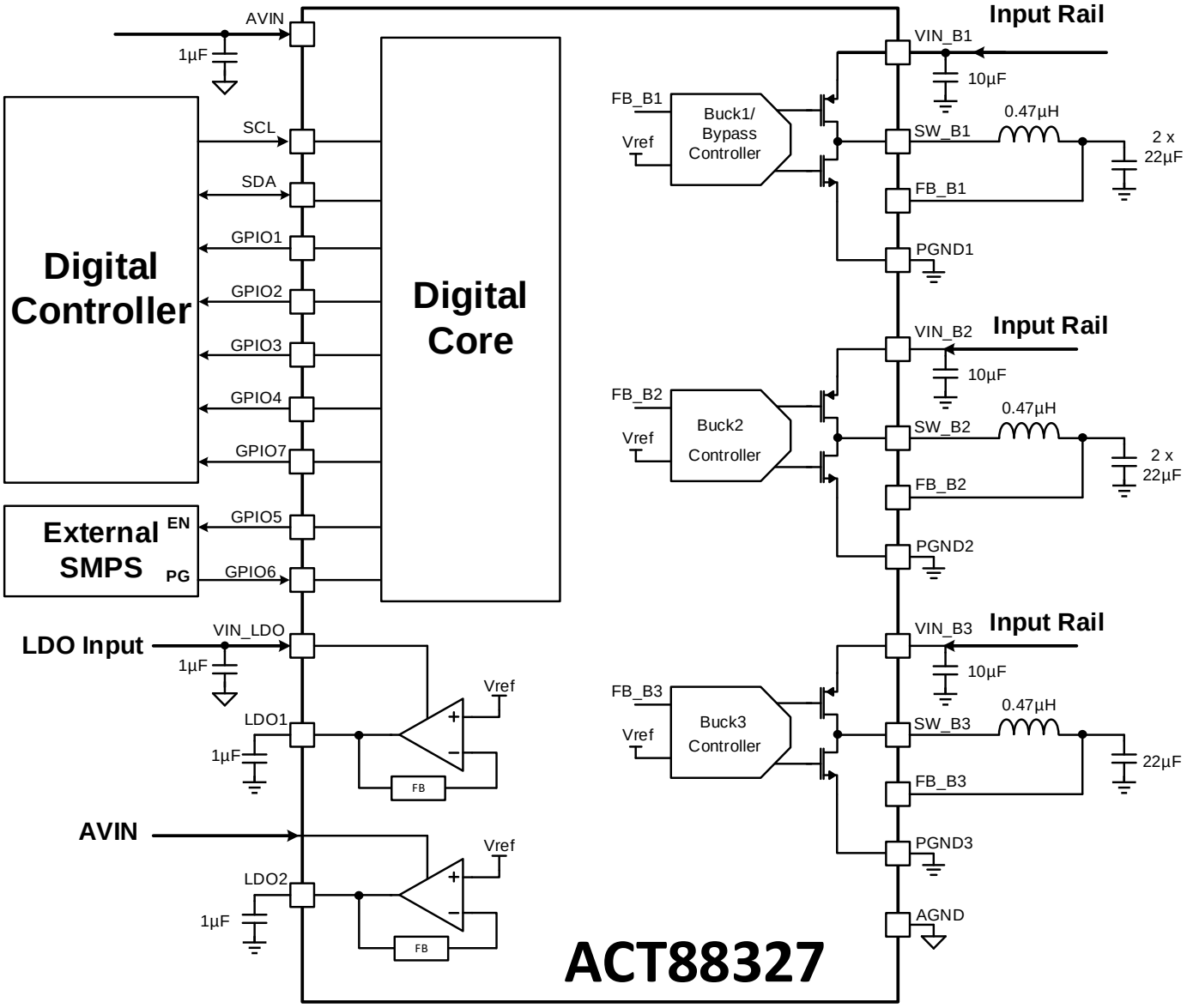
The core of the device includes three DC/DC step down converters using integrated power FETs, two low-dropout regulators (LDOs). Buck1 and LDO1 can be configured as a load switch. Each DC/DC regulator switches at either 1.125MHz or 2.25MHz, requiring only three small components for operation. The LDOs only require small ceramic capacitors. All are highly configurable via the I^2C interface.

The ACT88327 PMIC is available in a 2.18 x 2.581 mm 30 ball WLCSP package.

TYPICAL APPLICATION DIAGRAM

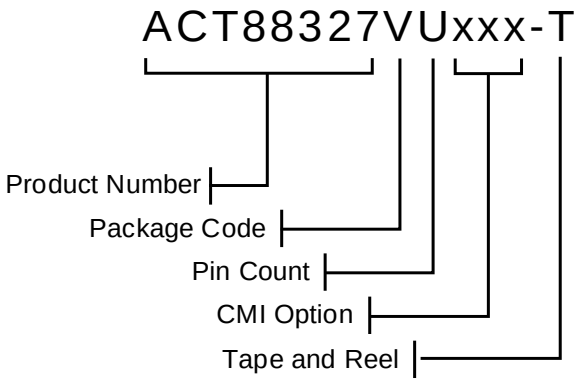


FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{LDO1}	V_{LDO2}	7-bit I^2C Address	Package
ACT88327VU101-T	2.9V	0.9V	1.8V	2.5V	1.8V	0x25h	30 pin WLCSP



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Qorvo components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator. “V” represents CSP.

Note 4: Pin Count designator. “U” represents 30 pins.

Note 5: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION - WLCSP

	1	2	3	4	5
A	VIN_B1	SW_B1	PGND1	VIN_LDO1	LDO1
B	VIN_B1	SW_B1	PGND1	AVIN	LDO2
C	FB_B1	GPIO3	SDA	SCL	GPIO4
D	GPIO7	GPIO2	GPIO5	GPIO6	AGND
E	FB_B3	GPIO1	PGND23	SW_B2	FB_B2
F	VIN_B3	SW_B3	PGND23	SW_B2	VIN_B2

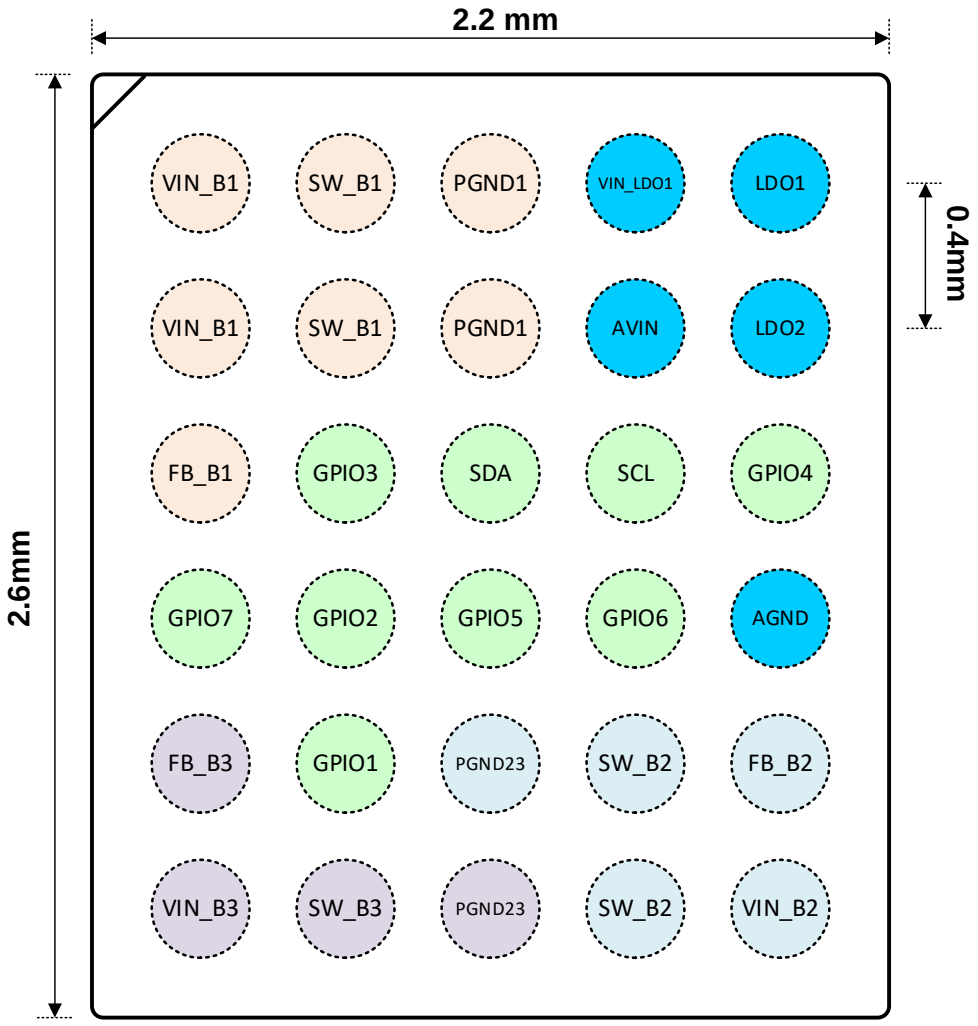


Figure 1: Pin Configuration – Top View (bumps down) – WLCSP- 30

PIN DESCRIPTIONS

Ball (CSP)	NAME	DESCRIPTION
A3, B3	PGND1	Dedicated Power Ground for Buck1 Regulator.
E3, F3	PGND23	Dedicated Power Ground for Buck1 and Buck3 Regulators
E4, F4	SW_B2	Switch Pin for Buck2 Regulator.
F5	VIN_B2	Dedicated VIN power input for Buck 2 Regulator.
E5	FB_B2	Feedback for Buck2 Regulator. Connect to the Buck2 output capacitor.
A5	LDO1	Output for LDO1 Regulator (Leave unconnected if LDO1 is not used and disabled).
A4	VIN_LDO	Dedicated VIN power input for LDO1 Regulator.
C4	SCL	I^2C Clock Input.
C3	SDA	I^2C Data Input and Output.
D5	AGND	Analog Ground. Kelvin connect to the other ground pins on the IC.
B5	LDO2	Output for LDO2 Regulator (Leave unconnected if LDO2 is not used and disabled).
E1	FB_B3	Feedback for Buck3 Regulator. Connect to the Buck3 output capacitor.
F1	VIN_B3	Dedicated VIN power input for Buck3 Regulator.
F2	SW_B3	Switch Pin for Buck3 Regulator.
E2	GPIO1	Configurable general-purpose input/open drain output.
D2	GPIO2	Configurable general-purpose input/open drain output.
C2	GPIO3	Configurable general-purpose input/open drain output.
C5	GPIO4	Configurable general-purpose input/open drain output.
D3	GPIO5	Configurable general-purpose input/open drain output.
D4	GPIO6	Configurable general-purpose input/open drain output.
D1	GPIO7	Configurable general-purpose input/open drain output.
C1	FB_B1	Feedback for Buck1 Regulator. Connect to the Buck1 output capacitor.
B4	AVIN	Analog Input supply and power input for LDO2. This is also the pin that is monitored for VIN OV and UV.
A1, B1	VIN_B1	Dedicated VIN power input for Buck1 Regulator.
A2, B2	SW_B1	Switch pin for Buck1 Regulator.

ABSOLUTE MAXIMUM RATINGS (NOTE1)

PARAMETER	VALUE	UNIT
All I/O and Power pins except PGND1, PGND2, PGND3, AGND	-0.3 to 6	V
Grounds: Any PGND referenced to AGND	-0.3 to +0.3	V
SW_Bx to PGNDx	-1 to VIN_Bx + 1	V
FB_Bx to PGNDx	-0.3 to AVIN + 0.3	V
LDO1 to AGND	-0.3 to VIN_LDO + 0.3 -0.3 to AVIN + 0.3 (Package option)	V
LDO2 to AGND	-0.3 to AVIN + 0.3	V
Junction to Ambient Thermal Resistance, CSP (Note2)	37	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Operating Junction Temperature	-40 to 125	°C
HBM ESD	2000	V
MSL Rating	1	

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.
Note2: Measured on Qorvo Evaluation Kit

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVIN, VIN_B1, VIN_B2, VIN_B3 (Note1)		2.7		5.5	V
VIN_LDO	LDO Mode	1.62		5.5	V
	NLSW Mode	0.4V		3	V
	PLSW Mode	1.62		AVIN	V
Operating Junction Temperature		-40		125	°C

Note1: AVIN must always be the highest input voltage to the IC.

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIOs Leakage Current	Output = 5V			1	µA
GPIOs Output Low (Open Drain)	IOL = 1mA			0.35	V
GPIOs Input Low				0.35	V
GPIOs Input High		1.25			V
GPIOs Delay Times			0		ms
			1		
			5		
			10		
GPIOs Deglitch Time			10		µs

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(VIO_IN = 1.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Inputs Voltage Range: VIN_B1 referenced to PGND1 VIN_B2 referenced to PGND2 VIN_B3 referenced to PGND3		2.7		5.5	V
VIN_LDO referenced to AGND	LDO Mode	1.62		5.5	V
	NLSW Mode	0.4		Min of (AVIN-1 or 3.6V)	
	PLSW Mode	1.62		AVIN	
UVLO Threshold Falling (Note 1)	VIN_LVL=0	2.5	2.6	2.7	V
	VIN_LVL=1	3.35	3.5	3.65	V
UVLO Hysteresis (Note 1)	VIN_LVL=0	50	100	150	mV
	VIN_LVL=1	250	300	350	mV
OV Threshold Rising – VIN_OV (Note 1)	From 3.7V to 5.8V with 0.3V steps. See details on OV table	-3.5	SET POINT	3.5	%
OV Hysteresis (Note 1)		100	200	300	mV
POK OV Interrupt Threshold Rising	From 3.5V to 5.6V with 0.3V steps. See details on POK_OV table	-3.5	SET POINT	3.5	%
POK OV Interrupt Threshold Hysteresis		100	200	300	mV
POK Deglitch Time OV or UV			5		µs
Operating Supply Current	All Regulators Disabled		42		µA
Operating Supply Current	All Regulators Enabled		260		µA
System Monitor (SYSMON) Programmable Range	In 100mV steps	2.7		4.8	V
System Monitor (SYSMON) Accuracy		-3.5	SET POINT	3.5	%
System Warning (SYSWARN) Programmable Range	In 100mV steps	2.7		5.7	V
System Warning (SYSWARN) Accuracy	In 100mV steps	-3.5	SET POINT	3.5	%
VIN Deglitch Time UV	Falling, enter UV		5		µs
VIN Deglitch Time UV	Rising, exit UV		100		µs
VIN Deglitch Time OV	Rising, enter OV		5		µs
VIN Deglitch Time OV	Falling, exit OV		200		µs
Thermal Shutdown Temperature TSD_SHUTDWN	Temperature rising		155		°C

Thermal Shutdown Hysteresis		30	°C
Startup Delay after initial AVIN	Time from AVIN > UVLO threshold to start of first regulator turning On. (zero turn on delay setting)	620 750	µs
Thermal Interrupt Threshold, TSD_ALERT	Temperature rising - Referenced to TSD_SHUTDWN	TSD_SHUTDWN - 30	°C
Thermal Interrupt Hysteresis		20	°C
Transition time from Deep Sleep (DPSLP) State to Active State	Time from PWREN pin low to high transition to time when the first regulator turns ON with minimum turn on delay configuration.	224 500	µs
	Using I^2C	84	µs
Transition time from Sleep State (SLEEP) to Active State	Time from I^2C command to clear sleep mode to time when the first regulator turns ON with minimum turn on delay configuration.	84	µs
Time to first power rail turn off	Time from turn Off command to when the first power rail turns off with minimum turn off delay configuration	180	µs
Startup Delay Programmable Range	ONDLY=000 ONDLY=001 ONDLY=010 ONDLY=011 ONDLY=100 ONDLY=101 ONDLY=110 ONDLY=111	0 0.5 1 2 4 8 16 32	ms
Turn Off Delay Programmable Range	OFFDLY=000 OFFDLY=001 OFFDLY=010 OFFDLY=011 OFFDLY=100 OFFDLY=101 OFFDLY=110 OFFDLY=111	0 0.5 1 2 4 8 16 32	ms
nRESET Programmable Range	TRST_DLY=000 TRST_DLY=001 TRST_DLY=010 TRST_DLY=011 TRST_DLY=100 TRST_DLY=101 TRST_DLY=110 TRST_DLY=111	0.5 1 2.5 5 10 20 50 100	ms
GPIOs Delay Programmable Range	IOx_DLY=00 IOx_DLY=01 IOx_DLY=10 IOx_DLY=11	0 1 5 10	ms

Note1: All Under-voltage Lockout, Overvoltage measurements are referenced between AVIN and AGND pin.

BUCK1 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_B1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 25mV steps	0.6		3.775	V
Maximum Output Current (Note1)		3			A
Maximum Operation Duty Cycle		99			%
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		40		µA
	Fixed On-time Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05), IC is in SLEEP or DEEP SLEEP Mode.		10		µA
Supply Current, Shutdown	Regulator Disabled		0.1		µA
Output Voltage Accuracy – PWM (Note2)	Default output voltage, I_{OUT} = 2A	-1	V_{NOM}	1	%
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 2A	1.5		1.5	%
Output Voltage Accuracy – PFM (Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM}	1	%
Output Voltage Accuracy – PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	1.5		1.5	%
Line Regulation	Default output voltage, V_{IN_B1} = 3.3V to 5.5V, PWM mode		0.05		%/V
Load Regulation	Default output voltage, PWM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B1} Rising	90.5	93	95.5	$\%V_{NOM}$
Power Good Hysteresis	V_{OUT_B1} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT_B1} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT_B1} Falling		3		$\%V_{NOM}$
Switching Frequency		2.00	2.25	2.36	MHz
		1.00	1.125	1.18	MHz
Soft-Start Period – Programmable	10% to 90% V_{NOM}		250 500		µs
Soft-Start Period	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B1_ILIMSET=0 B1_ILIMSET=1		3.8 5.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-20	ILIMSET	20	%
	At other set points	-25	ILIMSET	25	
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = all settings	+10	25	40	%

Low Side Peak Current Limit (Cycle-by-Cycle) ILIMSET (Note3)	B1_ILIMSET=0 B1_ILIMSET=1	3.8 5.0	A
PMOS On-Resistance	I_{SW} = -1A, VIN_B1 = 3.3V	50	mΩ
NMOS On-Resistance	I_{SW} = 1A, VIN_B1 = 3.3V	50	mΩ
SW Leakage Current – NMOS	V_{IN_B1} = 5V, V_{SW} = 5V	1.5	µA
SW Leakage Current – PMOS	V_{IN_B1} = 5V, V_{SW} = 0V	5	µA
Switching Rise / Fall Times	V_{IN_B1} = 5V B1_DRVADJ=00 B1_DRVADJ=01 B1_DRVADJ=10 B1_DRVADJ=11	2.2/2 1.9/1.9 1.7/1.8 1.6/1.7	ns
Output Pull Down Resistance	Enabled when regulator disabled, VOUT=0.1V	4.4	Ohms

Note1: There are only two balls for VIN_B1 and SW_B1 which is good for 2A average current for lifetime rating.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

BUCK1 ELECTRICAL CHARACTERISTICS, REGULATOR: – BYPASS MODE OPTION

(VIN_B1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Bypass Mode					
Input Voltage Range for By-Pass Mode		2.7	3.3	3.7	V
PMOS On-Resistance	I_{SW} = -1A, VIN = 3.3V		0.050		Ω
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	1.7	2.5	3.5	A
Internal PMOS Current Detection Deglitch Time			10		µs
Internal PMOS Current Shutdown (Note1)	Shuts down after deglitch time and stays off for Off Time	3.6	4.5	5.5	A
Internal PMOS Current Shutdown Deglitch Time			10		µs
Internal PMOS Current Shutdown Off time			14		ms
Internal PMOS Softstart	Only used with 3.3V Input		6.6		mV/us

Note1: There are only two balls for VIN_B1 and SW_B1 which is good for 2A average current for lifetime rating.

BUCK2 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B2 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 10mV steps	0.6		1.87	V
Maximum Output Current (Note1)		3			A
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		40		µA
	Fixed On-time Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05), IC is in SLEEP or DEEP SLEEP Mode.		10		µA
Supply Current, Shutdown	Regulator Disabled		0.1	3.5	µA
Output Voltage Accuracy – PWM(Note2)	Default output voltage, I_{OUT} = 1A	-1	V_{NOM}	1	%
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 1A	1.5		1.5	%
Output Voltage Accuracy - PFM(Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM}	1	%
Output Voltage Accuracy – PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	1.5		1.5	%
Line Regulation	Default output voltage, V_{IN_B2} = 3.3V to 5.5V, PWM mode		0.05		%/V
Load Regulation	Default output voltage, PWM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B2} Rising	90.5	93	95.5	$\%V_{NOM}$
Power Good Hysteresis	V_{OUT_B2} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT_B2} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT_B2} Falling		3		$\%V_{NOM}$
Switching Frequency		1.00 2.00	1.125 2.25	1.18 2.36	MHz
Soft-Start Period – Programmable	10% to 90% V_{NOM}		250 500		µs
Soft-Start Period	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B2_ILIMSET=0 B2_ILIMSET=1		3.8 5.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-20	ILIMSET	20	%
	At other set points	-25	ILIMSET	25	%
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = all settings	+10	+25	+40	%

Low Side Peak Current Limit (Cycle-by-Cycle) ILIMSET (Note3)	B2_ILIMSET=0 B2_ILIMSET=1	3.8 5.0	A
PMOS On-Resistance	I_{SW} = -500mA, VIN_B2 = 3.3V	80	mΩ
NMOS On-Resistance	I_{SW} = 500mA, VIN_B2 = 3.3V	35	mΩ
SW Leakage Current – NMOS	V_{IN_B2} = 5V, V_{SW} = 5V	2	µA
SW Leakage Current – PMOS	V_{IN_B2} = 5V, V_{SW} = 0V	3.5	µA
Dynamic Voltage Scaling Rate	B2_SLEW=00 B2_SLEW=01 B2_SLEW=10 B2_SLEW=11	22.5 11.25 5.625 2.8125	mV/µs
Switching Rise / Fall Times	V_{IN_B2} = 5V B2_DRVADJ=00 B2_DRVADJ=01 B2_DRVADJ=10 B2_DRVADJ=11	1.8/1.9 1.6/1.8 1.5/1.6 1.4/1.5	ns
Output Pull Down Resistance	Enabled when regulator disabled VOUT=0.1V	9.40	Ohms

Note1: There are only two balls for VIN_B2 and SW_B2 which is good for 2A average current for lifetime rating.
Note2: T_A = 25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

BUCK3 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B3 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Output Voltage Range	Configured for 100mV steps	0.6		3.7	V
Maximum Output Current (Note1)		1.5			A
Supply Current, Standby	Low Power Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05)		40		µA
	Fixed On-time Mode Enabled Regulator Only, No Load (VOUT = VSET*1.05), IC is in SLEEP or DEEP SLEEP Mode.		10		µA
Supply Current, Shutdown	Regulator Disabled		0.1	2.5	µA
Output Voltage Accuracy – PWM(Note2)	Default output voltage, I_{OUT} = 1A	-1	V_{NOM}	1	%
Output Voltage Accuracy – PWM	Default output voltage, I_{OUT} = 1A	-1.5	V_{NOM}	1.5	%
Output Voltage Accuracy - PFM(Note2)	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1	V_{NOM}	1	%
Output Voltage Accuracy – PFM	Default output voltage, I_{OUT} = 1mA, Average Ripple Voltage	-1.5	V_{NOM}	1.5	%
Line Regulation	Default output voltage, V_{IN_B3} = 3.3V to 5.5V, PWM mode		0.05		%/V
Load Regulation	Default output voltage, PWM Mode		0.05		%/A
Power Good Threshold	V_{OUT_B3} Rising	90.5	93	95.5	$\%V_{NOM}$
Power Good Hysteresis	V_{OUT_B3} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT_B3} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT_B3} Falling		3		$\%V_{NOM}$
Switching Frequency		1.00 2.00	1.125 2.25	1.18 2.36	MHz
Soft-Start Period – Programmable Range	10% to 90% V_{NOM}		250 500		µs
Soft-Start Period	Variation from set point	-40		40	%
Internal High Side Peak Current Limit (Cycle-by-Cycle) ILIMSET	B3_ILIMSET=0 B3_ILIMSET=1		2.0 3.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-20	ILIMSET	+20	%
	At other set points	-25	ILIMSET	+25	%
Internal High Side Peak Current Limit, Shutdown Level	Above ILIMSET = all settings	+10	+25	+40	%
Low Side Peak Current Limit (Cycle-by-Cycle) ILIMSET (Note3)	B3_ILIMSET=0 B3_ILIMSET=1		2.0 3.0		A

PMOS On-Resistance	I_{SW} = -500mA, VIN_B3 = 3.3V	100	mΩ
NMOS On-Resistance	I_{SW} = 500mA, VIN_B3 = 3.3V	75	mΩ
SW Leakage Current – NMOS	V_{IN_B3} = 5V, V_{SW} = 5V	1	µA
SW Leakage Current – PMOS	V_{IN_B3} = 5V, V_{SW} = 0V	2.5	µA
Switching Rise / Fall Times	V_{IN_B3} = 5V B3_DRVADJ=00 B3_DRVADJ=01 B3_DRVADJ=10 B3_DRVADJ=11	1.8/1.9 1.6/1.6 1.5/1.5 1.4/1.4	ns
Output Pull Down Resistance	Enabled when regulator disabled VOUT=0.1V	9.40	Ohms

Note1: There are only two balls for VIN_B2 and SW_B2 which is good for 2A average current for lifetime rating.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection. It is only enabled when the top FET on-time is less than 120ns.

LDO1 ELECTRICAL CHARACTERISTICS

(VIN_LDO1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.62		5.5	V
Output Voltage Range	Configurable in 50mV steps	0.6		3.75	V
Output Current	VIN_LDO1 = 1.62V to 5.5V, ILIM_SCL_LDO1=1	0.3			A
Output Voltage Accuracy (Note1)	At default output voltage setting V_{IN_LDO} - V_{LDO1} > 0.4V	-1	V_{NOM}	1	%
Output Voltage Accuracy	At default output voltage setting V_{IN_LDO} - V_{LDO1} > 0.4V	1.5	V_{NOM}	1.5	%
Line Regulation	V_{IN_LDO} - V_{LDO1} > 0.4V V_{IN_LDO} = 3V to 5V I_{LDO1} = 1mA		0.05		% / V
Load Regulation	I_{LDO1} = 1mA to 300mA V_{IN_LDO} - V_{LDO1} > 0.4V		0.02		% / A
Supply Current	Regulator Enabled No Load		14	30	µA
	Regulator Disabled		0	1	µA
Soft-Start Period	SST_LDO1 = 0. V_{LDO1} = 10% to 90% SST_LDO1 = 1. V_{LDO1} = 10% to 90%		160 320		µs
Power Good Threshold	V_{LDO1} Rising	90.5	93	95.5	%V_{NOM}
Power Good Hysteresis	V_{LDO1} Falling		3		%V_{NOM}
Overvoltage Fault Threshold	V_{LDO1} Rising	107.5	110	112.5	%V_{NOM}
Overvoltage Fault Hysteresis	V_{LDO1} Falling		3		%V_{NOM}
Discharge Resistance	Enabled when regulator disabled	10	20	35	Ω
Dropout Voltage	I_{LDO1} = 200mA, V_{IN_LDO} > 2.7V, LDO1_ILIM=0			200	mV
	I_{LDO1} = 400mA, V_{IN_LDO} > 2.7V, LDO1_ILIM=1			400	mV
Output Current Limit	V_{IN_LDO} = 2.7V to 5.5V, V_{IN_LDO} - V_{LDO1} > 0.4V ILIM_SCL_LDO1=0 ILIM_SCL_LDO1=1	310 410			mA
Short Output Foldback Current			35		%

Note1: T_A = 25°C

LDO1 ELECTRICAL CHARACTERISTICS – LOAD SWITCH

(VIN_LDO1 = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	AVIN	2.7	3.3	5.5	V
Load Switch Operation Range	NLSW Mode, Input Voltage Range of LDO1_IN	0.4		Minimum of (AVIN-1 or 3.6V)	V
	PLSW Mode, Input Voltage Range of LDO1_IN	1.62		AVIN	V
Load Switch On-Resistance	NLSW Mode, V_{LDO1_IN} = 0.4V I_{LDO1} = 100mA		55		mΩ
	NLSW Mode, V_{LDO1_IN} = 3.3V I_{LDO1} = 100mA		310		mΩ
	PLSW Mode, V_{LDO1_IN} = 3.3V I_{LDO1} = 100mA		380		mΩ
Load Switch Supply Current (each load switch)	NLSW Mode. Load Switch Enabled. No Load		16		µA
	PLSW Mode. Load Switch Enabled. No Load		20		
	Load Switch Disabled		0	1	
Soft-Start Period	NLSW Mode		200		µs
	PLSW Mode. Load Switch Uses Current Limit to accomplish softstart		N/A		
Output Current Limit	NLSW Mode: NLSW1_ILIM_SCL = 0 NLSW Mode: NLSW1_ILIM_SCL = 1 PLSW Mode: ILIM_SCL_LDO1 = 0 PLSW Mode: ILIM_SCL_LDO1 = 1	0.52 0.85 0.31 0.41	0.65 1.1 0.33 0.48		mA

LDO2 ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.62		5.5	V
Output Voltage Range	Configurable in 50mV steps	0.6		3.75	V
Output Current	AVIN = 1.62V to 5.5V, ILIM_SCL_LDO2=1	0.3			A
Output Voltage Accuracy (Note1)	At default output voltage setting AVIN - V_{LDO2_OUT} > 0.4V	-1	V_{SET}	1	%
Output Voltage Accuracy	At default output voltage setting AVIN - V_{LDO2_OUT} > 0.4V	-1.5	V_{SET}	1.5	%
Line Regulation	AVIN - V_{LDO2_OUT} > 0.4V AVIN = 2.7V to 5.5V I_{LDO2_OUT} = 1mA		0.007		% / V
Load Regulation	I_{LDO2_OUT} = 1mA to 100mA, LDO2_ILIM=1X		-1		% / A
Supply Current (each LDO output)	Regulator Enabled, No Load		15		µA
	Regulator Disabled		0	1	µA
Soft-Start Period	SST_LDO2 = 0. V_{LDO1} = 10% to 90% SST_LDO2 = 1. V_{LDO1} = 10% to 90%		160 320		µs
Power Good Threshold	V_{LDO2_OUT} Rising	90.5	93	95.5	$\%V_{NOM}$
Power Good Hysteresis	V_{LDO2_OUT} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{LDO2_OUT} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{LDO2_OUT} Falling		3		$\%V_{NOM}$
Dropout	ILDO2_OUT = 150mA AVIN > 2.7V LDO2_ILIM=11			200	mV
Discharge Resistance	Enabled when regulator disabled	10	20	35	Ω
Output Current Limit	AVIN = 1.62V to 5.5V, AVIN - V_{LDO2} > 0.4V ILIM_SCL_LDO2=0 ILIM_SCL_LDO2=1	310 410	400 500	450 600	mA

Note1: T_A = 25°C

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	AVIN = 3.3V			0.4	V
SCL, SDA Input High	AVIN = 3.3V	1.25			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Fall Time SDA, T_{of}	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I²C timings for 1MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering RESET, IDLE, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

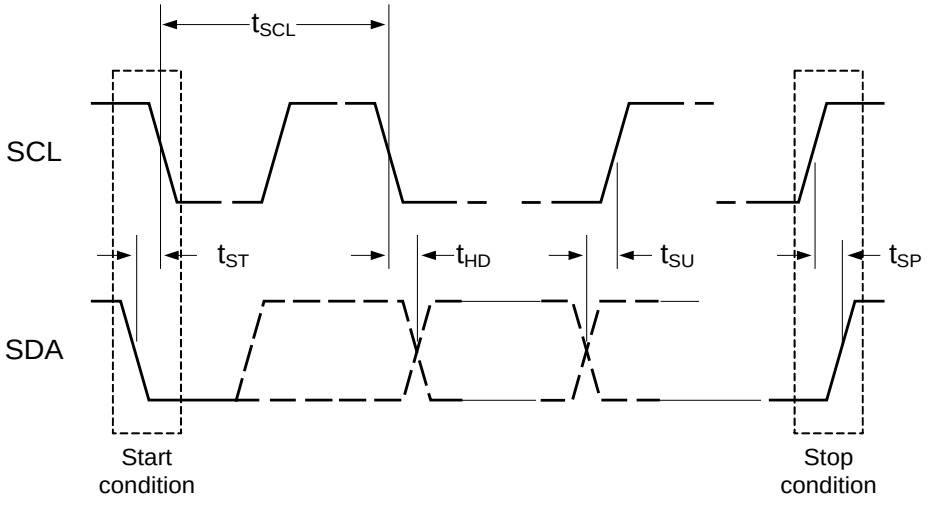


Figure 2: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT88327 is a single-chip integrated power management solution designed to power many processors. It integrates three highly efficient buck regulators, and two LDOs. Its high integration and high switching frequency result in an extremely small footprint and low-cost power solution. It contains a master controller that manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes. The built-in load bypass switch enables full sequencing configurability in 3.3V systems.

The ACT88327 master controller monitors all outputs and reports faults via I²C and hardwired status signals. Faults can be masked, and fault levels and responses are configurable via I²C.

Many of the ACT88327 GPIOs and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. The first part of the datasheet describes basic IC functionality and default pin functions. The last section of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@qorvo.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88327 uses standard I²C commands. The ACT88327 always operates as a slave device and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pullup resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

Table 1: ACT88327 I²C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h

I2C Registers

The ACT88327 has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please contact Qorvo for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

The ACT88327 contains an internal state machine with five internal states.

RESET State

In the RESET, or "cold" state, the ACT88327 is waiting for the input voltage on AVIN to be within a valid range defined by the UVLO and VIN_OV thresholds. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to POWER SEQUENCE START when the input voltage enters the valid range. The IC

transitions from any other state to RESET if the input voltage drops below the UVLO threshold voltage. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The outputs are enabled and are starting up in this state. The IC immediately transitions to the POWER ON or SLEEP states when the regulators go into regulation. If a regulator has a fault while powering up, IC will perform hiccup and retry for every 100ms.

POWER ON (Active) State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. The IC only enters the ACTIVE State from the POWER SEQUENCE START State.

SLEEP State

The SLEEP state is a configurable low power state. Based on the system's low power operational requirements, the user can configure the SLEEP state by defining which internal and external regulators are kept on or turned off during the SLEEP state. Each individual regulator output can be programmed to be either on or off in the SLEEP state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state. Buck2 can also be programmed to regulate to its VSET0 voltage, VSET1 voltage (DVS), or be turned off in the SLEEP state. The IC can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. Figure 3 shows how the NVM SLEEP_MODE factory bit sets the I²C and GPIO requirements to enter and exit the SLEEP state.

When the I²C bit SLEEP_MODE = 0, the IC enters SLEEP State with the logical AND of the I²C SLEEP bit and the GPIOs. If more than one GPIO is configured as a SLEEP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the SLEEP State, then only the SLEEP bit controls SLEEP State entry and exit. The IC immediately exits the SLEEP State when the SLEEP bit or a GPIO is deasserted.

When the I²C bit SLEEP_MODE = 1, the IC enters SLEEP State with the logical OR of the I²C SLEEP bit and the GPIOs. If no GPIOs are configured to control the SLEEP state, then only the SLEEP bit controls the SLEEP State. The IC exits SLEEP State when both I²C and GPIO are deasserted.

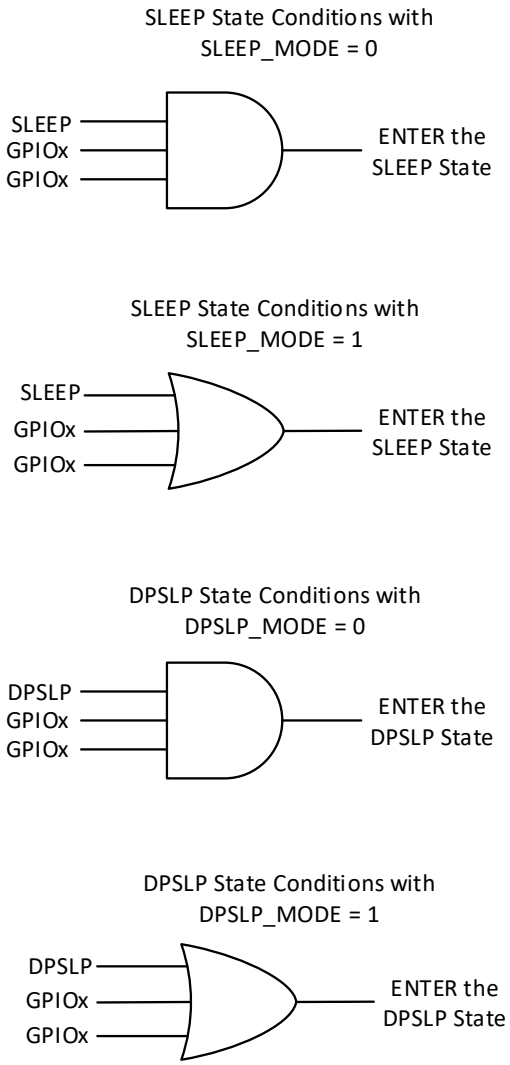


Figure 3. SLEEP and DPSLP State Truth Tables

DPSLP State

The DPSLP State is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP state. It is similar with the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Each output can be programmed to be on or off in the DPSLP state. Buck2 can be programed to operate at its VSET0 voltage, VSET1 voltage, or be turned off. All outputs can be programmed to have different functionality between the SLEEP and DPSLP states. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the DPSLP state. The IC can enter DPSLP state via the I²C register

DPSLP bit or by a GPIOs input. Figure 3 shows how the NVM DPSLP factory bit sets the I²C and GPIO requirements to enter and exit the DPSLP state.

Any GPIO can be configured to control the DPSLP state without requiring any I²C command. This GPIO hardware function is called PWREN. After the DPSLP state is enabled via I²C, the high to low transition on the PWREN input puts the IC in DPSLP state. When the PWREN input is toggled from low to high, the IC exits DPSLP state. PWREN inputs are level triggered and immediately cause the IC to enter or exit the DPSLP state.

Like the SLEEP state, an NVM factory bit DPSLP_MODE sets the logic OR or AND logic between I²C and GPIOs for entering and exiting the DPSLP state.

When DPSLP_MODE = 0, the IC enters DPSLP State with the logical AND of the I²C DPSLP bit and the GPIOs. If more than one GPIO is configured as a DPSLP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the DPSLP State, then only the DPSLP bit controls DPSLP State entry and exit. The IC immediately exits the DPSLP State when the DPSLP bit or a GPIO is deasserted.

GPIOs can also be programmed to individually turn one or multiple outputs on and off. This on/off GPIO functionality in addition to the PWREN functionality provide a wide range of configurability for setting different DPSLP on/off patterns. Note that the GPIOs have four delay time options for both the rising and falling edges. These settings are 0, 1ms, 2.5ms, and 5ms.

For example, in SSD applications, the host can use these GPIO and PWREN to enter different power save modes like PS3.5 and PS4.

In video applications, the GPIOs can be connected to sensor inputs to trigger the IC to exit the DPSLP mode when a sensor input triggers. The GPIO polarity can be programmed as active HIGH or LOW. GPIOs also have a programmable 1ms, 5ms, and 10ms deglitch time.

THERMAL State

In the THERMAL state, the IC has exceeded the thermal shutdown temperature. The IC shuts down all regulators and asserts the nRESET to protect the IC in this condition. The THERMAL state can be disabled by setting register 0x01h bit 4 (TMSK) = 1. Note that thermal shutdown fault bit, TWARN, still provides the thermal status even if TMSK = 1.

OVUVFLT State

In the OVUVFLT state, one of the regulators has exceed an OV level at any time or a UV level after the soft start ramp has completed. In this state, all regulators shutdown and the IC asserts the nRESET pin. After entering the OVUVFLT state, the IC stays there for 100ms and then goes back to the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state, the IC returns to the OVUVFLT state. The cycle continues until the OV or UV fault is removed, or the input power is removed. This state can be disabled by setting an output's OV_FLTMSK or UV_FLTMSK non-volatile bits high. The IC does not directly enter OVUVFLT in an overcurrent condition but does enter this state due to the resulting UV condition.

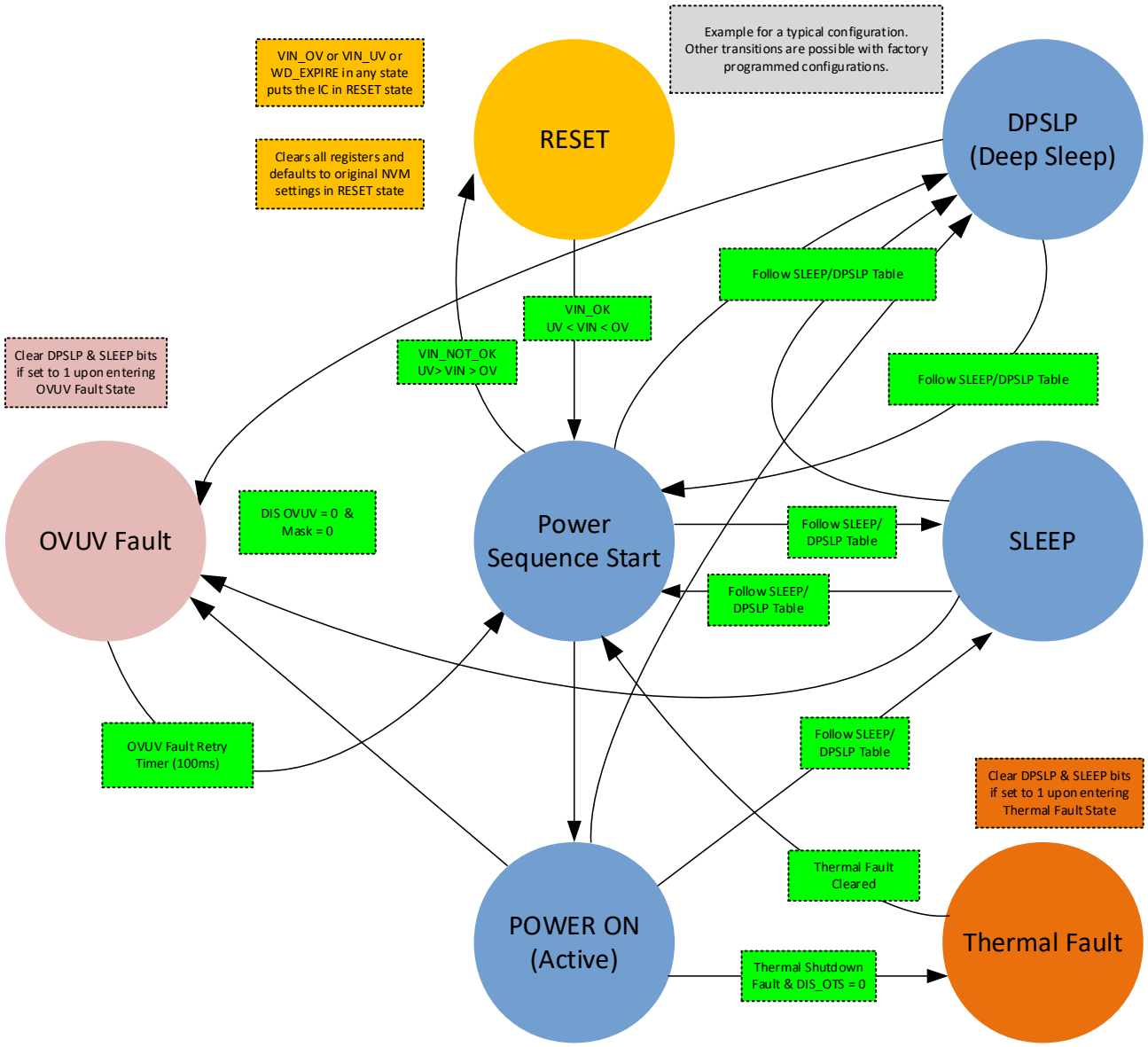


Figure 4: State Machine

Sequencing

The ACT88327 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the five outputs has four basic sequencing parameters: input trigger, turn-on delay, turn-off delay, softstart time, and output voltage. Each of these parameters is controlled via the ICs internal registers. Contact Qorvo for custom sequencing configurations. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Turn on and Turn off Options. The ACT88327 provides several options for enabling the IC. These include automatic power up when input power is applied as well as power up with a digital input signal to a GPIO. The GPIO can be configured to latch the IC on with an input pulse or to be level triggered. Once powered on, the IC can be turned off with either the GPIO or an I²C command.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to a GPIO. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with another external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can be changed with a custom CMI configuration. The nRESET, POK, PG, and EXT_EN outputs can be connected to a power supply's internal POK signal and used to trigger external supplies in the overall sequencing scheme.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ON_DELAY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between the input trigger for SLEEP or DPSLP Mode being asserted and when each output starts to turn off. Each output's turn-off delay is configured via its I²C bit OFF_DELAY. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 10% to 90% to its programmed voltage. Each output's softstart time is configured separately via its I²C bit SST. Softstart times can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Output Voltage. Each buck's output voltage is programmed via its I²C bits Bx_VSET0 and Bx_VSET1. Buck2 regulates to its B2_VSET0 voltage in ACTIVE mode. It can be programmed to regulate to B2_VSET1 in DVS mode, SLEEP state, or by a GPIO input. Buck2 can change between B2_VSET0 and B2_VSET1 on-the-fly. Buck1/3 cannot change between Bx_VSET0 and Bx_SET1 on-the-fly. Typically, Buck1/3 operate at the Bx_VSET0 voltage. If a system requires two different voltage options, a GPIO can be programmed as a voltage pinstrap input. The pinstrap input must be set before the output is enabled. The pinstrap input cannot be changed while the converter is running. If the input is a logic L, Buck1/3 operates from Bx_VSET0 and if the input is a logic H, Buck1/3 operate from VSET1. This polarity can be reversed. The LDOs only have a single register, LDOx_VSET, to set their output voltage.

Each output's Bx_VSET0 and Bx_VSET1 voltage can be changed via I²C after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. All bucks and LDO output voltages can be changed on-the-fly by writing a new value into their I²C registers. The Buck1 and Buck3 output voltage should only be changed by the minimum step size for each I²C write. The Buck2, LDO1, and LDO2 output voltages can be changed with larger step sizes, but Qorvo recommends minimizing the step size change to prevent the IC from detecting an instantaneous over or under voltage condition due to fault thresholds being immediately changed, but output voltage taking time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for Buck2 is available via the I²C interface. Note that Buck1/3 output voltage cannot be changed on-the-fly. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit

setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

The IC can be configured to enter DVS by I²C, by a GPIO pin, or by entering SLEEP/DPSLP mode. Entering DVS via I²C requires that the factory bit EN_DVS_BY_I2C be set to 1. To enter DVS, change I²C bit DVS_FROM_I2C from 000 to a different value. The required value is CMI specific. Entering DVS by a GPIO pin or when entering SLEEP/DPSLP are also CMI dependent, so contact Qorvo for details if this is required.

Input Voltage Monitoring (SYSMON)

The ACT88327 monitors the input voltage on the AVIN pin to ensure it is within specified limits for system level operation. The IC "wakes up" and allows I²C communication when AVIN rises above the UVLO threshold. UVLO can be set to either 2.6V or 3.5V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable. However, the outputs do not turn on until AVIN rises above the SYSMON threshold. SYSMON is programmable between 2.7V and 4.8V with 100mV steps. If AVIN drops below the SYSMON threshold the outputs continue to operate normally as long as AVIN is still above UVLO. A GPIO can be programmed to output an active low SYSMON signal so the host can use it for system control purposes. In the meantime, the IC asserts the nIRQ interrupt when AVIN < SYSMON. The nIRQ interrupt can be masked by an NVM register bit. The SYSMON signal output is a real-time signal. The IC also has a real-time status bit, SYSDAT, that follows the internal SYSMON signal. Note that the nIRQ output is latched until the SYSSTAT bit in register 0x00h is read via I²C. Figure 5 shows the SYSMON details.

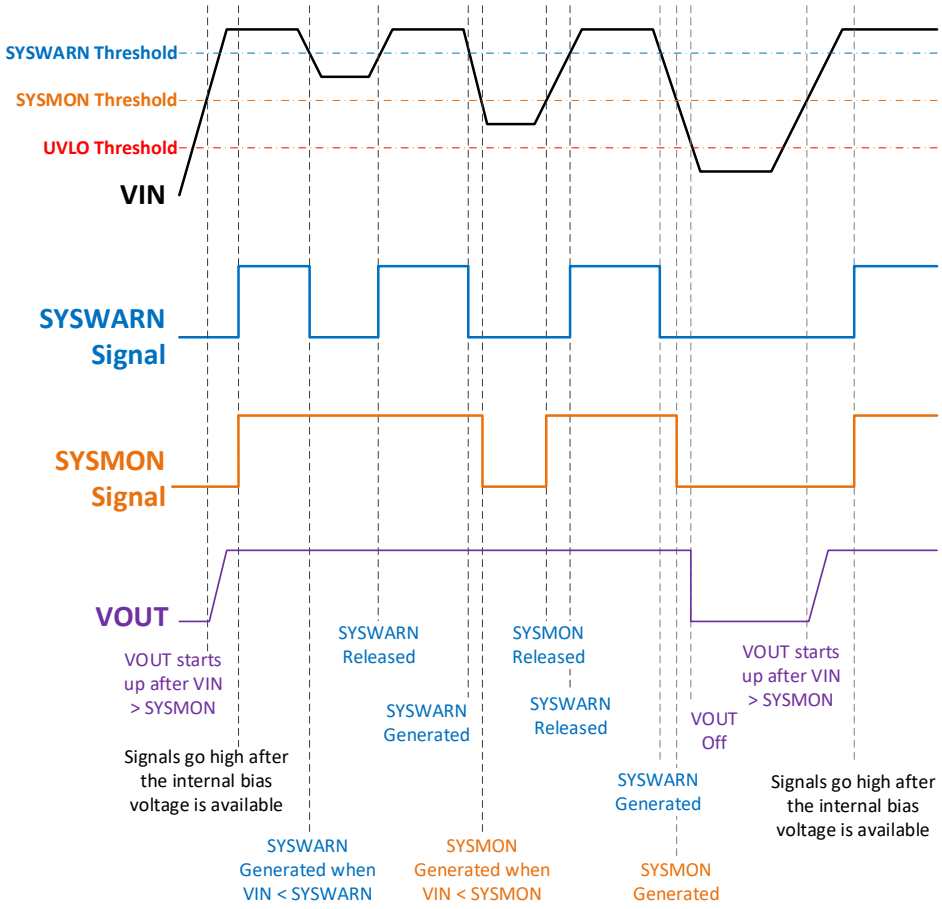


Figure 5: SYSMON and SYSWARN Signals

Input Voltage Warning (SYSWARN)

The ACT88327 also has a second level of input voltage monitoring, SYSWARN. SYSWARN provides another level of low input voltage warning to the host. It is programmable between 2.7V and 5.7V with 100mV steps by the SYSWARN bits. A GPIO can be programmed to output an active low SYSWARN signal so the host can use it for system control purposes. In the meantime, the IC asserts the nIRQ interrupt when VIN < SYSWARN. The nIRQ interrupt can be masked in the NVM register bit. The SYSWARN signal output is a real-time signal. The IC also has a real-time status bit, SYSWARN, that follows the internal SYSWARN signal. Note that the nIRQ output is latched until the SYSWARN bit in register 0x00h is read via I^{2}C.

Fault Protection

The ACT88327 contains several levels of fault protection, including the following:

Output Overvoltage

Output Undervoltage

Output Current Limit and Short Circuit

Thermal Warning

Thermal Shutdown

There are three types of I^{2}C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I^{2}C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only deasserts after the fault condition is no longer present and the corresponding fault bit is read via I^{2}C. Note that masked faults can still be read in the fault flag bit. Refer to the Qorvo Application Note describing the Register Map for full details on I^{2}C functionality and programming ranges.

Input Voltage UVLO

The ACT88327 monitors its input voltage at the AVIN pin for a UVLO condition. When the input voltage is below the UVLO threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I^{2}C functionality is not enabled until AVIN goes above the UVLO threshold. When the input voltage goes above UVLO, the IC transitions to the ACTIVE state and starts up normally. The UVLO threshold can be set to either 2.6V or 3.5V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable.

Input Voltage OV

The ACT88327 monitors its input voltage at the AVIN pin for an OV condition. There are two overvoltage levels, POK_OV and VIN_OV. The first level is set by the POK_OV register, which is programmable between 3.5V and 5.6V. When AVIN goes above the POK_OV threshold, an interrupt is generated on the nIRQ output, but all outputs stay on. If VIN_POK_OV_MASK = 0, the VIN_POK_OV register provides real-time status if. If it = 1, then VIN_POK_OV register is latched until read by I^{2}C. The second level, VIN_OV, is programmable between 3.7V and 5.81V. When the input voltage is above the VIN_OV threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I^{2}C functionality is still enabled while AVIN is above the VIN_OV threshold. When the input voltage goes below the VIN_OV threshold, the IC transitions back to the Power Sequence Start State and starts up normally.

Output Under/Over Voltage

The ACT88327 monitors the output voltages for under voltage and over voltage conditions. If one output enters an UV/OV fault condition, the IC enters the OVUV Fault State and shuts down all outputs for 100ms. It then enters the POWER START SEQUENCE State and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit. Each output still provides its real-time UV/OV fault status via its fault flag, even if the fault is masked. Masking an OV/UV fault just prevents the fault from being reported via the nIRQ pin. A UV/OV fault condition pulls the nRESET pins low. Note that then nRESET and nIRQ pins are configurable via CMI settings

Output Current Limit

The ACT88327 incorporates a three-level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 80% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. This may or may not

turn off that output or other outputs depending on the specific CMI. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies off for 100ms and restarts. The third level is when the peak switch current reaches 120% of the Cycle-by-Cycle current limit threshold. This immediately shuts down the regulator and waits 14ms before restarting.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for each output are adjustable via I²C. Overcurrent fault reporting can be masked via I²C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT88327 monitors its internal die temperature and reports a warning via nIRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 155 deg C. A temperature fault moves the state machine to the Thermal Fault State and shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I²C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin.

PWREN

PWREN is a digital input that helps determine if the IC operates in POWER ON mode or DPSLP mode. Refer to the DPSLP State section for details. PWREN has a bidirectional filter to prevent noise from triggering this function. The PWREN signal must be longer than 120µs to enter or exit DPSLP mode.

When PWREN is pulled low, the Buck2 can be configured to stay on, turn off, or regulate to a different voltage set by I²C register VSET1. Buck1/3 and the LDOs can be configured to either stay on or turn off. This feature provides the system with a single digital input to reconfigure the outputs for a system level low power mode.

nIRQ

The ACT88327 interrupt pin informs the host of any unmasked IC faults. In general, anything with a status change asserts the nIRQ pin. The status changes can be masked by set the corresponding register bits. If interrupt bit is set, the fault must be read before it clears the interrupt bit. If the fault remains the interrupt bit remains set.

The following status changes assert nIRQ:

- Input over-voltage, under-voltage
- Input voltage drops below SYSMON
- Input voltage drops below SYSWARN
- Thermal warning, thermal shutdown
- Buck operation faults
- Buck under-voltage shutdown
- Any buck regulator exceeding peak current limit for 16 cycles after soft start or a UV/OV condition.
- Any regulator exceeding current limit for more than 20uS after soft start or a UV/OV condition.
- Watch Dog timer expiring.
- GPIOs wake up mode high to low transition
- Enter ROM mode
- nIRQ can be re-configured to any GPIO pin.

nRESET

The nRESET pin is an open drain 5V compatible output used to issue the main reset to the system's CPU/controller. The output monitors the input voltage and valid regulator outputs to trigger a reset if the input voltage or regulator output voltages are not valid. The nRESET delay time is controlled by the TRST_DLY control bits. The delay time is programmable from 0.5ms to 100ms. nRESET is essentially the same as a Power Good (PG) function but with a fixed delay after all the supply rails go into regulation.

The nRESET output signal is typically tied to all regulators outputs that are necessary for the system controller and I/Os to function properly. Each regulator has a register bit that determines if that regulator's POK signal is

used as an input to the nRESET output signal. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs is not okay, the nRESET output will be asserted low. Any disabled regulator does not affect the nRESET signal, even if that regulator's POK signal is configured as an input to the nRESET output. This prevents a regulator's POK signal from triggering nRESET when the regulator is commanded by the user to turn off. A regulator's POK signal is typically low only from the time when it is enabled (enable to the regulator goes high) to the time when the output reaches 90% or higher of the final output voltage. nRESET can be reconfigured to any GPIO pin.

EXT_EN

The EXT_EN is a GPIO output function that is used to enable an external power supply. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_EN output can be triggered by one of the regulator's POK signals. It can be programmed with a 0, 1, 5, or 10ms delay time using the GPIOx's I^2C bits IOx_DLY in registers 0x0Bh and 0x0Ch.

EXT_PG

The EXT_PG is a GPIO input function that is used to determine that an external power supply has turned on and its output voltage is in regulation. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_PG output can be used as an input trigger to turn on one of the ACT88327 regulators.

POK

Any regulator's internal POK bit can be connected to a GPIO to provide an external POK signal. The POK function indicates that a regulator's output voltage is in regulation.

ROM Mode

In SSD applications, there is a chance the firmware, which is stored in the flash, is not loaded properly. In this situation, the SSD fails to startup and work properly. The SSD core must be put back into ROM mode to attempt a restart. In some systems, this requires recycling power, removing and reinserting the SSD card, or manually shorting pins on the SSD module.

ACT88327 includes a ROM Mode feature that significantly simplifies this process at a system level. The ACT88327 ROM Mode forces the SSD core to stay in its ROM state if it does not power up properly.

Figure 6 shows how ROM Mode is implemented. One GPIO is configured as the input for the ISP Ready signal, which is an output from the SSD core after the system powers up. Another GPIO is configured as output for the ROM state signal. After the ACT88327 startup sequence completes, the ACT88327 asserts its nRESET output and an internal watchdog timer starts monitoring the ISP Ready input signal (active high) to make sure system powers up successfully. If the ISP Ready input is not asserted within 7s (configurable between 7s and or 20s), the ACT88327 starts the ROM mode. It turns off all regulator outputs, asserts nRESET low, and asserts the ROM_Only signal low. After a 100ms (configurable between 100ms and 250ms) delay, the ACT88327 restarts the power up sequence. The ROM_Only output stays asserted low until nRESET is de-asserted high to make sure the SSD core stays in the ROM state when powered up.

ROM mode is only activated after after nRESET is de-asserted. I^2C bit NVM ROM_EN enables ROM mode. If the SSD driver needs to enter a power save mode before the 7s watchdog timer expires, the host needs to disable ROM mode before entering the power save mode to avoid the potential risk of activating the ROM_Only and nRESET outputs.

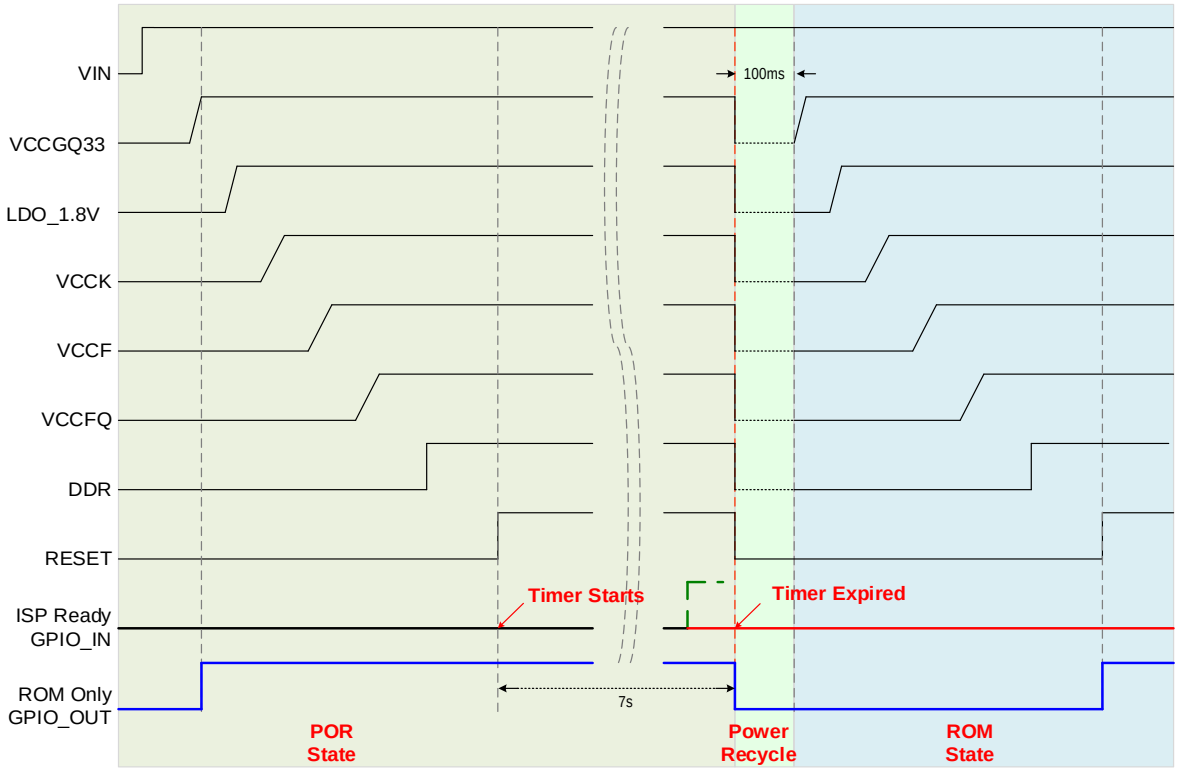


Figure 6: ROM State

GPIO Wake up Mode

All GPIOs can be configured to force the IC into and out of DPSLP mode. Any number of GPIOs can be configured for this functionality. Please see in DPSLP State section for details.

Pin Descriptions

The ACT88327 input and output pins are configurable via CMI configurations. The following descriptions refer to the basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

VIN_Bx

VIN_Bx pins are the dedicated input power pins to the buck converters. Each buck converter must be bypassed directly to its PGNDx pin on the top PCB layer with a high-quality ceramic capacitor. Refer to the Step-down DC/DC Converters section for more details.

AVIN

AVIN is the input power to LDO2. It also powers the IC's analog circuitry. AVIN must be bypassed directly to AGND on the top PCB layer with a 1uF ceramic capacitor.

VIN_LDO

This is the dedicated input power to the LDO1. VIN_LDO must be bypassed directly to AGND on the top PCB layer with a 1uF ceramic capacitor.

GPIOx

The ACT88327 has 7 GPIO pins. The GPIOs allow a variety of functions to be implemented. They can be used as inputs or open drain outputs. Their polarity can also be changed. These options allow implementation of a variety of system functions and also allow flexibility of functions tied to each pin. Examples of system functions that can be implemented are nRESET, Power Good (PG) output, interrupt request or interrupt pin (nIRQ), digital output from power okay (POK) signal from individual regulators, digital outputs to control external regulators (EXT_EN), digital input lines to monitor power good signals from external regulators (EXT_PG), digital input to control power sequencing or regulator ON/Off, control input used to enter or exit sleep (SLEEP) and deep sleep (DPSLP) modes, inputs to control Dynamic Voltage Scaling (DVS) in the Buck regulators,

and outputs for the SYSMON and SYMWARN functions. Are all GPIOs are 5V compliant and can be pulled to 5V regardless of their bias supply.

SCL, SDA

These are the I^2C clock and data pins to the IC. They have standard I^2C functionality.

PGNDx

The PGNDx pins are the buck converter power ground pins. They connect directly to the buck converters' low side FETs.

SW_Bx

SWx are the switch nodes for the buck converters. They connect directly to the buck inductor on the top layer.

FB_Bx

These are the feedback pins for the buck regulators. They should be kelvin connected to the buck output capacitors.

LDOx

These are the LDO output pins. Each LDO output must be bypassed to AGND with a 1uF capacitor.

AGND

AGND is the ground pin for the IC's analog circuitry and LDOs. AGND must be connected to the IC's PGNDx pins. The connection between AGND and the PGNDx pins should not have high currents flowing through it.

Step-down DC/DC Converters

General Description

The ACT88327 contains four fully integrated step-down converters. Buck1/2 are 3A max outputs, while Buck3 is 1.5A max output. All buck converters are fixed frequency, current mode controlled, synchronous PWM converters that achieve peak efficiencies of up to 96.5%. The buck converters switch at 1.125MHz or 2.25MHz and are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions.

Each buck converter has a dedicated input pin and power ground pin. Each buck converter must have a dedicated input capacitor that is optimally placed to minimize its power routing loops. Note that even though each buck converter has separate inputs, all buck converter inputs must be connected to the same voltage potential.

Buck1 is configurable as a bypass switch for systems with a 3.3V bus voltage. The bypass switch provides full sequencing capability by allowing the 3.3V bus to be used as the input to the other supplies and still be properly sequenced to the downstream load.

The ACT88327 buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

DVS Slew rate control

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to Qorvo's Register Map Definition application note for full details on I²C functionality and programming ranges.

Operating Mode

By default, all buck converters operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power. Power-save mode reduces conduction losses by preventing the inductor current from going negative.

To further optimize efficiency and reduce power losses at extremely light loads, an additional lower power mode, LPM, is available. LPM minimizes quiescent current in between switching cycles. This reduces input current to approximately 40µA in LPM mode. Light load output voltage ripple increases from approximately 5mV to 10mV when in LPM mode. Light load voltage droop when going from light load to heavier loads is only increased by 2-3mV when in LPM mode. LPM allows the customer to test the IC in their use case and optimize the balance between power consumption, voltage ripple, and transient response in their system. Each buck converter's LPM mode can controlled independently. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM.

ULPM Mode

The ACT88327 incorporates an ultra-low power mode, ULPM, that provides significant efficiency improvements at very light loads. This improvement can be as much as 8% with a 2mA load. ULPM mode reduces the buck converters quiescent current from ~40µA to ~10µA. ULPM mode helps systems like SSDs achieve very low power loss at extremely light loads, which is a requirement in their standby modes. ULPM mode regulates the output voltage between 99% to 101% of the setpoint. When the output voltage increases to 101%, the buck converter shuts down to save quiescent current until the output voltage drops to 99%. It then turns back on and increases the output voltage to 101% again. ULPM mode should only be used when the load current is less than 50mA. With higher load currents, the output voltage drop can trigger UVLO before the converter can react. Using it with greater than 50mA results in much lower efficiencies than standard PWM or LPM mode operation.

If DVS mode is not needed when going into and out of DPSLP mode, program ULPM mode to automatically turn on when the IC enters SLEEP/DPSLP mode. If DVS is needed when going into and out of SLEEP/DPSLP mode, ULPM mode must be manually

enabled after entering SLEEP/DPSLP mode and disabled before leaving SLEEP/DPSLP mode. The following table shows how to configure the IC's ULPM mode.

Table 2: ULPM Mode Configuration

DIS_LPM_ULPM	FORCE_LPM_ULPM	ULPM Mode
0	0	Automatically turns on/off when IC enters/exits SLEEP or DPSLP modes
0	1	Forced on under all conditions
1	X	Disabled

Synchronous Rectification

Buck1/2/3 each feature integrated synchronous rectifiers (or LS FETs) to maximize efficiency and minimize the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, all converters automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C. Each CMI version requires a different set of command to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is enabled via the I²C bit Dis_Pulldown.

Soft-Start

Each buck regulator contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition. Each output softstart time is adjustable to either 250µs or 500µs via their I²C SST registers.

Output Voltage Setting

Buck1/2/3 regulate to the voltage defined by I²C register VSET0 in normal operation and by VSET1 in DVS mode.

For Buck1, the output voltage programming range is 0.6V to 3.775V in 25mV steps.

VBUCK1 = 0.6V + VOUTx * 0.025V

Where VOUTx is the decimal equivalent of the value in I²C VOUTx register. The VOUTx registers contain an unsigned 7-bit binary value.

For Buck2, the output voltage programming range is 0.6V to 1.87V in 10mV steps.

VBUCK2 = 0.6V + VOUTx * 0.01V

For Buck3, the output voltage programming range is 0.6V to 3.7V in 100mV steps.

VBUCK3 = 0.6V + VOUTx * 0.1V

Qorvo recommends that a buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

100% Duty Cycle Operation

The buck regulators can operate at 100% duty cycle. With very low input voltage, the buck converters can operate at 100% duty cycle. The internal power

Dynamic Voltage Scaling

Buck2 supports Dynamic Voltage Scaling (DVS). DVS allows the user to optimize the processor's energy to complete tasks by lowering the processor's operating frequency and input voltage when lower performance is acceptable. In normal operation, each output regulates to the voltage programmed in its I²C register VSET0. During DVS, the output regulates to VSET1. The output transitions from VSET0 to VSET1 at a rate determined by the output capacitance and the load current. The outputs transition between VSET1 and VSET0 by the rate determined by the I²C bits DVS_SET. VSET1 must always be set equal to or lower than VSET0.

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Optimizing Noise

Each buck converter contains several features available via I²C to further optimize functionality. The top P-ch

FET's turn-on timing can be shifted 100ns from the master clock edge via the PHASE_DELAY I²C bit. It can also be aligned to the rising or falling clock edge via the PHASE I²C bit. The internal FET rise and fall times can be optimized to minimize switching noise at the cost of lower efficiency via the DRVADJ I²C bit.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the ILIM_SET I²C bits. If the peak current reaches the programmed threshold for 16 consecutive switching cycles, the IC asserts nIRQ low. A short circuit condition that results in the peak switch current being 122% of the value set by ILIM_SET immediately shuts down all supplies, asserts nIRQ low and restarts the system in 100ms. If a buck converter reaches overcurrent or short circuit protection, the status is reported in the ILIM I²C registers. The contents of these registers are latched until read via I²C. Overcurrent and short circuit conditions can be masked via the I²C bit ILIM_FLTMSK.

After a buck converter starts up (internal POK=1), if its output voltage drops below the POK falling threshold longer than the blanking time (~28µs to 56µs), the converter enters foldback current mode. This reduces the current limit to 1.25A to reduce output voltage overshoot when the load current drops and the converter recovers from the short circuit condition.

When the on-time is less than 120ns, the high side FET overcurrent circuitry will not have enough time to react. The IC includes a low-side current limit setting, LSILIM, to account for this condition. LSILIM can only be enabled with a factory setting. Once LSILIM enabled, the low side FET stays on until the inductor current decays lower than the LSILIM current threshold. The high side FET cannot turn on again until the low side FET current drops below this value. The current threshold is 3.5A when ILIM=0 and 4.5A when ILIM=1. This function also protects the inductor by preventing current runaway which could saturate the inductor. Qorvo does not recommend enabling this function when the steady state duty cycle is greater than 75%.

Compensation

The buck converters utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Minimum On-Time

The ACT88327 minimum on-time is 70ns. If the calculated on-time is less than 70ns with 2.25MHz operation, then the user must configure the output to switch at 1.125MHz. Setting I²C bits HalfFreq = 0 sets Fsw = 2.25MHz. Setting HalfFreq = 1 sets Fsw = 1.125MHz. The following equation calculates the on-time.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Where V_{out} is the output voltage, V_{in} is the input voltage, and F_{SW} is the switching frequency.

BUCK1 Bypass Switch

The ACT88327 provides a bypass mode for 3.3V systems. This allows the 3.3V input voltage to power the ACT88327 regulators and be sequenced to the downstream loads. In bypass mode, the Buck1 P-ch FET acts as a switch and the N-ch FET is disabled. The bypass switch turns on the 3.3V rail with the programmed delay and softstart time.

In bypass mode, the ACT88327 Buck1 I²C registers are reconfigured to the following settings.

1. POK register bit is reconfigured to be the output of the Soft Start ramp. When soft start is complete and the voltage on the SW1 pin reaches VIN_B1-200mV, this bit goes high to allow the sequencing of the other regulators to continue. no longer reports the Buck1 output voltage status.
2. ILIM register bit is reconfigured to be the output of the internal PMOS Current Detection circuit. This is set to 3A typical. If the bypass current exceeds the Internal PMOS Current Detection current, ILIM triggers the nIRQ output and gets latched in the ILIM0 bit if IRQ_nMASK = 1 (not masked). Overcurrent can also be masked with the ILIM_FLTMSK register.
3. POK register bit is reconfigured to the output of the Internal PMOS circuit. The voltage threshold is set to VIN_B1-300mV. If the bypass switch output goes below this value, it triggers

an under-voltage fault condition and moves the IC into the OVUVFLT state. This immediately shuts down all regulators including the bypass switch. The system restarts in 100ms, following the programmed startup sequencing. This fault can be masked with I²C bit UV_nMASK. This fault is latched in the UV_REG I²C bit. Shut-down due to overcurrent can also be masked via the I²C bit B1_PG_FLTMSK.

4. OV register bit is disabled. There is no overvoltage detection circuitry on the output of the bypass switch.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. Note that even though each buck converter has separate input pins, all input pins must be connected to the same voltage potential. 10µF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VIN_Bx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The Buck converters utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. The ACT88327 is optimized for operation with 0.47 to 1 µH inductors. Choose an inductor with a low DC resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where VOUT is the output voltage, VIN is the input voltage, FSW is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The ACT88327 is designed to use small, low ESR, ceramic output capacitors. Buck1/2/3 typically require a 22µF output capacitor. In order to ensure stability, the actual Buck1/2 capacitance must be greater than 15µF while Buck3 must be greater than 10µF. The maximum output capacitance is 100µF. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

LDO CONVERTERS

General Description

The ACT88327 contains two fully integrated low dropout linear regulators (LDO). LDO1 and LDO2 are 300mA outputs. The LDOs are require only two small external components (Cin, Cout) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions. LDO1 can also be configured in load switch mode.

LDO1 has a dedicated input pin, VIN_LDO, so it can operate from different input voltage than the other Buck converters and from LDO2. LDO2 input voltage comes from the AVIN pin.

Enable / Disable Control

When power is applied to the IC, all LDOs automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C or GPIO. Each CMI version requires a different set of commands to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. Each LDO's discharge function is enabled via its I²C bit LDOx_DIS_PLDN.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up in a monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. Each LDO's softstart time is adjustable to either 160µs or 320µs via its I²C bits LDOx_SST.

Output Voltage Setting

LDO1/2 regulate to the voltage defined by I²C registers LDOx_VSET. Unlike the buck converters, the LDOs only have one VSET register. The output voltage programming range is 0.6V to 3.75V in 50mV steps.

V_{LDOx} = 0.6V + LDOx_VSET * 0.05V

Where LDOx_VSET is the decimal equivalent of the value in each regulator's I²C LDOx_VSET register. The LDOxVSET registers contain an unsigned 6-bit binary value. As an example, if LDO 1's LDO1_VSET register contains 011000b (24 decimal), the output voltage is 1.8V.

Qorvo recommends that an LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent and short circuit protection. The overcurrent threshold is set by their I²C bits. The LDO1 current limit is set to 0.35A or 0.45A by the ILIM_SCL_LDO1 I²C bit. The LDO2 current limit is set to 0.35A or 0.45A by the ILIM_SCL_LDO2 I²C bit. Note that the LDO2 bits are only configurable by the factory.

In both an overload and a short circuit condition, the LDO limits the output current which causes the output voltage to drop. This can result in an undervoltage fault in addition to the current limit fault. When the current limiting results in a drop-in output voltage that triggers an undervoltage condition, the IC shuts down all power supplies, asserts nIRQ low, and enters the UVLOFLT state. The IC restarts in 100ms and starts up with default sequencing.

Input Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic input capacitor. A 1uF is typically suitable, but this value can be increased without limit. The input capacitor should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor. For output currents less than 200mA,

1µF capacitor is typically suitable. The minimum allowable capacitance value is 0.7µF. The maximum allowable capacitance is 10µF. For load currents greater than 200mA a 2.2µF capacitor is typically suitable, with a minimum allowable capacitance value of 1.5µF. The output capacitor should be a X5R, X7R, or similar dielectric.

LDO1 Load Switch Mode

LDO1 has the option to be used as a load switch. This option is only accessible via factory I^2C bits and requires a custom CMI. When in load switch mode, LDO1 still retains overcurrent protection. Overvoltage and undervoltage protection are disabled.

In load switch mode, LDO1 has two operating options: NLSW and PLSW modes. In NLSW mode, the load switch is an n-ch FET. NLSW mode is used with an input voltage between 0.4V and AVIN-1V. Due to the lower n-ch FET Rdson, NLSW mode can operate with up to 1A of bypass current while maintaining a low voltage drop. The NLSW current limit is set to 0.65A or 1.11A by the NLSW1_ILIM_SCL I^2C bit.

In PLSW mode, the load switch is a p-ch FET. It can operate with an input voltage between 1.62V and AVIN. The PLSW current limit is set to 0.35A or 0.45A by the ILIM_SCL_LDO1 I^2C bit.

NLSW and PLSW modes can only be fixed at the factory.

NLSW mode has a fixed 200µs softstart time. PLSW mode relies on the current limit setting for softstart.

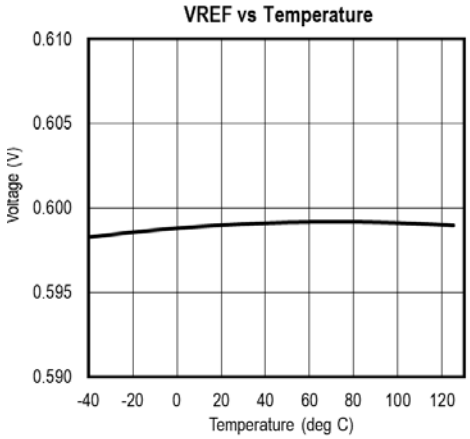
The LDO1 POK is functional in Load Switch mode. The POK signal is asserted when the switch is enabled and is not in current limit.

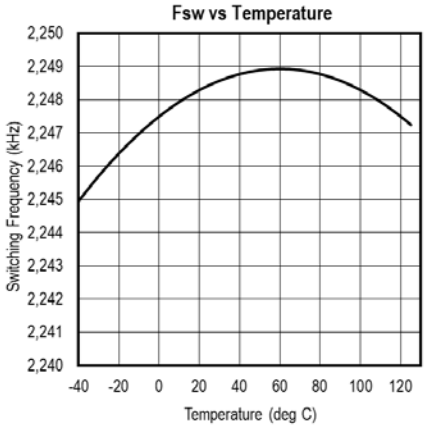
PC Board Layout Guidance

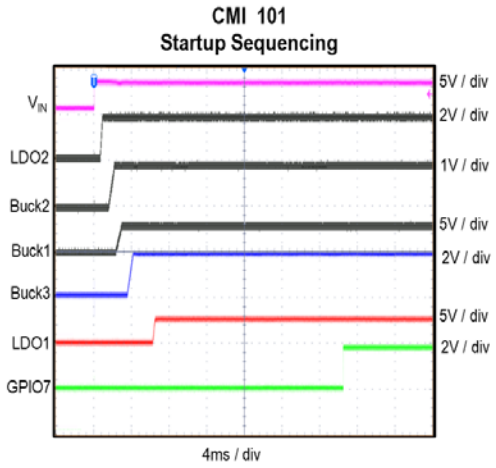
Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT88327 PCB. Refer to the Qorvo ACT88327 Evaluation Kits for layout examples

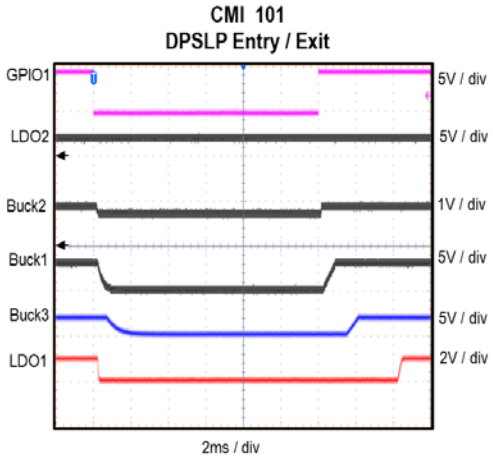
1. Place the buck input capacitors as close as possible to the IC. Connect the capacitors directly to the corresponding VIN_Bx input pin and PGNDx power ground pin. Avoid the use of vias if possible.
2. Minimize the switch node trace length between each SW_Bx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. Place the LDO input capacitors close to their input pins. Connect their ground pins into the ground plane that connects the IC's PGNDx pins.
4. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
5. Connect the PGNDx ground pins and the AGND ground pin directly to the PGND under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
6. Connect the VIN input capacitor to the AGND ground pin.
7. Remember that all open drain outputs need pullup resistors.
8. Connect the PGND directly the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions and are relatively insensitive to layout considerations.

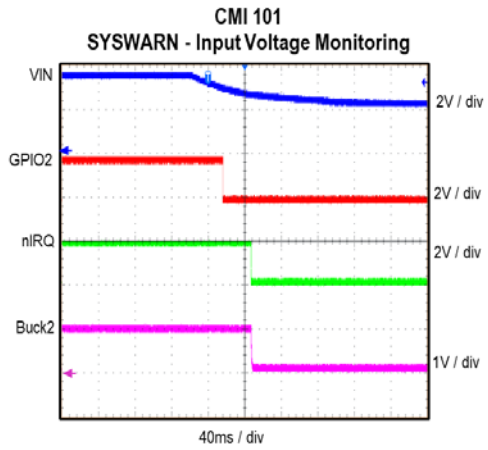
TYPICAL OPERATING CHARACTERISTICS

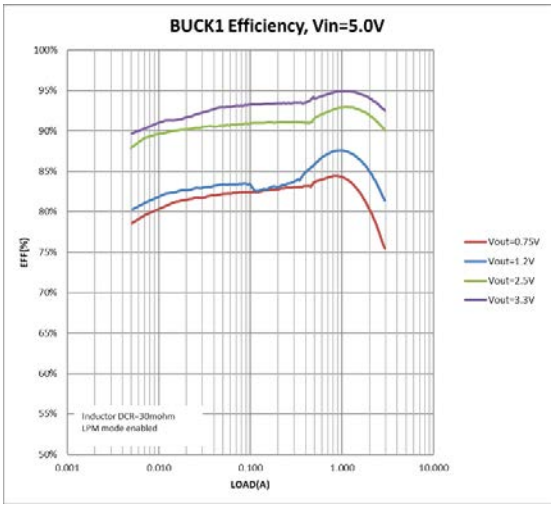


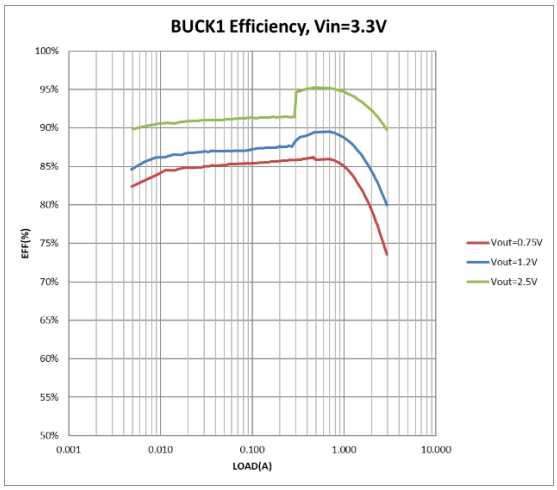


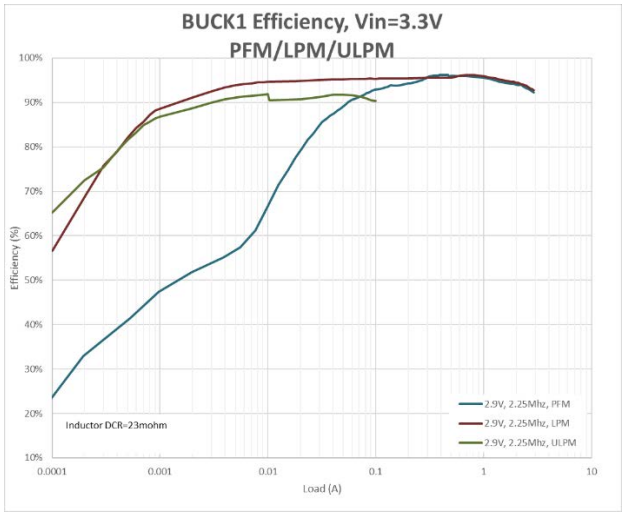


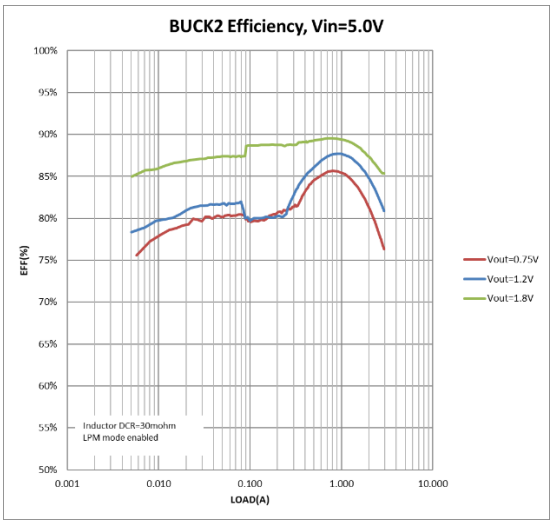


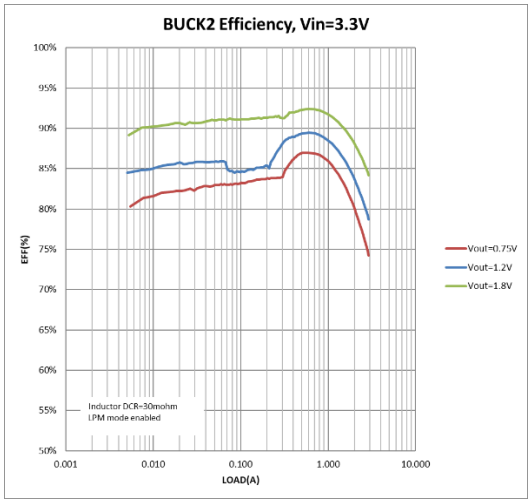


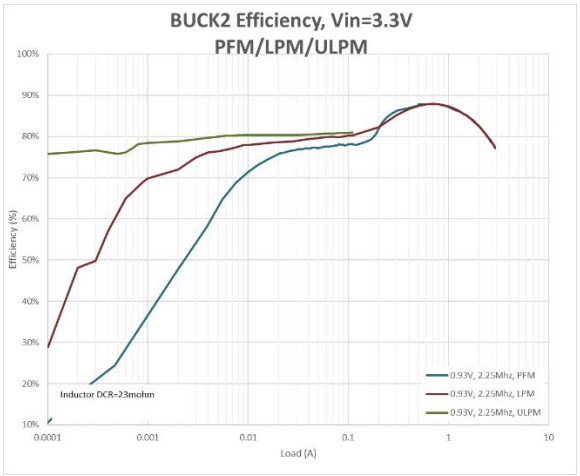


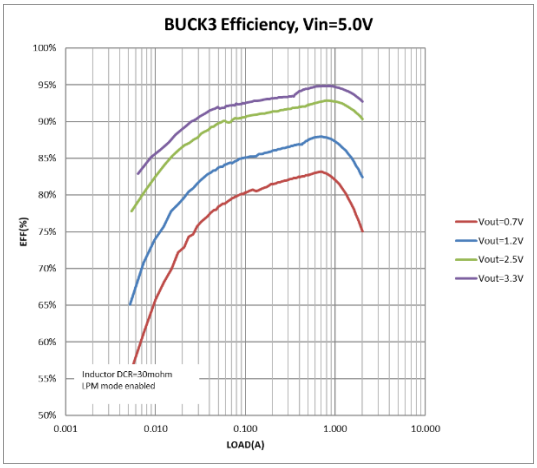

BUCK1 Efficiency, Vin=3.3V
EFF(%)
LOAD(A)
Vout=0.75V
Vout=1.2V
Vout=2.5V

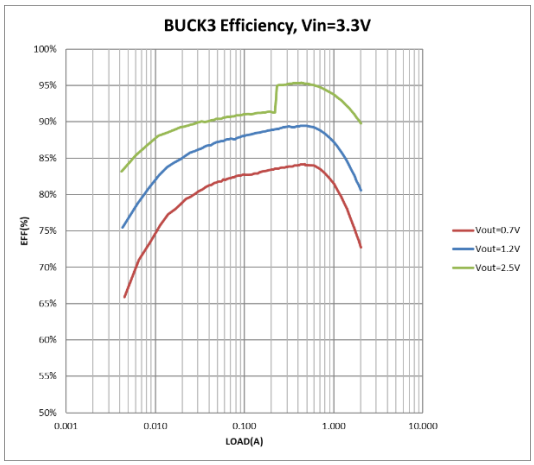

BUCK1 Efficiency, Vin=3.3V
PFM/LPM/ULPM
Efficiency (%)
Load (A)
Inductor DCR=23mohm
2.9V, 2.25Mhz, PFM
2.9V, 2.25Mhz, LPM
2.9V, 2.25Mhz, ULPM

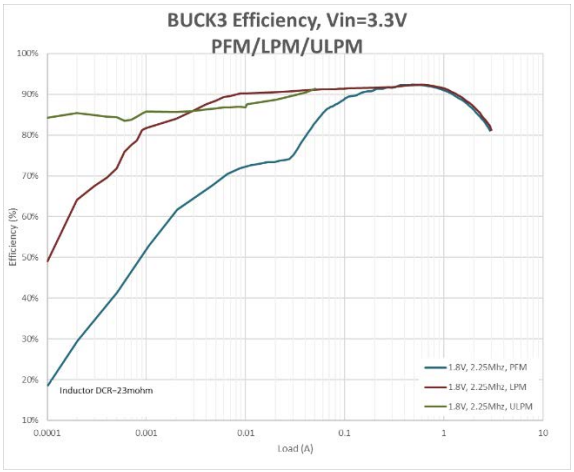

BUCK2 Efficiency, Vin=5.0V
EFF(%)
LOAD(A)
Vout=0.75V
Vout=1.2V
Vout=1.8V
Inductor DCR=30mohm
LPM mode enabled

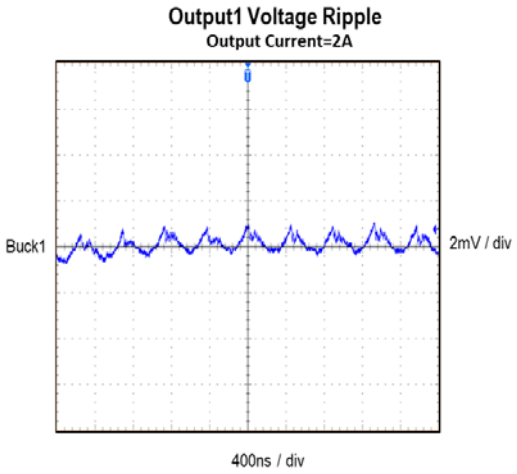

BUCK2 Efficiency, Vin=3.3V
EFF(%)
LOAD(A)
Vout=0.75V
Vout=1.2V
Vout=1.8V
Inductor DCR=30mohm
LPM mode enabled

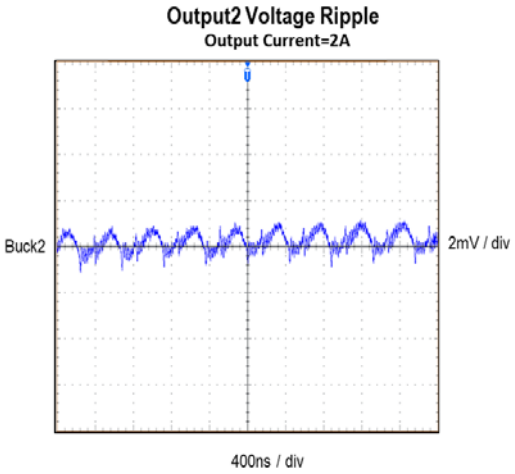

BUCK2 Efficiency, Vin=3.3V
PFM/LPM/ULPM
Efficiency (%)
Load (A)
Inductor DCR=23mohm
0.93V, 2.25Mhz, PFM
0.93V, 2.25Mhz, LPM
0.93V, 2.25Mhz, ULPM

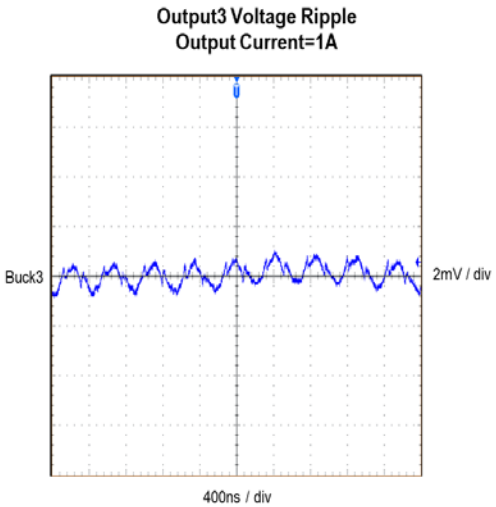

BUCK3 Efficiency, Vin=5.0V
EFF(%)
LOAD(A)
Vout=0.7V
Vout=1.2V
Vout=2.5V
Vout=3.3V
Inductor DCR=30mohm
LPM mode enabled

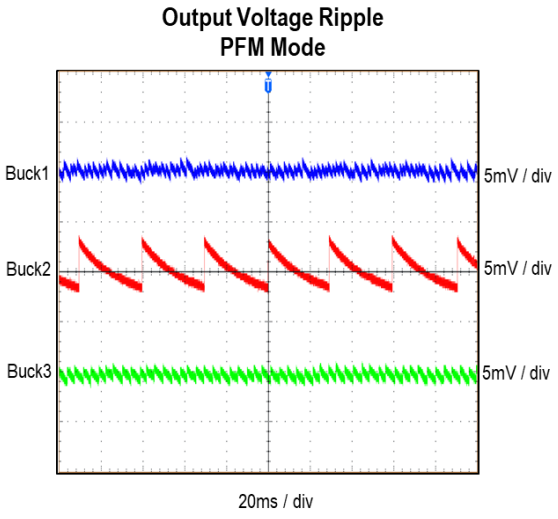

BUCK3 Efficiency, Vin=3.3V
EFF(%)
LOAD(A)
Vout=0.7V
Vout=1.2V
Vout=2.5V

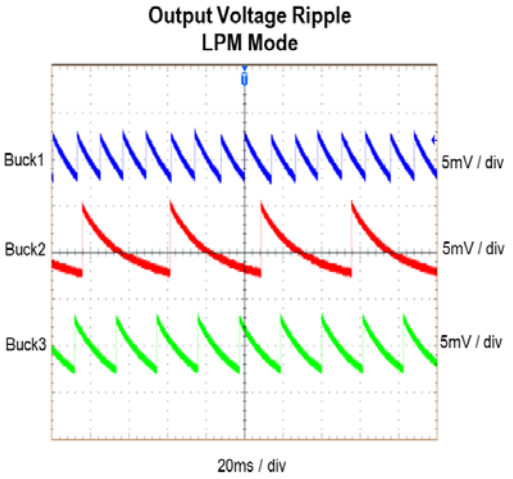

BUCK3 Efficiency, Vin=3.3V
PFM/LPM/ULPM
Efficiency (%)
Load (A)
Inductor DCR=23mohm
1.8V, 2.25Mhz, PFM
1.8V, 2.25Mhz, LPM
1.8V, 2.25Mhz, ULPM

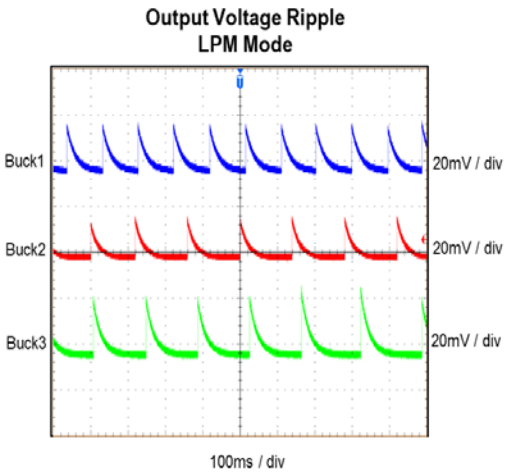

Output1 Voltage Ripple
Output Current=2A
Buck1
2mV / div
400ns / div

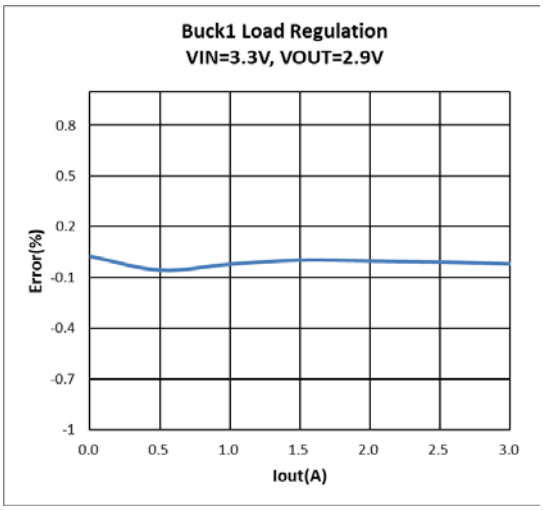

Output2 Voltage Ripple
Output Current=2A
Buck2
2mV / div
400ns / div

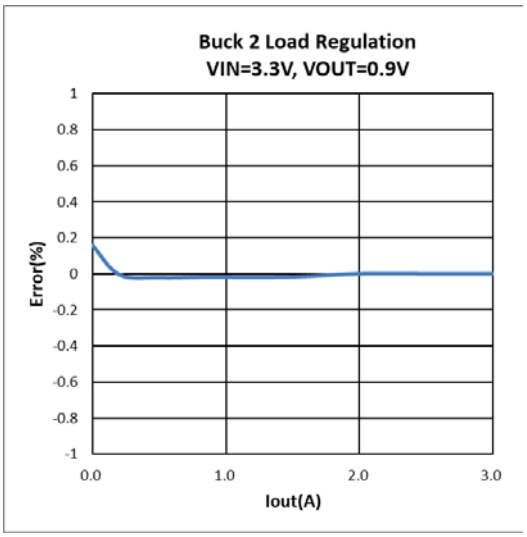

Output3 Voltage Ripple
Output Current=1A
Buck3
2mV / div
400ns / div

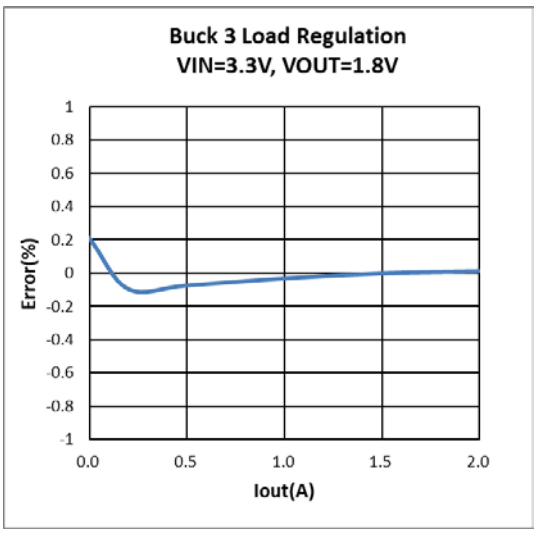

Output Voltage Ripple
PFM Mode
Buck1
5mV / div
Buck2
5mV / div
Buck3
5mV / div
20ms / div

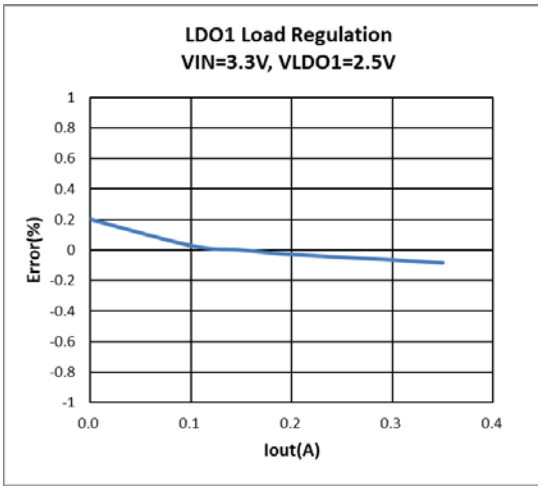

Output Voltage Ripple
LPM Mode
Buck1
Buck2
Buck3
5mV / div
5mV / div
5mV / div
20ms / div

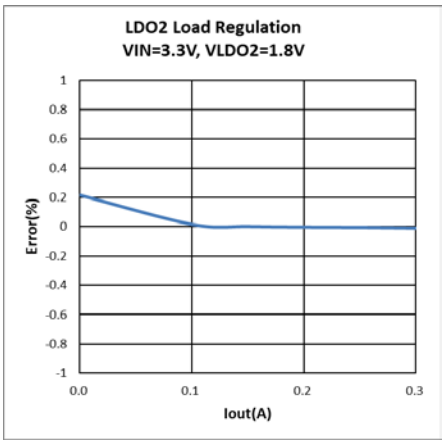

Output Voltage Ripple
LPM Mode
Buck1
Buck2
Buck3
20mV / div
20mV / div
20mV / div
100ms / div

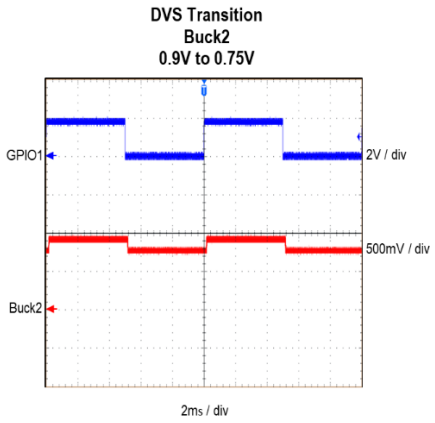

Buck1 Load Regulation
VIN=3.3V, VOUT=2.9V
Error(%)
0.8
0.5
0.2
-0.1
-0.4
-0.7
-1
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Iout(A)

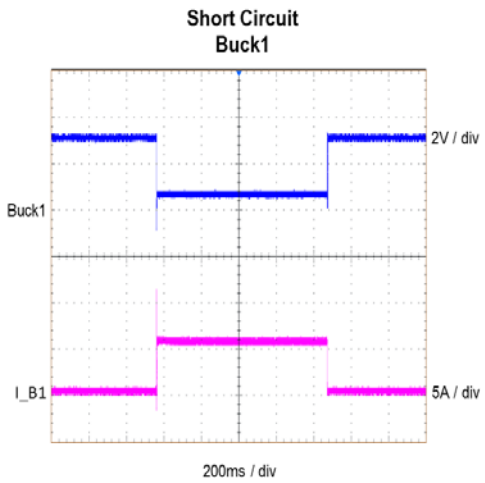

Buck 2 Load Regulation
VIN=3.3V, VOUT=0.9V
Error(%)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0.0
1.0
2.0
3.0
Iout(A)

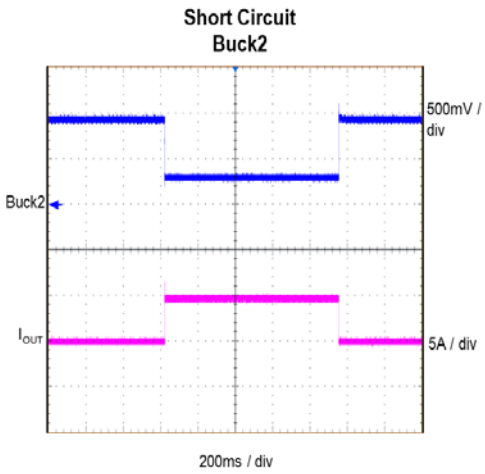

Buck 3 Load Regulation
VIN=3.3V, VOUT=1.8V
Error(%)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0.0
0.5
1.0
1.5
2.0
Iout(A)

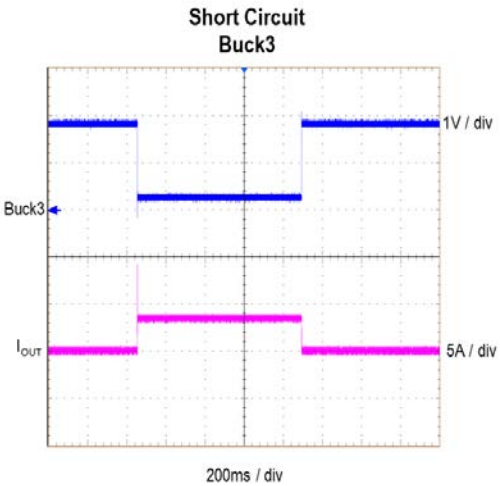

LDO1 Load Regulation
VIN=3.3V, VLDO1=2.5V
Error(%)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0.0
0.1
0.2
0.3
0.4
Iout(A)

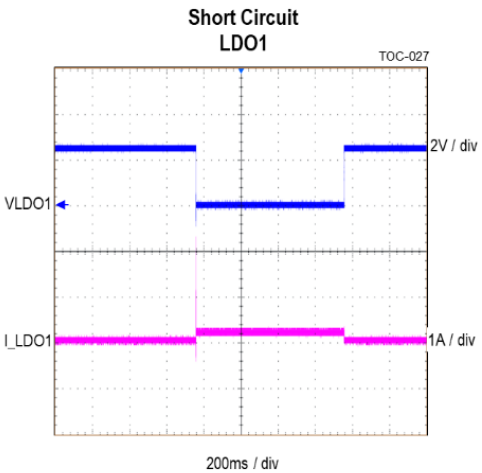

LDO2 Load Regulation
VIN=3.3V, VLDO2=1.8V
Error(%)
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0.0
0.1
0.2
0.3
Iout(A)


DVS Transition
Buck2
0.9V to 0.75V
GPIO1
2V / div
500mV / div
Buck2
2ms / div

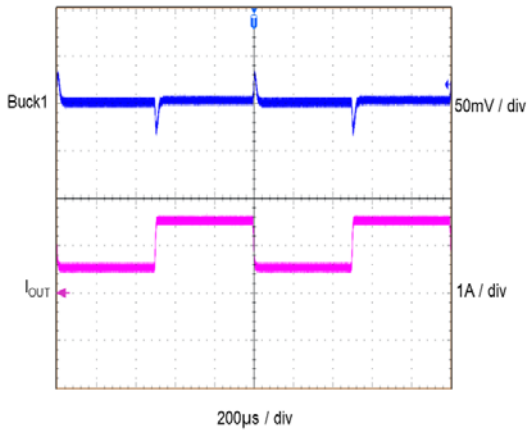

Short Circuit
Buck1
2V / div
Buck1
I_B1
5A / div
200ms / div


Short Circuit
Buck2
500mV / div
Buck2
IOUT
5A / div
200ms / div

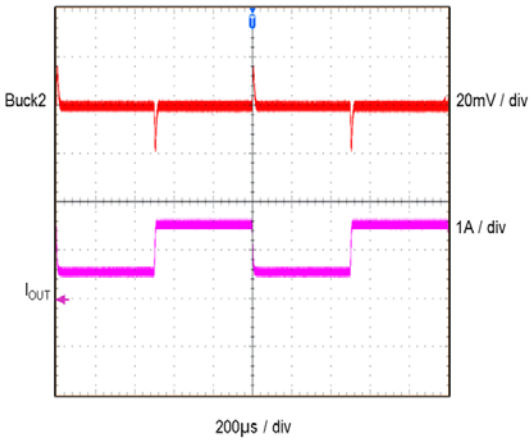

Short Circuit
Buck3
1V / div
Buck3
IOUT
5A / div
200ms / div


Short Circuit
LDO1
TOC-027
2V / div
VLDO1
I_LDO1
1A / div
200ms / div

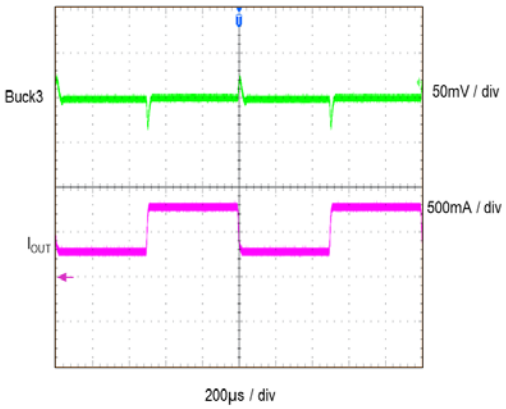
Load Transient
Buck1 Vout=2.9V
500mA to 1500mA



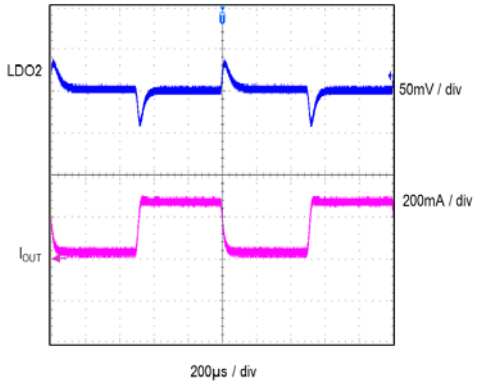
Load Transient
Buck2 Vout=0.9V
500mA to 1500mA



Load Transient
Buck3 Vout=1.8V
250mA to 750mA



Load Transient
LDO2 Vout=1.8V
30mA to 270mA



This section provides the basic default configuration settings for each available ACT88327 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 101: ACT88327VU101-T

CMI 101 is optimized to show the many of the ICs functionality and it is intended to provide the user with a base IC for initial testing. It is designed to operate from a 3.3V input voltage.

Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1(V)	DVS Voltage Trigger	Sleep Mode	DPSLP Mode	Current Limit (A)	Fsw (kHz)
Buck1	2.9	2.5	GPIO3	On	Off	5	2250
Buck2	0.90	0.75	n/a	On	VSET1	5	2250
Buck3	1.8	1.2	GPIO4	On	Off	3	2250
LDO1	2.5	n/a	n/a	On	Off	0.410	n/a
LDO2	1.8	n/a	n/a	On	On	0.410	n/a
EXT_EN	n/a	n/a	n/a	On	Off	n/a	n/a

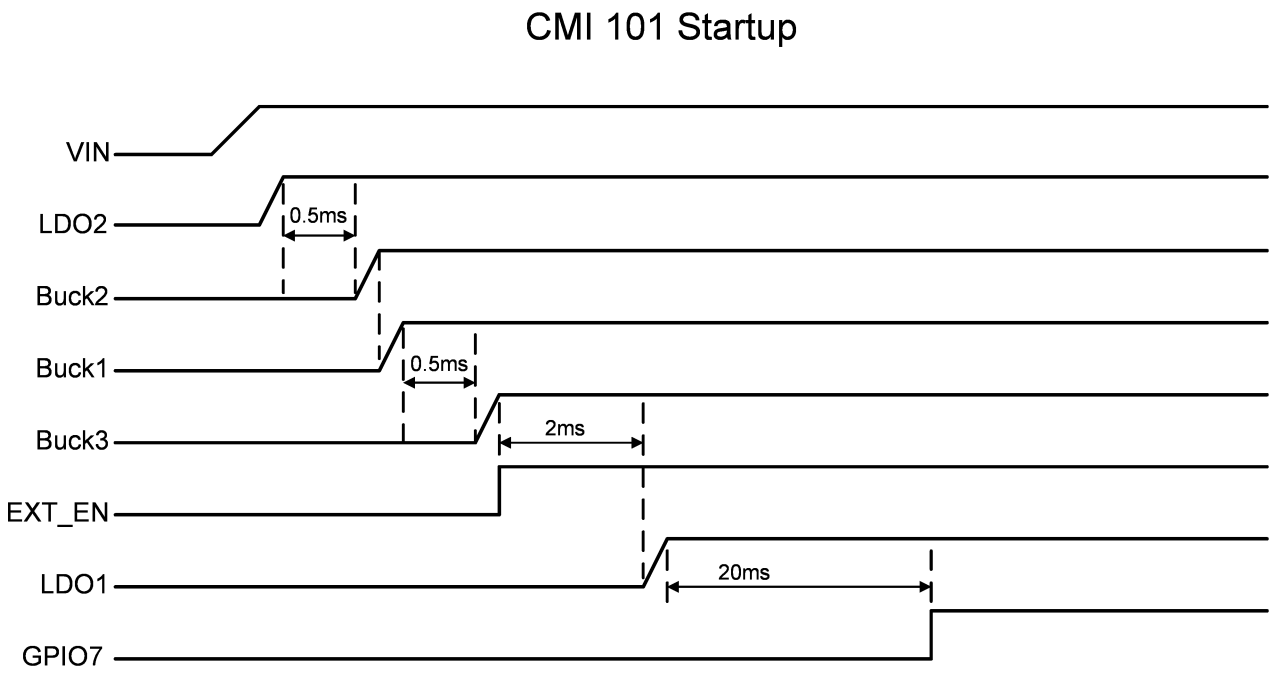
Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (ms)
LDO2	1	VIN_UVLO	41	0
Buck2	2	LDO2	41	0.5
Buck1	3	Buck2	41	0
Buck3	4	Buck1	41	0.5
EXT_EN	5	Buck3	41	0
LDO1	6	Buck3	41	2

Voltage Thresholds

Setting	Voltage Threshold
UVLO	2.6V
SYSMON	2.7V
SYSWARN	3.0V
POK_OV	3.5V
VIN_OV	3.7V

Startup



SLEEP Mode

SLEEP Mode is not enabled in CMI 101.

DPSLP Mode

Enter DPSLP Mode by pulling GPIO1 low. The Voltage and Currents table shows each output's operation in DPSLP Mode.

DVS Mode

DVS is not used as a standalone function in CMI 101. GPIO1 is effectively the DVS trigger for Buck2, but it achieves this by enabling the DPSLP Mode.

Voltage Select Inputs

GPIO3/4 are the voltage select inputs for Buck1/3. Note that GPIO3/4 cannot be changed while the outputs are enabled. When GPIO3 = H, Buck1 is set to its VSET0 voltage, 2.9V.

When GPIO3 = L, Buck1 is set to its VSET1 voltage, 2.5V.

When GPIO4 = H, Buck3 is set to its VSET0 voltage, 1.8V.

When GPIO4 = H, Buck3 is set to its VSET1 voltage, 1.2V.

GPIO1 - DPSLP Mode Trigger

Digital input. When GPIO1 = H, the IC is in Active Mode. When GPIO1 = L, the IC is in DPSLP Mode..

GPIO2 - SYSWARN

Open drain output. Active low SYSWARN output with 3.0V threshold.

GPIO3 – Buck1 Voltage Select

Digital input. When GPIO3 = H, Buck1 = 2.9V (VSET0). When GPIO3 = L, Buck1 = 2.5V (VSET1). Note that GPIO3 should be set before Buck1 is powered on.

GPIO4 – Buck3 Voltage Select

Digital input. When GPIO4 = H, Buck3 = 1.8V (VSET0). When GPIO4 = L, Buck3 = 1.25V (VSET1). Note that GPIO4 should be set before Buck3 is powered on.

GPIO5 – nIRQ

Digital output. Open drain.

GPIO6 – EXT_EN

Digital output. EXT_EN enables an external power supply. It is gated from Buck3 with a 2ms delay.

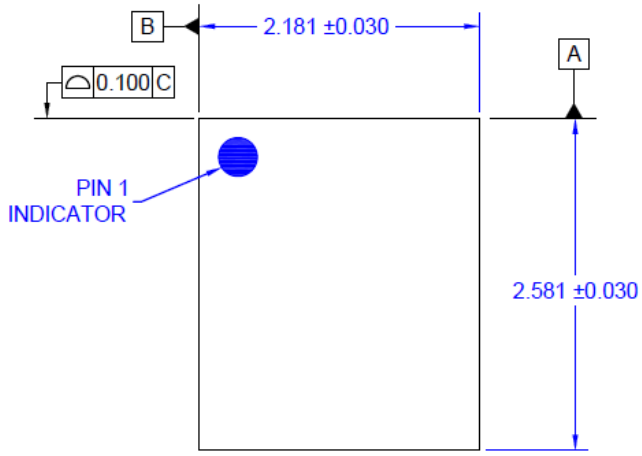
GPIO7 - nRESET

Digital output. Open drain. nRESET gated by LDO1 with a 20ms delay.

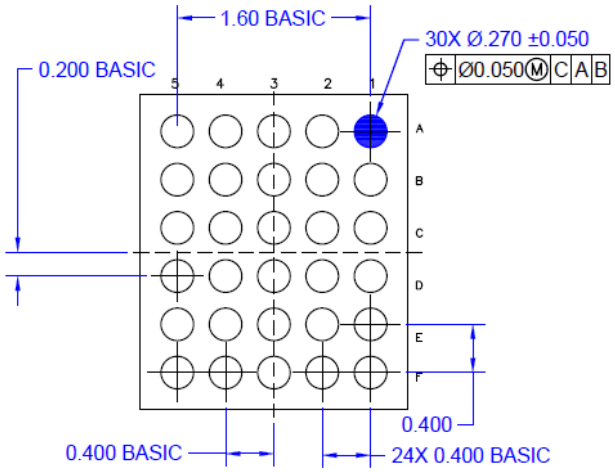
I^2C Address

The CMI 101 7-bit I^2C address is 0x25h. This results in 0x4Ah for a write address and 0x4Bh for a read address.

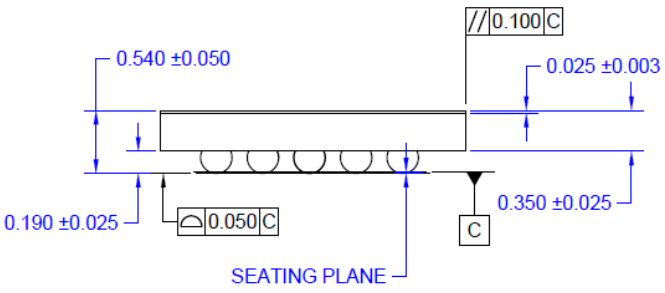
PACKAGE OUTLINE AND DIMENSIONS



TOP VIEW (BUMPS DOWN)



BOTTOM VIEW (BUMPS UP)



SIDE VIEW

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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