



ADVANCED

QM75041

5G PAMiD Module

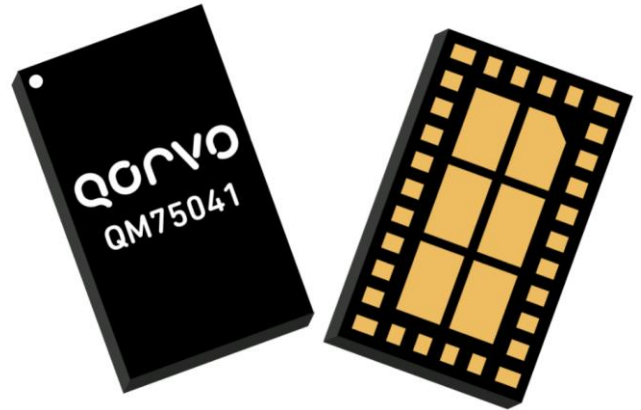
Product Description

The Qorvo® QM75041 is a highly integrated Sub-6GHz PAMiD compliant to 5G-NR standards focused on Best-in-class 5G performance and ease-of-use (EOU) for platforms targeting advanced RF, including flagship/premium smartphones and data devices.

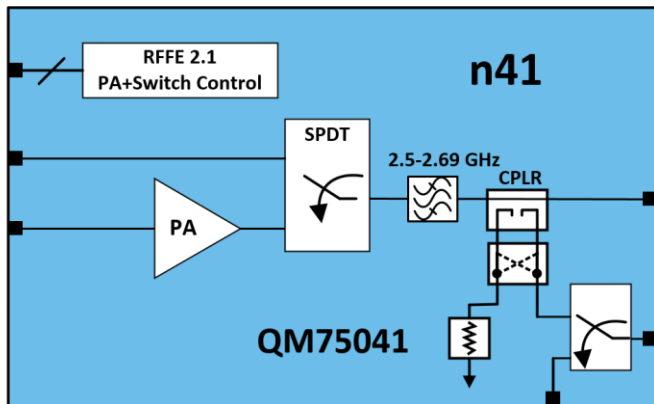
The module consists of a High Band PA, Filter, Directional Coupler and TxRx Switch for TDD operation.

The QM75041 supports Average Power Tracking (APT) PC2 power targets as well as Envelope Tracking (ET) up to 5.2 Vdc.

The QM75041 is packaged in a RoHS-compliant, 30 pin, 3mm x 5mm x 0.70mm lead less package.



Functional Block Diagram



Top View

30 Pin, 3.0 mm x 5.0 mm x 0.70 mm

Feature Overview

- 5G-NR supporting full n41 (2.496-2.690 GHz) Band
- Integrated filtering
- Integrated Vcc Bypass Cap Switch
- Bi-Directional Coupler
- Advanced Smartphones, Tablets and Cellular Devices
- Datacards
- Machine-to-Machine
- MIPI RFFE 2.1 Applications

Ordering Information

| PART NUMBER | DESCRIPTION |
|--------------|-----------------------------------|
| QM75041SB | 5pc Bag |
| QM75041TR7X | Any Size Reel |
| QM75041TR13 | 13" reel, Qty to order (5k units) |
| QM75041DK01 | Design Kit |
| QM75041EVB01 | Evaluation board |

Absolute Maximum Ratings

| Parameter | Symbol, Conditions | Rating | Units |
|----------------------------|--|------------|-------|
| Battery voltage | V _{BATT} | 6.0 | V |
| Max Supply Voltage | V _{CC1} , V _{CC2} | 6.0 | V |
| RFFE Control Interface Bus | VIO, SDATA, SCLK | 2.0 | V |
| Input RF Power | TX input, CW 50 Ohm, T=25 °C | +10.0 | dBm |
| Input RF Power | ANT port, Rx mode, in band frequencies | 25 | dBm |
| Storage Temperature | T _{storage} | -40 to 150 | °C |
| Operating Case Temperature | T _{case} | -20 to 85 | °C |
| No Damage Pout (5G) | All Temps, All Operating Voltage, VSWR<10:1 all phases | Prated + 2 | dBm |

Notes: Exceeding any one or combination of the Absolute Maximum Rating conditions may cause damage to the device. Extended application of the Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Conditions

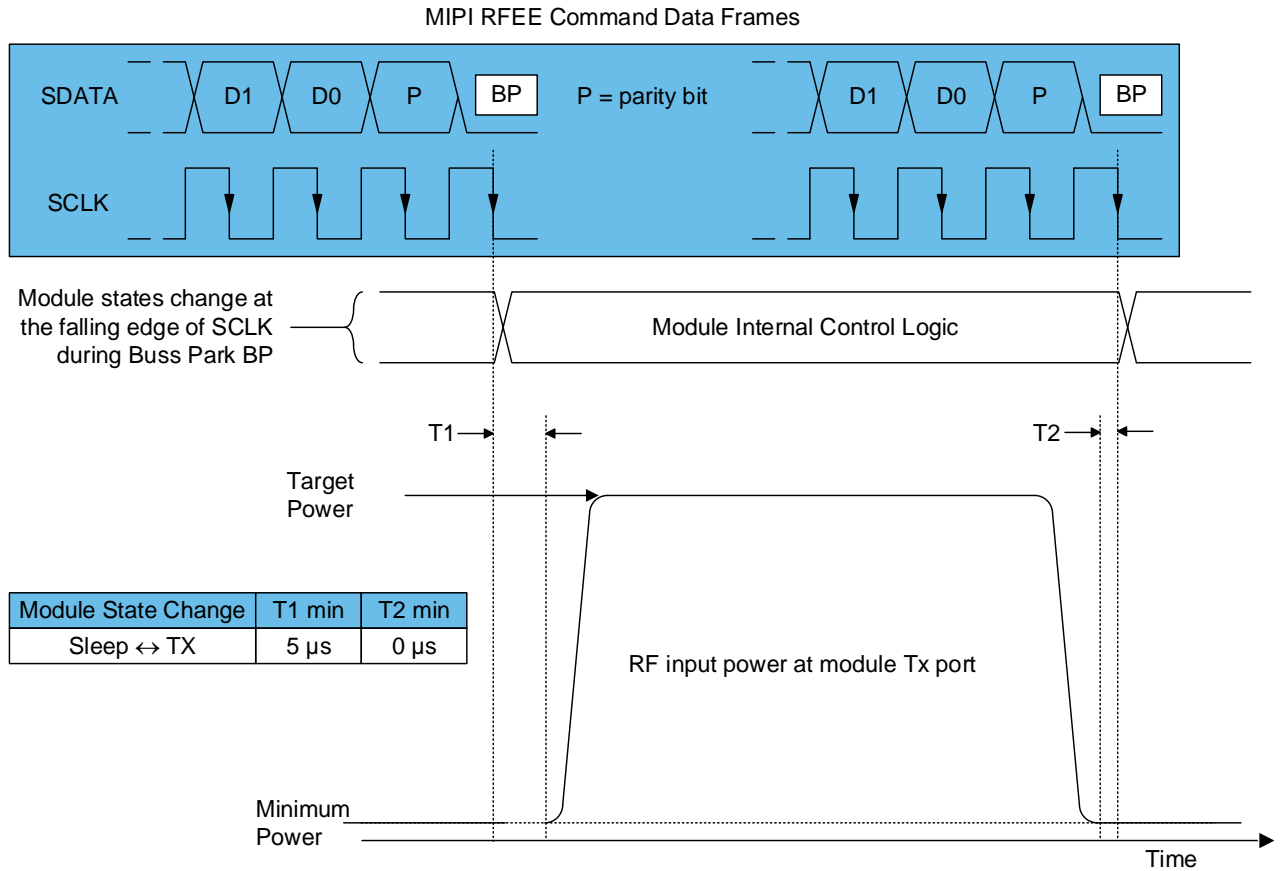
| Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------------------|---|---------|------|---------|-------|
| Supply Voltage | V _{BATT} | 3 | 3.8 | 4.8 | V |
| | APT V _{CC1} , V _{CC2} | 0.5 | 3.7 | 5.2 | |
| | ET V _{CC1} , V _{CC2} | 0.5 | 3.7 | 5.2 | |
| RFFE Control Interface Bus | VIO, SDATA, SCLK | 1.65 | 1.8 | 1.95 | V |
| VIO Power On Reset Voltage | VIO _{_Reset} | - | - | 0.45 | V |
| Logic Low | | 0 | 0 | 0.3*VIO | V |
| Logic High | | 0.7*VIO | | VIO | V |
| Leakage at VBatt | | | | 20 | uA |
| Leakage at VCC1/ VCC2 | | | | 20 | uA |
| Operating Case Temperature | | -20 | - | 85 | °C |
| Input and Output Impedance | | - | 50 | - | Ω |

Electrical Specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Timing Diagram

The QM75041 recommended control timing for Tx mode operation is shown below. The falling edge of SCLK during Bus Park (BP) is the master timing reference for all hardware events such as the application of RF input to the Tx input port of the module. Failure to comply with the specification below may result in RF output distortion or module damage.

For applications where MIPI RFEE V_{IO} is turned ON/OFF in accordance with MIPI RFEE bus activity, please refer to the **VIO Timing** specifications.



Delay application of RF power to Tx input by at least T1 μs after switching to Tx mode (TRX_SW_Control Bus Park BP).

Do not exit Tx mode until T2 μs after RF power at the Tx input has been removed. 2μs are recommended typically.

All test signals are 3GPP TS38.101 compliant

| WF TYPE | Modulation | MPR for all BW and SCS | |
|------------|------------|------------------------|-------|
| | | OUTER | INNER |
| DFT-s-OFDM | Pi/2-BPSK | ≤ 0.5 | 0 |
| | QPSK | ≤ 1 | 0 |
| | 16QAM | ≤ 2 | ≤ 1 |
| | 64QAM | ≤ 2.5 | |
| | 256QAM | ≤ 4.5 | |
| CP-OFDM | QPSK | ≤ 3 | ≤ 1.5 |
| | 16QAM | ≤ 3 | ≤ 2 |
| | 64QAM | ≤ 3.5 | |
| | 256QAM | ≤ 6.5 | |

5G NR n41 Tx Characteristics, PC2

Test conditions unless otherwise specified: $V_{CC1} = V_{CC2} = +5.2V$, $V_{BATT} = +3.8V$, Temp. = 25 °C. Characterized Operating Bandwidth: APT = 100MHz.

Performance referenced to module pin location.

| Parameter | Conditions | Power Mode | Product Spec. | | | Units |
|---|--|---------------------|---------------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| Frequency | | | 2496 | - | 2690 | MHz |
| Output Power | | | | | | |
| Linear Output Power n41 | Pout = +29.5 dBm, DFT-S-OFDM QPSK 100 MHz Inner RB | APT, HPM, MPR = 0 | 29.5 | 29.7 | - | dBm |
| Gain | | | | | | |
| Gain (G) n41 | Pout = +29.5 dBm, DFT-S-OFDM QPSK 100 MHz Inner RB | APT, HPM, MPR = 0 | | 30 | | dB |
| Linearity | | | | | | |
| Adjacent Channel Leakage Power Ratio (ACLR) n41 | EUTRA _{ACLR} , Pout = +26.5dBm, CP-OFDM QPSK, 100 MHz FRB | APT, HPM, MPR = 3 | | -38 | | dBc |
| EVM | | | | | | |
| EVM n41 | EVM, Pout = +23.0dBm, CP-OFDM 256 QAM, 100 MHz FRB | APT, HPM, MPR = 6.5 | | 1.85 | 2.0 | % |
| Current | | | | | | |
| Current n41 | Current, Pout = +29.5 dBm, DFT-S-OFDM QPSK 100 MHz Inner RB | APT, HPM, MPR = 0 | | | 1000 | mA |
| Output Power | | | | | | |
| Linear Output Power n41 | Pout = +3.0 dBm, DFT-S-OFDM QPSK 100 MHz FRB | APT LPM | 3.0 | - | - | dBm |
| Gain | | | | | | |
| Gain (G) n41 | Pout = +3.0 dBm, DFT-S-OFDM QPSK 100 MHz FRB | APT LPM | | 23 | | dB |

| Parameter | Conditions | Power Mode | Product Spec. | | | Units |
|--|--|------------|---------------|------|-------|----------|
| | | | Min. | Typ. | Max. | |
| Frequency | | | 2496 | - | 2690 | MHz |
| Linearity | | | | | | |
| Adjacent Channel Leakage Power Ratio (ACLR) n41 | EUTRA _{ACLR} , Pout = +3.0 dBm, DFT-S-OFDM QPSK, 100 MHz FRB | APT LPM | | -38 | | dBc |
| Adjacent Channel Leakage Power Ratio (ACLR) n41 | EUTRA _{ACLR} , Pout = +3.0 dBm, CP-OFDM QPSK, 100 MHz FRB | APT LPM | | -38 | | dBc |
| Current | | | | | | |
| Current n41 | Current, Pout = +3.0 dBm | APT LPM | | | 115 | mA |
| Rx Band Noise | | | | | | |
| Rx BN at n41 Tx output, 600 - 960MHz, (LB) | MPR=1, Pout = +28.5 dBm, QPSK, MPR=3, Pout = +26.5 dBm, QPSK | APT HPM | | -170 | | dBm/ Hz |
| Rx BN at n41 Tx output, 1574 - 1577MHz, (GPS, GLONASS) | MPR=1, Pout = +28.5 dBm, QPSK, MPR=3, Pout = +26.5 dBm, QPSK | APT HPM | | -171 | | dBm/ Hz |
| Rx BN at n41 Tx output, 1805 - 1880MHz, (MB) | MPR=1, Pout = +28.5 dBm, QPSK, MPR=3, Pout = +26.5 dBm, QPSK | APT HPM | | -171 | | dBm/ Hz |
| Rx BN at n41 Tx output, 2475 - 2495MHz (2.4GHz WiFi) | MPR=1, Pout = +28.5 dBm, QPSK, MPR=3, Pout = +26.5 dBm, QPSK | APT HPM | | -128 | | dBm/ Hz |
| Rx BN at n41 Tx output, 3300 - 5000MHz, (UHB) | MPR=1, Pout = +28.5 dBm, QPSK, MPR=3, Pout = +26.5 dBm, QPSK | APT HPM | | -137 | | dBm/ Hz |
| HARMONICS | | | | | | |
| 2 nd Harmonic n41 | Pout ≤ max power, measured with 100MHz DFTS-OFDM-QPSK 1 RB 1 SRB, 136 SRB, 1 RB 2702SRB MPR=0 waveform, Pout=+29.5 dBm | APT HPM | | | -40.0 | dBm/ MHz |
| 3 rd Harmonic n41 | Pout ≤ max power, measured with 100MHz DFTS-OFDM-QPSK 1 RB 1 SRB, 136 SRB, 1 RB 2702SRB MPR=0 waveform, Pout=+29.5 dBm | APT HPM | | | -40.0 | dBm/ MHz |
| 4 th Harmonic n41 | Pout ≤ max power, measured with 100MHz DFTS-OFDM-QPSK 1 RB 136 SRB MPR=0 waveform, Pout=+29.5 dBm | APT HPM | | | -40.0 | dBm/ MHz |
| Spurious Levels | All Loads ≤ 6:1 | All Modes | | | -70.0 | dBc |

5G NR n41 Rx Characteristics

Test conditions unless otherwise specified: $V_{BATT} = +3.8\text{ V}$, Temp. = $25\text{ }^{\circ}\text{C}$, PA disabled.
 Performance referenced to module pin location.

| Parameter | Conditions | Product Spec. | | | Units |
|-------------------------|-------------------------------------|---------------|------|------|-------|
| | | Min. | Typ. | Max. | |
| Frequency | | 2496 | - | 2690 | MHz |
| Insertion Loss | | | | | |
| I.L. n41 | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | 2.6 | - | dB |
| Return Loss | | | | | |
| I.R.L. n41 | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | -14 | - | dB |
| O.R.L. n41 | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | -14 | - | dB |
| Rx Rejection | | | | | |
| LB Tx,699 – 915 MHz | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | 43 | - | dB |
| B3 Tx,1710-1785 MHz | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | 43 | - | dB |
| ISM Tx,2400 MHz | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | 47 | - | dB |
| Tx,3300-5000 MHz | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | 43 | - | dB |
| ISM 5G Tx,5000-5925 MHz | $V_{CC1} = V_{CC2} = +5.2\text{ V}$ | - | 36 | - | dB |

5G NR n41 Coupler Characteristics

Test conditions unless otherwise specified: $V_{BATT} = +3.8\text{ V}$, Temp. = $25\text{ }^{\circ}\text{C}$, PA disabled.
 Performance referenced to module pin location.

| Parameter | Conditions | Product Spec. | | | Units |
|---|-------------------|---------------|------|------|-------|
| | | Min. | Typ. | Max. | |
| Frequency | | 2496 | - | 2690 | MHz |
| Coupling Factor | | | | | |
| Coupling Factor | | - | 20 | - | dB |
| Coupler Variation over Output VSWR | | | | | |
| Coupler Variation | 2.5:1 at Ant Port | -0.5 | - | 0.5 | dB |



Recommended Register Settings for PA Section (RFFE1)

MIPI RFE Description

The RFFE interface implemented in the QM75041 is in compliance with the **MIPI Alliance Specification for RF Front-End Control Interface Version 2.1 - April 2018**

TX FFE Registers (RFFE1)

| Register address | Data Bits | Register Name | Qorvo Bit Field Name | Default [msb:lsb] | Qorvo Description | Read/Write | Trigger support | Mask Write Support |
|------------------|------------|---------------|----------------------|-------------------|---|------------|-----------------|--------------------|
| 0x00 | Reg00[7:4] | PA_CTRL0 | Reserved | 4b0000 | Reserved | R/W | T0 | Yes |
| 0x00 | Reg00[3] | PA_CTRL0 | PA_EN | 1b0 | PA Enable 0: PA OFF 1: PA ON | R/W | T0 | Yes |
| 0x00 | Reg00[2] | PA_CTRL0 | VCC_CAP_BYP | 1b0 | VCC Capacitor control 0: iso mode (VCC cap switched out) 1: bypass mode (VCC cap switched in) OR'ed with Reg05[0] VCC_CAP_SW | R/W | T0 | Yes |
| 0x00 | Reg00[1:0] | PA_CTRL0 | PA_MODE[1:0] | 2b00 | PA Mode 00: ET HPM 01: APT HPM 10: APT LPM 11: Reserved (same as APT LPM) | R/W | T0 | Yes |
| 0x01 | Reg01[7:0] | PA_CTRL2 | PA_BIAS2[7:0] | 8b00000000 | PA Bias - power stage | R/W | T0 | No |
| 0x02 | Reg02[7:0] | PA_CTRL1 | PA_BIAS1[7:0] | 8b00000000 | PA Bias - driver stage | R/W | T0 | No |
| 0x03 | Reg03[7:4] | TR_CTRL | Reserved | 4b0000 | Reserved | R/W | T1 | Yes |
| 0x03 | Reg03[3:0] | TR_CTRL | ANT_SW[3:0] | 4b0000 | Transmit/Receive Switch Control. 0000: OFF 0001: reserved (same as 0000) 0010: TX (load switch open) 0011: PC3 TX (load switch closed) 0100: reserved (same as 0000) 0101: reserved (same as 0000) 0110: reserved (same as 0000) 0111: reserved (same as 0000) 1000: reserved (same as 0000) 1001: RX 1010: reserved (same as 0000) 1011: reserved (same as 0000) 1100: reserved (same as 0000) 1101: reserved (same as 0000) 1110: reserved (same as 0000) 1111: reserved (same as 0000) | R/W | T1 | Yes |
| 0x04 | Reg04[7:2] | CPL_CTRL | Reserved | 6b000000 | Reserved | R/W | T2 | Yes |
| 0x04 | Reg04[1:0] | CPL_CTRL | CPL_OUT[1:0] | 2b00 | Coupler Output 00: High Isolation 01: Forward Port 10: Reverse Port 11: Coupler In | R/W | T2 | Yes |
| 0x05 | Reg05[7:1] | PA_CTRL2 | Reserved | 7b00000000 | Reserved | R/W | T0 | Yes |
| 0x05 | Reg05[0] | PA_CTRL2 | VCC_CAP_SW | 1b0 | VCC Capacitor control 0: iso mode (VCC cap switched out) 1: bypass mode (VCC cap switched in) OR'ed with Reg00[2] VCC_CAP_BYP | R/W | T0 | Yes |

TX FFE Registers (RFFE1)

| Register address | Data Bits | Register Name | Qorvo Bit Field Name | Default [msb:lsb] | Qorvo Description | Read/Write | Trigger support | Mask Write Support |
|------------------|------------|------------------------|---------------------------|-------------------|---|------------|-----------------|--------------------|
| 0x1C | Reg28[7] | PM_TRIG | PWR_MODE | 1b1 | 0: Normal operation (ACTIVE) 1: Secondary mode (LOW POWER) | R/W | No | No |
| 0x1C | Reg28[6] | PM_TRIG | PWR_STATE | 1b0 | 0: Normal operation 1: initialization state note - this bit always reads 0. Writing a 1 to this bit forces a reset. | R/W | No | No |
| 0x1C | Reg28[5:3] | PM_TRIG | TriggerMask[2:0] | 3b000 | Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). TriggerMask[2] = TriggerMask_2, TriggerMask[1] = TriggerMask_1, & TriggerMask[0] = TriggerMask_0 | R/W | No | No |
| 0x1C | Reg28[2:0] | PM_TRIG | Trigger[2:0] | 3b000 | Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Trigger[2] = Trigger_2, Trigger[1] = Trigger_1, and Trigger[0] = Trigger_0 | R/W | No | No |
| 0x1D | Reg29[7:0] | PRODUCT_ID | PRODUCT_ID[7:0] | 8b00101100 | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value. | RM | No | No |
| 0x1E | Reg30[7:0] | MAN_ID | MANUFACTURER_ID_LSB [7:0] | 8b11000110 | This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. Note: This is the lower 8 least significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[7:0] = MANUFACTURER_ID_LSB[7:0]) | RM | No | No |
| 0x1F | Reg31[7:4] | MAN_US_ID | MANUFACTURER_ID_MSB [3:0] | 4b0011 | These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. Note: This is the 4 most significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[11:8] = MANUFACTURER_ID_MSB[3:0]) | RM | No | No |
| 0x1F | Reg31[3:0] | MAN_US_ID | USID[3:0] | 4b1111 | Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. | RM | No | No |
| 0x20 | Reg32[7:0] | EXT_PRODUCT_ID | EXT_PRODUCT_ID[7:0] | 8b00000000 | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value. | RM | No | No |
| 0x21 | Reg33[7:0] | REVISION_ID | REVISION_ID[7:0] | 8b00000000 | This is an RFFE2 register to contain information about the revision of this module. The intent here is to use this as a type of scratch register -- to contain various information or serialization. | RM | No | No |
| 0x22 | Reg34[7:4] | GROUP_ID2 | GSID0_2[3:0] | 4b0000 | Group slave ID 0 | R/W | No | No |
| 0x22 | Reg34[3:0] | GROUP_ID2 | GSID1_2[3:0] | 4b0000 | Group slave ID 1 | R/W | No | No |
| 0x23 | Reg35[7] | UDR_RST (RFFE_STATUS2) | SW_RESET_2 | 1b0 | 0: Normal operation 1: Software reset (reset of all configurable registers to default values, except for USID) | R/W | No | No |
| 0x23 | Reg35[6] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b6 | 1b0 | Reserved | R/W | No | No |
| 0x23 | Reg35[5] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b5 | 1b0 | Reserved | R/W | No | No |
| 0x23 | Reg35[4] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b4 | 1b0 | Reserved | R/W | No | No |
| 0x23 | Reg35[3] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b3 | 1b0 | Reserved | R/W | No | No |
| 0x23 | Reg35[2] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b2 | 1b0 | Reserved | R/W | No | No |
| 0x23 | Reg35[1] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b1 | 1b0 | Reserved | R/W | No | No |
| 0x23 | Reg35[0] | UDR_RST (RFFE_STATUS2) | Reserved_Reg35_b0 | 1b0 | Reserved | R/W | No | No |



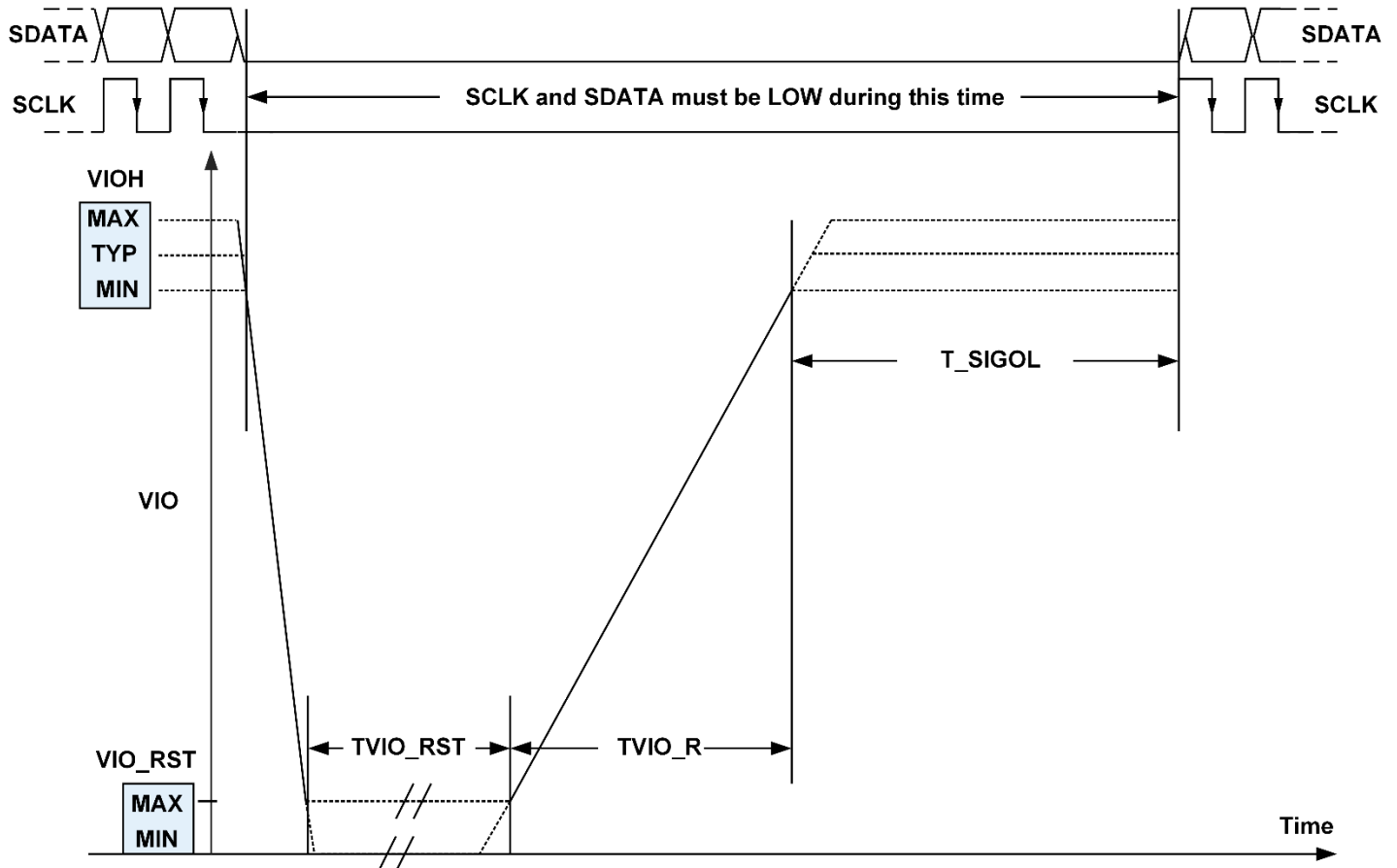
TX FFE Registers (RFFE1)

| Register address | Data Bits | Register Name | Qorvo Bit Field Name | Default [msb:lsb] | Qorvo Description | Read/Write | Trigger support | Mask Write Support |
|------------------|------------|------------------------|----------------------|-------------------|---|------------|-----------------|--------------------|
| 0x1C | Reg28[7] | PM_TRIG | PWR_MODE | 1b1 | 0: Normal operation (ACTIVE) 1: Secondary mode (LOW POWER) | R/W | No | No |
| 0x24 | Reg36[7] | ERR_SUM (RFFE_STATUS3) | Reserved_Reg36_b7 | 1b0 | Reserved | R/W | No | No |
| 0x24 | Reg36[6] | ERR_SUM (RFFE_STATUS3) | CMD_FRAME_P_ERR_2 | 1b0 | Command sequence received with parity error – discard command. | R/W | No | No |
| 0x24 | Reg36[5] | ERR_SUM (RFFE_STATUS3) | CMD_LEN_ERR_2 | 1b0 | Command length error | R/W | No | No |
| 0x24 | Reg36[4] | ERR_SUM (RFFE_STATUS3) | ADDR_FRAME_P_ERR_2 | 1b0 | Address frame parity error = 1 | R/W | No | No |
| 0x24 | Reg36[3] | ERR_SUM (RFFE_STATUS3) | DATA_FRAME_P_ERR_2 | 1b0 | Data frame with parity error | R/W | No | No |
| 0x24 | Reg36[2] | ERR_SUM (RFFE_STATUS3) | READ_UNUSED_REG_2 | 1b0 | Read command to an invalid address | R/W | No | No |
| 0x24 | Reg36[1] | ERR_SUM (RFFE_STATUS3) | WRITE_UNUSED_REG_2 | 1b0 | Write command to an invalid address | R/W | No | No |
| 0x24 | Reg36[0] | ERR_SUM (RFFE_STATUS3) | BID_GID_ERR_2 | 1b0 | Read command with a Broadcast_ID or GROUP_ID | R/W | No | No |
| 0x2B | Reg43[7:4] | BUS_LOAD | reserved_Reg_43 | 4b0000 | Reserved | R/W | No | No |
| | | | | 4b0100 | SDATA Driver strength in Readback Mode 0x0: 10pf 0x1: 20pf 0x2: 30pf 0x3: 40pf 0x4: 50pf 0x5: 60pf 0x6: 80pf 0x7: 100pf 0x8: 120pf 0x9: 140pf 0xA: 160pf 0xB: 180pf 0xC: 200pf 0xD: 250pf 0xE-0xF: reserved | R/W | No | No |
| 0x2B | Reg43[3:0] | BUS_LOAD | BUS_LOAD[3:0] | | | | | |
| 0x2C | Reg44[7:0] | TEST_PATTERN | Test_Pattern[7:0] | 8b11010010 | A read of this register returns the test pattern | R | No | No |

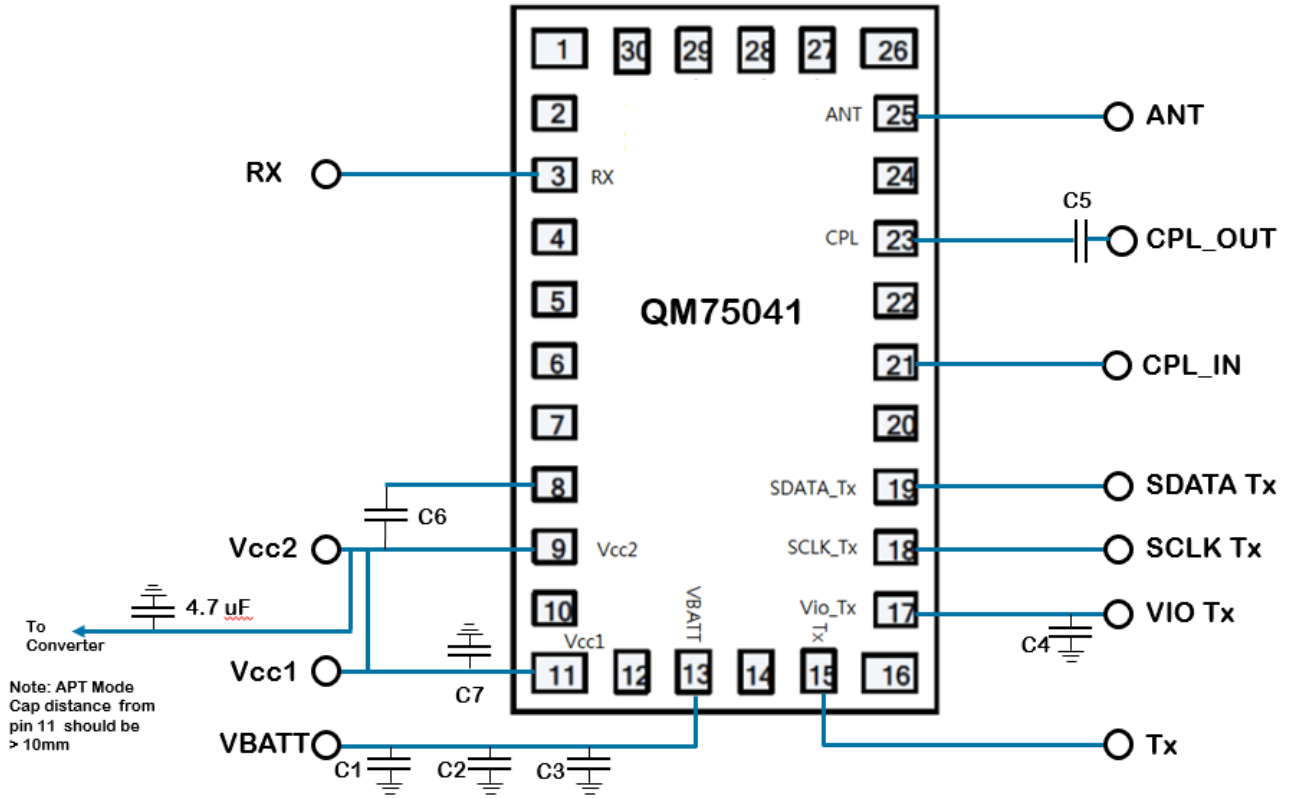
VIO Power On Reset (POR) Timing

For applications where MIPI RFEE VIO is turned ON/OFF in accordance with MIPI RFEE bus activity, the timing recommendations below should be used to ensure error-free RFEE register writes following VIO power on reset (POR)

| Parameter | Description | MIN | TYP | MAX |
|-----------|--------------------------------|-------|-------|-------|
| VIOH | VIO High Voltage | 1.65V | 1.80V | 1.95V |
| VIO_RST | VIO Reset Voltage | 0V | 0V | 0.45V |
| TVIO_RST | VIO Reset Time | 10μs | - | - |
| TVIO_RST | VIO Rise Time | 1μs | - | 400μs |
| T_SIGOL | Minimum Wait Time after TVIO_R | 190μs | - | - |

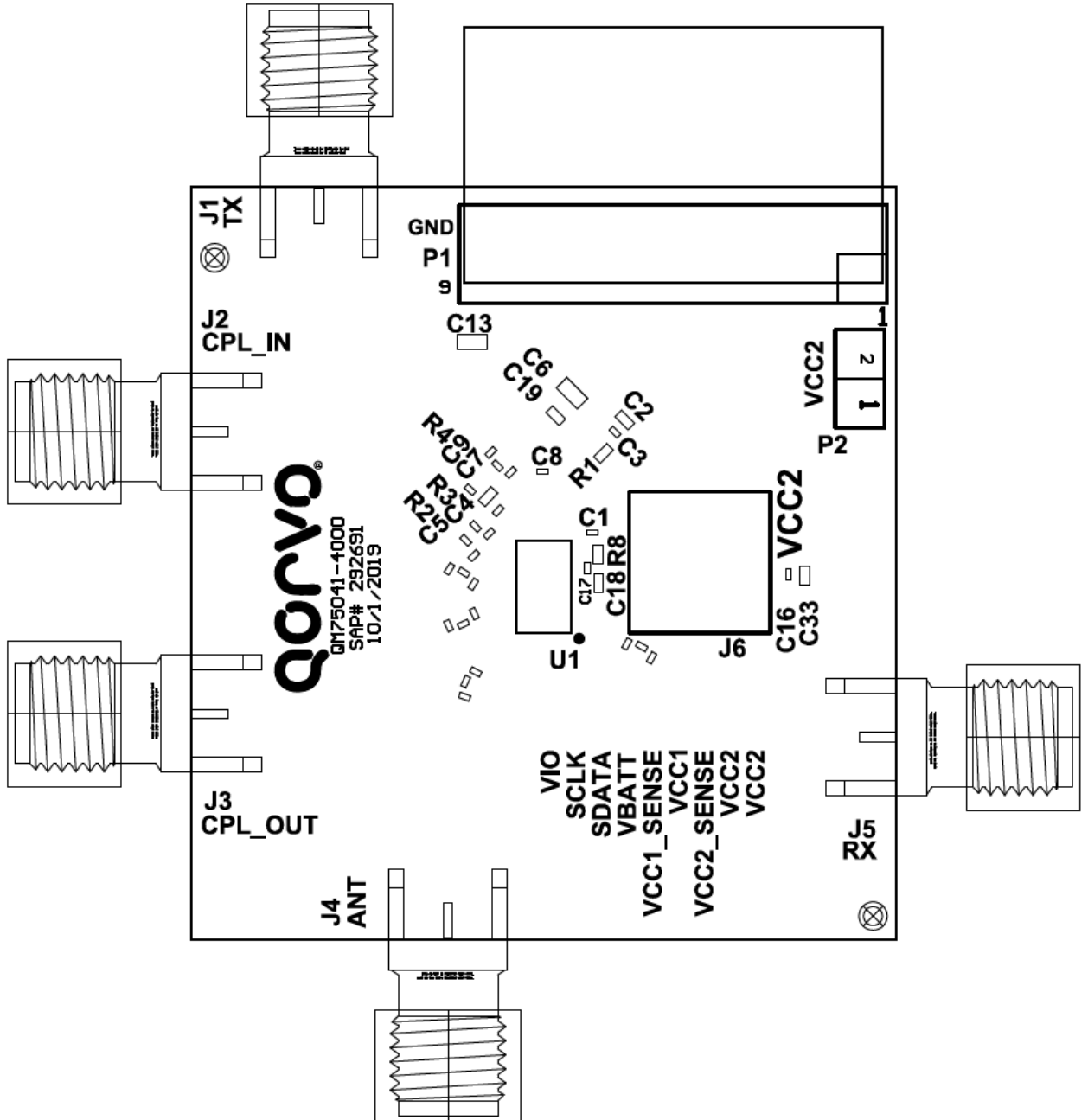


Application Schematic

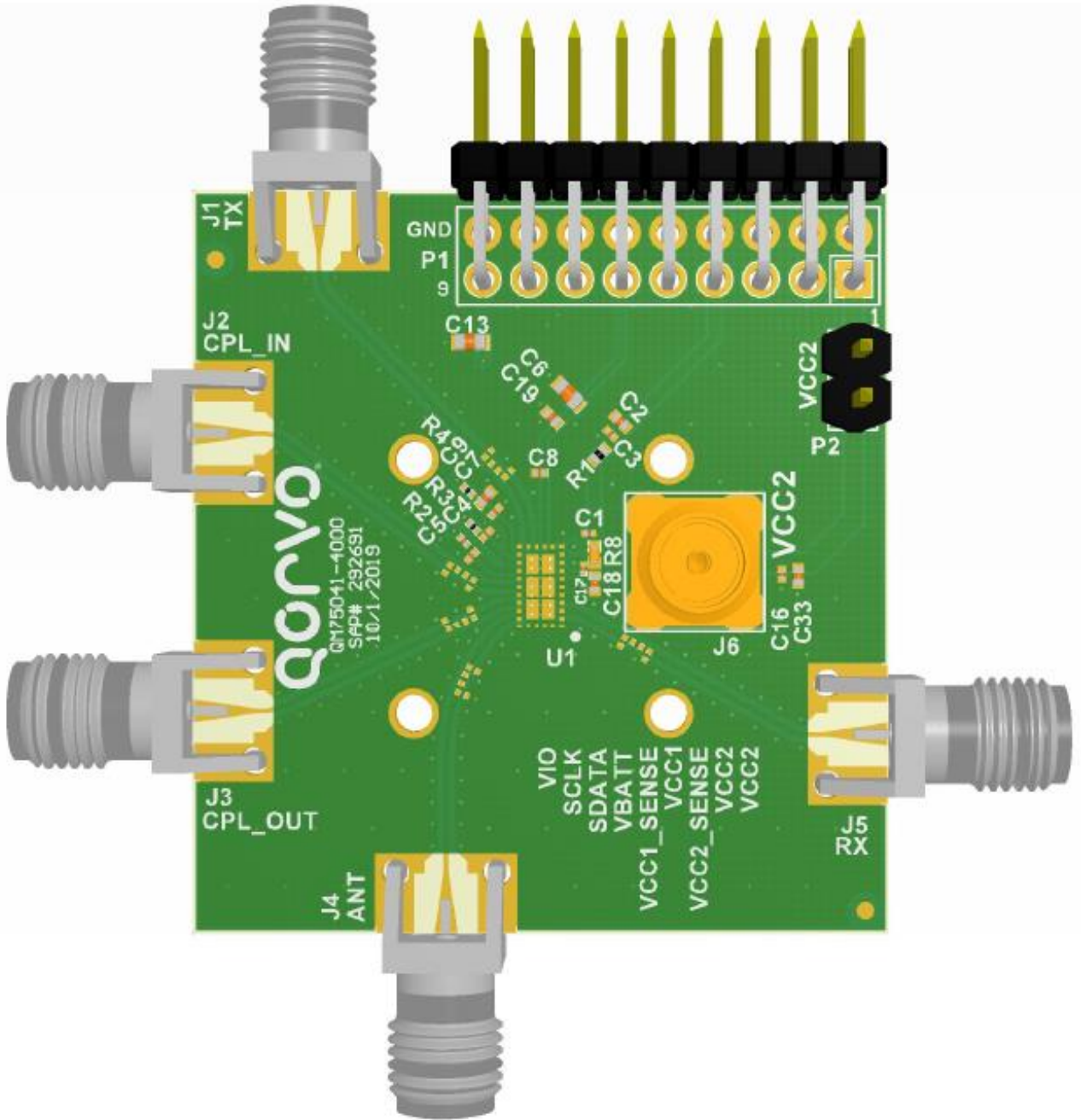


| Ref. Des. | Recommended Value | Purpose |
|-----------|-------------------|---------------------|
| C1 | 4.7uF | VBATT bypassing |
| C2 | 10nF or NC | VBATT bypassing |
| C3 | 100pF or NC | VBATT bypassing |
| C4 | 100pF or NC | VIO bypassing |
| C5 | 18 pF | DC Block |
| C6 | 1uF | Switched Bypass cap |
| C7 | 100 pF | VCC bypassing |

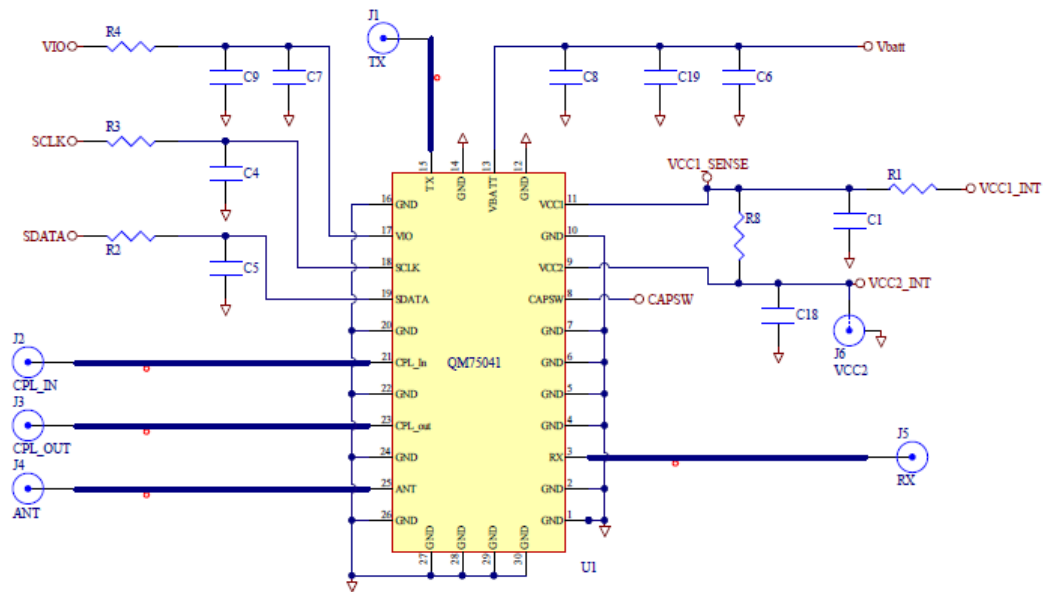
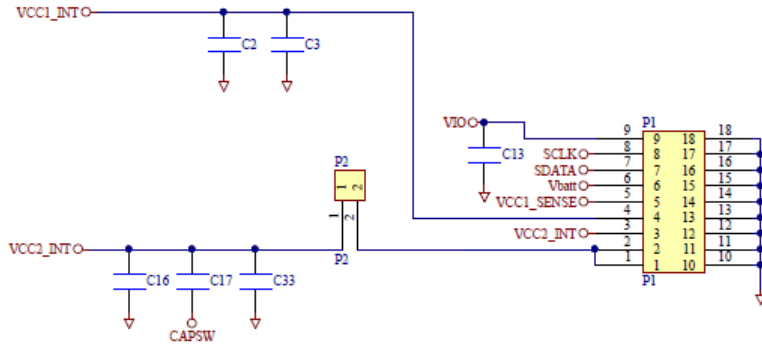
Evaluation Board Layout



Evaluation Board Layout (continued)



Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)



BOM Report
(DRAFT – Not Released)

Draft

AQM75041EVB Rev(A)

Plant: 5100
BOM: Usage(1) Alt(01)
Plant Type: Production
Nickname: QM75041-4000

Effective: TBD (Draft) System Time
ECN: 500000651031

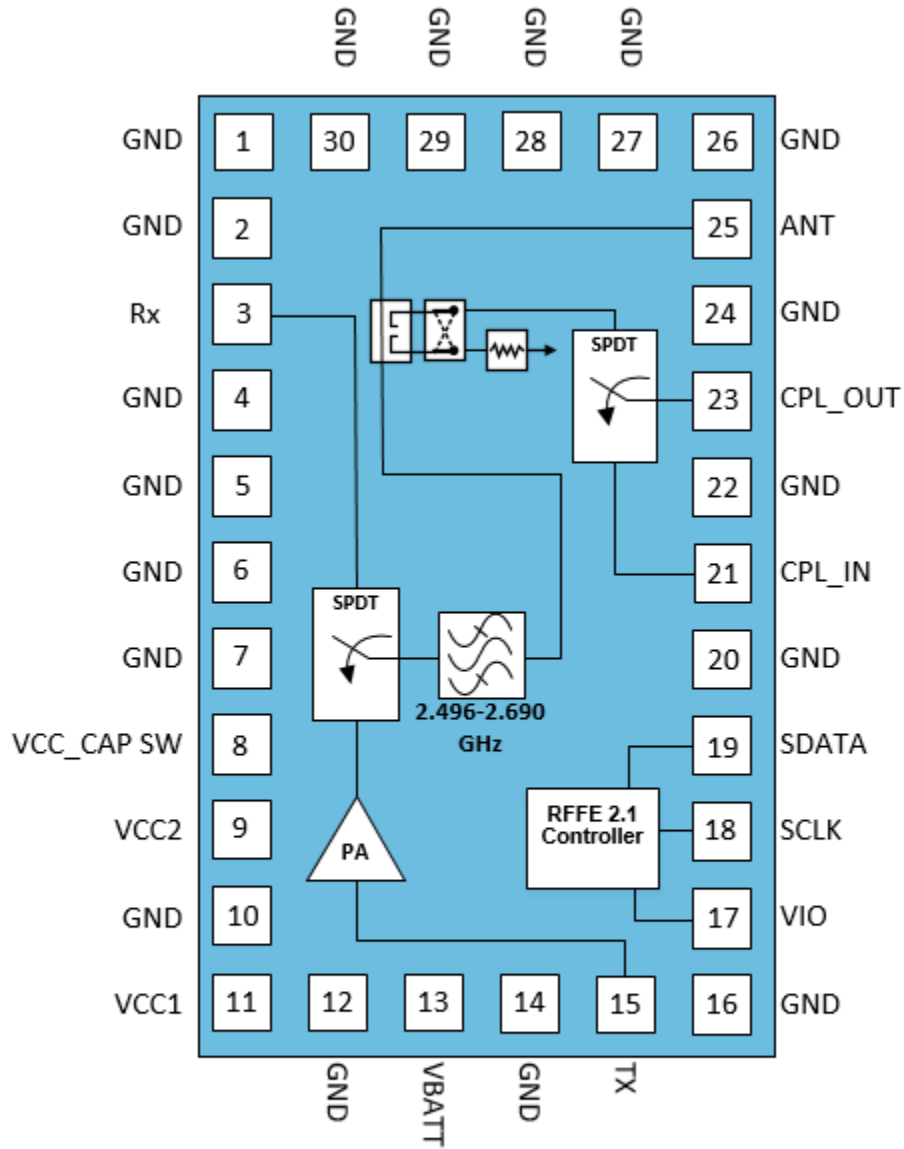
Package System: PCBAStruct
Work Center: Qorvo (Beijing)
Package Type: PCBA

Associated Documents

| | | |
|--------------|-------|---------------------------------------|
| QM75041-4000 | Rev A | QM75041 Evaluation PCB Design Package |
|--------------|-------|---------------------------------------|

| Ref Des | Qty | Material # | Alt Grp | Usage Prob % | Description | Manufacturer | Manufacturer Part # |
|----------------|-----|------------|---------|--------------|---|-------------------------------------|---------------------|
| | 1 | 292691 | | | PCB, QM75041 | TTM TECHNOLOGIES INC | QM75041-4000(A) |
| C1,C7,C8 | 3 | 1030745 | | | CAP, 100pF, ±5%, 25V, C0G, 0201 | MURATA ELECTRONICS SINGAPORE PTE LT | GRM0335C1E101JA01D |
| C9 | 1 | 271052 | | | CAP, 2.2uF, 10%, 6.3V, X5R, 0402 | TAIYO YUDEN (SINGAPORE) PTE LTD | RM JMK105BJ225KV-F |
| C6 | 1 | 271154 | | | CAP, 2.2uF, 10%, 10V, X7R, 0603 | TDK SINGAPORE (PTE) LTD | C1608X7R1A225K080AC |
| C17 | 1 | 272645 | | | CAP, 1uF, 20%, 6.3V, X5R, 0201 | MURATA ELECTRONICS SINGAPORE PTE LT | GRM033R60J105MEA2D |
| C18 | 1 | 283855 | | | CAP, 4.7uF, 20%, 10V, X5R, 0.65mm, 0402 | MURATA ELECTRONICS SINGAPORE PTE LT | GRM155R61A475MEAAD |
| C4,C5 | 2 | CAP1211 | | | CAP, 39pF, 5%, 25V, C0G, 0201 | Qorvo | CAP1211 |
| R2,R3,R4 | 3 | 21253 | | | RES, 0 OHM, 5%, 1/20W, 0201 | Kamaya, Inc | RMC1/20JPPA15 |
| R8 | 1 | 21592 | | | RES, 0 OHM, 5%, 1/10W, 0402 | Kamaya, Inc | RMC1/16SJPTH |
| J1,J2,J3,J4,J5 | 5 | 22539 | | | CONNECTOR,SMA EL FLT VIPER MAT -21-1038 | AMPHENOL—KAI JACK (SHENZHEN) INC | 20-001CH-T |
| P2 | 1 | 23669 | | | CONN, HDR, ST, PLRZD, 2-PIN, 0.100" | AMP | 640454-2 |
| J6 | 1 | 266994 | | | CONN, SMB, ST PLUG REC, T/H | Aliner Industries, Inc. | 21-003B0-T |
| P1 | 1 | 280114 | | | CONN, HDR, 2x9, RT-ANG, 0.100", T/H | SAMTEC INC. | TSW-109-08-G-D-RA |
| R1 | 1 | 4XXX1 | | | NOT POPULATED ITEM-1 | | DUMMY PART |
| C3,C16 | 2 | 4XXX2 | | | NOT POPULATED ITEM-2 | | DUMMY PART |
| C2,C19,C33 | 3 | 4XXX4 | | | NOT POPULATED ITEM-4 | | DUMMY PART |
| C13 | 1 | 4XXX6 | | | NOT POPULATED ITEM-6 | | DUMMY PART |

Pin Configuration and Description



Top View (looking through device)

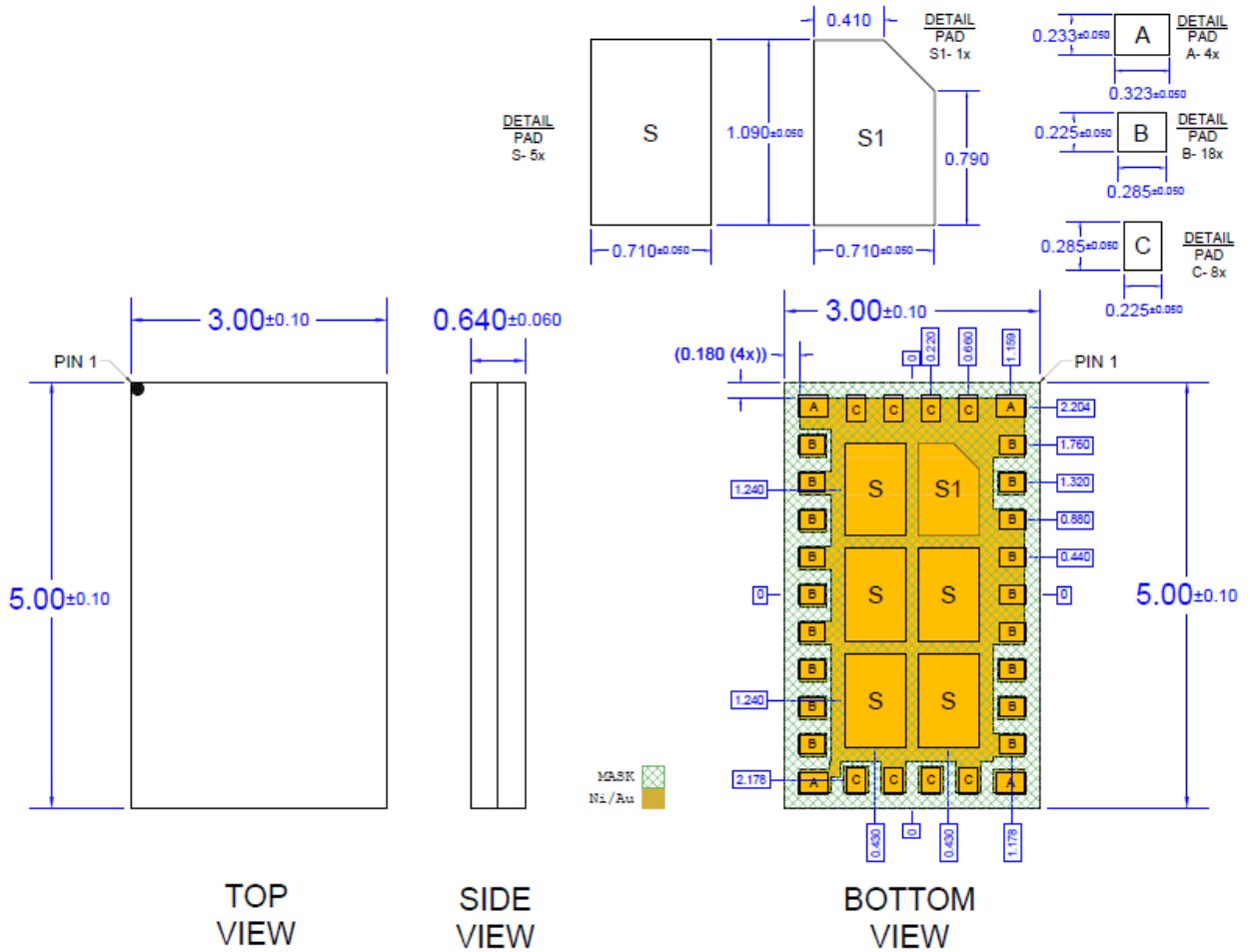
Pin Configuration and Description (continued)

| PIN NUMBER | LABEL | DESCRIPTION |
|------------|------------|--|
| 1 | GND | Ground |
| 2 | GND | Ground |
| 3 | RXout_n41 | RX Output |
| 4 | GND | Ground |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 | GND | Ground |
| 8 | VCC_CAP_SW | Switchable Ground connection for large external SMD Bypass Capacitor |
| 9 | VCC2 | Supply voltage for n41 2 nd stage PA |
| 10 | GND | Ground |
| 11 | VCC1 | Supply voltage for n41 1 st and stage PA |
| 12 | GND | Ground |
| 13 | VBATT | Battery supply voltage for controller |
| 14 | GND | Ground |
| 15 | TX | N41 PA RF Input |
| 16 | GND | Ground |
| 17 | VIO | Supply voltage for MIPI RFFE interface |
| 18 | SCLK | Clock signal for MIPI RFFE interface |
| 19 | SDATA | Data signal for MIPI RFFE interface |
| 20 | GND | Ground |
| 21 | CPL_IN | Coupler Input Port |
| 22 | GND | Ground |
| 23 | CPL_OUT | Coupler Output Port |
| 24 | GND | Ground |
| 25 | Ant_n41 | N41 Antenna Port |
| 26 | GND | Ground |
| 27 | GND | Ground |
| 28 | GND | Ground |
| 29 | GND | Ground |
| 30 | GND | Ground |

Mechanical Information – Dimensions

Package Marking and Dimensions

Marking: Part number –QM75041



Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

Mechanical Information – Package Marking

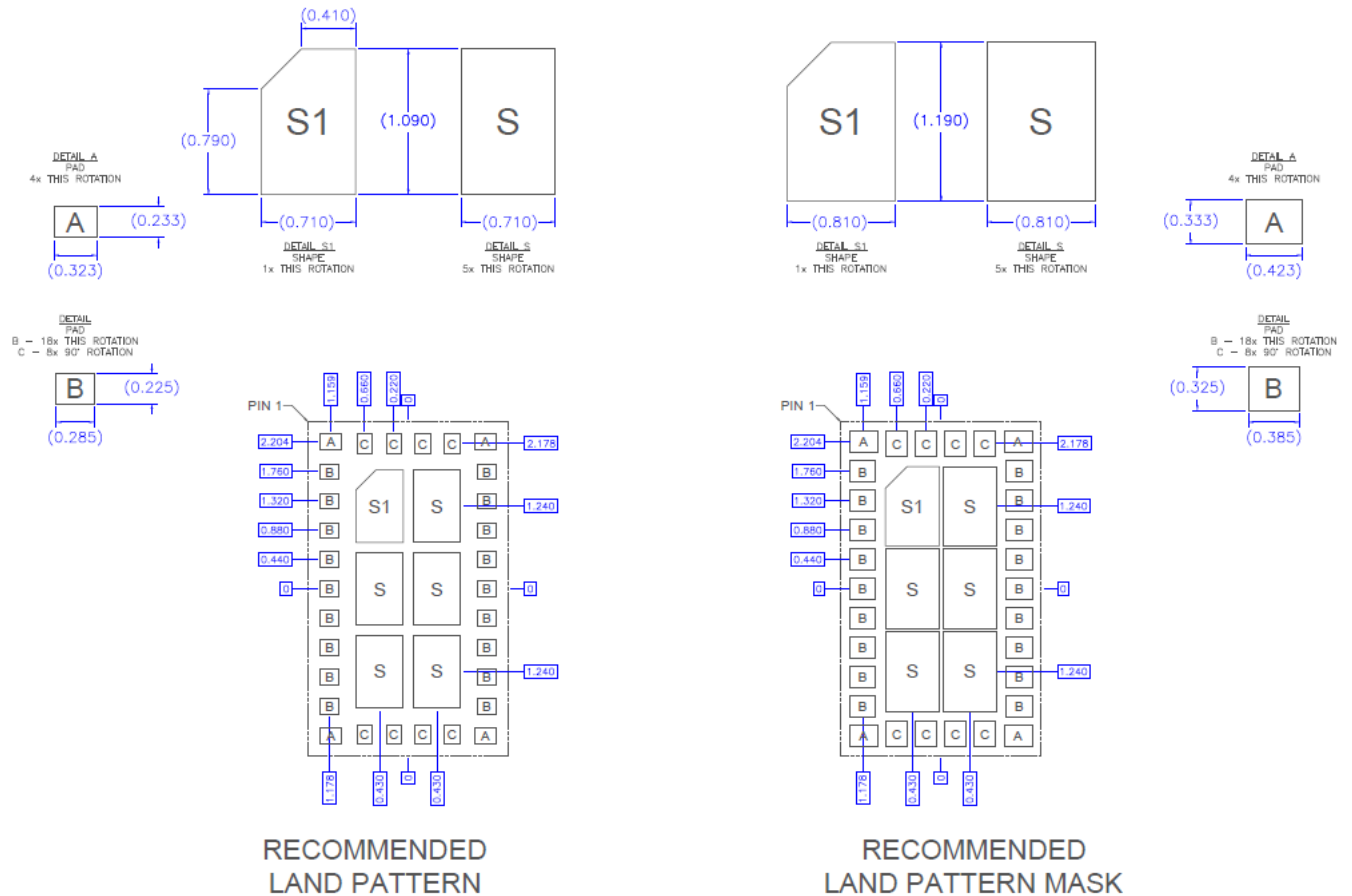


Pin 1 Indicator

Qorvo Logo - Use Q5D

Trace Code to be assigned by SubCon

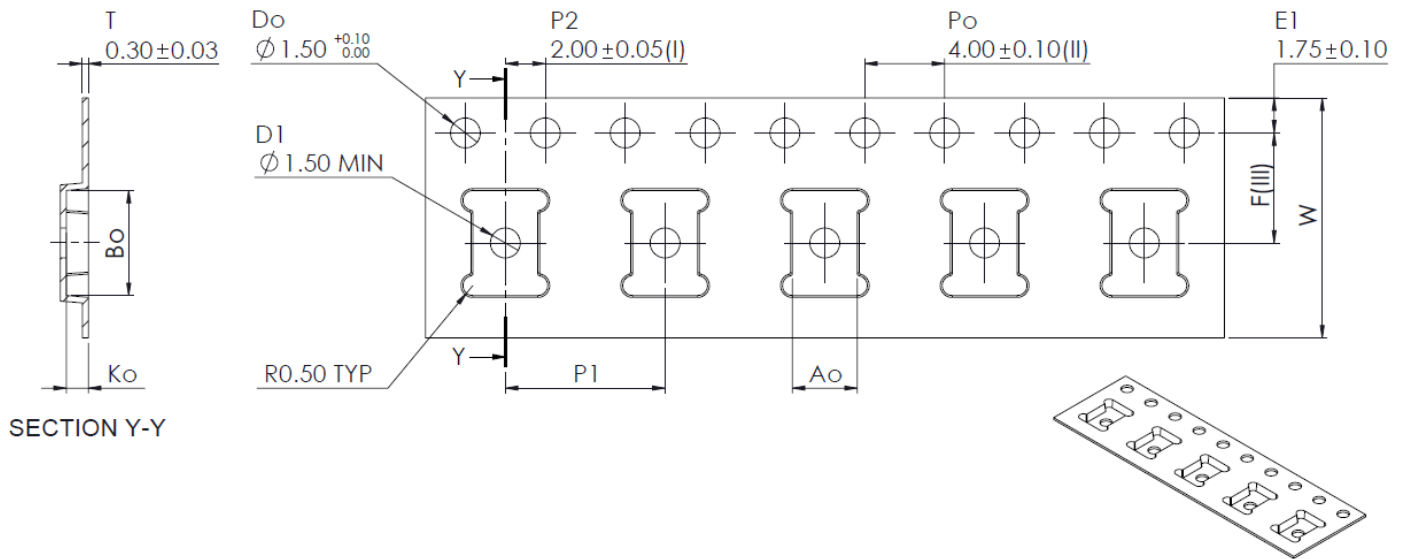
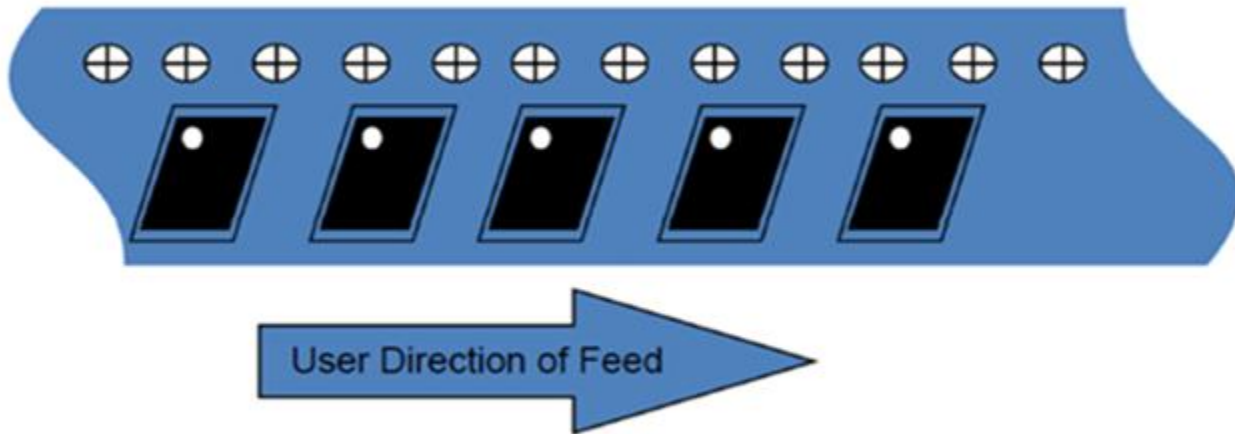
Mechanical Information – Recommended Land Pattern and Mask



RECOMMENDED
LAND PATTERN

RECOMMENDED
LAND PATTERN MASK

Tape and Reel Information – Carrier and Cover Tape Dimensions



SECTION Y-Y

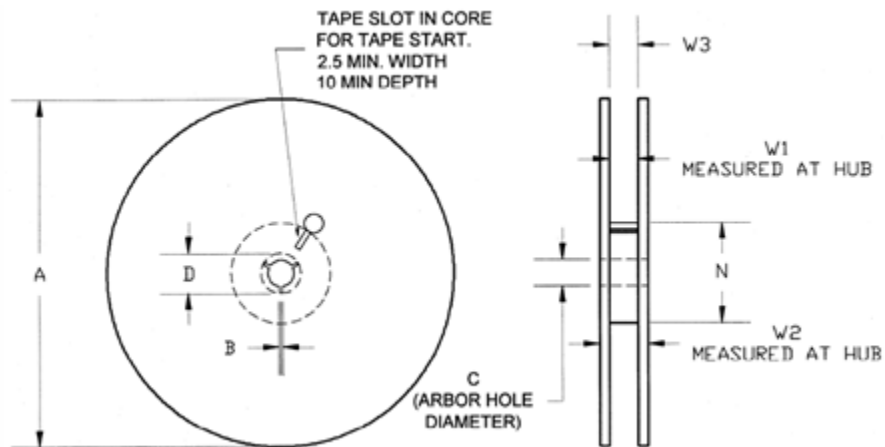
| | | |
|----|-------|---------------|
| Ao | 3.25 | +/- 0.05 |
| Bo | 5.25 | +/- 0.05 |
| Ko | 1.10 | +/- 0.05 |
| F | 5.50 | +/- 0.05 |
| P1 | 8.00 | +/- 0.10 |
| W | 12.00 | +0.30 / -0.10 |

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Tape and Reel Information – Reel Dimensions

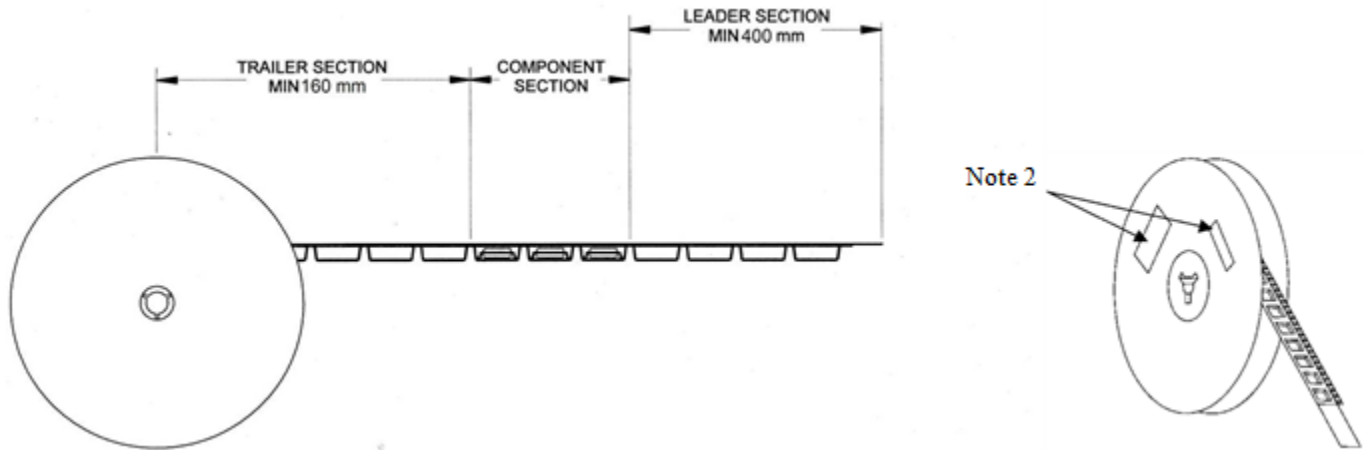
Packaging reels are used to prevent damage to devices during shipping and storage. Loaded carrier tape is typically wound onto a plastic take-up reel. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices. The reel size is either 7" or 13" in diameter based on the minimum number of samples. Standard T/R size = 5000 pieces on a 13" reel and 1000 pieces on a 7" reel.



| Packaging Reel for 12mm Wide Carrier Tape | | | 7" Reel | | 13" Reel | |
|---|----------------------|--------|-----------|-----------|-----------|-----------|
| PART | FEATURE | SYMBOL | SIZE (in) | SIZE (mm) | SIZE (in) | SIZE (mm) |
| FLANGE | DIAMETER | A | 6.969 | 177.0 | 12.992 | 330 |
| | THICKNESS | W2 | 0.717 | 18.2 | 0.717 | 18.2 |
| | SPACE BETWEEN FLANGE | W1 | 0.504 | 12.8 | 0.504 | 12.8 |
| HUB | OUTER DIAMETER | N | 2.283 | 58.0 | 4.016 | 102.0 |
| | ARBOR HOLE DIAMETER | C | 0.512 | 13.0 | 0.512 | 13.0 |
| | KEY SLIT WIDTH | B | 0.079 | 2.0 | 0.079 | 2.0 |
| | KEY SLIT DIAMETER | D | 0.787 | 20.0 | 0.787 | 20.0 |

Tape and Reel Information – Tape length and label placement

. Standard T/R size = 5000 pieces on a 13” reel and 1000 pieces on a 7” reel.



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
2. Labels are placed on a flange opposite the sprockets in the carrier tape.

Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|--|------------------------|
| ESD – Human Body Model (HBM) | All pins other than pin 8 Class 1C, Pin 8 Class1B | ESDA/JEDEC JS-001-2012 |
| ESD – Charged Device Model (CDM) | Class C2A | JEDEC JESD22-C101F |
| MSL – Moisture Sensitivity Level | MSL3 | IPC/JEDEC J-STD-020 |



Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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REVISION HISTORY

| Revision | Date | Description |
|----------|------------|-------------|
| F2 | 2020-01-23 | Baseline |