Dual-, Differential, Low-Pass Filter μModule with Gain and ADC Driver

Data Sheet

ADAQ8088

FEATURES

- **Dual-channel differential input/output**
- **Integrated 36 MHz, 8-pole low-pass filter**
- **Low power dissipation**
  - **213 mW typical at 3 V supply**
- **2 integrated fully differential ADC drivers**
- **30 dB maximum differential gain**
  - **Adjustable down to 14 dB**
  - **Gain error: ±0.2 dB**
  - **Gain drift: 0.01 dB/°C typical**
- **2.7 V to 3.3 V supply range**
- **84-ball, 6 mm × 12 mm CSP_BGA package with 0.8 mm ball pitch**
- **Operating temperature range: −40°C to +85°C**
- **Built-in supply decoupling capacitors**

APPLICATIONS

- **IF broadband demodulators**
- **Medical imaging (CW ultrasound beam forming)**
- **Phased array systems**
  - **Radar**
  - **Adaptive antennas**
- **Communications receivers**
- **Radio Links**
- **Wireless local loop**
- **IF broadband demodulators**
- **RF instrumentation**
- **Satellite modems**
- **Baseband data acquisition system**
  - **Multichannel digitizer instruments**
  - **Ultrasonic non-destructive test**

FUNCTIONAL BLOCK DIAGRAM

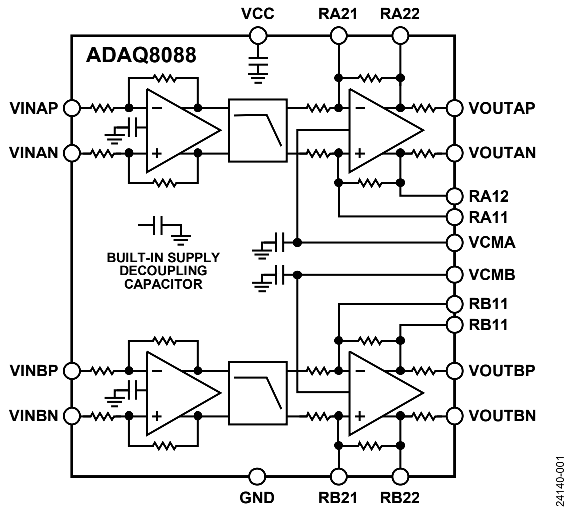

Figure 1.

GENERAL DESCRIPTION

The ADAQ8088 is a dual-channel analog system in package (SIP) that integrates three common signal processing and conditioning blocks to support a variety of demodulator applications and data acquisition applications. The device integrates all active and passive components to form a complete signal chain between the output of an I/Q demodulator and the input to an analog-to-digital converter (ADC). The device also forms the complete signal chain between a transducer output and the input to an ADC in baseband data acquisition systems. No external components are required for proper functionality.

Each channel contains a preamplifier, followed by an 8-pole, low-pass filter with a 36 MHz, 3 dB frequency and a differential ADC driver optimized to drive 12-bit to 14-bit pipeline ADCs with speeds up to 150 MSPS. Encapsulated in a 6 mm × 12 mm CSP_BGA package, the ADAQ8088 minimizes space requirements in high density multichannel systems.

The ADAQ8088 operating temperature range is from −40°C to +85°C.

Rev. 0

Document Feedback

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Technical Support
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REVISION HISTORY

2/2021—Revision 0: Initial Version

SPECIFICATIONS

VCC = 3.0 V, common-mode voltage (V_{CM}) floating, VINAP, VINAN, VINBP, and VINBN are self biased, differential 63 mV p-p input at 1 MHz, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Impedance	Each input to GND		249/1		Ω/pF
Open Circuit Voltage at V_{IN} Pins	VCC = 2.7 V		1.15		V dc
	VCC = 3.0 V		1.25		V dc
	VCC = 3.3 V		1.38		V dc
Input Current	Each input to GND, VCC = 2.7 V		−550		µA
	VCC = 3.0 V		−610		µA
	VCC = 3.3 V		−670		µA
Input Offset Current	Each input to GND, VCC = 2.7 V		±3.5		µA
	VCC = 3.0 V		±4.0		µA
	VCC = 3.3 V		±4.5		µA
Input Common-Mode Voltage Range		GND		VCC	V
Differential RTI Vos	Each input to GND, maximum = average + 4δ		+0.7		mV
V_{OS} Drift	T_A = −40°C to +85°C		7.5		µV/°C
DYNAMIC CHARACTERISTICS					
Bandwidth	V_{OUT} = 2 V p-p differential, R_L = 1 kΩ		36		MHz
Bandwidth Drift	T_A = -40°C to +85°C		0.1		MHz/°C
Total Harmonic Distortion (THD)			−63		dB
Slew Rate			180		V/µs
Differential Gain	With no external resistors		30		dB
Gain Error	Channel to channel, at 10 MHz		±0.2		dB
Gain Drift	T_A = -40°C to +85°C		0.01		dB/°C
Phase Match Error	Channel to channel, at 10 MHz		0.5		Degrees
OUTPUT CHARACTERISTICS					
Output Voltage					
High	R_L = 806 Ω, either output pin		2.15		V
Low	R_L = 806 Ω, either output pin		0.17		V
Output Short-Circuit Current			50		mA
Output Balance Error			−60		dB
Output Resistance	In series with each output		10		Ω
Crosstalk			80		dB
NOISE AND HARMONIC PERFORMANCE					
RTI Voltage Noise Density	At 1 MHz		7		nV/√Hz
	At 10 MHz		6		nV/√Hz
RTO Voltage Noise Density	Gain = 30 dB, f = 1 MHz		220		nV/√Hz
	Gain = 30 dB, f = 10 MHz		190		nV/√Hz
1/f Corner			20		kHz
V_{CM} CHARACTERISATICS					
V_{CM} Gain			1		V/V
V_{CM} Range		0.5		2	V
V_{CM} Input Resistance			18		kΩ
POWER SUPPLY					
Operating Range		2.7		3.3	V
Quiescent Current			71	88	mA
PSRR			70		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Analog Inputs	3.5 V
Supply Voltage	3.5 V
Storage Temperature Range	−55°C to +125°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020
Electrostatic Discharge (ESD) Ratings	500 V
Human Body Model (HBM)	2k V
Field Induced Charged Device Model	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA} (°C/W)	θ_{JC_TOP} (°C/W)	θ_{JC_BOTTOM} (°C/W)	θ_{JB} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)
BC-84-4	33	21.1	12.2	13.7	11	13

[1] Test Condition 1: Thermal impedance simulated values are based on use of a 2S2P with vias JEDEC PCB excluding the θ_{JCtop} which uses 1S0P JEDEC PCB.

Thermal resistance values specified in table 3 are simulated based on JEDEC specs (unless specified otherwise) and should be used in compliance with JESD51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADAQ8088
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VINAP	DNC	DNC	GND	DNC	DNC	GND	GND	VCMA	DNC	DNC	RA21	RA22	VOUTAP
B	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
C	VINAN	DNC	DNC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	DNC	RA11	RA12	VOUTAN
D	VINBP	DNC	DNC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	DNC	RB11	RB12	VOUTBP
E	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
F	WINBN	DNC	DNC	GND	DNC	DNC	GND	GND	VCMB	DNC	DNC	RB21	RB22	VOUTBN

NOTES
1. DNC = DO NOT CONNECT.

24140-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	VINAP	AI	Analog Input for Channel A.
A2, A3, A5, A6, A10, A11, C2, C3, C11, D2, D3, D11, F2, F3, F5, F6, F10, F11	DNC	DNC	Do Not Connect. Do not connect to these pins.
A4, A7, A8, B1 to B14 E1 to E14, F4, F7, F8	GND	P	Analog Ground.
A9	VCMA	AI	V_{CM} Input from the ADC.
A12, A13	RA21, RA22	AI	External Resistors for Channel A.
A14	VOUTAP	AO	Analog Output for Channel A.
C1	VINAN	AI	Analog Input for Channel A.
C4 to C10, D4 to D10	VCC	P	Power Supplies, 2.7 V to 3.3 V.
C12, C13	RA11, RA12	AI	External Resistors for Channel A.
C14	VOUTAN	AO	Analog Output for Channel A.
D1	VINBP	AI	Analog Input for Channel B.
D12, D13	RB11, RB12	AI	External Resistors for Channel B.
D14	VOUTBP	AO	Analog Output for Channel B.
F1	VINBN	AI	Analog Input for Channel B.
F9	VCMB	AI	V_{CM} Input from the ADC.
F12, F13	RB21, RB22	AI	External Resistors for Channel B.
F14	VOUTBN	AO	Analog Output for Channel B.

[1] AI is analog input, DNC is do not connect, P is power, and AO is analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 3 V; V_{CM} is floating, typically 1.25 V; R_{LOAD} = 1 kΩ ;T = 25°C, inputs and outputs are measured differentially, unless otherwise noted.

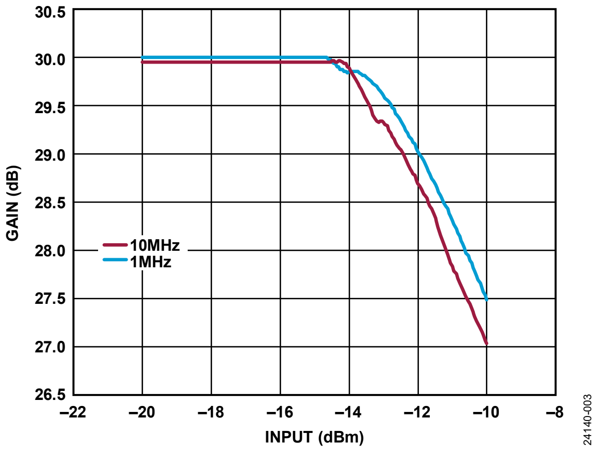


Figure 3. Gain vs. Input Power, Input Frequency at 1 MHz and 10 MHz

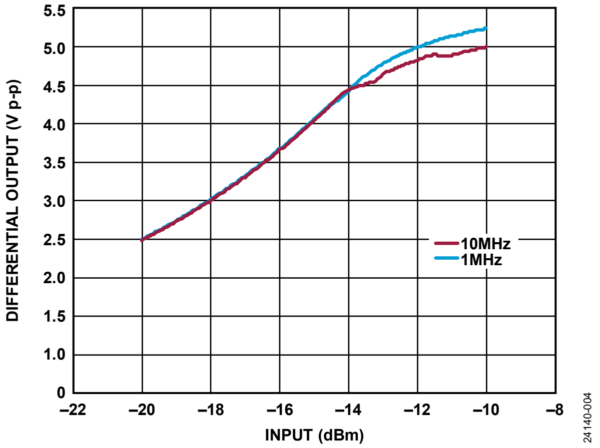


Figure 4. V_{OUT} vs. Input Power with Gain Set to 30 dB, Input Frequency at 1 MHz and 10 MHz

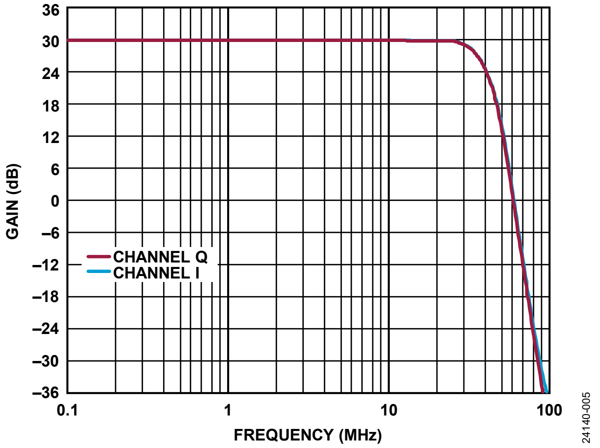


Figure 5. Frequency Response, Input = −20 dBm

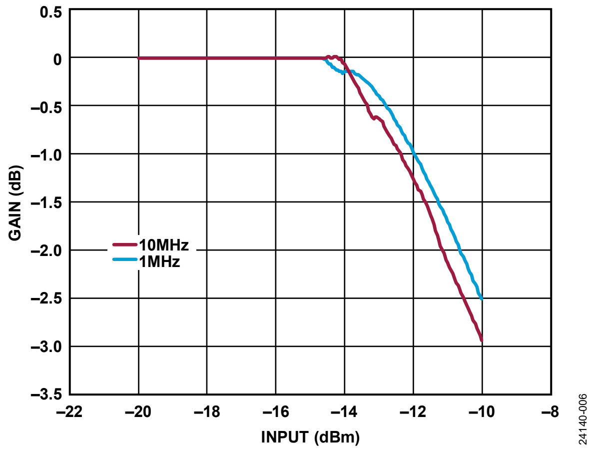


Figure 6. Normalized Gain vs. Input Power, Input Frequency at 1 MHz and 10 MHz

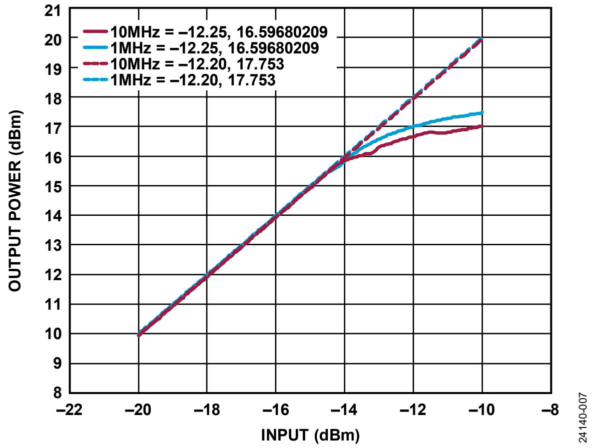


Figure 7. 1 dB Gain Compression with Gain Set to 30 dB, Input Frequency at 1 MHz and 10 MHz

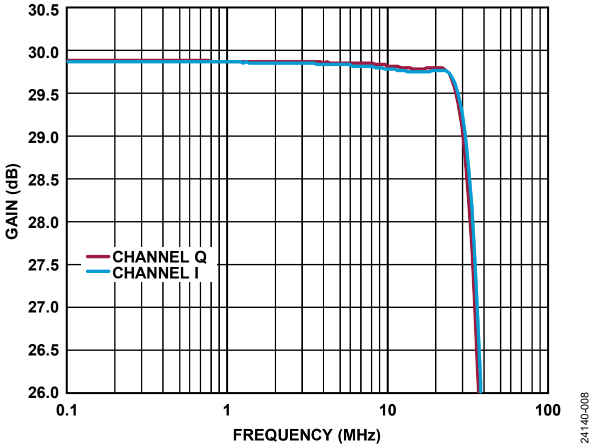


Figure 8. Gain Flatness, Input = −20 dBm

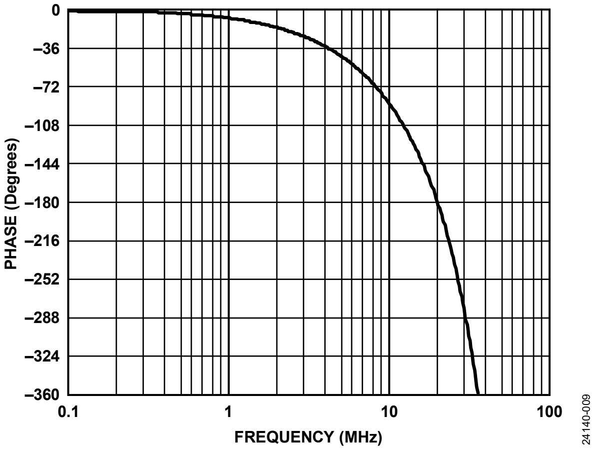


Figure 9. Phase Response with Gain Set to 30 dB, Input = −20 dBm

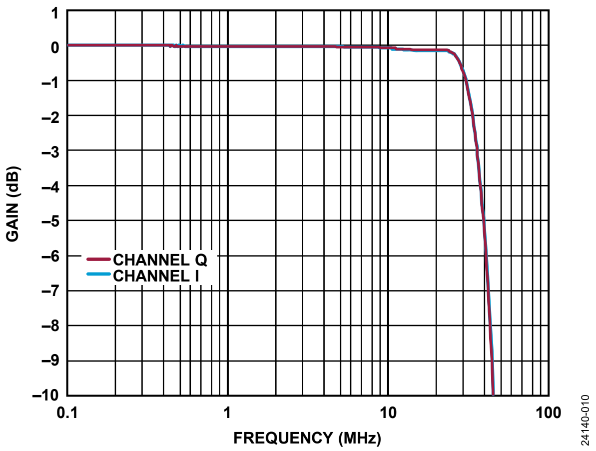


Figure 10. Normalized Frequency Response, Input = −20 dBm

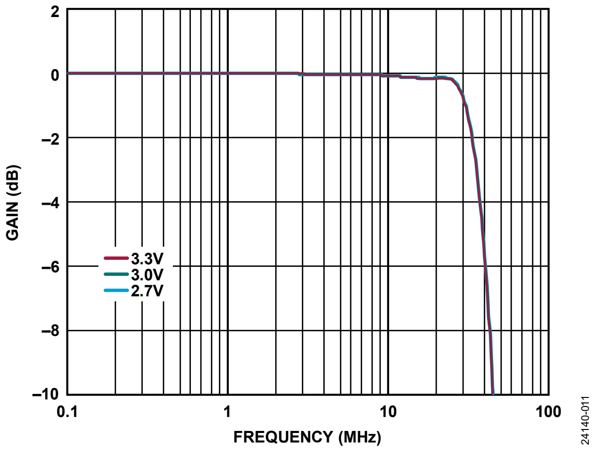


Figure 11. Frequency Response vs. Supply, Input = −20 dBm

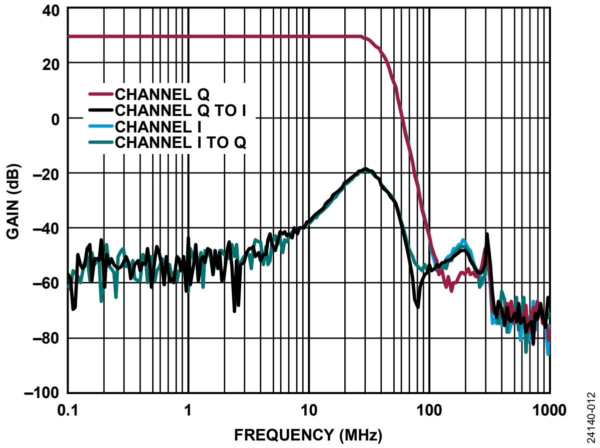


Figure 12. I/Q Channel Crosstalk

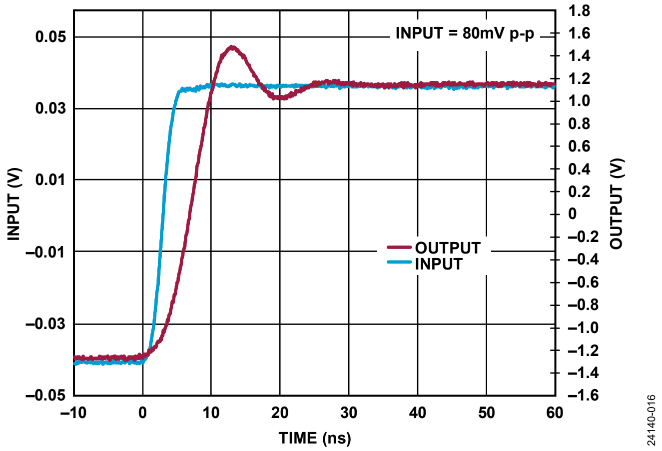


Figure 13. Step Response with Gain Set to 30 dB

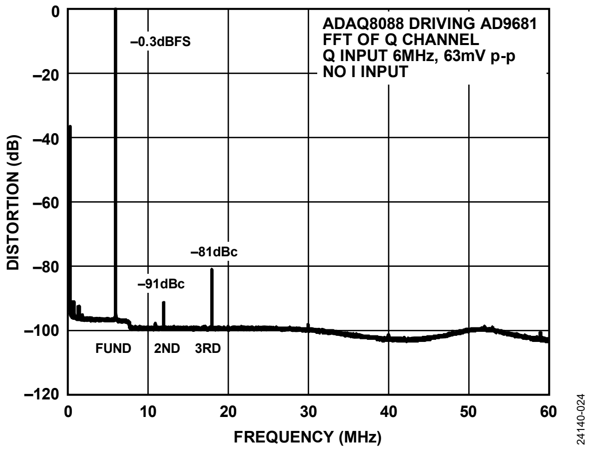


Figure 14. Distortion

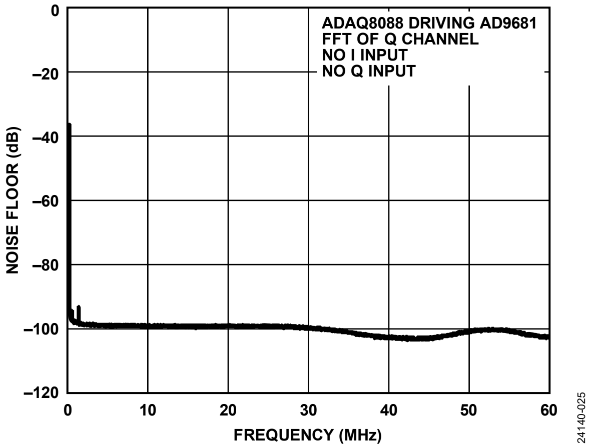


Figure 15. Noise Floor

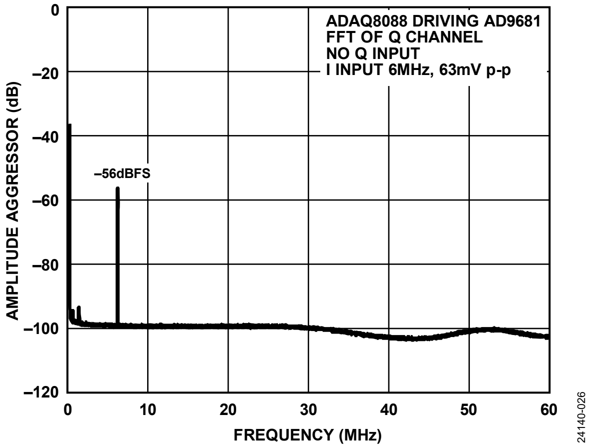


Figure 16. Amplitude Aggressor

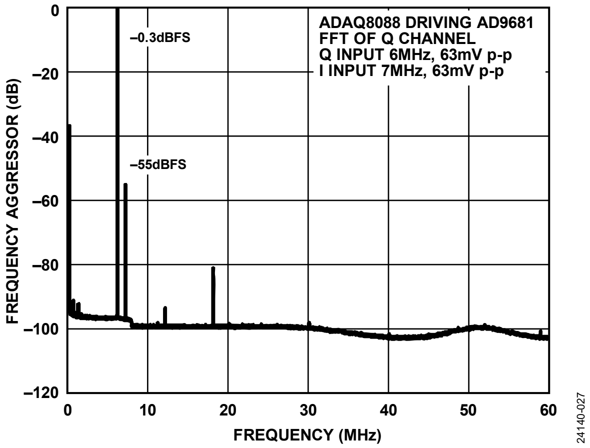


Figure 17. Frequency Aggressor

THEORY OF OPERATION

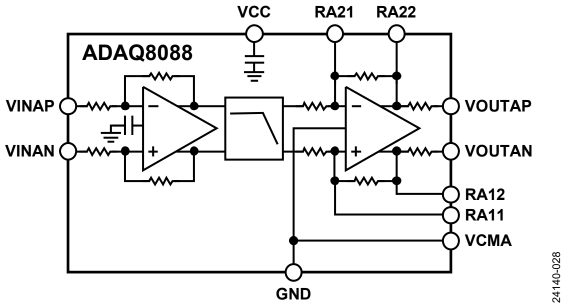


Figure 18. ½ ADAQ8088 Simplified Schematic

CIRCUIT INFORMATION

The ADAQ8088 system in package (SiP) is an analog signal chain designed to interface baseband I/Q from quadrature demodulators to 12-bit to 14-bit pipeline ADCs.

INPUT RESISTANCE

The equivalent input impedance of each input of the ADAQ8088 is a 249 Ω resistor connected to VCC/2.

Each baseband output of the demodulator is loaded with the input impedance of the ADAQ8088. To avoid saturating the ADAQ8088 inputs, ac couple demodulators with high dc bias on the I/Q outputs to the ADAQ8088.

LOW PASS FILTER

An 8-pole Butterworth low-pass filter provides steep roll-off beyond the filter corner frequency of 36 MHz typical.

NOISE

Input referred broad band noise density of the ADAQ8088 is

6 nV/√Hz

1/f corner is located at 20 kHz.

OUTPUT STAGE

The output stage is optimized to drive 12-bit to 14-bit pipeline ADCs with speeds of 150 MSPS or lower.

The output resistance of the ADAQ8088 is set to 10 Ω. Additional resistors in series with each output and a differential capacitor placed as close to the ADC inputs as possible provides additional filtering.

DC bias of the outputs is set by the voltage on the VCMA pin and the VCMB pin. Floating these pins self adjusts the outputs to 1.25 V (internally biased). Additionally, these pins are typically connected to the chosen ADC V_{CM} output pin.

RESOLUTION

Two 15 Ω resistors, each in series with an output pin of the ADAQ8088 and a 10 pF capacitor across the ADC input pins, allows just over a 10-bit effective resolution at full-scale input for an ADC with a 4 ns acquisition time.

The 190 nV/√Hz RTO noise density of the ADAQ8088 at a gain value of 30 dB, integrated over the 36 MHz signal bandwidth, allows an effective signal resolution of 9 bits which is suitable for a 10-bit ADC with 2 V p-p FS analog input.

Reducing the gain to 20 dB increases the effective resolution to 10.5 bits in an ADC with 2 V p-p FS analog input.

POWER SUPPLY DECOUPLING

The ADAQ8088 features built in, 0.1 µF supply decoupling capacitors on VCC.

GAIN

With no external component, the gain of the ADAQ8088 is set to 30 dB. This gain can be reduced with external resistors (R_{EXT}) connected between the following pins: RA11 and RA12, RA21 and RA22, RB11 and RB12, and RB21 and RB22.

The maximum gain is 30 dB with no resistors. The minimum gain is 14 dB when R_{EXT} = 110 Ω. Figure 19 shows the gain vs. R_{EXT} value.

Gain can be further reduced by a factor of 249/(249 + R) with external resistors connected in series with each input.

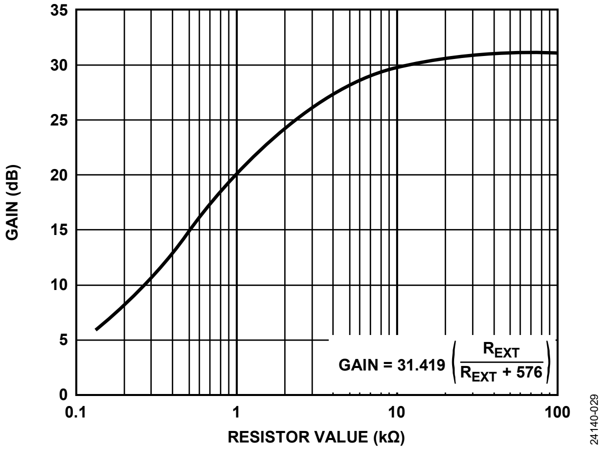


Figure 19. Gain vs. External Resistor Value

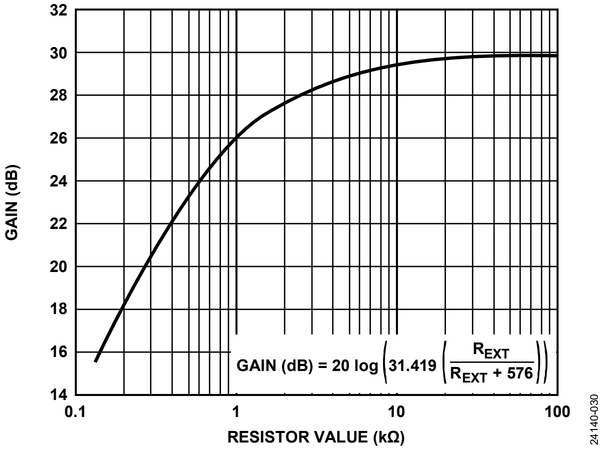


Figure 20. Gain (dB) vs. External Resistor Value

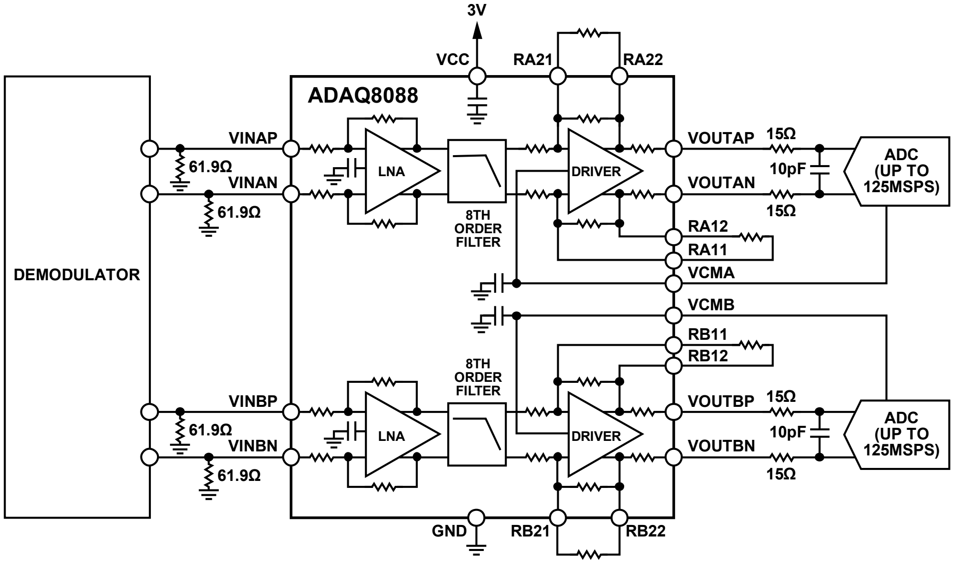
APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 21 shows an example of how the ADAQ8088 can be directly coupled to a demodulator. Place the 61.9 Ω resistors close to the ADAQ8088 input pins. The parallel combination of the resistors and the 249 Ω input impedance of the ADAQ8088 provides a 50 Ω termination for the demodulator outputs. If the ADC is located physically some distance from the ADAQ8088 and is driven with a transmission line, place the 40.2 Ω series resistors close to the ADAQ8088 output pins. These resistors, along with the device internal impedance, provide a 50 Ω series termination. The value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

Figure 22 shows an example of how the ADAQ8088 can be used as part of an ultrasonic non-destructive test.

Figure 23 shows an example of how the ADAQ8088 works on high accuracy, wide bandwidth, multichannel digitizer instruments.



RA1, RA1, RB1, RB2

DNI FOR 30dB GAIN
267Ω FOR 20dB GAIN

24140-031

Figure 21. ADAQ8088 Direct Coupled to Demodulator, Driving 12-Bit to 14-Bit ADCs with Speeds up to 150 MSPS

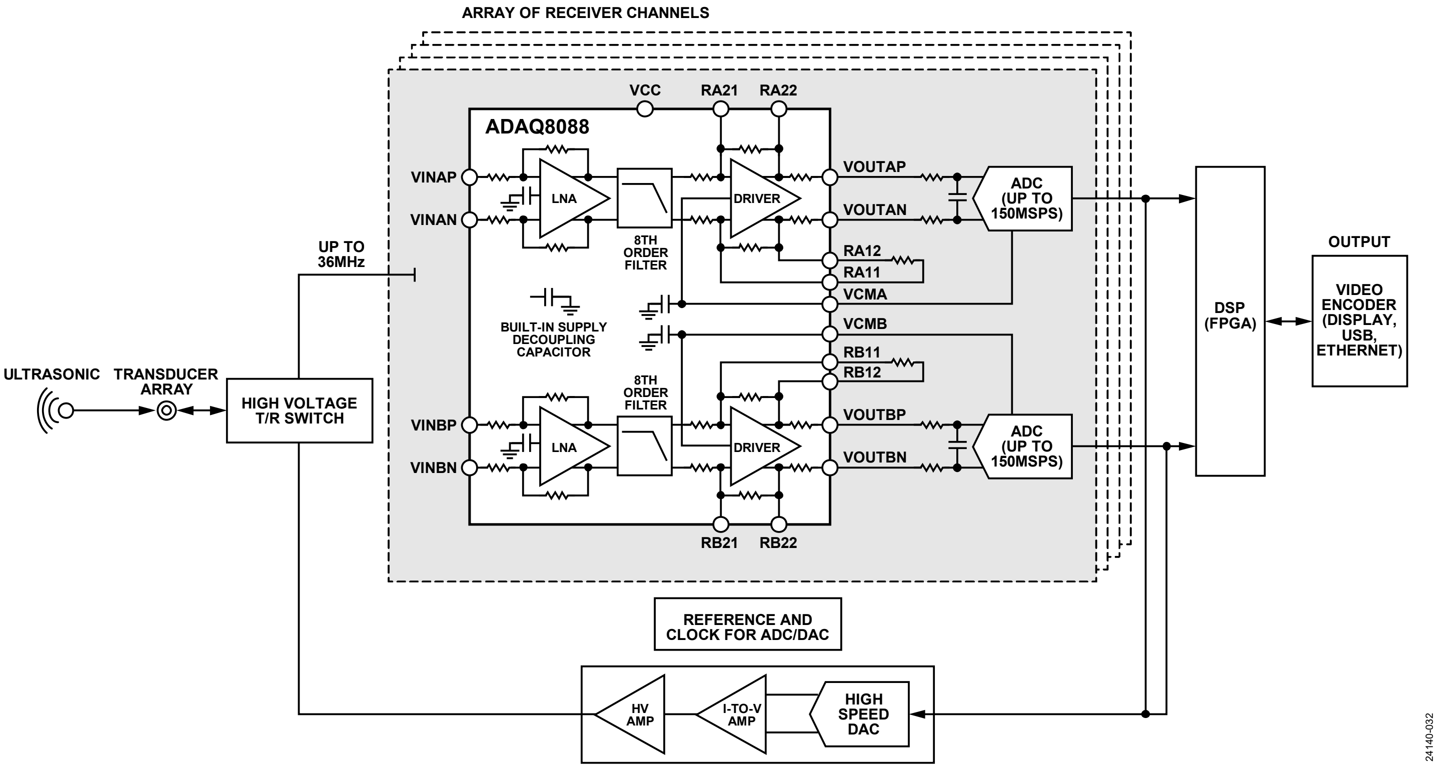


Figure 22. Ultrasonic Non-Destructive Test

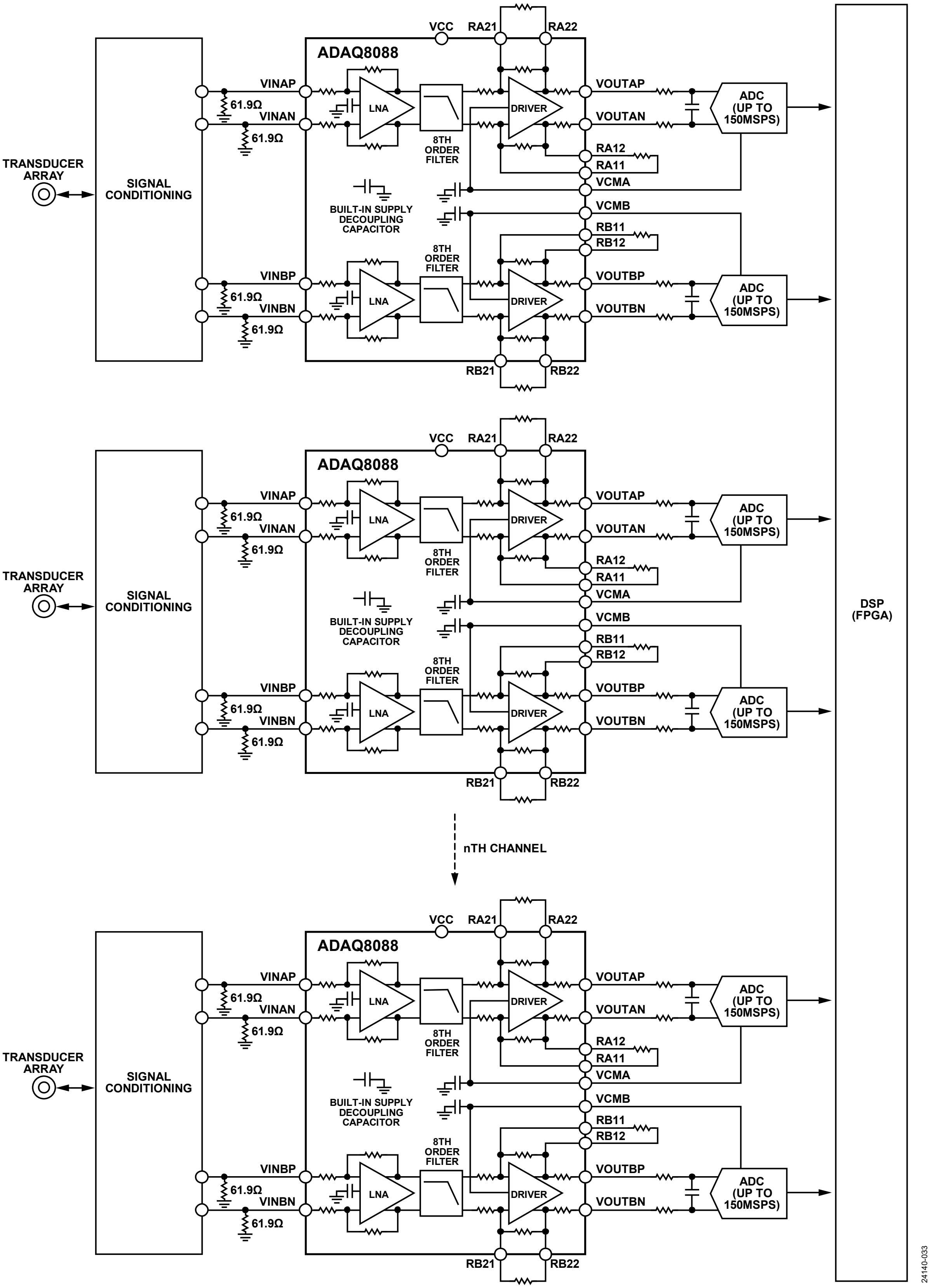


Figure 23. Multichannel Digitizer Instrument

OUTLINE DIMENSIONS

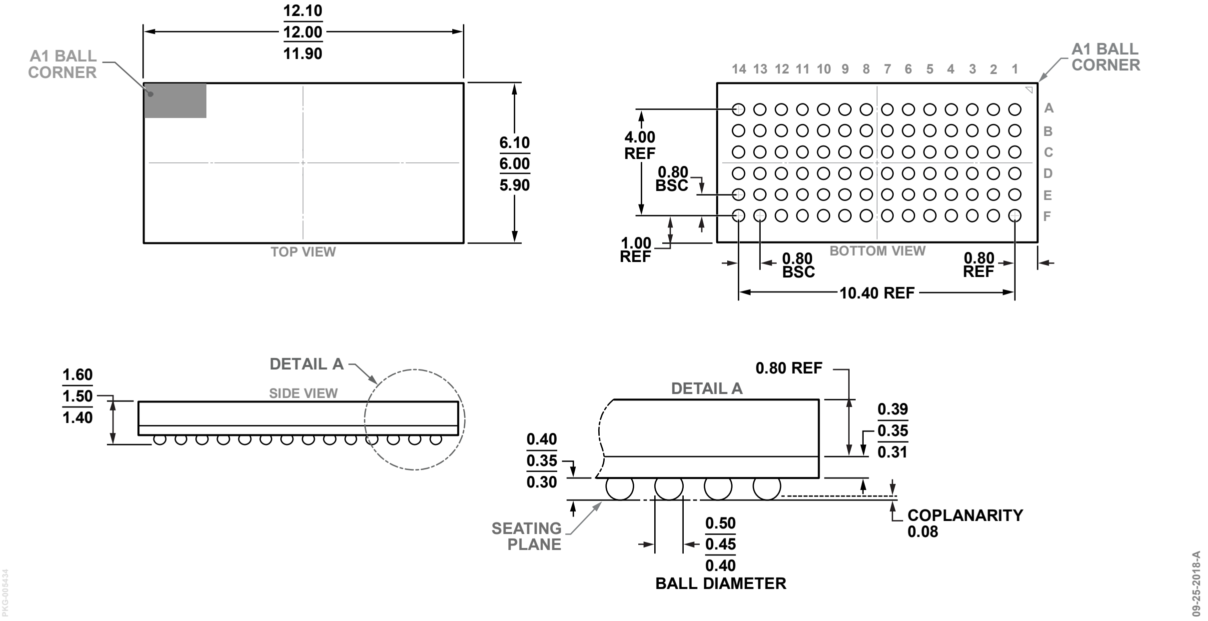


Figure 24. 84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-84-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Ordering Quantity	Package Description	Package Option
ADAQ8088BBCZ	−40°C to +85°C	Tray, 280	84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-84-4

[1] Z = RoHS Compliant Part.