# Die-On-Carrier, Silicon SPDT Switch 100 MHz to 60 GHz

Preliminary Technical Data

# ADRF5424

## FEATURES

- Ultrawideband frequency range: 100 MHz to 60 GHz
- Reflective design
- Bond pads for wire-bond and ribbon-bond
- Low insertion loss
  - 0.8 dB typical to 18 GHz
  - 1.2 dB typical to 44 GHz
  - 1.8 dB typical to 55 GHz
- High input linearity
  - P1dB: TBD dBm typical
  - IP3: 50 dBm typical
- High RF input power handling
  - Through path: 27 dBm to 40 GHz
  - Hot switching: 27 dBm to 40 GHz
- No low frequency spurious
- RF settling time (50% $V_{CTRL}$ to 0.1 dB of final RF output): 17 ns
- 14-terminal bond pads, 2.5 mm x 2.6 mm, Die-on-carrier

## APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

## FUNCTIONAL BLOCK DIAGRAM

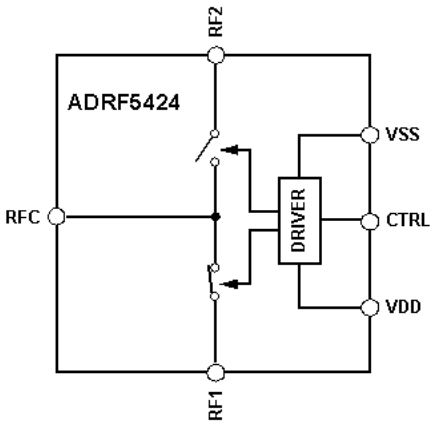


*Figure 1.*

## GENERAL DESCRIPTION

The ADRF5424 is a reflective, single-pole double-throw (SPDT) switch manufactured in a silicon process attached on a GaAs carrier substrate. The substrate incorporates the bond pads for chip-and-wire assembly and the device bottom is metalized, connected to ground.

This device operates from 100 MHz to 60 GHz with better than 1.8 dB of insertion loss and 35 dB of isolation at 55 GHz. The ADRF5424 has a radio frequency (RF) input power handling capability of 27 dBm up to 40 GHz for both the through path and hot switching.

The ADRF5424 draws a low current of 14 µA on the positive supply of +3.3 V and 120 µA on negative supply of −3.3 V. The device features complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5424 RF ports are designed to match a characteristic impedance of 50 Ω.

Rev. PrD


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# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

$V_{DD}$ = 3.3 V, $V_{SS}$ = −3.3 V, $V_{CTRL}$ = 0 V or $V_{DD}$, and die temperature ($T_{DIE}$)[1] = 25°C for 50 Ω system, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | f | | 100 | | 60,000 | MHz |
| INSERTION LOSS | | | | | | |
| Between RFC and RF1/RF2 (On) | | 100 MHz to 18 GHz | | 0.8 | | dB |
| | | 18 GHz to 26 GHz | | 1.0 | | dB |
| | | 26 GHz to 44 GHz | | 1.2 | | dB |
| | | 44 GHz to 55 GHz | | 1.8 | | dB |
| | | 55 GHz to 60 GHz | | 2.2 | | dB |
| RETURN LOSS | | | | | | |
| RFC and RF1/RF2 (On) | | 100 MHz to 18 GHz | | 13 | | dB |
| | | 18 GHz to 44 GHz | | 12 | | dB |
| | | 44 GHz to 55 GHz | | 12 | | dB |
| | | 55 GHz to 60 GHz | | 12 | | dB |
| ISOLATION | | | | | | |
| Between RFC and RF1/RF2 or | | 100 MHz to 18 GHz | | 44 | | dB |
| Between RF1 and RF2 | | 18 GHz to 44 GHz | | 35 | | dB |
| | | 44 GHz to 55 GHz | | 35 | | dB |
| | | 55 GHz to 60 GHz | | 30 | | dB |
| SWITCHING CHARACTERISTICS | | | | | | |
| Rise and Fall Time | $t_{RISE}$, $t_{FALL}$ | 10% to 90% of RF output | | 2 | | ns |
| On and Off Time | $t_{ON}$, $t_{OFF}$ | 50% $V_{CTRL}$ to 90% of RF output | | 10 | | ns |
| RF Settling Time | | | | | | |
| 0.1 dB | | 50% $V_{CTRL}$ to 0.1 dB of final RF output | | 17 | | ns |
| 0.05 dB | | 50% $V_{CTRL}$ to 0.05 dB of final RF output | | 22 | | ns |
| INPUT LINEARITY[2] | | 200 MHz to 40 GHz | | | | |
| 1 dB Power Compression | P1dB | | | TBD | | dBm |
| Third-Order Intercept | IP3 | Two tone input power = 12 dBm each tone, Δf = 1 MHz | | 50 | | dBm |
| SUPPLY CURRENT | | $V_{DD}$ and $V_{SS}$ pads | | | | |
| Positive Supply Current | $I_{DD}$ | | | 14 | | µA |
| Negative Supply Current | $I_{SS}$ | | | 120 | | µA |
| DIGITAL CONTROL INPUTS | | CTRL pad | | | | |
| Voltage | | | | | | |
| Low | $V_{INL}$ | | 0 | | 0.8 | V |
| High | $V_{INH}$ | | 1.2 | | 3.3 | V |
| Current | | | | | | |
| Low and High | $I_{INL}$, $I_{INH}$ | | | <1 | | µA |
| RECOMMENDED OPERATING CONDITONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | $V_{DD}$ | | 3.15 | | 3.45 | V |
| Negative | $V_{SS}$ | | −3.45 | | −3.15 | V |
| Digital Control Voltage | $V_{CTRL}$ | | 0 | | $V_{DD}$ | V |
| RF Input Power[3] | $P_{IN}$ | f = 200 MHz to 40 GHz, $T_{DIE}$[1] = 85°C[4] | | | | |
| Through Path | | RF signal is applied to RFC or through connected RF1/RF2 | | | 27 | dBm |
| Hot Switching | | RF signal is present at RFC while switching between RF1 and RF2 | | | 27 | dBm |
| Die Temperature[1] | $T_{DIE}$[1] | | -40 | | +105 | °C |

[1] $T_{DIE}$ refers to the bottom of the die-on-carrier.
[2] For input linearity performance over frequency, see Figure 14 to Figure 17.
[3] For power derating over frequency, see Figure 2 and Figure 3.
[4] For 105°C operation, the power handling degrades from the $T_{DIE}$ = 85°C specification by 3 dB.

# ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

**Table 2.**

| Parameter | Rating |
|---|---|
| Positive Supply Voltage | −0.3 V to +3.6 V |
| Negative Supply Voltage | −3.6 V to +0.3 V |
| Digital Control Input Voltage | |
| Voltage | −0.3 V to $V_{DD}$ + 0.3 V |
| Current | 3 mA |
| RF Input Power (f = 200 MHz to 40 GHz, $T_{DIE}$ = 85°C[1]) | |
| Through Path | 27.5 dBm |
| Hot Switching | 27.5 dBm |
| RF Input Power Under Unbiased Condition[2] ($V_{DD}$, $V_{SS}$ = 0 V) | 21 dBm |
| Temperature | |
| Junction, $T_J$ | 135°C |
| Storage Range | −65°C to +150°C |
| Epoxy Cure | 170°C |
| ESD Sensitivity | |
| Human Body Model (HBM) | |
| RFC, RF1, and RF2 Pads | 500 V |
| Digital Pads | 2000 V |

[1] For 105°C operation, the power handling degrades from the $T_{DIE}$ = 85°C specification by 3 dB.
[2] For power derating vs. frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path and hot switching power specifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case bottom (channel to die-on-carrier package bottom) thermal resistance.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JC}$ | Unit |
|---|---|---|
| C-14-8, Through Path | 352 | °C/W |

## POWER DERATING CURVES

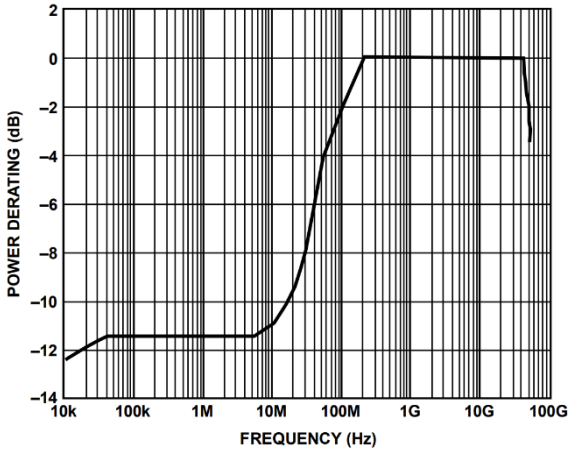


*Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{DIE}$ = 85°C*

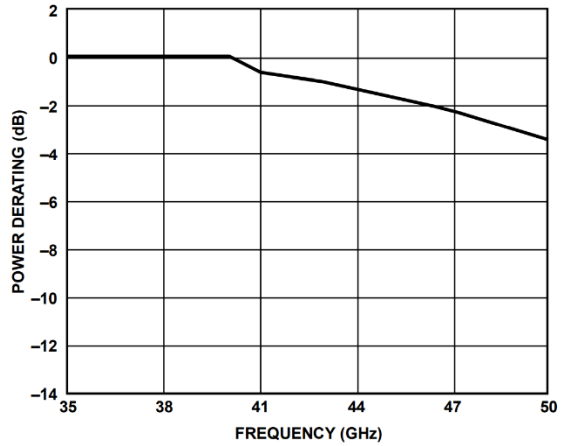


*Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{DIE}$ = 85°C*

## DIE-ON-CARRIER DEVICE CONSTRUCTION AND TEMPERATURE CYCLE RELIABILITY

CAUTION: Users must qualify their assemblies against the end use conditions. Guidance in IPC-9701A and IPC-SM-785 can be followed for accelerated test conditions in different end applications. Users may apply conformal coating or underfill to mitigate stress and strain in their assemblies, however the impact on performance needs to be validated. As both dies are attached with solder joints, users must follow best practices for the thermo-mechanical design of their module assemblies. The temperature expansion coefficient of the substrate material has to match the thermal expansion coefficient of the GaAs and Si die; warpage or other mechanical deformation on the substrate should not be allowed. The die attach-process and the epoxy cure temperatures should be set to lower the accumulated stress after assembly. ADI qualified the die-on-carrier parts per Jedec JESD22-A104F on "stand alone" units, not mounted on a substrate. Contact ADI for experimental results and best practices with regard to material selection for mounting components on a substrate.

The construction of a Die-On-Carrier part is depicted in the Figure 4. A Si die on top side is face-to-face attached to a GaAs die on the bottom side. The Si and GaAs dies incorporate SnAg plated Cu pillars individually that are designed to match and mate on the other die. After accurate placement and alignment, both dies are attached with a reflow process. The SnAg solder joint is the only structure keeping both dies attached, no underfills or other adhesives are applied. The GaAs die incorporate through wafer vias to carry the GND return signals from the RF substrate on the bottom side when attached using a conductive epoxy on the RF substrate. The GaAs die works as the carrier for the complete structure after assembly.

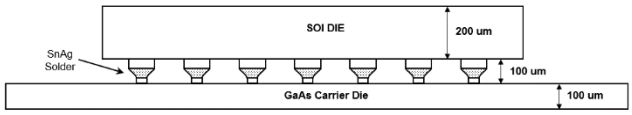


*Figure 4. Die-On-Carrier Construction*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

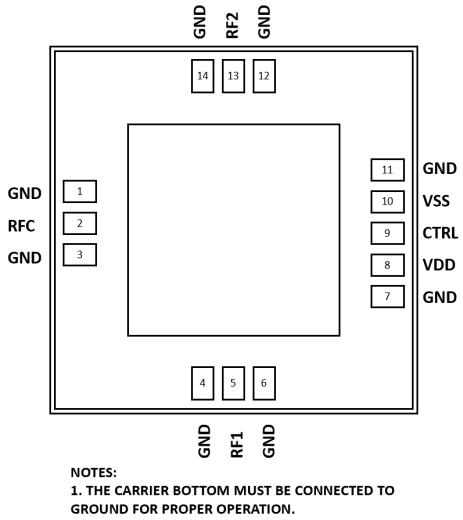


*Figure 5. Pad Configuration (Top View)*

**Table 4. Pad Function Descriptions**

| Pad No. | Mnemonic | Description |
|---|---|---|
| 1, 3, 4, 6, 7, 11, 12, 14 | GND | Ground. Bonding of these ground pads are optional. See Application section. |
| 2 | RFC | RF Common Port. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic. |
| 5 | RF1 | RF Port 1. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic. |
| 8 | VDD | Positive Supply Voltage. See Figure 7 for the interface schematic. |
| 9 | CTRL | Control Input Voltage. See Figure 8 for the interface schematic. |
| 10 | VSS | Negative Supply Voltage. See Figure 9 for the interface schematic. |
| 13 | RF2 | RF Port 2. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic. |
| | Carrier Bottom | The carrier bottom is gold metallized and must be attached directly to the ground plane using conductive epoxy. |

## INTERFACE SCHEMATICS

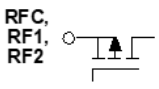


*Figure 6. RFC, RF1, RF2 Interface Schematic*

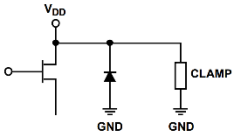


*Figure 7. VDD Interface Schematic*

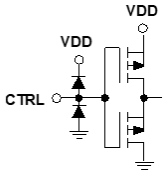


*Figure 8. CTRL Interface Schematic*

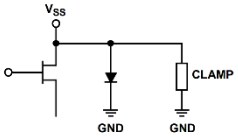


*Figure 9. VSS Interface Schematic*

# TYPICAL PERFORMANCE CHARACTERISTICS

## INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD}$ = 3.3 V, $V_{SS}$ = −3.3 V, $V_{CTRL}$ = 0 V or $V_{DD}$, and $T_{DIE}$ = 25°C, and a 50 Ω system, unless otherwise noted. S-parameters are measured with microstrip launchers and 2-mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are de-embedded.

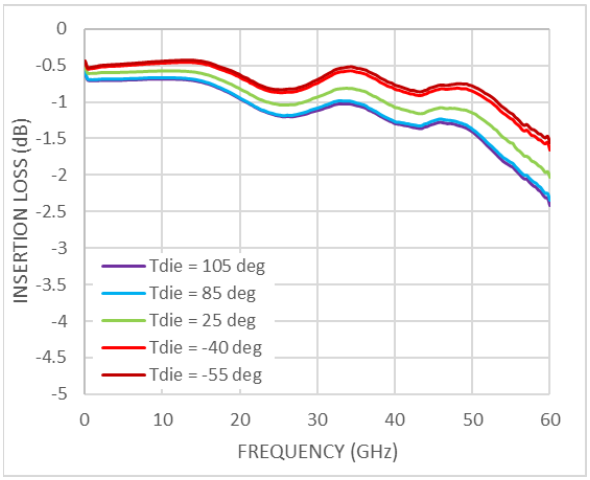


*Figure 10. Insertion Loss vs. Frequency over temperature*

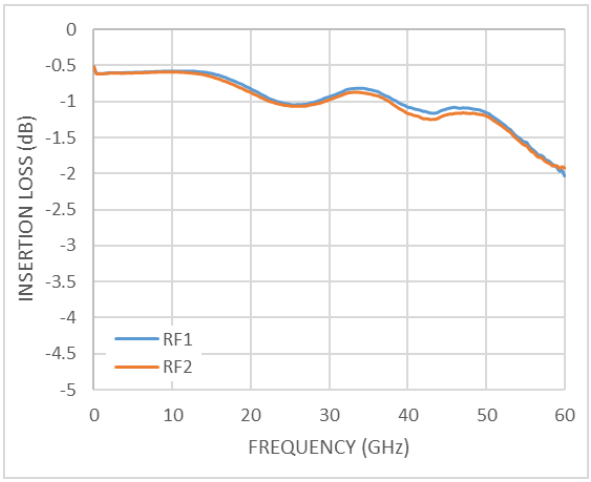


*Figure 12. Insertion Loss vs. Frequency for RF1 and RF2*

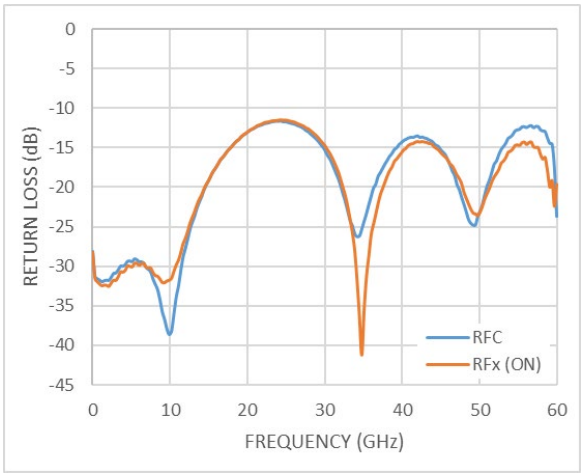


*Figure 11. Return Loss vs. Frequency for RFC and RFx (On)*

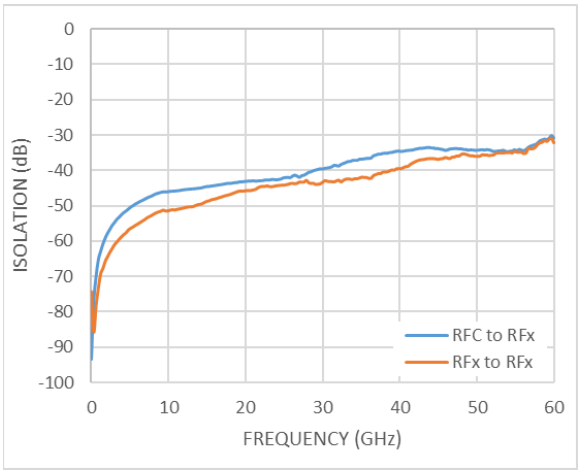


*Figure 13. Isolation vs. Frequency*

## INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD}$ = 3.3 V, $V_{SS}$ = −3.3 V, $V_{CTRL}$ = 0 V or $V_{DD}$, and $T_{DIE}$ = 25°C for a 50 Ω system, unless otherwise noted.

TBD

*Figure 14. Input P1dB vs. Frequency*

TBD

*Figure 16. Input P1dB vs. Frequency (Low Frequency Detail)*

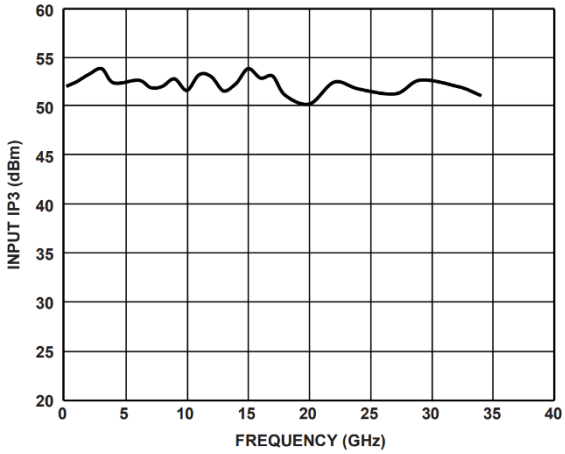


*Figure 15. Input IP3 vs. Frequency*

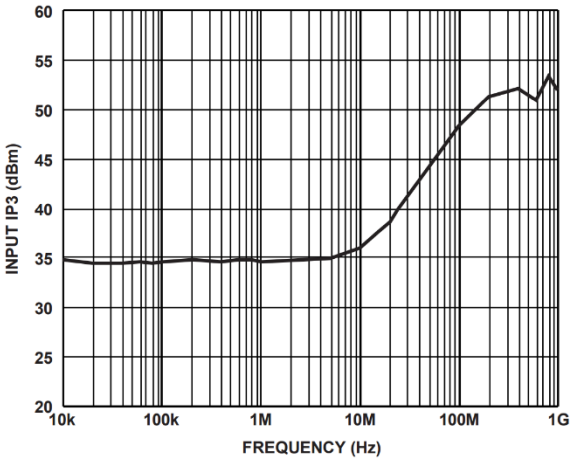


*Figure 17. Input IP3 vs. Frequency (Low Frequency Detail)*

# THEORY OF OPERATION

The ADRF5424 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS/LVTTL-compatible control interface. This driver features a single digital control input pad, CTRL. The logic level applied to the CTRL pad determines which RF port is in the insertion loss state and in the isolation state (see Table 5). The unselected RF port of the ADRF5424 is reflective. The isolation path provides high isolation between the unselected port and the insertion loss path.

## RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

## POWER SUPPLY

The ADRF5424 requires a positive supply voltage applied to the VDD pad and a negative supply voltage applied to the VSS pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect to GND.
2. Power up the VDD and VSS voltages. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs before the VDD voltage supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the VDD voltage is powered up and the control pads are not driven to a valid logic state.
4. Apply an RF input signal to RFC, RF1, or RF2.

The ideal power-down sequence is the reverse order of the power-up sequence.

**Table 5. Control Voltage Truth Table**

| | RF Path | |
|---|---|---|
| **Digital Control Input ($V_{CTRL}$)** | **RF1 to RFC** | **RF2 to RFC** |
| Low | Isolation (off) | Insertion loss (on) |
| High | Insertion loss (on) | Isolation (off) |

# APPLICATIONS INFORMATION

## ASSEMBLY DIAGRAM

An assembly diagram of the ADRF5424 is shown in Figure 18.

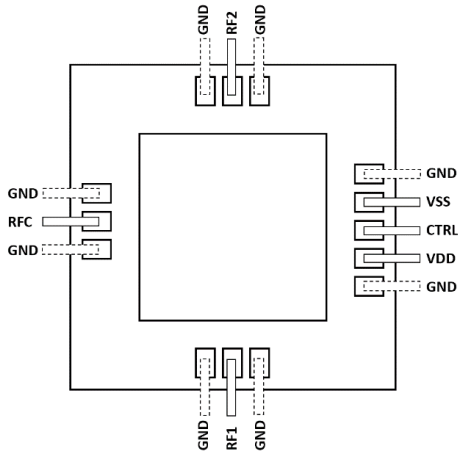


*Figure 18. Die Assembly Diagram*

## MOUNTING AND BONDING TECHNIQUES

The part is designed to have the optimum RF input and output impedance match with 2 mil x 0.5 mil gold ribbon wire and typical 3 mil loop height. Bonding diagram is shown in Figure 19 and Figure 20. Alternatively, using multiple wire bonds with equivalent inductance will yield similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad as the device is designed to match internally the recommended ribbon bond-wire. A spacing of 3 mils from RF transmission line to device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The DC pads are big enough also to accommodate ribbon bods if preferred.

The device is metallized on the backside and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

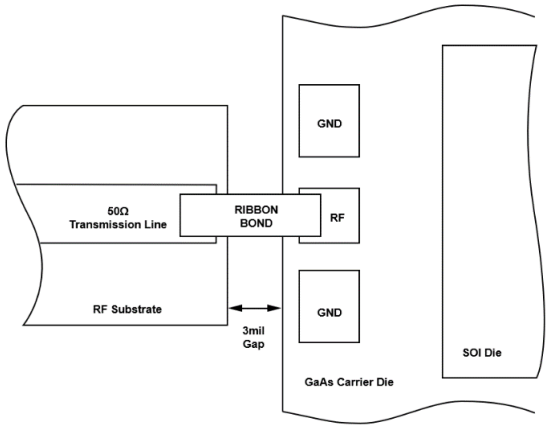


*Figure 19. Bonding Diagram-Top View*

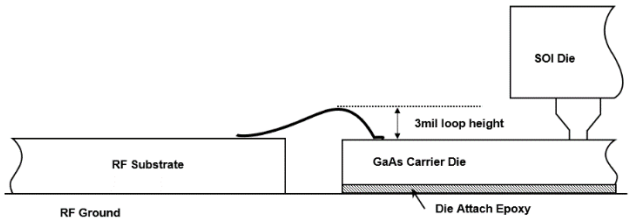


*Figure 20. Bonding Diagram-Side View*

### *Wire Bonding*

RF bonds using ribbon wire must be thermo-sonically bonded a nominal stage temperature of 150°C and apply a minimum amount of ultrasonic energy to achieve reliable bonds.

### *Handling, Mounting and Epoxy Die Attach*

Keep devices in ESD protective sealed bags for shipment and store all bared die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs parts, however for die-on-carrier devices using a vacuum tool is recommended to avoid any damage on the device substrate. Handle parts in clean environment and do not attempt to clean using liquid cleaning systems.

For epoxy die is attached, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Epoxy cure temperatures should be set per the manufacturer's recommendations taking into account the device maximum ratings and also to lower the accumulated mechanical stress after assembly.

# OUTLINE DIMENSIONS

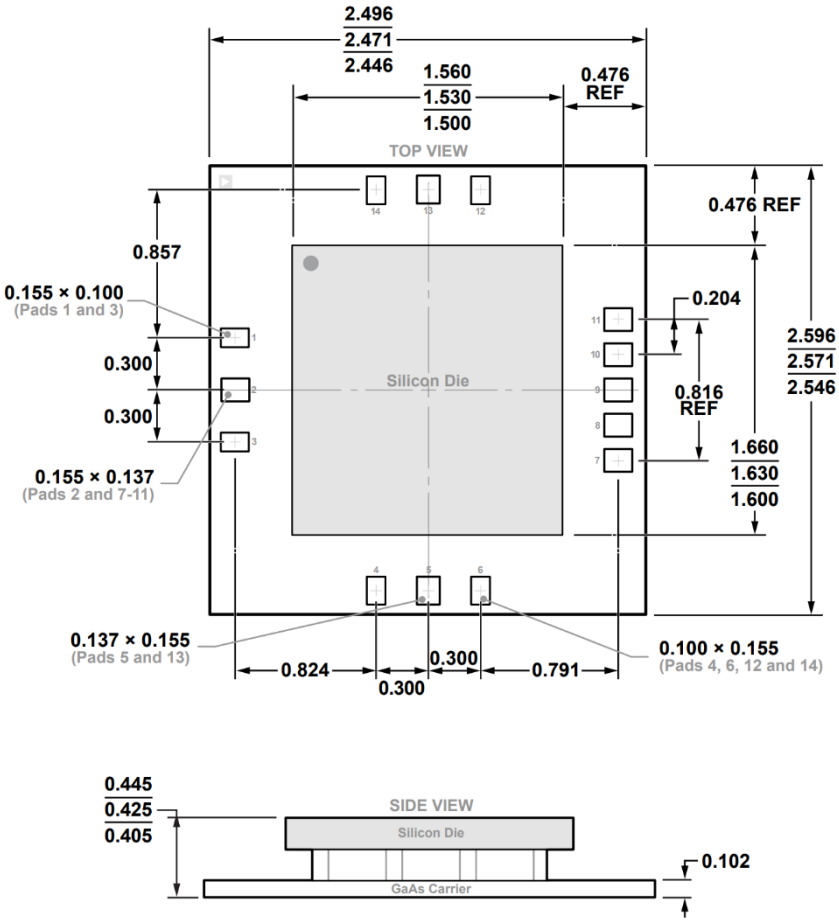


*Figure 21. 14-Pad Bare Die [CHIP]*
*2.50 mm x 2.60 mm Body and 0.425 mm Height*
*(C-14-8)*
*Dimensions shown in millimeters*


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