Die-on-Carrier, Silicon Digital Attenuator 0.5 dB LSB, 6-Bit, 100 MHz to 40 GHz

Preliminary Technical Data

ADRF5473

FEATURES

- Ultrawideband frequency range: 100 MHz to 40 GHz
- Attenuation range: 0.5 dB steps to 31.5 dB
- Bond pads for wire-bond and ribbon-bond
- Low insertion loss
  - 1.7 dB up to 18 GHz
  - 2.2 dB up to 26 GHz
  - 3.2 dB up to 40 GHz
- Attenuation accuracy
  - ±(0.10 + 2.0% of attenuation state) up to 26 GHz
  - ±(0.13 + 1.5% of attenuation state) up to 35 GHz
  - ±(0.30 + 1.5% of attenuation state) up to 40 GHz
- Typical step error
  - ±0.12 dB up to 26 GHz
  - ±0.30 dB up to 35 GHz
  - ±0.60 dB up to 40 GHz
- High input linearity
  - P0.1dB insertion loss state: 31 dBm
  - P0.1dB other attenuation states: 28 dBm
  - IP3: 50 dBm typical
- High RF input power handling: 26 dBm average, 31 dBm peak
- Tight distribution in relative phase
- No low frequency spurious signals
- SPI and parallel mode control, CMOS/LVTTL compatible
- RF settling time (0.1 dB of final RF output): 250 ns
- 18-terminal bond pads, 1.64 mm x 3.20 mm, Die-on-carrier

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

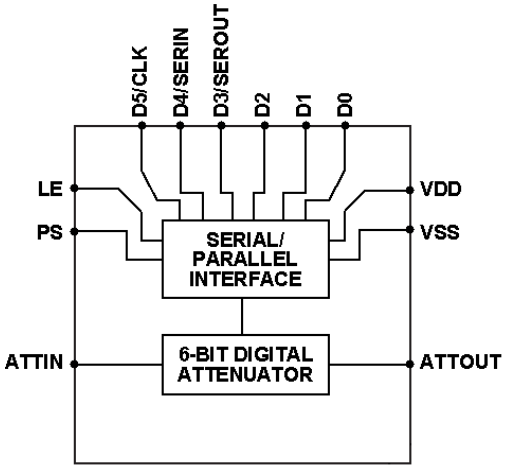

Figure 1.

GENERAL DESCRIPTION

The ADRF5473 is a 6-bit digital attenuator with 31.5 dB attenuation control range in 0.5 dB steps manufactured in a silicon process attached on a GaAs carrier substrate. The substrate incorporates the bond pads for chip-and-wire assembly, the device bottom is metalized and connected to ground.

This device operates from 100 MHz to 40 GHz with better than 3.2 dB of insertion loss and excellent attenuation accuracy. The ADRF5473 has a radio frequency (RF) input power handling capability of 26 dBm average and 31 dBm peak for all states.

The ADRF5473 requires a dual supply voltage of +3.3 V and −3.3 V. The device features serial peripheral interface (SPI), parallel mode control, and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5473 is designed to match a characteristic impedance of 50 Ω.

Rev. PrE
Document Feedback

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, case temperature (T_{DIE})[1] = 25°C, and 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		40,000	MHz
INSERTION LOSS (IL)	100 MHz to 10 GHz		1.3		dB
	10 GHz to 18 GHz		1.7		dB
	18 GHz to 26 GHz		2.2		dB
	26 GHz to 35 GHz		2.8		dB
	35 GHz to 40 GHz		3.2		dB
RETURN LOSS (RL)	ATTIN and ATTOUT, all attenuation states				
	100 MHz to 10 GHz		17		dB
	10 GHz to 18 GHz		18		dB
	18 GHz to 26 GHz		16		dB
	26 GHz to 35 GHz		15		dB
	35 GHz to 40 GHz		15		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		31.5		dB
Step Size	Between any successive attenuation states		0.5		dB
Accuracy	Referenced to insertion loss				
	100 MHz to 10 GHz		±(0.05 +1.5% of state)		dB
	10 GHz to 18 GHz		±(0.07 +2.0% of state)		dB
	18 GHz to 26 GHz		±(0.10 +2.0% of state)		dB
	26 GHz to 35 GHz		±(0.13 +1.5% of state)		dB
	35 GHz to 40 GHz		±(0.30 +1.5% of state)		dB
Step Error	Between any successive state				
	100 MHz to 10 GHz		±0.11		dB
	10 GHz to 18 GHz		±0.12		dB
	18 GHz to 26 GHz		±0.12		dB
	26 GHz to 35 GHz		±0.30		dB
	35 GHz to 40 GHz		±0.60		dB
RELATIVE PHASE	Referenced to insertion loss				
	10 GHz		18		Degrees
	18 GHz		33		Degrees
	26 GHz		50		Degrees
	35 GHz		75		Degrees
	40 GHz		80		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power = 10 dBm				
Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		35		ns
On and Off Time (t_{ON} and t_{OFF})	50% triggered control (CTL) to 90% of RF output		125		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered CTL to 0.1 dB of final RF output		250		ns
0.05 dB	50% triggered CTL to 0.05 dB of final RF output		350		ns
Overshoot			1		dB
Undershoot			−2.5		dB
RF Phase Settling Time	f = 5 GHz				
5°	50% triggered CTL to 5° of final RF output		160		ns
1°	50% triggered CTL to 1° of final RF output		180		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT LINEARITY[2]	100 MHz to 30 GHz				
0.1 dB Power Compression (P0.1dB)					
Insertion Loss State			31		dBm
Other Attenuation States			28		dBm
Third-Order Intercept (IP3)	Two-tone input power = 14 dBm per tone, Δf = 1 MHz, all attenuation states		50		dBm
DIGITAL CONTROL INPUTS	LE, PS, D0, D1, D2, D3/SEROUT,[3] D4/SERIN, D5/CLK pads				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			<1		µA
High (I_{INH})	D0, D1, D2		33		µA
	LE, PS, D3/SEROUT[3], D4/SERIN, D5/CLK pads		<1		µA
DIGITAL CONTROL OUTPUT	D3/SEROUT pad[3]				
Voltage					
Low (V_{OUTL})			0 ± 0.3		V
High (V_{OUTH})			V_{DD} ± 0.3		V
Current (I_{OUTL}, I_{OUTH})				0.5	mA
SUPPLY CURRENT	V_{DD} and V_{SS} pads				
Positive Supply Current			117		µA
Negative Supply Current			−117		µA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
Positive (V_{DD})		3.15		3.45	V
Negative (V_{SS})		−3.45		−3.15	V
Digital Control Voltage		0		V_{DD}	V
RF Power [4]	f = 100 MHz to 30 GHz, T_{DIE}[1] = 85°C,[5] all attenuation states				
Input at ATTIN	Steady state average			26	dBm
	Steady state peak			31	dBm
	Hot switching average			23	dBm
	Hot switching peak			27	dBm
Input at ATTOUT	Steady state average			17	dBm
	Steady state peak			21	dBm
	Hot switching average			14	dBm
	Hot switching peak			18	dBm
Die Temperature (T_{DIE})[1]		−40		+105	°C

[1] T_{DIE} refers to the bottom of the die-on-carrier.
[2] Input linearity performance degrades over frequency, see Figure 21 to Figure 24.
[3] The D3/SEROUT pad is an input in parallel control mode and an output in serial control mode. See Table 5 for the pad function descriptions.
[4] For power derating over frequency, see Figure 2 to Figure 3. Applicable for all ATTIN and ATTOUT power specifications.
[5] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specifications by 3 dB.

TIMING SPECIFICATIONS

See Figure 26, Figure 27, and Figure 28 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period, see Figure 26	70			ns
t_{CS}	Control setup time, see Figure 26	15			ns

Parameter	Description	Min	Typ	Max	Unit
t_{CH}	Control hold time, see Figure 26		3	5	ns
t_{LN}	LE setup time, see Figure 26	15			ns
t_{LEW}	Minimum LE pulse width, see Figure 26 and Figure 28		10		ns
t_{LES}	Minimum LE pulse spacing, see Figure 26		630		ns
t_{CKN}	Serial clock hold time from LE, see Figure 26		0		ns
t_{PH}	Hold time, see Figure 28		10		ns
t_{PS}	Setup time, see Figure 28		2		ns
t_{CO}	Clock to output (SEROUT) time, see Figure 27	15	20	25	ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Inputs	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3mA
RF Input Power[1] (f = 100 MHz to 30 GHz, T_{DIE} = 85°C[2])	
ATTIN	
Steady State Average	27 dBm
Steady State Peak	32 dBm
Hot Switching Average	24 dBm
Hot Switching Peak	28 dBm
ATTOUT	
Steady State Average	18 dBm
Steady State Peak	22 dBm
Hot Switching Average	15 dBm
Hot Switching Peak	19 dBm
RF Power Under Unbiased Condition (V_{DD}, V_{SS} = 0 V)	
Input at ATTIN	21 dBm
Input at ATTOUT	15 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Epoxy cure	170 °C
Continuous Power Dissipation (P_{DISS})	0.4 W
ESD Sensitivity	
Human Body Model (HBM)	
ATTIN and ATTOUT Pads	500 V
Digital Pads	2000 V

[1] For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.
[2] For 105°C operation, the power handling degrades from the T_{DIE} = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
C-18-1	125	°C/W

POWER DERATING CURVES

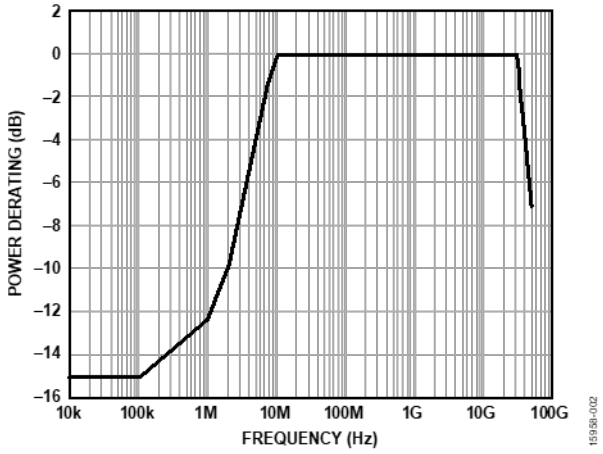

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{DIE} = 85°C

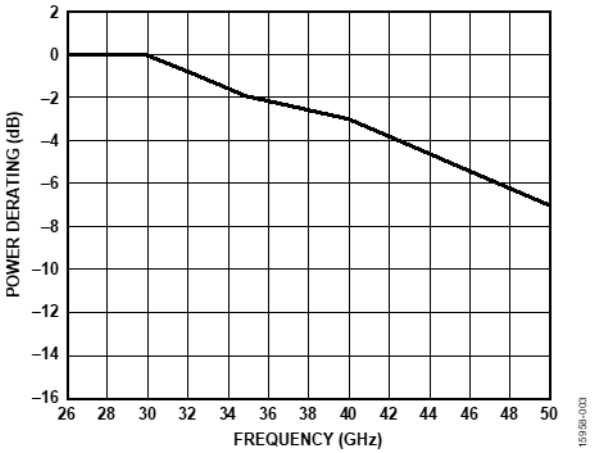

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{DIE} = 85°C

DIE-ON-CARRIER DEVICE CONSTRUCTION AND TEMPERATURE CYCLE RELIABILITY

CAUTION: Users must qualify their assemblies against the end use conditions. Guidance in IPC-9701A and IPC-SM-785 can be followed for accelerated test conditions in different end applications. Users may apply conformal coating or underfill to mitigate stress and strain in their assemblies, however the impact on performance needs to be validated. As both dies are attached with solder joints, users must follow best practices for the thermo-mechanical design of their module assemblies. The temperature expansion coefficient of the substrate material has to match the thermal expansion coefficient of the GaAs and Si die; warpage or other mechanical deformation on the substrate should not be allowed. The die attach-process and the epoxy cure temperatures should be set to lower the accumulated stress after assembly. ADI qualified the die-on-carrier parts per Jedec JESD22-A104F on "stand alone" units, not mounted on a substrate. Contact ADI for experimental results and best

practices with regard to material selection for mounting components on a substrate.

The construction of a Die-On-Carrier part is depicted in the Figure 4. A Si die on top side is face-to-face attached to a GaAs die on the bottom side. The Si and GaAs dies incorporate SnAg plated Cu pillars individually that are designed to match and mate on the other die. After accurate placement and alignment, both dies are attached with a reflow process. The SnAg solder joint is the only structure keeping both dies attached, no underfills or other adhesives are applied. The GaAs die incorporate through wafer vias to carry the GND return signals from the RF substrate on the bottom side when attached using a conductive epoxy on the RF substrate. The GaAs die works as the carrier for the complete structure after assembly.

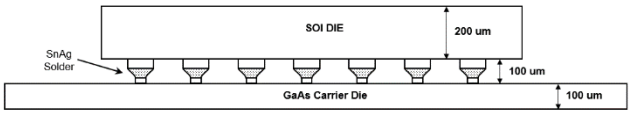

Figure 4. Die-On-Carrier Construction

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

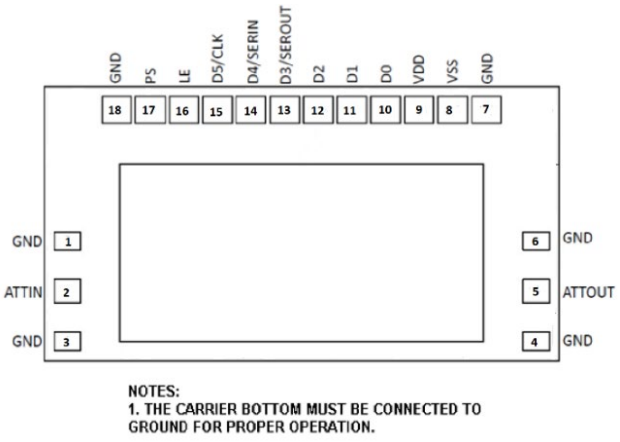

Figure 5. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1,3, 4, 6, 7, 18	GND	Ground. Bonding of these ground pads are optional. See Application section.
2	ATTIN	Attenuator Input. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 8 for the interface schematic.
5	ATTOUT	Attenuator Output. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 8 for the interface schematic.
8	VSS	Negative Supply Input. See Figure 10 for the interface schematic.
9	VDD	Positive Supply Input. See Figure 9 for the interface schematic.
10	D0	Parallel Control Input for 0.5 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
11	D1	Parallel Control Input for 1 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
12	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
13	D3/SEROUT	Parallel Control Input for 4 dB Attenuator Bit (D3). See Figure 6 for the interface schematic. Serial Data Output (SEROUT). See the Theory of Operation section for more information.
14	D4/SERIN	Parallel Control Input for 8 dB Attenuator Bit (D4). See Figure 6 for the interface schematic. Serial Data Input (SERIN). See the Theory of Operation section for more information.
15	D5/CLK	Parallel Control Input for 16 dB Attenuator Bit (D5). See Figure 6 for the interface schematic. Serial Clock Input (CLK). See the Theory of Operation section for more information.
16	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
17	PS	Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
	Carrier Bottom	The carrier bottom is gold metallized and must be directly attached to the ground plane using conductive epoxy.

INTERFACE SCHEMATICS

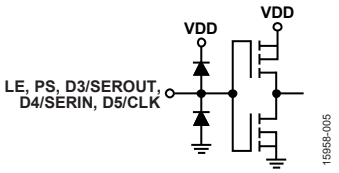

Figure 6. Digital Input Interface (LE, PS, D3/SEROUT, D4/SERIN, D5/CLK)

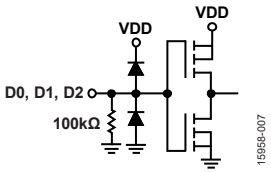

Figure 7. Digital Input Interface (D0, D1, D2)

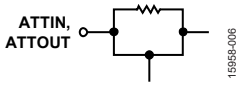

Figure 8. ATTIN and ATTOUT Interface

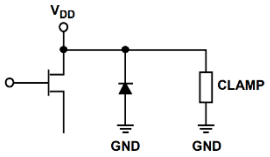

Figure 9. VDD Interface Schematic

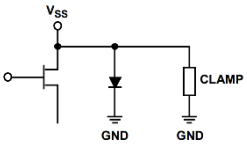

Figure 10. VSS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted. S-parameters are measured with microstrip launchers and 3-mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are de-embedded.

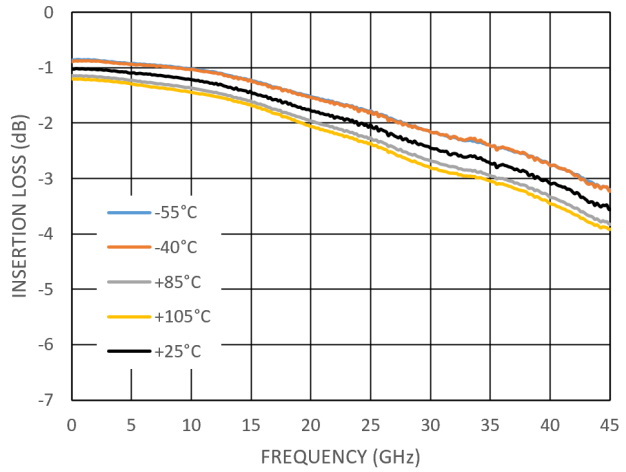

Figure 11. Insertion Loss vs. Frequency over Temperature

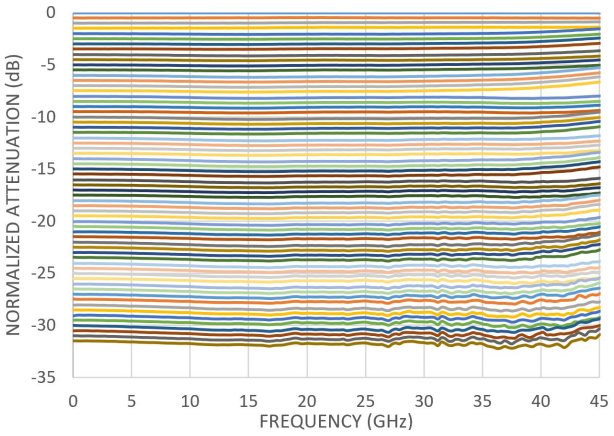

Figure 13. Normalized Attenuation vs. Frequency for All States at Room Temperature

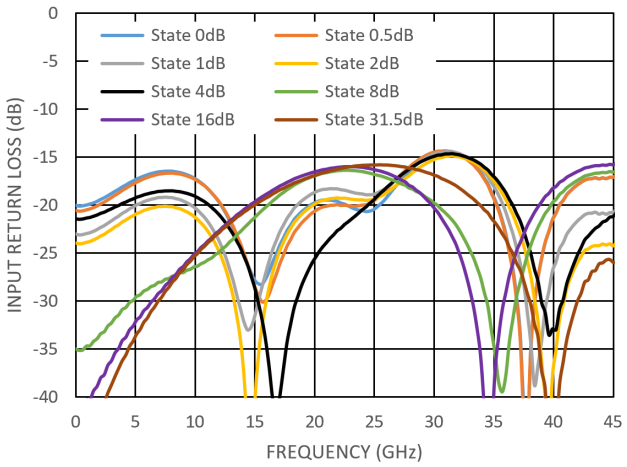

Figure 12. Input Return Loss vs. Frequency (Major States Only)

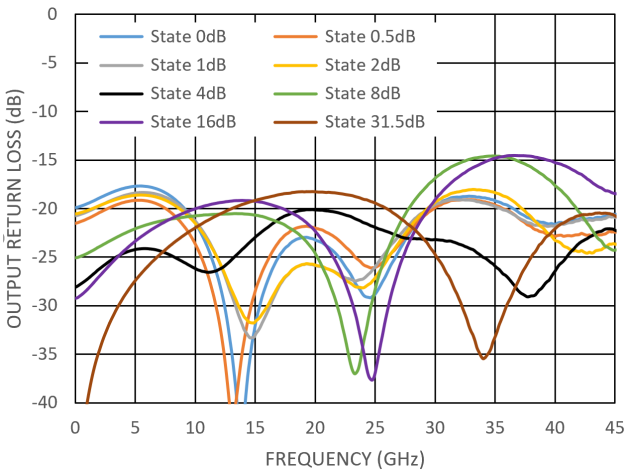

Figure 14. Output Return Loss vs. Frequency (Major States Only)

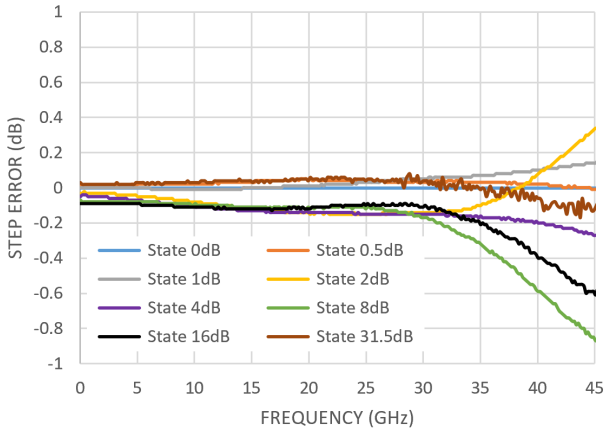

Figure 15. Step Error vs. Frequency (Major States Only)

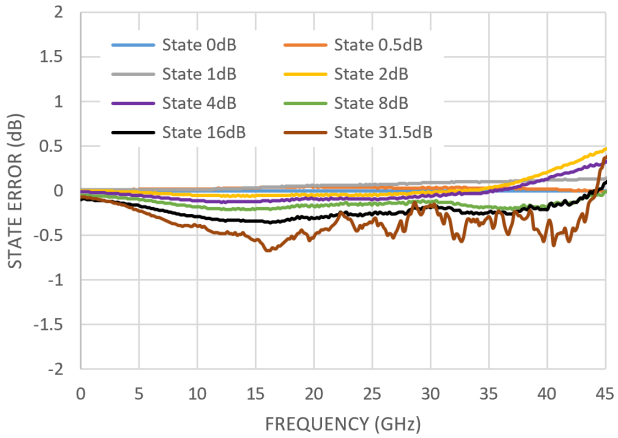

Figure 16. State Error vs. Frequency (Major States Only)

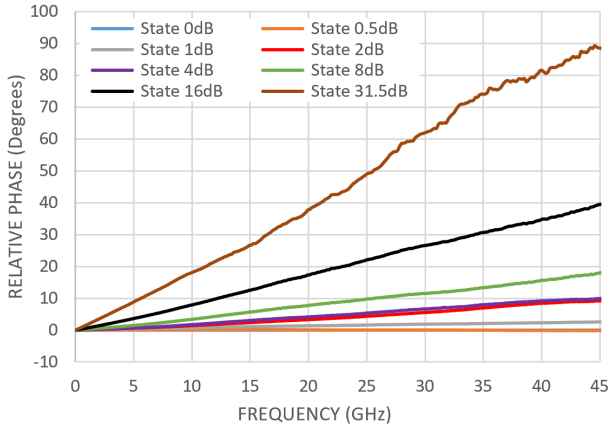

Figure 17. Relative Phase vs. Frequency (Major States Only)

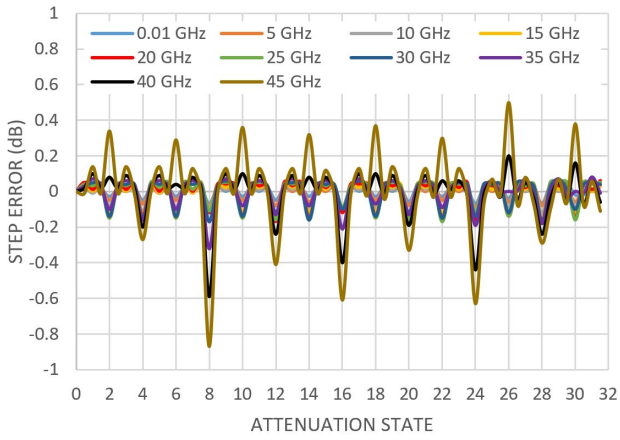

Figure 18. Step Error vs. Attenuation State over Frequency

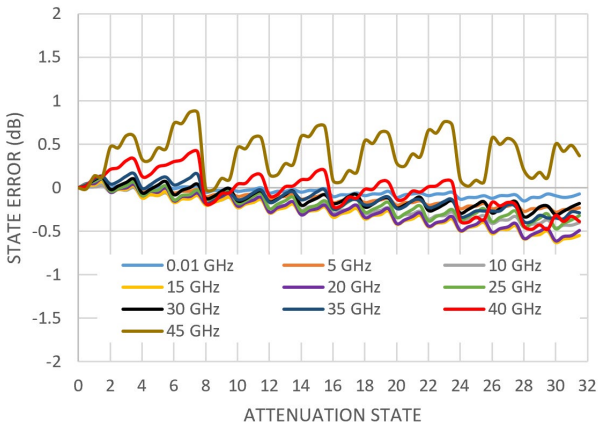

Figure 19. State Error vs. Attenuation State over Frequency

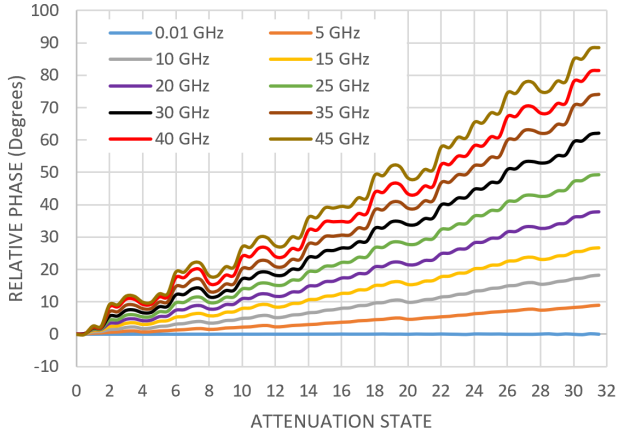

Figure 20. Relative Phase vs. Attenuation State over Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

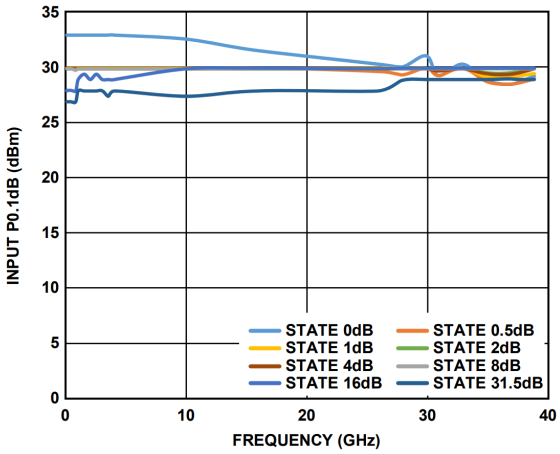

Figure 21. Input P0.1dB vs. Frequency (Major States Only)

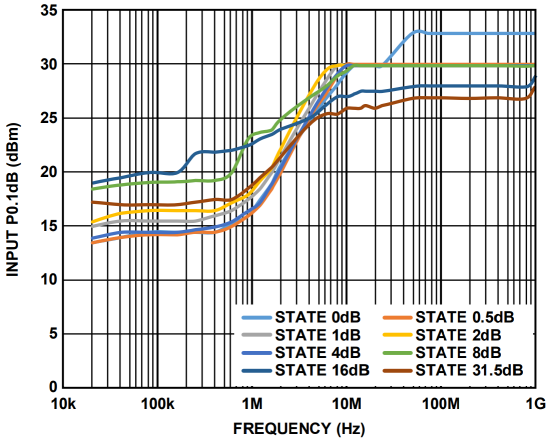

Figure 23. Input P0.1dB vs. Frequency (Major States Only), Low Frequency Detail

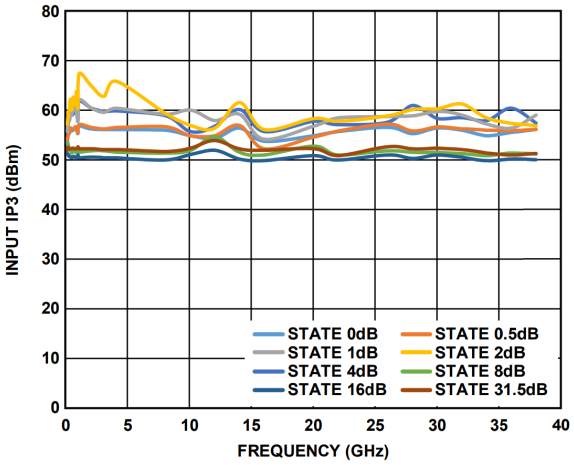

Figure 22. Input IP3 vs. Frequency (Major States Only)

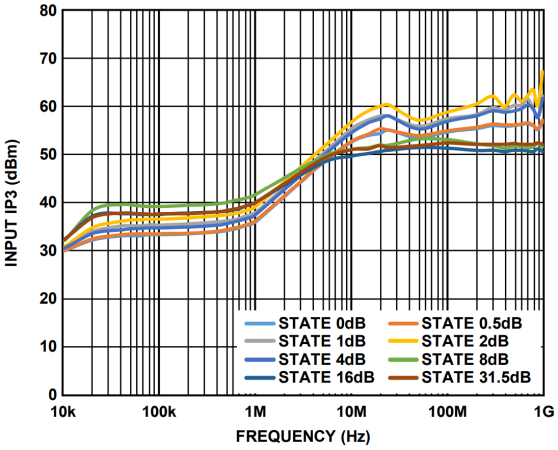

Figure 24. Input IP3 vs. Frequency (Major States Only), Low Frequency Detail

THEORY OF OPERATION

The ADRF5473 incorporates a 6-bit fixed attenuator array that offers an attenuation range of 31.5 dB in 0.5 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 25).

Note that when referring to a single function of a multifunction pad in this section, only the portion of the pad name that is relevant is mentioned. For full pad names of the multifunction pads, refer to the Pad Configuration and Function Descriptions section.

POWER SUPPLY

The ADRF5473 requires a positive supply voltage applied to the VDD pad and a negative supply voltage applied to the VSS pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the VDD and VSS voltages. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the VDD voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the VDD voltage is powered up and the control pads are not driven to a valid logic state.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5473 has internal power-on-reset circuity. This sets the attenuator to maximum attenuation state (31.5 dB) when VDD and VSS voltages are applied and LE is set to low.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. No dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The ADRF5473 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

SERIAL OR PARALLEL MODE SELECTION

The ADRF5473 can be controlled in either serial or parallel mode by setting the PS pad to high or low, respectively (see Table 6).

Table 6. Mode Selection

PS	Control Mode
Low	Parallel
High	Serial

Table 7. Truth Table

Digital Control Input[1]						
D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	High	0.5
Low	Low	Low	Low	High	Low	1.0
Low	Low	Low	High	Low	Low	2.0
Low	Low	High	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	31.5

[1] Any combination of the control voltage input states shown in Table 7 provides an attenuation equal to the sum of the bits selected.

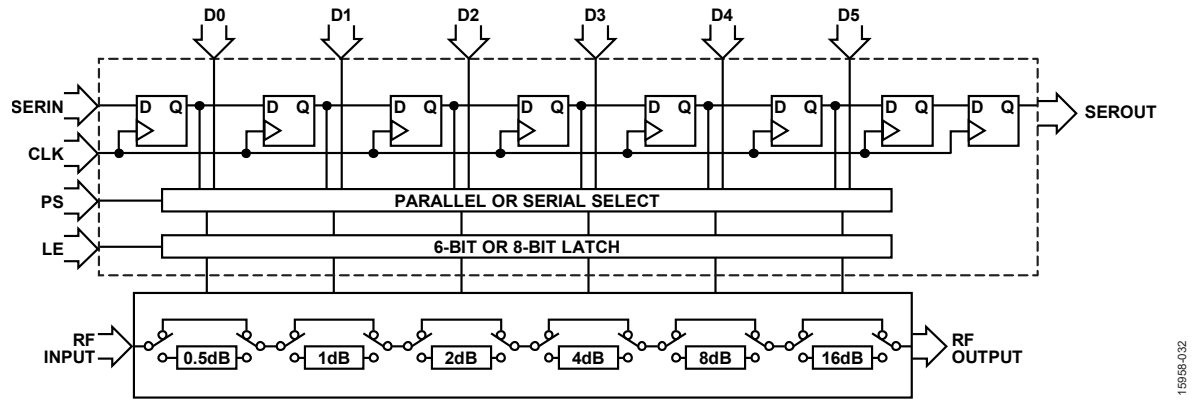

Figure 25. Simplified Circuit Diagram

SERIAL MODE INTERFACE

The ADRF5473 supports a 4-wire SPI: serial data input (SERIN), clock (CLK), serial data output (SEROUT), and latch enable (LE). The serial control interface is activated when PS is set to high.

The ADRF5473 attenuation states can be controlled using 6-bit or 8-bit SERIN data. If an 8-bit word is used to control the state of the attenuator, the first two bits, D7 and D6, are don't care bits. It does not matter if these two bits are held low or high, or if they are omitted altogether. Only Bits [D0:D5] set the state of the attenuator.

In serial mode, the SERIN data is clocked most significant bit (MSB) first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new SERIN data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 26 in conjunction with Table 2 and Table 7.

Using SEROUT

The ADRF5473 also features a serial data output, SEROUT. SEROUT outputs the serial input data at the 8th clock cycle and can control a cascaded attenuator using a single SPI bus. Figure 27 shows the serial out timing diagram.

When using the attenuator in a daisy-chain operation, 8-bit SERIN data must be used due to the 8-clock cycle delay between SERIN and SEROUT. The SEROUT pad does not support high impedance mode. A tristate buffer can be used to interface a shared bus.

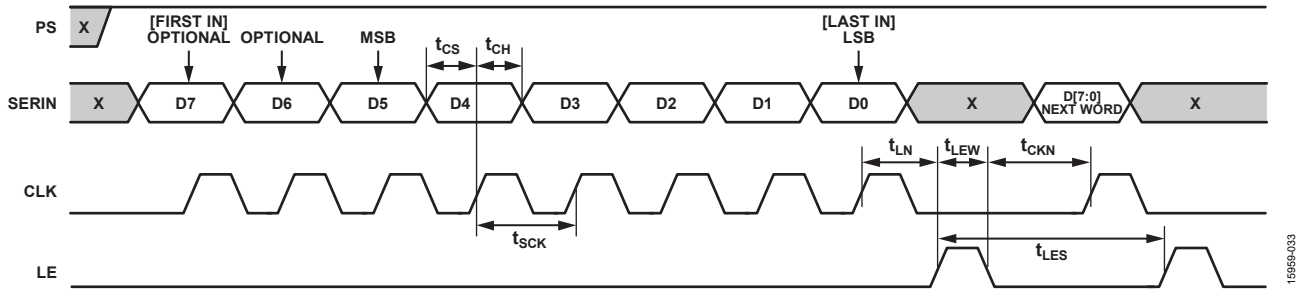

Figure 26. Serial Control Timing Diagram

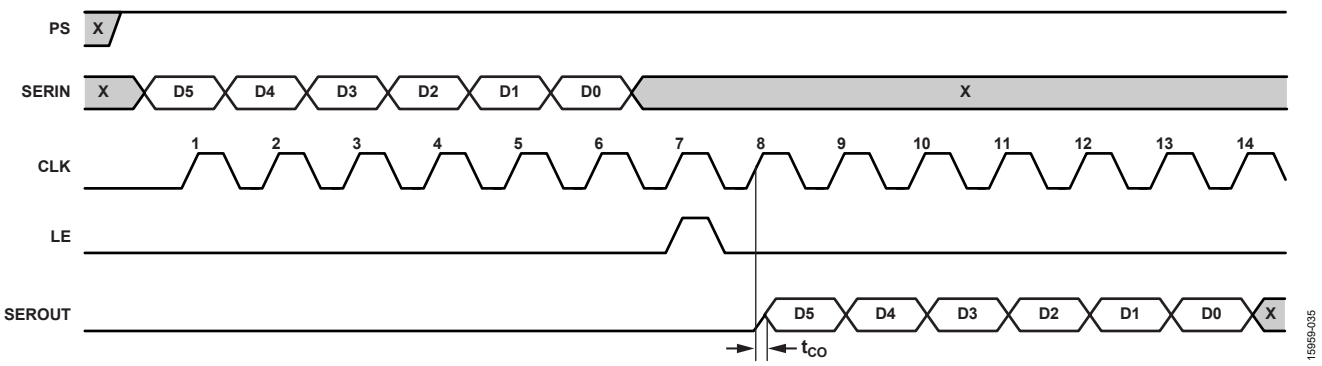

Figure 27. Serial Output Timing Diagram

PARALLEL MODE INTERFACE

The ADRF5473 has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 7. The parallel control interface is activated when PS is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, the LE pad must be kept high. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pad must be kept low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled low to latch the change into the device until the next desired attenuation change (see Figure 28 in conjunction with Table 2).

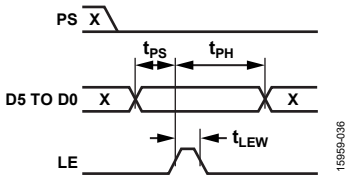

Figure 28. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

ASSEMBLY DIAGRAM

An assembly diagram of the ADRF5473 is shown in Figure 29.

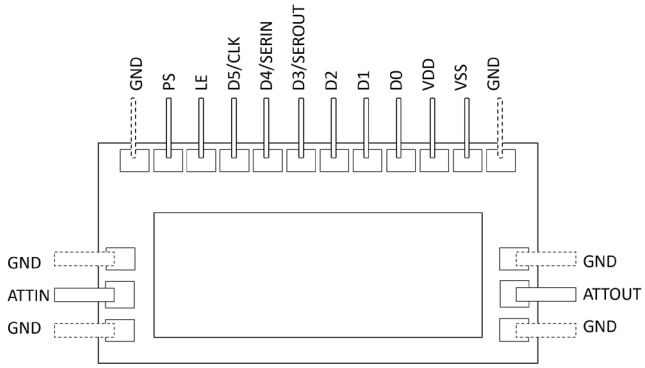

Figure 29. Die Assembly Diagram

MOUNTING AND BONDING TECHNIQUES

The part is designed to have the optimum RF input and output impedance match with 3 mil x 0.5 mil gold ribbon wire and typical 3 mil loop height. Bonding diagram is shown in Figure 30 and Figure 31. Alternatively, using multiple wire bonds with equivalent inductance will yield similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad as the device is designed to match internally the recommended ribbon bond-wire. A spacing of 3 mils from RF transmission line to device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The DC pads are big enough also to accommodate ribbon bods if preferred.

The device is metallized on the backside and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

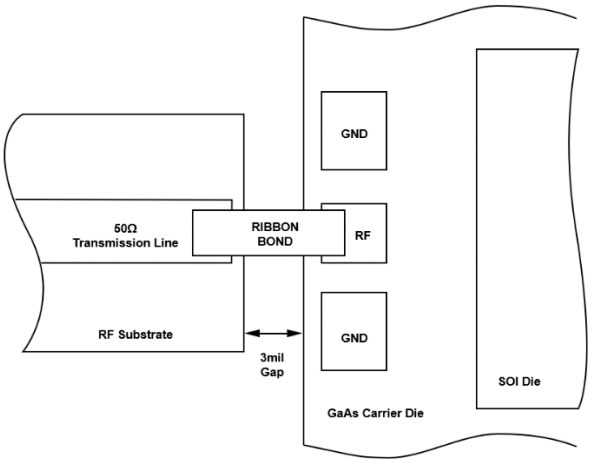

Figure 30. Bonding Diagram-Top View

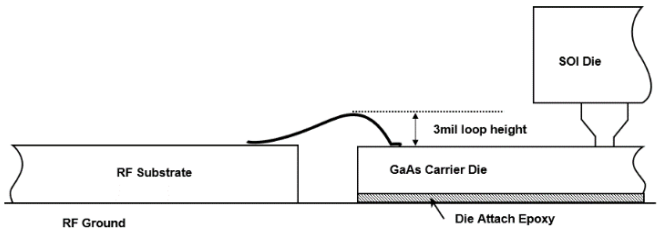

Figure 31. Bonding Diagram-Side View

Wire Bonding

RF bonds using ribbon wire must be thermo-sonically bonded a nominal stage temperature of 150°C and apply a minimum amount of ultrasonic energy to achieve reliable bonds.

Handling, Mounting and Epoxy Die Attach

Keep devices in ESD protective sealed bags for shipment and store all bared die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs parts, however for die-on-carrier devices using a vacuum tool is recommended to avoid any damage on the device substrate. Handle parts in clean environment and do not attempt to clean using liquid cleaning systems.

For epoxy die is attached, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Epoxy cure temperatures should be set per the manufacturer's recommendations taking into account the device maximum ratings and also to lower the accumulated mechanical stress after assembly.

OUTLINE DIMENSIONS

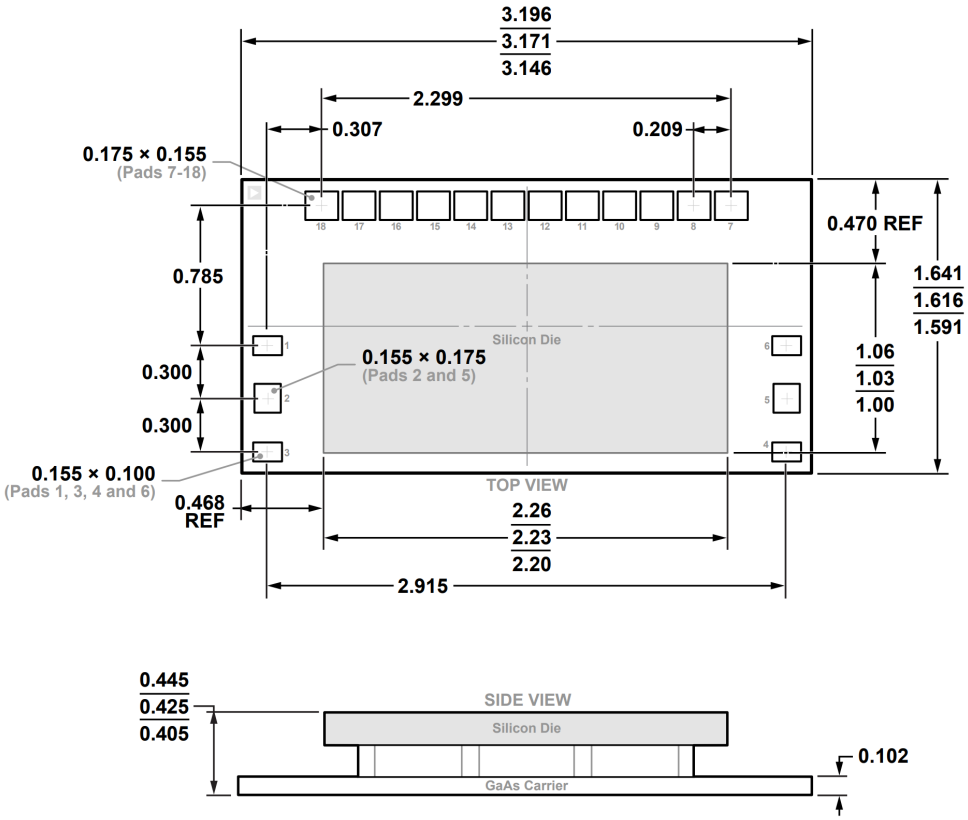

Figure 32. 18-Pad Bare Die [CHIP]
3.20 mm x 1.64 mm Body and 0.425 mm Height
(C-18-1)
Dimensions shown in millimeters