150 MBPS Quad-Channel Digital Isolator

ADuM141ES

1.0 Scope

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

This data specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at http://www.analog.com/ADuM141

2.0 Part Number

The complete part number(s) of this specification follows:

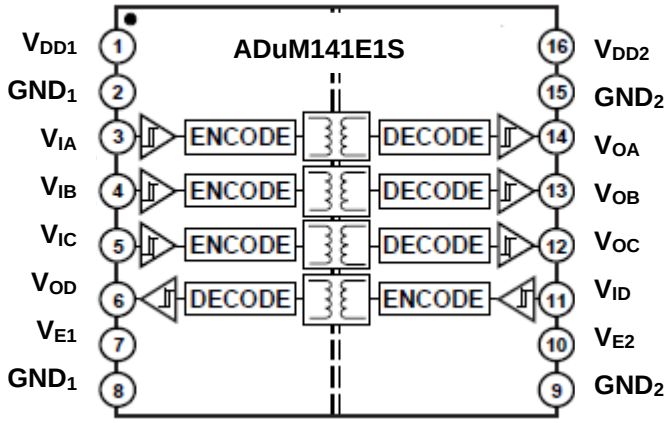
Specific Part Number	Description
ADuM141E1L703F	150 MBPS Quad-Channel Digital Isolator

3.0 Case Outline

The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline Letter	Descriptive Designator	Terminals	Lead Finish	Package style
X	CDFP4-F16	16 lead	Hot Solder Dip	Bottom Brazed Flat Pack

FUNCTIONAL BLOCK DIAGRAM



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Package: X			
Pin Number	**Terminal Symbol**	**Pin Type**	**Pin Description**
1	VDD1	Power	Supply Voltage for Isolator Side 1 1/
2	GND1	Power	Ground 1. Ground reference for Isolator Side 1. 2/
3	VIA	Digital Input	Logic Input A.
4	VIB	Digital Input	Logic Input B
5	VIC	Digital Input	Logic Input C
6	VOD	Digital Output	Logic Output D
7	VE1	Digital Input	Output Enable for side 1. Active high logic input
8	GND1	Power	Ground 1. Ground reference for Isolator Side 1. 2/, 4/
9	GND2	Power	Ground 2. Ground reference for Isolator Side 2. 3/
10	VE2	Digital Input	Output Enable for side 2. Active high logic input
11	VID	Digital Input	Logic Input D.
12	VOC	Digital Output	Logic Output C
13	VOB	Digital Output	Logic Output B
14	VOA	Digital Output	Logic Output A
15	GND2	Power	Ground 2. Ground reference for Isolator Side 2. 3/
16	VDD2	Power	Supply Voltage for Isolator Side 2 1/
Lid		Power	Metal Lid electrically connected to ground (GND1)

Figure 1 – Terminal Connections

1/ Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between VDD1 (Pin 1) and GND1 (Pin 2), and between VDD2 (Pin 16) and GND2 (Pin 15)
2/ Pin 2 and Pin 8 are internally connected, and connecting both to GND1 is recommended.
3/ Pin 9 and Pin 15 are internally connected, and connecting both to GND2 is recommended.
4/ Internally connected to Metal Lid.

4.0 Specifications

4.1. Absolute Maximum Ratings 1/

Supply voltage (V_{DD1} , V_{DD2}) ..... -0.5V to 7.0V
Input voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}) ..... -0.5V to V_{DDI} + 0.5V 2/
Output voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD}) ..... -0.5V to V_{DDO} + 0.5V2/
Storage temperature range ..... -65°C to +150°C
Output current per pin (I_{O1}, I_{O2}) ..... -10mA to +10mA
Junction temperature maximum (T_J) ..... +150°C
Lead temperature (soldering, 60 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 72 °C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 162 °C/W 3/
ESD Sensitivity (HBM)…….. Class 2

4.2. Recommended Operating Conditions

Supply voltage (V_{DDI}) ..... +1.8 V to +5.0 V
Ambient operating temperature range (T_A)…… -55°C to +125°C

4.3. Nominal Operating Performance Characteristics 4/

Jitter
Peak-to-Peak..... 800ps
RMS..... 190ps
Capacitance (Input-to-Output) 14pF 5/
Input Capacitance 4pF 6/

4.4. Radiation Features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)…… 50k rads(Si)
Single event phenomenon (SEP):
No single event latchup (SEL) occurs at effective linear energy transfer (LET): …….. ≤ 80MeV-cm2/mg 7/

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
2/ VDDI and VDDO refer to the supply voltages on the input and output sides of a given channel, respectively.
3/ Measurement taken under absolute worst case condition and represent data taken with thermal camera for highest power density location. See MIL-STD-1835 for average ΘJC number.
4/ All typical specifications are at TA = 25°C, 3.6 V ≤ VDD1 ≤ 5. V, 3.3 V ≤ VDD2 ≤ 5.0 V, unless otherwise noted. Switching specifications are tested with CL = 15 pF and CMOS signal levels, unless otherwise noted.
5/ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.
6/ Input capacitance is from any input data pin to ground.
7/ Limits are characterized at initial qualification and after any design or process changes that may affect the SEP characteristics, but are not production lot tested unless specified by the customer through the purchase order or contract. For more information on single event effect (SEE) test results, customers are requested to contact ADI. SEL test report is available on the external website: www.analog.com.

TABLE IA – ELECTRICAL PERFORMANCE CHARACTERISTICS - 5V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ 9/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate 8/	DR	Within PWD Limit	9,10,11		150	Mbps
		D,P,L	9		150	
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9	4.8	13.5	ns
			10	4.8	13.5	
			11	4.2	13.5	
		D,P,L	9	4.8	13.5	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	9,10,11		3	ns
		D,P,L	9		3	
Pulse Width	PW	Within PWD limit	9,10,11	6.6		ns
		D,P,L	9	6.6		
Propagation Delay Skew 3/, 4/	t_{PSK}		9,10,11		6.1	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11	-25	25	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		3	ns
		D,P,L	9		3	
Channel Matching Opposing-Direction	t_{PSKOD}		9,10,11		3	ns
		D,P,L	9		3	
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	9		4	ns
			10		4.5	
			11		3.5	
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 1MBPS	4,5,6		10.3	mA
		D,P,L	4		10.3	
		F = 25MBPS	4,5,6		10.9	
		D,P,L	4		10.9	
		F = 100MBPS	4,5,6		15.9	
		D,P,L	4		15.9	
		F = 150MBPS	4,5,6		17	
		D,P,L	4		17	
	$I_{DD2(D)}$	F = 1MBPS	4,5,6		6.85	
		D,P,L	4		6.85	
		F = 25MBPS	4,5,6		8.5	
		D,P,L	4		8.5	
		F = 100MBPS	4,5,6		14	
		D,P,L	4		14	
		F = 150MBPS	4,5,6		17.5	
		D,P,L	4		17.5	
Quiescent Supply Current	$I_{DD1(Q)}$	V_{Ix} = 1 5/	1,2,3		2.46	mA
		D,P,L	1		2.46	
		V_{Ix} = 0 5/	1,2,3		17	
		D,P,L	1		17	
Quiescent Supply Current	$I_{DD2(Q)}$	V_{Ix} = 1 5/	1,2,3		2.62	mA
		D,P,L	1		2.62	
		V_{Ix} = 0 5/	1,2,3		10	
		D,P,L	1		10	
DC CHARACTERISTICS						

Parameter See notes at end of table	Symbol	Conditions 1/ 9/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
Logic High Input Threshold	V_{IH}	7/		1,2,3	0.7 V_{DDx}		V
			D,P,L	1	0.7 V_{DDx}		
Logic Low Input Threshold	V_{IL}	7/		1,2,3		0.3 V_{DDx}	V
			D,P,L	1		0.3 V_{DDx}	
Logic High Output Voltages	V_{OH}	I_{Ox} = −20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.1		V
			D,P,L	1	V_{DDx} − 0.1		
		I_{Ox} = −4 mA, VIx = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.4		
			D,P,L	1	V_{DDx} − 0.4		
Logic Low Output Voltages	V_{OL}	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.1	V
			D,P,L	1		0.1	
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.4	
			D,P,L	1		0.4	
Input Current per Channel	I_I	V_{Ix} = V_{DDx} and V_{Ix} = 0V 5/, 6/,7/		1,2,3	-10	+10	µA
			D,P,L	1	-10	+10	
Enable Pull-Up Current	I_{PU}	V_{Ex} = 0 V 10/		1,2,3	-10		µA
			D,P,L	1	-10		
Enable Pull-Down Current	I_{PD}	V_{Ex} = V_{DDx} 7/,10/		1,2,3		15	µA
			D,P,L	1		15	
Tristate Output Current per Channel	I_{OZ}	0 V ≤ V_{Ox} ≤ V_{DDx} 7/		1,2,3	-10	10	µA
			D,P,L	1	-20	20	
Undervoltage Lockout Positive VDDX Threshold	V_{DDxUV+}			1,2		1.75	V
				3		1.71	
			D,P,L	1		1.75	
Undervoltage Lockout Negative VDDX Threshold	V_{DDxUV-}			1,2,3	1.35		V
			D,P,L	1	1.35		
Undervoltage Lockout VDDX Hysteresis	V_{DDxUVH}			1,2,3		0.4	V
			D,P,L	1		0.4	

TABLE IA NOTES:
1/ TA nom = 25ºC, TA max = 125ºC, and TA min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted, VDDx nom = 5 V, VDDx max = 5.5V, VDDx min = 4.5V.
2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Parameter is not tested post irradiation
4/ tPSK is the magnitude of the worst-case difference in tPHL or tPLH that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
5/ VIx refer to the input voltage.
6/ IOx refer to the output current of a given channel (A, B, C, or D).
7/ VDDx refers to the power supply on either side of a given channel (A, B, C, or D).
8/ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible
9/ Do not exceed VDDxnom where VDD1 = VDD2 = 5V at T = -55°C when all four channels are running in parallel. Device instability may occur.
10/ V_{Ex} refers to V_{E1} and V_{E2}

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS – 3.3V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS							
Data Rate 8/	DR	Within PWD Limit		9,10,11		150	Mbps
			D,P,L	9		150	
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output		9,10	4	14	ns
				11	3.6	14	
			D,P,L	9	4	14	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	9,10,11		3	ns
		D,P,L	9		3	
Pulse Width	PW	Within PWD limit	9,10,11	6.6		ns
		D,P,L	9	6.6		
Propagation Delay Skew 3/, 4/	t_{PSK}		9,10,11		7.5	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11	-25	25	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		3	ns
		D,P,L	9		3	
Channel Matching Opposing-Direction	t_{PSKOD}		9,10,11		3	ns
		D,P,L	9		3	
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	9		4	ns
			10		4.5	
			11		3.5	
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 1MBPS	4,5,6		10.1	mA
		D,P,L	4		10.1	
		F = 25MBPS	4,5,6		10.5	
		D,P,L	4		10.5	
		F = 100MBPS	4,5,6		14.9	
		D,P,L	4		14.9	
		F = 150MBPS	4,5,6		14.9	
		D,P,L	4		14.9	
	$I_{DD2(D)}$	F = 1MBPS	4,5,6		6.65	
		D,P,L	4		6.65	
		F = 25MBPS	4,5,6		8	
		D,P,L	4		8	
		F = 100MBPS	4,5,6		12.8	
		D,P,L	4		12.8	
		F = 150MBPS	4,5,6		14.5	
		D,P,L	4		14.5	
Quiescent Supply Current	$I_{DD1(Q)}$	V_{Ix} = 1 5/	1,2,3		2.36	mA
		D,P,L	1		2.36	
		V_{Ix} = 0 5/	1,2,3		16.7	
		D,P,L	1		16.7	
Quiescent Supply Current	$I_{DD2(Q)}$	V_{Ix} = 1 5/	1,2,3		2.52	mA
		D,P,L	1		2.52	
		V_{Ix} = 0 5/	1,2,3		9.7	
		D,P,L	1		9.7	
DC CHARACTERISTICS						
Logic High Input Threshold	V_{IH}	7/	1,2,3	0.7 V_{DDx}		V
		D,P,L	1	0.7 V_{DDx}		
Logic Low Input Threshold	V_{IL}	7/	1,2,3		0.3 V_{DDx}	V
		D,P,L	1		0.3 V_{DDx}	
Logic High Output Voltages	V_{OH}	I_{Ox} = −20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} − 0.1		V
		D,P,L	1	V_{DDx} − 0.1		
		I_{Ox} = −4 mA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} − 0.4		
		D,P,L	1	V_{DDx} − 0.4		
Logic Low Output Voltages	V_{OL}	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.1	V
		D,P,L	1		0.1	
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.4	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
		D,P,L	1		0.4	
Input Current per Channel	I_I	$V_{Ix} = V_{DDx}$ and $V_{Ix} = 0V$ 5/, 6/,7/	1,2,3	-10	+10	µA
		D,P,L	1	-10	+10	
Enable Pull-Up Current	I_{PU}	$V_{Ex} = 0$ V 9/	1,2,3	-10		µA
		D,P,L	1	-10		
Enable Pull-Down Current	I_{PD}	$V_{Ex} = V_{DDx}$ 7/,9/	1,2,3		15	µA
		D,P,L	1		15	
Tristate Output Current per Channel	I_{OZ}	$0 V \le V_{Ox} \le V_{DDx}$ 7/	1,2,3	-10	10	µA
		D,P,L	1	-20	20	
Undervoltage Lockout Positive VDDX Threshold	V_{DDxUV+}		1,2		1.75	V
			3		1.71	
		D,P,L	1		1.75	
Undervoltage Lockout Negative VDDX Threshold	V_{DDxUV-}		1,2,3	1.35		V
		D,P,L	1	1.35		
Undervoltage Lockout VDDX Hysteresis	V_{DDxUVH}		1,2,3		0.4	V
		D,P,L	1		0.4	

TABLE IB NOTES:
1/ TA nom = 25ºC, TA max = 125ºC, and TA min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. VDDx nom = 3.3 V, VDDx max = 3.6V, VDDx min = 3V
2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Parameter is not tested post irradiation
4/ tPSK is the magnitude of the worst-case difference in tPHL or tPLH that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
5/ VIx refer to the input voltage.
6/ IOx refer to the output current of a given channel (A, B, C, or D).
7/ VDDx refers to the power supply on either side of a given channel (A, B, C, or D).
8/ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.
9/ V_{Ex} refers to V_{E1} and V_{E2}

TABLE IC – ELECTRICAL PERFORMANCE CHARACTERISTICS – 2.5V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate 8/	DR	Within PWD Limit	9,10,11		150	Mbps
		D,P,L	9		150	
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9	4.7	14	ns
			10	4.7	14	
			11	4	14	
		D,P,L	9	4.7	14	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	9,10,11		3	ns
		D,P,L	9		3	
Pulse Width	PW	Within PWD limit	9,10,11	6.6		ns
		D,P,L	9	6.6		
Propagation Delay Skew 3/, 4/	t_{PSK}		9,10,11		6.8	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11	-25	25	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		3	ns
		D,P,L	9		3	
Channel Matching Opposing-Direction	t_{PSKOD}		9,10,11		3	ns
		D,P,L	9		3	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%		9		4	ns
				10		4.5	
				11		3.5	
SUPPLY CURRENT							
Dynamic Supply Current	$I_{DD1(D)}$	F = 1MBPS		4, 5, 6		10	mA
			D,P,L	4		10	
		F = 25MBPS		4, 5, 6		10.4	
			D,P,L	4		10.4	
		F = 100MBPS		4, 5, 6		14.5	
			D,P,L	4		14.5	
		F = 150MBPS		4, 5, 6		14.5	
			D,P,L	4		14.5	
	$I_{DD2(D)}$	F = 1MBPS		4,5,6		6.55	
			D,P,L	4		6.55	
		F = 25MBPS		4,5,6		7.7	
			D,P,L	4		7.7	
		F = 100MBPS		4,5,6		11.5	
			D,P,L	4		11.5	
		F = 150MBPS		4, 5, 6		13	
			D,P,L	4		13	
Quiescent Supply Current	$I_{DD1(Q)}$	V_{Ix} = 1 5/		1,2,3		2.32	mA
			D,P,L	1		2.32	
		V_{Ix} = 0 5/		1,2,3		16.6	
			D,P,L	1		16.6	
Quiescent Supply Current	$I_{DD2(Q)}$	V_{Ix} = 1 5/		1,2,3		2.47	mA
			D,P,L	1		2.47	
		V_{Ix} = 0 5/		1,2,3		9.67	
			D,P,L	1		9.67	
DC CHARACTERISTICS							
Logic High Input Threshold	V_{IH}	7/		1,2,3	0.7 V_{DDx}		V
			D,P,L	1	0.7 V_{DDx}		
Logic Low Input Threshold	V_{IL}	7/		1,2,3		0.3 V_{DDx}	V
			D,P,L	1		0.3 V_{DDx}	
Logic High Output Voltages	V_{OH}	I_{Ox} = −20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.1		V
			D,P,L	1	V_{DDx} − 0.1		
		I_{Ox} = −4 mA, VIx = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.4		
			D,P,L	1	V_{DDx} − 0.4		
Logic Low Output Voltages	V_{OL}	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.1	V
			D,P,L	1		0.1	
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.4	
			D,P,L	1		0.4	
Input Current per Channel	I_I	V_{Ix} = V_{DDx} and V_{Ix} = 0V 5/, 6/,7/		1,2,3	-10	+10	µA
			D,P,L	1	-10	+10	
Enable Pull-Up Current	I_{PU}	V_{Ex} = 0 V 9/		1,2,3	-10		µA
			D,P,L	1	-10		
Enable Pull-Down Current	I_{PD}	V_{Ex} = V_{DDx} 7/,9/		1,2,3		15	µA
			D,P,L	1		15	
Tristate Output Current per Channel	I_{OZ}	0 V ≤ V_{Ox} ≤ V_{DDx} 7/		1,2,3	-10	10	µA
			D,P,L	1	-20	20	
Undervoltage Lockout Positive VDDX Threshold	V_{DDxUV+}			1,2		1.75	V
				3		1.71	
			D,P,L	1		1.75	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
Undervoltage Lockout Negative VDDX Threshold	V_{DDxUV-}			1,2,3	1.35		V
			D,P,L	1	1.35		
Undervoltage Lockout VDDX Hysteresis	V_{DDxUVH}			1,2,3		0.4	V
			D,P,L	1		0.4	

TABLE IC NOTES:
1/ TA nom = 25ºC, TA max = 125ºC, and TA min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. VDDx nom = 2.5 V, VDDx max = 2.75V, VDDx min = 2.25V
2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Parameter is not tested post irradiation
4/ tPSK is the magnitude of the worst-case difference in tPHL or tPLH that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
5/ VIx refer to the input voltage.
6/ IOx refer to the output current of a given channel (A, B, C, or D).
7/ VDDx refers to the power supply on either side of a given channel (A, B, C, or D).
8/ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible
9/ V_{Ex} refers to V_{E1} and V_{E2}

TABLE ID – ELECTRICAL PERFORMANCE CHARACTERISTICS –1.8V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS							
Data Rate 8/	DR	Within PWD Limit		9,10,11		150	Mbps
			D,P,L	9		150	
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output		9	4.8	15	ns
				10	5.8	15	
				11	5.4	15	
			D,P,L	9	4.8	15	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$		9,10,11		3	ns
			D,P,L	9		3	
Pulse Width	PW	Within PWD limit		9,10,11	6.6		ns
			D,P,L	9	6.6		
Propagation Delay Skew 3/, 4/	t_{PSK}			9,10,11		7.0	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD			10,11	-25	25	ps/°C
Channel Matching Codirection	t_{PSKCD}			9,10,11		3	ns
			D,P,L	9		3	
Channel Matching Opposing-Direction	t_{PSKOD}			9,10,11		3	ns
			D,P,L	9		3	
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%		9		4	ns
				10		4.5	
				11		3.5	
SUPPLY CURRENT							
Dynamic Supply Current	$I_{DD1(D)}$	F = 1MBPS		4, 5, 6		9.1	mA
			D,P,L	4		9.1	
		F = 25MBPS		4, 5, 6		10	
			D,P,L	4		10	
		F = 100MBPS		4, 5, 6		14	
			D,P,L	4		14	
		F = 150MBPS		4, 5, 6		14	
			D,P,L	4		14	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
	$I_{DD2(D)}$	F = 1MBPS	4, 5, 6		6.45	
		D,P,L	4		6.45	
		F = 25MBPS	4, 5, 6		7.5	
		D,P,L	4		7.5	
		F = 100MBPS	4, 5, 6		11.2	
		D,P,L	4		11.2	
		F = 150MBPS	4, 5, 6		13	
		D,P,L	4		13	
Quiescent Supply Current	$I_{DD1(Q)}$	V_{Ix} = 1 5/	1,2,3		2.28	mA
		D,P,L	1		2.28	
		V_{Ix} = 0 5/	1,2,3		16.5	
		D,P,L	1		16.5	
Quiescent Supply Current	$I_{DD2(Q)}$	V_{Ix} = 1 5/	1,2,3		2.45	mA
		D,P,L	1		2.45	
		V_{Ix} = 0 5/	1,2,3		9.6	
		D,P,L	1		9.6	
DC CHARACTERISTICS						
Logic High Input Threshold	V_{IH}	7/	1,2,3	0.7 V_{DDx}		V
		D,P,L	1	0.7 V_{DDx}		
Logic Low Input Threshold	V_{IL}	7/	1,2,3		0.3 V_{DDx}	V
		D,P,L	1		0.3 V_{DDx}	
Logic High Output Voltages	V_{OH}	I_{Ox} = −20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} − 0.1		V
		D,P,L	1	V_{DDx} − 0.1		
		I_{Ox} = −4 mA, VIx = V_{IxH} 5/, 6/,7/	1,2,3	V_{DDx} − 0.4		
		D,P,L	1	V_{DDx} − 0.4		
Logic Low Output Voltages	V_{OL}	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.1	V
		D,P,L	1		0.1	
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/	1,2,3		0.4	
		D,P,L	1		0.4	
Input Current per Channel	I_I	V_{Ix} = V_{DDx} and V_{Ix} = 0V 5/, 6/,7/	1,2,3	-10	+10	µA
		D,P,L	1	-10	+10	
Enable Pull-Up Current	I_{PU}	V_{Ex} = 0 V 9/	1,2,3	-10		µA
		D,P,L	1	-10		
Enable Pull-Down Current	I_{PD}	V_{Ex} = V_{DDx} 7/,9/	1,2,3		15	µA
		D,P,L	1		15	
Tristate Output Current per Channel	I_{OZ}	0 V ≤ V_{Ox} ≤ V_{DDx} 7/	1,2,3	-10	10	µA
		D,P,L	1	-20	20	
Undervoltage Lockout Positive VDDX Threshold	V_{DDxUV+}		1,2		1.75	V
			3		1.71	
		D,P,L	1		1.75	
Undervoltage Lockout Negative VDDX Threshold	V_{DDxUV-}		1,2,3	1.35		V
		D,P,L	1	1.35		
Undervoltage Lockout VDDX Hysteresis	V_{DDxUVH}		1,2,3		0.4	V
		D,P,L	1		0.4	

TABLE ID NOTES:
1/ TA nom = 25ºC, TA max = 125ºC, and TA min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted. VDDx nom = 1.8 V, VDDx max = 1.9V, VDDx min = 1.7V
2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Parameter is not tested post irradiation
4/ tPSK is the magnitude of the worst-case difference in tPHL or tPLH that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
5/ VIx refer to the input voltage.
6/ IOx refer to the output current of a given channel (A, B, C, or D).
7/ VDDx refers to the power supply on either side of a given channel (A, B, C, or D).

8/ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible
9/ V_{Ex} refers to V_{E1} and V_{E2}

TABLE IE – ELECTRICAL PERFORMANCE CHARACTERISTICS – MIXED 5V / 1.8V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/9/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate 8/	DR	Within PWD Limit	9,10,11		150	Mbps
		D,P,L	9		150	
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9	4.8	13	ns
			10	4.8	14.5	
			11	4.2	13	
		D,P,L	9	4.8	13	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	9,10,11		3	ns
		D,P,L	9		3	
Pulse Width	PW	Within PWD limit	9,10,11	6.6		ns
		D,P,L	9	6.6		
Propagation Delay Skew 3/, 4/	t_{PSK}		9,10,11		7.0	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11	-25	25	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		3	ns
		D,P,L	9		3	
Channel Matching	t_{PSKOD}		9		4	ns
			10		4.3	
			11		3.8	
Opposing-Direction		D,P,L	9		4	
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	9		4	ns
			10		4.5	
			11		3.5	
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 1MBPS	4, 5, 6		10.3	mA
		D,P,L	4		10.3	
		F = 25MBPS	4, 5, 6		10.9	
		D,P,L	4		10.9	
		F = 100MBPS	4, 5, 6		15.9	
		D,P,L	4		15.9	
		F = 150MBPS	4, 5, 6		17	
		D,P,L	4		17	
	$I_{DD2(D)}$	F = 1MBPS	4, 5, 6		6.45	
		D,P,L	4		6.45	
		F = 25MBPS	4, 5, 6		7.5	
		D,P,L	4		7.5	
		F = 100MBPS	4, 5, 6		11.2	
		D,P,L	4		11.2	
		F = 150MBPS	4, 5, 6		13	
		D,P,L	4		13	
Quiescent Supply Current	$I_{DD1(Q)}$	V_{Ix} = 1 5/	1,2,3		2.46	mA
		D,P,L	1		2.46	
		V_{Ix} = 0 5/	1,2,3		17	
		D,P,L	1		17	
Quiescent Supply Current	$I_{DD2(Q)}$	V_{Ix} = 1 5/	1,2,3		2.45	mA
		D,P,L	1		2.45	
		V_{Ix} = 0 5/	1,2,3		9.6	
		D,P,L	1		9.6	
DC CHARACTERISTICS						

Parameter See notes at end of table	Symbol	Conditions 1/9/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
Logic High Input Threshold	V_{IH}	7/		1,2,3	0.7 V_{DDx}		V
			D,P,L	1	0.7 V_{DDx}		
Logic Low Input Threshold	V_{IL}	7/		1,2,3		0.3 V_{DDx}	V
			D,P,L	1		0.3 V_{DDx}	
Logic High Output Voltages	V_{OH}	I_{Ox} = −20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.1		V
			D,P,L	1	V_{DDx} − 0.1		
		I_{Ox} = −4 mA, VIx = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.4		
			D,P,L	1	V_{DDx} − 0.4		
Logic Low Output Voltages	V_{OL}	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.1	V
			D,P,L	1		0.1	
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.4	
			D,P,L	1		0.4	
Input Current per Channel	I_I	V_{Ix} = V_{DDx} and V_{Ix} = 0V 5/, 6/,7/		1,2,3	-10	+10	µA
			D,P,L	1	-10	+10	
Enable Pull-Up Current	I_{PU}	V_{Ex} = 0 V 10/		1,2,3	-10		µA
			D,P,L	1	-10		
Enable Pull-Down Current	I_{PD}	V_{Ex} = V_{DDx} 7/, 10/		1,2,3		15	µA
			D,P,L	1		15	
Tristate Output Current per Channel	I_{OZ}	0 V ≤ V_{Ox} ≤ V_{DDx} 7/		1,2,3	-10	10	µA
			D,P,L	1	-20	20	
Undervoltage Lockout Positive VDDX Threshold	V_{DDxUV+}			1,2		1.75	V
				3		1.71	
			D,P,L	1		1.75	
Undervoltage Lockout Negative VDDX Threshold	V_{DDxUV-}			1,2,3	1.35		V
			D,P,L	1	1.35		
Undervoltage Lockout VDDX Hysteresis	V_{DDxUVH}			1,2,3		0.4	V
			D,P,L	1		0.4	

TABLE IE NOTES:
1/ TA nom = 25ºC, TA max = 125ºC, and TA min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted VDD1 nom = 5 V, VDD1 max = 5.5V, VDD1 min = 4.5V and VDD2 nom = 1.8 V, VDD2 max = 1.9V, VDD2 min = 1.7V.
2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Parameter is not tested post irradiation
4/ tPSK is the magnitude of the worst-case difference in tPHL or tPLH that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
5/ VIx refer to the input voltage.
6/ IOx refer to the output current of a given channel (A, B, C, or D).
7/ VDDx refers to the power supply on either side of a given channel (A, B, C, or D).
8/ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible
9/ Do not exceed Do not exceed VDD1nom where VDD1 = 5V at T = -55°C when all four channels are running in parallel. Device instability may occur.
10/ V_{Ex} refers to V_{E1} and V_{E2}

TABLE IF – ELECTRICAL PERFORMANCE CHARACTERISTICS – MIXED 1.8V / 5V OPERATION

Parameter See notes at end of table	Symbol	Conditions 1/9/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
SWITCHING CHARACTERISTICS						
Data Rate 8/	DR	Within PWD Limit	9,10,11		150	Mbps
		D,P,L	9		150	
Propagation Delay	t_{PHL}, t_{PLH}	50% input to 50% output	9,10	4.8	14.5	ns
			11	4.5	14.5	
		D,P,L	9	4.8	14.5	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	9,10,11		3	ns
		D,P,L	9		3	
Pulse Width	PW	Within PWD limit	9,10,11	6.6		ns
		D,P,L	9	6.6		
Propagation Delay Skew 3/, 4/	t_{PSK}		9,10,11		7.0	ns
Pulse Width Distortion Change vs. Temperature 3/	ΔPWD		10,11	-25	25	ps/°C
Channel Matching Codirection	t_{PSKCD}		9,10,11		3	ns
		D,P,L	9		3	
Channel Matching	t_{PSKOD}		9		4	ns
			10		4.5	
			11		4	
Opposing-Direction		D,P,L	9		4	
Output Rise/Fall Time 2/, 3/	t_R/t_F	10% to 90%	9		4	ns
			10		4.5	
			11		3.5	
SUPPLY CURRENT						
Dynamic Supply Current	$I_{DD1(D)}$	F = 1MBPS	4, 5, 6		9.1	mA
		D,P,L	4		9.1	
		F = 25MBPS	4, 5, 6		10	
		D,P,L	4		10	
		F = 100MBPS	4, 5, 6		14	
		D,P,L	4		14	
		F = 150MBPS	4, 5, 6		14	
		D,P,L	4		14	
	$I_{DD2(D)}$	F = 1MBPS	4,5,6		6.85	
		D,P,L	4		6.85	
		F = 25MBPS	4, 5, 6		8.5	
		D,P,L	4		8.5	
		F = 100MBPS	4, 5, 6		14	
		D,P,L	4		14	
		F = 150MBPS	4, 5, 6		17	
		D,P,L	4		17	
Quiescent Supply Current	$I_{DD1(Q)}$	V_{Ix} = 1 5/	1,2,3		2.28	mA
		D,P,L	1		2.28	
		V_{Ix} = 0 5/	1,2,3		16.5	
		D,P,L	1		16.5	
	$I_{DD2(Q)}$	V_{Ix} = 1 5/	1,2,3		2.8	
Quiescent Supply Current		D,P,L	1		2.8	mA
		V_{Ix} = 0 5/	1,2,3		10	
		D,P,L	1		10	
DC CHARACTERISTICS						
Logic High Input Threshold	V_{IH}	7/	1,2,3	0.7 V_{DDx}		V

Parameter See notes at end of table	Symbol	Conditions 1/9/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
			D,P,L	1	0.7 V_{DDx}		
Logic Low Input Threshold	V_{IL}	7/		1,2,3		0.3 V_{DDx}	V
			D,P,L	1		0.3 V_{DDx}	
Logic High Output Voltages	V_{OH}	I_{Ox} = −20 µA, V_{Ix} = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.1		V
			D,P,L	1	V_{DDx} − 0.1		
		I_{Ox} = −4 mA, VIx = V_{IxH} 5/, 6/,7/		1,2,3	V_{DDx} − 0.4		
			D,P,L	1	V_{DDx} − 0.4		
Logic Low Output Voltages	V_{OL}	I_{Ox} = 20 µA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.1	V
			D,P,L	1		0.1	
		I_{Ox} = 4 mA, V_{Ix} = V_{IxL} 5/, 6/,7/		1,2,3		0.4	
			D,P,L	1		0.4	
Input Current per Channel	I_I	V_{Ix} = V_{DDx} and V_{Ix} = 0V 5/, 6/,7/		1,2,3	-10	+10	µA
			D,P,L	1	-10	+10	
Enable Pull-Up Current	I_{PU}	V_{Ex} = 0 V 10/		1,2,3	-10		µA
			D,P,L	1	-10		
Enable Pull-Down Current	I_{PD}	V_{Ex} = V_{DDx} 7/,10/		1,2,3		15	µA
			D,P,L	1		15	
Tristate Output Current per Channel	I_{OZ}	0 V ≤ V_{Ox} ≤ V_{DDx} 7/		1,2,3	-10	10	µA
			D,P,L	1	-20	20	
Undervoltage Lockout Positive VDDX Threshold	V_{DDxUV+}			1,2		1.75	V
				3		1.71	
			D,P,L	1		1.75	
Undervoltage Lockout Negative VDDX Threshold	V_{DDxUV-}			1,2,3	1.35		V
			D,P,L	1	1.35		
Undervoltage Lockout VDDX Hysteresis	V_{DDxUVH}			1,2,3		0.4	V
			D,P,L	1		0.4	

TABLE IF NOTES:
1/ TA nom = 25ºC, TA max = 125ºC, and TA min = -55ºC unless otherwise noted. Switching specifications are tested with CL = 15 pF, and CMOS signal levels, unless otherwise noted VDD1 nom = 1.8 V, VDD1 max = 1.9V, VDD1 min = 1.7V and VDD2 nom = 5 V, VDD2 max = 5.5 V, VDD2 min = 4.5V .
2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Parameter is not tested post irradiation
4/ tPSK is the magnitude of the worst-case difference in tPHL or tPLH that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
5/ VIx refer to the voltage input signals of a given channel (A, B, C, or D).
6/ IOx refer to the output current of a given channel (A, B, C, or D).
7/ VDDx refers to the power supply on either side of a given channel (A, B, C, or D).
8/ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible
9/ Do not exceed Do not exceed VDD2nom where VDD2 = 5V at T = -55°C when all four channels are running in parallel. Device instability may occur.
10/ V_{Ex} refers to V_{E1} and V_{E2}

TABLE IG – ELECTRICAL PERFORMANCE CHARACTERISTICS- INSULATION AND SAFETY-RELATED SPECIFICATIONS 1/,2/

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage 3/	Iso	400	Vrms	1-minute duration
Resistance (Input-to-Output) 4/	R_{I-O}	10^9	Ω	
Maximum Working Insulation Voltage 5/	CWV	393	Vpeak	1ppm for 30-year minimum lifetime 6/
Common-Mode Transient Immunity 7/	|CMH|	70	KV/µs	VIx = VDDx, VCM = 1000 V, transient magnitude = 800 V
	|CML|	50	KV/µs	VIx = 0 V, VCM = 1000 V, transient magnitude = 800 V

TABLE IG NOTES:
1/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
2/ Parameter is not tested post irradiation
3/ Operation at this high voltage can lead to shortened isolation life. Continuous working voltage exceeding the rated value may cause permanent damage.
4/ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.
5/ Refers to continuous voltage magnitude imposed across the isolation barrier. Long term operation at this high voltage can lead to shortened isolation life. Continuous working voltage exceeding the rated value may cause permanent damage.
6/ For Bipolar AC Voltage environment which is worst case condition for *i*Coupler products.
7/ |CMH| is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (VO) > 0.8 VDDx. |CML| is the maximum common-mode voltage slew rate that can be sustained while maintaining VO > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

V_{Ix} Input[1/2]	V_{Ex} Input[1/2]	V_{DDI} State[2/]	V_{DDO} State[2/]	Default High (E1), V_{Ox} Output[1/2/]	Description
L	H or NC	Powered	Powered	L	Normal operation
H	H or NC	Powered	Powered	H	Normal operation
X	L	Powered	Powered	Z	Outputs disabled
L	H or NC	Unpowered	Powered	H	Fail-safe output
X[3]	L[3]	Unpowered	Powered	Z	Outputs disabled
X[3]	X[3]	Powered	Unpowered	Indeterminate	

Figure 2 - Truth Table (Positive Logic)

1/ L means low, H means high, X means don't care, NC means not connected, and Z means high impedance.
2/ VIX and VOX refer to the input and output signals of a given channel (A, B, C, or D). Vex refers to the output enable signal on the same side as the VOX outputs. VDDI and VDDO refer to the supply voltages on the input and output sides of the given channel, respectively.
3/ Input pins (VIX, VE1 and VE2) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

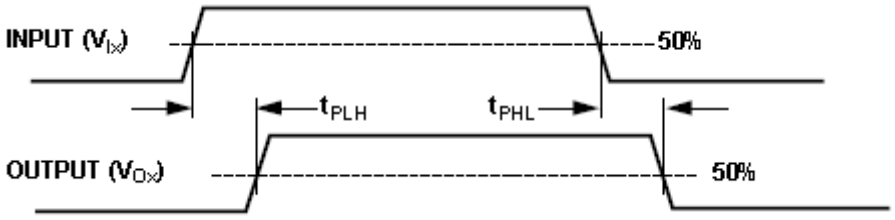

Figure 3 – Propagation Delay Parameters

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	**Subgroups (in accordance with MIL-PRF-38535, Table III)**
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6, 9, 10, 11 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 4, 5, 6, 9, 10, 11 2/
Group D end-point electrical parameters	1, 2, 3, 4, 5, 6, 9, 10, 11
Group E end-point electrical parameters	1, 4, 9 3/

Table IIA Notes:
1/ PDA applies to Table I subgroup 1 and Table IIB delta parameters.
2/ See Table IIB for delta parameters
3/ Parameters noted in Table I are not tested post irradiation.

TABLE IIB – LIFE TEST/BURN-IN DELTA LIMITS

Table IIB			
Parameter	**Symbol**	**Delta**	**Units**
IDD1 Dynamic Supply Current VDD1=VDD2=5V, 150MBPS	$I_{DD1(D)}$	0.7	mA
IDD2 Dynamic Supply Current VDD1=VDD2=5V, 150MBPS	$I_{DD2(D)}$	0.7	mA
IDD1 Quiescent Supply Current VDD, VDD1=VDD2=5V Vi = 1	$I_{DD1(Q)}$	0.05	mA
IDD2 Quiescent Supply Current VDD, VDD1=VDD2=5V Vi = 1	$I_{DD2(Q)}$	0.05	mA
IDD1 Quiescent Supply Current VDD, VDD1=VDD2=5V Vi = 0	$I_{DD1(Q)}$	0.08	mA
IDD2 Quiescent Supply Current VDD, VDD1=VDD2=5V Vi = 0	$I_{DD2(Q)}$	0.08	mA
Input Current, VDD1=VDD2=5V, V_{Ix} = 0V	I_I	0.2	µA
Input Current, VDD1=VDD2=5V, V_{Ix} = 5V	I_I	0.2	µA
Logic High Output Voltages VDD1=VDD2=5V, Iox = 20uA	VOH	2	mV
Logic Low Output Voltages VDD1=VDD2=5V, Iox = 20uA	VOL	2	mV

5.0 Burn-In Life Test, and Radiation

5.1. Burn-In Test Circuit, Life Test Circuit

5.1.1. The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition D of MIL –STD-883.

5.1.2. HTRB is not applicable for this drawing.

5.2. Radiation Exposure Circuit

5.2.1. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0 MIL-PRF-38535 QMLV Exceptions

6.1. Wafer Fabrication

Wafer fabrication occurs at MIL-PRF-38535 QML Class Q certified facility.

6.2. Wafer Lot Acceptance (WLA)

Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM inspection per MIL-STD-883 TM2018 is not applicable to the ADuM141E1S. The wafer fabrication process is manufactured using planarized metallization.

6.3. Device contains bi-metallic wire bonds (Gold bond wires on Aluminum die pads).

7.0 Application Notes

OVERVIEW

The ADuM141E1S use a high frequency carrier to transmit data across the isolation barrier using iCoupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 4, the ADuM141E1S have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

For the ADuM141E1S that have a high fail-safe output state, Figure 4 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high (ADuM141E1S) sets the output to high.

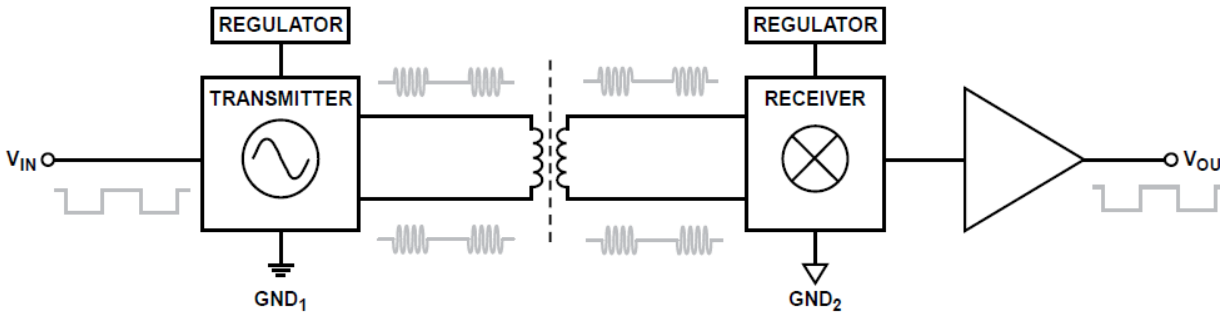

Figure 4 – Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

PC BOARD LAYOUT

The ADuM141E1S digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 5).Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for VDD1 and between Pin 15 and Pin 16 for VDD2. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

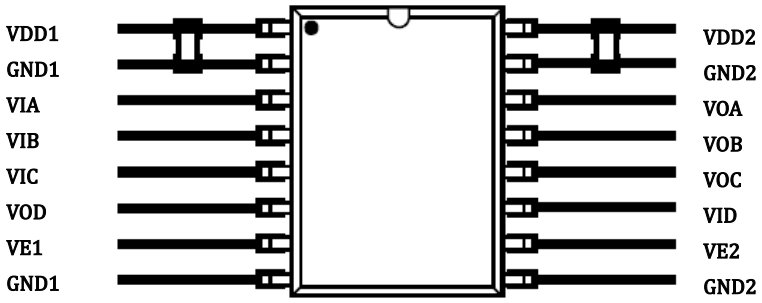

Figure 5 – Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage. See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition. See Figure 3.

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM141E1S component. Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM141E1S components operating under the same conditions.

8.0 Package Outline Dimensions

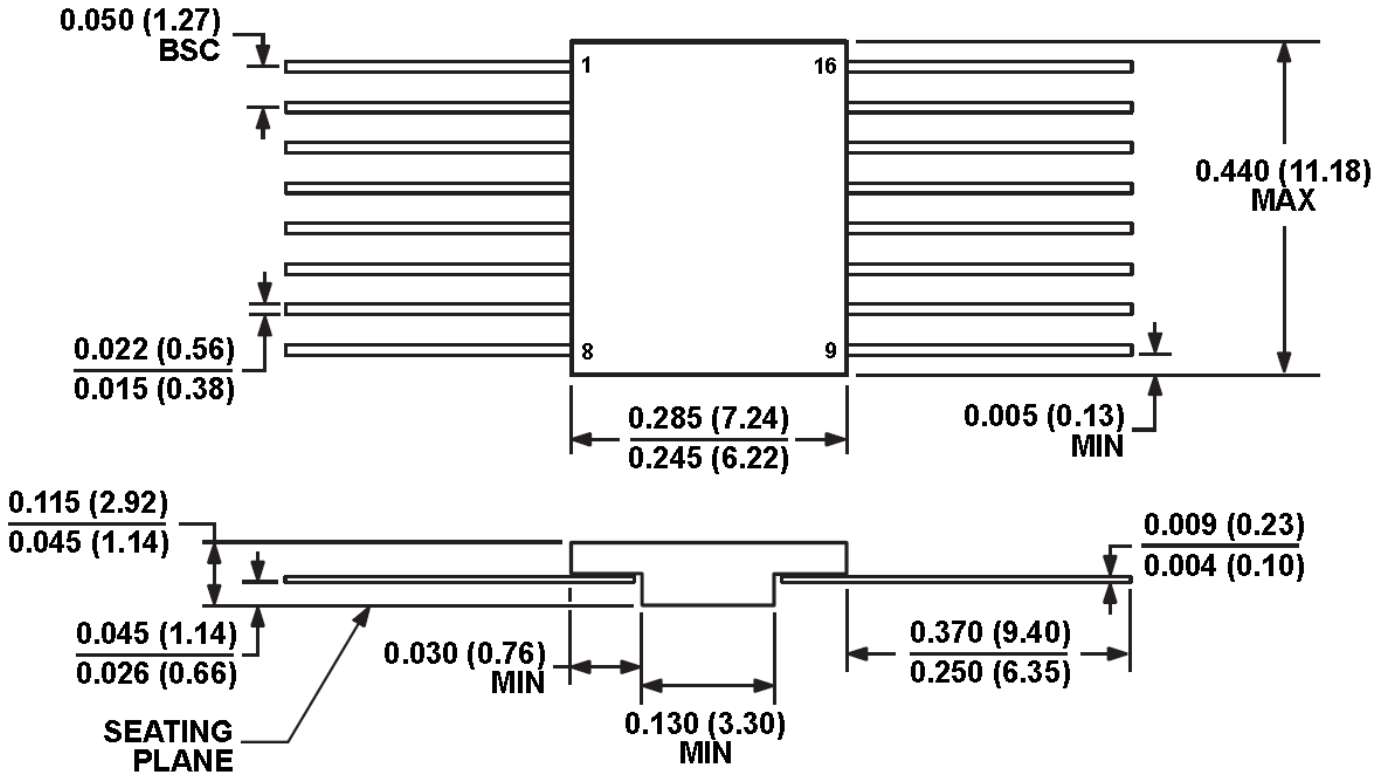

Figure 6. 16-Lead Bottom Brazed Flatpack

Dimensions shown in inches and (millimeters)

9.0 ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuM141E1L703F	–55°C to +125°C	16 Lead Bottom Brazed Flat Pack	CDFP4-F16

10.0 Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial Release	8/30/18
B	Correct page 1 block diagram error	10/26/18
C	Update and move Maximum Working Voltage and Common Mode Transient Immunity from Section 4.3 to Table IG.	7/20/20