Data Sheet

ADAU1850

Three ADCs, One DAC, Low Power Codec with Audio/FastDSP

FEATURES

- Programmable FastDSP audio processing engine
  - Up to 768 kHz sample rate
  - Biquad filters, limiters, volume controls, mixing
- Low latency, 24-bit ADCs and DAC
  - 106 dB SNR (signal through ADC with A-weighted filter)
  - 110 dB combined SNR (signal through DAC and headphone with A-weighted filter)
- Serial port sample rates from 8 kHz to 768 kHz
- 5 µs analog-to-analog group delay
- Programmable, double precision MAC engine for 13-stage equalizer
- 3 analog inputs (2 differential and 1 single-ended), configurable as microphone or line inputs
- Analog differential audio output, configurable as either line output or headphone driver
- PLL supporting any input clock rate from 30 kHz to 27 MHz
- 1-channel ASRCI, 3-channel ASRCO
- Serial audio ports supporting I^2S, left justified, or up to 16-channel TDM (TDM16)
- 2 interpolators and 4 decimators with flexible routing
- Power supplies
  - Analog AVDD at 1.8 V
  - Digital I/O IOVDD at 1.8 V to 3.3 V
  - Headphone HPVDD at 1.8 V
  - Headphone HPVDD_L at 1.2 V to1.8 V
- Control/communication interfaces
  - I^2C, SPI, or UART
- 28-ball, 0.4 mm pitch, 2.957 mm × 1.757 mm WLCSP

APPLICATIONS

- Noise canceling handsets, headsets, and headphones
- Bluetooth active noise canceling (ANC) handsets, headsets, and headphones
- Personal navigation devices
- Digital still and video cameras
- Musical instrument effect processors
- Multimedia speaker systems
- Smartphones

GENERAL DESCRIPTION

The ADAU1850 is a codec with three inputs and one output that incorporates one digital signal processor. The path from the analog input to the DSP core to the analog output is optimized for low latency and is ideal for noise canceling earphones. With the addition of a few passive components, the ADAU1850 provides a complete headset solution.

The ADAU1850 is provided in a small, 28-ball, 2.957 mm × 1.757 mm wafer level chip scale package (WLCSP).

Rev. 0

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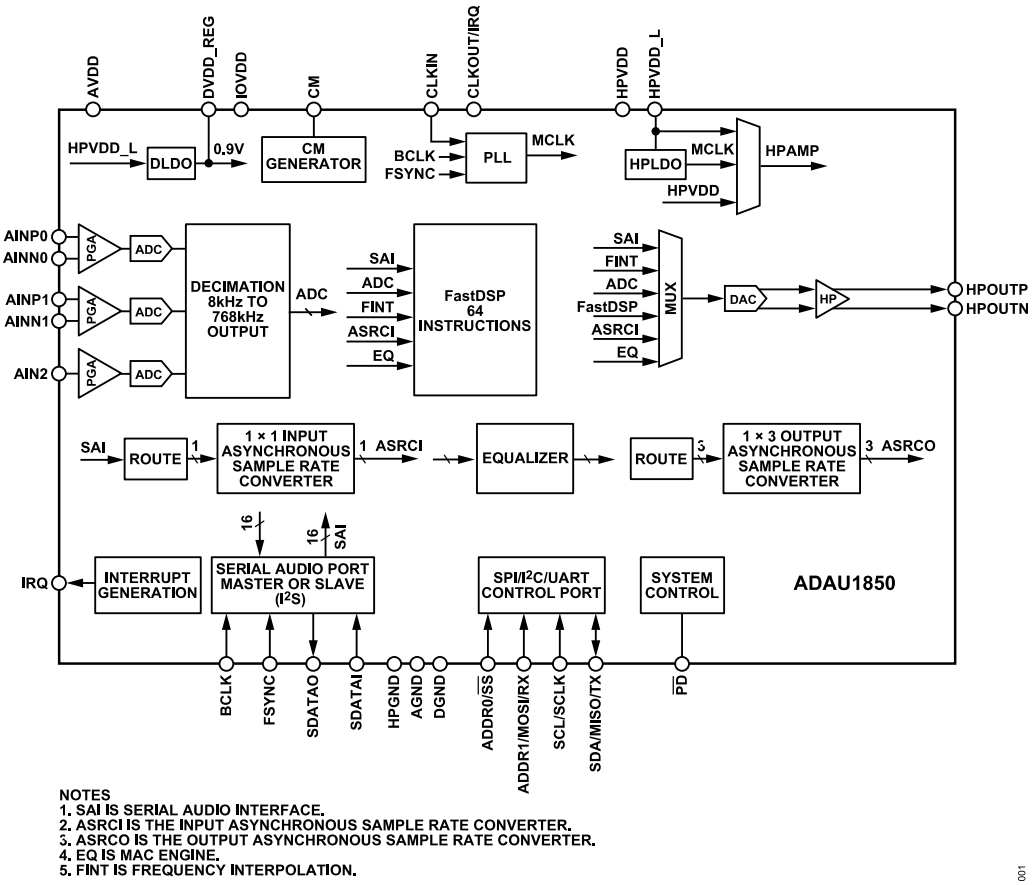
REVISION HISTORY

7/2021—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. SAI IS SERIAL AUDIO INTERFACE.
2. ASRCI IS THE INPUT ASYNCHRONOUS SAMPLE RATE CONVERTER.
3. ASRCO IS THE OUTPUT ASYNCHRONOUS SAMPLE RATE CONVERTER.
4. EQ IS MAC ENGINE.
5. FINT IS FREQUENCY INTERPOLATION.

Figure 1.

SPECIFICATIONS

Master clock = 24.576 MHz, serial input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, ambient temperature (T_A) = 25°C, line output load = 10 kΩ, unless otherwise noted.

ANALOG PERFORMANCE SPECIFICATIONS

Supply voltages: AVDD = HPVDD = IOVDD = 1.8 V, HPVDD_L = 1.2 V, unless otherwise noted.

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS (ADCs)					
ADC Resolution	All ADCs		24		Bits
Digital Gain Step			0.375		dB
Digital Gain Range		−71.25		+24	dB
INPUT RESISTANCE					
Single-Ended Line Input	Non voice wake-up mode		9		kΩ
	Voice wake-up mode		18		kΩ
Differential Line Input	Non voice wake-up mode		36		kΩ
	Voice wake-up mode		36		kΩ
Programmable Gain Amplifier (PGA) Single-Ended Inputs	PGA high resolution, normal, 0 dB gain		20.6		kΩ
	PGA high resolution, normal, 24 dB gain		2.4		kΩ
	PGA low resolution, enhanced, 0 dB gain		10.3		kΩ
	PGA low resolution, enhanced, 24 dB gain		1.2		kΩ
PGA Differential Inputs	PGA high resolution, normal, 0 dB gain		41.2		kΩ
	PGA high resolution, normal, 24 dB gain		4.8		kΩ
	PGA low resolution, enhanced, 0 dB gain		20.6		kΩ
	PGA low resolution, enhanced, 24 dB gain		2.4		kΩ
SINGLE-ENDED LINE INPUT	PGAx_EN = 0, PGAx_SLEW_DIS = 1				
Full-Scale Input Voltage	0 dBFS		0.49		V rms
	0 dBFS		1.39		V p-p
Dynamic Range[2]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		102		dB
	Normal performance		102		dB
	Power saving		101		dB
	Voice wake-up		98		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		98		dB
	Normal performance		98		dB
	Power saving		97		dB
	Voice wake-up		94		dB
Signal-to-Noise Ratio (SNR)[3]					
With A- Weighted Filter (RMS)	Enhanced performance		102		dB
	Normal performance		102		dB
	Power saving		101		dB
	Voice wake-up		98		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		98		dB
	Normal performance		98		dB
	Power saving		97		dB
	Voice wake-up		94		dB

SPECIFICATIONS

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Interchannel Gain Mismatch			40		mdB
Total Harmonic Distortion Plus Noise (THD + N)	20 Hz to 20 kHz, −1 dB full-scale output				
	Enhanced performance		−78		dBFS
	Normal performance		−78		dBFS
	Power saving		−78		dBFS
	Voice wake-up		−78		dBFS
Offset Error			±0.3		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		100		dB
Power Supply Rejection Ratio (PSRR)	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		60		dB
	100 mV p-p at 10 kHz		40		dB
DIFFERENTIAL LINE INPUT	PGAx_EN = 0, PGAx_SLEW_DIS = 1				
Full-Scale Input Voltage	0 dBFS		0.98		V rms
	0 dBFS		2.78		V p-p
Dynamic Range[2]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		106		dB
	Normal performance		106		dB
	Power saving		106		dB
	Voice wake-up		100		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		103		dB
	Normal performance		103		dB
	Power saving		103		dB
	Voice wake-up		99		dB
Signal-to-Noise Ratio (SNR)[3]					
With A-Weighted Filter (RMS)	Enhanced performance		106		dB
	Normal performance		106		dB
	Power saving		106		dB
	Voice wake-up		100		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		103		dB
	Normal performance		103		dB
	Power saving		103		dB
	Voice wake-up		99		dB
Interchannel Gain Mismatch			40		mdB
Total Harmonic Distortion + Noise (THD + N)	20 Hz to 20 kHz, −1 dB full-scale output				
	Enhanced performance		−96		dBFS
	Normal performance		−96		dBFS
	Power saving		−96		dBFS
	Voice wake-up		−94		dBFS
Offset Error			±0.2		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		100		dB
Power Supply Rejection Ratio (PSRR)	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		70		dB

SPECIFICATIONS

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
	100 mV p-p at 10 kHz		65		dB
SINGLE-ENDED PGA INPUT	PGAx_EN = 1				
Full-Scale Input Voltage	0 dBFS		0.49		V rms
	0 dBFS		1.39		V p-p
Dynamic Range[2]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		101		dB
	Normal performance		100		dB
	Power saving		100		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		97		dB
	Normal performance		96		dB
	Power saving		96		dB
	Voice wake-up		94		dB
Signal-to-Noise Ratio[3]					
With A-Weighted Filter (RMS)	Enhanced performance		101		dB
	Normal performance		100		dB
	Power saving		100		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		97		dB
	Normal performance		96		dB
	Power saving		96		dB
	Voice wake-up		94		dB
Total Harmonic Distortion + Noise	20 Hz to 20 kHz, −1 dBFS				
	Enhanced performance		−78		dBFS
	Normal performance		−78		dBFS
	Power saving		−78		dBFS
	Voice wake-up		−78		dBFS
PGA Gain Range		0		24	dB
PGA Gain Variation					
With 0 dB Setting	Standard deviation		0.05		dB
With 24 dB Setting	Standard deviation		0.15		dB
Interchannel Gain Mismatch			50		mdB
Offset Error			0.3		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		83		dB
Power Supply Rejection Ratio (PSRR)	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		60		dB
	100 mV p-p at 10 kHz		50		dB
DIFFERENTIAL PGA INPUT	PGAx_EN = 1				
Full-Scale Input Voltage	0 dBFS		0.98		V rms
	0 dBFS		2.78		V p-p
Dynamic Range[2]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		104		dB
	Normal performance		103		dB

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Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
	Power saving		103		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		102		dB
	Normal performance		101		dB
	Power saving		101		dB
	Voice wake-up		96		dB
Signal-to-Noise Ratio[3]					
With A-Weighted Filter (RMS)	Enhanced performance		104		dB
	Normal performance		103		dB
	Power saving		103		dB
	Voice wake-up		97		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		102		dB
	Normal performance		101		dB
	Power saving		101		dB
	Voice wake-up		96		dB
Total Harmonic Distortion + Noise	20 Hz to 20 kHz, −1 dBFS				
	Enhanced performance		−95		dBFS
	Normal performance		−95		dBFS
	Power saving		−95		dBFS
	Voice wake-up		−93		dBFS
PGA Gain Range		0		24	dB
PGA Gain Variation					
With 0 dB Setting	Standard deviation		0.05		dB
With 24 dB Setting	Standard deviation		0.15		dB
Interchannel Gain Mismatch			0.04		mdB
Offset Error			±0.2		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 1 µF		100		dB
Power Supply Rejection Ratio (PSRR)	CM capacitor = 1 µF				
	100 mV p-p at 1 kHz		70		dB
	100 mV p-p at 10 kHz		65		dB
DIGITAL-TO-ANALOG CONVERTERS (DACs)					
Internal Converter Resolution	All DACs		24		Bits
Digital Gain					
Step			0.375		dB
Range		−71.25		+24	dB
Ramp Rate			4.5		dB/ms
DAC DIFFERENTIAL OUTPUT	Differential operation				
Full-Scale Output Voltage	0 dBFS to DAC		1.0		V rms
Dynamic Range[2]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	Enhanced performance		110		dB
	Normal performance		105		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		107		dB
	Normal performance		102		dB

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Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Signal-to-Noise Ratio[3]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	Enhanced performance		110		dB
	Normal performance		105		dB
With Flat 20 Hz to 20 kHz Filter	Enhanced performance		107		dB
	Normal performance		102		dB
Total Harmonic Distortion + Noise Level	Headphone mode				
32 Ω Load	−15 dBFS input, output power (P_{OUT}) = 1 mW, enhanced performace		−96		dBV
	−15 dBFS input, P_{OUT} = 1 mW, normal performance		−85		dBV
	−1 dBFS input, enhanced performance		−84		dBV
	−1 dBFS input, normal performance		−75		dBV
24 Ω Load	−2 dBFS input, enhanced performance		−84		dBV
	−2 dBFS input, normal performance		−75		dBV
16 Ω Load	−3 dBFS input, enhanced performance		−84		dBV
	−3 dBFS input, normal performance		−75		dBV
32 Ω Load	Low voltage mode, P_{OUT} = 10 mW, enhanced performance		−90		dBV
Gain Error			±2.5		%
DC Offset			±0.1		mV
Power Supply Rejection Ratio	CM capacitor = 1 µF				
HPVDD	100 mV p-p at 1 kHz		80		dB
	100 mV p-p at 10 kHz		80		dB
HPVDD_L (Low Dropout Regulator (LDO) By-pass)	100 mV p-p at 1 kHz		85		dB
	100 mV p-p at 10 kHz		85		dB
AVDD Undervoltage Trip Point			1.5		V
CM REFERENCE	CM pin				
Output			0.85		V
Source Impedance			5		kΩ
PLL					
Input Frequency	After input prescale	0.03		27	MHz
Output Frequency			24.576		MHz
Fractional Limits	Fractional mode, fraction part (numerator (N)/denominator (M))	0.1		0.9	
Integer Limits	Fractional mode, integer part	2		3072	
Lock Time	48 kHz input		6.5		ms
	12.288 MHz input		0.46	0.55	ms
DVDD REGULATOR					
Line Regulation			1		mV/V
Load Regulation			0.5		mV/mA

[1] See the ADAU1850 Hardware Reference Manual for register details.

[2] Dynamic range is the ratio of the sum of noise and harmonic power in the band of interest with a −60 dBFS signal present to the full-scale power level, in decibels.

[3] SNR is the ratio of the sum of all noise power in the band of interest with no signal present to the full-scale power level in decibels.

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DIGITAL INPUT AND OUTPUT SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 1.8 V to 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbols	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE						
High	V_{IH}		0.7 × IOVDD			V
Low	V_{IL}				0.3 × IOVDD	V
INPUT LEAKAGE						
High	I_{IH}	IOVDD = 1.8 V, V_{IH} = 1.1 V			10	µA
Low	I_{IL}	V_{IL} = 0.45 V			10	µA
OUTPUT VOLTAGE HIGH	V_{OH}					
Drive Strength						
Low		Output high current (I_{OH}) = 1 mA	0.7 × IOVDD	0.83 × IOVDD		V
High		I_{OH} = 3 mA	0.7 × IOVDD	0.83 × IOVDD		V
OUTPUT VOLTAGE LOW	V_{OL}					
Drive Strength						
Low		Output low current (I_{OL}) = 1 mA		0.1 × IOVDD	0.3 × IOVDD	V
High		I_{OL} = 3 mA		0.1 × IOVDD	0.3 × IOVDD	V
INPUT CAPACITANCE					5	pF

POWER SUPPLY SPECIFICATIONS

Supply voltages: AVDD = HPVDD = IOVDD = 1.8 V, unless otherwise noted. Digital input/output (I/O) lines loaded with 25 pF.

Table 3.

Parameter	Min	Typ	Max	Unit
SUPPLIES				
AVDD Voltage	1.7	1.8	1.98	V
HPVDD Voltage	1.7	1.8	1.98	V
IOVDD Voltage	1.62		3.63	V
HPVDD_L Voltage	1.17		HPVDD	V

POWER-DOWN CURRENT

Supply voltages: AVDD = HPVDD = IOVDD = 1.8 V and HPVDD_L = 1.2 V. PLL disabled and bypassed.

Table 4.

	AVDD Current			DVDD Current			IOVDD Current			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
$\overline{PD}$ PIN LOW (HARDWARE POWER-DOWN)		4.4			2.1			0.7		µA
POWER_EN = 0										
No Keep Alives		75			187			23		µA
KEEP_MEM = 1		75			187			23		µA

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TYPICAL POWER CONSUMPTION

Input clock = 24.576 MHz, PLL disabled, AVDD = HPVDD = IOVDD = 1.8 V, and HPVDD_L = 1.2 V supplied externally. Where applicable, ADC0 and ADC1 running at 192 kHz and differential mode, and ADC2 running at 192 kHz. FastDSP™ running at 192 kHz (biquad filters with 27-bit precision). DAC running at 192 kHz, DAC_LPM = 0. One serial port input and output, configured as a slave, with headphone load of 32 Ω. DVDD current is measured from HPVDD_L pin, DAC HPAMP(Headphone Amplifier) works in normal voltage mode. Quiescent current (no signal).

Table 5. Power Supply Current in Different Configuration

ADC Channels	DAC Channels	ASRCI/ ASRCO Channels	FastDSP Instructions	Interpolator/ Decimator Channels	Equalizer	DVDD Current (mA)	AVDD Current (mA)	IOVDD Current (mA)
2	1	0/0	32	0	0	1.051	2.326	0.024
3	1	1/3	40	0	1	2.221	2.733	0.154
1	1	1/1	0	0	1	1.052	1.818	0.090
2	1	1/0	32	0	1	1.643	2.327	0.024
0	1	1/0	0	0	1	0.846	0.995	0.024

Typical active noise canceling (ANC) settings with different power mode. Master clock = 24.576 MHz (PLL bypassed and disabled). AVDD = HPVDD = IOVDD = 1.8 V, and HPVDD_L = 1.2 V supplied externally. Two ADCs without PGA and configured in differential mode. The DAC configured for differential headphone operation at low voltage mode, which is supplied by HPVDD_L, and DAC output loaded with 32 Ω, 1 mW output, DAC_LPM = 0. FastDSP running 32 instructions (biquad filters with 27-bit precision) at 192 kHz. DVDD current is measured from HPVDD_L pin.

Table 6. Power Consumption in ANC Mode

		Typical Current (mA)			
Operating Voltage	Power Management Setting	AVDD	DVDD	IOVDD	Total Power Consumption (mW)
AVDD = IOVDD = 1.8 V	ADC power saving mode, DAC normal mode	1.513	5.961	0.024	9.92
HPVDD_L = 1.2V	ADC power saving mode, DAC enhanced mode	1.966	6.007	0.024	10.79

DIGITAL FILTERS

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC INPUT TO DAC OUTPUT PATH					
Pass-Band Ripple	DC to 20 kHz, sampling frequency (f_S) = 192 kHz (ADC_FCOMP = 1, DAC_FCOMP = 1)			±0.02	dB
Group Delay[1]	f_S = 192 kHz		12.9		µs
	f_S = 384 kHz		7.5		µs
	f_S = 768 kHz		5		µs
SAMPLE RATE CONVERTER					
Pass Band	FSYNC clock < 63 kHz			0.475 × f_S	kHz
	63 kHz < FSYNC clock < 112 kHz			0.4286 × f_S	
	FSYNC clock > 112 kHz		0.2383 × f_S		
Audio Band Ripple	20 Hz to 20 kHz	−0.1		+0.1	dB
Input and Output Sample Frequency Range		7		224	kHz
Dynamic Range	ASRCx_LPM = 0		130		dB
	ASRCx_LPM = 1		130		dB
	ASCRx_LPM_II = 1		130		dB
THD + N	20 Hz to 20 kHz, input: typical at 1 kHz and maximum at 20 kHz				
	ASRCx_LPM = 0		−130	−120	dBFS
	ASRCx_LPM = 1		−120	−110	dBFS
	ASRCx_LPM_II = 1		−115	−90	dBFS

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Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Start-Up Time to Lock				25	ms

[1] Group delay measured with FastDSP using zero instructions.

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 1.8 V to 3.3 V. Multifunction pins, such as SCL/SCLK, are referred to by a single function of the pin, for example, SCLK, when only that function is relevant. See the Pin Configuration and Function Descriptions section for full pin names and descriptions.

Table 8. Digital Timing

Parameter	Min	Typ	Max	Unit	Description
MASTER CLOCK					CLKIN period
t_{MPI}	0.037		33.3	µs	30 kHz to 27 MHz input clock using PLL in integer mode
t_{MPF}	0.037		1.0	µs	1 MHz to 27 MHz input clock using PLL in fractional mode
SERIAL PORT					See Figure 2 and Figure 3
t_{BL}	18			ns	BCLK low pulse width (master and slave modes)
t_{BH}	18			ns	BCLK high pulse width (master and slave modes)
f_{BCLK}	0.512		24.576	MHz	BCLK frequency
t_{LS}	3			ns	FSYNC setup, time to BCLK rising (slave mode)
t_{LH}	5			ns	FSYNC hold, time from BCLK rising (slave mode)
f_{SYNC}	8		768	kHz	FSYNC frequency
t_{SS}	3			ns	SDATAI setup, time to BCLK rising (master and slave modes)
t_{SH}	10			ns	SDATAI hold, time from BCLK rising (master and slave modes)
t_{TS}			6	ns	BCLK falling to FSYNC timing skew (master mode)
t_{SOD}	0		16	ns	SDATAO delay, time from BCLK falling (master and slave modes), IOVDD at 1.62 V minimum
	0		32	ns	SDATAO delay, time from BCLK falling (master and slave modes), IOVDD at 1.1 V minimum
t_{SOTD}	0		16	ns	BCLK falling to SDATAO driven in tristate mode
t_{SOTX}	0		16	ns	BCLK falling to SDATAO tristated in tristate mode
SERIAL PERIPHERAL INTEFACE (SPI) PORT					See Figure 4
f_{SCLK}			24	MHz	SCLK frequency
t_{CCPL}	15			ns	SCLK pulse width low
t_{CCPH}	15			ns	SCLK pulse width high
t_{CLS}	4			ns	$\overline{SS}$ setup, time to SCLK rising
t_{CLH}	18			ns	$\overline{SS}$ hold, time from SCLK rising
t_{CLPH}	10			ns	$\overline{SS}$ pulse width high
t_{CDS}	8			ns	MOSI setup, time to SCLK rising
t_{CDH}	6			ns	MOSI hold, time from SCLK rising
t_{COD}			17	ns	MISO delay, time from SCLK falling
t_{COTS}			24	ns	MISO high-Z, time from $\overline{SS}$ rising
I^2C PORT					See Figure 5
f_{SCL}			1	MHz	SCL frequency
t_{SCLH}	0.26			µs	SCL high
t_{SCLL}	0.5			µs	SCL low
t_{SCS}	0.26			µs	SCL rise setup time (to SDA falling), relevant for repeated start condition
t_{SCR}			120	ns	SCL and SDA rise time, load capacitance (C_{LOAD}) = 400 pF
t_{SCH}	0.26			µs	SCL fall hold time (from SDA falling), relevant for start condition
t_{DS}	50			ns	SDA setup time (to SCL rising)

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Table 8. Digital Timing

Parameter	Min	Typ	Max	Unit	Description
t_{SCF}			120	ns	SCL and SDA fall time, C_{LOAD} = 400 pF
t_{BFT}	0.5			µs	SCL rise setup time (to SDA rising), relevant for stop condition
UART			1.152	Mbps	Baud rate
$\overline{PD}$ PIN					
t_{RLPW}	20			ns	$\overline{PD}$ low pulse width

Digital Timing Diagrams

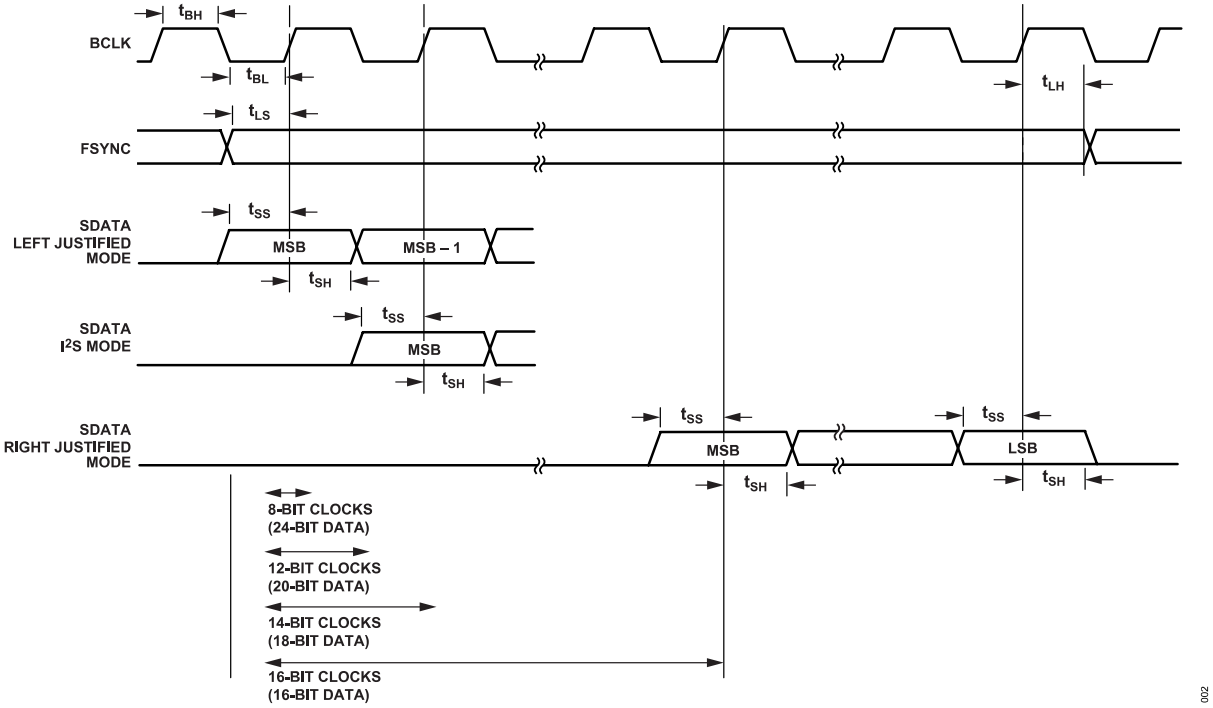

Figure 2. Serial Input Port Timing Diagram

SPECIFICATIONS

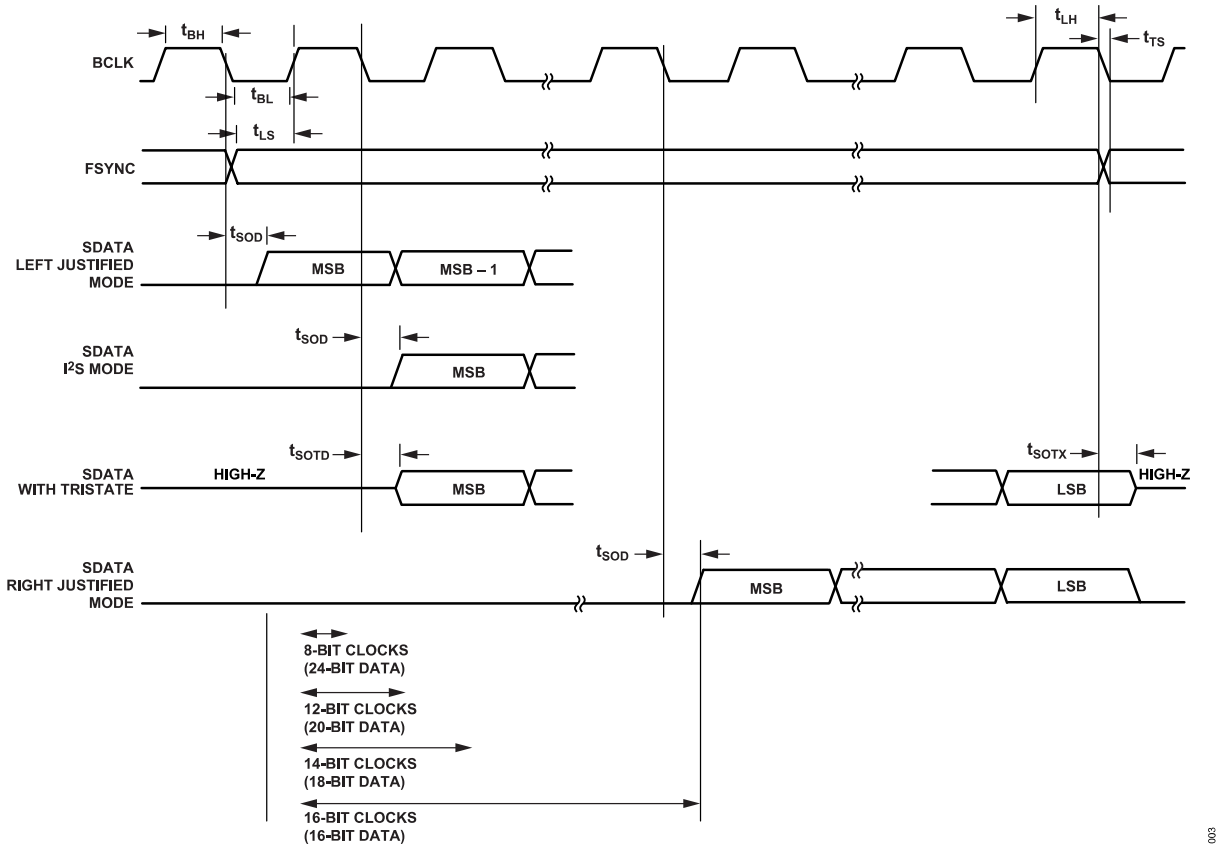

Figure 3. Serial Output Port Timing Diagram

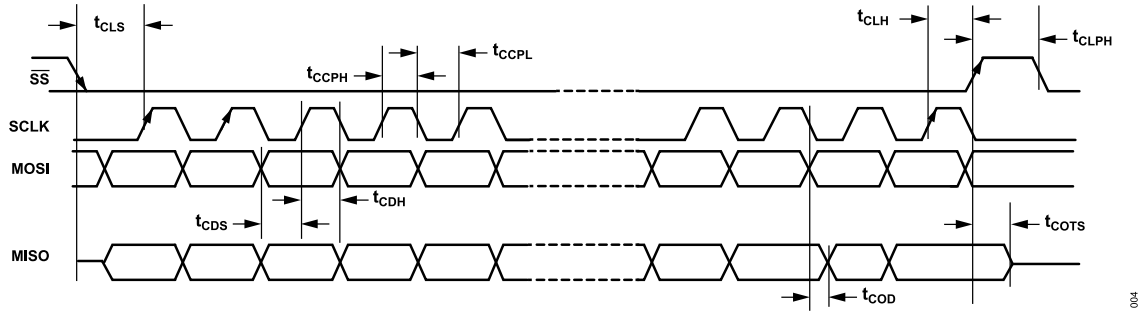

Figure 4. SPI Port Timing Diagram

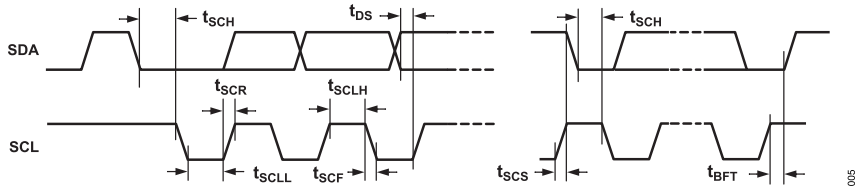

Figure 5. I²C Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
Supply	
Power (AVDD, HPVDD, HPVDD_L)	−0.3 V to +1.98 V
IOVDD	−0.3 V to +3.63 V
Input	
Current (Except Supply Pins)	±20 mA
Analog Voltage (Signal Pins)	–0.3 V to AVDD + 0.3 V
Digital Voltage (Signal Pins)	−0.3 to IOVDD + 0.3 V
Temperature	
Operating Range (Case)	−40°C to +85°C
Storage Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 10. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
CB-28-5	94	1.1	°C/W

Table 10. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with two thermal vias. θ_{JA} and θ_{JC} are determined according to JESD51-9 on a 4-layer PCB with natural convection cooling.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAU1850

Table 11. ADAU1850, 28-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class Level
HBM	1000	1C
CDM	500	C2a

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

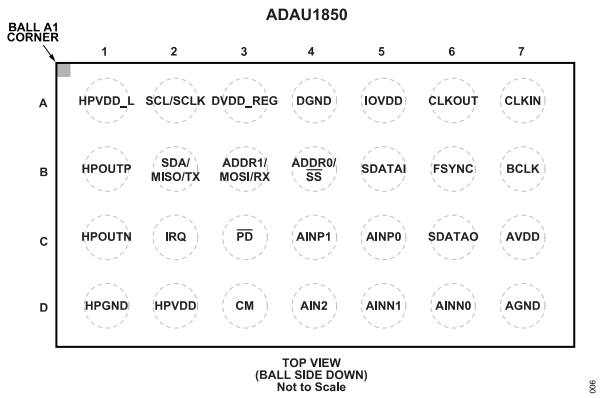

Figure 6. Pin Configuration (Top View)

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	HPVDD_L	PWR	Headphone Amplifier Power, 1.2 V Analog Supply. Decouple this pin to HPGND with a 10 µF capacitor. The PCB trace to this pin must be wider to supply the higher current necessary for driving the headphone outputs.
A2	SCL/SCLK	D_IN	I²C Clock (SCL). This pin is always an open-collector input when the device is in I²C control mode. The line connected to this pin must have a 2.0 kΩ pull-up resistor. SPI Clock (SCLK). This pin can either run continuously or be gated off between SPI transactions.
A3	DVDD_REG	PWR	Internal DVDD regulator supply output. Decouple this pin to DGND via a 1 µF and 0.1 µF capacitor.
A4	DGND	PWR	Digital Ground. The AGND and DGND pins can be tied together in a common ground plane.
A5	IOVDD	PWR	Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, and this supply sets the highest input voltage that is seen on the digital input pins. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. Decouple IOVDD to DGND with a ≥0.1 µF capacitor.
A6	CLKOUT/IRQ	D_OUT	Clock Output (CLKOUT). CLKOUT is the default function of this multifunction pin. Interrupt Request Output (IRQ).
A7	CLKIN	D_IN	Clock Input.
B1	HPOUTP	A_OUT	Headphone Output Noninverted.
B2	SDA/MISO/TX	D_IO	I²C Data (SDA). This pin is a bidirectional open-collector. The line connected to this pin must have a 2.0 kΩ pull-up resistor. SPI Data Output (MISO). This SPI data output is used for reading back registers and memory locations. MISO is tristated when an SPI read is not active. UART Port Data Transmit/Output (TX).
B3	ADDR1/MOSI/RX	D_IN	I²C Address 1 (ADDR1). SPI Data Input (MOSI). UART Port Data Transmit/Input (RX).
B4	ADDR0/$\overline{SS}$	D_IN	I²C Address 0 (ADDR0). SPI Latch Signal ($\overline{SS}$). This pin must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of SCLK cycles to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction.
B5	SDATAI	D_IN	Serial Audio Port Input Data.
B6	FSYNC	D_IN	Serial Audio Port Frame Synchronization/Left Right Clock.
B7	BCLK	D_IN	Serial Audio Port Bit Clock.
C1	HPOUTN	A_OUT	Headphone Output Inverted.
C2	IRQ	D_OUT	Interrupt Request Output.
C3	$\overline{PD}$	D_IN	Active Low Power-Down. All digital and analog circuits are powered down. There is an internal pull-down resistor on this pin; therefore, the ADAU1850 is held in power-down mode if its input signal is floating while power is applied to the supply pins.
C4	AINP1	A_IN	ADC1 Noninverting Input.
C5	AINP0	A_IN	ADC0 Noninverting Input.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
C6	SDATAO	D_OUT	Serial Audio Port Output Data.
C7	AVDD	PWR	1.8 V Analog Supply. Decouple this pin to AGND with a 10 µF capacitor.
D1	HPGND	PWR	Headphone Amplifier Ground.
D2	HPVDD	PWR	Headphone Amplifier Power, 1.8 V Analog Supply. Decouple this pin to HPGND with a 10 µF capacitor. The PCB trace to this pin must be wider to supply the higher current necessary for driving the headphone outputs.
D3	CM	A_OUT	Common-Mode Reference, Fixed at 0.85 V Nominal. Connect a 1 µF decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp).
D4	AIN2	A_IN	ADC2 Input. ADC2 is a single-end input ADC.
D5	AINN1	A_IN	ADC1 Inverting Input.
D6	AINN0	A_IN	ADC0 Inverting Input.
D7	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane.

[1] D_IO means digital input/output, PWR means power, A_OUT means analog output, D_IN means digital input, D_OUT means digital output, and A_IN means analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

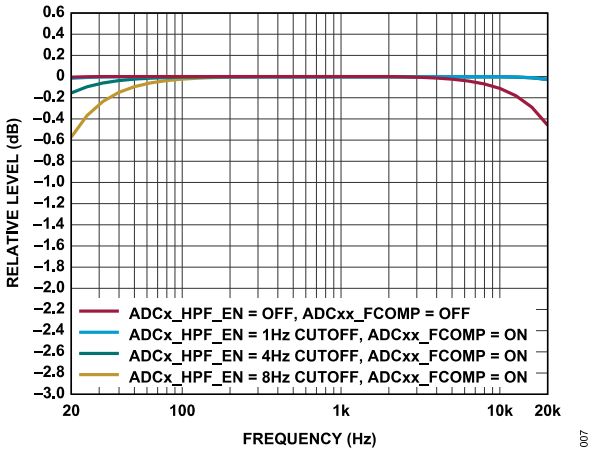

Figure 7. Frequency Response, f_S = 48 kHz, −20 dBV Input, Signal Path = AINx to SDATAO, No PGA, ADC0 and ADC1 Differential Mode, ADC2 Single-Ended Mode

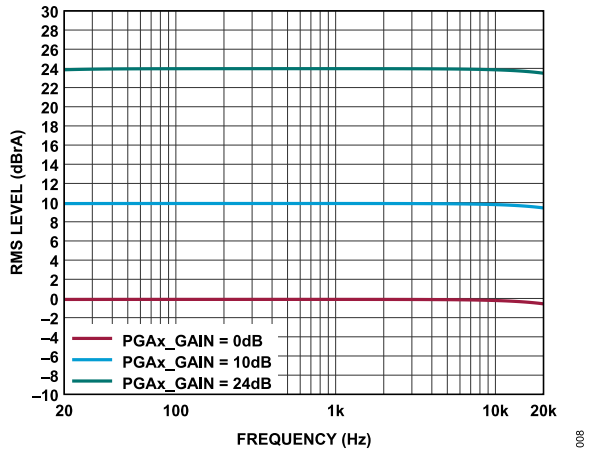

Figure 8. Frequency Response, f_S = 48 kHz, Signal Path = AINx to SDATAO, Output Relative to PGA Gain Settings (0 dB, 10 dB, 24 dB)

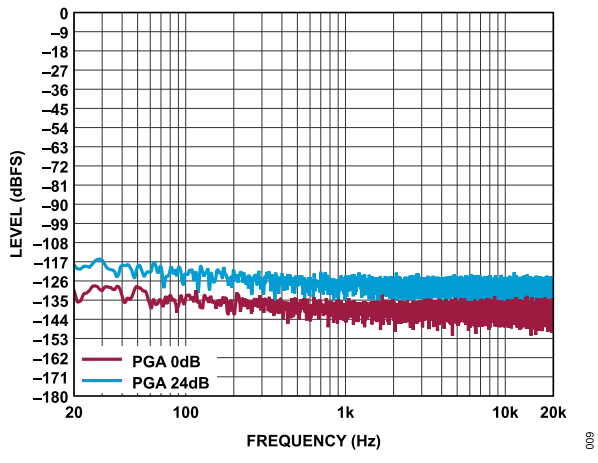

Figure 9. FFT, No Signal, f_S = 48 kHz, Signal Path = AINx to SDATAO, PGA = 0 dB and 24 dB (PGAx_GAIN), ADC0 and ADC1 Differential Mode

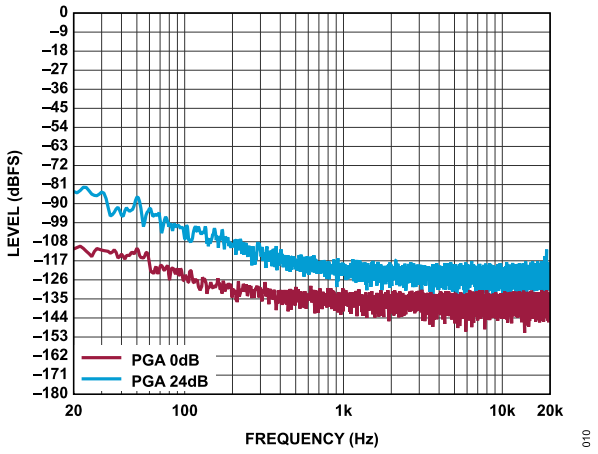

Figure 10. FFT, No Signal, f_S = 48 kHz, Signal Path = AINx to SDATAO, PGA = 0 dB and 24 dB (PGAx_GAIN), ADC2 Single-Ended Mode

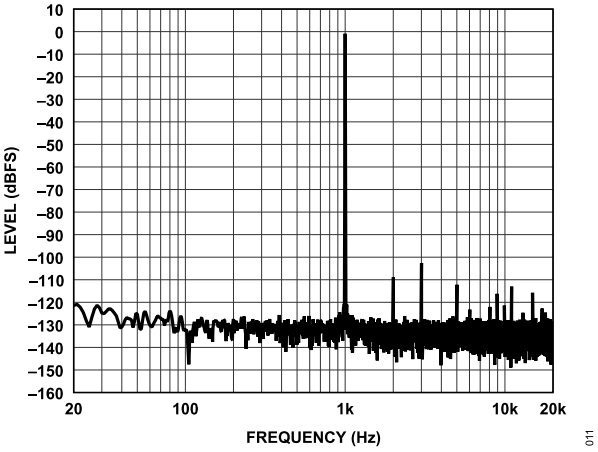

Figure 11. FFT, −7 dBV Input, −1 dBFS Output, f_S = 48 kHz, Signal Path = AINx to SDATAO, No PGA, ADC0 and ADC1 Differential Mode

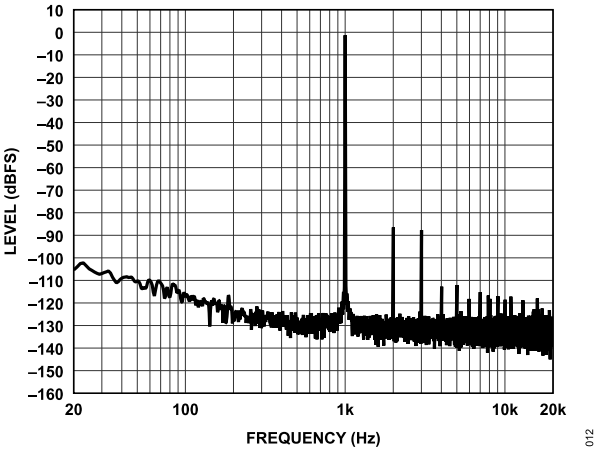

Figure 12. FFT, −7 dBV Input, −1 dBFS Output, f_S = 48 kHz, Signal Path = AINx to SDATAO, No PGA, ADC2 Single-Ended Mode

TYPICAL PERFORMANCE CHARACTERISTICS

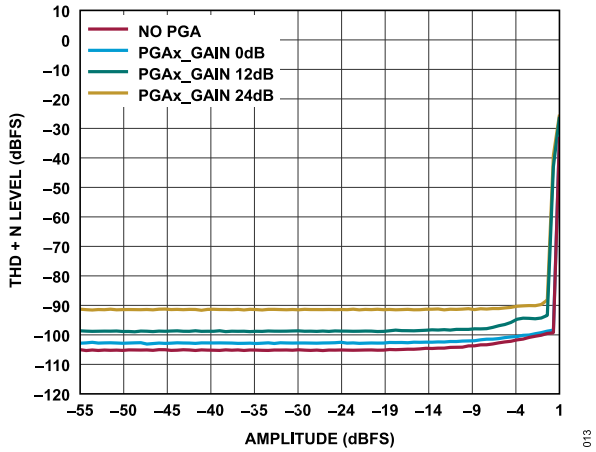

Figure 13. THD + N Level vs. Amplitude, f_S = 48 kHz, Signal Path = AINx to SDATAO, No PGA and PGA Gain Settings (0 dB, 12 dB, 24 dB), ADC0 and ADC1 Differential Mode

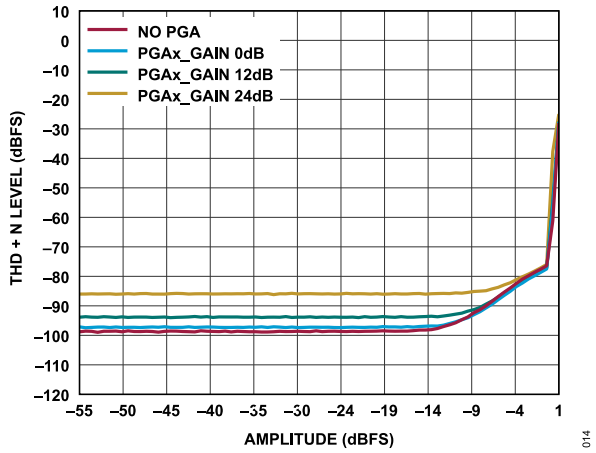

Figure 14. THD + N Level vs. Amplitude, f_S = 48 kHz, Signal Path = AINx to SDATAO, No PGA and PGA Gain Settings (0 dB, 12 dB, 24 dB), ADC2 Single-Ended Mode

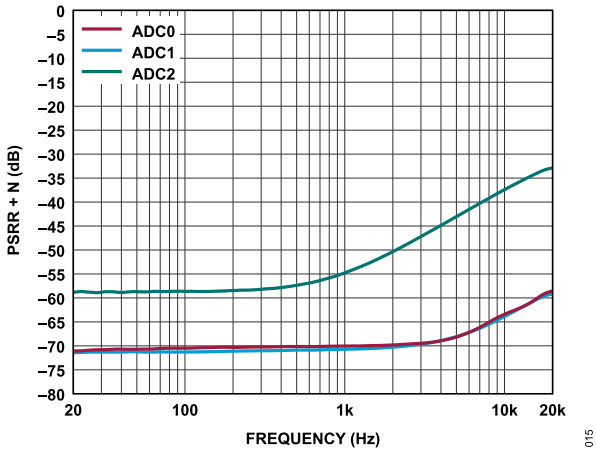

Figure 15. PSRR + N, Signal Path = AINx to SDATAO, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD, No PGA, ADC0 and 1 Differential Mode, ADC2 Single-Ended Mode

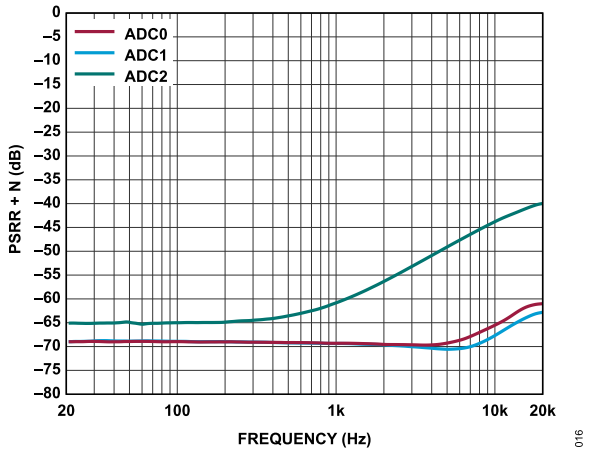

Figure 16. PSRR + N, Signal Path = AINx to SDATAO, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD, PGA = 0 dB, ADC0 and ADC1 Differential Mode, ADC2 Single-Ended Mode

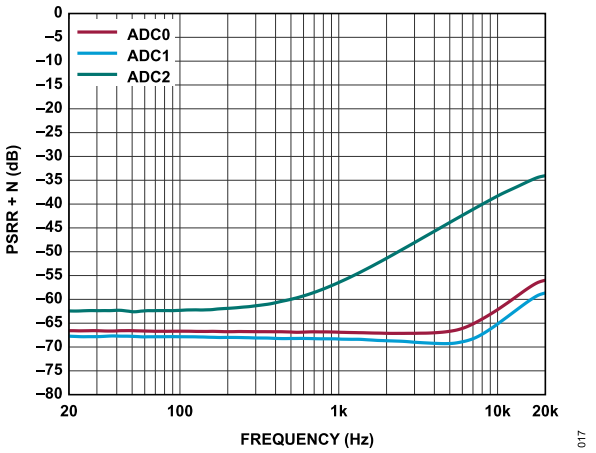

Figure 17. PSRR + N, Signal Path = AINx to SDATAO, f_S = 48 kHz, 100 mV p-p Ripple Input on AVDD, PGA = 10 dB, ADC0 and ADC1 Differential Mode, ADC2 Single-Ended Mode

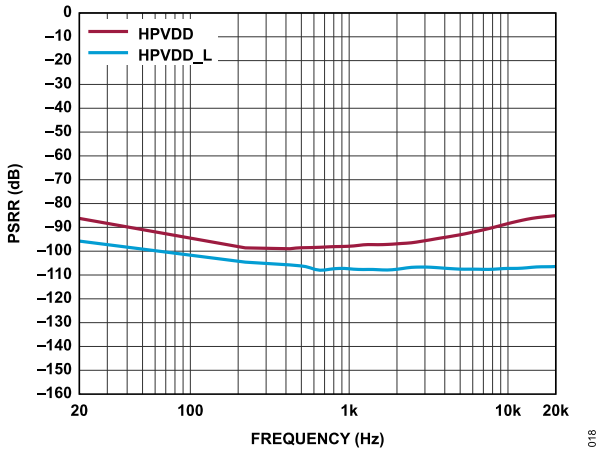

Figure 18. PSRR, Signal Path = SDATAI to Headphone Output, f_S = 48 kHz, 100 mV p-p Ripple Input on HPVDD and HPVDD_L, Load = 32 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

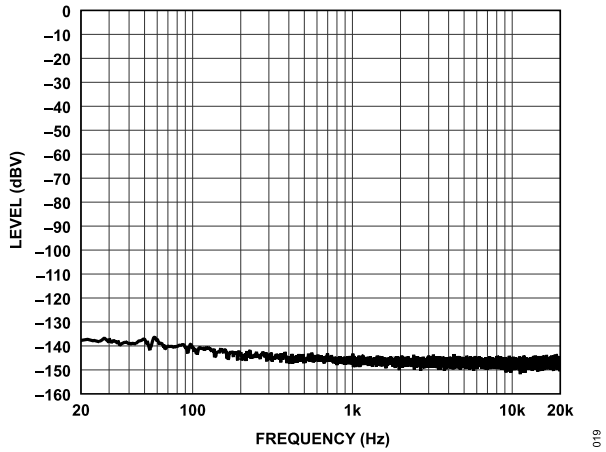

Figure 19. FFT, No Signal, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output, Headphone Mode, Load = 16 Ω

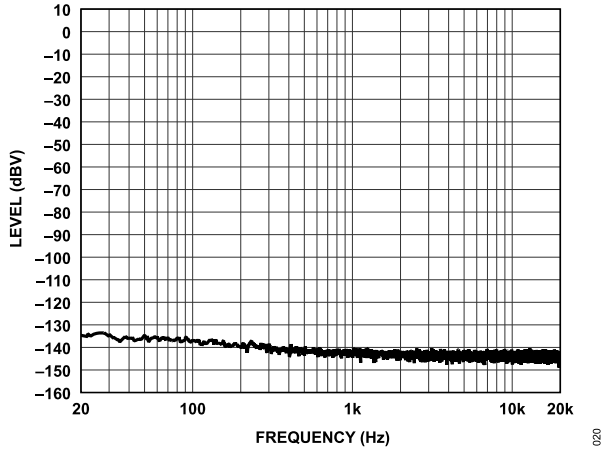

Figure 20. FFT, No Signal, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output, Line Output Mode, Load = 10 kΩ

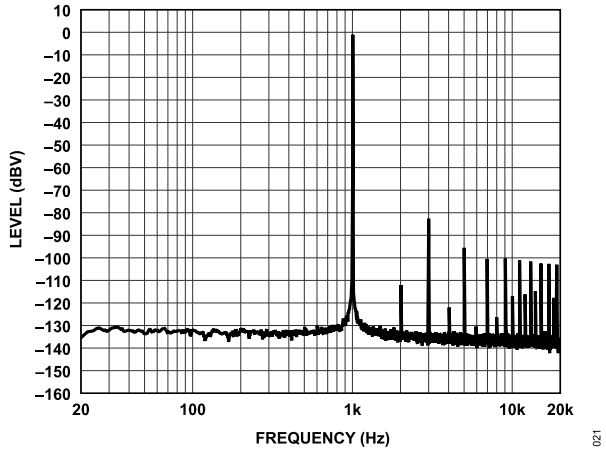

Figure 21. FFT, −1 dBFS, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output, Headphone Mode, Load = 32 Ω

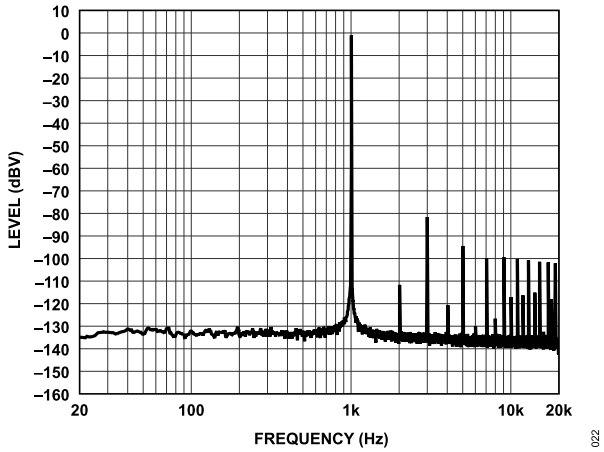

Figure 22. FFT, −1 dBFS, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output, Headphone Mode, Load = 24 Ω

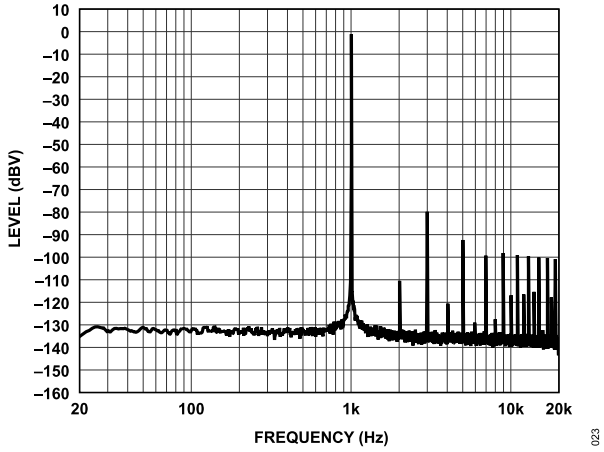

Figure 23. FFT, −1 dBFS, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output, Headphone Mode, Load = 16 Ω

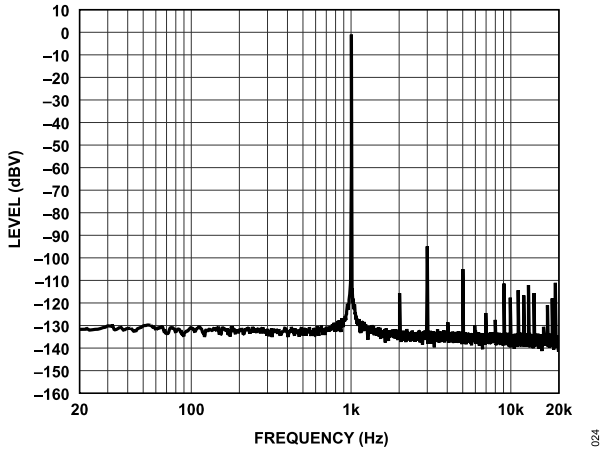

Figure 24. FFT, −1 dBFS, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output, Line Output Mode, Load = 10 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

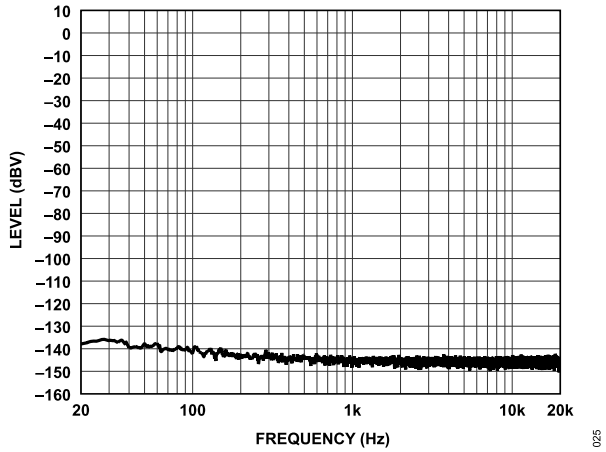

Figure 25. FFT, No Signal, f_S = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Headphone Output, Headphone Mode, Load = 16 Ω

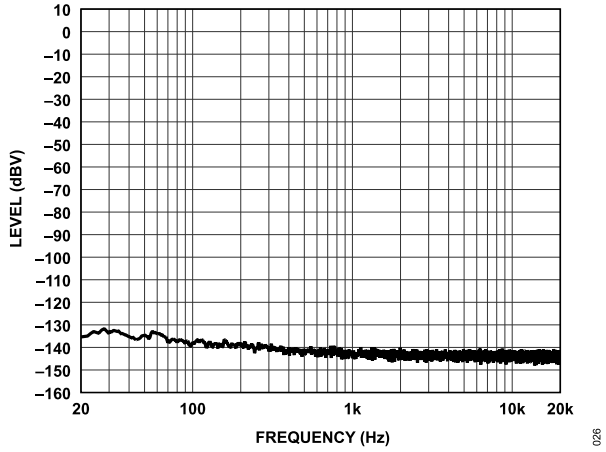

Figure 26. FFT, No Signal, f_S = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Headphone Output, Line Output Mode, Load = 10 kΩ

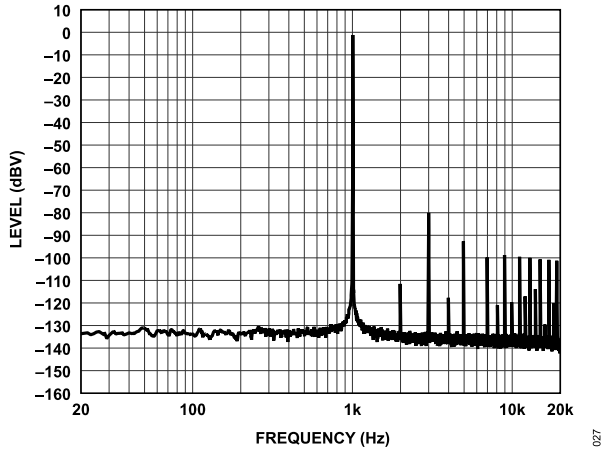

Figure 27. FFT, −1 dBFS, f_S = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Headphone Output, Headphone Mode, Load = 16 Ω

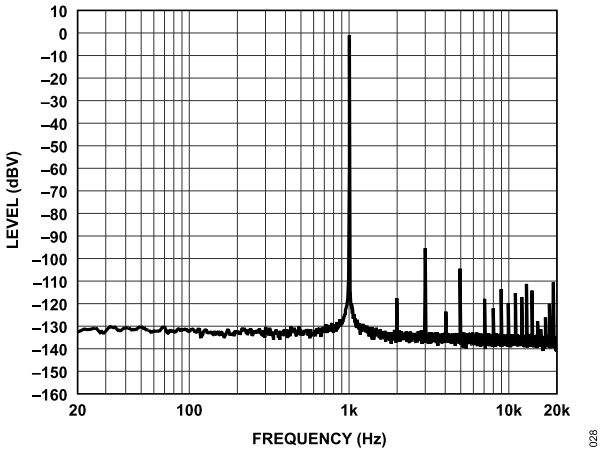

Figure 28. FFT, −1 dBFS, f_S = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Headphone Output, Line Output Mode, Load = 10 kΩ

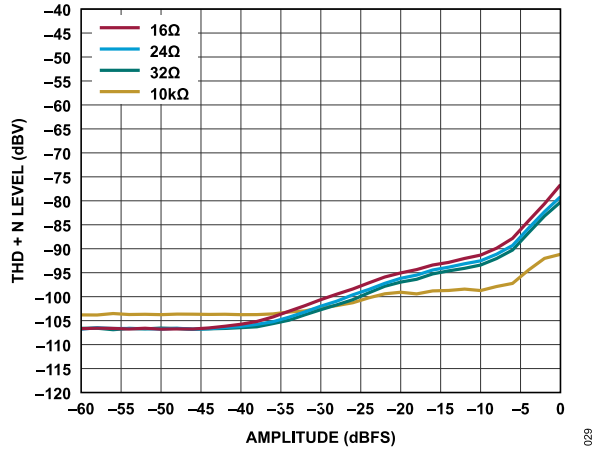

Figure 29. THD + N Level vs. Input Amplitude, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output (16 Ω, 24 Ω, 32 Ω) or Line Output Mode (10 kΩ)

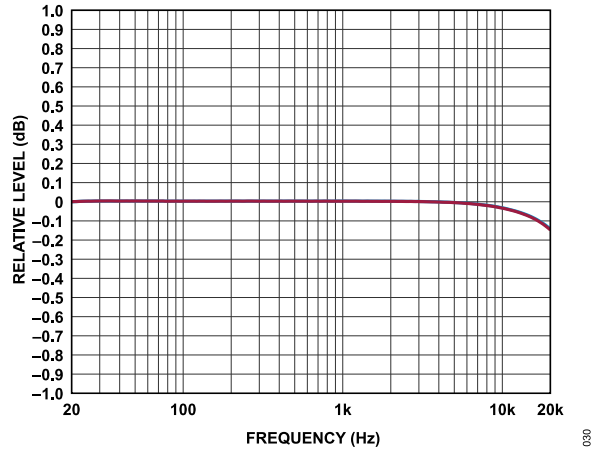

Figure 30. Relative Level vs. Frequency, f_S = 48 kHz, Signal Path = SDATAI to Headphone Output (16 Ω) or Line Output Mode (10 kΩ)

TYPICAL PERFORMANCE CHARACTERISTICS

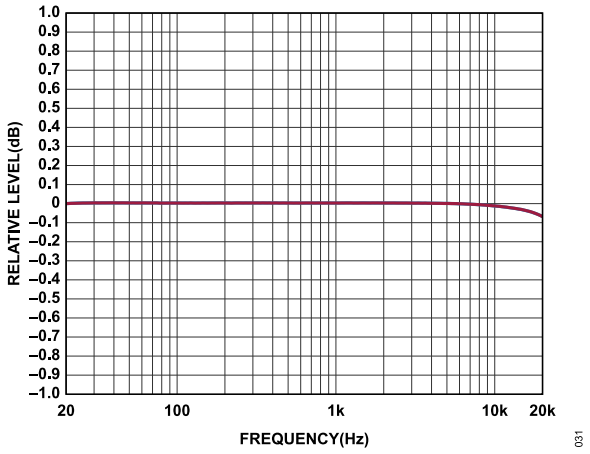

Figure 31. Relative Level vs. Frequency, f_S = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Headphone Output (16 Ω) or Line Output Mode (10 kΩ)

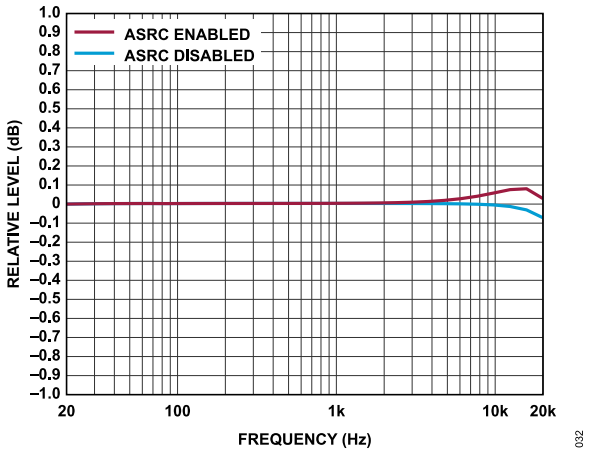

Figure 32. Relative Level vs. Frequency, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI to ASRCI to Equalizer to Interpolator to FastDSP to Decimator to ASRCO to SDATAO

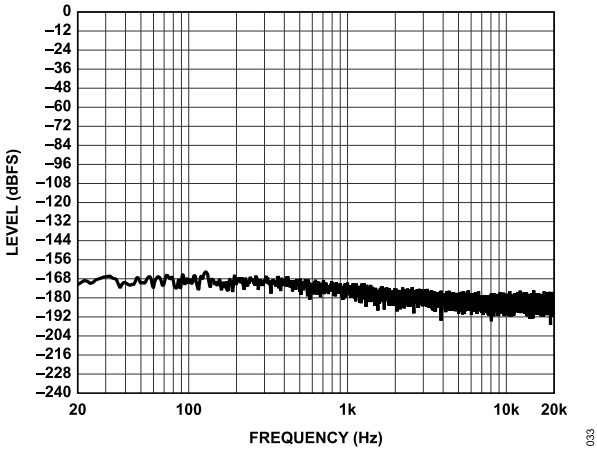

Figure 33. FFT, No Signal, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI to ASRCI to Equalizer to Interpolator to FastDSP to Decimator to ASRCO to SDATAO

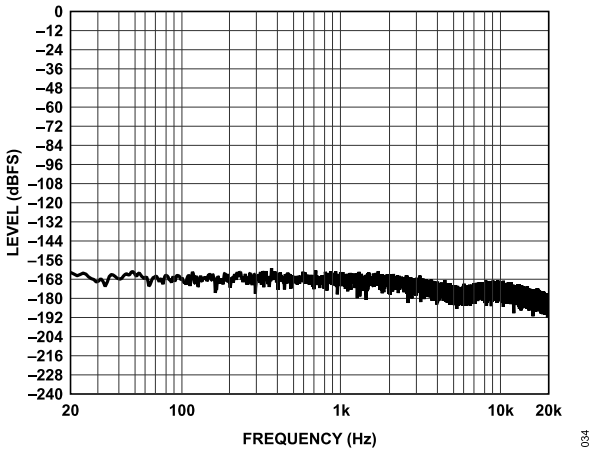

Figure 34. FFT, No Signal, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Decimator to SDATAO

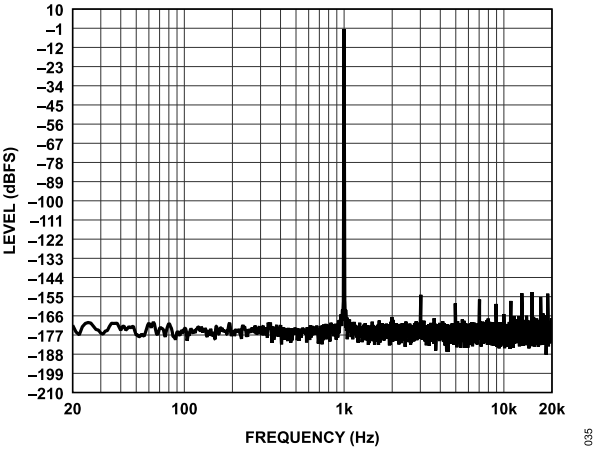

Figure 35. FFT, −1 dBFS, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI to ASRCI to Equalizer to Interpolator to FastDSP to Decimator to ASRCO to SDATAO

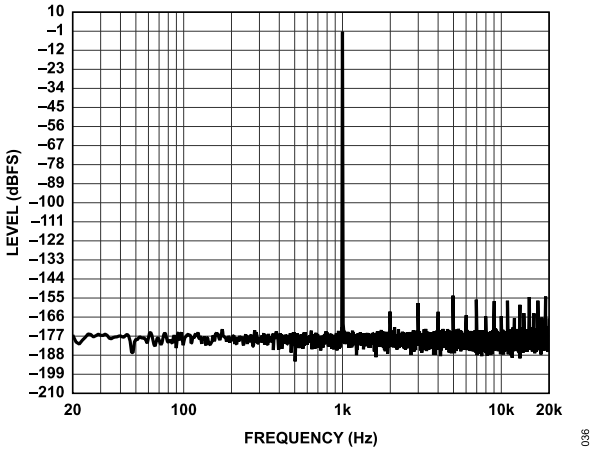

Figure 36. FFT, −1 dBFS, f_S = 48 kHz Throughout Except FastDSP = 768 kHz, Signal Path = SDATAI to Interpolator to FastDSP to Decimator to SDATAO

TYPICAL PERFORMANCE CHARACTERISTICS

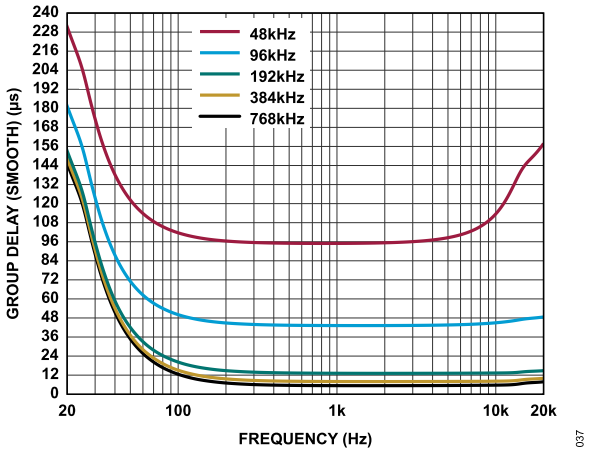

Figure 37. Group Delay (Smooth) vs. Frequency, f_S = 192 kHz to 768 kHz, Signal Path = AINx to FastDSP to Headphone Output Mode or Line Output Mode, ADC0 and ADC1 Differential Mode

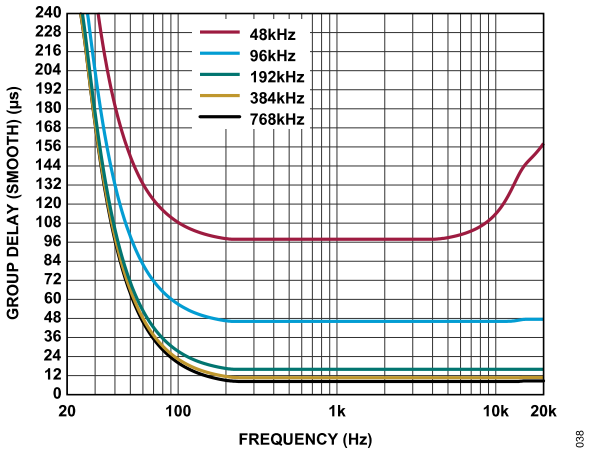

Figure 38. Group Delay (Smooth) vs. Frequency, f_S = 192 kHz to 768 kHz, Signal Path = AINx to FastDSP to Headphone Output Mode or Line Output Mode, ADC2 Single-Ended Mode

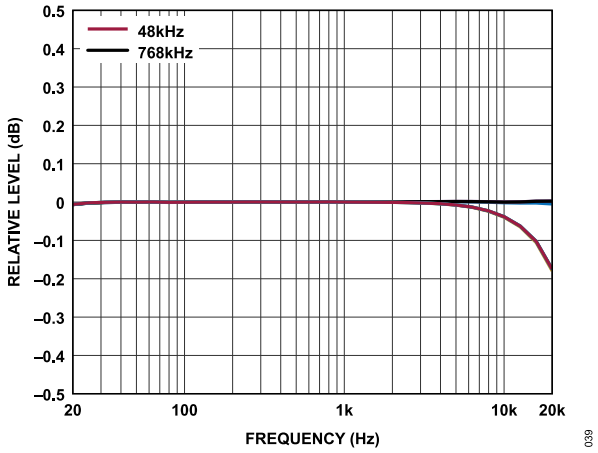

Figure 39. Relative Level vs. Frequency, Headphone Mode (16 Ω) or Line Output Mode (10 kΩ), f_S = 48 kHz and 768 kHz, Signal Path = AINx to DAC, ADC0 and ADC1 Differential Mode, ADC2 Single-Ended Mode

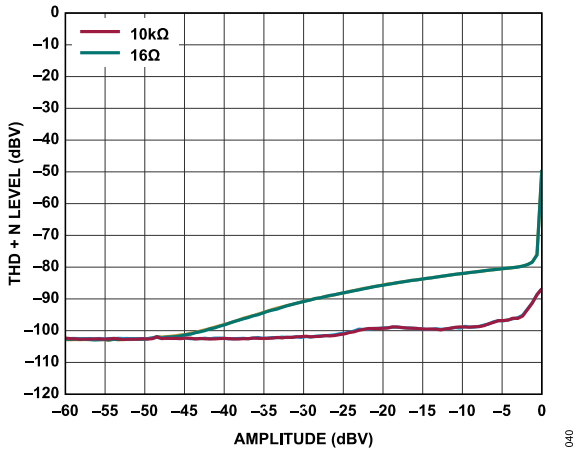

Figure 40. THD + N Level vs. Amplitude, f_S = 48 kHz to 768 kHz, Signal Path = AINx to Headphone Mode (16 Ω) or Line Output Mode (10 kΩ), ADC0 and ADC1 Differential Mode

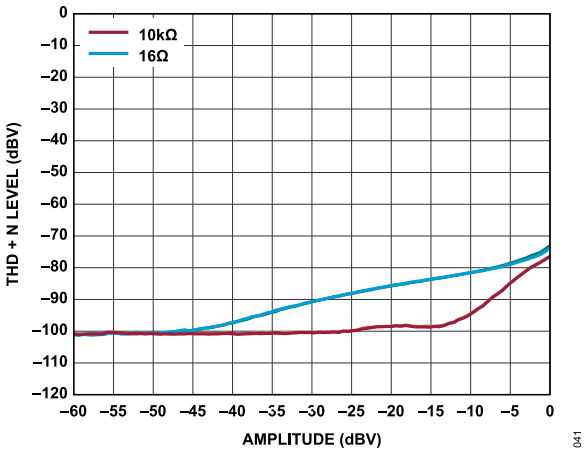

Figure 41. THD + N Level vs. Amplitude, f_S = 48 kHz to 768 kHz, Signal Path = AINx to Headphone Mode (16 Ω) or Line Output Mode (10 kΩ), ADC2 Single-Ended Mode

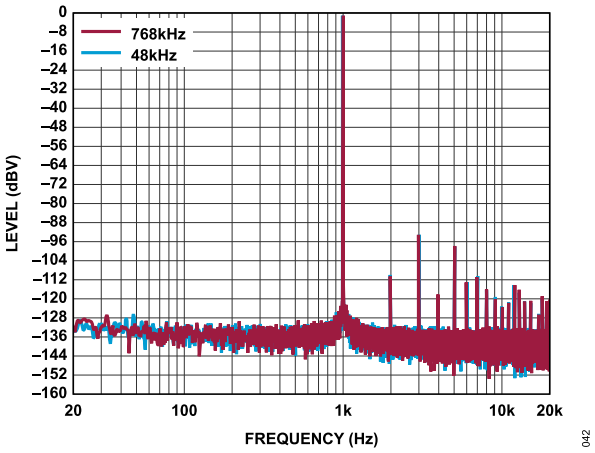

Figure 42. FFT, −1 dBV, Line Output Mode, Load = 10 kΩ, f_S = 48 kHz to 768 kHz, Signal Path = AINx to DAC, ADC0 and ADC1 Differential Mode

TYPICAL PERFORMANCE CHARACTERISTICS

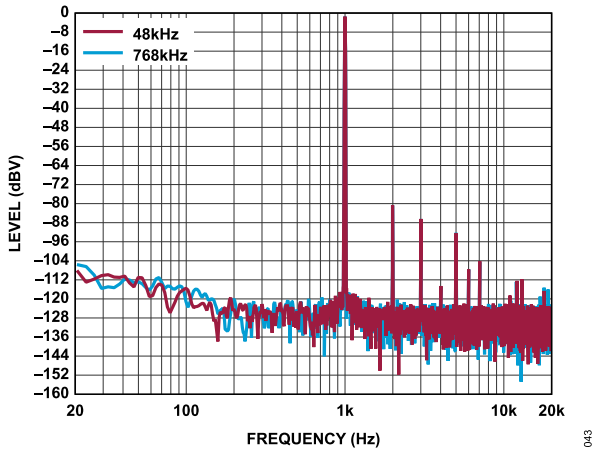

Figure 43. FFT, −1 dBV, Line Output Mode, Load = 10 kΩ, f_S = 48 kHz to 768 kHz, Signal Path = AINx to DAC, ADC2 Single-Ended Mode

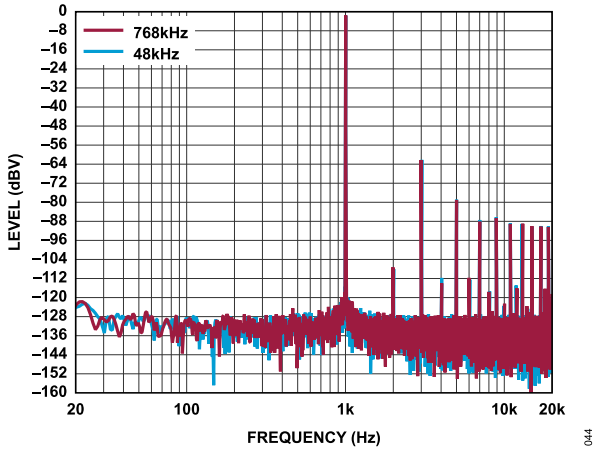

Figure 44. FFT, −1 dBV, Headphone Mode, Load = 16 Ω, f_S = 48 kHz to 768 kHz, Signal Path = AINx to DAC, ADC0 and ADC1 Differential Mode

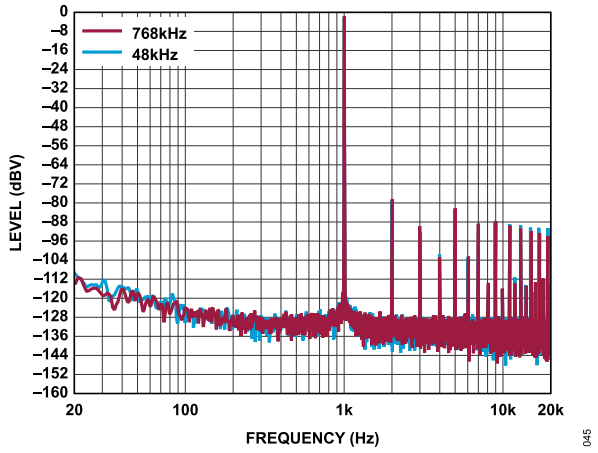

Figure 45. FFT, −1 dBV, Headphone Mode, Load = 16 Ω, f_S = 48 kHz to 768 kHz, Signal Path = AINx to DAC, ADC2 Single-Ended Mode

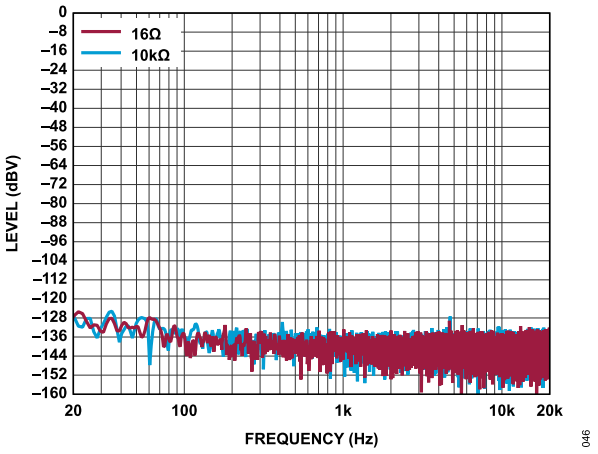

Figure 46. FFT, −1 dBV, f_S = 48 kHz to 768 kHz, Signal Path = AINx to DAC Headphone Mode (16 Ω) or Line Output Mode (10 kΩ), ADC0 and ADC1 Differential Mode

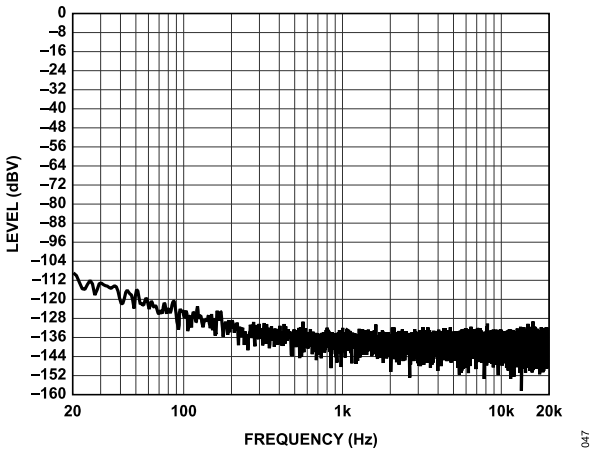

Figure 47. FFT, −1 dBV, f_S = 48 kHz to 768 kHz, Signal Path = AINx to DAC Headphone Mode (16 Ω) or Line Output Mode (10 kΩ), ADC2 Single-Ended Mode

THEORY OF OPERATION

The ADAU1850 is a low power audio codec with an optimized audio processing core, making it ideal for noise canceling applications that require high quality audio, low power, small size, and low latency. The serial audio port is compatible with I^2S, left justified, right justified, and time division multiplexing (TDM) modes, with tristating for interfacing to digital audio data. The operating voltage of AVDD and HPVDD is 1.8 V, and an internal regulator is used to generate the digital supply voltage.

The input signal path includes flexible configurations that can accept differential or single-ended analog microphone inputs. AIN2 supports single-ended analog microphone inputs only. Each input signal has its own programmable gain amplifier (PGA) for volume adjustment.

The ADCs and DAC are high quality, 24-bit sigma-delta (Σ-Δ) converters that operate at a selectable 12 kHz to 768 kHz sampling rate and the ADCs also support 8 kHz or 16 kHz sampling rate in voice wake-up mode. The ADCs and DAC have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz and fine step digital soft volume controls.

The DAC output is capable of differentially driving a headphone earpiece speaker with 16 Ω impedance or higher. There is also the option to change to line output mode when the output is loaded differentially with ≥10 kΩ.

The FastDSP core has a reduced instruction set that optimizes this codec for noise cancellation. The program and parameter RAMs can be loaded with custom audio processing signal flow built using the Lark Studio graphical user interface (GUI). The values stored in the parameter random access memory (RAM) control individual signal processing blocks.

Use the Lark Studio GUI to program and control the core through the control port. Along with designing and tuning a signal flow, the GUI can configure all the ADAU1850 registers. The GUI allows anyone with digital or analog audio processing knowledge to design the digital signal processor (DSP) signal flow and export the flow to a target application. The interface also provides enough flexibility and programmability for an experienced DSP programmer to have control of the design. In the Lark Studio GUI, the user can connect graphical blocks (such as biquads filters, volume controls, and arithmetic operations), compile the design, and load the program and parameter files into the ADAU1850 memory through the control port.

The ADAU1850 can generate the internal clocks from a wide range of input clocks by using the on-chip bypassable fractional PLL. The PLL accepts inputs from 30 kHz to 27 MHz.

The ADAU1850 is provided in a small, 28-ball, 2.957 mm × 1.757 mm WLCSP.

APPLICATIONS INFORMATION

POWER SUPPLY BYPASS CAPACITORS

Bypass each analog and digital power supply pin to its nearest appropriate ground pin with a single 0.1 µF capacitor. In Figure 48, VDD refers to all power supplies (IOVDD, AVDD, HPVDD, and HPVDD_L). Keep the connections to each side of the capacitor as short as possible, and route the trace on a single layer with no vias. For maximum effectiveness, place the capacitor equidistant from the power to the ground pins or slightly closer to the power pins if equidistant placement is not possible. Make thermal connections to the ground planes on the far side of the capacitor.

Bypass each supply signal on the board with a single bulk capacitor (10 µF to 47 µF).

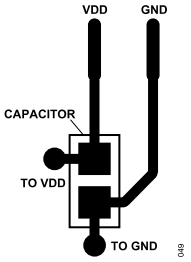

Figure 48. Recommended Power Supply Bypass Capacitor Layout

LAYOUT

The HPVDD and HPVDD_L supplies are for the headphone amplifiers. If the headphone amplifiers are enabled, the PCB trace to this pin must be wider than traces to other pins to increase the current carrying capacity. Use a wider trace for the headphone output lines.

GROUNDING

Use a single ground plane in the application layout. Place components in an analog signal path away from digital signals.

OUTLINE DIMENSIONS

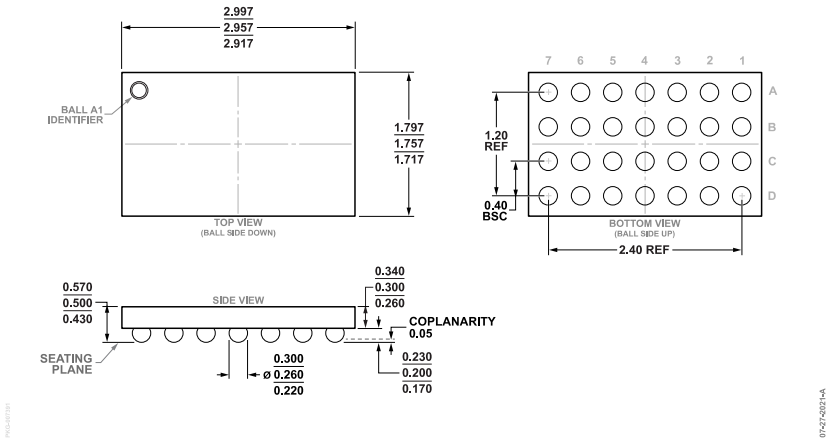

Figure 49. 28-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-28-5)
Dimensions shown in millimeters

Updated: July 27, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADAU1850BCBZRL	−40°C to +85°C	28-Ball WLCSP (2.957 mm × 1.757 mm × 0.50 mm)	Reel, 5000	CB-28-5

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADAU1850EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).