DRV8955 Quad Half-Bridge Driver With Integrated Current Sense

1 Features

- Quad Half-bridge DC motor driver
  - Can drive up to four Solenoid Loads, Two DC Motors, One Stepper Motor, or Other Loads
  - Full Individual Half Bridge Control
- Integrated current sensing and regulation
- 4.5 V to 48 V Operating supply voltage range
- Pin to pin compatible with -
  - DRV8932: 33 V, 900 mΩ HS + LS
  - DRV8935: 33 V, 330 mΩ HS + LS
- Industry Standard IN/IN Digital Control Interface
- Half-bridges can be connected in parallel to increase output current
- Configurable Off-Time PWM Chopping
  - 7, 16, 24 or 32 µs
- Supports 1.8 V, 3.3 V, 5.0 V logic inputs
- Low-current sleep mode (2 µA)
- Spread spectrum clocking for low EMI
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Refrigerator Damper and Ice Maker
- Textile Machines
- Factory Automation and Robotics
- Office and home automation
- Washers, Dryers and Dishwashers
- Gaming Machines
- General Purpose Solenoid Loads

3 Description

The DRV8955 provides four individually controllable half-bridge drivers for industrial applications. The device can be used for driving up to four solenoid loads, two DC motors, one stepper motor, or other loads.

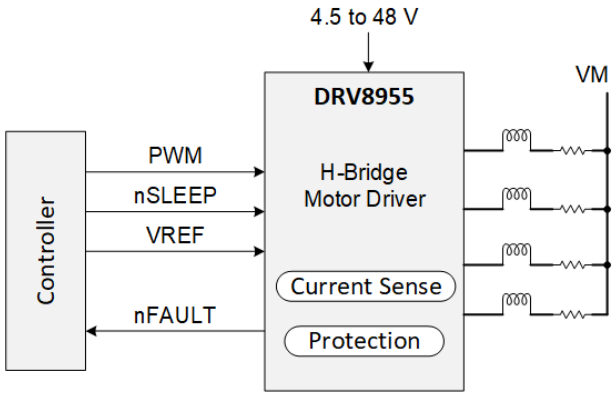
The output driver for each channel consists of N-channel power MOSFET's configured in a half-bridge. A simple PWM (IN/IN) interface allows easy interface with the controller. Separate inputs to independently control each half-bridge are provided. Additionally, the outputs can be paralleled together to provide more current for output loads.

The DRV8955 operates off a single power supply and supports a wide input supply range from 4.5 V to 48 V. A low-power sleep mode is provided to achieve a low quiescent current draw by shutting down much of the internal circuitry. Internal protection functions are provided for undervoltage-lockout, overcurrent protection on each FET, short circuit protection, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
DRV8955PPWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8955PRGER	VQFN (24)	4.0mm x 4.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV8955 Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release.

5 Pin Configuration and Functions

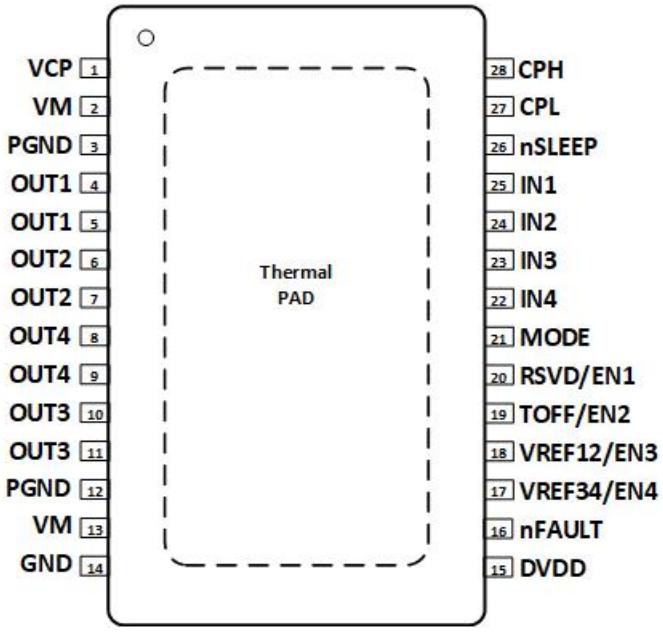


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8955

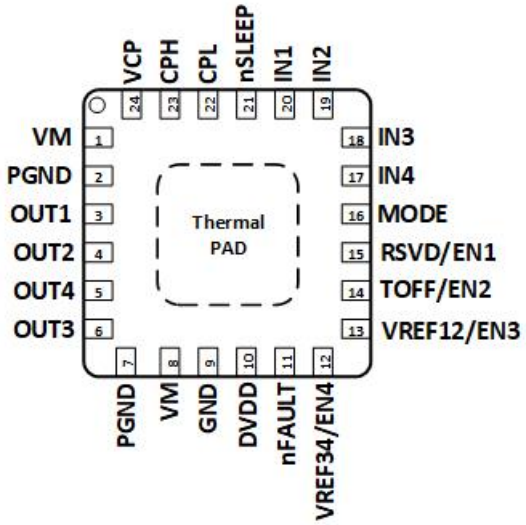


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8955

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	PWP	RGE		
IN1	25	20	I	PWM input. Logic controls the state of Half-bridge 1; internal pulldown.
IN2	24	19	I	PWM input. Logic controls the state of Half-bridge 2; internal pulldown.
IN3	23	18	I	PWM input. Logic controls the state of Half-bridge 3; internal pulldown.
IN4	22	17	I	PWM input. Logic controls the state of Half-bridge 4; internal pulldown.
OUT1	4, 5	3	O	Output of Half-bridge 1.
OUT2	6, 7	4	O	Output of Half-bridge 2.

PIN			TYPE	DESCRIPTION
NAME	PWP	RGE		
OUT3	10, 11	6	O	Output of Half-bridge 3.
OUT4	8, 9	5	O	Output of Half-bridge 4.
VREF12/EN3	18	13	I	When MODE pin is 0, 1 or Hi-Z, this pin acts as the reference voltage input pin and controls the current level for Half-bridges 1 and 2. When a 330k resistor is connected from MODE pin to ground, a logic high on this pin enables OUT3.
VREF34/EN4	17	12	I	When MODE pin is 0, 1 or Hi-Z, this pin acts as the reference voltage input pin and controls the current level for Half-bridges 3 and 4. When a 330k resistor is connected from MODE pin to ground, a logic high on this pin enables OUT4.
RSVD/EN1	20	15	-	When MODE pin is 0, 1 or Hi-Z, leave this pin unconnected. When a 330k resistor is connected from MODE pin to ground, a logic high on this pin enables OUT1.
MODE	21	16	I	Volatge on the MODE pin selects the paralleling of individual half-bridges, or selects independent high-z operation for the bridges. When MODE is 0, four independent solenoid loads can be driven. When MODE is 1, pairs of half-bridges are paralleled, so that two solnoid loads can be driven with higher output current. When MODE is open, all the half-bridges are paralleled, and a single solenoid load will be driven. When a 330k resistor is connected from MODE to ground, independent high-z operation is enabled - each half-bridge output can be enabled or disabled independently.
CPH	28	23	PWR	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	22		
GND	14	9	PWR	Device ground. Connect to system ground.
TOFF/EN2	19	14	I	When MODE pin is 0, 1 or Hi-Z, this pin sets the off-time during current chopping. When a 330k resistor is connected from MODE to ground, a logic high on this pin enables OUT2.
DVDD	15	10	PWR	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCP	1	24	O	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	2, 13	1, 8	PWR	Power supply. Connect to supply voltage and bypass to PGND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
PGND	3, 12	2, 7	PWR	Power ground. Connect to system ground.
nFAULT	16	11	O	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	26	21	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
PAD	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control and reference pin voltage (IN1, IN2, IN3, IN4, nFAULT, RSVD/EN1, TOFF/EN2, MODE, VREF12/EN3, VREF34/EN4)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Continuous phase node pin voltage (OUT1, OUT2, OUT3, OUT4)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (OUT1, OUT2, OUT3, OUT4)	–3	V_{VM} + 3	V
Peak drive current (OUT1, OUT2, OUT3, OUT4)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	48	V
V_I	Logic level input voltage	0	5.5	V
V_{REF}	Reference rms voltage range (VREF)	0.05	3.3	V
f_{PWM}	Applied PWM signal (IN1, IN2, IN3, IN4)	0	100	kHz
I_{FS}	Peak output current (MODE = 0 or 330k to GND)	0	2.5	A
	Peak output current (MODE = 1)	0	5	A
	Peak output current (MODE = Hi-Z)	0	10	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC		PWP (HTSSOP)	RGE (VQFN)	UNIT
		28 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	39.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.0	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	16.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.2	15.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	3.4	°C/W

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 48 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 48 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, EN1, EN2, EN3, EN4, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
t_1	ENx high to OUTx high delay	INx = 1			5	µs
t_2	ENx low to OUTx low delay	INx = 1			5	µs
t_3	ENx high to OUTx low delay	INx = 0			5	µs
t_4	ENx low to OUTx high delay	INx = 0			5	µs
t_5	INx high to OUTx high delay			800		ns
t_6	INx low to OUTx low delay			800		ns
QUAD-LEVEL INPUTS (MODE, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z (>500kΩ to GND)	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						
$R_{DS(ONH)}$	High-side FET on resistance (MODE = 0 or 330k to GND)	T_J = 25 °C, I_O = -1 A		165	200	mΩ
		T_J = 125 °C, I_O = -1 A		250	300	mΩ
		T_J = 150 °C, I_O = -1 A		280	350	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance (MODE = 0 or 330k to GND)	T_J = 25 °C, I_O = 1 A		165	200	mΩ
		T_J = 125 °C, I_O = 1 A		250	300	mΩ
		T_J = 150 °C, I_O = 1 A		280	350	mΩ

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ONH)}$	High-side FET on resistance (MODE = 1)	T_J = 25 °C, I_O = -1 A		80	100	mΩ
		T_J = 125 °C, I_O = -1 A		125	150	mΩ
		T_J = 150 °C, I_O = -1 A		140	175	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance (MODE = 1)	T_J = 25 °C, I_O = 1 A		80	100	mΩ
		T_J = 125 °C, I_O = 1 A		125	150	mΩ
		T_J = 150 °C, I_O = 1 A		140	175	mΩ
$R_{DS(ONH)}$	High-side FET on resistance (MODE = Hi-Z)	T_J = 25 °C, I_O = -1 A		40	50	mΩ
		T_J = 125 °C, I_O = -1 A		60	75	mΩ
		T_J = 150 °C, I_O = -1 A		70	90	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance (MODE = Hi-Z)	T_J = 25 °C, I_O = 1 A		40	50	mΩ
		T_J = 125 °C, I_O = 1 A		60	75	mΩ
		T_J = 150 °C, I_O = 1 A		70	90	mΩ
t_{RF}	Output rise/fall time	VM = 24V		100		ns
CURRENT REGULATION (VREF)						
K_V	Transimpedance gain	**VREF = 3.3V, MODE = 0 or 330k to GND**	1.254	1.32	1.386	V/A
		VREF = 3.3V, MODE = 1	0.627	0.66	0.693	V/A
		VREF = 3.3V, MODE = Hi-Z	0.313	0.33	0.347	V/A
I_{VREF}	VREF leakage current	**VREF = 3.3V**			8.25	µA
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	Current trip accuracy	10% to 20% of ITRIP setting	-12		12	%
		20% to 40% of ITRIP setting	-6		6	
		40% to 100% ITRIP setting	-4		4	
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET (MODE = 0 or 330k to GND)	4			A
		Current through any FET (MODE = 1)	8			A
		Current through any FET (MODE = Hi-Z)	16			A
t_{OCP}	Overcurrent deglitch time			2		µs
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.5.1 Typical Characteristics

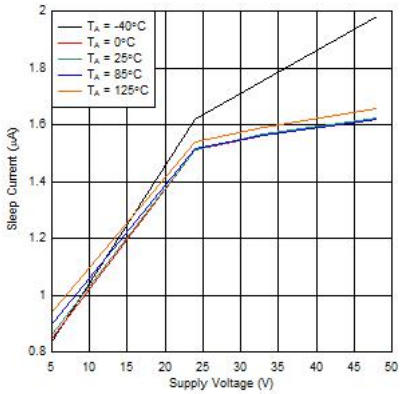


Figure 6-1. Sleep Current over Supply Voltage

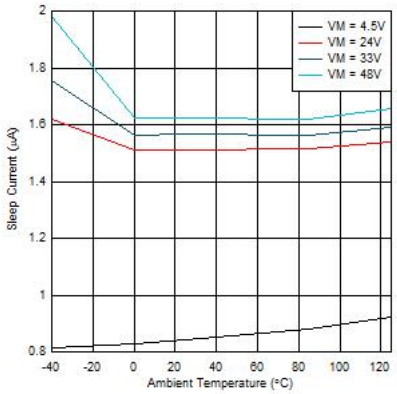


Figure 6-2. Sleep Current over Temperature

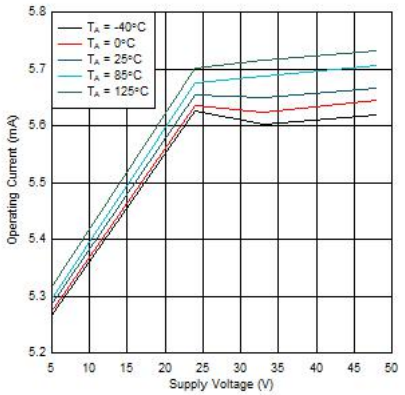


Figure 6-3. Operating Current over Supply Voltage

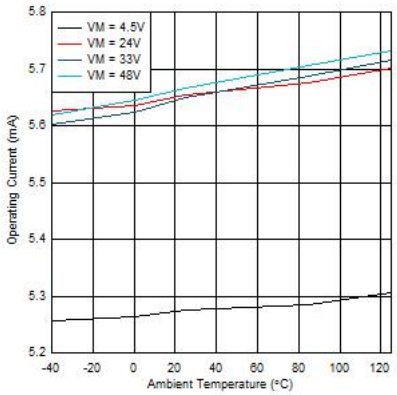


Figure 6-4. Operating Current over Temperature

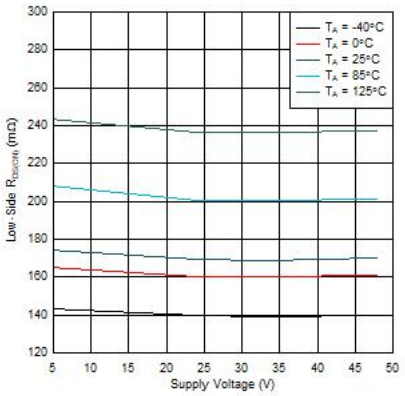


Figure 6-5. Low-Side $R_{DS(ON)}$ over Supply Voltage (MODE = 0 or 330k to GND)

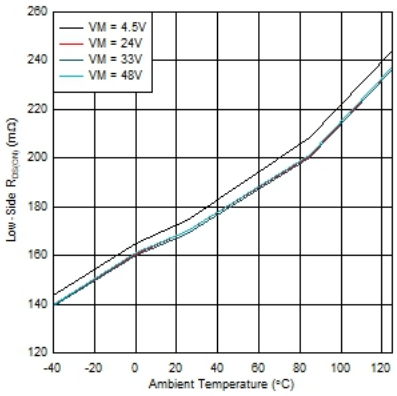


Figure 6-6. Low-Side $R_{DS(ON)}$ over Temperature (MODE = 0 or 330k to GND)

6.5.1 Typical Characteristics (continued)

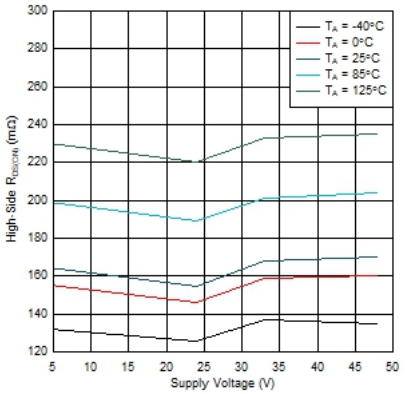


Figure 6-7. High-Side $R_{DS(ON)}$ over Supply Voltage (MODE = 0 or 330k to GND)

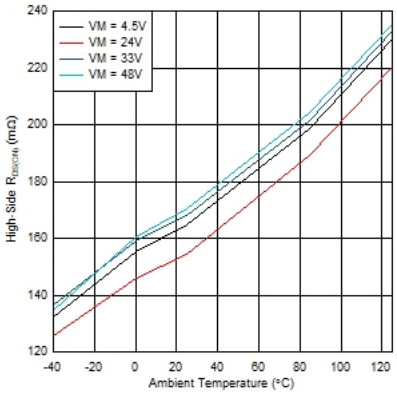


Figure 6-8. High-Side $R_{DS(ON)}$ over Temperature (MODE = 0 or 330k to GND)

7 Detailed Description

7.1 Overview

The DRV8955 supports a wide 4.5 V to 48 V supply voltage and can drive up to four solenoid loads.

A simple PWM interface option allows easy interfacing to the outputs. A MODE pin allows configuring the half-bridges to drive one, two or four solenoid loads, or allows independent high-z control for each half-bridge. When the half-bridges are paralleled to drive one or two loads, the device can support higher output currents. The trip point for current regulation is controlled by the value of the VREF pin voltage. The PWM off-time, t_{OFF}, can be adjusted to 7, 16, 24, or 32 µs. A low-power sleep mode is included which lets the system save power when not driving the load.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin.

7.2 Functional Block Diagrams

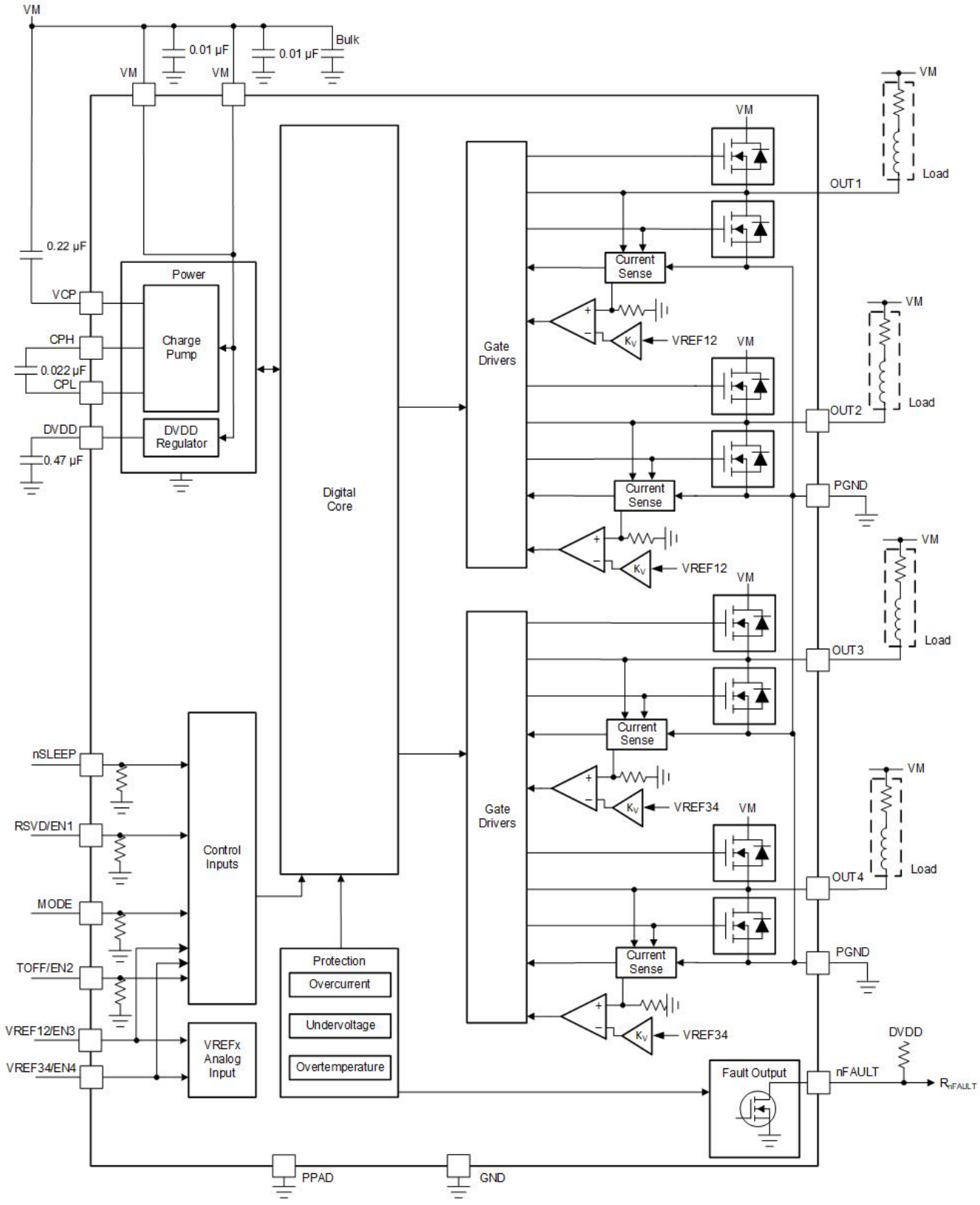


Figure 7-1. DRV8955 Block Diagram

7.3 Feature Description

The following table shows the recommended values of the external components for the driver.

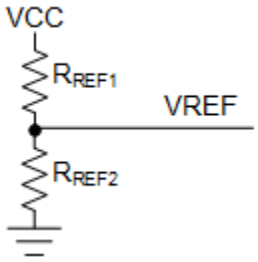


Figure 7-2. Resistor divider connected to the VREF pins

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	VCC	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF12	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF12	GND	
R_{REF3}	VREF34	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF3} and R_{REF4} should be less than 50-kΩ.
R_{REF4} (Optional)	VREF34	GND	

VCC is not a pin on the device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.

7.3.1 Configuration Options and Bridge Control

The MODE pin configures the half-bridges such that one, two or four solenoid loads can be driven by the device. Higher load currents can be supported by paralleling half-bridges. Table 7-2 shows the four possible settings -

Table 7-2. DRV8955 Configuration Options

MODE	Number of Half-bridges	Independent High-z Control	RdsON (HS + LS)	Maximum ITRIP	Input Control Pins	Current Control
0	Four	No	330 mΩ	2.5 A	IN1, IN2, IN3, IN4	VREF12 controls the ITRIP for OUT1 and OUT2, VREF34 controls the ITRIP for OUT3 and OUT4.
1	Two (Connect OUT1 and OUT2 together, and OUT3 and OUT4 together)	No	160 mΩ	5 A	IN2 controls OUT1 and OUT2, IN4 controls OUT3 and OUT4	VREF12 controls the ITRIP for OUT1 and OUT2, VREF34 controls the ITRIP for OUT3 and OUT4.
Hi-z	One (connect all four OUT pins together)	No	80 mΩ	10 A	IN4 controls the combined output	VREF12 must be shorted to VREF34 to control the ITRIP for output load.
330kΩ to GND	Four (independent High-z)	Yes	330 mΩ	No ITRIP control available.	IN1, IN2, IN3, IN4, EN1, EN2, EN3, EN4	The current for each output has to be controlled by the input PWM pulse width. The VREF and TOFF pins are reassigned as enable (ENx) pins in this mode.

The INx input pins directly control the state (high or low) of the OUTx outputs. When MODE pin is connected to a 330k resistor to GND, the ENx input pins enable or disable the OUTx drivers, as shown below.

Table 7-3. DRV8955 H-Bridge Logic (for MODE = 0, 1 or Hi-Z)

nSLEEP	INx	OUTx	DESCRIPTION
0	X	Hi-Z	Sleep mode; Half-bridge disabled (Hi-Z)
1	0	L	OUTx Low-side ON
1	1	H	OUTx High-side ON

Table 7-4. DRV8955 H-Bridge Logic (for MODE = 330k to GND)

nSLEEP	INx	ENx	OUTx	DESCRIPTION
0	X	X	Hi-Z	Sleep mode; Half-bridge disabled (Hi-Z)
1	X	0	Hi-Z	Individual outputs disabled (Hi-Z)
1	0	1	L	OUTx Low-side ON
1	1	1	H	OUTx High-side ON

When MODE pin is connected to a 330k resistor to GND, the inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. The following table is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 7-5. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
PWM	1	0	1	Forward PWM, slow decay
0	1	PWM	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

7.3.2 Current Regulation

When an output load is connected to the VM supply, and MODE pin is 0, 1 or Hi-Z; the load current can be regulated to the ITRIP level. Table 7-2 describes how the VREF pins control the output current in various modes of operation.

With MODE = 0, the ITRIP current (I_{TRIP}) can be calculated as I_{TRIP} (A) = V_{REF} (V) / 1.32 (V/A).

For MODE = 1, I_{TRIP} (A) = V_{REF} (V) / 0.66 (V/A).

For MODE = Hi-Z, I_{TRIP} (A) = V_{REF} (V) / 0.33 (V/A).

The V_{REF} voltage can be programmed by connecting resistor dividers from DVDD pin to ground. Both V_{REF} pins can be tied together to program the same ITRIP current for all output channels.

With INx = 0, the low side FET is turned ON till the current increases and hits the ITRIP level. Once the load current equals ITRIP, the low-side FET is turned OFF and the high-side FET is turned on for a period of off-time determined by the TOFF pin. After the off-time expires, the low-side FET is again turned ON and the cycle repeats.

For resistive loads connected to VM, if the ITRIP is higher than the (VM / R_{LOAD}), the load current is regulated at VM / R_{LOAD} level while INx = 0. For inductive loads connected to VM, it should be ensured that the current decays enough every cycle to prevent runaway and triggering overcurrent protection. The different scenarios are shown below -

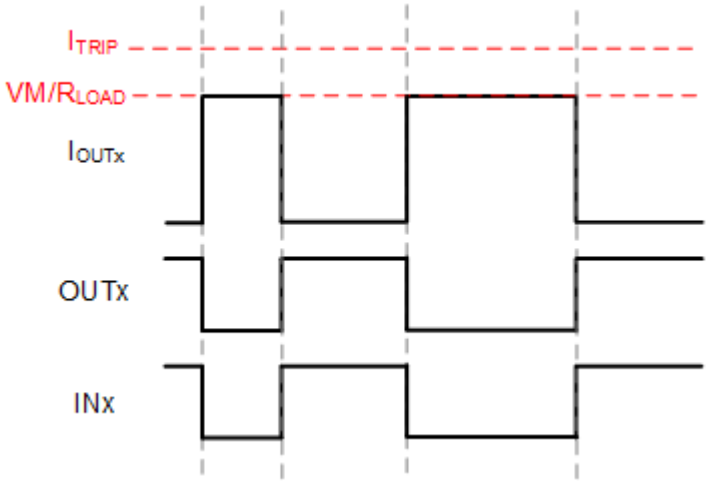


Figure 7-3. Resistive Load Connected to VM, Cycle-by-cycle control, I_{TRIP} is higher than VM/R_{LOAD}.

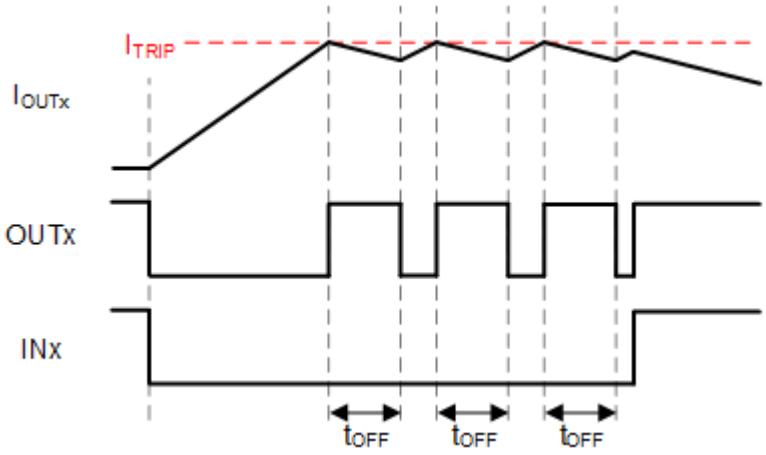


Figure 7-4. Inductive Load Connected to VM, fixed off-time current chopping

In this scenario, with INx = 0, the high-side MOSFET is turned on for t_{OFF} duration after IOUT exceeds ITRIP. After t_{OFF}, the low side MOSFET is again turned on till IOUT exceeds ITRIP again. The fixed off-time mode allows for a simple current chopping scheme without involvement from the external controller. Fixed off-time mode will support 100% duty cycle current regulation.

Another way of controlling the load current is the cycle-by-cycle control mode, where PWM pulse width of the INx input pins are controlled. This allows for additional control of the current chopping scheme by the external controller. For loads connected to VM, when INx = 0, the current through the load builds up; and when INx = 1, the current through the load decays. By properly choosing the duty cycle of the INx pulse, current can be regulated to a target value. Various such scenarios are shown below -

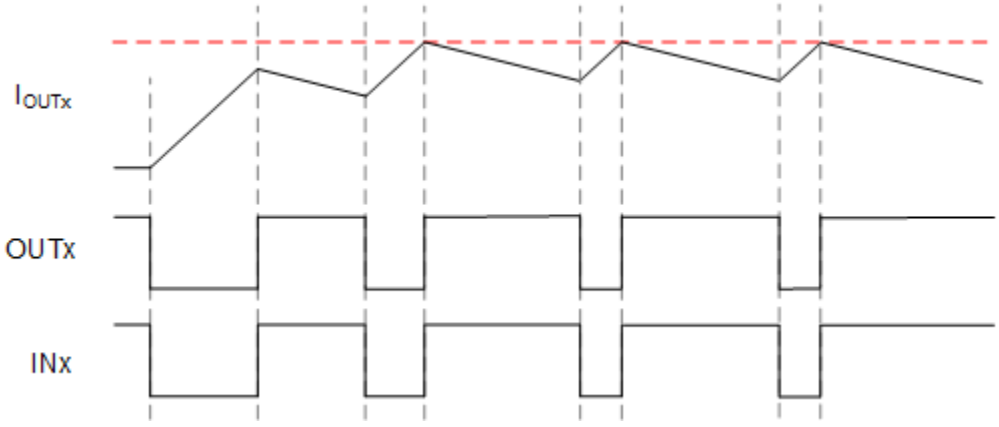


Figure 7-5. Inductive Load Connected to VM, Cycle-by-cycle control

This scenario requires INx pin duty cycle adjustment to ensure that the current does not run away.

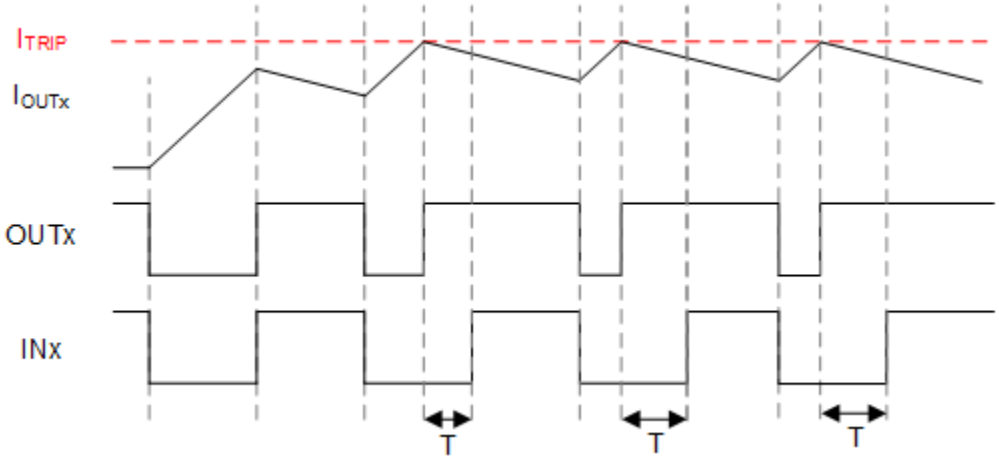


Figure 7-6. Inductive Load Connected to VM, Cycle-by-cycle control, T has to be less than T_{OFF} of the DRV8955.

Similarly, current through loads connected to ground can be controlled by controlling the INx pin pulse width - INx = 1 builds up the current, and INx = 0 decays the current. Two such scenarios are shown below -

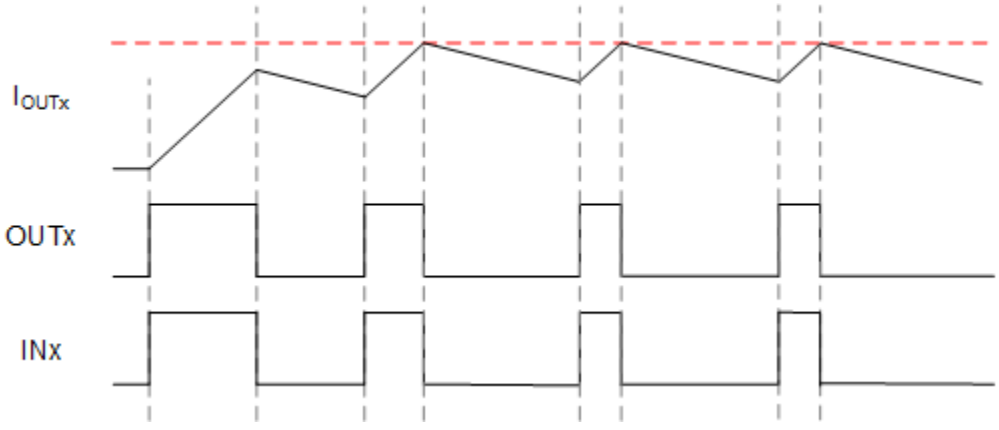


Figure 7-7. Inductive Load Connected to ground, Cycle-by-cycle control

This scenario requires INx pin duty cycle adjustment to ensure that the current does not run away.

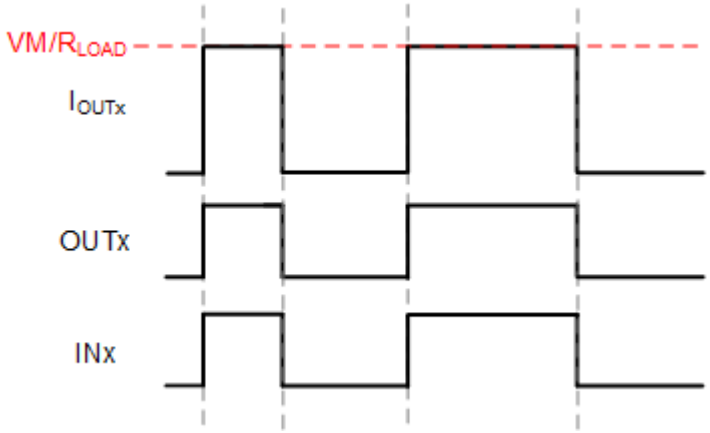


Figure 7-8. Resistive Load Connected to ground, Cycle-by-cycle control

Table 7-6. Off-Time Settings

TOFF	OFF-TIME t_{OFF}
0	7 µs
1	16 µs
Hi-Z	24 µs
330kΩ to GND	32 µs

7.3.3 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

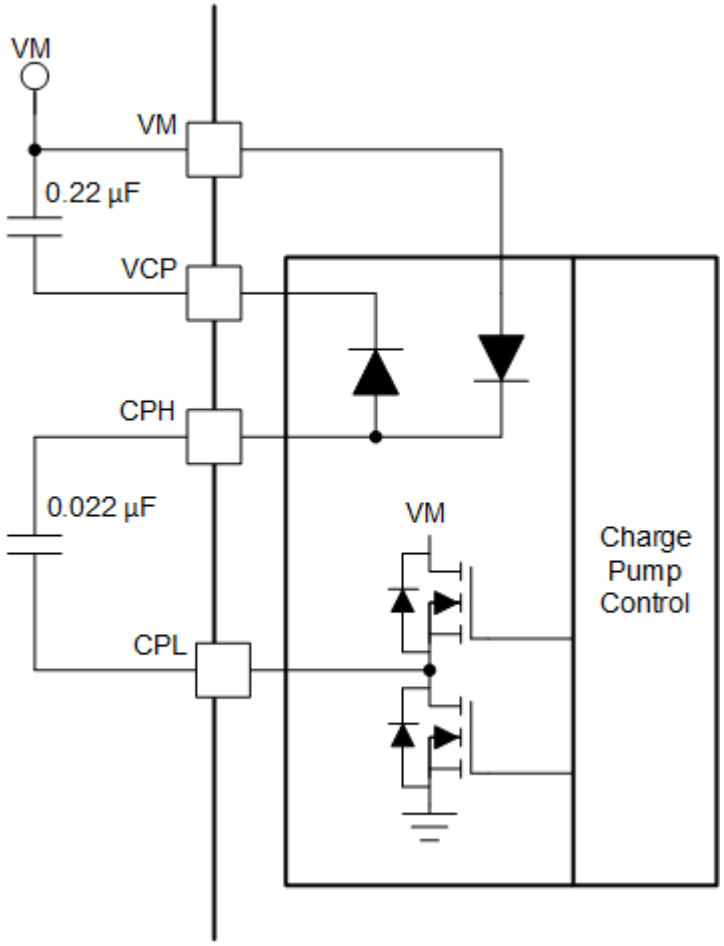


Figure 7-9. Charge Pump Block Diagram

7.3.4 Linear Voltage Regulators

A linear voltage regulator is integrated in the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

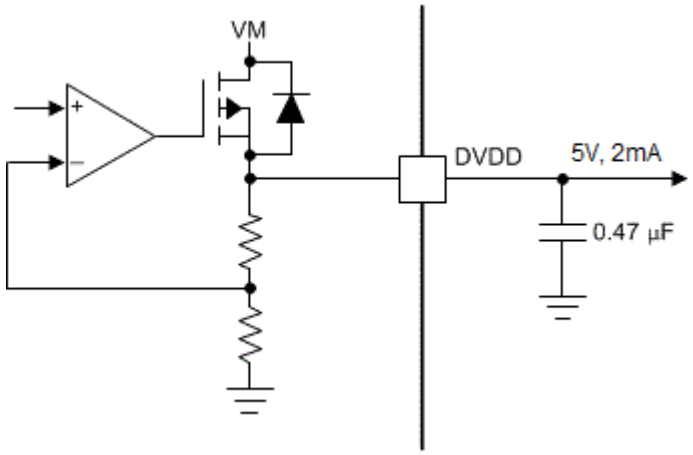


Figure 7-10. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, MODE or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.5 Logic and Quad-Level Pin Diagrams

Figure 7-11 gives the input structure for logic-level pins IN1, IN2, IN3, IN4 and nSLEEP:

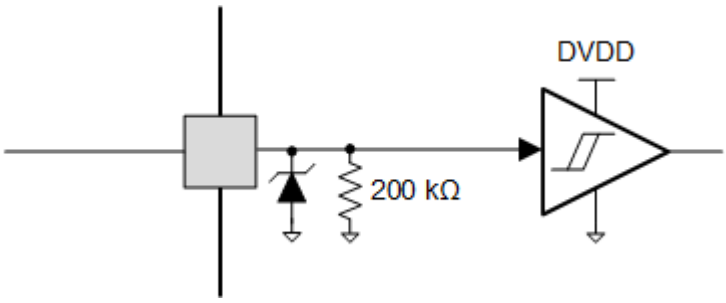


Figure 7-11. Logic-level Input Pin Diagram

Quad-level logic pins MODE and TOFF have the following structure as shown in Figure 7-12.

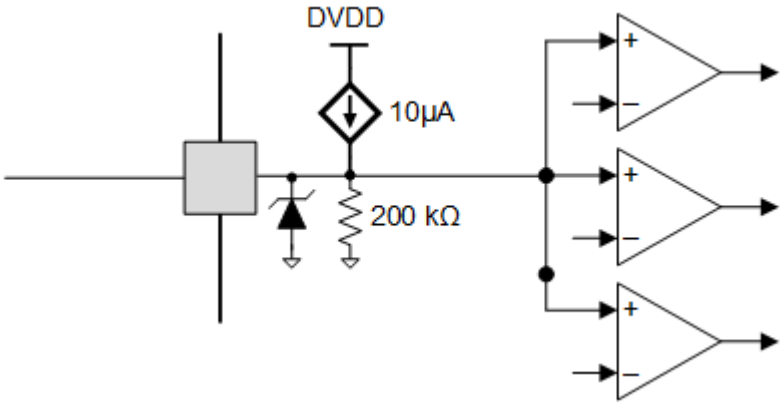


Figure 7-12. Quad-Level Input Pin Diagram

7.3.5.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

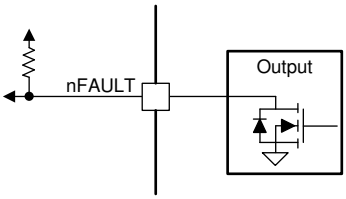


Figure 7-13. nFAULT Pin

7.3.6 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.6.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. Normal

operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.6.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.6.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the half-bridge in which OCP is detected is disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.6.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

Fault Condition Summary

Table 7-7. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	HALF-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	All Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
CP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	All Disabled	Operating	Operating	VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	nFAULT	Half-bridge with OCP is Disabled	Operating	Operating	Latched
Thermal Shutdown (OTSD)	T_J > T_{TSD}	nFAULT	All Disabled	Disabled	Operating	Latched

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The state of the device is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 nSLEEP Reset Pulse

A latched fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20 µs and shorter than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 7-14). This reset pulse does not affect the status of the charge pump or other functional blocks.

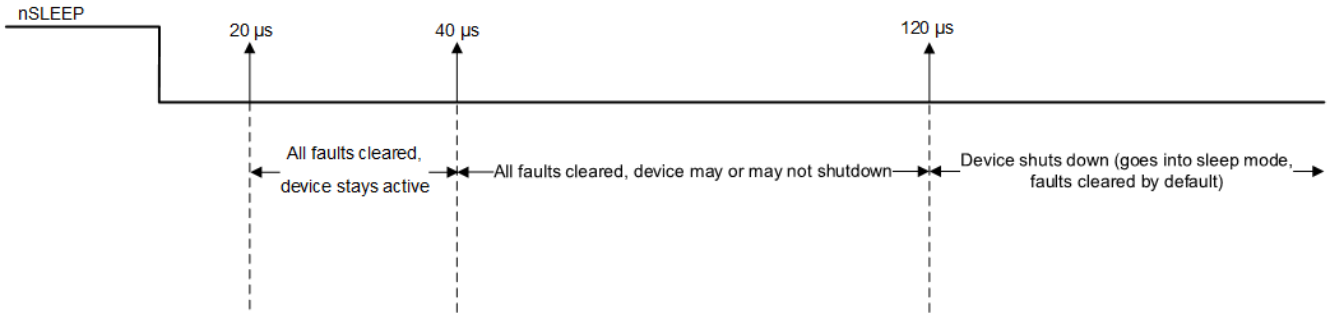


Figure 7-14. nSLEEP Reset Pulse

Functional Modes Summary

Table 7-8lists a summary of the functional modes.

Table 7-8. Functional Modes Summary

CONDITION		CONFIGURATION	HALF-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 48 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled
Operating	4.5 V < VM < 48 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8955 is a four channel half-bridge driver with protection features. The device can be used to drive one stepper motor, multiple brushed DC motors, or up to four solenoid loads.

8.2 Typical Application

The following design procedure can be used to configure the DRV8955. In this application, the device will be used to drive four solenoid loads.

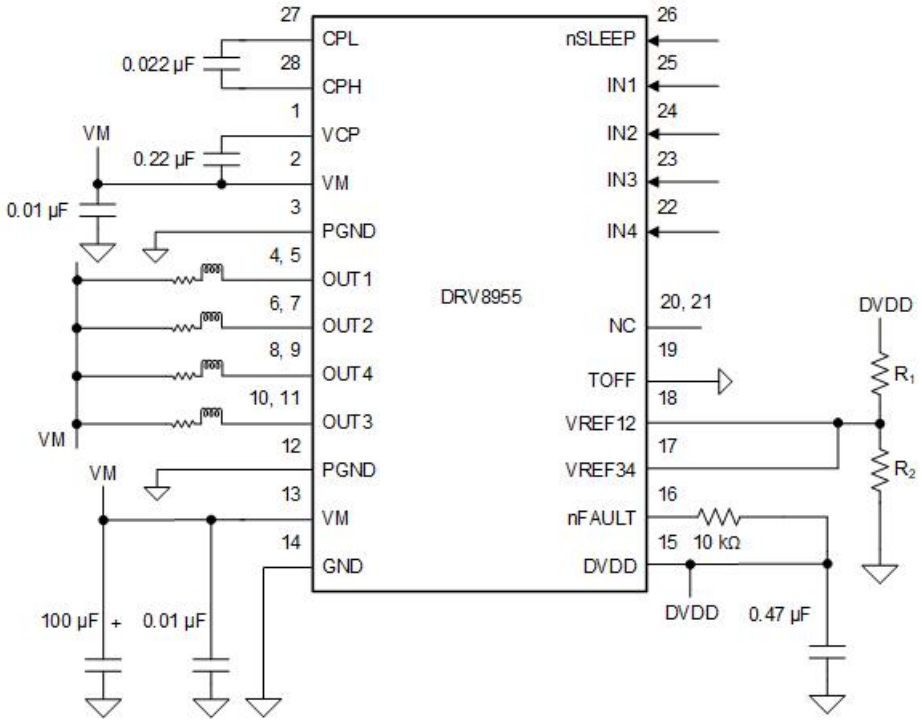


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for a typical application.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage Range	VM	19-29 V
Current per Channel	I_{OUT}	1.5 A
PWM Frequency	f_{PWM}	40 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

When an output load is connected to the VM supply, the load current can be regulated to the ITRIP level. The ITRIP current level for OUT1 and OUT2 outputs is controlled by the VREF12 pin, and the ITRIP level for OUT3 and OUT4 outputs is controlled by the VREF34 pin. The ITRIP current (ITRIP) can be calculated as ITRIP (A) = VREF (V) / 1.32 (V/A). The VREF voltage can be programmed by connecting resistor dividers from DVDD pin to ground.

8.2.2.2 Power Dissipation and Thermal Calculation

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$P_{TOT} = P_{COND} + P_{SW} + P_Q$

For loads connected to VM, assuming that all the outputs are loaded with same current, total conduction loss can be expressed as -

$P_{COND} = 4 \times (I_{OUT})^2 \times R_{DS(ONL)}$

As the high-side and low-side MOSFETs of the DRV8955 have the same on-resistance, the conduction loss will be independent of the duty cycle of the input PWM or the amount of PWM off-time. It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(ON)}$ with temperature can be found in the Typical Characteristics curves.

$P_{COND} = 4 \times (1.5\ A)^2 \times 0.165\ \Omega = 1.485\ W$

P_{SW} can be calculated from the nominal supply voltage (VM), regulated output current (I_{OUT}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

Assuming that all the four outputs are switching simultaneously -

$P_{SW} = 4 \times (P_{SW\_RISE} + P_{SW\_FALL})$

$P_{SW\_RISE} = 0.5 \times VM \times I_{OUT} \times t_{RISE} \times f_{PWM}$

$P_{SW\_FALL} = 0.5 \times VM \times I_{OUT} \times t_{FALL} \times f_{PWM}$

$P_{SW\_RISE} = 0.5 \times 24\ V \times 1.5\ A \times 100\ ns \times 40\ kHz = 0.072\ W$

$P_{SW\_FALL} = 0.5 \times 24\ V \times 1.5\ A \times 100\ ns \times 40\ kHz = 0.072\ W$

$P_{SW} = 4 \times (0.072W + 0.072W) = 0.576\ W$

P_Q can be calculated from the nominal supply voltage (VM) and the I_{VM} current specification.

$P_Q = VM \times I_{VM} = 24\ V \times 5\ mA = 0.12\ W$

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss.

$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.485\text{-}W + 0.576\text{-}W + 0.12\text{-}W = 2.181\text{-}W$

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 29.7 °C/W for the HTSSOP package and 39 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as -

T_J = 25°C + (2.181-W x 29.7°C/W) = 89.78 °C

The junction temperature for the VQFN package is calculated as -

T_J = 25°C + (2.181-W x 39°C/W) = 110.06 °C

It should be ensured that the device junction temperature is within the specified operating region.

8.2.2.3 Application Curves

CH1 = IN1 (3 V/div), CH3 = OUT1 (24 V/div), CH7 = IOUT1 (1.5 A/div)

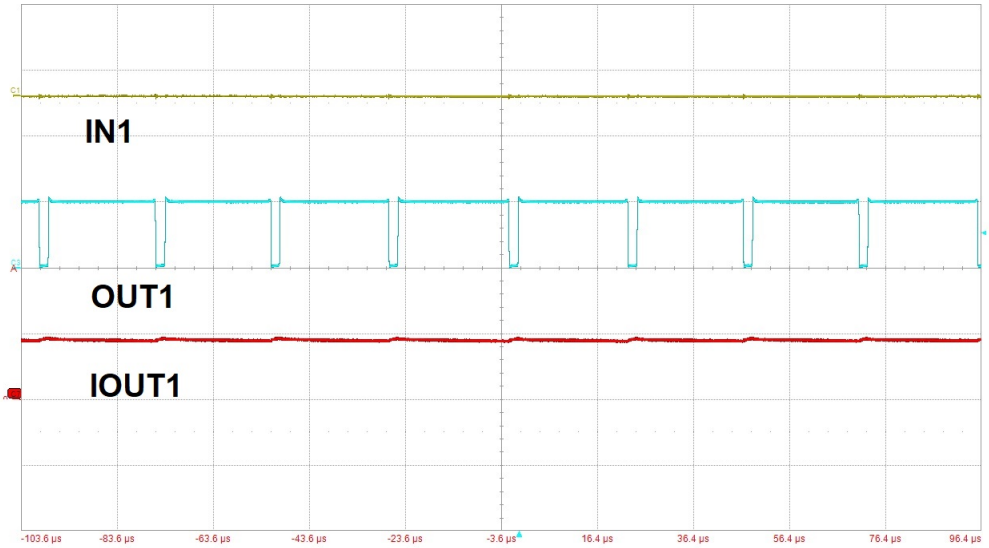


Figure 8-2. Current Regulation with VM-connected Load

CH1 = IN1 (3 V/div), CH3 = OUT1 (24 V/div)

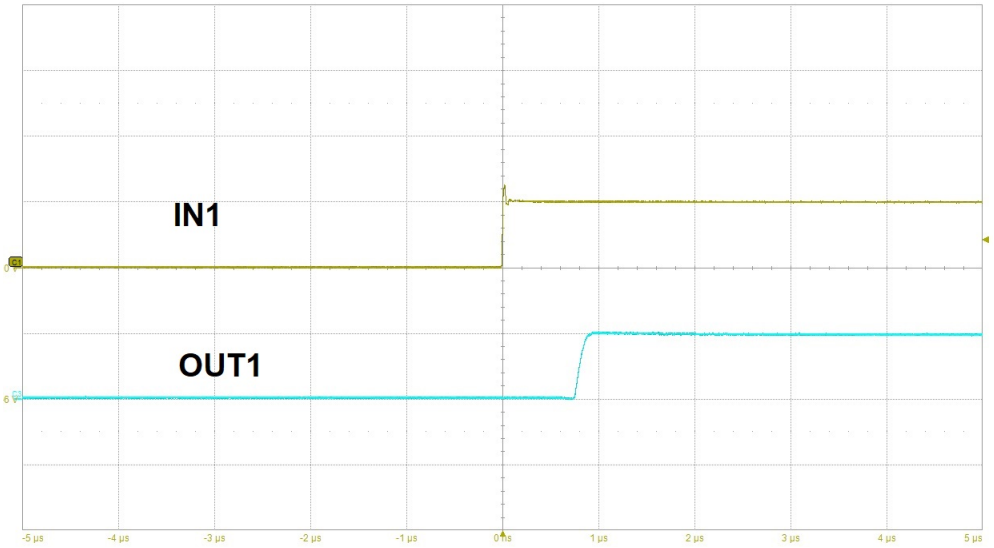


Figure 8-3. Input-to-Output Propagation Delay

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

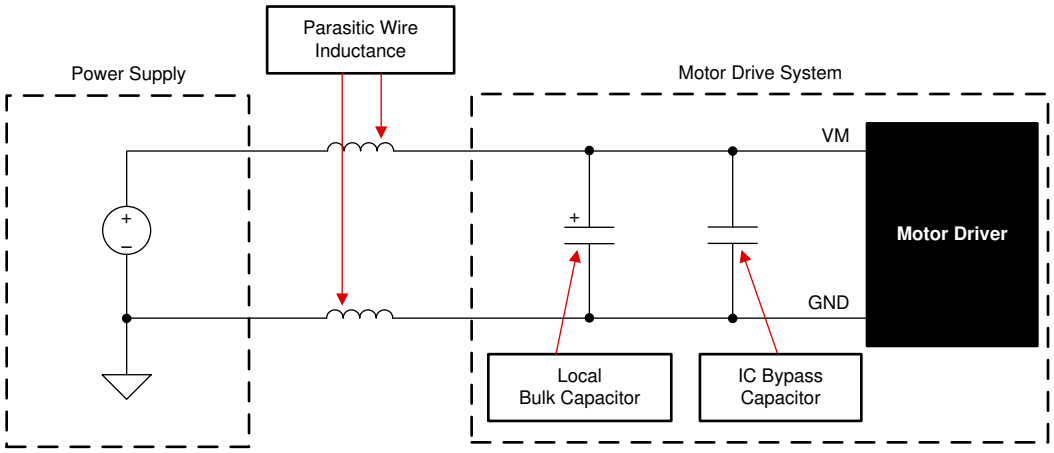


Figure 9-1. Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

10.2 Layout Example

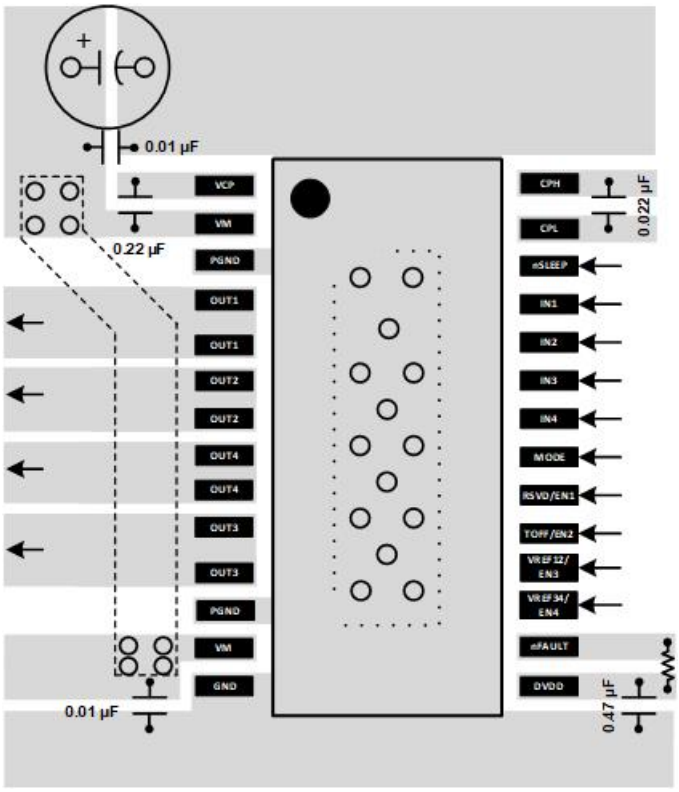


Figure 10-1. HTSSOP Layout Example

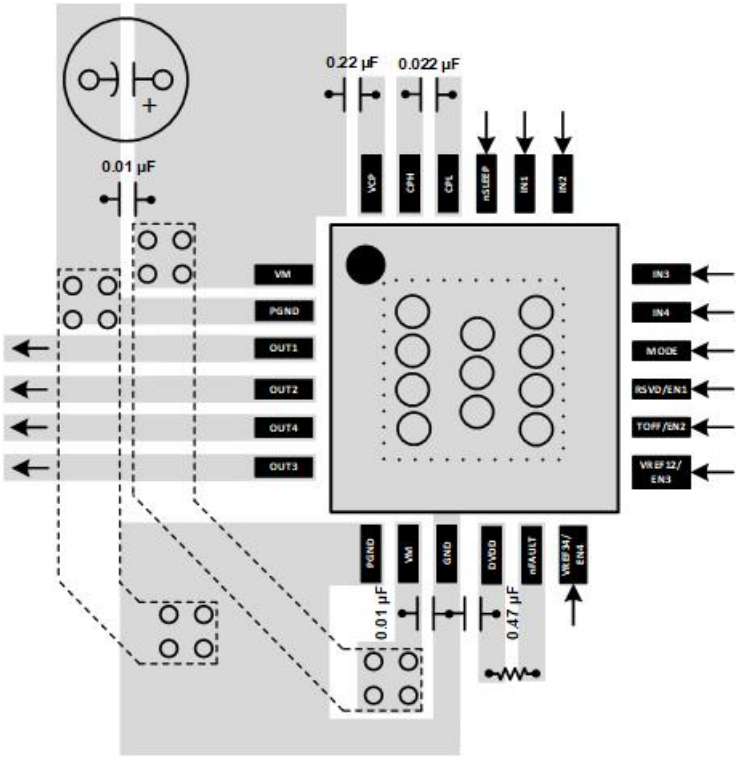


Figure 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *High Resolution Microstepping Driver With the DRV88xx Series* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

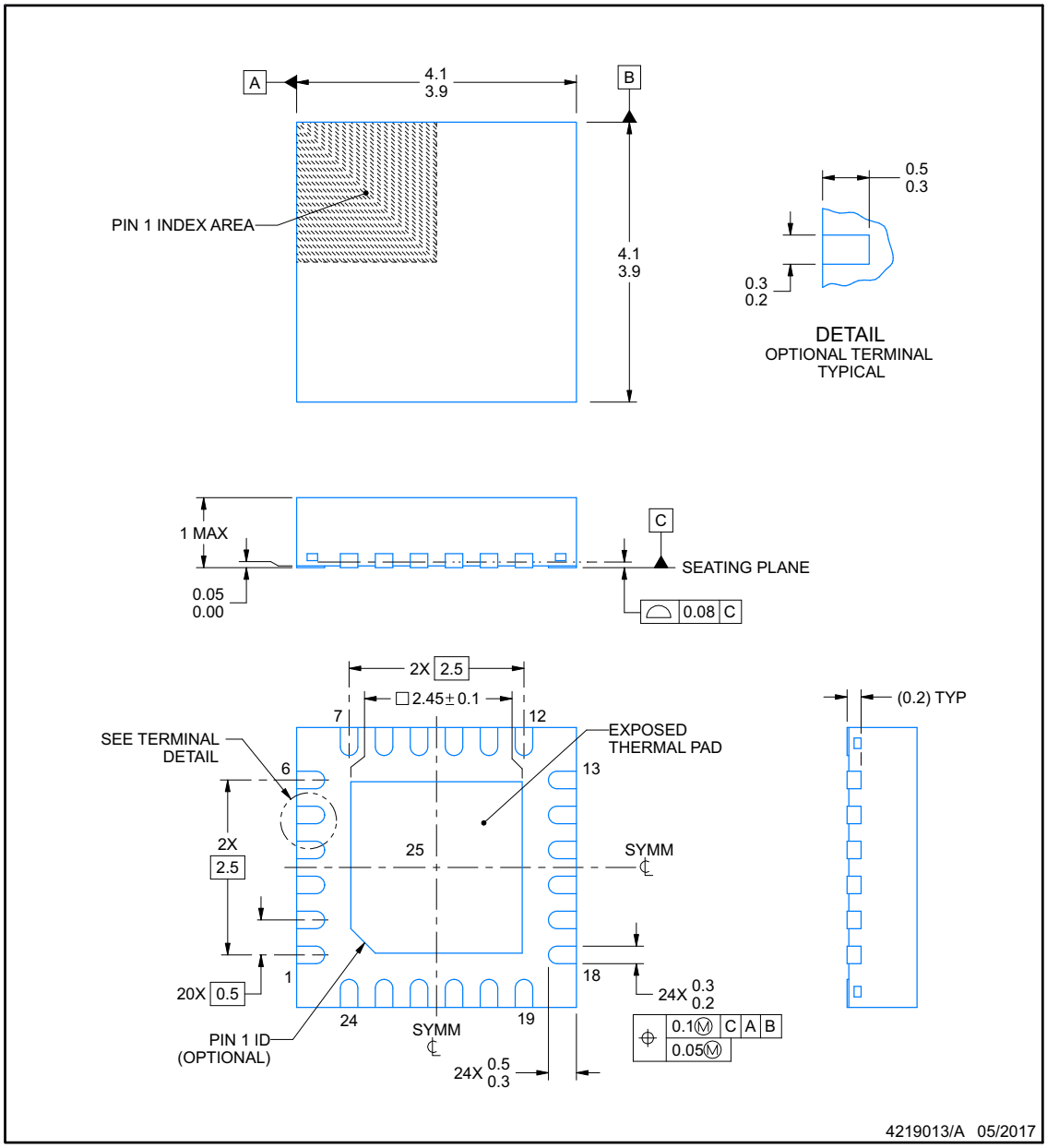
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

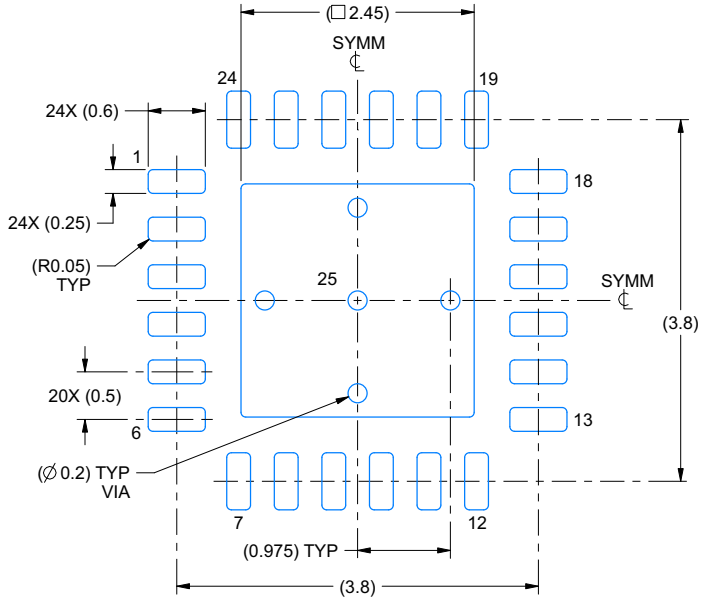
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

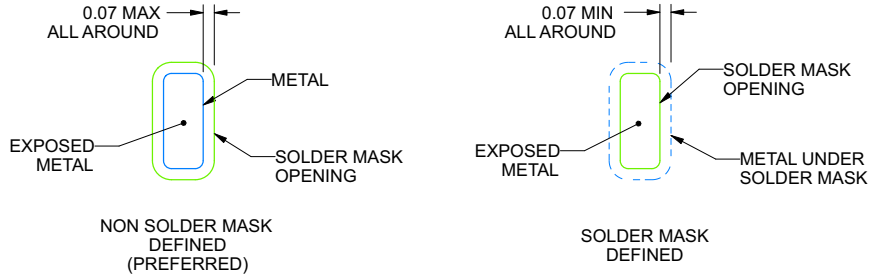
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

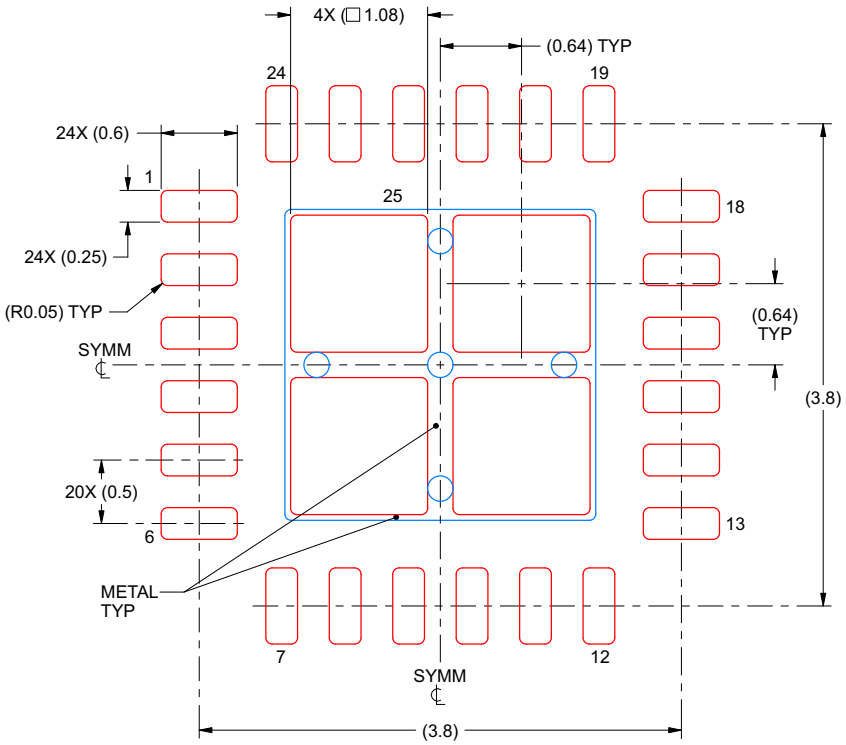
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

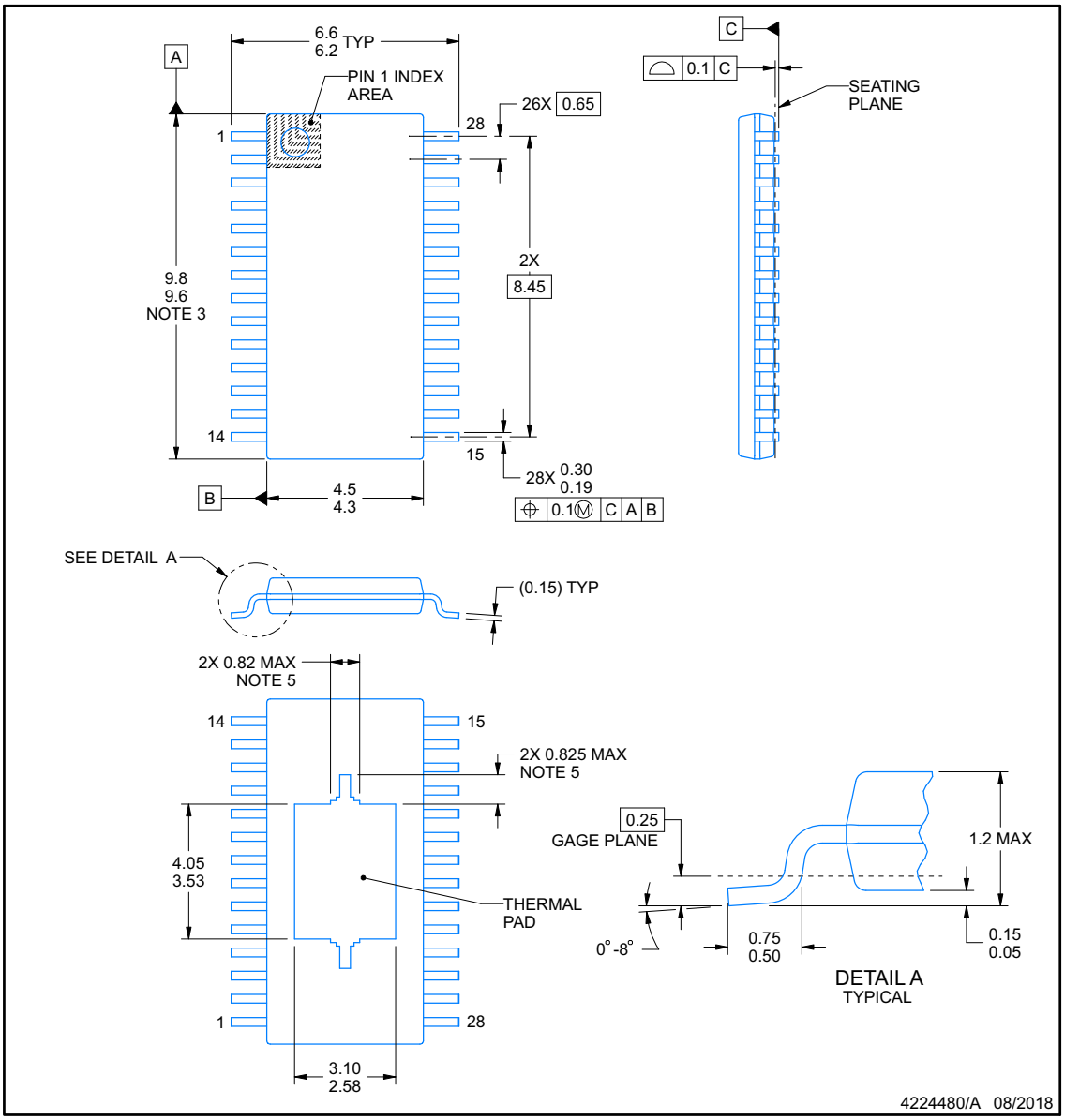
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

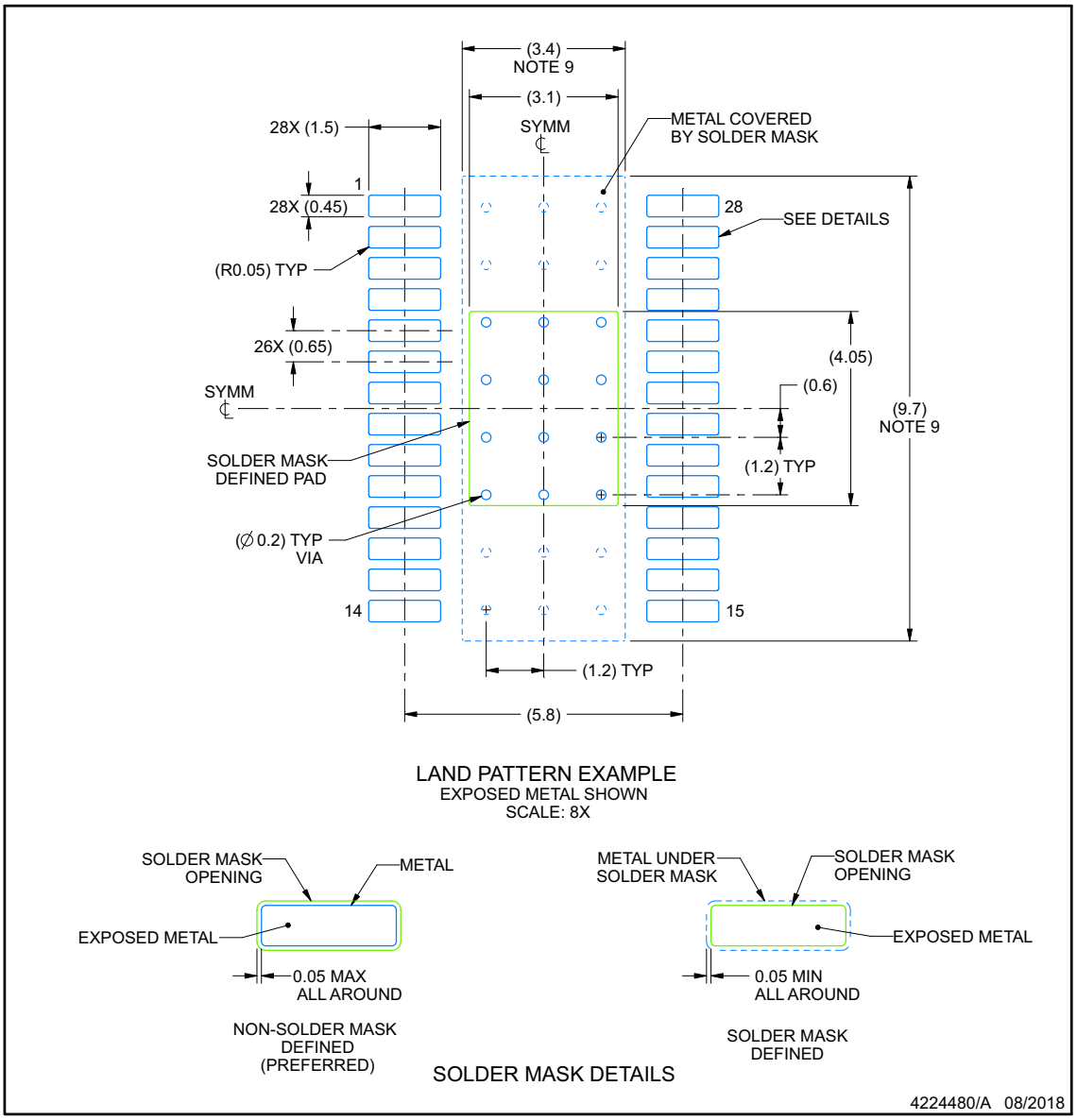
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

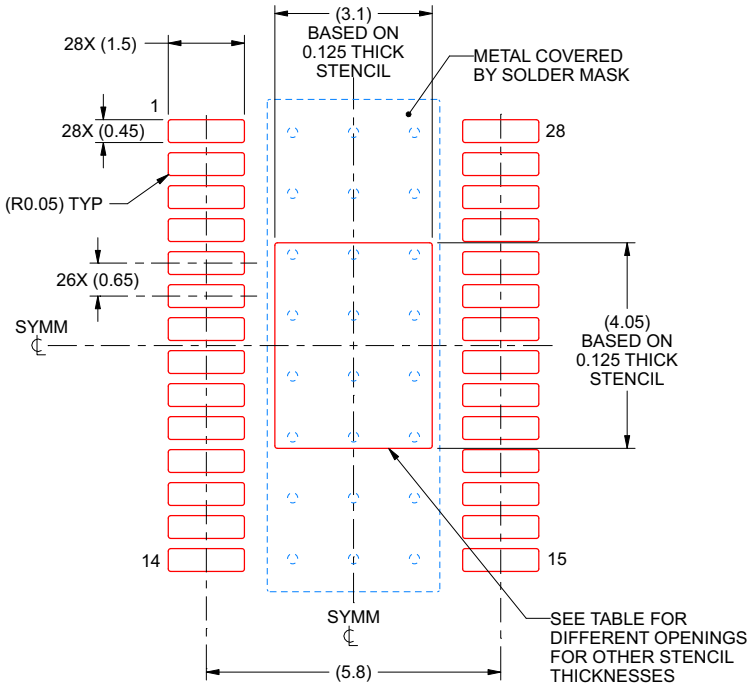
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8955PPWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8955P	Samples
DRV8955PRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8955P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

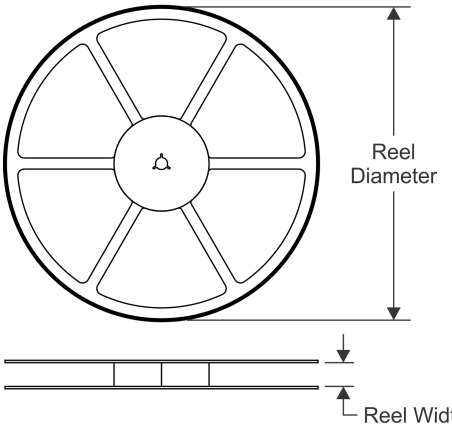
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

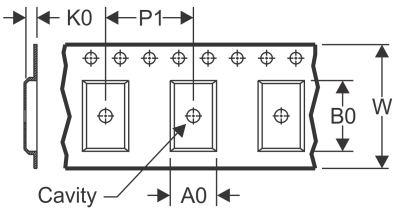
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

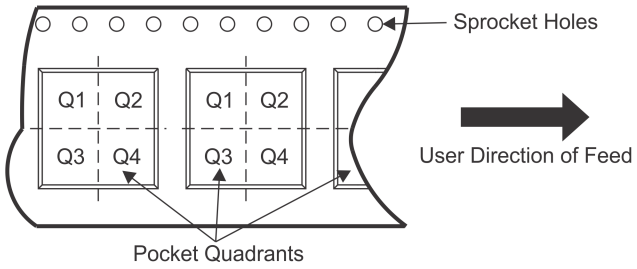


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

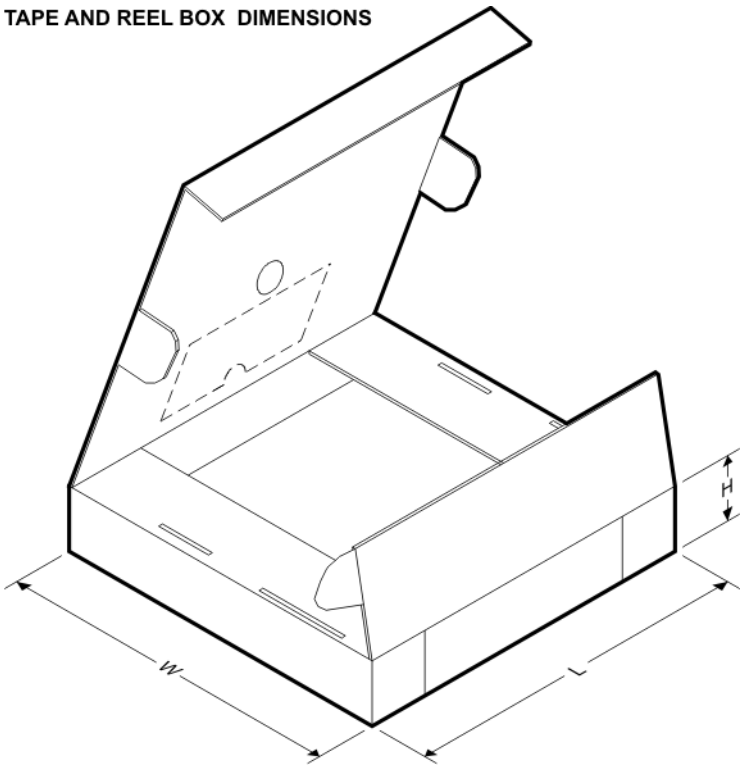
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8955PPWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8955PRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8955PPWPR	HTSSOP	PWP	28	2500	853.0	449.0	35.0
DRV8955PRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

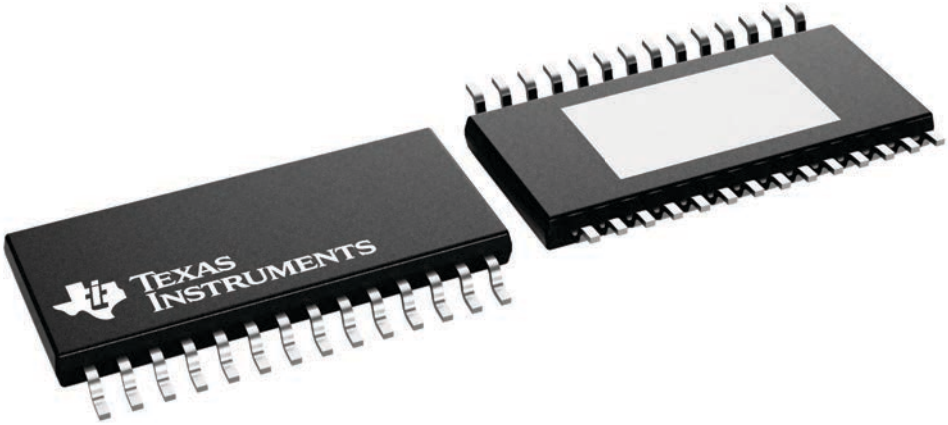
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

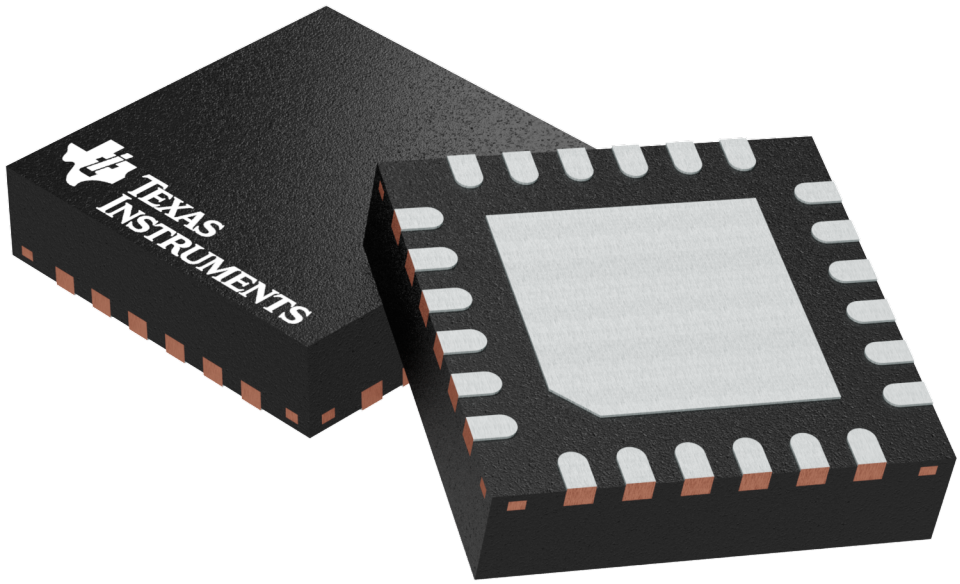


4224765/B

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

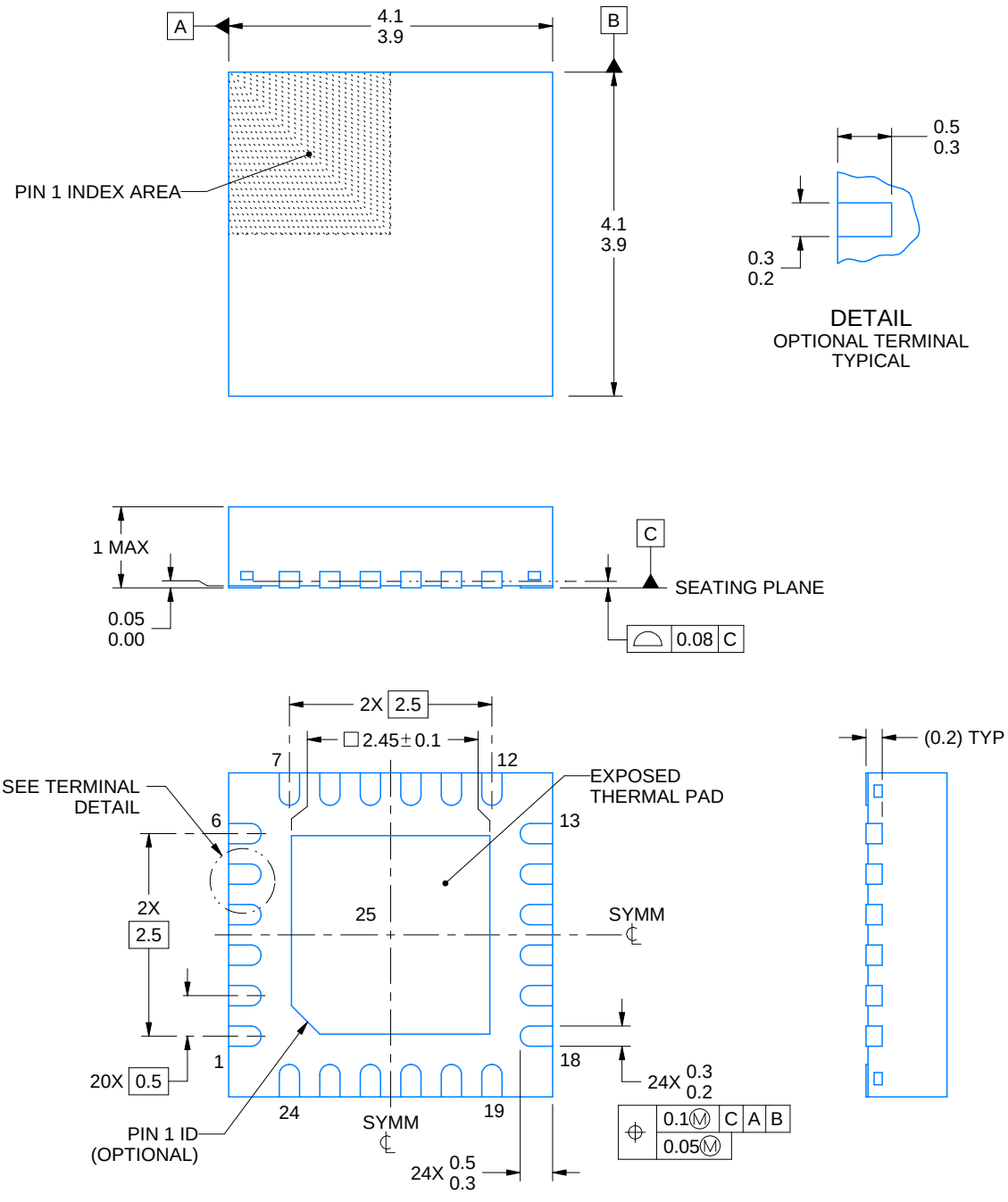
4204104/H

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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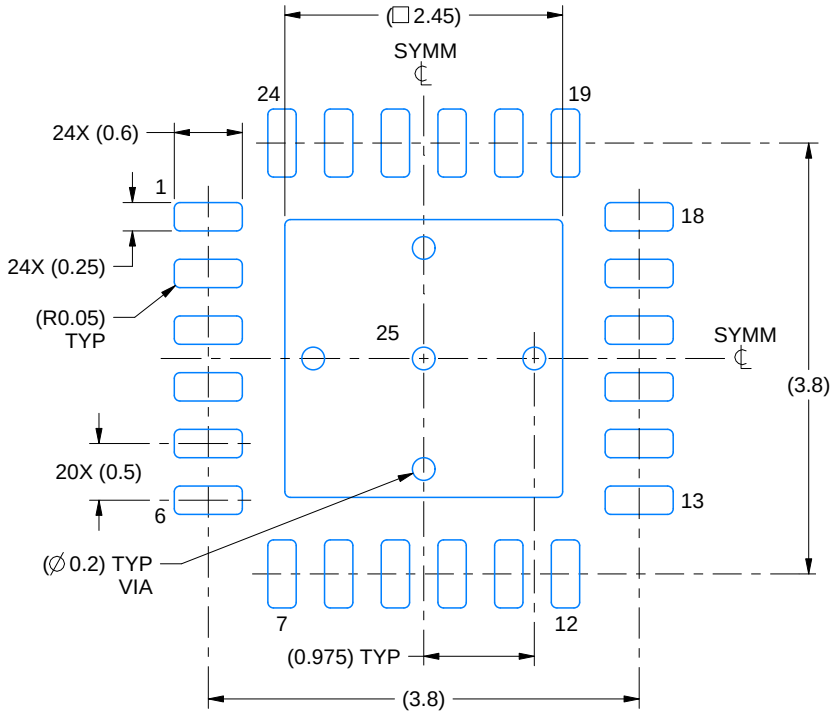
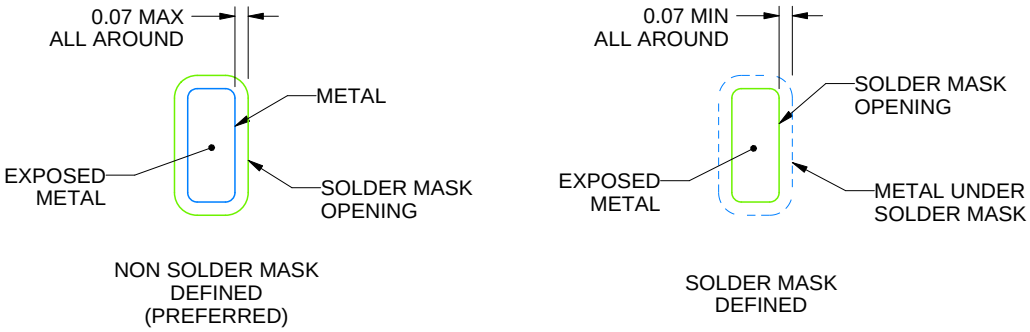


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

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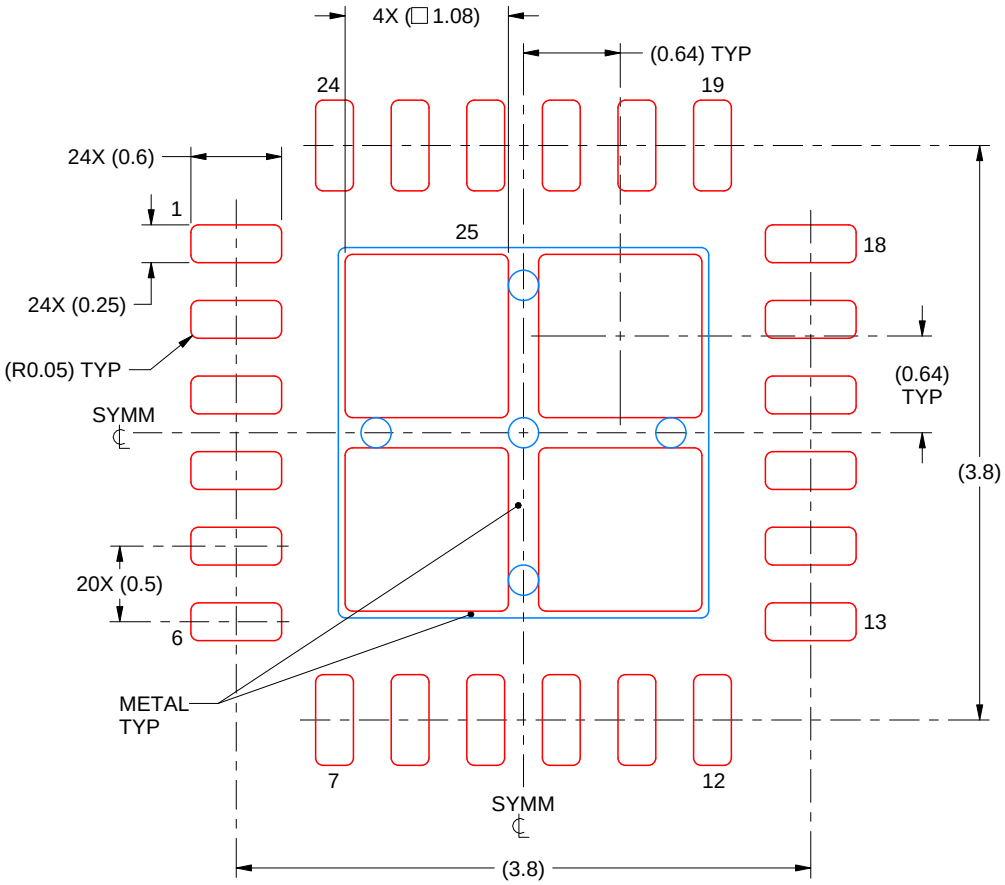

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

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