具有集成辅助偏置电源的 LM5036 半桥 PWM 控制器

1 特性

- 适用于小外形尺寸、高密度直流/直流电源转换器的高集成度控制器
- 集成 100V、100mA 辅助偏置电源
- 全稳压预偏置启动
- 适用于低侧和高侧初级 FET 的具有脉冲匹配的增强型逐周期电流限制
- 针对初级侧 FET 优化了最大占空比
- 带有输入电压前馈的电压模式控制
- 100V 高压启动稳压器
- 可配置锁存器，支持 OVP
- 用于初级侧 FET 的集成式 100V、2A MOSFET 驱动器
- 初级侧和同步整流器 (SR) FET 之间的死区时间可编程
- 使用 LM5036 并借助 Excel 计算器工具或 WEBENCH®电源设计器创建定制设计方案

2 应用

- 电信和数据通信隔离式电源
- 工业电源和工厂自动化
- 测试和测量设备

3 说明

LM5036 器件是一款 PWM 控制器，集成了辅助偏置电源，可为工业隔离式电源 应用提供高功率密度。该器件包含 使用 带有输入电压前馈的电压模式控制来实现半桥功率转换器所需的所有功能。该器件适合在直流输入电压高达 100V 的隔离式转换器的初级侧运行。

LM5036 包含的 功能 可提高功率密度和可靠性，同时可降低系统成本：

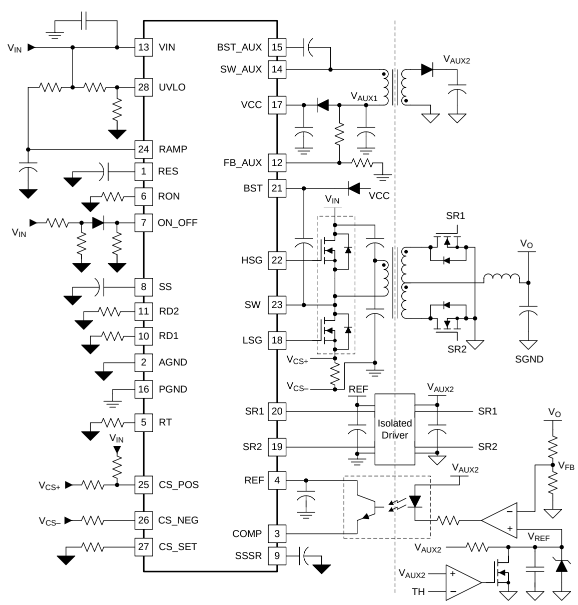
- 作为辅助偏置电源的集成 Fly-Buck 转换器。为一级和二级电路提供偏置电源，具有极少的外部组件。
- 全稳压预偏置启动。即使启动到预充电输出电容器时，也可消除输出电压过冲或突降。
- 具有脉冲匹配的增强型逐周期峰值电流限制。LM5036 可限制正负电流。脉冲匹配可确保低侧和高侧器件具有相等的脉宽，以避免变压器饱和。输出电流限制在整个输入电压范围内保持大致恒定。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
LM5036	WQFN (28)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用



目录

4 修订历史记录

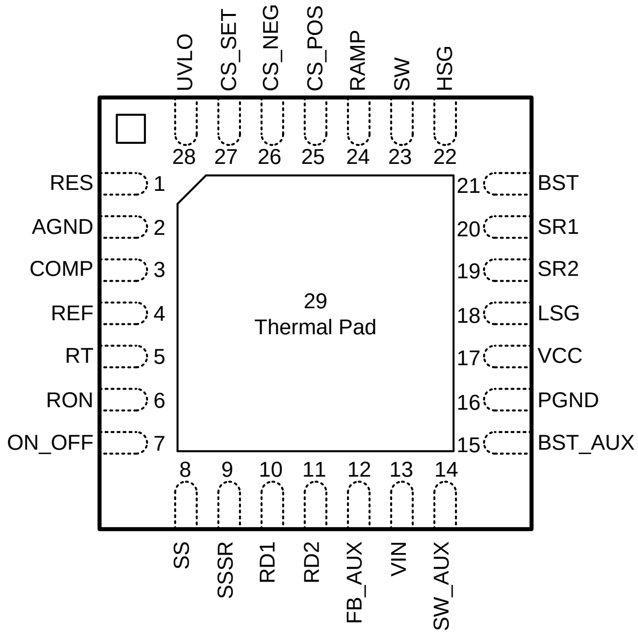
Changes from Revision A (May 2018) to Revision B **Page**

修订历史记录 (接下页)

Changes from Original (May 2018) to Revision A **Page**

5 Pin Configuration and Functions

RJB Package
28-Pin WQFN
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	2	G	Analog ground
BST	21	I	Half-bridge high-side gate drive bootstrap
BST_AUX	15	I	Auxiliary supply high-side gate drive bootstrap
COMP	3	I	Control current input to half-bridge PWM comparator
CS_NEG	26	I	Current sense amplifier negative input terminal
CS_POS	25	I	Current sense amplifier positive input terminal
CS_SET	27	I	Current limit setting
FB_AUX	12	I	Auxiliary supply output voltage feedback
HSG	22	O	Half-bridge high-side MOSFET output driver
LSG	18	O	Half-bridge low-side MOSFET output driver
ON_OFF	7	I	Configurable for over voltage protection (OVP) or latch mode
PGND	16	G	Power ground
RAMP	24	I	RAMP signal input to half-bridge PWM comparator
RD1	10	I	Synchronous rectifier trailing-edge delay
RD2	11	I	Synchronous rectifier leading-edge delay
REF	4	O	5-V reference regulator output
RES	1	I	Hiccup mode restart timer
RON	6	I	Auxiliary supply on-time control
RT/SYNC	5	I	Oscillator frequency control or external clock synchronization
SR1	20	O	Synchronous rectifier PWM control output
SR2	19	O	Synchronous rectifier PWM control output
SS	8	I	Soft-start input

(1) I = input, O = output, G = ground

Pin Functions (continued)

PIN		I/O [(1)]	DESCRIPTION
NAME	NO.		
SSSR	9	I	Synchronous rectifier soft-start input
SW	23	I	Half-bridge switch node
SW_AUX	14	I	Auxiliary supply switch node
UVLO	28	I	Input undervoltage lockout
VCC	17	I	Bias supply
VIN	13	I	Input voltage
Pad	29	G	Exposed thermal pad

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
VIN to GND	-0.3	105	V
SW/SW_AUX to GND	-5	105	V
BST TO SW, BST_AUX TO SW_AUX	-0.3	16	V
HSG to SW	-0.3	16	V
LSG to GND	-0.3	16	V
SR1/SR2 to GND	-0.3	5	V
VCC to GND	-0.3	16	V
RT, UVLO, ON/OFF, RON, RAMP, RES, FB_AUX, CS_POS, CS_NEG, CS_SET to GND	-0.3	5	V
COMP to GND		-0.3	V
COMP Input Current		10	mA
Junction Temperature		150	ºC
Storage Temperature, Tstg	-55	150	ºC

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	16		100	V
External V_{CC}	Supply Voltage	8.5		14	V
RD_x	RD_1, RD_2 Resistor value	5			kΩ
T_J	Junction Temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM5036 RJB (WQFN) 28 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	29.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	18.2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.3	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report*.

6.5 Electrical Characteristics

MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, R_T = 25 kΩ, RD_1 = RD_2 = 20 kΩ, R_{ON} =100 kΩ. No load on LSG, HSG, SR1, SR2, UVLO = 2.5 V, ON_OFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
START-UP REGULATOR						
V_{CC}	Vcc voltage	I_{CC} = 10 mA	7.5	7.8	8.1	V
$I_{CC\ (Lim)}$	Vcc current limit	V_{CC} = 6 V, V_{IN} = 20 V	69	81	94	mA
$I_{CC(ext)}$	Vcc supply current	Supply current into Vcc from an externally applied source. V_{CC} = 9 V, FB_AUX = 0 V	6.6	9	11	mA
$V_{CC(reg)}$	Vcc load regulation	I_{CC} from 0 to 50 mA	31	49	73	mV
$V_{CC(UV)}$	Vcc undervoltage threshold	Positive going Vcc	7.4	7.7	8.0	V
		Negative going Vcc	6.1	6.3	6.7	V
	V_{IN} shutdown current	V_{IN} = 20 V, V_{UVLO} = 0 V, R_{ON} = 100 kΩ	276	580	670	µA
		V_{IN} = 100 V, V_{UVLO} = 0 V, R_{ON} = 100 kΩ	299	600	717	µA
	V_{IN} start-up regulator leakage	V_{CC} = 9 V, applied externally, FB_AUX > 2 V, SS = 0 V, R_{ON} = 100 kΩ	180	234	304	µA
VOLTAGE REFERENCE REGULATOR (REF PIN)						
V_{REF}	REF voltage	I_{REF} = 0 mA	4.85	5	5.15	V
$V_{REF(REG)}$	REF load regulation	I_{REF} = 0 to 25 mA	24	37	57	mV
$I_{REF(LIM)}$	REF current limit	V_{REF} = 4.5 V, V_{IN} = 20 V	28	39	47	mA
$V_{REF(UV)}$	REF undervoltage threshold	Positive going V_{REF}	4.3	4.5	4.7	V
	Hysteresis		0.16	0.26	0.37	V
UNDERVOLTAGE LOCK OUT AND SHUTDOWN (UVLO PIN)						
V_{UVLO}	UVLO threshold		1.205	1.25	1.305	V
I_{UVLO}	UVLO Hysteresis current		15	20	24	µA
V_{SD}	Internal startup regulator enable threshold	SS = 0 V, FB_AUX = 2.5 V	0.34	0.38	0.41	V
	Hysteresis		90	135	175	mV
OVER-VOLTAGE/LATCH (ON_OFF PIN)						
V_{ON_OFF}	ON_OFF threshold		1.18	1.25	1.32	V
I_{OVL}	ON_OFF hysteresis current		40	50	60	µA
SOFT-START (SS PIN, SSSR PIN)						
I_{SS}	SS charge current	SS = 0 V	17	20	24	µA

Electrical Characteristics (continued)

MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, R_T = 25 kΩ, RD_1 = RD_2 = 20 kΩ, R_{ON} =100 kΩ. No load on LSG, HSG, SR1, SR2, UVLO = 2.5 V, ON_OFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SSSecEn}$	SS threshold to enable SSSR charge current	I_{COMP} < 800 µA	1.93	2.06	2.2	V
	SS output low voltage	Sinking 100 µA	30	48	57	mV
	SS threshold to disable switching		865	1000	1198	mV
I_{SSSR}	SSSR charge current	SS > 2 V, I_{COMP} < 800 µA	17	20	24	µA
	SSSR output low voltage	Sinking 100 µA	30	38.7	49	mV
V_{SSREn}	SSSR threshold to enable SR freewheeling pulse		0.65	1.17	1.67	V
CURRENT SENSE (CS_POS, CS_NEG, and CS_SET PIN)						
V_{LIM}	Current limit setting voltage		0.72	0.75	0.77	V
	Ratio of internal negative to positive current limit threshold		0.3	0.58	0.9	
t_{CSLSG}	CS to gate driver output delay		60	85	122	ns
t_{CSBLK}	CS leading-edge blanking		33	53	76	ns
K_{CBC1} (1)	V_{LIM} x (K_{2a} X K_{10b} - K_{10a})	At CBC trip threshold	7.28	7.51	7.81	V
$V_{CSOffset}$ (1)	V_{CS_POS} - V_{CS_NEG}	At CBC trip threshold	-0.63	-0.02	0.32	mV
$I_{BiasOffset}$ (1)	$I_{BiasPOS}$ - $I_{BiasNEG}$	At CBC trip threshold	-0.67	0.02	0.29	µA
I_{SLOPE} (1)	Peak value of current source for slope compensation		50	54	59	µA
REVERSE CURRENT PROTECTION						
N	Number of switching periods to reset negative over-current event counter			4		
SR_CTR_TH	SSSR threshold to reset SSSR cap clamp event counter		4.8	4.94	5.1	V
HICCUP MODE (RES PIN)						
R_{RES}	RES pulldown resistance	Termination of hiccup timer	24	36	55	Ω
V_{RESTh1}	RES hiccup threshold		0.90	1	1.04	V
V_{RESTh3}	RES upper counter threshold		3.91	4	4.07	V
V_{RESTh2}	RES lower counter threshold		1.95	2	2.04	V
$I_{RES-SRC1}$	Charge current source1	V_{RES} < 1 V, CBC active	12	15	18	µA
$I_{RES-SRC2}$	Charge current source2	1 V < V_{RES}< 4 V	25	30	36	µA
$I_{RES-DIS1}$	Discharge current source1	CBC not active	3.2	5	5.5	µA
$I_{RES-DIS2}$	Discharge current source2	2 V < V_{RES} < 4 V	2.5	5	7.5	µA
HICCUP MODE BLANKING						
$V_{HC\_BLK\_TH}$	SSSR threshold to disable the hiccup blanking		5.26	5.5	5.66	V
VOLTAGE FEED-FORWARD (RAMP PIN)						
	RAMP sink impednace (clocked)		3.9	6.0	9.1	Ω
OSCILLATOR (RT PIN)						
f_{SW1}	Frequency (half oscillator frequency)	R_T = 25 kΩ	185	200	215	kHz
f_{SW2}	Frequency (half oscillator frequency)	R_T = 10 kΩ	420	480	540	kHz
V_{RTReg}	DC level		1.85	2	2.06	V
V_{RTSync}	RT sync threshold		2.8	3	3.3	V
SYNCHRONOUS RECTIFIER TIMING CONTROL (RD1 and RD2 PINS)						
t_1	SR trailing edge delay SR turn-off to primary switch turn-on	RD_1 = 20 kΩ	94	123	157	ns

(1) Guaranteed By Design

Electrical Characteristics (continued)

MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, R_T = 25 kΩ, RD_1 = RD_2 = 20 kΩ, R_{ON} =100 kΩ. No load on LSG, HSG, SR1, SR2, UVLO = 2.5 V, ON_OFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		RD_1 = 100 kΩ	213	278	350	ns
t_2	SR leading edge delay primary switch turn-off to SR turn-on	RD_2 = 20 kΩ	60	79	102	ns
		RD_2 = 100 kΩ	188	250	315	ns
t_{clk}	Pulse width of the clock		47	65	87	ns
COMP PIN						
I_{PWM-OS}	COMP current to RAMP offset	RAMP = 0 V	596	800	1063	µA
V_{SS-OS}	SS to RAMP offset	RAMP = 0 V	0.86	1	1.15	V
	COMP current to RAMP gain	delta RAMP/delta I_{COMP}	1895	2400	2936	Ω
	SS to RAMP gain	delta SS/delta RAMP	0.574	0.646	0.74	
$I_{COSsrEn}$	COMP current for SSSR charge curent enable	SS > 2 V	600	750	900	µA
	COMP to gate driver output delay		100	120	150	ns
	Minimum duty cycle	I_{COMP} = 1 mA			0	%
BOOST (BST PIN)						
$V_{BST(UV)}$	BST under-voltage threshold	V_{BST} - V_{SW} rising	3.2	4.137	5.6	V
	Hysteresis		0.37	0.481	0.65	V
LSG, HSG GATE DRIVERS						
V_{OL_PRI}	Low-state output voltage	$I_{HSG/LSG}$ = 100 mA	0.1	0.3	0.41	V
V_{OH_PRI}	High-state output voltage	$I_{HSG/LSG}$ = 100 mA, V_{OHL_PRI} = V_{CC} - V_{LSG}, V_{OHH_PRI} = V_{BST} - V_{HSG}	0	0.38	1	V
	Rise Time	C-load =1000 pF	2	8	12	ns
	Fall Time	C-load =1000 pF	2	10	14	ns
I_{SO_PRI}	Peak Source Current	$V_{HSG/LSG}$ = 0V		1.5		A
I_{SI_PRI}	Peak Sink Current	$V_{HSG/LSG}$ = VCC		2		A
SR1, SR2 GATE DRIVERS						
V_{OL_SR}	Low-state output voltage	$I_{SR1/SR2}$ = 10 mA			0.12	V
V_{OH_SR}	High-state output voltage	$I_{SR1/SR2}$ = 10 mA, V_{OH_SR} = V_{REF} - V_{SR}			0.313	V
	Rise Time	C-load = 1000 pF	25	45	65	ns
	Fall Time	C-load = 1000 pF	4	10	16	ns
I_{SO_SR}	Peak Source Current	V_{SR} = 0 V	0.05	0.09	0.14	A
I_{SI_SR}	Peak Sink Current	V_{SR} = V_{REF}	0.1	0.2	0.4	A
HALF BRIDGE THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temp			150		ºC
	Thermal Shutdown Hysteresis			25		ºC
AUX SUPPLY SWITCH CHARACTERISTICS						
	Buck Switch $R_{DS(ON)}$	I_{TEST}= 60 mA	3.0	5.2	7.5	Ω
	Synchronous Switch $R_{DS(ON)}$	I_{TEST}= 60 mA	1.2	2.8	4.5	Ω
AUX SUPPLY UNDERVOLTAGE LOCKOUT						
$V_{BST\_AUX(UV)}$	BST_AUX undervoltage threshold	V_{BST_AUX} - V_{SW_AUX} rising	2.1	2.8	3.6	V
V_{AUX_UVLO}	AUX supply UVLO input voltage rising threshold		12.2	15	16.0	V
	AUX supply UVLO input voltage falling threshold		7.9	11.2	12.7	V
AUX SUPPLY REGULATION						

Electrical Characteristics (continued)

MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, R_T = 25 kΩ, RD_1 = RD_2 = 20 kΩ, R_{ON} =100 kΩ. No load on LSG, HSG, SR1, SR2, UVLO = 2.5 V, ON_OFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{AUX\text{-}OFF}$	OFF-State AUX Voltage Regulation Level		1.26	1.4	1.53	V
$V_{AUX\text{-}ON}$	ON-State AUX Voltage Regulation Level		0.95	1	1.04	V
AUX SUPPLY CURRENT LIMIT						
$I_{AUX(LIM)}$	AUX Supply Current Limit Threshold		150	200	250	mA
t_{CSBLKA}	Current limit comparator blanking period measured from start of t_{ON} period (1)			50		ns
$t_{AUX(LIM)}$	Delay from Comparator Threshold to upper MOSFET turn-OFF (1)			116		ns
τ_{AuxSns}	Aux Current Limit Parasitic Filter time constant (1)			41		ns
AUX SUPPLY THERMAL SHUTDOWN						
T_{SD_AUX}	AUX Supply Thermal Shutdown Temp			160		ºC
	AUX Supply Thermal Shutdown Hysteresis			28		ºC

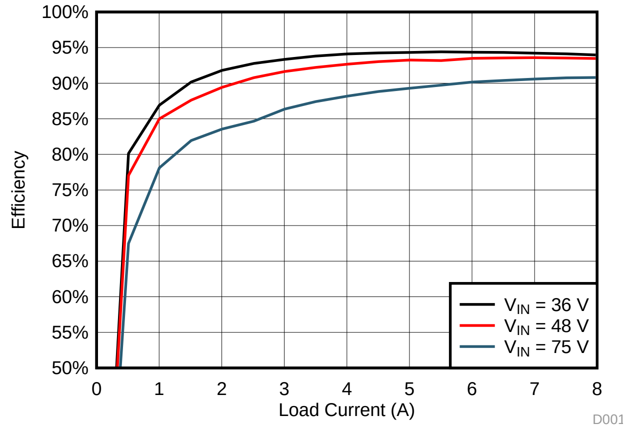
6.6 Switching Characteristics

MIN and MAX limits apply the junction temperature range of –40°C to 125°C. Unless otherwise specified, the following conditions apply: V_{IN} = 48 V, R_T = 25 kΩ, RD_1 = RD_2 = 20 kΩ, R_{ON} =100 kΩ. No load on LSG, HSG, SR1, SR2, UVLO = 2.5 V, ON_OFF = 0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	AUX SUPPLY ON-TIME	V_{IN} = 32 V, R_{ON} = 100 kΩ	240	330	440	ns
t_{ON}	AUX SUPPLY ON-TIME (1)	V_{IN}=54 V, R_{ON} = 250 kΩ		493		ns
t_{ON}	AUX SUPPLY ON-TIME (1)	V_{IN}=75V, R_{ON} = 250 kΩ		370		ns
$t_{OFF(MIN)}$	AUX SUPPLY MINIMUM OFF-TIME	FB_AUX = 0 V	69	103	136	ns

(1) Guaranteed by design.

6.7 Typical Characteristics



f_{SW} = 200-kHz V_O = 12-V

图 1. Application Board Efficiency vs Load Current

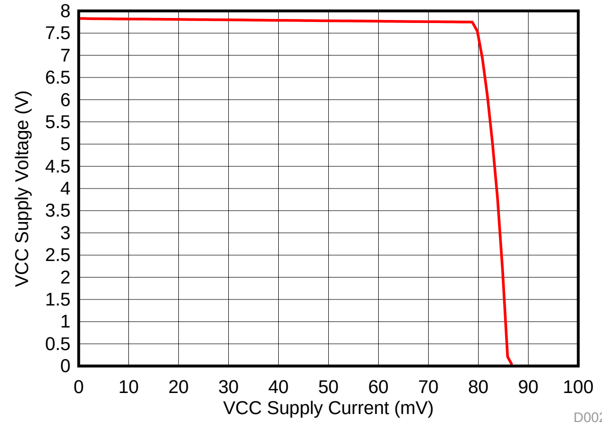


图 2. VCC Load Regulation

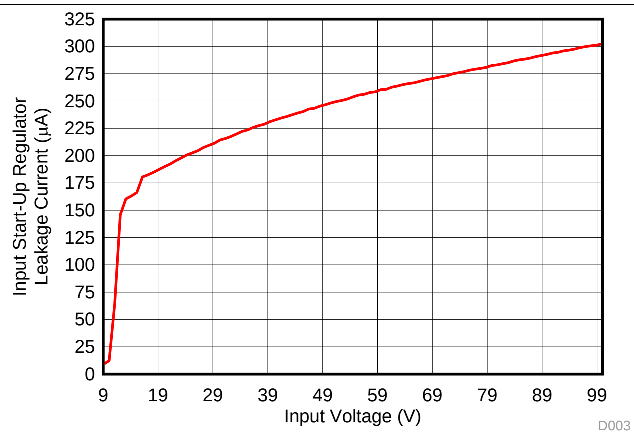


图 3. Input Leakage Current of Start-up Regulator vs Input Voltage

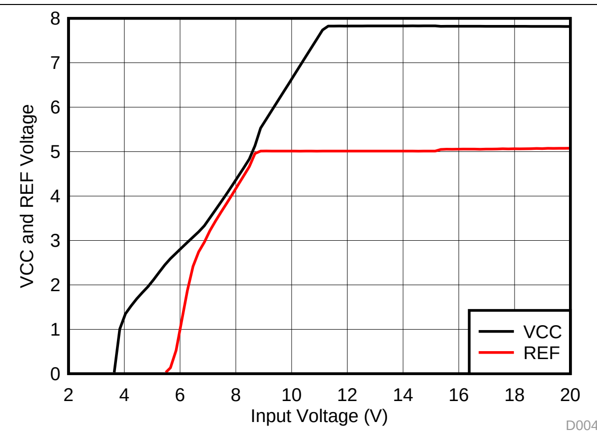


图 4. VCC and REF Voltage vs Input Voltage

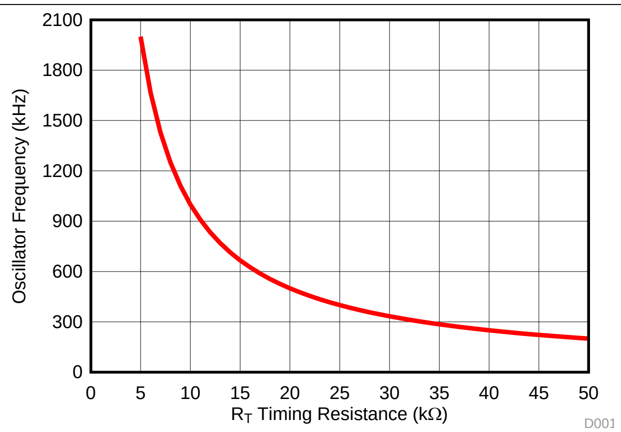


图 5. Oscillator Frequency vs R_T Timing Resistance

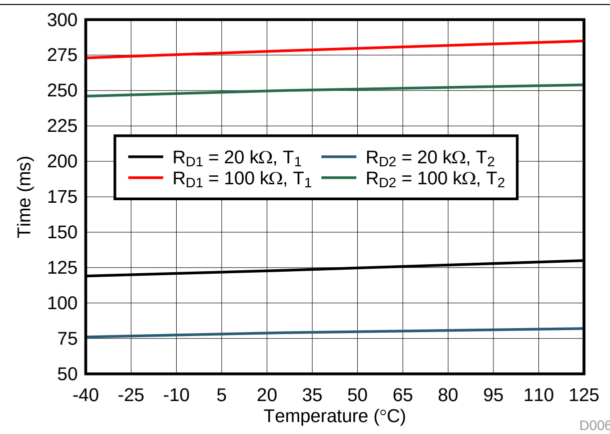


图 6. Dead Time vs Temperature

Typical Characteristics (接下页)

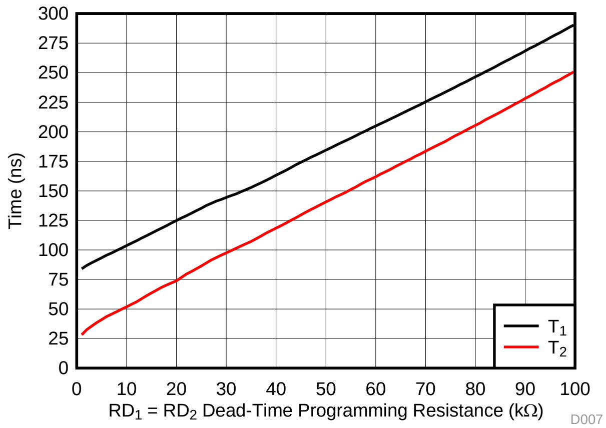


图 7. Dead Time vs Programming Resistance

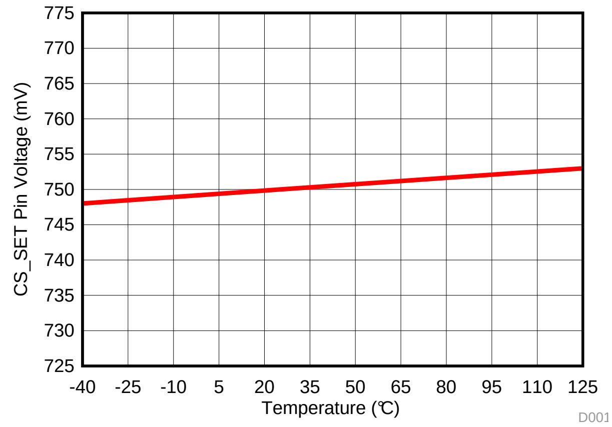


图 8. CS_SET Pin Voltage vs Temperature

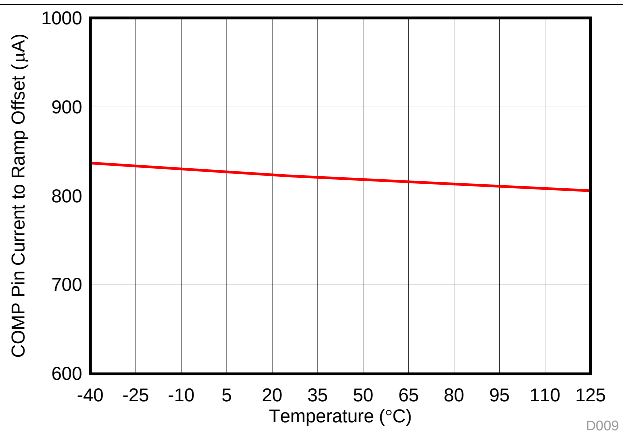


图 9. COMP Pin to 1-V RAMP Offset vs Temperature

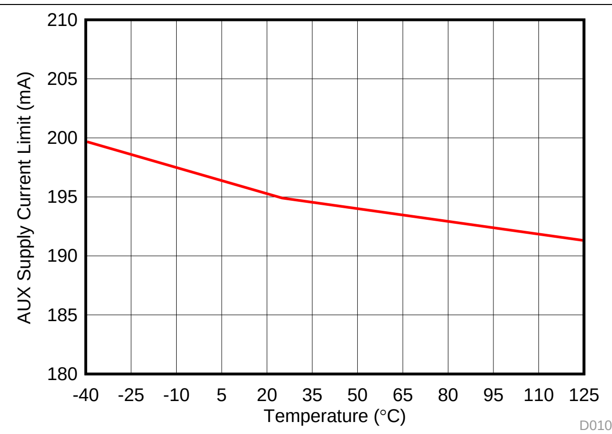


图 10. Auxiliary Supply Current Limit vs Temperature

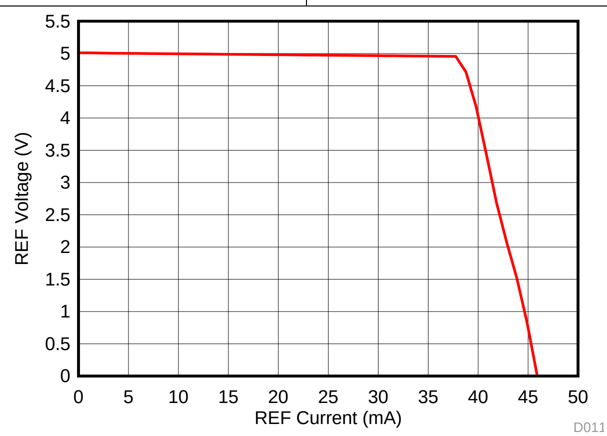


图 11. REF Load Regulation

7 Detailed Description

7.1 Overview

The LM5036 device is a highly-integrated, half-bridge PWM controller with integrated auxiliary bias supply. It provides a high power-density solution for telecom, datacom and industrial power converters. The device has all of the features necessary to implement a power converter that uses half-bridge topology. The device employs voltage-mode control and includes input voltage feed-forward to improve performance. This device operates on the primary side of an isolated DC-DC power converter with input voltage up to 100-V.

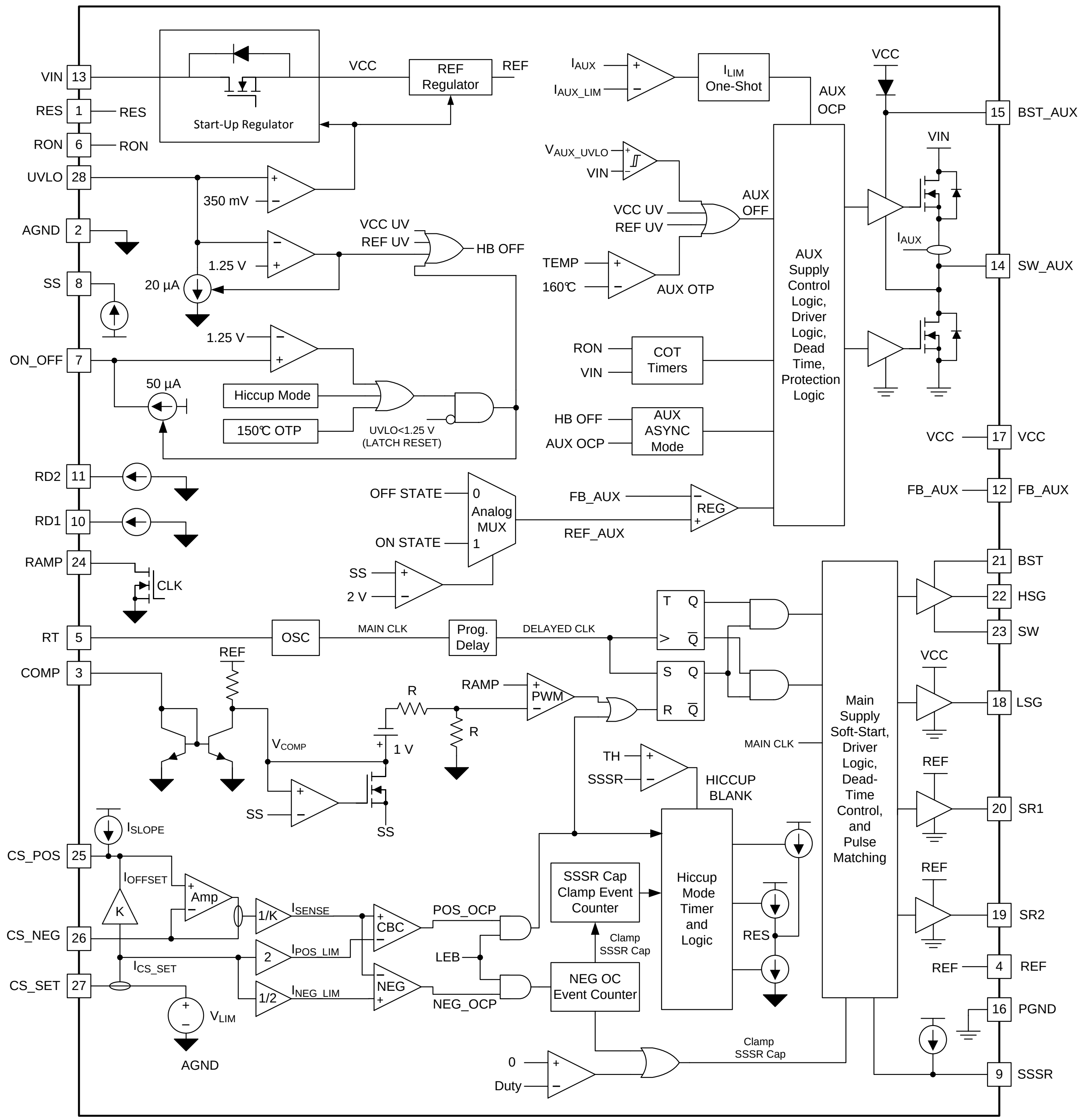
The soft-start function provides a fully regulated and monotonic rise of output voltage, even when the converter energizes into a pre-biased load. The device uses an enhanced cycle-by-cycle (CBC) current limit. This function matches the pulse to maintain the voltage balance of the half-bridge capacitor divider. This method ensures flux balance of the transformer during CBC operation. The input voltage compensation function helps to minimize the variation of the current limit level across the entire input voltage range.

The LM5036 device has these other features:

- configurable latch protection
- configurable overvoltage protection (OVP)
- optimized maximum duty cycle operation for the primary MOSFETs
- integrated half-bridge MOSFET gate drivers
- programmable dead-time between the primary MOSFETs and synchronous rectifiers
- auxiliary supply synchronous and asynchronous mode transition
- 5-V synchronous rectifier PWM outputs
- programmable line undervoltage lockout (UVLO)
- hiccup mode overcurrent protection (OCP)
- reverse current protection
- a 2-MHz capable oscillator with synchronization capability
- two-level thermal shutdown protection

An Excel Calculator Tool is provided to ease the process of creating custom designs using this controller. This tool calculates values for all the external components required by the controller to meet a given specification. It also generates many key parameters of the power stage including, for example, the turns ratio of the half-bridge transformer. The tool generates graphs predicting, for a given set of current limit components, how the output current limit will vary with input voltage. Maximum flexibility is offered by calculating suggested values for most components, but allowing the user to input values of their own choice.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM5036 device contains a high-voltage VCC start-up regulator that allows the input pin (VIN) to be connected directly to an input voltage up to 100-V. Higher input voltages can be accommodated by adding some additional external parts, as described in Applications with V_{IN} > 100-V. When the UVLO pin voltage is greater than V_{SD} (0.38-V typical), the start-up regulator is enabled to charge an external capacitor connected to the VCC pin. The output voltage of the VCC regulator is regulated at V_{CC} (7.8-V typical). The VCC regulator provides power to the reference (REF) regulator. The regulator output at VCC is internally current limited to $I_{CC(Lim)}$ (81-mA typical) . The value of the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.47-µF to 10-µF.

LM5036 can power itself using its internal high-voltage start-up linear regulator, but internal power dissipation can be reduced by powering VCC from an auxiliary switched mode supply. LM5036 device integrates all of the functions needed to implement a low-cost and easy-to-design isolated fly-buck auxiliary supply based on the constant-on-time (COT) control scheme. The primary output V_{AUX1} of the auxiliary supply must be connected through a diode to the VCC pin, as shown in 图 12. The auxiliary supply must raise the VCC voltage above the internally generated V_{CC} voltage in order to shut off the internal start-up regulator. Powering VCC from an auxiliary switched mode supply improves efficiency while reducing the power dissipation of the controller IC. The VCC under-voltage (UV) circuit will still function in this mode, requiring that VCC never falls below its UV threshold during the start-up sequence. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore, the auxiliary VCC voltage should never exceed the V_{IN} voltage.

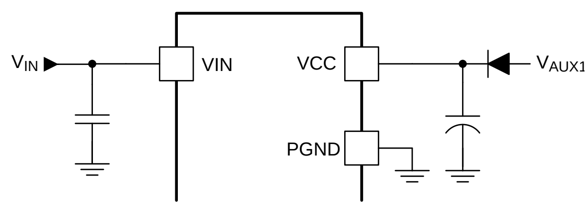


图 12. External VCC Bias Supply Connection

7.3.2 Undervoltage Lockout (UVLO)

The LM5036 device contains a three-level under-voltage lockout circuit. When the UVLO pin voltage is below V_{SD} (0.38-V typical), the controller is in a low current shutdown mode where the functional circuit blocks are not enabled including VCC startup regulator, auxiliary supply and the main half-bridge control logic and gate drive circuitry, etc.

When UVLO pin voltage is above V_{SD}, the VCC and REF regulators become active.

When the VCC and REF outputs exceed their respective UV thresholds and the input voltage V_{IN} rises above V_{AUX_UVLO} (15-V typical), the auxiliary supply is enabled.

When UVLO pin voltage rises above V_{UVLO} (1.25-V typical) and VCC and REF voltage are above their respective UV thresholds, the control logic of the main half-bridge converter is enabled. The soft-start capacitor is released and normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the half-bridge converter. The divider must be designed such that the voltage at the UVLO pin is greater than V_{UVLO} when V_{IN} enters the desired operating range. UVLO hysteresis is accomplished with an internal current sink I_{UVLO} (20-µA typical) that is switched on or off into the impedance of the external set-point divider. When the UVLO pin voltage threshold of V_{UVLO} is exceeded, the current sink is deactivated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the V_{UVLO} threshold, the current sink is enabled causing the voltage at the UVLO pin to quickly fall. See 表 1 for more detail on functional modes of LM5036.

7.3.3 Reference Regulator

The REF pin is the output of a 5-V linear regulator that can be used to bias an opto-coupler transistor, primary side of an isolated gate driver or digital isolator, among other housekeeping circuits. The regulator output is internally current limited to $I_{REF(LIM)}$ (39-mA typical). The REF pin must be locally decoupled with a ceramic capacitor, the recommended range of values is from 0.1-µF to 10-µF.

7.3.4 Oscillator, Synchronized Input

The oscillator frequency of LM5036 device is set by a resistor connected between the RT pin and AGND. The R_T resistor should be located close to the device. To set a desired oscillator frequency (f_{OSC}), the value of R_T resistor can be calculated from 公式 1.

$$R_T = \frac{1}{f_{OSC} \times 1 \times 10^{-10}} \tag{1}$$

For example, if the desired oscillator frequency is 400-kHz, that is, each phase (LSG and HSG) switches at 200-kHz, the value of R_T is calculated to be 25-kΩ. If the LM5036 device is to be synchronized to an external clock, that signal must be coupled into the RT pin through a 100-pF capacitor. The RT pin voltage is nominally regulated at V_{RTReg} (2-V typical) and the external pulse amplitude should lift the pin to between 3.5-V and 5.0-V on the low-to-high transition. The synchronization pulse width should be between 15-ns and 200-ns. The R_T resistor is always required, whether the oscillator is free running or externally synchronized and SYNC frequency must be equal to or greater than the frequency set by the R_T resistor.

7.3.5 Voltage-Mode Control

The LM5036 device employs voltage-mode control with input voltage feed-forward for the main half-bridge converter. A simplified block diagram of the voltage-mode feedback control loop is shown in 图 13.

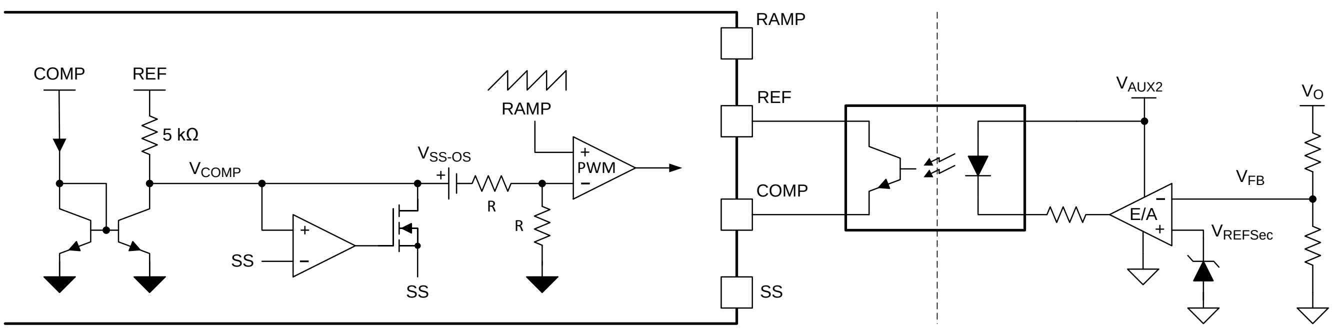


图 13. Voltage-Mode Feedback Control Loop for Half-Bridge Converter

The output voltage (V_O) is sensed and compared against a reference voltage (V_{REFSec}) on the secondary side which produces an error voltage which is then processed by the error amplifier. The compensated error signal is transmitted across the isolation boundary through an opto-coupler and then gets injected into the COMP pin in the form of a control current. The COMP pin current is internally mirrored by a matching pair of NPN transistors which sink current through a 5-kΩ resistor connected to the 5-V internal reference. The resulting control voltage V_{COMP} is compared with the soft-start capacitor voltage (SS) and the smaller of the two passes through an offset $V_{SS\text{-}OS}$ (1-V typical), followed by a 2:1 resistor divider before being applied to the PWM comparator to determine the duty cycle of the half-bridge converter. The PWM comparator polarity is configured such that with no current flowing into the COMP pin, the controller produces maximum duty cycle for the primary FETs.

An opto-coupler detector can be connected between the REF pin and the COMP pin. Because the COMP pin is controlled by a current input, the voltage across the opto-coupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the opto-coupler is thereby greatly reduced. Higher loop bandwidths can be realized because the bandwidth limiting pole associated with the opto-coupler is now at a much higher frequency.

The voltage at the RAMP pin provides the modulation ramp for the PWM comparator. The PWM comparator compares the modulation ramp signal at the RAMP pin to the COMP voltage to control the duty cycle. The modulation ramp signal can be implemented as a ramp proportional to the input voltage, known as feed-forward voltage mode control, as shown in 图 14. The RAMP pin is reset by an internal MOSFET when RAMP voltage passes COMP voltage, current limit event, or at the conclusion of each PWM cycle, whichever comes earlier.

(1) Slope proportional to input voltage (see 图 15)

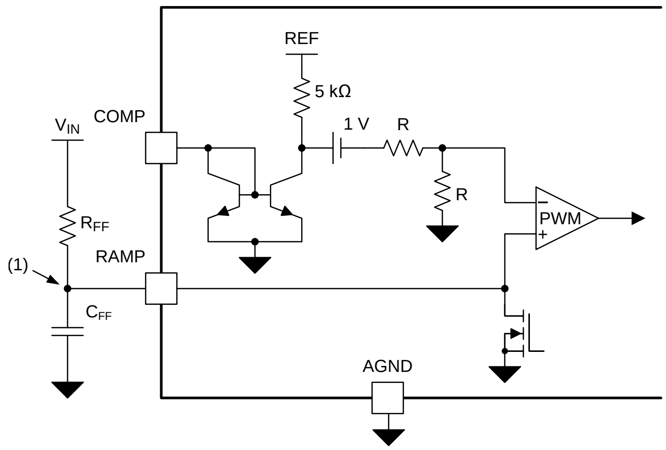


图 14. Feed-Forward Voltage-Mode Control Configuration

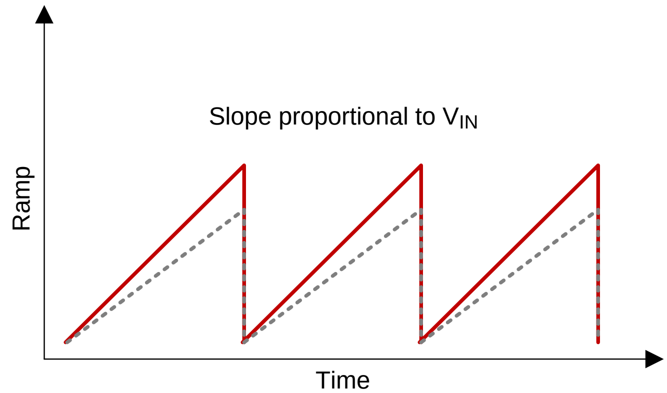


图 15. Modulation Ramp Slope

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins are required to create a saw-tooth modulation ramp signal. The slope of the signal at RAMP will vary in proportion to the input voltage. The varying slope provides line feed-forward information necessary to improve line transient response with voltage-mode control. With a constant control signal, the on-time (t_{ON}) varies inversely with the input voltage (V_{IN}) to stabilize the volt-second product of the transformer. Using a line feed-forward ramp for PWM control requires very little change in the voltage regulation loop to compensate for changes in input voltage, as compared to a ramp with fixed slope. In addition, voltage-mode control is less susceptible to noise. Therefore, it is a good choice for wide input range power converter applications. However, voltage-mode control requires a Type-III compensation network due to the complex-conjugate poles of the L-C output filter.

Assistance with half-bridge voltage control loop design may be obtained using the Power Stage Designer™ tool.

The recommended capacitor value range for C_{FF} is from 100-pF to 1800-pF. Referring to 图 14, it can be seen that C_{FF} value must be small enough to be discharged within the clock pulse-width (t_{CLK}). The value of R_{FF} required can be calculated from 公式 2

$$R_{FF} = \frac{-1}{f_{OSC} \times C_{FF} \times \ln\left(1 - \frac{V_{RAMP}}{V_{IN(min)}}\right)} \tag{2}$$

For example, assuming a V_{RAMP} voltage of 1.5-V (a good compromise of signal range and noise immunity), $V_{IN(min)}$ of 36-V, oscillator frequency of 400-kHz and C_{FF} = 560-pF results in R_{FF} = 105-kΩ.

7.3.6 Primary-Side Gate Driver Outputs (LSG and HSG)

The LM5036 device provides two gate driver outputs for the primary FETs of the main half-bridge converter: one floating high-side gate driver output HSG and one ground referenced low-side gate driver output LSG. Each internal gate driver is capable of sourcing 1.5-A peak and sinking 2-A peak (typical). Initially, the LSG output is turned on during the power transfer phase, followed by a freewheeling period during which both LSG and HSG outputs are turned off. In the subsequent power transfer phase, the HSG output is turned on followed by another freewheeling period.

The low-side LSG gate driver is powered directly by the VCC bias supply. The HSG gate driver is powered from a bootstrap capacitor connected between BST and SW. An external diode connected between VCC and BST provides the high-side gate driver power by charging the bootstrap capacitor from VCC when the switching node SW is low. When the high side FET is turned on, BST rises to a peak voltage equal to VCC + V_{IN}.

The BST and VCC capacitors should be placed close to the pins of the LM5036 device to minimize voltage transients due to parasitic inductance because the peak current source to the MOSFET gates can exceed 1.5-A (typical). The recommended value of the BST capacitor is 0.1-µF or greater. A low ESR/ESL capacitor, such as a surface mount ceramic, should be used to prevent voltage drop during the HSG transitions.

7.3.7 Half-Bridge PWM Scheme

Synchronous rectification on the secondary side of the transformer provides higher efficiency, especially for low output voltage and high output current converter, compared to the diode rectification. The reduction of the diode forward voltage drop (0.5-V to 1.5-V) to 10-mV to 200-mV V_{DS} voltage for a MOSFET significantly reduces rectification losses. In a typical application, the secondary windings of the transformer can be center tapped, with the output power inductor in series with the center tap, as shown in 图 16. The synchronous rectifiers (SRs) provide the ground path for the energized secondary winding and the inductor current.

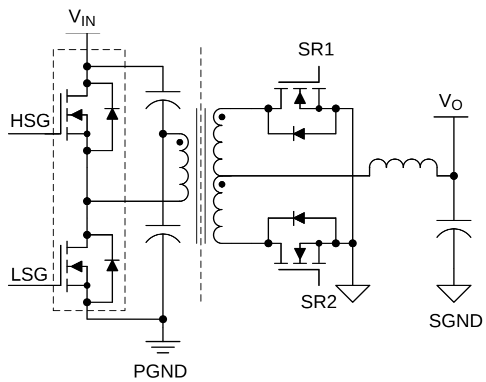


图 16. Half-bridge Topology with Center-Tap Rectification

The internal SR drivers are powered by the REF regulator and each SR output is capable of sourcing 0.1-A and sinking 0.2-A peak (typical). The amplitude of the SR drivers is limited to 5-V. The 5-V SR signals enable the transfer of SR control signals across the isolation barrier either through a digital isolator or isolated gate driver. It should be noted that the actual gate sourcing and sinking currents for the SRs are provided by the secondary-side gate drivers.

The timing diagram of the four PMW signals (LSG, HSG, SR1, and SR2) with dead-times is illustrated in 图 17. The main clock is generated by the internal oscillator. A delayed clock is derived by adding a delay of t_D to the main clock. t_D can be calculated from 公式 3, where RD_1 is the value of the resistor connected between RD1 pin and AGND.

$$t_D = RD_1 \times 2\,pF + 20\,ns \tag{3}$$

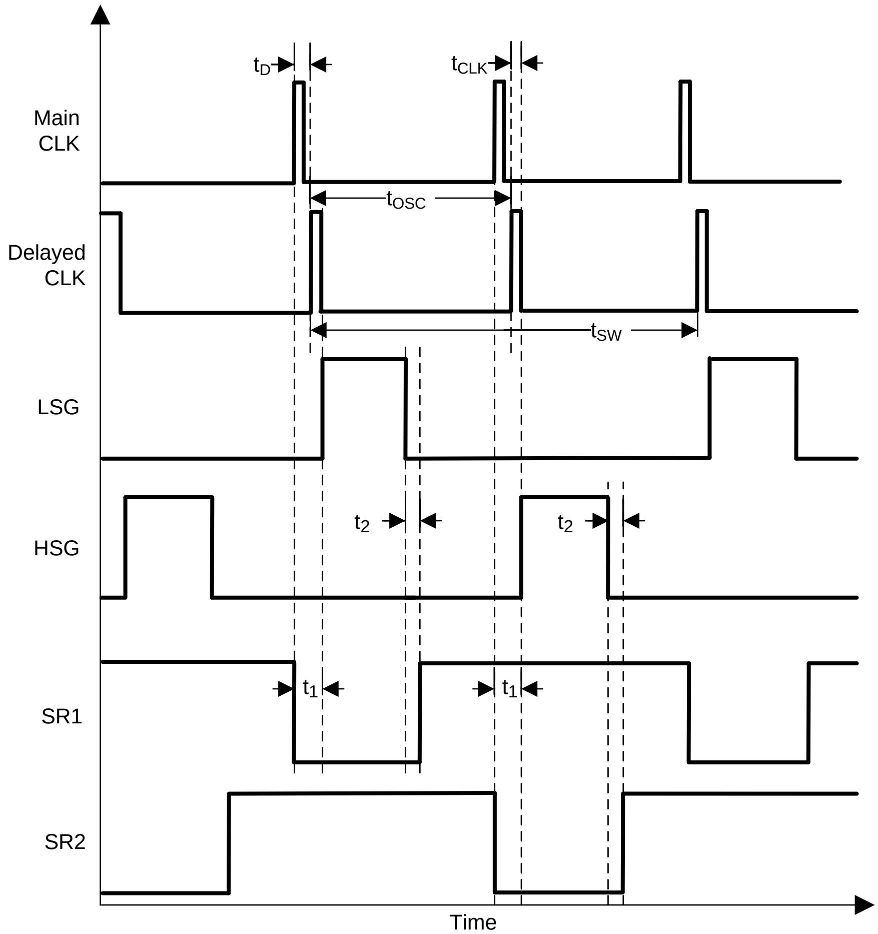


图 17. PWM Signal Timing Diagram

As illustrated in 图 17, the rising edge of the main clock is used to turn off the SRs. Primary FET drive signal LSG/HSG is turned on at the falling edge of the delayed clock. Therefore, the dead-time between the falling edge of SR and the rising edge of the respective primary FET can be calculated from 公式 4

$$t_1 = t_D + t_{CLK}$$

where

- t_{CLK} is the pulse width of the clock which is 65 ns (typical). (4)

The minimum achievable t_1 is dominated by the pulse width of the clock when t_D is set to minimum (30 ns).

After SR1 is turned off, the body diode of SR1 continues to carry about half the inductor current until the primary power raises the drain voltage of the SR1 and reverse biases its body diode. Ideally, dead-time t_1 would be set to the minimum time that allows the SR to turn off before the body diode starts conducting.

Power is transferred from the primary to the secondary side when the LSG is turned on. During this power transfer period, the SR2 is still turned on while the SR1 is turned off. The drain voltage of SR1 is twice the voltage of the center tap at this time. Under the normal operation, the LSG is turned off either when the RAMP signal exceeds the COMP signal or at the rising edge of the next delayed clock signal (maximum duty cycle condition), whichever comes earlier. A dead-time t_2 is inserted between the falling edge of LSG and rising edge of SR1. t_2 can be calculated from 公式 5, where RD_2 is the value of the resistor connected between RD2 pin and AGND.

$$t_2 = RD_2 \times 2\ \text{pF} + 30\ \text{ns} \tag{5}$$

During the dead-time t_2, the inductor current continues to flow through the body diode of SR1. Because the body diode causes more conduction loss than the SR, efficiency can be improved by minimizing the t_2 period while maintaining sufficient margin across the entire operating conditions (component tolerances, input voltages, etc.) to prevent the cross conduction between the primary FET and SR.

During the freewheeling period where both of the primary FETs are turned off while both of the SRs are turned on, the inductor current is almost equally shared between SR1 and SR2 which effectively shorts the secondary winding of the transformer. SR2 is then turned off before HSG is turned on. The power is transferred from the primary to secondary side again when HSG is turned on. After HSG is disabled and the dead-time t_2 expires, SR1 and SR2 both conduct again during the freewheeling period.

Resistor values of no less than 5-kΩ should be connected between the RD1/RD2 pins and AGND

7.3.8 Maximum Duty Cycle Operation

The LSG and HSG will operate at maximum duty cycle when they are turned off at the rising edge of the delayed clock, instead of by the event where RAMP voltage passes COMP voltage, as shown in 图 18. In LM5036 device, it is intended to achieve optimized maximum duty cycle for the primary FETs in order to accommodate wider range of operation.

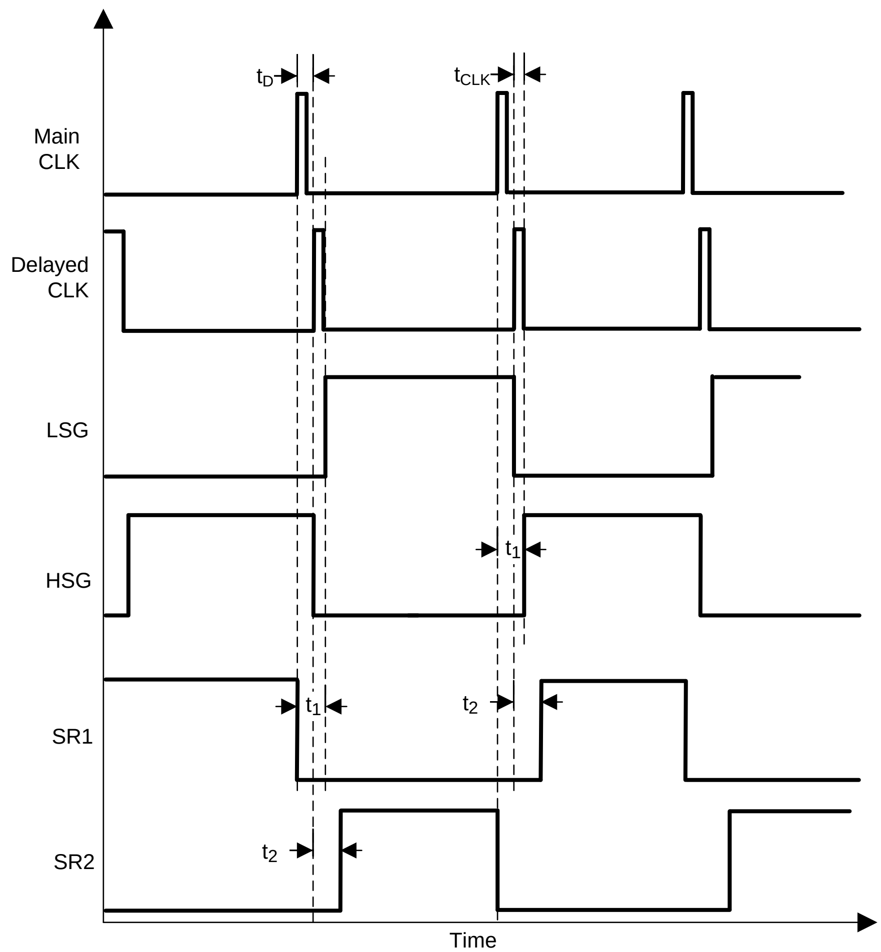


图 18. PWM Signals at Maximum Duty Cycle Condition

Use 公式 6 to calculate the maximum duty cycle for the primary FETs

$$D_{MAX} = \frac{\frac{1}{f_{OSC}} - t_{CLK}}{\frac{2}{f_{OSC}}}$$

where

- f_{OSC} is the oscillator frequency which is twice the switching frequency (6)

The pulse width of the clock is used in this case to prevent cross-conduction between the two primary FETs during the maximum duty cycle operation.

7.3.9 Pre-Biased Start-Up Process

The soft-start functionality limits the inrush current and voltage stress of the power converter. A common requirement for the power converters used in the telecom/datacom applications is to have a monotonic output voltage start-up into pre-biased load conditions where the output capacitor is pre-charged prior to start-up. In a pre-biased load condition, if the synchronous rectifiers are engaged prematurely they will sink current from the pre-charged output capacitors resulting in undesired output voltage dip or even power converter damage. The LM5036 device implements unique circuitry to ensure intelligent turn-on of the synchronous rectifiers such that the output voltage has monotonic start-up.

The start-up process can be divided into two phases:

- soft-start of the primary FETs
- soft-start of the SRs

The pre-biased start-up process is handled automatically by LM5036. The user need only select values for C_{SS}, C_{SSSR}, and the ramp rate of the secondary reference (V_{REFSec}) soft-start 图 19. The circuit of 图 19 uses a comparator to, detect the voltage change of V_{AUX2} and, release the FET shorting across the secondary soft-start capacitor (C_{SSSec}). This comparator circuit may also be replaced by the transistor based circuit of Figure 41.

7.3.9.1 Primary FETs Soft-Start Process

图 19 shows a simplified block diagram of the soft-start function.

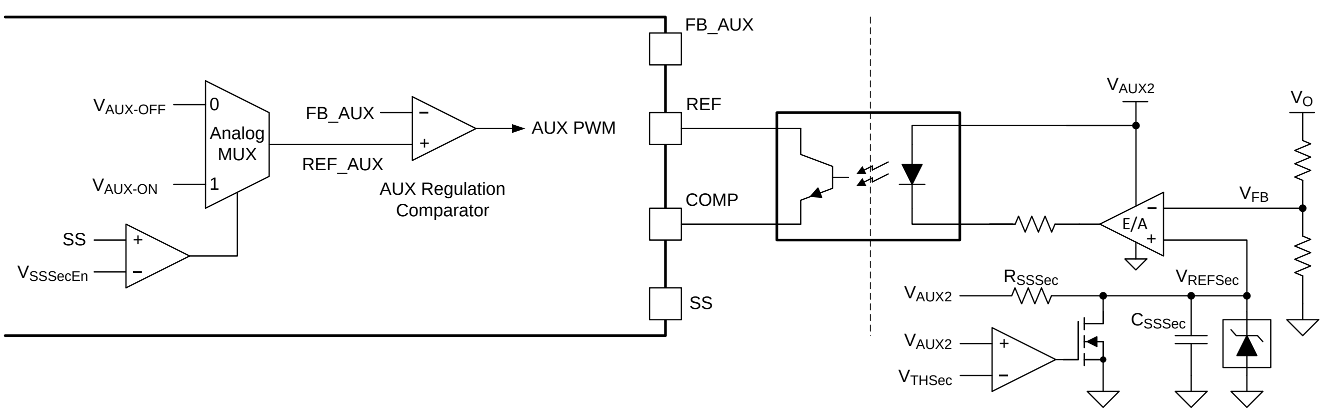


图 19. Soft-Start Function

The auxiliary supply has two reference output voltage levels of $V_{AUX\text{-}OFF}$ (1.4 -V typical, off state) and $V_{AUX\text{-}ON}$ (1-V typical, on state) which facilitates easy voltage level shift detection on the secondary side. The auxiliary supply starts to operate as soon as V_{IN} > V_{AUX_UVLO} (15-V typical) and VCC and REF are above the respective UV thresholds. When the soft-start capacitor is below $V_{SSSecEn}$ (2.06-V typical), the auxiliary supply will produce the off-state voltage on the primary ($V_{AUX1\text{-}OFF}$) and secondary side ($V_{AUX2\text{-}OFF}$), as shown in 图 20.

The off-state auxiliary output voltage level present on the secondary side $V_{AUX2\text{-}OFF}$ is above the threshold V_{THSec}, which activates a reset circuit that discharges the output voltage reference V_{REFSec}. This ensures that the opto-coupler is producing a 0% duty-cycle command. When UVLO exceeds V_{UVLO} (1.25-V typical) and VCC and REF are above the respective UV thresholds, the soft-start capacitor starts to charge. The auxiliary supply will produce the on-state voltage level when the soft-start capacitor reaches $V_{SSSecEn}$.

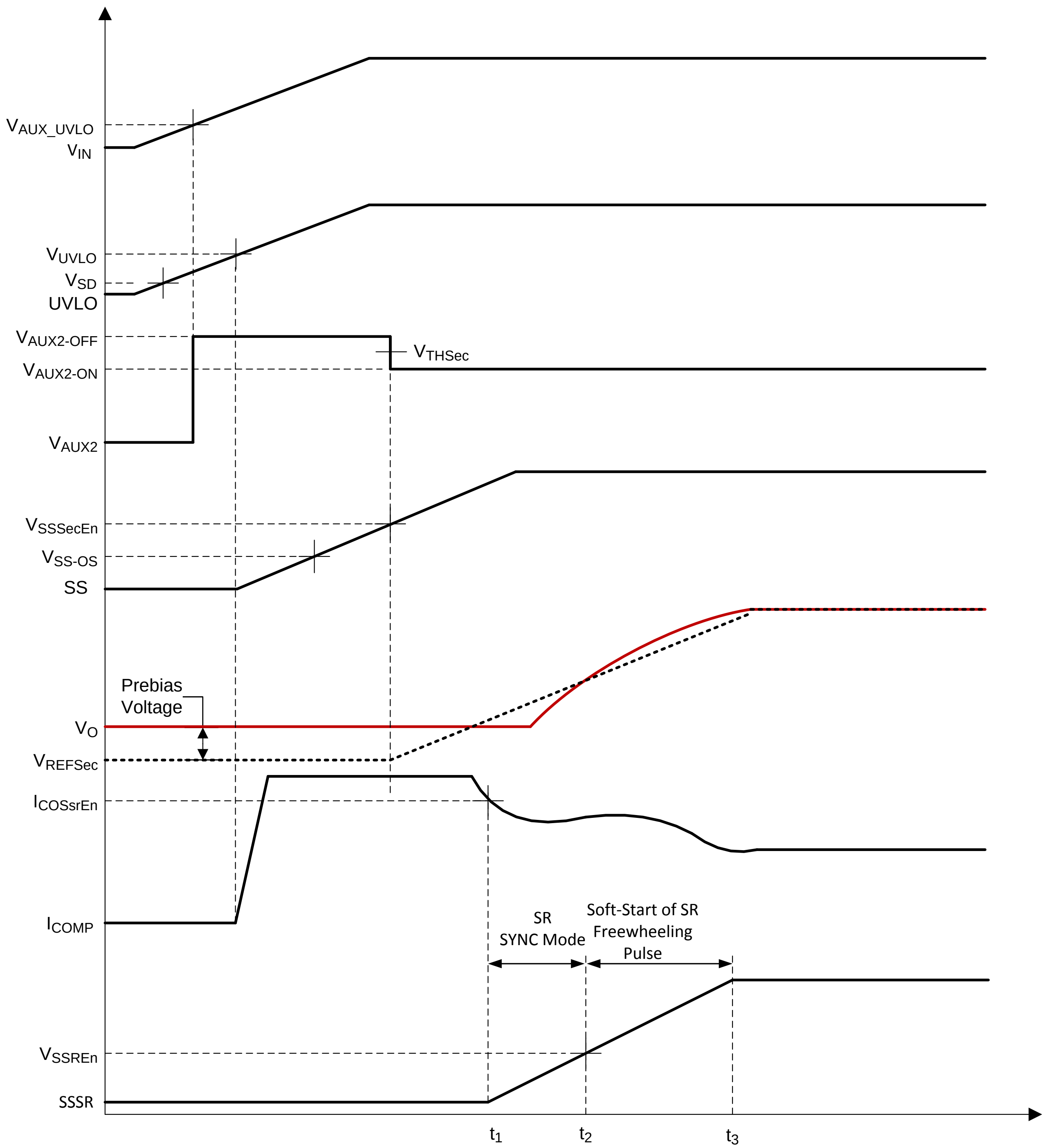


图 20. Pre-biased Start-Up Waveform

The secondary side reset circuit will now be disabled because $V_{AUX2\text{-}ON} < V_{THSec}$, and the output voltage reference is released. The reference capacitor soft-starts the output voltage under full regulation. By modulation of the auxiliary output voltage, the communication between the primary and secondary side is established without the need of any additional opto-coupler.

Due to the introduced programmable soft-start delay (before SS capacitor reaches $V_{SSSecEn}$), the duty cycle is controlled by the feedback control loop at all times without being interfered by the SS capacitor voltage (because $V_{COMP} < V_{SS}$). When the reference voltage exceeds the pre-bias voltage at the output, the I_{COMP} starts to fall as the secondary side error amplifier demands increased power. As I_{COMP} falls the internal V_{COMP} voltage will rise and when it exceeds $V_{SS\text{-}OS}$, which corresponds to zero duty cycle, the duty cycle of the primary FETs starts to increase. Once the I_{COMP} current falls below $I_{COSsrEn}$ the device starts to charge SSSR capacitor with current I_{SSSR} (20-µA typical).

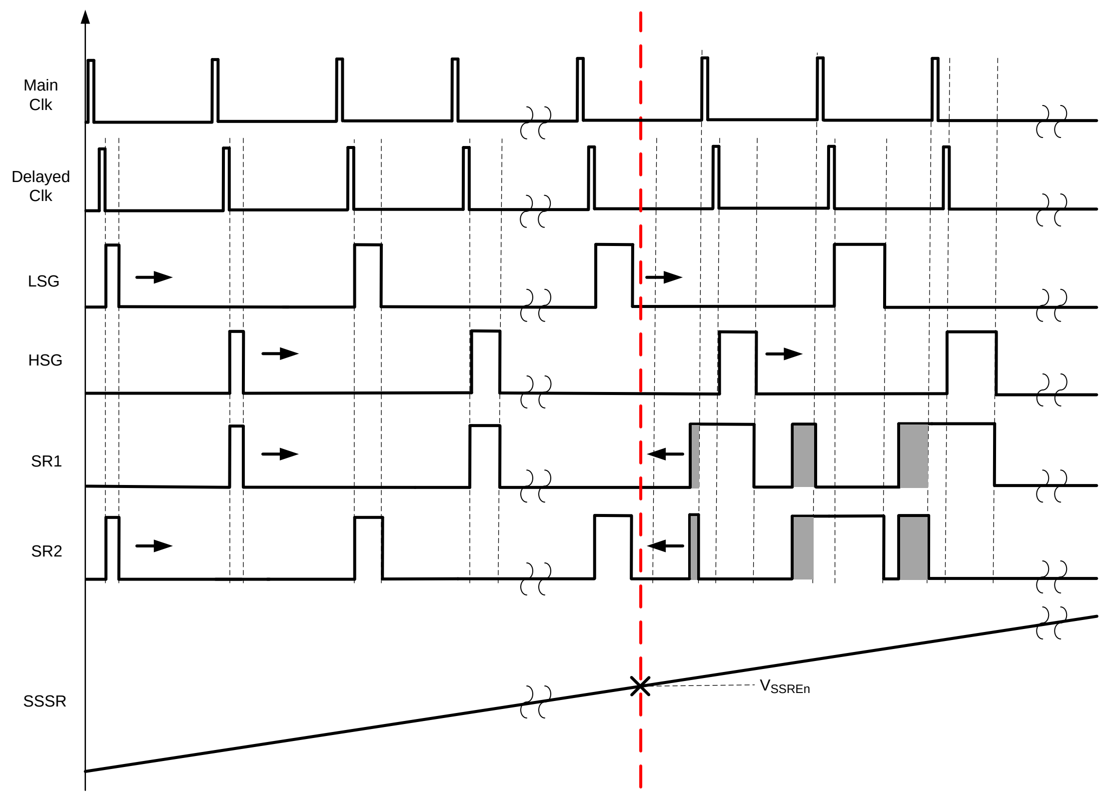


图 21. PWM Timing During Startup Process

7.3.9.2 Synchronous Rectifier (SR) Soft-Start Process

Until SSSR capacitor reaches V_{SSREn} (1-V typical), the controller operates at SR synchronization (SYNC) mode where the SR pulses are synchronized to the respective primary FET pulses, as shown in 图 21. This helps to reduce the conduction loss of the SRs. In addition, due to the fact that the SRs only conduct during power transfer phase, there is no risk of reverse current in SYNC mode. Since the pulse width of SRs gradually increases, the output voltage disturbance due to the difference in the voltage drop between the body diode and the on resistance of the SRs is prevented.

Once the SSSR capacitor crosses the V_{SSREn}, the LM5036 device begins the soft-start of the SRs freewheeling period (highlighted in gray in 图 21) where the SRs may sink current from the output if they are engaged prematurely. The V_{SSREn} offset on the SSSR pin is intended to provide additional delay which ensures that the primary duty cycle ramps up to a point where the output voltage is in-regulation, thereby avoiding reverse current when the SRs are engaged. The SR soft-start follows a leading-edge modulation technique such that the leading-edge of the SR pulse is soft-started as opposed to the trailing-edge modulation of the primary FETs. As shown in 图 21, SR1 and SR2 are turned on simultaneously with a narrow pulse-width during the freewheeling period. At the end of the freewheel period, that is, at the rising edge of the main CLK, the SR in phase with the next power transfer cycle remains on while the SR out of phase with it is turned off. The in-phase SR remains on throughout the power transfer cycle and at the end of it, both the primary FET and the in-phase SR are turned off simultaneously. At the end of the soft-start, the SR pulses will become complementary to the respective primary FETs, as shown in 图 17.

7.3.10 Zero Duty Cycle Operation

The zero duty cycle detection ensures that there is no excessive reverse current when the primary duty cycle is zero. In that case, the SSSR capacitor would be clamped to ground and therefore SRs will be turned off (SR SYNC mode). Normal operation will resume (SSSR capacitor start to charge) as soon as the load is applied. It should be noted about a special application scenario where there is a low output capacitance value. During the start-up under no load condition, the output capacitor acts like a load. With small output capacitor the converter might get stuck in zero duty until load is applied.

7.3.11 Enhanced Cycle-by-Cycle Current Limiting with Pulse Matching

图 22 illustrates the half-bridge converter with low-side current sensing using a sense resistor.

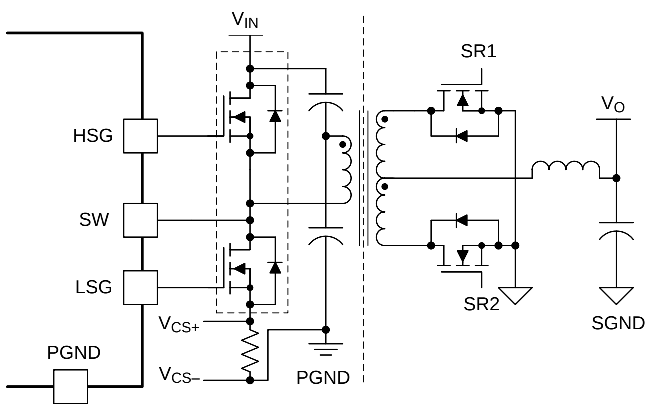


图 22. Half-Bridge Converter with Low-Side Current Sensing

In LM5036 device, current limiting for the half-bridge converter is accomplished with three pins, including CS_SET, CS_POS and CS_ NEG pins, as shown in 图 23. The current sense circuit limits positive current flowing from input to output and also negative current flowing from output to input. An input voltage compensation function helps to minimize the variation of effective output current limit across the range of input voltage. A pulse matching function is automatically implemented when the peak current limit circuit is active. This function matches the pulse width on the high and low primary FETs to maintain voltage balance of the half-bridge capacitor divider. This method ensures flux balance of the transformer during peak current limit operation.

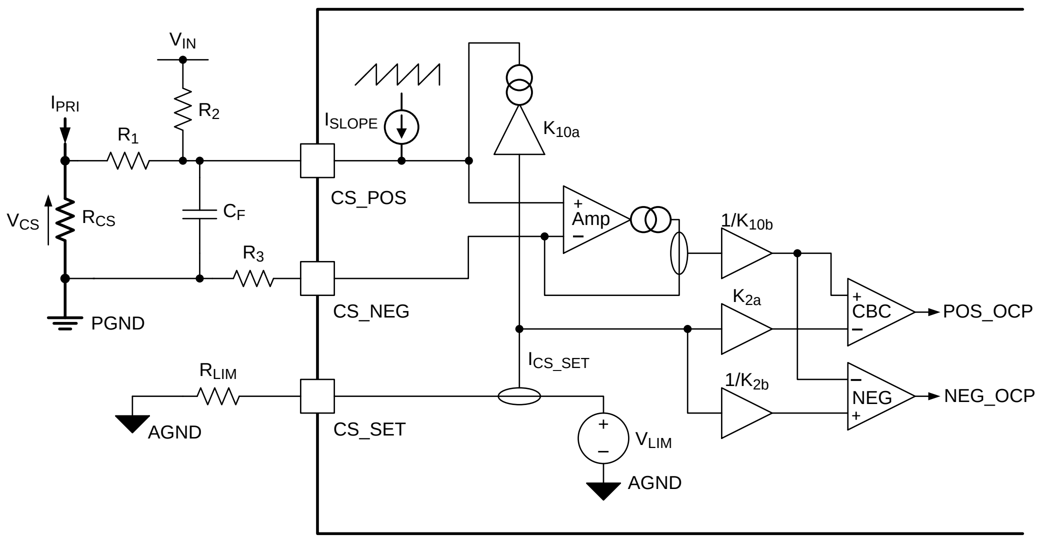


图 23. Block Diagram of the Current Limiting Function

CS_SET pin is used to set the internal current limit threshold with an external resistor R_{LIM} according to 公式 7.

$$I_{CS\_SET} = \frac{V_{LIM}}{R_{LIM}}$$

where

- V_{LIM} (0.75-V typical) is the internal current limit setting voltage. (7)

The CS_POS pin is driven by a signal representative of the current flowing through the low-side FET of the half-bridge converter. The current sense voltage at CS_POS pin (equal to CS_NEG pin voltage) is converted to a current sense signal through R_3 which is then sensed, scaled and compared against the internal current limit thresholds. In order to blank the leading-edge transient noise seen when the low-side FET is turned on, the current sense signal is blanked for t_{CSBLK} after LSG is turned on. If the magnitude of the noise spike is excessive, an additional filter capacitor C_F may be added to form an RC filter with R_1 to reduce the high-frequency noise spike. Both the leading-edge blanking and RC filter help to prevent false triggering of CBC current limiting operation.

In order to achieve bi-directional current sensing, an internal offset current (K_{10a} x I_{CS_SET}), is injected to the CS_POS pin. This offset allows positive internal thresholds on the CBC and NEG comparators that correspond to effective I_{CS_SET} and -I_{CS_SET} / 2 thresholds at the input.

When the current sense signal (I_{R3} x 1 / K_{10b}) reaches the positive threshold (K_{2a} x I_{CS_SET}), CBC current limiting operation is activated. The controller essentially operates in peak current mode control, with the voltage loop open, during the CBC operation. A common issue with peak current mode control is sub-harmonic oscillation. This occurs when the effective duty cycle is greater than 50%. A common solution for sub-harmonic oscillation is to add slope compensation. The slope of the compensation ramp must be set to at least one half the downslope of the output inductor current transformed to the primary side across the current sense resistor. To eliminate sub-harmonic oscillation after one switching cycle, the slope compensation must be equal to the downslope of the output inductor current. This is known as deadbeat control. In LM5036, the slope compensation signal is a saw-tooth current signal ramping up from 0 to I_{SLOPE} at the oscillator frequency (twice the switching frequency of each primary FET).

However, another issue will arise after slope compensation is added. The current limit level varies with the input voltage, as illustrated in 图 24. Because the slope compensation magnitude is different at different input voltages, the actual current limit level varies with input voltage for a given internal current limit threshold.

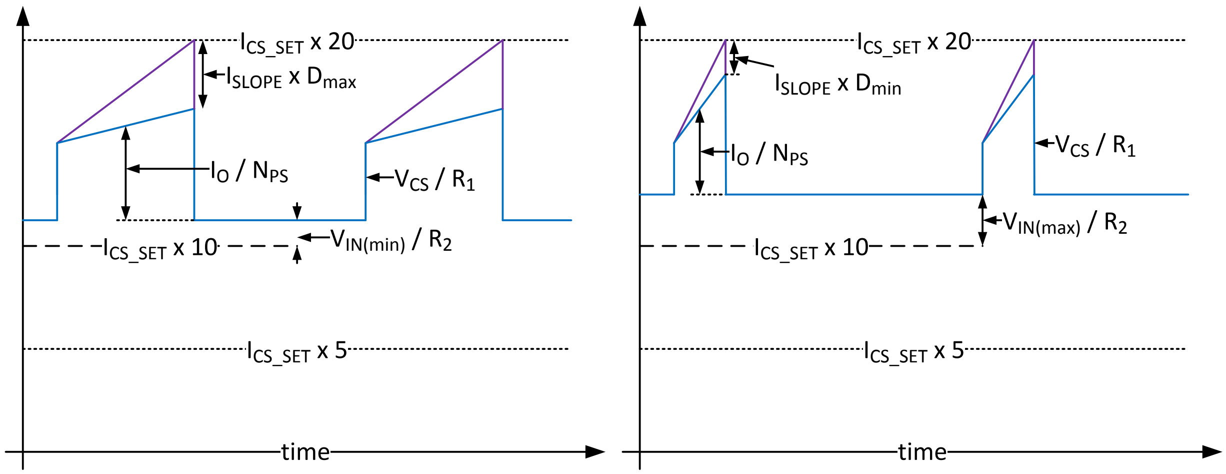


图 24. Current Sense and Current Limit Waveforms

A new feature, input voltage compensation, is provided by LM5036. By adding an extra signal, which is a function of input voltage, on top of the current sense signal and the slope compensation signal, variation of the current limit level can be minimized over the entire input voltage range. The CS_POS pin voltage at time t, after the rising edge of LSG, is expressed by 公式 8:

$$v_{CS\_POS}(t) = v_{CS}(t) + R_1 \times \left(I_{CS\_SET} \times K_{10a} + \frac{V_{IN} - v_{CS\_POS}(t)}{R_2} + I_{SLOPE} \times t \times f_{OSC} \right) \tag{8}$$

$$v_{CS\_POS}(t) = \frac{v_{CS}(t) + R_1 \times \left(I_{CS\_SET} \times K_{10a} + \frac{V_{IN}}{R_2} + I_{SLOPE} \times t \times f_{OSC} \right)}{1 + \frac{R_1}{R_2}} \tag{9}$$

At the trip threshold, of the CBC comparator, both its inputs are at the same potential. In this case the voltage on the CS_NEG pin is expressed by 公式 10.

$$v_{CS\_NEG} = I_{CS\_SET} \times K_{2a} \times K_{10b} \times R_3 \tag{10}$$

$$v_{CS\_POS}(t) = v_{CS\_NEG} \tag{11}$$

For a given duty cycle (D) the current sense threshold voltage that will just trigger the CBC comparator can be determined by combining 公式 9, 公式 10 and 公式 11.

$$v_{CS\_CBCTh} = R_1 \times \left(I_{CS\_SET} \times \left(K_{2a} \times K_{10b} \times R_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - K_{10a} \right) - \frac{V_{IN}}{R_2} - I_{SLOPE} \times D \right) \tag{12}$$

Now if we assume:

$$\frac{1}{R_3}=\frac{1}{R_1}+\frac{1}{R_2}$$
$$K_{10a}=K_{10b}=10$$
$$K_{2a}=2$$
$$D=t_{ON}\times f_{OSC}=\frac{2\times V_O}{V_{IN}}\times N_{PS}$$
$$N_{PS}=\frac{N_P}{N_S} \tag{13}$$

公式 12 simplifies to 公式 14.

$$v_{CS\_CBCTh}=R_1\times\left(\frac{K_{CBC1}}{R_{LIM}}-\frac{V_{IN}}{R_2}-I_{SLOPE}\times\frac{2\times V_O}{V_{IN}}\times N_{PS}\right)$$
Where
$$K_{CBC1}=V_{LIM}\times\left(K_{2a}\times K_{10b}-K_{10a}\right) \tag{14}$$

Current Limit gives an example design process for calculating the CBC external resistor values. The Excel Calculator Tool can also be used to assist in the process of selecting these resistor values.

LM5036 ensures flux balance of the main transformer during CBC operation. The duty cycles of the two primary FETs are always matched. If the low-side FET is terminated due to a current limit event, a matched duty cycle will be applied to the high-side FET during the next half switching period, regardless of the current condition. The matched duty cycles ensure voltage-second balance of the transformer which prevents transformer saturation.

The pulse matching operation is illustrated in 图 25. When the current limit is reached during the low-side phase, a FLAG signal goes high. The RAMP signal is sampled at the rising edge of the FLAG signal and then held through the next half switching period for the high-side phase. When the high-side phase RAMP signal rises above the sampled value, the high-side PWM pulse is turned off so that the duty cycle are matched for both phases. In the meantime, the hiccup restart capacitor is charged with a current source $I_{RES\text{-}SRC1}$ (15-µA typical) during CBC operation. The pulse matching feature is handled automatically by the LM5036 controller and requires no action from the designer.

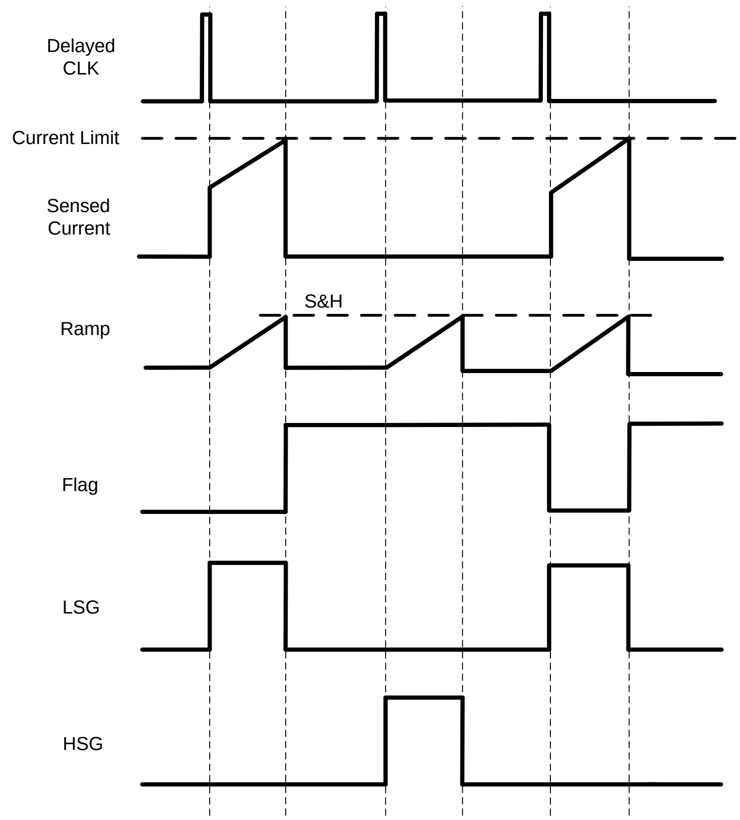


图 25. Pulse Matching Operation

7.3.12 Reverse Current Protection

In addition to the CBC current limit, a negative current limit, which is set to be half of the positive current limit as shown in 图 26. This is used to prevent excessive reverse current which could cause significant output voltage dip and potentially damage the power converter. When the negative current limit is exceeded twice, the SSSR capacitor will be clamped to ground so the controller enters the SR SYNC mode where the SR pulses are synchronized to the respective primary FET pulses. Therefore, the SR freewheeling pulses are turned off. The negative current limit event counter will be reset if the number of negative current limit events detected within four switching periods is less than two.

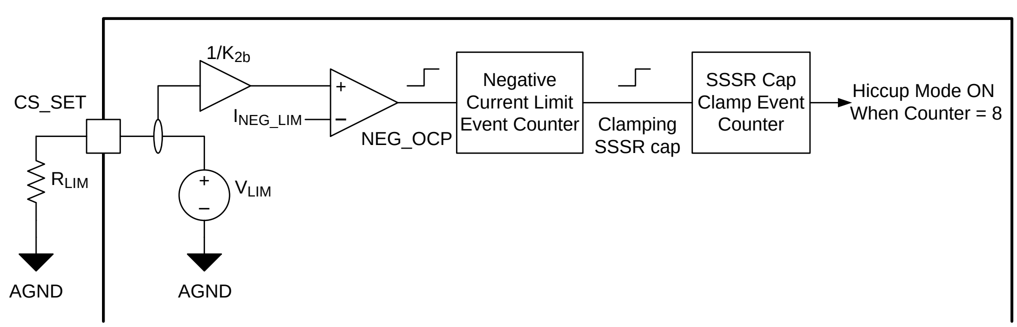


图 26. Reverse Current Protection Circuit

At the trip threshold of the NEG comparator both inputs are at the same potential. In this case the voltage on the CS_NEG pin is expressed by 公式 15.

$$V_{CS\_NEG} = I_{CS\_SET} \times \frac{1}{K_{2b}} \times K_{10b} \times R_3 \tag{15}$$

The voltage across the CS resistor at the trip threshold of the NEG comparator can therefore be determined by combining 公式 9, 公式 11 and 公式 15.

$$V_{CS\_NEGTh} = R_1 \times \left(\frac{K_{CBC2}}{R_{LIM}} - \frac{V_{IN}}{R_2} - I_{SLOPE} \times t_{CSBLK} \times f_{osc} \right)$$

Where:

$$K_{2b} = 2$$

$$K_{CBC2} = V_{LIM} \times \left(\frac{1}{K_{2b}} \times K_{10b} - K_{10a} \right) \tag{16}$$

Notice that the inductor current has its most negative value at the start of the LSG on period. The NEG comparator trip will occur immediately after the blanking period (t_{CSBLK}) has expired.

The Excel Calculator Tool predicts both the positive and negative output current limit levels as a function of input voltage for a given set of resistor values.

7.3.13 CBC Threshold Accuracy

The CBC current limit amplifier deployed within LM5036 is a precise component. In common with all such devices the input bias currents and input offset voltage will lead to small variations in the current trip threshold between parts and across temperature.

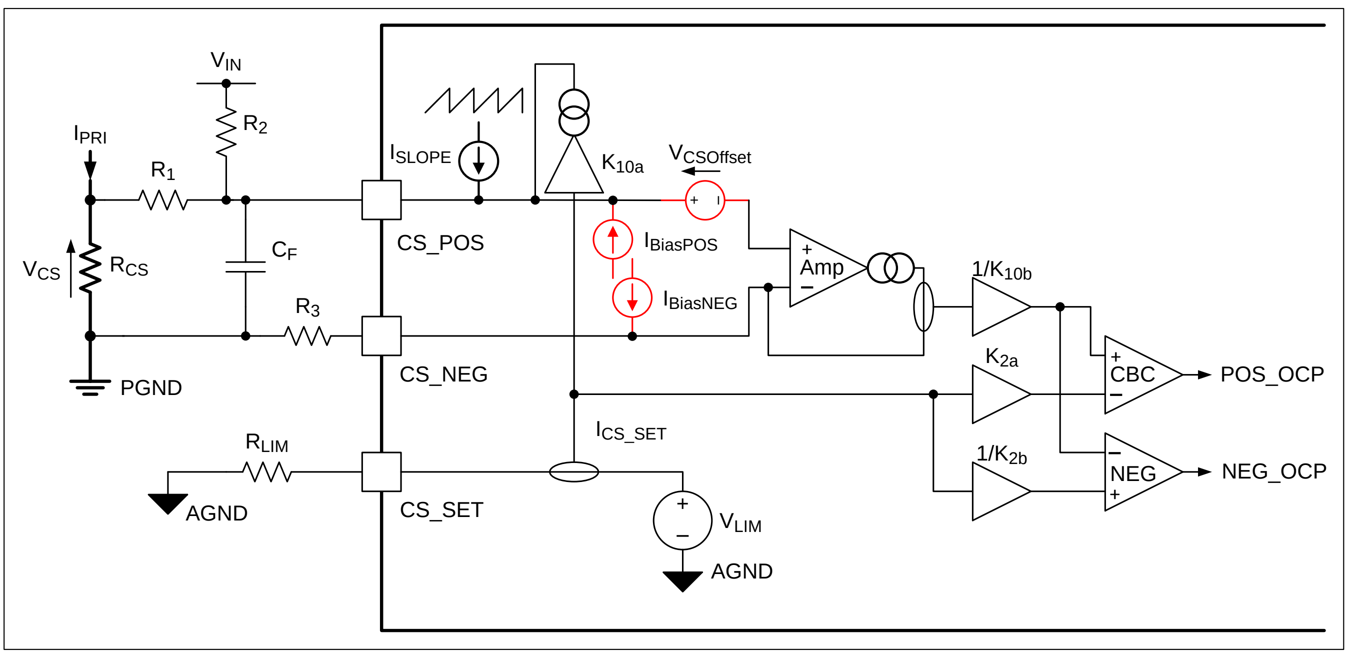


图 27. Diagram of Current Limiting Function with Error Terms Shown in Red

At its trip threshold the two inputs of the CBC comparator must be equal. At this condition the voltage on the CS_NEG pin is given by 公式 17.

$$V_{CS\_NEG} = \left(\frac{V_{LIM}}{R_{LIM}} \times K_{2a} \times K_{10b} + I_{BiasNEG} \right) \times R_3 \tag{17}$$

The voltage drop across the ideal amplifier input must be zero. The voltage of the CS_POS pin, at the trip threshold can be expressed as follows:

$$V_{CS\_POS} = V_{CS\_NEG} + V_{CSOffset} \tag{18}$$

$$v_{CS\_POS} = v_{CS\_CBCTh} + \left(\frac{V_{LIM}}{R_{LIM}} \times K_{10a} + I_{BiasPOS} + D \times I_{SLOPE} + \frac{V_{IN} - v_{CS\_POS}}{R_2} \right) \times R_1 \quad (19)$$

Combining 公式 17, 公式 18 and 公式 19 and re-arranging gives an expression for the voltage across the current sense resistor at the trip threshold 公式 20.

$$v_{CS\_CBCTh} = R_1 \times \left(\frac{K_{CBC1}}{R_{LIM}} - I_{BiasOffset} + \frac{v_{CSOffset}}{R_3} - D \times I_{SLOPE} - \frac{V_{IN}}{R_2} \right)$$

Where:

$$I_{BiasOffset} = I_{BiasPOS} - I_{BiasNEG} \quad (20)$$

Hence, for a given set of external component values, the variation in current trip threshold across parts and temperature can be found using data supplied in the Electrical Tables.

A short delay will exist (t_{CSLSG}), after the CBC comparator inputs reach their trip threshold, before the LSG falling edge. During this delay the primary current will continue to ramp, giving rise to a further error in the apparent trip threshold. The peak primary current flowing when the low side MOSFET switches OFF (I_{PriCBC}), is expressed by 公式 21.

$$I_{PriCBC} = \frac{V_{CS\_CBCTh}}{R_{CS}} + t_{CSLSG} \times \left(\frac{1}{2} \times \left(\frac{V_{IN}}{L_{Mag}} + \frac{V_{IN}}{L_O \times N_{PS}^2} \right) - \frac{V_O}{L_O \times N_{PS}} \right) \quad (21)$$

The output current at which the primary peak current threshold is reached is expressed by 公式 22.

$$I_{LIM} = N_{PS} \times \left[I_{PriCBC} - \frac{\Delta I_{LO}}{N_{PS}} - \Delta I_{LMag} \right] \quad (22)$$

ΔI_{LO} is the amplitude of ripple current in the output inductor and is expressed in 公式 23.

$$\Delta I_{LO} = \frac{V_O \times (1-D)}{2 \times L_O \times f_{OSC}} \quad (23)$$

ΔI_{LMag} is the amplitude of ripple current in the magnetising inductor and is expressed in 公式 24.

$$\Delta I_{LMag} = \frac{V_{IN}}{2} \times \frac{D}{2 \times L_{Mag} \times f_{OSC}} = \frac{N_{PS} \times V_O}{2 \times L_{Mag} \times f_{OSC}} \quad (24)$$

Combining 公式 22, 公式 23 and 公式 24 gives an expression for output current limit as a function of primary current limit threshold 公式 25.

$$I_{LIM} = N_{PS} \times \left[I_{PriCBC} - \frac{V_O \times (1-D)}{2 \times L_O \times f_{OSC} \times N_{PS}} - \frac{V_O \times N_{PS}}{2 \times L_{Mag} \times f_{OSC}} \right] \quad (25)$$

The Excel Calculator Tool can be used to evaluate the tolerance of output current limit.

7.3.14 Hiccup Mode Protection

A block diagram of the hiccup mode function is shown in 图 28. Both the repetitive CBC and negative current limit events will trigger hiccup mode operation in LM5036 device.

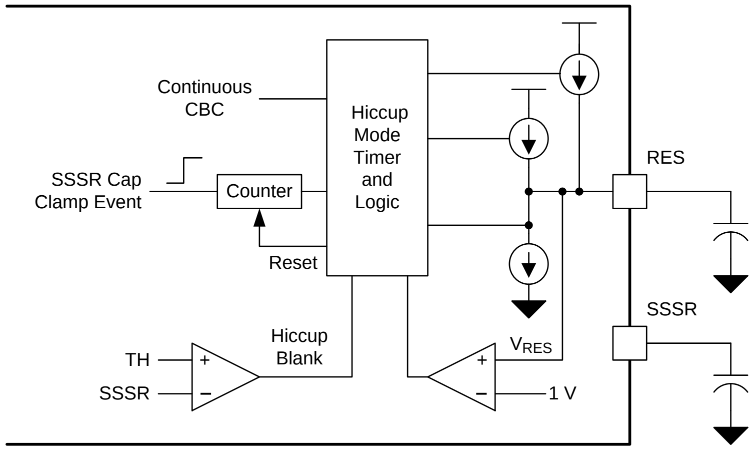


图 28. Hiccup Mode Circuitry

The device charges the hiccup restart capacitor with a current source $I_{RES\text{-}SRC1}$ (15-µA typical) during CBC operation. The hiccup mode is activated when V_{RES} exceeds 1 V. During hiccup mode operation, the SS and SSSR capacitors are fully discharged and the half-bridge converter remains off for a period of time (t_{HIC}) before a new soft-start sequence is initiated.

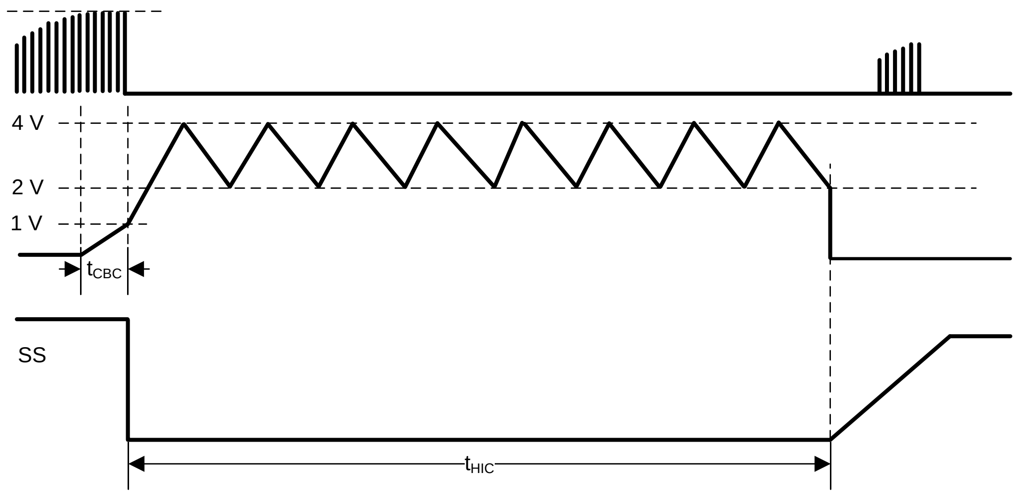


图 29. Hiccup Mode Activated By Continuous CBC Operation

Use 公式 26 to calculate the duration of CBC operation before entering the hiccup mode.

$$t_{CBC} = \frac{C_{RES} \times 1\,V}{I_{RES-SRC1}} \tag{26}$$

where

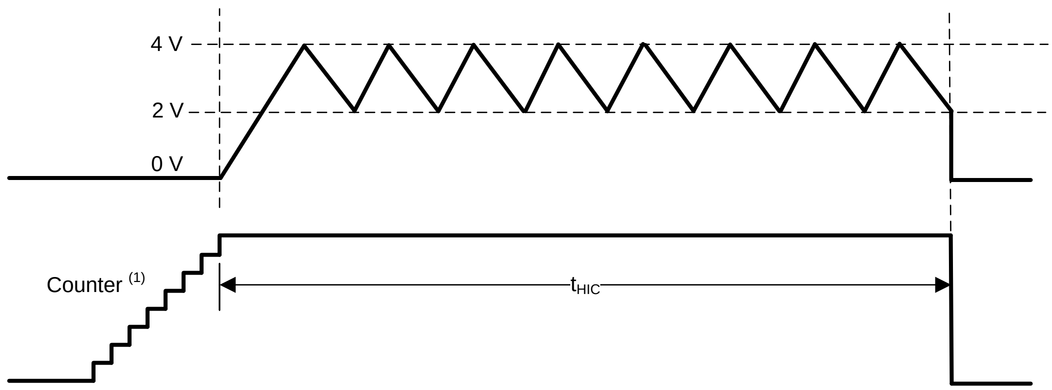
- C_{RES} is the value of the hiccup capacitor

After the RES pin reaches 1.0-V, current source $I_{RES\text{-}SRC1}$ (15-µA typical) is turned off and current source $I_{RES\text{-}SRC2}$ (30-µA typical) is turned on which charges the RES capacitor to 4-V. Then current source $I_{RES\text{-}DIS2}$ (5-µA typical) is enabled which discharges the RES capacitor to 2-V.

Use 公式 27 to calculate the hiccup mode off-time.

$$t_{HIC} = \frac{C_{RES} \times 2\,V \times 8}{I_{RES-DIS2}} + \frac{C_{RES} \times \left(2\,V \times 8 + 1\,V\right)}{I_{RES-SRC2}} \tag{27}$$

In addition to the repetitive CBC current limit condition, the device also enters hiccup mode if the SSSR capacitor is clamped for eight times due to repetitive negative current limit condition. The operating pattern of the hiccup mode activated by the negative current limit is similar to that activated by CBC current limit. The only difference is that at the beginning of the hiccup mode operation the RES capacitor is charged with current source $I_{RES\text{-}SRC2}$ when activated by negative current limit as illustrated in 图 30 whereas the RES capacitor is charged with current source $I_{RES\text{-}SRC1}$ when activated by CBC current limit condition.



(1) SSSR capacitor clamp event counter

图 30. Hiccup Mode Activated By Repetitive Negative OCP Condition

Once the hiccup off-timer expires, the SSSR capacitor clamp event counter will be reset. If SSSR capacitor gets clamped for less than eight times before the SSSR capacitor voltage is fully ramped up to its maximum value, the SSSR capacitor clamp event counter will also be reset. This is because the fact that SSSR capacitor voltage is able to fully ramp up to its maximum value indicates that repetitive negative current limit condition no longer exists.

7.3.15 Hiccup Mode Blanking

In some application scenarios such as high output capacitance and/or heavy load, there can be excessive inrush current during the start-up process. This would trigger CBC current limit which in turn activates the hiccup mode operation, thereby causing the converter to keep attempting to restart. In LM5036 device, a hiccup mode blanking circuitry is implemented to disable the hiccup mode operation during the start-up. The hiccup capacitor is clamped to ground until the SSSR capacitor voltage rises above the hiccup blank threshold $V_{HC\_BLK\_TH}$ (5.5-V typical).

7.3.16 Over-Temperature Protection (OTP)

Two-level internal thermal shutdown circuitry is implemented in LM5036 device to protect the integrated circuit should its maximum rated junction temperature be exceeded. When the internal temperature is above the lower-level threshold of 150°C, the half-bridge converter is turned off and thereby the SS and SSSR capacitors are fully discharged.

Typically, the internal temperature should drop after the main half-bridge converter is turned off. However, if the temperature continues to rise above the higher-level threshold of 160°C, the auxiliary supply will be disabled in order to prevent the device from catastrophic failure due to accidental device overheating . Note that the internal VCC and REF bias regulators still remain active during thermal shutdown to provide the bias power for the external house-keeping circuitry.

7.3.17 Over-Voltage / Latch (ON_OFF Pin)

The ON_OFF pin can be configured as a latch pin or OVP pin. In the latch configuration, the half-bridge converter remains off even after the faults are cleared. A new soft-start sequence will not be initiated until the latch is reset. One latch configuration is illustrated in 图 31 where a large latch resistor R_L (for example, 50 kΩ) and a diode are tied to the ON_OFF pin.

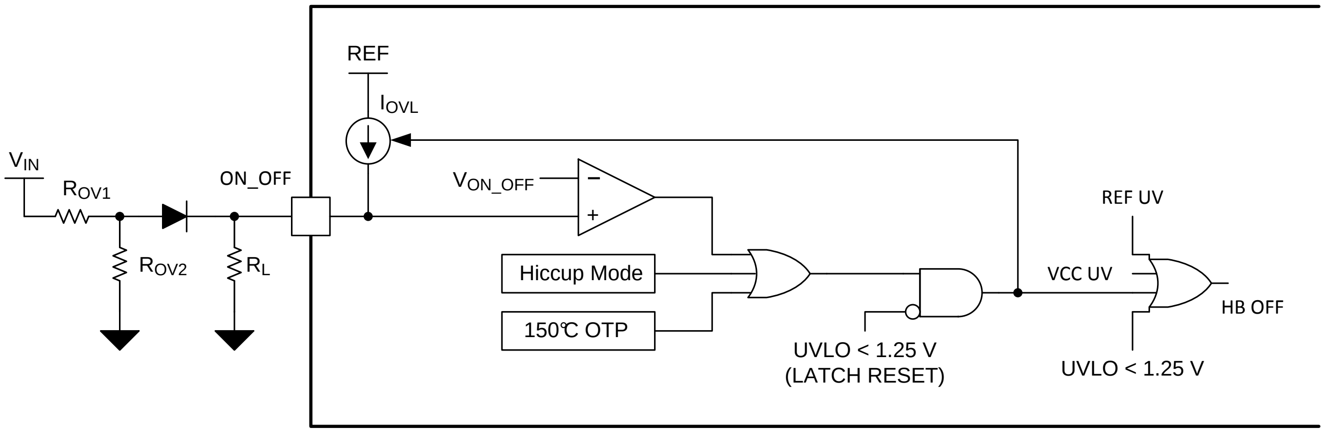


图 31. ON/OFF Pin Latch Function

When any of the faults is detected including OVP, hiccup mode OCP and 150 ºC OTP, the ON_OFF pin current source, I_{OVL} (50-µA typical), is activated, that raises the ON_OFF pin voltage quickly. As a result, the latch diode is reverse biased. The current source I_{OVL} remains active even if the fault is cleared because the ON_OFF pin voltage is latched above V_{ON_OFF} (1.25-V typical). To reset the latch operation, simply pulling down the UVLO pin voltage below V_{ON_OFF} disables the current source and thus the ON_OFF pin voltage falls quickly. A new soft-start sequence will be initiated as soon as the latch is reset and the faults are cleared.

Use 公式 28 to design the external voltage divider in latch mode.

$$V_{IN\_L} = \left(\frac{V_{ON\_OFF} + V_F}{R_{OV2}} + \frac{V_{ON\_OFF}}{R_L} \right) \times R_{OV1} + V_{ON\_OFF} + V_F$$

where

- V_F is the forward voltage drop of the latch diode
- V_{IN_L} is the desired input voltage latch threshold, and R_L is the latch resistor. (28)

Note that the current source I_{OVL} does not provide any hysteresis when ON_OFF pin is configured in latch mode.

The ON_OFF pin can also be configured as an OVP pin as shown in 图 32. In this configuration, the external voltage divider should be designed such that the ON_OFF pin voltage is greater than V_{ON_OFF} when an over-voltage condition occurs.

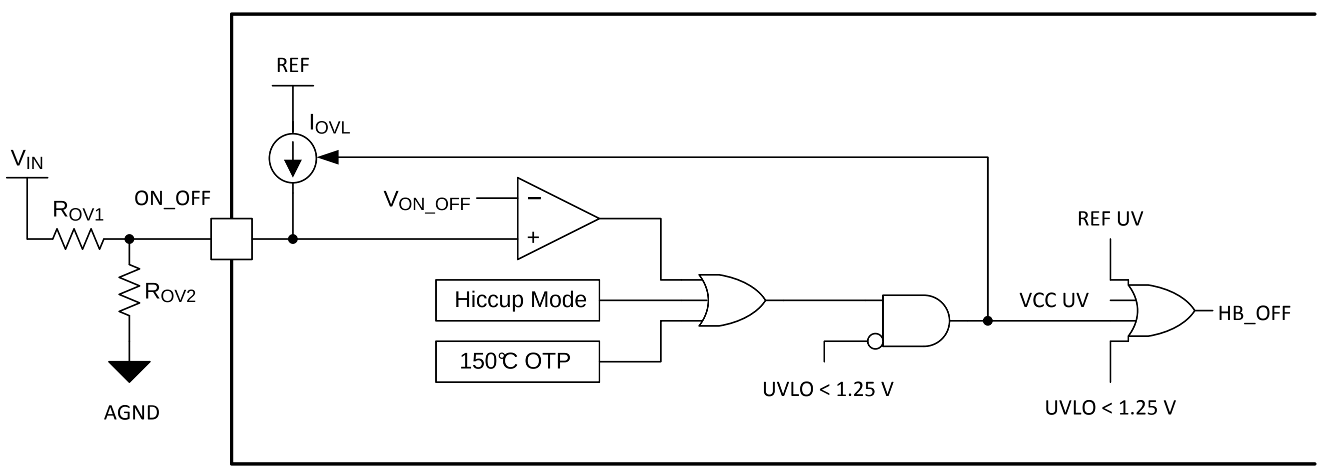


图 32. ON/OFF Pin Configured as OVP Pin

The OVP hysteresis is accomplished with the I_{OVL} current source. When the ON_OFF pin voltage exceeds V_{ON_OFF}, the I_{OVL} current source is activated which quickly raises the voltage at the pin. The half-bridge converter is turned off and the SS and SSSR capacitors are fully discharged. When the ON_OFF pin voltage falls below V_{ON_OFF}, the current source is deactivated causing the voltage at the pin to quickly fall followed by a new soft-start sequence. In addition to the OVP fault, hiccup mode and internal 150-ºC thermal shutdown faults will also cause the half-bridge converter to turn off. Once the faults are cleared, a new soft-start sequence automatically begins. Because the hiccup mode or 150-ºC thermal shutdown fault also activates the current source, it is important to make sure that the ON_OFF pin voltage doesn't rise above V_{ON_OFF} when the input voltage is high, which otherwise would lead to latch operation. Avoid this scenario by selecting a proper voltage divider.

Use 公式 29 and 公式 30 to select the voltage divider for the OVP configuration.

$$R_{OV1} = \frac{V_{HYS(OVP)}}{I_{OVL}}$$

where

- $V_{HYS(OVP)}$ is the OVP hysteresis (29)

$$R_{OV2} = \frac{V_{ON\_OFF} \times R_{OV1}}{V_{IN(OFF)} - V_{ON\_OFF}}$$

where

- $V_{IN(OFF)}$ is the OVP rising threshold (30)

7.3.18 Auxiliary Constant On-Time Control

图 33 shows a block diagram of the constant on-time (COT) controlled fly-buck converter. The LM5036 device integrates an N-channel high-side MOSFET and associated high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01-µF ceramic capacitor connected between the BST_AUX pin and SW_AUX pin provides the voltage to the driver during the on-time. During each off-time, the SW_AUX pin is at approximately 0-V, and the bootstrap capacitor charges from VCC through the internal diode. The minimum off-timer ensures a minimum time in each cycle to recharge the bootstrap capacitor. The LM5036 device also provides an internal N-channel SR MOSFET and associated driver. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The integrated auxiliary supply employs constant on-time (COT) hysteretic control which provides excellent transient response and ease of use. The control principle is based on a comparator and a one-shot on-timer, with the output voltage feedback (FB_AUX) compared to an internal reference. If the feedback voltage is below the reference the internal buck switch is switched on for the one-shot timer period, which is a function of the input voltage and the on-time resistor (R_{ON}). Following the on-time the switch remains off until the FB_AUX voltage falls below the reference, and the forced minimum off-time has expired. When the feedback voltage falls below the reference and the minimum off-time one-shot period expires, the high-side buck switch is then turned on for another on-time one-shot period. This will continue until regulation is achieved.

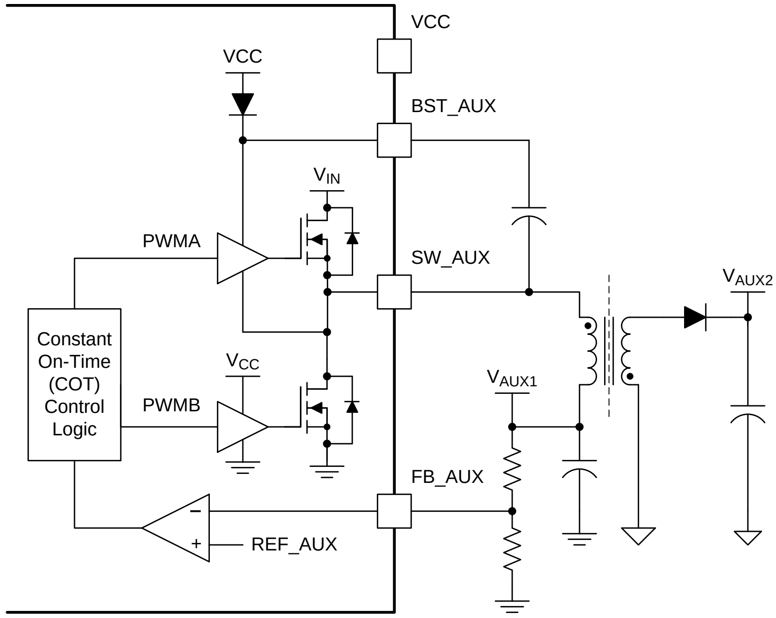


图 33. COT Controlled Fly-Buck Auxiliary Supply Circuitry

In a fly-buck converter, the low-side SR MOSFET is on when the high-side switch is off. The inductor current ramps up when the high-side switch is on and ramps down when the low-side switch is on.

The switching frequency remains relatively constant with load and line variations. Use 公式 31 to calculate the switching frequency of the auxiliary supply.

$$f_{SW\_AUX} = \frac{V_{AUX1}}{9 \times 10^{-11} \times R_{ON}}$$

where

- V_{AUX1} is the primary output voltage of the auxiliary supply. (31)

Two external resistor values set the value of V_{AUX1}. This regulation of the output voltage depends on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{AUX1}). A minimum of 25-mV of ripple voltage at the feedback pin is required for stable operation of the auxiliary supply. The *Auxiliary Ripple Configuration and Control* section describes auxiliary ripple circuit configuration.

7.3.19 Auxiliary On-Time Generator

The on-time for the auxiliary supply is determined by the resistor R_{ON}, and is inversely proportional to the input voltage, resulting in a nearly constant switching frequency as the input voltage is varied over its entire range. 图 34 shows the block diagram for the on-time generator.

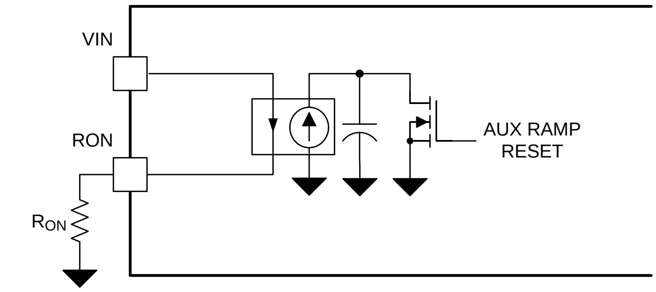


图 34. On-Time Generator

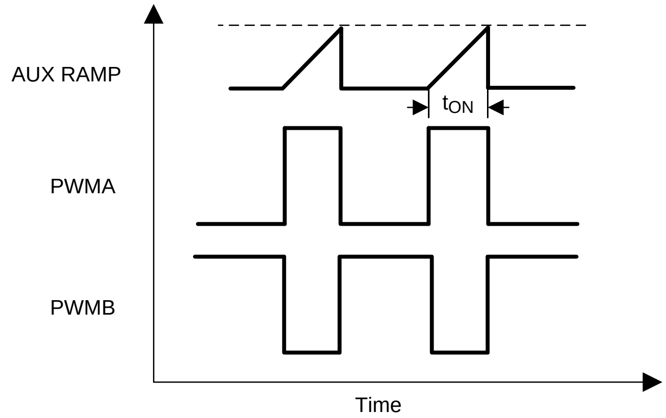


图 35. Constant On-Time Control Waveform

A current source, which is a function of the input voltage and the R_{ON} resistor value, charges a capacitor. The capacitor voltage ramps up linearly and gets reset when it reaches the threshold.

Use 公式 32 to calculate the on time t_{ON} of the high-side switch.

$$t_{ON} = \frac{9 \times 10^{-11} \times R_{ON}}{V_{IN}} \tag{32}$$

7.3.20 Auxiliary Supply Current Limiting

The LM5036 device contains an intelligent current limit off-timer for the auxiliary supply. If the current in the high-side switch exceeds $I_{AUX(LIM)}$ (200-mA typical), both the high-side MOSFET and the low-side SR are immediately turned off, and a non-resetable off-timer is initiated. The length of the off-time is a function of the FB_AUX pin voltage and the input voltage V_{IN}. As an example, when V_{FB_AUX} = 0-V and V_{IN} = 48-V, a maximum off-time is set to 16-µs. This condition occurs when the output is shorted, and during the initial phase of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 100-V.

In cases of overload where the FB_AUX voltage is above zero volts (not a short circuit) the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The current limit off-time is calculated from 公式 33.

$$t_{OFF\,(ILIM)} = \frac{(0.07 \times V_{IN})}{V_{FB\_AUX} + 0.2\ V}\ \mu s \tag{33}$$

Because the current limit protection feature of the auxiliary supply is peak limited, the maximum average output is less than the peak.

To prevent excessive reverse current during the off-time of the current limit, the auxiliary supply will operate in asynchronous (ASYNC) mode where the low-side SR is turned off during current limit operation. The body diode of the internal low-side MOSFET (QB) incurs significant power loss during asynchronous operation. Designers are advised to add an external schottky diode (D_{FW}) between the PGND and SW_AUX pins to ensure robust and efficient current limit operation. This is particularly important when operating from high input voltage. The external schottky diode (D_{FW}) should be rated to carry the maximum Aux current and block the maximum input voltage ($V_{IN(max)}$).

For high density designs it is desirable to use an Aux transformer with low magnetising inductance and saturation current. The peak magnetising current flowing in the Aux transformer can exceed $I_{AUX(LIM)}$ due to delays in the peak current detection and comparator circuit. The actual peak magnetising current reached is a function of the maximum slope of the transformer magnetising current. This in turn depends upon both maximum input voltage $V_{IN(max)}$ and magnetising inductance value. The method outlined below allows designers to estimate the peak magnetising current that will flow in the Aux transformer (I_{LPk}).

As illustrated in 图 36, it is convenient to model the internal current sense circuit as a simple RC time constant, τ_{AuxSns} (41-ns typical), that delays the sensed current signal presented to the OCP comparator input. There is a further delay $t_{AUX(LIM)}$ (116-ns typical), after the comparator input reaches its trip threshold before the OCPb fault flag is set. The extended off time, $t_{OFF(ILIM)}$, will only be applied if the OCPb fault flag is set before the COT (t_{ON}) period ends. 公式 34 is an expression for the sensed and delayed magnetising current inductor signal applied to the non-inverting input of the OCP comparator.

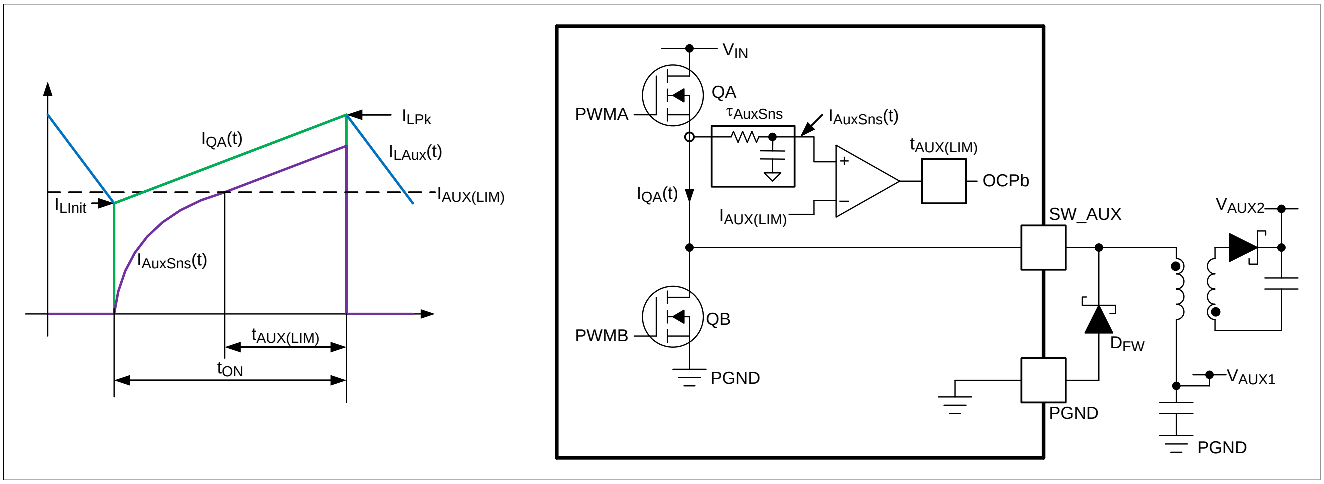


图 36. Aux Current Limit Circuit Model

$$I_{AuxSns}(t) = \left(I_{LInit} - m_{Aux} \times \tau_{AuxSns}\right) \times \left(1 - e^{\frac{-t}{\tau_{AuxSns}}}\right) + m_{Aux} \times t$$

where

- m_{Aux} is the slope of Aux transformer magnetising inductor current during QA on period
- τ_{AuxSns} is the time constant of the internal current sensing circuit feeding the OCP comparator (34)

Maximum peak current will occur when the magnetising inductor current slope has its highest value. This occurs at start-up, or when a short circuit is applied across the V_{AUX1} output, while operating from maximum input voltage ($V_{IN(max)}$). The maximum inductor current slope is given by 公式 35.

$$m_{Aux} = \frac{V_{IN(max)}}{L_{AUX}}$$

where

- L_{AUX} is the magnetising inductance of the Aux transformer (35)

Let us assume the inductor current slope is fixed at its maximum value (m_{Aux}). In this case the highest peak current will occur when the inductor current at the start of the pulse (I_{LInit}) is just high enough to trip the OCPb flag before the COT period (t_{ON}) expires. Once this has occurred the extended OFF period ($t_{OFF(ILIM)}$) will be applied to reduce the inductor current for subsequent pulses. This condition is given in 公式 36 and is shown graphically in 图 36

$$I_{AuxSns}\left(t_{ON} - t_{AUX(LIM)}\right) = I_{AUX(LIM)}$$

where

- $t_{AUX(LIM)}$ is the time delay between comparator input threshold being achieved and the OCPb flag set (36)

Combining 公式 34 and 公式 36 enables us to determine the initial inductor current for a pulse containing the highest peak current 公式 37.

$$I_{LInit} = \frac{I_{AUX(LIM)} - m_{Aux} \times \left(t_{ON} - t_{AUX(LIM)}\right)}{1 - e^{\frac{-\left(t_{ON} - t_{AUX(LIM)}\right)}{\tau_{AuxSns}}}} + m_{Aux} \times \tau_{AuxSns} \quad (37)$$

The COT period used in 公式 37 should be for the maximum input voltage 公式 38

$$t_{ON} = \frac{K_{ON} \times R_{ON}}{V_{IN(max)}}$$

where

- K_{ON} (9 x 10^{-11} typical) is an internal constant that defines the COT period for a given V_{IN} and R_{ON} (38)

Having calculated I_{LInit} the estimated peak inductor current is given by 公式 39.

$$I_{LPk} = I_{LInit} + m_{Aux} \times t_{ON} \quad (39)$$

This method may be used to ensure that the Aux transformer saturation current is not exceeded under transient or fault conditions. Note that the method above assumes fixed transformer magnetising inductance. The method will only provide reasonable accuracy if the transformer magnetising inductance has not fallen significantly at the predicted peak current.

To avoid excessive peak magnetising current during transient or fault events the COT period (t_{ON}) should be longer than the response time of the peak current protection circuit. This may be expressed as a minimum required value for R_{ON} as in 公式 40.

$$R_{ON} \geq \frac{\left(\tau_{AuxSns} + t_{AUX(LIM)}\right) \times 1.2}{K_{ON}} \times V_{IN(max)} = V_{IN(max)} \times 2.09\ k\Omega \quad (40)$$

7.3.21 Auxiliary Primary Output Capacitor Ripple

Equation 92 describes the output ripple voltage amplitude for a buck converter. This equation may be used if there is no secondary winding or if the current supplied by V_{AUX2} is small compared with that supplied by V_{AUX1} (I_{AUX1}>>I_{AUX2}). Equation 92 neglects capacitor ESR and therefore calculates only the capacitive component of output voltage ripple.

$$\Delta V_{AUX1Cap} = \frac{\Delta I_{L(AUX)}}{2 \times f_{SW\_AUX} \times C_{AUX1}} \quad (41)$$

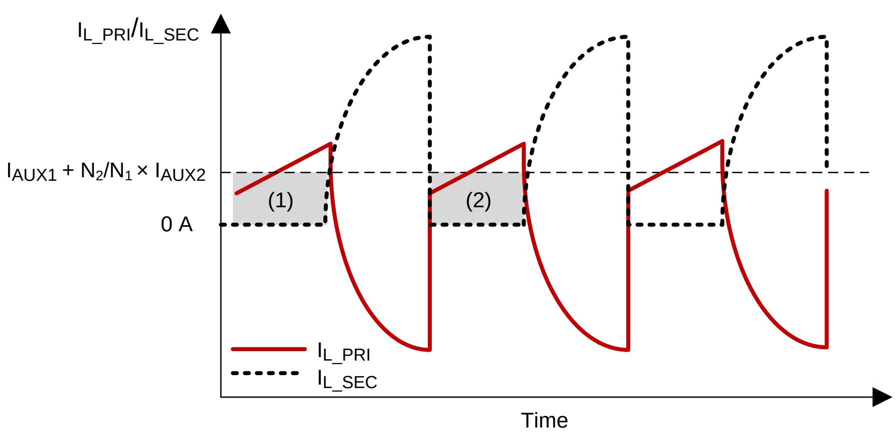


图 37. Auxiliary Transformer Current Waveform for C_{AUX1} Ripple Calculation

Equation 93 shows the flybuck primary and secondary winding current waveforms I_{L_PRI} and I_{L_SEC}. The reflected secondary winding current adds to the primary winding current during the off-time of the high-side switch. Due to this increased current, the output voltage ripple is not the same as in a conventional buck converter. In this case the average current flowing into C_{AUX1} during the t_{ON} period is the reflected secondary current. Hence Equation 94 can be used to calculate $\Delta V_{AUX1Cap}$, the voltage ripple across the primary side capacitor, for the more typical case when the secondary current cannot be neglected. Notice that Equation 94 neglects capacitor ESR and therefore calculates only the capacitive component of ripple voltage amplitude.

$$\Delta V_{AUX1Cap} = \frac{I_{AUX2} \times \frac{N_2}{N_1} \times t_{ON(max)}}{2 \times C_{AUX1}} \tag{42}$$

7.3.22 Auxiliary Ripple Configuration and Control

The voltage ripple across the output capacitor C_{AUX1} is made up of two components:

- Resistive ripple appears across the Equivalent Series Resistance (ESR) of the output capacitor. This component of ripple is in phase with the inductor current and is 90-Deg delayed compared with the applied PWM signal.
- Capacitive ripple appears across the ideal capacitor. This component of ripple is 90-Deg delayed compared with the inductor current ripple and 180-Deg delayed compared with the applied PWM signal.

With COT control, the on-time of the high-side FET is terminated by an on-timer, and the off-time is terminated when the feedback voltage V_{FB_AUX} falls below the reference voltage ($V_{AUX\text{-}ON}$). For a buck topology this type of hysteretic control provides stable operation if these two conditions are met:

- Output voltage ripple is dominated by the resistive ESR component. Let us say the resistive ripple amplitude must be five times the capacitive ripple amplitude to guarantee stable operation.
- Output voltage ripple amplitude present at the FB_AUX pin must be greater than noise coupled onto this pin from other sources. Let us say that an output voltage ripple amplitude of 25-mV at the FB_AUX pin will ensure that other sources of noise coupled to the pin may be assumed small

Aux transformer magnetising inductor ripple current amplitude is expressed by 公式 43.

$$\Delta I_{L(AUX)} = \frac{V_{AUX1}}{2 \times L_{AUX}} \times \left(\frac{1}{f_{SW\_AUX}} - t_{ON} \right) = \frac{K_{ON} \times R_{ON}}{2 \times L_{AUX}} \times \left(1 - \frac{V_{AUX1}}{V_{IN}} \right) \tag{43}$$

For a buck converter the capacitive component of output voltage ripple amplitude is expressed by Equation 92. The resistive component of output ripple voltage amplitude is expressed by 公式 44.

$$\Delta V_{AUX1Res} = \Delta I_{L(AUX)} \times R_{Esr} \tag{44}$$

Our condition for stable operation requires that 公式 45 and 公式 46 are both satisfied.

$$\Delta V_{AUX1Res} \geq 5 \times \Delta V_{AUX1Cap} \tag{45}$$

$$\Delta V_{AUX1Res} \geq 25 - mV \tag{46}$$

The method outlined above allows us to calculate the resistance (R_{Esr}) that must be present in series with the output capacitor (C_{AUX1}) to provide stable operation of a buck converter. This simple method has disadvantages of high output voltage ripple amplitude and high dissipation in the series resistor R_{Esr}. The method is also not ideal for a flybuck topology, especially if most of the load current is drawn from the secondary winding. In this case much of the magnetising inductor current flows into the secondary output capacitor (C_{AUX2}) and not the primary output capacitor (C_{AUX1}) during the low side FET conduction period (t_{OFF}). The circuit of 图 38 provides a better solution that is well suited to the flybuck topology. A series branch R_r - C_r is connected across L_{AUX}. The same PWM voltage is applied across this series branch as appears across L_{AUX}. Assuming most of the PWM voltage is dropped across R_r, the voltage across C_r will have the almost the same shape and phase as the inductor current. The voltage ripple across C_r can be used to substitute the voltage across R_{Esr} and thus provide stable operation without the need for high output ripple and dissipation. By coupling this capacitor voltage signal directly to the FB_AUX pin we can achieve the same result as a large ESR resistor, but without the penalty of dissipation and high output voltage ripple amplitude. The method is suitable for a flybuck topology, since the down-slope of the magnetising current is synthesised, across C_r, and therefore available on the primary side to couple onto the FB_AUX pin.

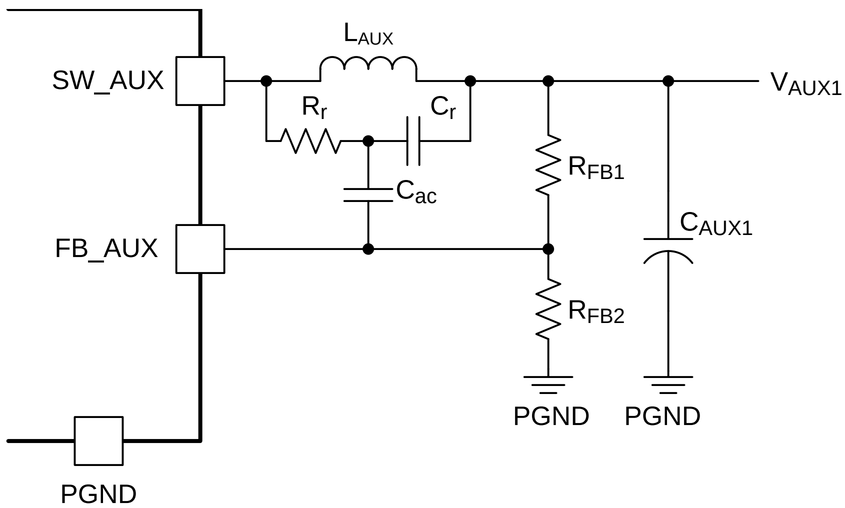


图 38. Minimum Ripple Configuration

The impedance of the capacitor generating the synthesised inductor current ripple signal, at the Aux switching frequency (f_{SW_AUX}), must be low compared with the impedance of the R_{FBx} divider network.

$$C_r > \frac{3}{2 \times \pi \times f_{SW\_AUX}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1} \times R_{FB2}} \tag{47}$$

The synthesised inductor ripple, generated across C_r, is added to the ripple across the output capacitor (C_{AUX1}). The resultant signal is coupled to the FB_AUX pin via capacitor C_{ac}. The value of series resistor R_r is chosen to ensure the synthesised resistive ripple amplitude satisfies 公式 45 giving 公式 48.

$$R_r \leq \frac{K_{ON} \times R_{ON}}{10 \times C_r \times \Delta V_{AUX1Cap}} \times \left(1 - \frac{V_{AUX1}}{V_{IN(min)}}\right) \tag{48}$$

Capacitor C_{ac} couples the ripple signal directly onto the FB_AUX pin. The value of this capacitor should be at least five times greater than the value of C_r. This ensures minimum attenuation and phase shift of the coupled ripple signal.

$$C_{ac} \geq 5 \times C_r \tag{49}$$

7.3.23 Asynchronous Mode Operation of Auxiliary Supply

In LM5036 device, there are two conditions where the auxiliary supply will enter asynchronous (ASYNC) mode operation where the low-side SR is turned off and only its body diode is allowed to conduct. The first condition is when the half-bridge converter is turned off (Refer to the *Device Functional Modes* section). This helps to reduce the power consumption of the auxiliary supply at light loads. As described in the *Auxiliary Supply Current Limiting* section, the auxiliary supply will also be forced to operate at ASYNC mode during current limit operation to prevent excessive reverse current.

7.4 Device Functional Modes

The functional modes of the device are summarized in the following table. Faults include hiccup mode OCP, OVP, and 150°C OTP.

表 1. Device Functional Modes

CRITERIA	VCC AND REF REGULATORS	AUXILIARY SUPPLY	HALF-BRIDGE CONVERTER
UVLO < V_{SD}	OFF	OFF	OFF
(V_{SD} < UVLO < V_{UVLO}) & (V_{IN} < V_{AUX_UVLO})	ON	OFF	OFF
(V_{SD} < UVLO < V_{UVLO}) & (VCC & REF > UV) & (V_{IN} > V_{AUX_UVLO})	ON	ON at ASYNC Mode	OFF
(UVLO > V_{UVLO}) & (V_{IN} > V_{AUX_UVLO}) & (VCC & REF > UV) & No Faults	ON	ON at SYNC Mode	ON
(UVLO > V_{UVLO}) & (V_{IN} > V_{AUX_UVLO}) & (VCC & REF > UV) & Any Faults	ON	ON at ASYNC Mode	OFF
(VCC & REF > UV) & (V_{IN} > V_{AUX_UVLO}) & AUX Current Limit	ON	ON at ASYNC Mode	NA

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5036 device is a highly integrated half-bridge PWM controller that contains all the features necessary for implementing the half-bridge topology power converters using voltage-mode control with input voltage feed-forward. The device targets isolated DC-DC converter applications with input voltage of up to 100 V_{DC}.

8.2 Typical Application

The following schematic shows an example of an isolated half-bridge DC-DC converter controlled by LM5036 device. The operating input voltage range is 36-V to 75-V, and the output voltage is 12-V. The maximum load current is 8-A and the output current limit is configured to be 10-A.

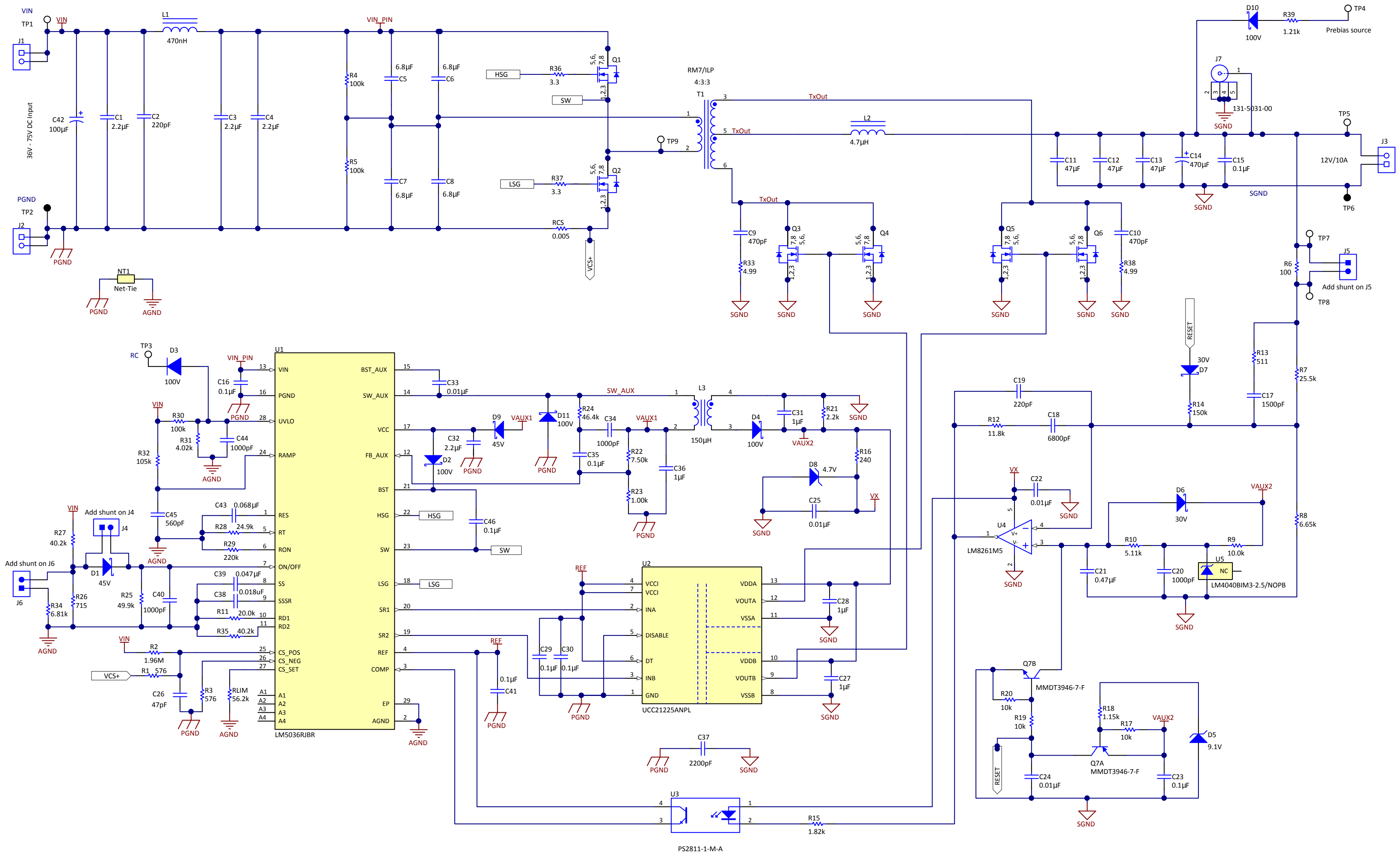


Figure 39. Evaluation Board Schematic

8.2.1 Design Requirements

PARAMETER		VALUE
V_{IN}	Input voltage	36-V to 75-V
V_O	Output voltage	12-V
$I_{O(max)}$	Maximum load current	8-A
I_{LIM}	Output current limit	10-A
η	Peak efficiency	94.4-%
	Efficiency at V_{IN} = 48 V and I_O = 8 A	93.5-%
$V_{AUX1-OFF}$	Off-state auxiliary output voltage	11.9-V
$V_{AUX1-ON}$	On-state auxiliary output voltage	8.5-V
	Load regulation	0.2-%
	Line regulation	0.1-%
	Line UVLO rising/falling threshold	34-V / 32-V
	Line OVP rising/falling threshold	80-V / 78-V
	Latch threshold	80-V
$I_{AUX(max)}$	Maximum load current for auxiliary supply	100-mA

8.2.2 Detailed Design Procedure

The Excel Calculator Tool can be used to assist with selecting both power stage and controller setup components.

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5036 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Input Transient Protection

The voltage applied to the VIN pin of LM5036 device serves as the input voltage for the internal VCC startup regulator and auxiliary supply. In typical applications, the VIN pin voltage is the same as the input voltage for the main half-bridge converter. The recommended range of the VIN pin voltage is 18-V to 100-V. Figure 40 shows the recommended filter to suppress transients that may occur at the input supply. This suppression is particularly important when the input voltage rises to a level near the maximum recommended operating rating (100-V) of the LM5036 device.

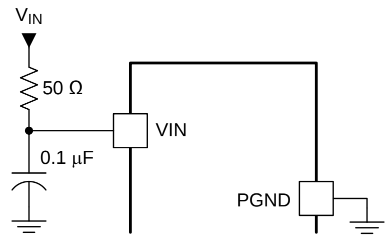


Figure 40. Input Transient Protection

8.2.2.3 Level-Shift Detection Circuit

An example implementation of the V_{AUX2} level-shift detection circuit is shown in Figure 41. The zener voltage must be between the off-state and on-state level of V_{AUX2}. When V_{AUX2} is above the zener voltage, both Q1A and Q1B are turned on and therefore the reference output voltage V_{REFSec} is clamped to ground. Once V_{AUX2} falls below the zener voltage, both Q1A and Q1B are turned off, and the reference is released.

Designers who wish to benefit from the fully regulated pre-biased startup feature of LM5036 must use separate voltage reference and error amplifier devices. Popular combined error amplifier and voltage reference devices, such as TL431, can be used only when the fully regulated pre-biased startup feature is not required.

Assistance with half-bridge voltage control loop design may be obtained using the Power Stage Designer™ tool.

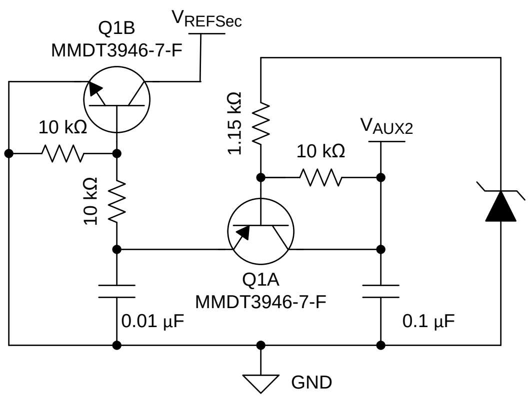


Figure 41. Secondary Auxiliary Voltage Level-Shift Detection Circuit

8.2.2.4 Applications with V_{IN} > 100-V

For applications where the input voltage exceeds 100-V, all of the 100V-rated internal circuit blocks, including VCC start-up regulator, auxiliary supply and half-bridge gate drivers, need to be bypassed, or powered from a reduced voltage. In this case, VIN pin can be powered from an external start-up regulator, as shown in Figure 42. If pre-biased start-up is required the integrated flybuck aux circuit should be used from the reduced VIN pin voltage to supply the secondary control circuit. If pre-biased start-up is not required, the bias supply V_{AUX1}, can be derived from an external auxiliary supply. An external gate driver with higher voltage rating should be used to drive the half bridge.

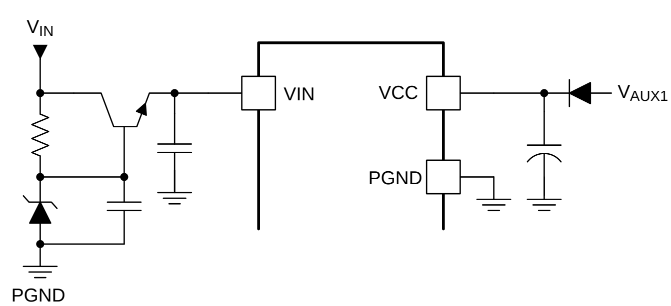


Figure 42. External Start-Up Regulator

8.2.2.5 Applications without Pre-Biased Start-Up Requirement

For applications where the pre-biased startup is not required, the level-shift detection circuit described in the *Pre-Biased Start-Up Process* section is not necessary. Without the level-shift detection circuit, the reference voltage on the secondary side would be released as soon as the secondary bias is established. The external VCC bias supply can be derived from the integrated auxiliary supply or an auxiliary winding of the main transformer.

8.2.2.6 UVLO Voltage Divider Selection

As described in the *Undervoltage Lockout (UVLO)* section, two external resistors can be used to program the minimum operating voltage for the power converter, as shown in Figure 43. When the UVLO pin voltage falls below V_{UVLO} (1.25-V typical), an internal current sink I_{UVLO} (20-µA typical) is enabled to lower the voltage at the UVLO pin, thus providing threshold hysteresis. Resistance values for R_{UV1} and R_{UV2} can be determined from Equation 50 and Equation 51.

$$R_{UV1} = \frac{H_{HYS(UVLO)}}{I_{UVLO}}$$

where

- $V_{HYS(UVLO)}$ is the UVLO hysteresis (50)

$$R_{UV2} = \frac{V_{UVLO} \times R_{UV1}}{V_{IN(on)} - V_{UVLO} - I_{UVLO} \times R_{UV1}}$$

where

- $V_{IN(on)}$ is the input voltage above which the main converter will start to operate. (51)

Figure 44 illustrates one way to configure a latch reset operation by pulling the UVLO pin voltage below V_{UVLO}. The diode voltage drop must be between 0.35-V and 1.25-V. The controller can be forced to enter shutdown mode by pulling UVLO pin to GND.

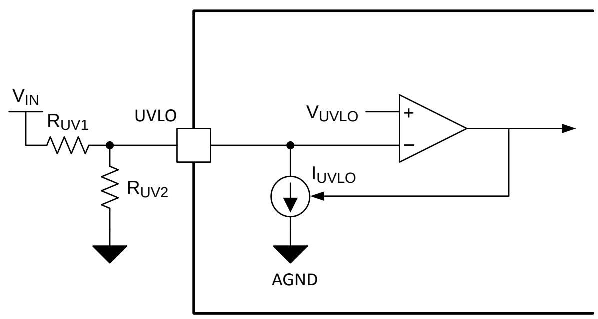


Figure 43. UVLO Configuration

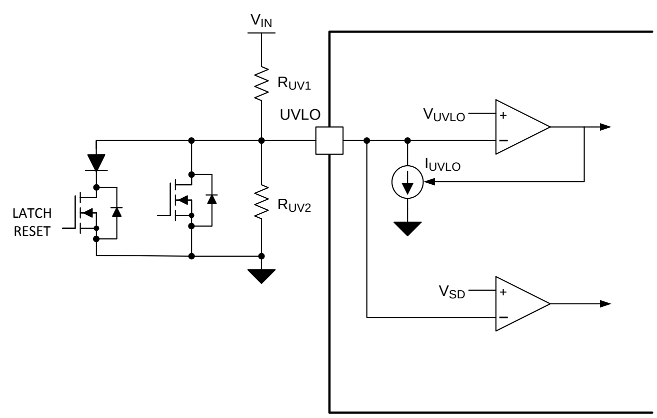


Figure 44. Latch Reset

8.2.2.7 Over Voltage / Latch (ON_OFF Pin) Voltage Divider Selection

As described in the *Over-Voltage / Latch (ON_OFF Pin)* section, the ON_OFF pin can be configured as a latch pin or an OVP pin. 图 31 shows the latch configuration. The ON_OFF pin is latched when the pin voltage reaches I_{OVL} × R_L when any of the internal faults is detected. The latch diode is reverse-biased during latch operation. The latch resistor R_L should be selected such that I_{OVL} × R_L > V_{ON_OFF}. In this design example, R_L is selected to be 49.9-kΩ. If the latch threshold is 80-V, R_{OV1} should be 40-kΩ, and R_{OV2} should be 710-Ω.

If the ON_OFF pin is configured as an OVP pin, two resistors can be used to program the maximum operating input voltage for the half-bridge converter, as illustrated in 图 32. When the ON_OFF pin voltage rises above the V_{ON_OFF} threshold, an internal current source I_{OVL} is enabled to raise the ON_OFF pin voltage, thus providing the threshold hysteresis. Use 公式 29 and 公式 30 to determine resistance values for R_{OV1} and R_{OV2}. If the LM5036 device is to be disabled when V_{IN} rises above 80-V and enabled when it falls below 78-V. R_{OV1} should be 40-kΩ, and R_{OV2} should be 635-Ω. In addition, the ON_OFF pin can also be used for external thermal protection with a thermistor.

8.2.2.8 SS Capacitor

The soft-start delay $t_{D(SS)}$, which is the time it takes for the soft-start capacitor to rise from 0 V to $V_{SSSecEn}$ (2.06-V typical), can be programmed with the SS capacitor value according to Equation 52

$$C_{SS} = \frac{I_{SS} \times t_{D(SS)}}{V_{SSSecEn}}$$

where

- I_{SS} (20-µA typical) is the current source of the soft-start pin (52)

8.2.2.9 SSSR Capacitor

The SSSR capacitor value determines the rate at which the pulse width of the SR's of the half-bridge converter increases. To achieve a monotonic start-up for the output voltage, the SSSR capacitor value should satisfy the following two conditions:

- SR soft-start sequence should be completed before regulation set-point of the output voltage is reached.
- With a lower control loop bandwidth, the primary-side duty cycle tends to increase at a slower rate. Therefore the ramp-up speed of the SSSR capacitor voltage should be reduced accordingly in order to prevent excessive reverse current.

A general rule of thumb is to maintain the control loop bandwidth of the half-bridge converter above 1-kHz. With a slow control loop bandwidth, the output voltage needs to drop at least 25% from the regulation set-point during the restart time period where the SS pin voltage rises from 0-V to $V_{SSSecEn}$ (2.06-V typical) and then the secondary-side reference V_{REF} rises to 75% of regulation set-point. To satisfy the first condition above, the rise time of the SSSR capacitor voltage should be less than 25% of the rise time of the output voltage, as described in Equation 53.

$$C_{SSSR} < \frac{I_{SSSR} \times 25\% \times t_{RAMP}}{5\ V}$$

where

- I_{SSSR} (20-µA typical) is the current source of the SSSR pin. t_{RAMP} is the ramp-up time of the output voltage. (53)

Use the SSSR capacitor value calculated from Equation 53 as a starting point. Fine-tuning may be needed based on the actual control loop design and other specific design requirements such as pre-bias conditions and loading profile.

8.2.2.10 Half-Bridge Power Stage Design

For a PWM operating frequency of 400kHz applied to the output inductor the oscillator frequency of LM5036 must also be set to 400kHz. The value of resistor R_T is obtained using Equation 54.

$$R_T = \frac{1}{f_{OSC} \times 1 \times 10^{-10}} = 25 - k\Omega \quad (54)$$

Maximum effective duty cycle that can be applied to the output inductor is Equation 55.

$$D_{MAX} = 1 - t_{CLK} \times f_{OSC} = 0.974 \quad (55)$$

Maximum transformer turns ratio that will deliver the required output voltage from minimum input voltage is given by Equation 56.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{IN(min)}}{2 \times V_O} = 1.46 \quad (56)$$

For our example design we will opt for a planar transformer with 4 primary turns and 3 secondary turns. The turns are located in an un-gapped RM7/ILP ferrite core made of 3C95 material. This core has an inductance factor AL = 4.4-µH/turn^2. Hence the actual turns ratio (N_{PS}) and magnetising inductance (L_{Mag}) are given by Equation 57 and Equation 58.

$$N_{PS} = \frac{N_P}{N_S} = \frac{4}{3} \quad (57)$$

$$L_{Mag} = N_P{}^2 \times AL = 70.4 - \mu H \quad (58)$$

Maximum inductor current ripple will occur at maximum input voltage. The output inductor value L_O will be selected to limit inductor current ripple amplitude to 20-% of the maximum output current I_{LIM}

$$L_O = \frac{V_O \times (1 - D_{MIN})}{20\% \times 2 \times I_{LIM} \times f_{OSC}} = 4.3 - \mu H \quad (59)$$

Hence a catalog part with an inductance of 4.7-µH, capable of carrying the full output current, and with a saturation current of more that 120-% of I_{LIM}, is selected.

$$L_O = 4.7 - \mu H \quad (60)$$

8.2.2.11 Current Limit

The *Enhanced Cycle-by-Cycle Current Limiting with Pulse Matching* section describes the CBC current limiting functionality in detail. Figure 45 illustrates the current limiting block diagram of the LM5036 device. There are five resistors associated with the current limiting function of the half-bridge converter, as listed below:

- R_{CS}
- R_3
- R_2
- R_{LIM}
- R_1

Because R_3 is equal to the equivalent resistance of R_1 and R_2 as given by 公式 13, there are four unknown resistor values to be determined.

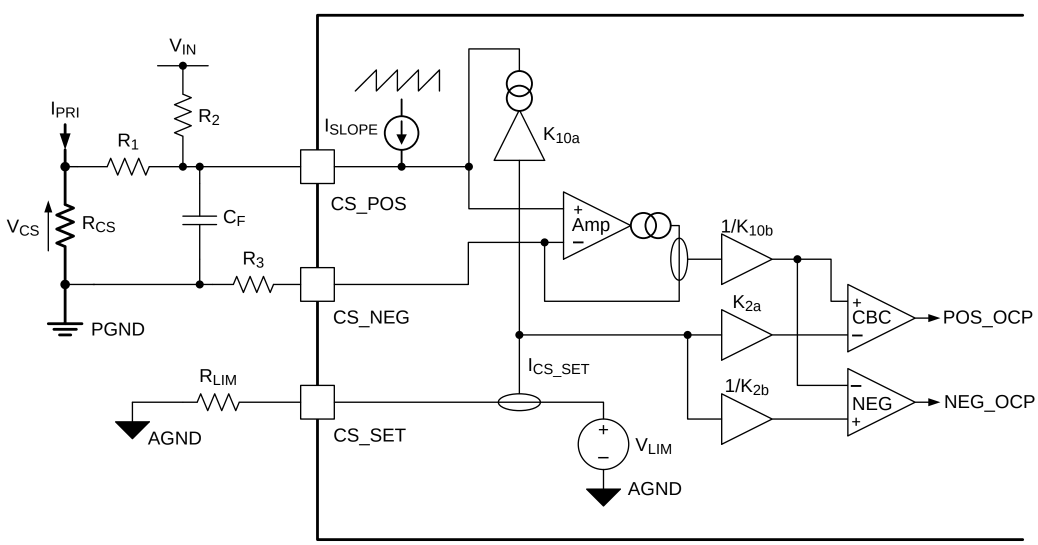


Figure 45. Current Limiting Block

The value of current sense resistor R_{CS} is determined based on the maximum power consumption requirement. Typically, the current sense resistor should consume less than 0.5% of the input power of the converter at the worst case scenario. The sense resistor conducts every alternate current pulse flowing in the primary winding. The power dissipated in the sense resistor is determined by Equation 61.

$$P_{CS} = \frac{I_{Pri\_RMS}^{2}}{2} \times R_{CS} \tag{61}$$

The RMS current flowing in the primary winding may be calculated using Equation 62.

$$I_{Pri\_RMS} = \frac{I_O}{N_{PS}} \times \sqrt{D \times \left(1 + \frac{1}{3} \times \left(\frac{\Delta I_{Pri}}{I_O}\right)^2\right)}$$

Where :

$$\Delta I_{Pri} = \frac{\Delta I_{LO}}{N_{PS}} + \Delta I_{LMag} = \frac{V_O}{2 \times L_O \times N_{PS}} \times \left(\frac{1-D}{f_{OSC}}\right) + \frac{V_{IN}}{4 \times L_{Mag}} \times \frac{D}{f_{OSC}} \tag{62}$$

Maximum loss in the current sense resistor will occur while maximum output current (I_{LIM}) is delivered from minimum input voltage ($V_{IN(min)}$). Evaluating Equation 62 gives Equation 63.

$$I_{Pri\_RMS} = 7.07\,A \tag{63}$$

To achieve our target of dissipating less than 0.5% of maximum output power the current sense resistor must satisfy Equation 64.

$$R_{CS} < 0.5\% \times V_O \times I_{LIM} \times \frac{2}{I_{Pri\_RMS}^{2}} = 0.024\,\Omega \tag{64}$$

In our example design the current sense resistor value selected is given in Equation 65.

$$R_{CS} = 5\,m\Omega \tag{65}$$

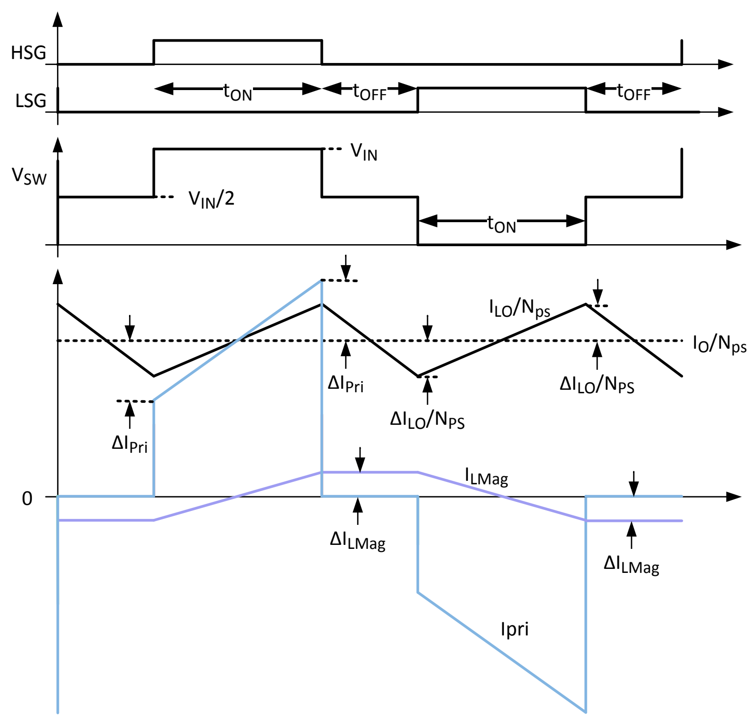


Figure 46. Main Converter Operating Waveforms

The resistor R_1 is used to set the slope compensation magnitude. In LM5036 device, the slope of the compensation ramp is given by Equation 66. To eliminate sub-harmonic oscillation, m_C should be set to at least one-half the down-slope of output inductor current transformed to the primary side across the current sense resistor, as given by Equation 67 and Equation 68. To damp the sub-harmonic oscillation after one cycle, m_C must be set equal to one times the down-slope of the output inductor current. This configuration is known as deadbeat control. In LM5036 device, the slope compensation signal is a saw-tooth current waveform of magnitude I_{SLOPE} at the oscillator frequency (twice the switching frequency).

$$m_C = I_{SLOPE} \times f_{OSC} \times R_1$$

where
- m_C is the slope of the compensation ramp
- I_{SLOPE} is the amplitude of the saw-tooth current signal used for slope compensation (66)

$$m_L = \frac{V_O}{L_O} \times \frac{1}{N_{PS}} \times R_{CS} = 9.57\ \frac{mV}{\mu s}$$

where
- m_L is the down-slope of the output inductor current transformed to the primary side
- N_P is the number of turns for the primary winding of the main transformer
- N_S is the number of turns for the secondary winding of the main transformer
- V_O is the output voltage of the half-bridge converter
- L_O is the output inductor value of the half-bridge converter
- R_{CS} is the current sense resistor value (67)

$$m_C > \frac{1}{2} \times m_L \tag{68}$$

Substituting Equation 66 and Equation 67 into Equation 68 gives an expression for the minimum value for resistor R_1 to avoid sub-harmonic oscillation.

$$R_1 > \frac{1}{2} \times \frac{V_O}{L_O} \times \frac{1}{N_{PS}} \times R_{CS} \times \frac{1}{I_{SLOPE} \times f_{OSC}} = 221 - \Omega \tag{69}$$

Deadbeat control is ensured by doubling this value. For our example design the value given in Equation 70 has been selected

$$R_1 = 576\ \Omega \tag{70}$$

Values have now been selected for both R_{CS} and R_1. Values for R_{LIM} and R_2 are yet to be determined. These values define the peak current limit threshold and how this level will vary with input voltage. The relationship between peak primary current limit and maximum output current is defined by 公式 20, 公式 21 and 公式 25. For this design example we will neglect $I_{BiasOffset}$, $V_{CSOffset}$. Since these parameters have only a small effect on output current limit. Setting these parameters to zero we arrive at Equation 71, Equation 72 and Equation 73.

$$I_O\left(V_{IN}, R_{LIM}, R_2\right) = N_{PS} \times \left[I_{PriCBC}\left(V_{IN}, R_{LIM}, R_2\right) - \frac{V_O}{2 \times L_O \times f_{OSC} \times N_{PS}} \times (1-D) - \frac{V_O \times N_{PS}}{2 \times L_{Mag} \times f_{OSC}} \right] \tag{71}$$

$$I_{PriCBC}\left(V_{IN}, R_{LIM}, R_2\right) = \frac{V_{CS\_CBCTh}(V_{IN}, R_{LIM}, R_2)}{R_{CS}} + t_{CSLSG} \times \left(\frac{1}{2} \times \left(\frac{V_{IN}}{L_{Mag}} + \frac{V_{IN}}{L_O \times N_{PS}^2} \right) - \frac{V_O}{L_O \times N_{PS}} \right) \tag{72}$$

$$V_{CS\_CBCTh}(V_{IN}, R_{LIM}, R_2) = R_1 \times \left(\frac{K_{CBC1}}{R_{LIM}} - I_{SLOPE} \times D - \frac{V_{IN}}{R_2} \right) \tag{73}$$

The output current limit will vary with input voltage. For this design example the output current limit is set to I_{LIM} at the extremes of input voltage giving Equation 74 and Equation 75. This is done to limit the spread of output current limit across the range of input voltage.

$$I_O\left(V_{IN(min)}, R_{LIM}, R_2\right) = I_{LIM} \tag{74}$$

$$I_O\left(V_{IN(max)}, R_{LIM}, R_2\right) = I_{LIM} \tag{75}$$

Solving Equation 74 and Equation 75 simultaneously yields values for resistors R_{LIM} and R_2.

$$R_2 = \frac{1}{\frac{t_{CSLSG}}{2} \times \frac{R_{CS}}{R_1 \times N_{PS}} \times \left(\frac{1}{L_{Mag}} + \frac{1}{L_O \times N_{PS}^2}\right) - \frac{1}{V_{IN(min)} \times V_{IN(max)}}\left(\frac{V_O^2}{L_O \times f_{OSC}} \times \frac{R_{CS}}{R_1} - I_{SLOPE} \times 2 \times V_O \times N_{PS}\right)} = 2.32 - M\Omega \tag{76}$$

$$R_{LIM} = \frac{K_{CBC1}}{\frac{R_{CS}}{R_1} \times \left[\frac{I_{LIM}}{N_{PS}} + \frac{V_O}{2 \times L_O \times N_{PS} \times f_{OSC}} \times \left(1 - \frac{2 \times V_O \times N_{PS}}{V_{IN(min)}}\right) + \frac{V_O \times N_{PS}}{2 \times L_{Mag} \times f_{OSC}} - \frac{t_{CSLSG}}{N_{PS}} \times \left[\frac{V_{IN(min)}}{2 \times L_{Mag}} + \frac{V_{IN(min)}}{2 \times L_O \times N_{PS}^2} - \frac{V_O}{L_O \times N_{PS}}\right]\right] + I_{SLOPE} \times \frac{2 \times V_O \times N_{PS}}{V_{IN(min)}} + \frac{V_{IN(min)}}{R_2}} = 55.2 - k\Omega \tag{77}$$

Having determined values for R_1 and R_2, the value of resistor R_3 is fixed by 公式 13.

The selected values for R_2 and R_{LIM} are given in Equation 78. Figure 47 presents the measured output current limit vs input voltage for the circuit presented in Figure 39. Figure 47 also presents the output current limit vs line for the same circuit predicted by Equation 71, Equation 72 and Equation 73. There is good agreement between measured and predicted results.

$$R_2 = 1.96\ M\Omega$$
$$R_{LIM} = 56.2\ k\Omega \tag{78}$$

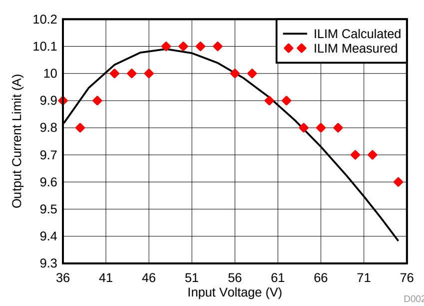


Figure 47. Main Converter Measured vs Predicted Output Current Limit

If the magnitude of the leading-edge spike is excessive, an additional filter capacitor C_F should be added to form an RC filter with R_1, to reduce the high-frequency noise spike. Both the leading-edge blanking (t_{CSBLK}) and the RC filter help to prevent false triggering of the CBC current limiting operation.

The circuit connected to the CS_POS pin may be approximated by the simplified schematic of Figure 48.

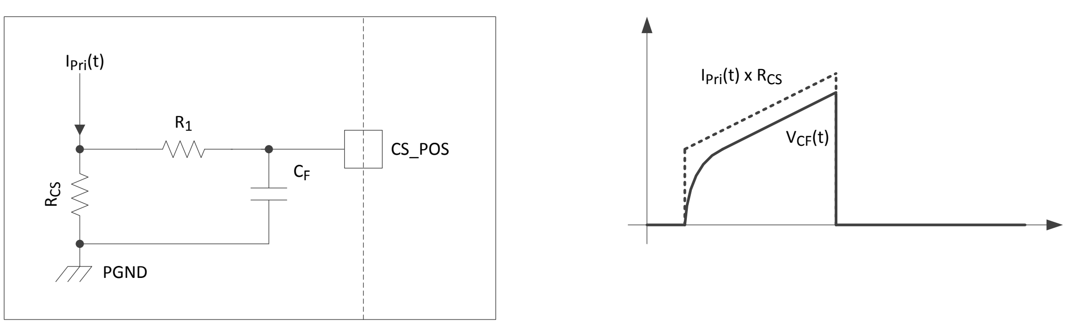


Figure 48. CS_POS Filter Circuit Model and Waveform

The voltage across the current sense resistor during the conduction period of the lower MOSFET is represented by Equation 79.

$$I_{Pri}(t) \times R_{CS} = (I_{P0} + m \times t) \times R_{CS} \tag{79}$$

Where I_{P0} is the primary current at the start of the on period of the lower switch, and m is the slope of the primary current during the on period.

$$I_{P0} = \frac{I_O}{N_{PS}} - \Delta I_{LMag} - \frac{\Delta I_{LO}}{N_{PS}} \tag{80}$$

$$m = \left(\frac{V_{IN(max)}}{2 \times N_{PS}} - V_O \right) \times \frac{1}{L_O \times N_{PS}} + \frac{V_{IN(max)}}{2 \times L_{Mag}} \tag{81}$$

It can be shown that the voltage across capacitor C_F for the circuit shown is expressed by Equation 82.

$$V_{CF}(t) = R_{CS} \times \left[(I_{P0} - m \times C_F \times R_1) \times \left(1 - e^{\frac{-t}{C_F \times R_1}} \right) + m \times t \right] \tag{82}$$

Let us assume that the on period of the lower switch is more than four times longer than the time constant made up of C_F and R_1. In this case the exponential term of Equation 82 will tend to zero and the voltage across capacitor C_F at the end of the t_{ON} period may be expressed by Equation 83.

$$V_{CF}(t_{ON}) = R_{CS} \times [I_{P0} - m \times C_F \times R_1 + m \times t_{ON}] \tag{83}$$

Comparing Equation 79 and Equation 83 we can see that capacitor C_F introduces an error in the sensed peak current given by Equation 84.

$$ErrCF = \frac{V_{CS}(t_{ON}) - V_{CF}(t_{ON})}{\frac{I_{LIM}}{N_{PS}} \times R_{CS}} = \frac{m \times C_F \times R_1}{\frac{I_{LIM}}{N_{PS}}} = \frac{\left[\left(\frac{V_{IN(max)}}{2 \times N_{PS}} - V_O \right) \times \frac{1}{L_O \times N_{PS}} + \frac{V_{IN(max)}}{2 \times L_{Mag}} \right] \times C_F \times R_1}{\frac{I_{LIM}}{N_{PS}}} \tag{84}$$

Hence, to ensure the error introduced by the filter capacitor is less than 2%, the value of capacitor C_F should not exceed the value given by Equation 85.

$$C_F \le \frac{0.02 \times I_{LIM}}{\left[\left(\frac{V_{IN(max)}}{2 \times N_{PS}} - V_O \right) \times \frac{1}{L_O \times N_{PS}} + \frac{V_{IN(max)}}{2 \times L_{Mag}} \right] \times R_1 \times N_{PS}} = 84 - pF \tag{85}$$

The Excel Calculator Tool can be used to facilitate the process of calculating all the external CBC component values.

8.2.2.12 Auxiliary Transformer

A coupled inductor or a flyback-type transformer is required for this fly-buck topology auxiliary supply. Energy is transferred from primary to secondary when the low-side SR MOSFET is conducting.

The transformer turns ratio is selected based on the ratio of the primary output voltage to the secondary output voltage. In this design example, the two outputs are set to be equal and a 1:1 turns ratio transformer is selected, i.e., N_2/N_1 = 1. The primary output voltage is normally selected based on the input voltage range such that the duty cycle of the converter does not exceed 50% at the minimum input voltage. This condition is satisfied if $V_{AUX1} < V_{IN(min)} / 2$.

Use Equation 86 to calculate the maximum inductor current ripple amplitude $\Delta I_{L(AUX)}$ that can be tolerated without exceeding the peak current limit threshold $I_{AUX(LIM)}$ (200-mA typical) of the high-side switch,

$$\Delta I_{L(AUX)} = \left(I_{AUX(LIM)} - I_{AUX1} - I_{AUX2} \times \frac{N_2}{N_1} \right)$$

where

- I_{AUX1} is the primary output current, and I_{AUX2} is the secondary output current of the auxiliary supply, respectively. (86)

In this design example, the maximum total output current $I_{AUX(max)}$ of the auxiliary supply referred to the primary side is 100-mA, as given by Equation 87.

$$I_{AUX(max)} = I_{AUX1} + I_{AUX2} \times \frac{N_2}{N_1} = 0.1\ A \tag{87}$$

Therefore, $\Delta I_{L(AUX)}$ = 0.1-A. Use Equation 88 to calculate the minimum inductor value for the auxiliary supply.

$$L_{AUX} \geq \frac{K_{ON} \times R_{ON}}{2 \times \Delta I_{L(AUX)}} \times \left(1 - \frac{V_{AUX1}}{V_{IN(max)}}\right) = 88 - \mu H \tag{88}$$

Select a higher value of 150-µH to ensure the high-side switch current doesn't exceed the minimum peak current limit threshold.

8.2.2.13 Auxiliary Feedback Resistors

The two feedback resistors are selected to set the primary output voltage V_{AUX1} of the auxiliary supply. The internal reference for the off-state and on-state auxiliary output voltage levels are $V_{AUX\text{-}OFF}$ (1.4-V typical) and $V_{AUX\text{-}ON}$ (1-V typical). The feedback resistors are calculated such that both of the off-state and on-state auxiliary output voltage fall into the recommended operating range (8.5-V to 14-V). In this design example, the off-state and on-state auxiliary output voltages are set to 11.9-V and 8.5-V, respectively. R_{FB2} is selected to be 1-kΩ and R_{FB1} is calculated to be 7.5-kΩ according to Equation 89. Note that it is the valley of the output voltage that is regulated at the reference value. Therefore the average output voltage is greater than the reference value due to the ripple injected to the feedback node.

$$V_{AUX1-ON} = V_{AUX-ON} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \tag{89}$$

8.2.2.14 R_{ON} Resistor

Use 公式 31 to calculate the value of R_{ON} required to achieve the desired switching frequency for the auxiliary supply. Make sure that the calculated R_{ON} value is greater than the minimum value required by 公式 40. For this design example where on-state V_{AUX1} is 8.5-V and target f_{SW_AUX} is 500-kHz, the calculated value of R_{ON} is 189-kΩ. The minimum recommended value calculated using 公式 40 is 209-kΩ. A standard value of 220-kΩ is selected to satisfy this minimum R_{ON} requirement giving and actual switching frequency (f_{SW_AUX}) of 430-kHz.

8.2.2.15 VIN Pin Capacitor

Place the required bypass capacitor close to the VIN pin of the LM5036 device. Ensure that the capacitance is large enough to limit the ripple of the VIN pin voltage to a desired level. Use Equation 90 to calculate the value of C_{IN} required to meet the ripple voltage ΔV_{IN} requirement.

$$C_{IN} \geq \frac{I_{AUX(max)}}{4 \times f_{SW\_AUX} \times \Delta V_{IN}} \tag{90}$$

Choosing a value of 0.5-V for ΔV_{IN} yields a minimum C_{IN} value of 0.12-µF. Select the standard value of 0.1-µF for this design. Ensure that the voltage rating of the input capacitor is greater than the maximum input voltage under all conditions.

8.2.2.16 Auxiliary Primary Output Capacitor

The output capacitor value (C_{AUX1}), needed to achieve our target output ripple amplitude ($\Delta V_{AUX1Cap}$ = 25-mV), may be calculated using Equation 94.Highest ripple voltage will be observed if all the Aux current is drawn from V_{AUX2} (I_{AUX2}=$I_{AUX(max)}$). In this case a capacitor value of 1.1-µF is required to limit capacitive ripple voltage amplitude to 25-mV. A standard 1-µF, 25-V capacitor is selected for this design.

8.2.2.17 Auxiliary Secondary Output Capacitor

A simplified waveform for the secondary winding current I_{L_SEC} is shown in Figure 49.

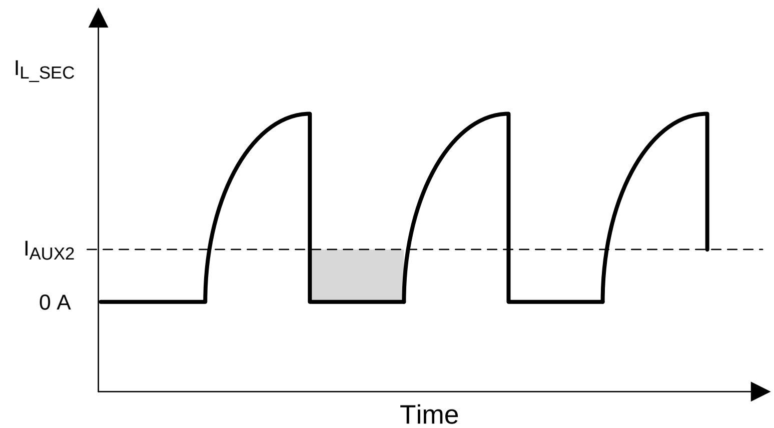


Figure 49. Auxiliary Transformer Secondary Winding Current Waveforms for C_{AUX2} Ripple Calculation

The secondary output current I_{AUX2} is sourced by C_{AUX2} during on-time of the high-side switch, t_{ON}. Ignoring the current transition times in the secondary winding, the secondary output capacitor ripple voltage amplitude can be calculated using Equation 91.

$$\Delta V_{AUX2Cap} = \frac{I_{AUX2} \times t_{ON(max)}}{2 \times C_{AUX2}} \tag{91}$$

For a 1:1 auxiliary transformer turns ratio, the primary and secondary voltage ripple equations are identical. Therefore, C_{AUX2} is chosen to be equal to C_{AUX1} (1 µF) to achieve comparable ripple voltages on the primary and secondary outputs.

8.2.2.18 Auxiliary Feedback Ripple Circuit

The auxiliary feedback ripple circuit employed is presented in 图 38. Having selected appropriate values for R_{ON} in R_{ON} Resistor and R_{FBx} in Auxiliary Feedback Resistors, the value of C_r required can be calculated using 公式 47. For our design we have opted to use a standard value C_r = 1-nF.

$$C_r > \frac{3}{2 \times \pi \times f_{SW\_AUX}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1} \times R_{FB2}} = 1.3 - nF \tag{92}$$

Based on our target output ripple specification a value for the primary output capacitor (C_{AUX1} = 1-µF) was chosen in Auxiliary Primary Output Capacitor. The primary output ripple voltage $V_{AUX1Cap}$ can be calculated using Equation 94. Since the value of $V_{AUX1Cap}$ is already greater than 25-mV there is no danger that we will fail to meet the requirement of 公式 46. Hence the value of R_r needed to ensure stable operation is calculated using 公式 48. For our design example a value of 46.4-kΩ has been selected.

$$R_r \le \frac{K_{ON} \times R_{ON}}{10 \times C_r \times \Delta V_{AUX1Cap}} \times \left(1 - \frac{V_{AUX1}}{V_{IN(min)}}\right) = 55 - k\Omega \tag{93}$$

The minimum value of C_{ac} is determined using 公式 49. The precise value of this component is not very critical and for our design example we selected a convenient value of C_{ac} = 100-nF.

$$C_{ac} \ge 5 \times C_r = 5 - nF \tag{94}$$

8.2.2.19 Auxiliary Secondary Diode

Use Equation 95 to calculate the reverse voltage across secondary rectifier of the auxiliary supply when the high-side switch is on.

$$V_D = \frac{N_2}{N_1} \times V_{IN(max)} \tag{95}$$

For a maximum input voltage of 75-V and the 1:1 turns ratio of this design, select a schottky diode with a rating of 75-V or higher.

8.2.2.20 VCC Diode

A diode must be connected between the primary output V_{AUX1} and the VCC pin. When V_{AUX1} is more than one diode voltage drop greater than the internal VCC voltage, the VCC bias current is supplied from V_{AUX1}. This results in reduced power losses in the internal VCC regulator, especially at high input voltage.

8.2.2.21 Opto-Coupler Interface

Figure 50 illustrates the opto-coupler interface for the main feedback control loop. The primary side of the opto-coupler is biased with V_{REF} voltage from LM5036 device. R_{OPTO} should be selected such that with the minimum error amplifier output, the comp current flowing into the COMP pin of the device is greater than I_{PWM-OS} (800-µA typical) which corresponds to zero duty cycle, as given by Equation 96.

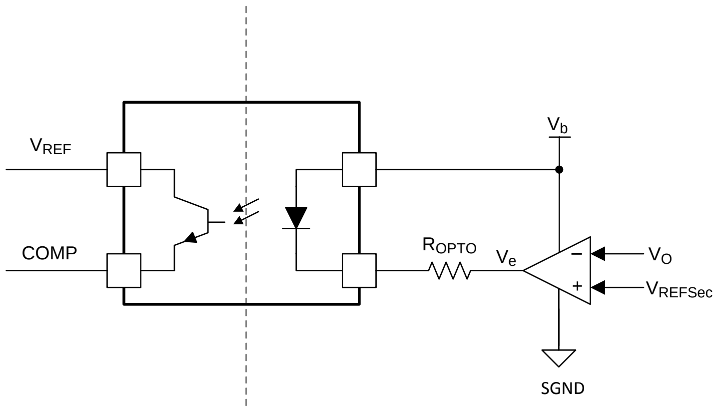


Figure 50. Opto-Coupler Interface

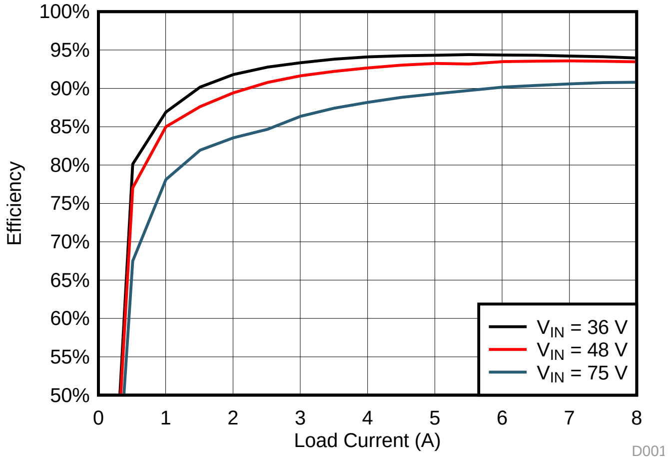
$$I_{COMP} = \frac{V_b - V_f - V_e}{R_{opto}} \times CTR$$

where
- V_b is the bias supply for the error amplifier and opto-coupler on the secondary side
- V_f is the diode forward voltage drop of the opto-coupler LED
- V_e is the error amplifier output
- CTR is the current transfer ratio of the opto-coupler
- I_{COMP} is the comp current flowing into the COMP pin
- V_{REF} (5-V typical) is the reference of LM5036 device (96)

8.2.2.22 Full-Bridge Converter Applications

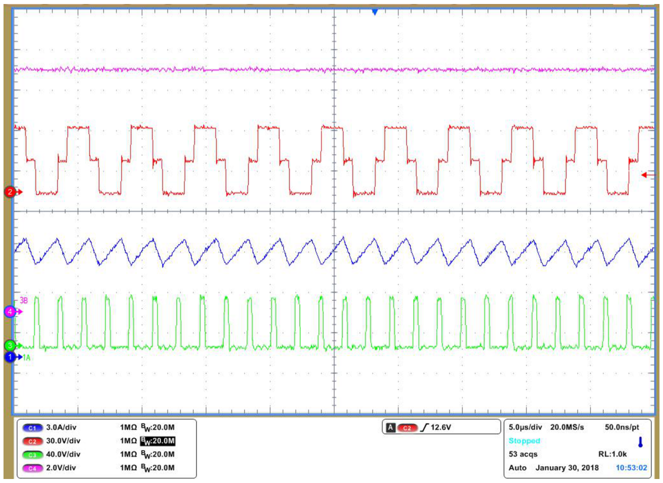
While LM5036 device is optimized for half-bridge applications, it can also be used for full-bridge applications. External gate drivers are needed to support an additional pair of FETs in full-bridge configuration. In addition, a DC-blocking capacitor is required to ensure voltage-second balance of the main transformer with the voltage-mode control of LM5036 device. Only one phase current information is needed for current protection in the full-bridge applications.

8.2.3 Application Curves



f_{SW} = 200-kHz V_O= 12 V

Figure 51. Efficiency



V_{IN} = 48-V V_O = 12-V
I_O = 8-A

Figure 52. Steady State Operation Waveform

9 Power Supply Recommendations

The power converter controlled by LM5036 device can have considerable current level. Care should be taken that components with the correct current rating are chosen. This includes magnetic components, power MOSFETS and diodes, connectors and wire sizes. Input and output capacitors should have the correct ripple current rating.

The recommended maximum input voltage for the VIN pin of LM5036 device is 100-V. The recommended voltage for the VCC pin is between 8.5-V and 14-V. Both VCC pin and REF pin must be locally decoupled with a ceramic capacitor. The recommended range of values is 0.47-µF to 10-µF for VCC pin, and 0.1-µF to 10-µF for REF pin. To reduce the power consumption of the internal VCC regulator, an external bias supply can be connected to VCC pin through a diode.

10 Layout

10.1 Layout Guidelines

- The two ground planes (AGND and PGND) of LM5036 device should be tied together with a short and direct connection to avoid jitter due to relative ground bounce. The connection point could be at the negative terminal of the input power supply.
- The VIN, VCC, REF pin capacitors, and CS_NEG resistor should be tied to PGND plane. UVLO, ON_OFF, RT, RON, RD1 and RD2 resistors, RAMP, RES, SS and SSSR capacitors, and the thermal pad should all be tied to AGND plane.
- SW and SW_AUX are switching nodes which switch rapidly between VIN and GND every cycle which are sources of high dv/dt noise. Therefore, large SW/SW_AUX node area should be avoided.
- The differential current sense signals at CS_POS and CS_NEG pins should be routed in parallel and close to each other to minimize the common-mode noise.
- The area of the loop formed by the main feedback control signal traces (COMP and REF) should be minimized in order to reduce the noise pick up. This can be accomplished by placing the COMP and REF signal traces on top of each other in adjacent PCB layers. In addition, the main feedback control signal traces should be routed away from the SW_AUX switching node to avoid high dv/dt noise coupling.
- The gate drive outputs (LSG and HSG) should have short and direct paths to the power MOSFETs to minimize parasitic inductance in the gate driving loop.
- The VCC and REF decoupling capacitors should be placed close to their respective pins with short trace inductance. Low ESR and ESL ceramic capacitors are recommended for the boot-strap, VCC and the REF capacitors.
- A decoupling capacitor should be placed close to the IC, directly across VIN and PGND pins. The connections to these two pins should be direct to minimize the loop area which carries switching currents.
- The boot-strap capacitors required for the high-side gate drivers of the half-bridge converter and auxiliary supply should be located close to the IC and connected directly to the BST/BST_AUX and SW/SW_AUX pins.
- The area of the switching loop of the power stage consisting of input capacitor, capacitive divider, transformer, and the primary MOSFETs should be minimized.

10.2 Layout Example

See 图 53 for an example layout that matches the schematic of Figure 39.

Layout Example (接下页)

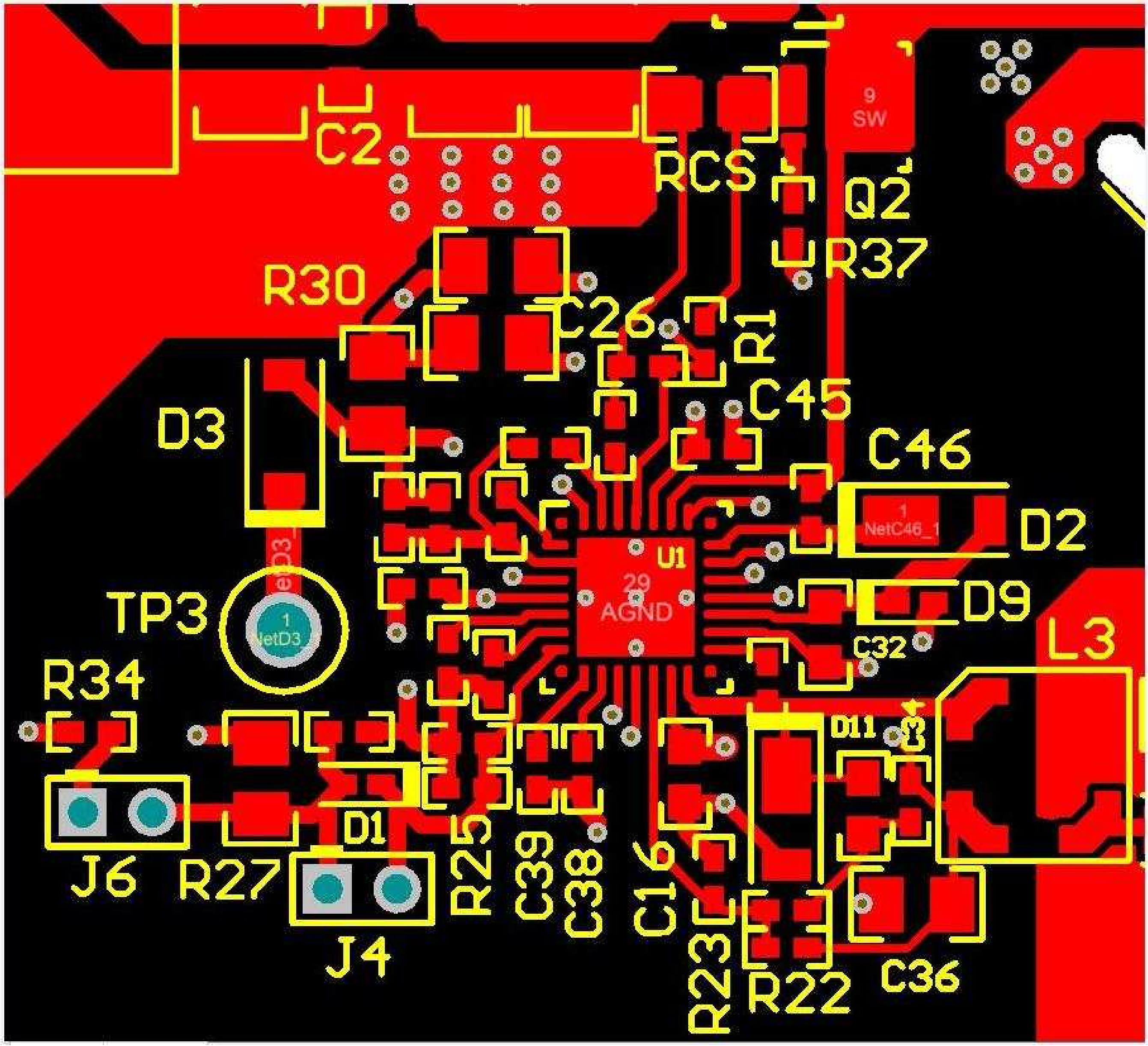


图 53. LM5036 PCB Layout Example

11 器件和文档支持

11.1 使用 WEBENCH® 工具创建定制设计

请单击此处，使用 LM5036 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5036RJBR	ACTIVE	WQFN	RJB	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5036	Samples
LM5036RJBT	ACTIVE	WQFN	RJB	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5036	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

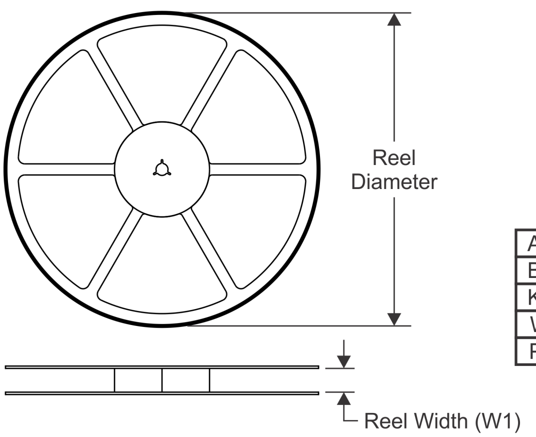
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

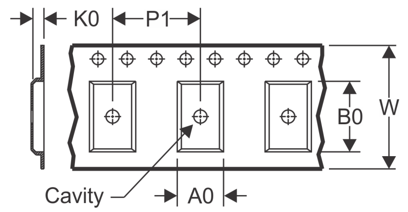
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

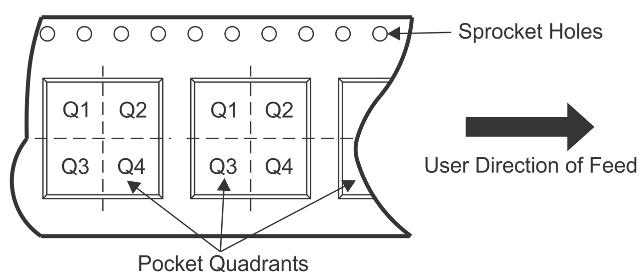
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





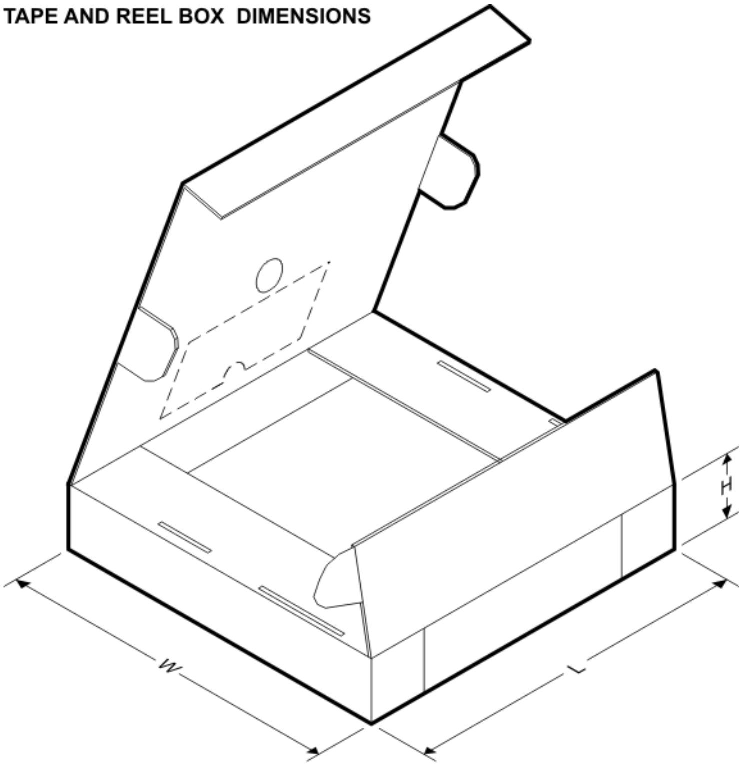
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

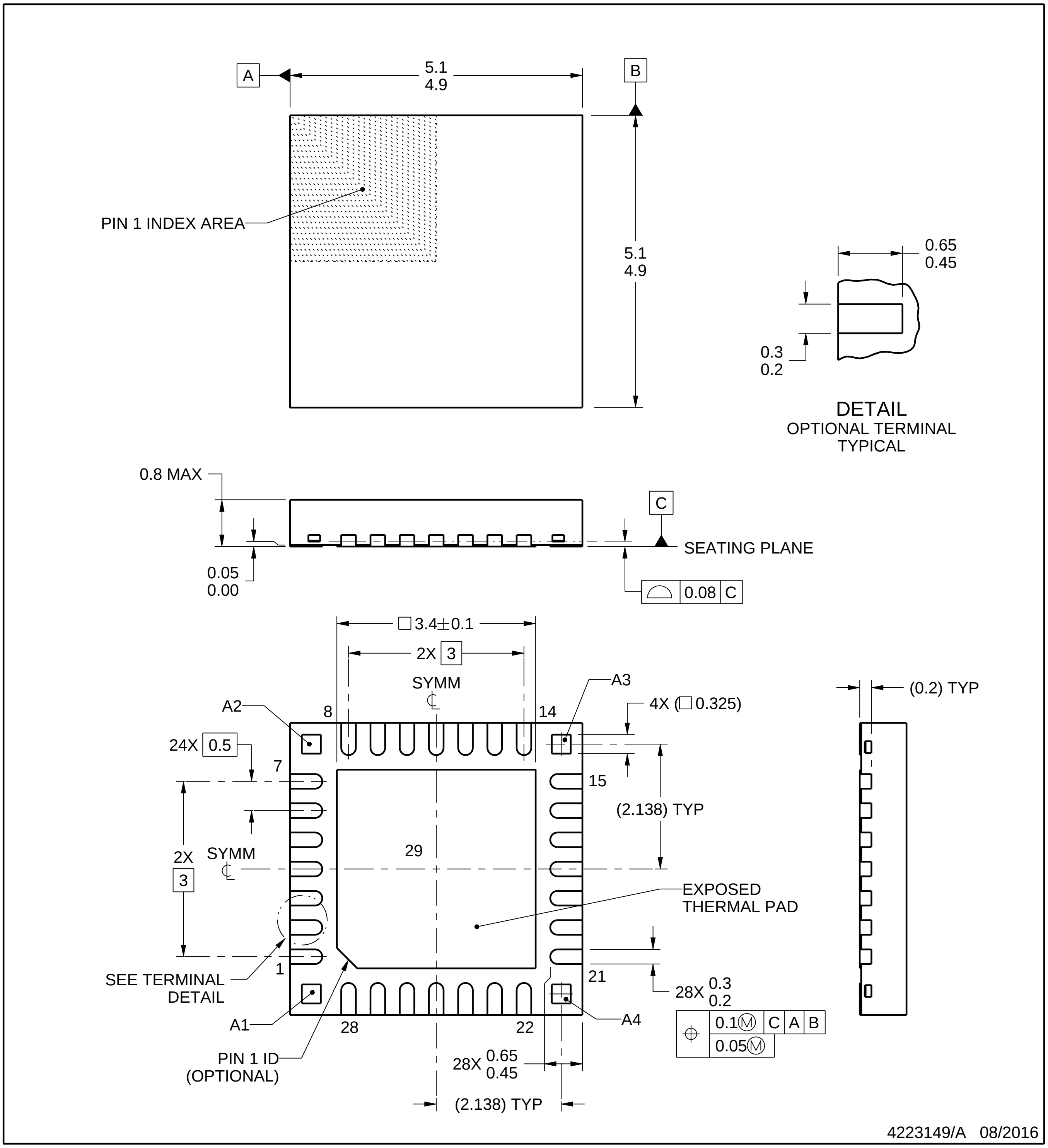
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5036RJBR	WQFN	RJB	28	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



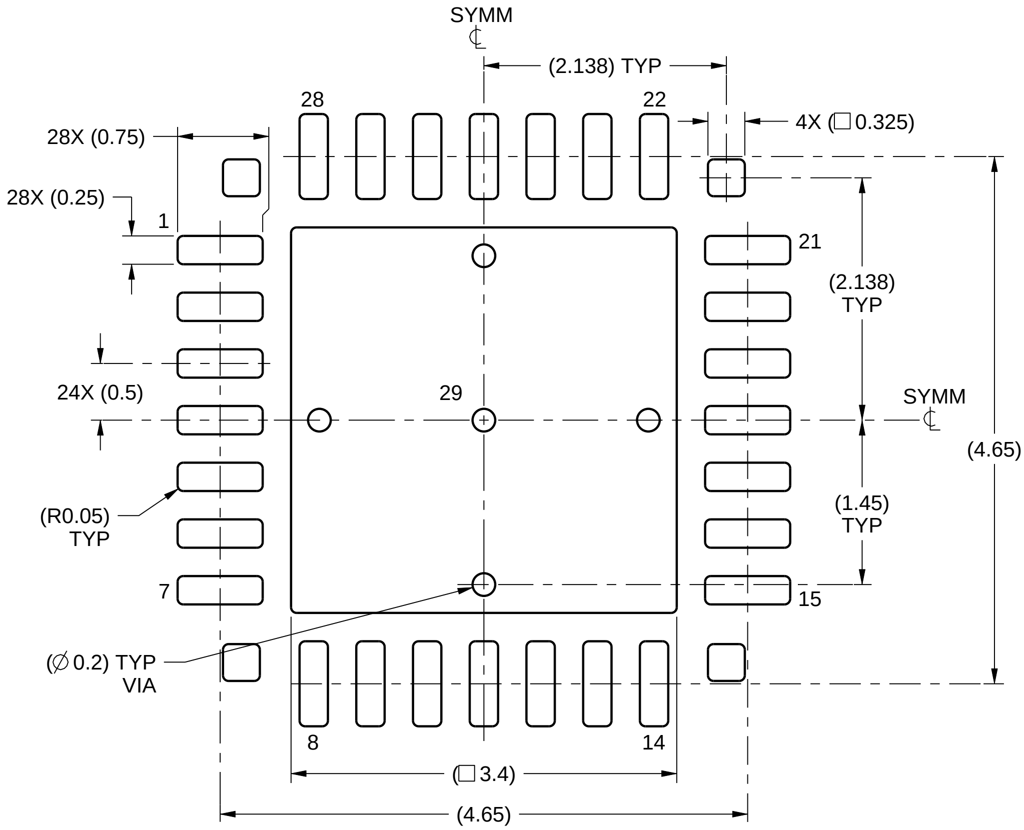
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5036RJBR	WQFN	RJB	28	3000	367.0	367.0	38.0

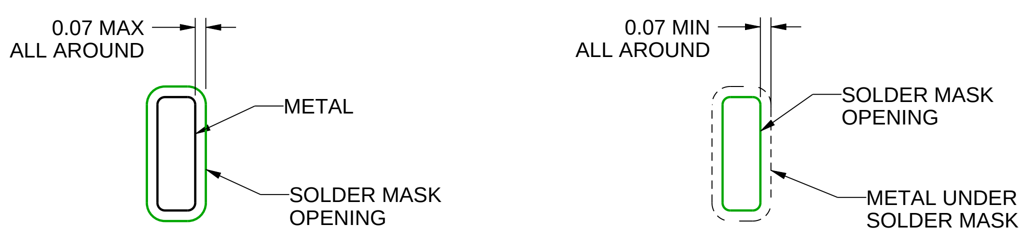


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

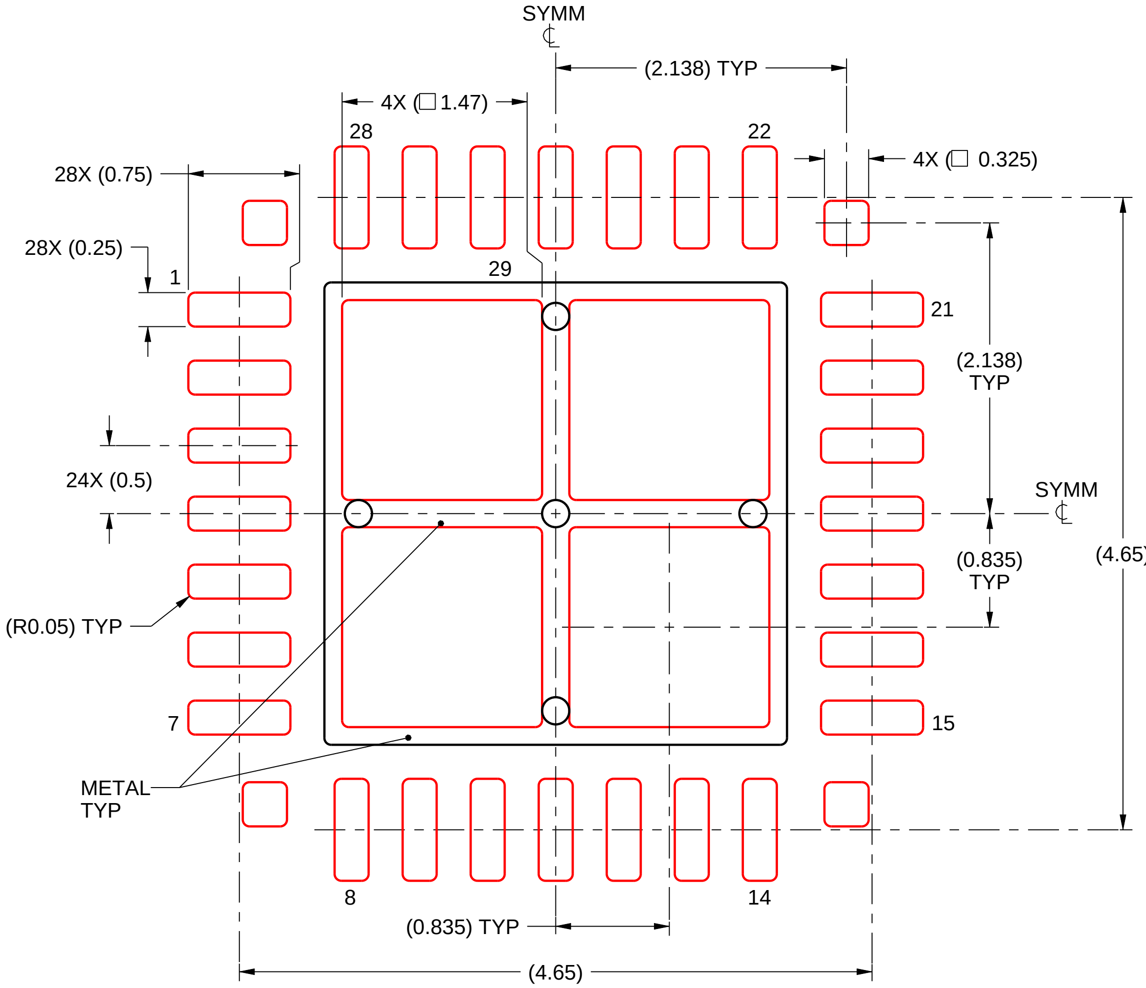
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4223149/A 08/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:18X

4223149/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122