SN74LVC4245A-EP
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

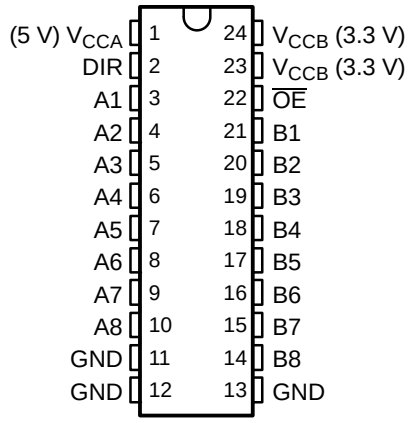
SCAS742–DECEMBER 2003–REVISED AUGUST 2005

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Bidirectional Voltage Translator**
- **5.5 V on A Port and 2.7 V to 3.6 V on B Port**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3 V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.

ORDERING INFORMATION

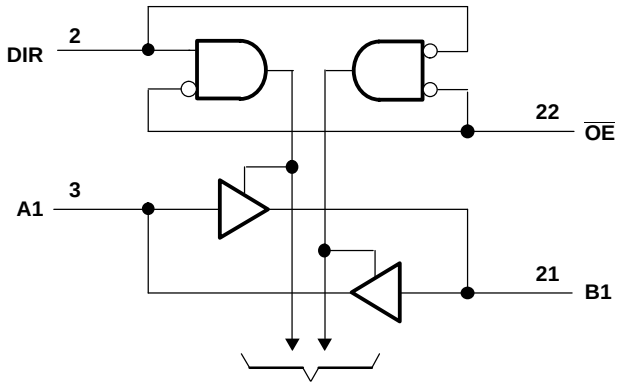
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Reel of 2000	SN74LVC4245AIPWREP	C4245AEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range	A port(2)	–0.5	V_{CCA} + 0.5	V
		Control inputs	–0.5	6	
V_O	Output voltage range	A port(2)	–0.5	V_{CCA} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)			88	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Absolute Maximum Ratings(1)

over operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range	B port(2)	–0.5	V_{CCB} + 0.5	V
V_O	Output voltage range	B port(2)	–0.5	V_{CCB} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCB} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)			88	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

for V_{CCA} = 4.5 V to 5.5 V

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CCA}	V
V_O	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions(1)

for V_{CCB} = 2.7 V to 3.6 V

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CCB}	V
V_O	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		–12	mA
		V_{CCB} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)

over recommended operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP(2)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		4.5 V	4.3			V
				5.5 V	5.3			
		I_{OH} = –24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL}		I_{OL} = 100 μA		4.5 V			0.2	V
				5.5 V			0.2	
		I_{OL} = 24 mA		4.5 V			0.55	
				5.5 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		5.5 V			±1	μA
I_{OZ}(3)	A port	$V_O = V_{CCA}$ or GND		5.5 V			±5	μA
I_{CCA}		$V_I = V_{CCA}$ or GND,	I_O = 0	5.5 V			80	μA
ΔI_{CCA}(4)		One input at 3.4 V,	Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND		Open		5		pF
C_{io}	A port	$V_O = V_{CCA}$ or GND		5 V		11		pF

(1) V_{CCB} = 2.7 V to 3.6 V
(2) All typical values are measured at V_{CC} = 5 V, T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.

Electrical Characteristics(1)

over recommended operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	TYP(2)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		2.7 V to 3.6 V	V_{CC} – 0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_{OZ}(3)	B port	$V_O = V_{CCB}$ or GND		3.6 V			±5	μA
I_{CCB}		$V_I = V_{CCB}$ or GND,	I_O = 0	3.6 V			50	μA
ΔI_{CCB}(4)		One input at V_{CCB} – 0.6 V,	Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{io}	B port	$V_O = V_{CCB}$ or GND		3.3 V		11		pF

(1) V_{CCA} = 5 V ± 0.5 V
(2) All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

Operating Characteristics

V_{CCA} = 4.5 V to 5.5 V, V_{CCB} = 2.7 V to 3.6 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0,	f = 10 MHz	39.5	pF
		Outputs disabled			5	

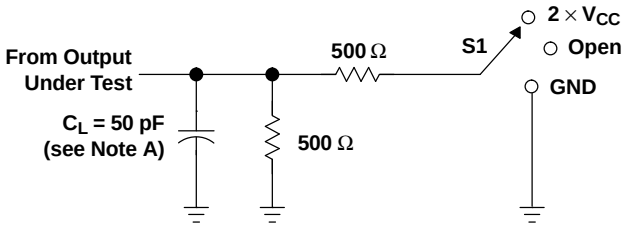
Power-up Considerations(1)

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

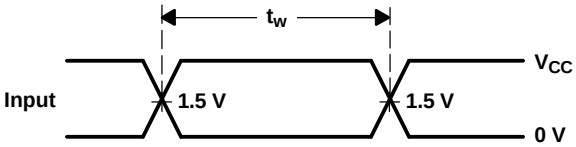
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION
A PORT

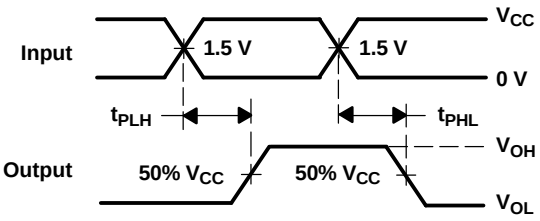


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

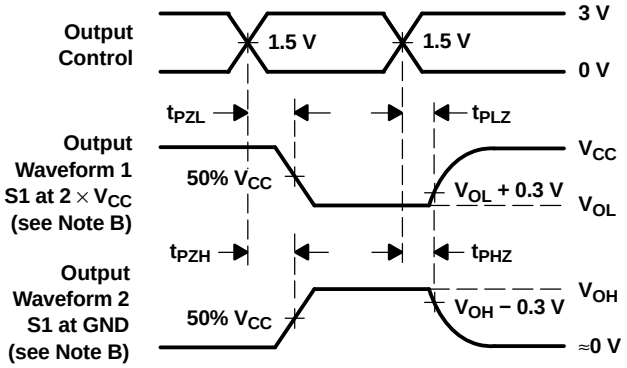
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

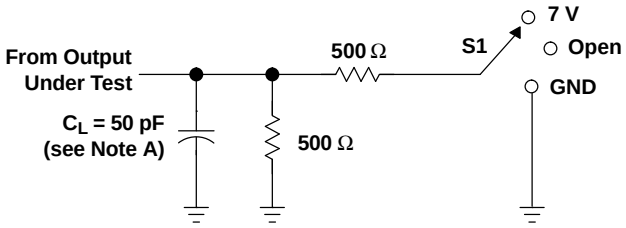


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

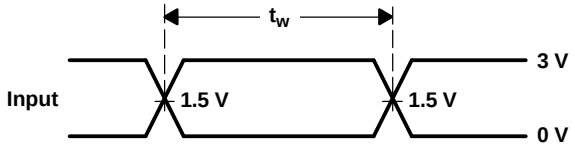
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
B PORT

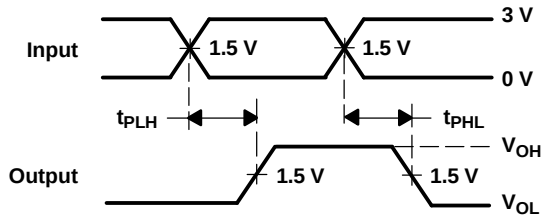


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

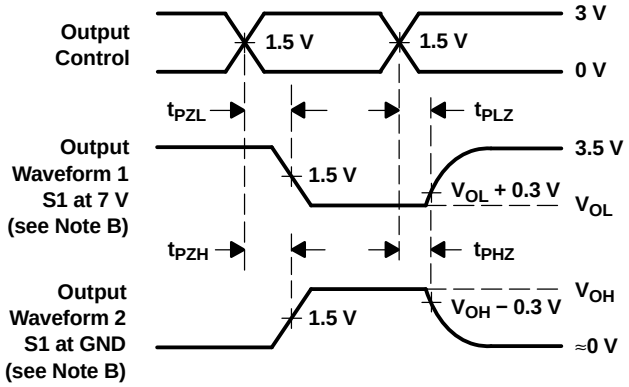
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
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C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC4245AIPWREP	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4245AEP	Samples
V62/04664-01XE	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4245AEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC4245A-EP :

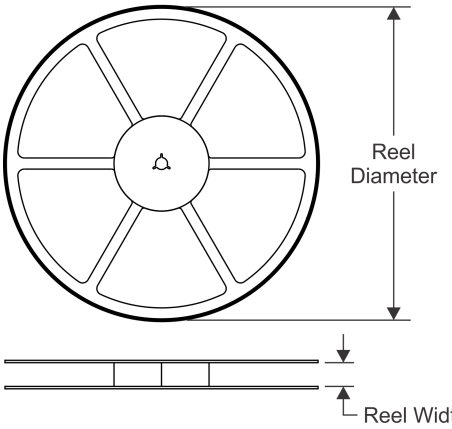
- Catalog: SN74LVC4245A

NOTE: Qualified Version Definitions:

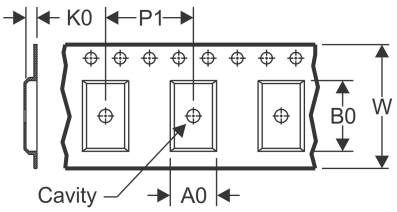
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

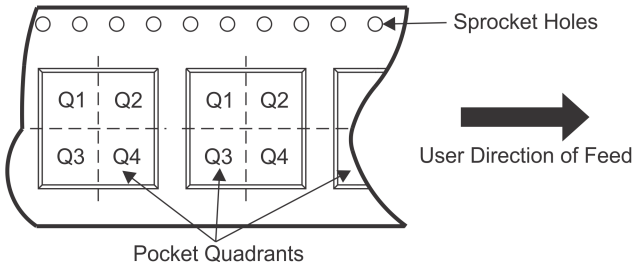


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

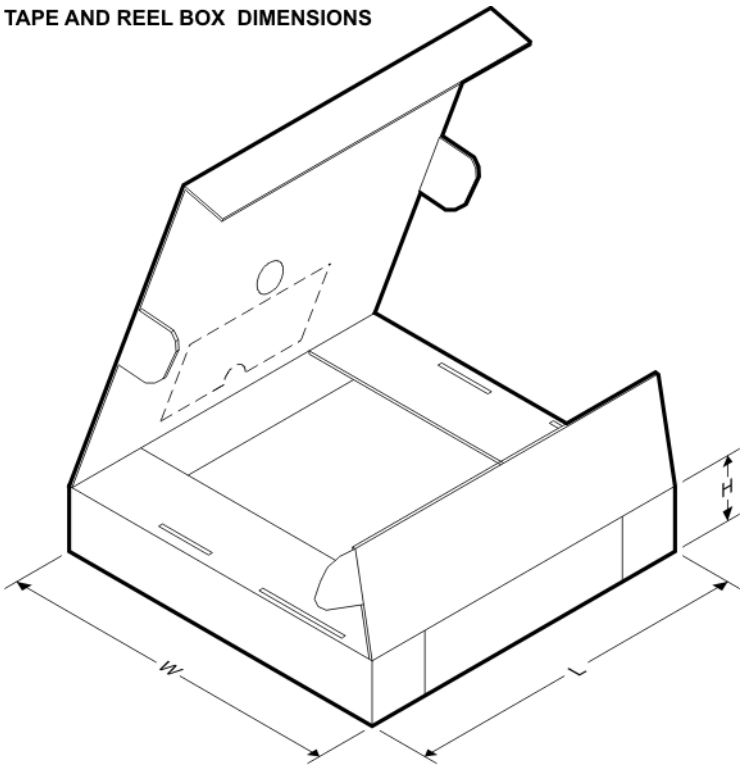
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC4245AIPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

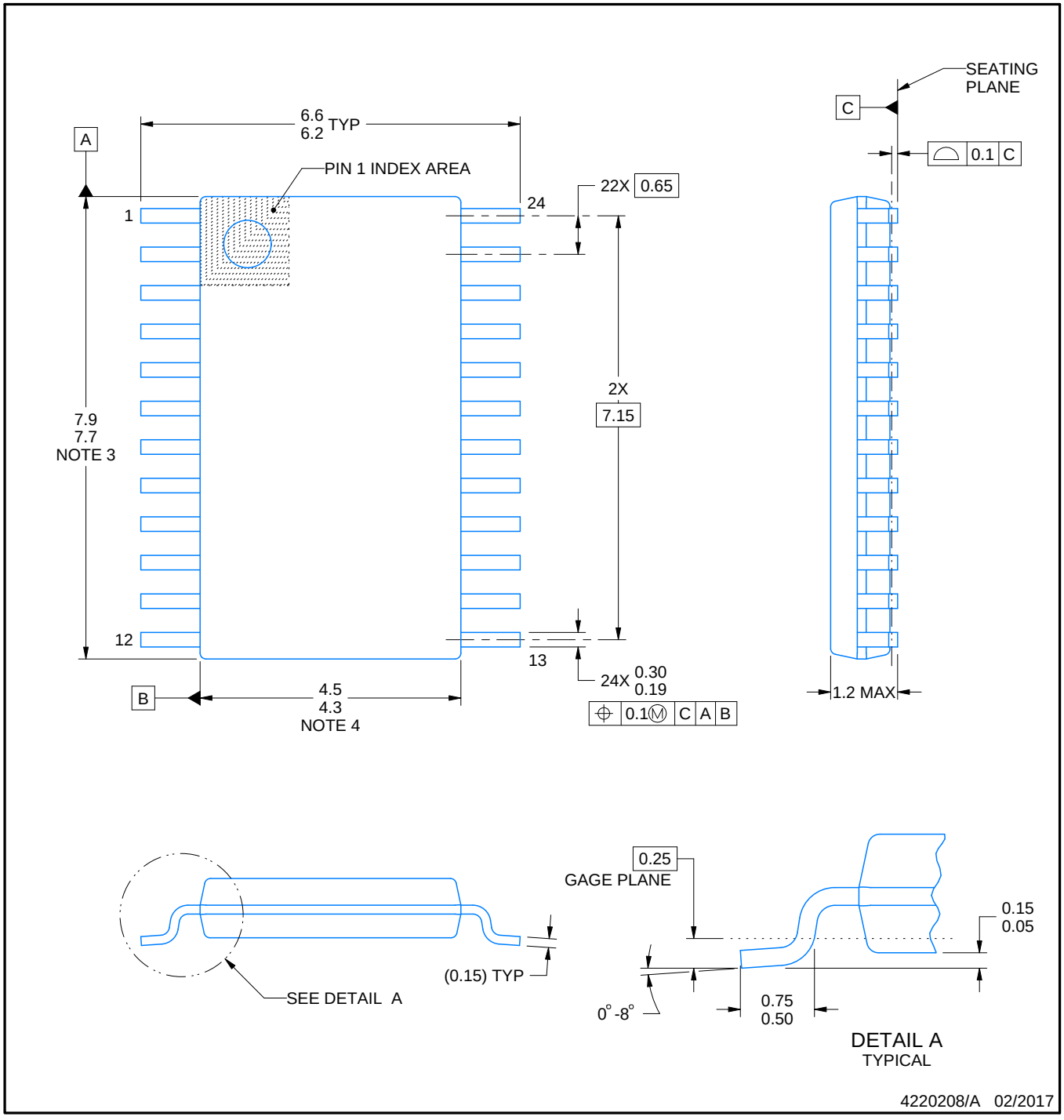
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC4245AIPWREP	TSSOP	PW	24	2000	853.0	449.0	35.0

PACKAGE OUTLINE

PW0024A

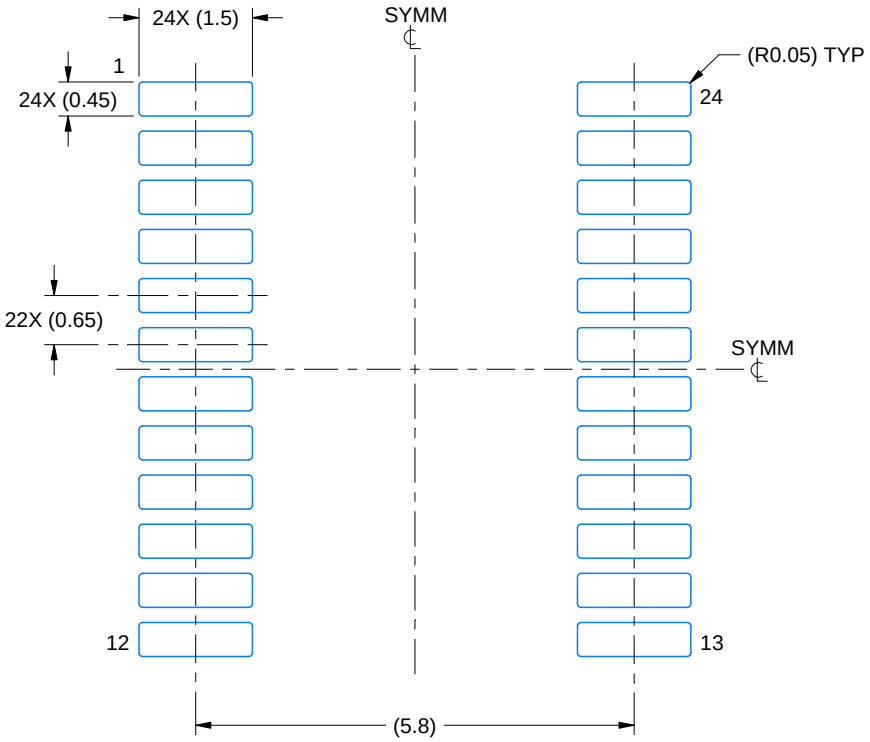
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

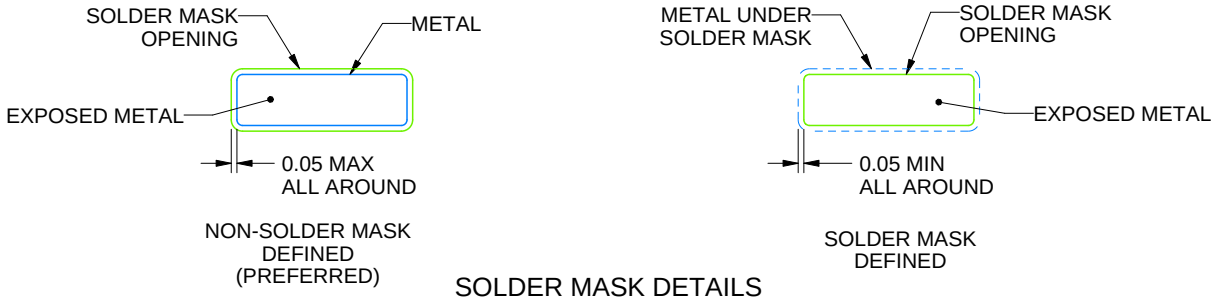


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

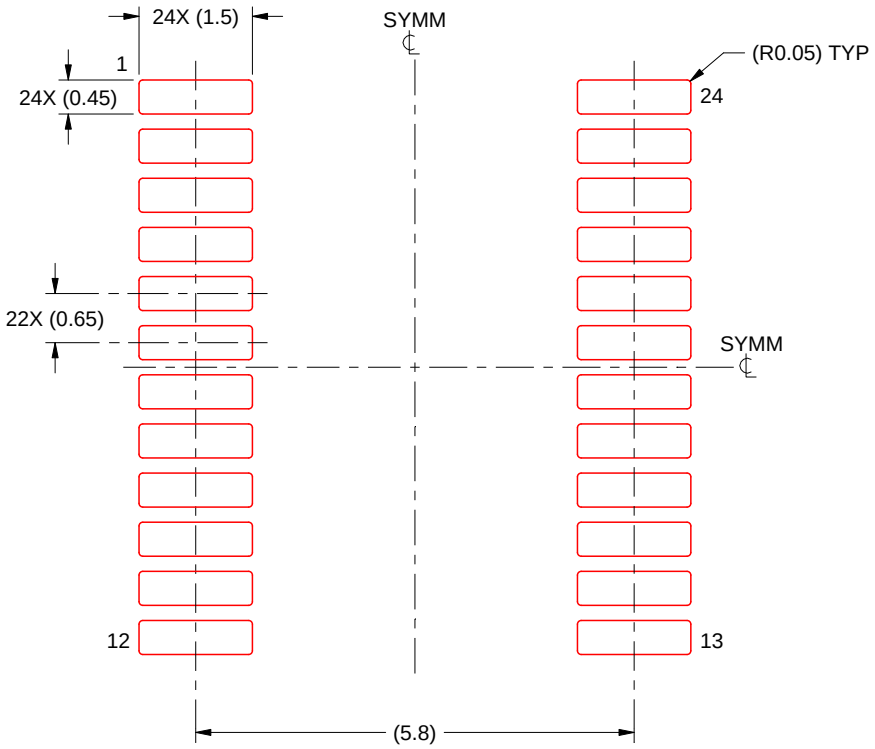


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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