通过汽车认证的 LSF0204-Q1 4 位自动双向多电压电平转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C ≤ T_A ≤ 125°C
  - 器件 HBM ESD 分类等级 2
  - CDM ESD 分类等级 C6
- 可在无方向引脚的情况下提供自动双向电压转换
- 支持漏极开路或推挽 应用 ，如 I^2C、I2S、SPI、UART、JTAG、MDIO、SDIO 和 GPIO
- 在不超过 30pF 的容性负载条件下支持最高达 100MHz 的上行转换和超过 100MHz 的下行转换 ，在 50pF 的容性负载条件下支持高达 40MHz 的上行/下行转换
- 支持 I_{off} 局部断电模式（请参阅*特性 说明*）
- 可实现以下电压之间的双向电压电平转换
  - 0.95V ↔ 1.8、2.5、3.3、5.5V
  - 1.2V ↔ 1.8、2.5、3.3、5.5V
  - 1.8V ↔ 2.5、3.3、5.5V
  - 2.5V ↔ 3.3、5.5V
  - 3.3V ↔ 5.5V
- I/O 端口可耐受 5V 电压
- 低 R_{on} 可实现更佳的信号完整性
- 采用直通引脚排列以简化 PCB 布线
- 闩锁性能超过 100mA，符合 JESD17 规范

2 应用

- I2S、JTAG、SPI、SDIO、UART、I^2C、MDIO、PMBus、SMBus 和其他接口
- 信息娱乐系统音响主机
- 图形群集
- ADAS 融合
- ADAS 前置摄像头
- HEV 电池管理系统

3 说明

LSF0204-Q1 是一款通过汽车认证的四通道自动双向电压转换器，可在 0.8V 至 4.5V (Vref_A) 和 1.8V 至 5.5V (Vref_B) 电压范围内运行。该范围支持在 0.8 至 5V 之间进行双向电压转换，而无须使用方向引脚。

当 An 或 Bn 端口为低电平时，此开关处于接通状态，并且在 An 和 Bn 端口之间存在一个低电阻连接。此开关具有低导通电阻，可以在最短传播延迟和最小信号失真情况下建立连接。A 侧或 B 侧上的电压将低于 Vref_A，且可上拉至 Vref_A 到 5.5V 之间的任何电平

您可以使用上拉电阻器单独设置每个通道的电源电压 (V_{PUn})。例如，CH1 可用于上行转换模式 (1.2V ↔ 3.3V)，CH2 可用于下行转换模式 (2.5V ↔ 1.8V)。

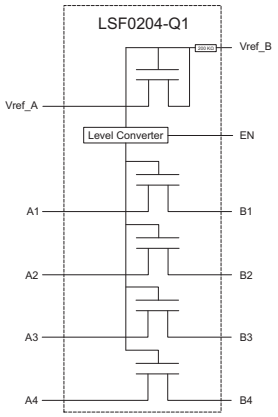
当 EN 为高电平时，转换器开关打开，并且 An I/O 被分别连接至 Bn I/O，从而实现端口间的双向数据流。当 EN 为低电平时，转换器开关关闭，在端口之间存在一个高阻抗状态。EN 输入电路被设计成由 Vref_A 供电。EN 必须为低电平，以确保上电或断电期间的高阻抗状态。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
LSF0204QPWRQ1	TSSOP (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.8 V) ... 6
6.7 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.2 V) ... 6
6.8 Switching Characteristics: AC Performance (Translating Up, 1.8 V to 3.3 V) ... 7
6.9 Switching Characteristics: AC Performance (Translating Up, 1.2 V to 1.8 V) ... 7
6.10 Typical Characteristics ... 7
7 **Parameter Measurement Information** ... 8
7.1 Load Circuit AC Waveform for Outputs ... 9
8 **Detailed Description** ... 10
8.1 Overview ... 10
8.2 Functional Block Diagram ... 10
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 11
9 **Application and Implementation** ... 12
9.1 Application Information ... 12
9.2 Typical Applications ... 12
10 **Power Supply Recommendations** ... 16
11 **Layout** ... 16
11.1 Layout Guidelines ... 16
11.2 Layout Example ... 16
12 器件和文档支持 ... 17
12.1 文档支持 ... 17
12.2 社区资源 ... 17
12.3 商标 ... 17
12.4 静电放电警告 ... 17
12.5 术语表 ... 17
13 机械、封装和可订购信息 ... 17

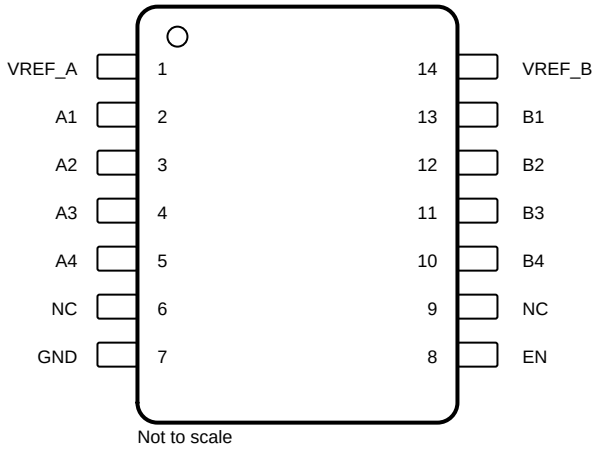
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2018) to Revision A	Page
• 已更改 产品状态从“预告信息”改为“生产数据”	1

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions 2

PIN		I/O	DESCRIPTION
NAME	NO.		
VREF_A	1	--	Reference supply voltage; see Application and Implementation section
A1	2	I/O	Input/output 1.
A2	3	I/O	Input/output 2.
A3	4	I/O	Input/output 3.
A4	5	I/O	Input/output 4.
NC	6	--	No connection. Not internally connected.
GND	7	--	Ground
EN	8	I	Translation enable input, EN is active-high
NC	9	--	No connection. Not internally connected.
B4	10	I/O	Input/output 4.
B3	11	I/O	Input/output 3.
B2	12	I/O	Input/output 2.
B1	13	I/O	Input/output 1.
VREF_B	14	--	Reference supply voltage; see Application and Implementation section

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage, V_I (2)		–0.5	7	V
Input and output voltage, $V_{I/O}$ (2)		–0.5	7	V
Continuous channel current			128	mA
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-001	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
$V_{ref\_A/B/EN}$	Reference voltage	0	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LSF0204-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.9	°C
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.3	°C
$R_{\theta JB}$	Junction-to-board thermal resistance	100.0	°C
ψ_{JT}	Junction-to-top characterization parameter	22.9	°C
ψ_{JB}	Junction-to-board characterization parameter	99.0	°C
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C

(1) For more information about traditional and new thermal metrics, refer to the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA, V_{EN} = 0				–1.2	V
I_{IH}	I/O input high leakage	V_I = 5 V, V_{EN} = 0				5.0	µA
I_{CCBA}	Leakage from Vref_B to Vref_A	V_{ref_B} = 3.3 V, V_{ref_A} = 1.8 V, V_{EN} = V_{ref_A} I_O = 0, V_I = 3.3 V or GND				3.5	µA
I_{CCA} + I_{CCB} (2)	Total Current through GND	V_{ref_B} = 3.3 V, V_{ref_A} = 1.8 V, V_{EN} = V_{ref_A} I_O = 0, V_I = 3.3 V or GND			0.2		µA
I_{IN}	Control pin current	V_{ref_B} = 5.5 V, V_{ref_A} = 4.5 V, V_{EN} = 0 to V_{ref_A} I_O = 0				±1	µA
I_{off}	Power Off Leakage Current	V_{ref_B} = V_{ref_A} = 0 V, V_{EN} = GND I_O = 0, V_I = 5 V or GND				±1	µA
$C_{I(ref\_A/B/EN)}$	Input capacitance	V_I = 3 V or 0			7		pF
$C_{io(off)}$	I/O pin off-state capacitance	V_O = 3 V or 0, VEN = 0			5.0	6.0	pF
$C_{io(on)}$	I/O pin on-state capacitance	V_O = 3 V or 0, VEN = Vref_A			10.5	13	pF
$V_{IH\ (EN\ pin)}$	High-level input voltage	V_{ref_A} = 1.5 V to 4.5 V		0.7×Vref_A			V
$V_{IL\ (EN\ pin)}$	Low-level input voltage	V_{ref_A} = 1.5 V to 4.5 V				0.3×Vref_A	V
$V_{IH\ (EN\ pin)}$	High-level input voltage	V_{ref_A}= 1.0 V to 1.5 V		0.8×Vref_A			V
$V_{IL\ (EN\ pin)}$	Low-level input voltage	V_{ref_A} = 1.0 V to 1.5 V				0.3×Vref_A	V
Δt/Δv (EN pin)	Input transition rise or fall rate for EN pin				10		ns/V
r_{on} (3)	On-state resistance	V_I = 0, I_O = 64 mA	V_{ref_A} = V_{EN} = 3.3 V; V_{ref_B} = 5 V		3		Ω
			V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 5 V		4		
		V_I = 0, I_O = 32 mA	V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 5 V		9		Ω
			V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 5 V		4		
		V_I = 0, I_O = 32 mA , V_{ref_A} = V_{EN} = 2.5 V; V_{ref_B} = 5 V			10		Ω
		V_I = 1.8 V, I_O = 15 mA, V_{ref_A} = V_{EN} = 3.3 V; V_{ref_B} = 5 V			5		Ω
		V_I = 1.0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.8 V; V_{ref_B} = 3.3 V			8		Ω
		V_I = 0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 3.3 V			6		Ω
		V_I = 0 V, I_O = 10 mA, V_{ref_A} = V_{EN} = 1.0 V; V_{ref_B} = 1.8 V			6		Ω

(1) All typical values are at T_A = 25°C.
(2) The actual supply current for LSF0204 is I_{CCA} + I_{CCB}; the leakage from Vref_B to Vref_A can be measured on Vref_A and Vref_B pin
(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

6.6 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.8 V)

over recommended operating free-air temperature range, V_{rev-A} = 1.8 V, V_{rev-B} = 3.3 V, V_{EN} = 1.8 V, Vpu_1 = 3.3 V, Vpu_2 = 1.8 V, R_L = NA, V_{IH} = 3.3 V, V_{IL} = 0 V_M = 1.15 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time (low-to-high output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		0.7	5.49	ns
			C_L = 30 pF		0.5	5.29	
			C_L = 15 pF		0.3	5.19	
t_{PHL}	Propagation delay time (high-to-low output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		0.9	4.9	ns
			C_L = 30 pF		0.7	4.7	
			C_L = 15 pF		0.5	4.5	
t_{PLZ}	Disable time (from low level)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		13	18	ns
			C_L = 30 pF		12	16.5	
			C_L = 15 pF		11	15	
t_{PZL}	Disable time	(Input) A or B-to-B or A (Output)	C_L = 50 pF		33	45	ns
			C_L = 30 pF		30	40	
			C_L = 15 pF		23	37	
f_{MAX}	Maximum time	(Input) A or B-to-B or A (Output)	C_L = 50 pF		50		MHz
			C_L = 30 pF		100		
			C_L = 15 pF		100		

6.7 Switching Characteristics: AC Performance (Translating Down, 3.3 V to 1.2 V)

over recommended operating free-air temperature range V_{rev-A} = 1.2 V, V_{rev-B} = 3.3 V, V_{EN} = 1.2 V, Vpu_1 = 3.3 V, Vpu_2 = 1.2 V, R_L = NA, V_{IH} = 3.3V, V_{IL} = 0 V_M = 0.85 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time (low-to-high output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		0.8	4.1	ns
			C_L = 30 pF		0.5	3.9	
			C_L = 15 pF		0.3	3.8	
t_{PHL}	Propagation delay time (high-to-low output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		0.9	4.7	ns
			C_L = 30 pF		0.7	4.5	
			C_L = 15 pF		0.6	4.3	
f_{MAX}	Maximum time	(Input) A or B-to-B or A (Output)	C_L = 50 pF		50		MHz
			C_L = 30 pF		100		
			C_L = 15 pF		100		

6.8 Switching Characteristics: AC Performance (Translating Up, 1.8 V to 3.3 V)

over recommended operating free-air temperature range V_{rev-A} = 1.8 V, V_{rev-B} = 3.3 V, V_{EN} = 1.8 V, Vpu_1 = 3.3 V, Vpu_2 = 1.8V, R_L = 500 Ω, V_{IH} = 1.8V, $_{VIL}$ = 0 V_M = 0.9V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time (low-to-high output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		0.6	5.7	ns
			C_L = 30 pF		0.4	5.3	
			C_L = 15 pF		0.2	5.13	
t_{PHL}	Propagation delay time (high-to-low output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		1.3	6.7	ns
			C_L = 30 pF		1	6.4	
			C_L = 15 pF		0.7	5.3	
t_{PLZ}	Disable time (from low level)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		13	18	ns
			C_L = 30 pF		12	16.5	
			C_L = 15 pF		11	15	
t_{PZL}	Disable time	(Input) A or B-to-B or A (Output)	C_L = 50 pF		33	45	ns
			C_L = 30 pF		30	40	
			C_L = 15 pF		23	37	
f_{MAX}	Maximum time	(Input) A or B-to-B or A (Output)	C_L = 50 pF		50		MHz
			C_L = 30 pF		100		
			C_L = 15 pF		100		

6.9 Switching Characteristics: AC Performance (Translating Up, 1.2 V to 1.8 V)

over recommended operating free-air temperature range, V_{rev-A} = 1.2 V, V_{rev-B} = 1.8 V, V_{EN} = 1.2 V, Vpu_1 = 1.8 V, Vpu_2 = 1.2 V, R_L = 500 Ω, V_{IH} = 1.2V, V_{IL} = 0 V_M = 0.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time (low-to-high output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		0.65	7.25	ns
			C_L = 30 pF		0.4	7.05	
			C_L = 15 pF		0.2	6.85	
t_{PHL}	Propagation delay time (high-to-low output)	(Input) A or B-to-B or A (Output)	C_L = 50 pF		1.6	7.03	ns
			C_L = 30 pF		1.3	6.5	
			C_L = 15 pF		1	5.4	
f_{MAX}	Maximum time	(Input) A or B-to-B or A (Output)	C_L = 50 pF		50		MHz
			C_L = 30 pF		100		
			C_L = 15 pF		100		

6.10 Typical Characteristics

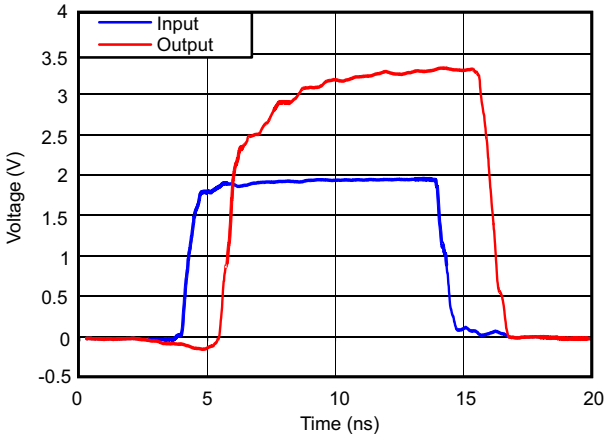
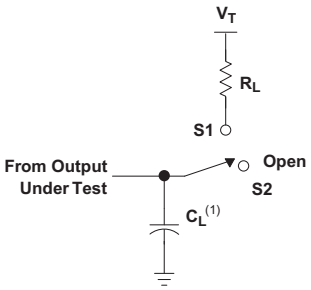


图 1. Signal Integrity (1.8 V to 3.3 V Translation Up at 50 MHz)

7 Parameter Measurement Information

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10 MHz
- Z_O = 50 Ω
- T_r ≤ 2 ns
- T_f ≤ 2 ns



(1) C_L includes probe and jig capacitance.

图 2. Load Circuit for Outputs

USAGE	SWITCH
Translating up	S1
Translating down	S2

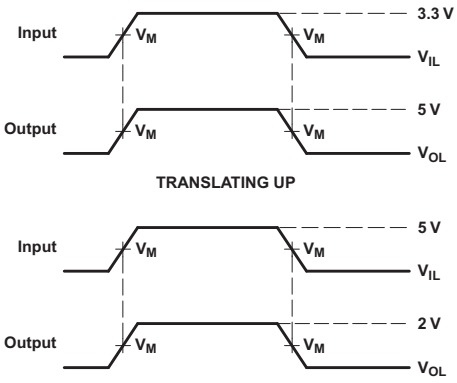


图 3. Translating Down

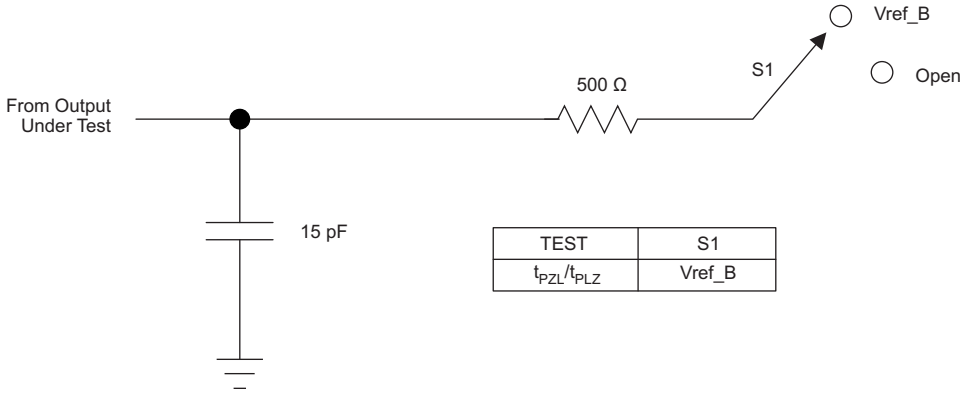


图 4. Load Circuit for Enable/Disable Time Measurement

Parameter Measurement Information (接下页)

7.1 Load Circuit AC Waveform for Outputs

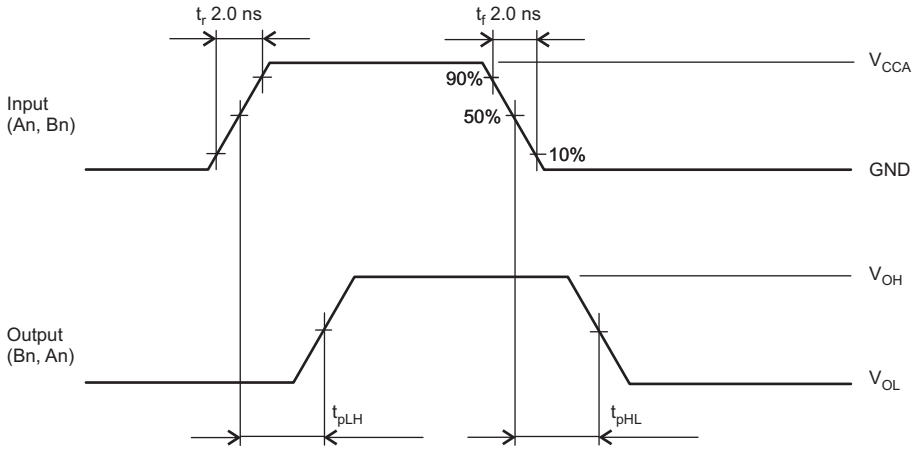


图 5. t_{PLH}, t_{PHL}

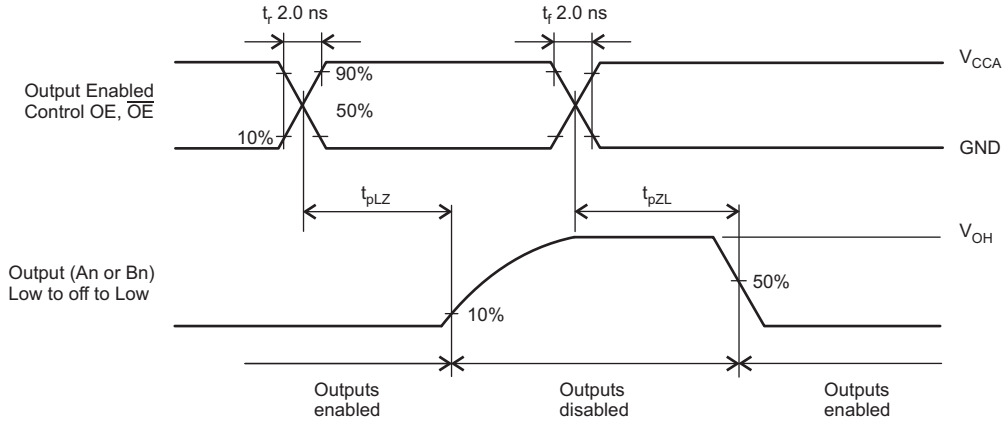


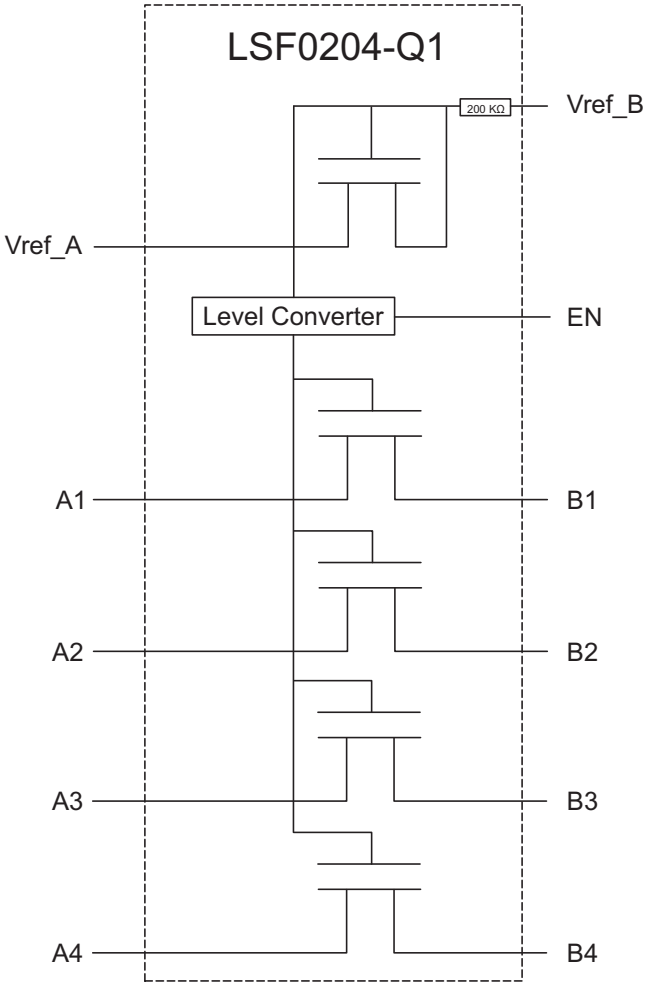
图 6. t_{PLZ}, t_{PZL}

8 Detailed Description

8.1 Overview

The LSF0204-Q1 may be used in level translation applications for interfacing devices or systems operating at different interface voltages. The LSF0204-Q1 is ideal for use in applications where an open-drain driver is connected to the data I/Os. LSF0204-Q1 can achieve 100 MHz data rate with the appropriate pull-up resistors and layout design. The LSF0204-Q1 can also be used in applications where a push-pull driver is connected to the data I/Os.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto-Bidirectional Voltage Translation Without DIR Pin Terminal

The LSF0204-Q1 device is an auto bidirectional voltage level translator that operates from 0.95 V to 4.5 V on Vref_A and 1.8 V to 5.5 V on Vref_B. This allows bidirectional voltage translation between 0.95 V and 5.5 V without the need for a direction pin in open-drain or push-pull applications.

8.3.2 Support Multiple High Speed Translation Interfaces

The LSF0204-Q1 device is able to perform voltage translation for open-drain interfaces such as I2C, MDIO, SMBUS, and PMBUS or push-pull interfaces such as I2S, SPI, UART, SDIO, and GPIO. The LSF0204-Q1 device supports level translation applications with transmission speeds greater than 100 MHz using a 200-Ω pullup resistor with a 15-pF capacitive load. See the *Down Translation with the LSF family* and *Up Translation with the LSF family* videos.

8.3.3 5-V Tolerance on IO Port and 125°C Support

The LSF0204-Q1, provides up to 5-V over-voltage tolerance on each of its IO channels. The device operating ambient temperature from –40°C to 125°C is critical in supporting automotive applications.

8.3.4 Channel Specific Translation

The LSF0204-Q1 can work as multi-voltage level translator using specific pullup voltage (Vpu) on each IO channel. Watch the *Multi-Voltage Translation with the LSF Family video*.

8.3.5 Ioff, Partial Power Down Mode

When V_{ref_A} or V_{ref_B} = 0, all the data IO pins are in high impedance.

EN logic circuit is referenced to V_{ref_A} supply. No power sequence is required to enable and operate LSF0204-Q1.

8.4 Device Functional Modes

表 1 lists the device functional modes of the LSF0204-Q1 device.

表 1. Function Table

INPUT EN(1) TERMINAL	FUNCTION
H	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_A} logic levels.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

LSF0204-Q1 performs voltage translation for open-drain or push-pull interface. 表 2 provides examples of interfaces as reference in regards to the different channel numbers that are supported by the LSF0204-Q1.

表 2. Voltage Translator by Interface

PART NAME	CHANNEL NUMBER	INTERFACE
LSF0204-Q1	4	Open Drain : I^2C, MDIO, SMBus, PMBus, GPIO
		Push Pull: GPIO, SPI, I2S, UART, JTAG, SD

9.2 Typical Applications

9.2.1 I^2C, PMBus, SMBus, GPIO Application

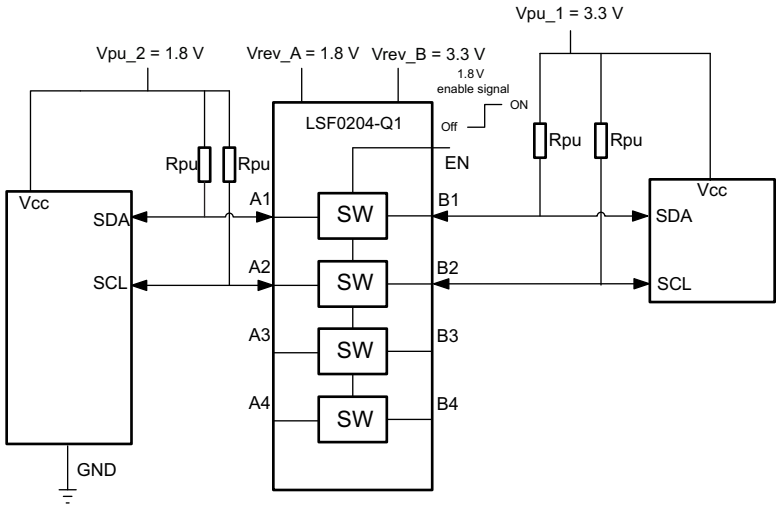


图 7. Bidirectional Translation to Multiple Voltage Levels

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF0204-Q1 has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF0204-Q1 is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF0204-Q1 for bidirectional application (I2C, SMBus, PMBus, or MDIO).

Typical Applications (接下页)

表 3. Application Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Vref_A	Reference voltage (A)	0.8		4.5	V
Vref_B	Reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$ (1)	Input voltage on EN terminal	0		Vref_A	V
Vpu	Pull-up supply voltage	0		Vref_B	V

(1) Refer V_{IH} and V_{IL} for $V_{I(EN)}$

Vref_B is recommended to be 1.0 V higher than Vref_A for best signal integrity.

The LSF0204-Q1 device enables multi-voltage translation by using the desired pull up voltage on each of the channels.

注

Vref_A must be set as lowest voltage level while using the device in multi-voltage translation application.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

The master output driver may be push-pull (pull-up resistors may be required) or open-drain (pull-up resistors required) and the slave device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

注

However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

In 图 7, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through to a 3.3 V Vpu power supply, and Vref_A is set 1.0V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to Vpu.

9.2.1.2.1.1 Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pull-up resistor value use 公式 1.

$$Rpu = (Vpu – 0.35\ V) / 0.015\ A \quad (1)$$

表 4 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF0204-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the LSF0204-Q1 device.

The LSF0204-Q1 does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the LSF0204-Q1 is being driven by standard CMOS totem pole output driver. Best practice is to minimize the trace length from the LSF0204-Q1 on the sink side (1.8 V) to minimize signal degradation.

表 4. Pullup Resistor Values(1)(2)

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA		10mA		3 mA	
	NOMINAL	+10%(3)	NOMINAL	+10%(3)	NOMINAL	+10%(3)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.3 Application Curve

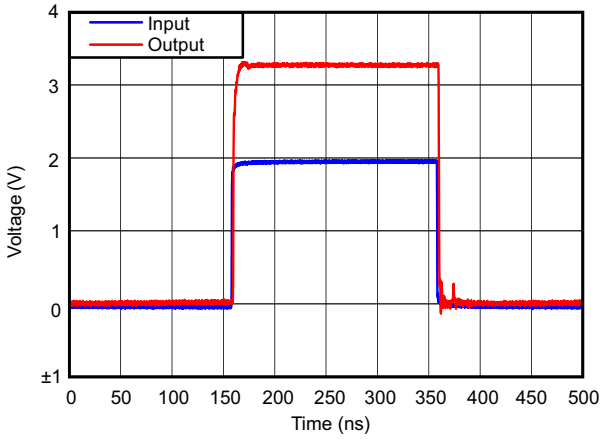


图 8. Captured Waveform From Above I²C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

9.2.2 MDIO Application

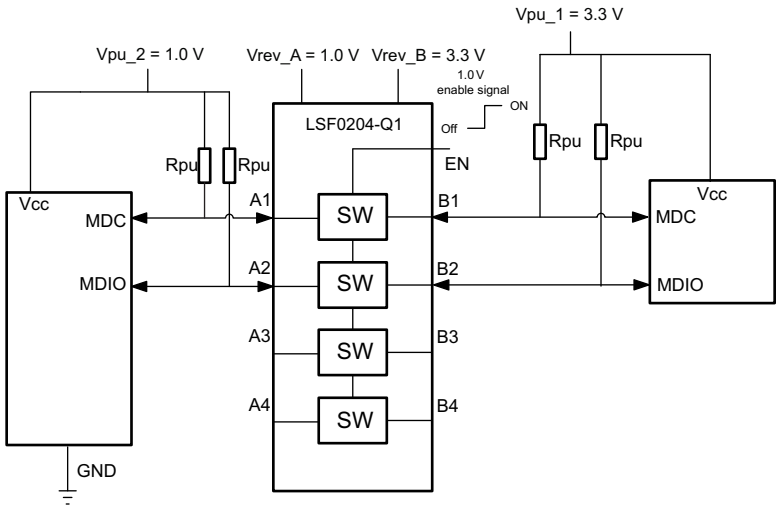


图 9. Typical Application Circuit (MDIO/Bidirectional Interface)

9.2.2.1 Design Requirements

See the *Design Requirements*.

9.2.2.2 Detailed Design Procedure

See the *Detailed Design Procedure*.

9.2.3 Multiple Voltage Translation in Single Device, Application

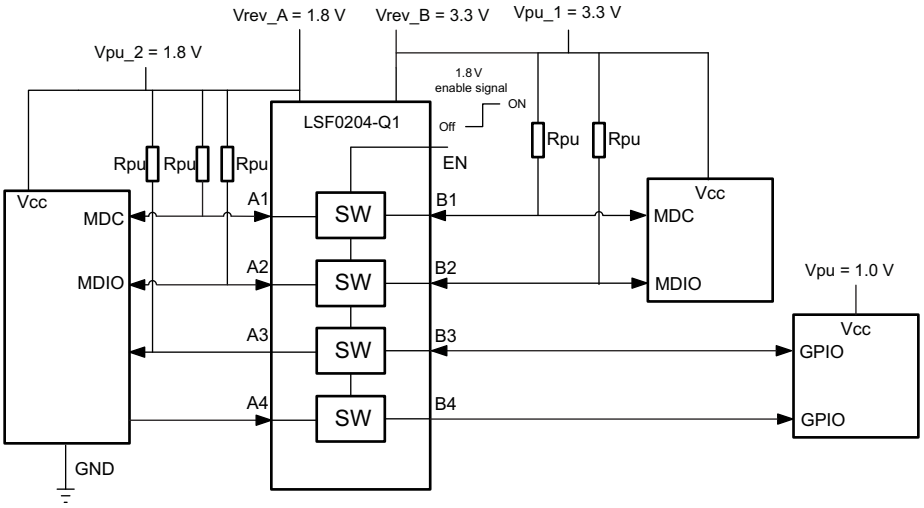


图 10. Bidirectional Translation to Multiple voltage levels

9.2.3.1 Design Requirements

See the *Design Requirements*.

9.2.3.2 Detailed Design Procedure

See the *Detailed Design Procedure*.

10 Power Supply Recommendations

There are no power sequence requirements for the LSF0204-Q1. See *表 3* for recommended operating voltages for all supply and input pins.

11 Layout

11.1 Layout Guidelines

The signal integrity of the switch-type based LSF0204-Q1 level translator is dependent on the pull-up resistor and the PCB board parasitic capacitance. Consider the following recommendations when designing with the LSF0204-Q1:

- Minimize the trace length to reduce the parasitic capacitance
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region
- Minimize stubs on the signal path
- Place the LSF0204-Q1 device near the high voltage side

11.2 Layout Example

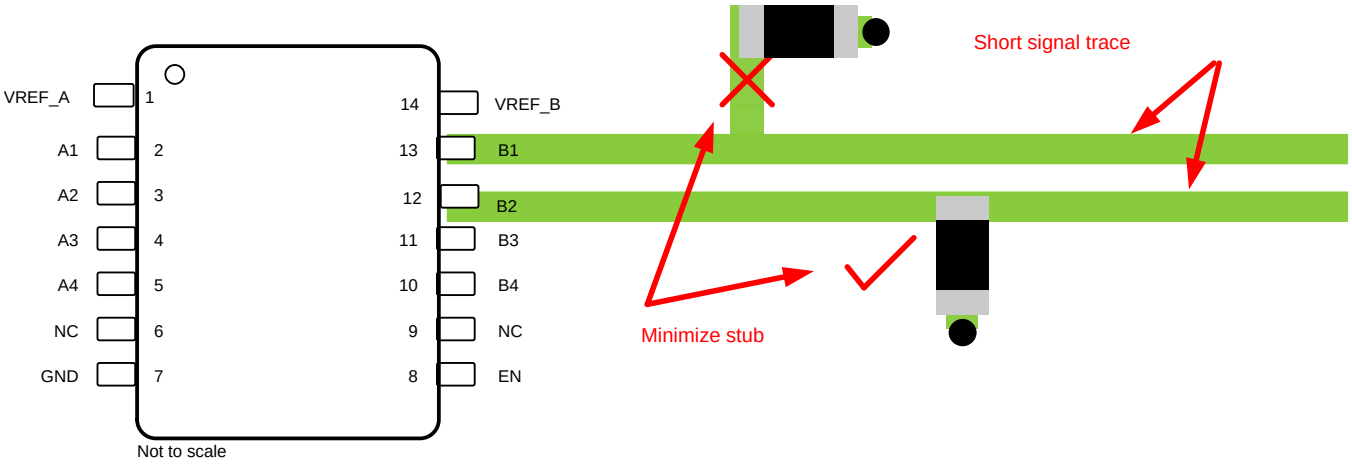


图 11. Short Trace Layout

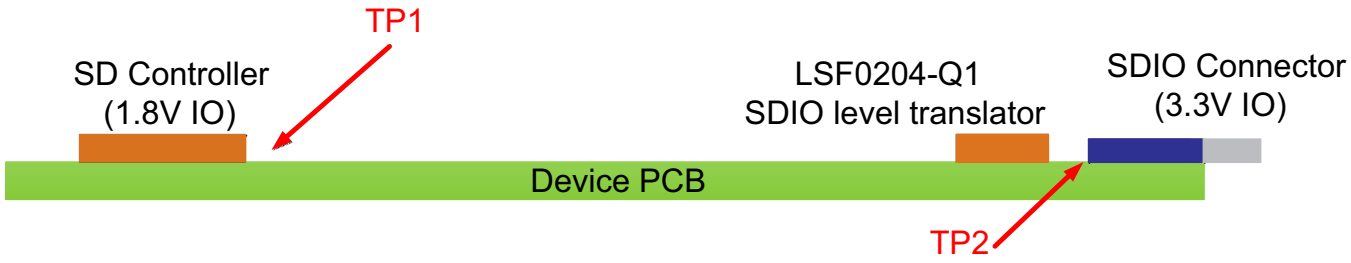


图 12. Device Placement

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，TI Logic Minute：*《简介 – 使用 LSF 系列进行电压电平转换》* 视频
- 德州仪器 (TI)，*《使用 LSF 系列进行电压电平转换》* 应用报告
- 德州仪器 (TI)，《TXS、TXB 和 LSF 转换器的偏置要求》 应用报告
- 德州仪器 (TI)，《TXS 和 LSF 转换器件的 VoI 影响因素》应用报告

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0204QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF204Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

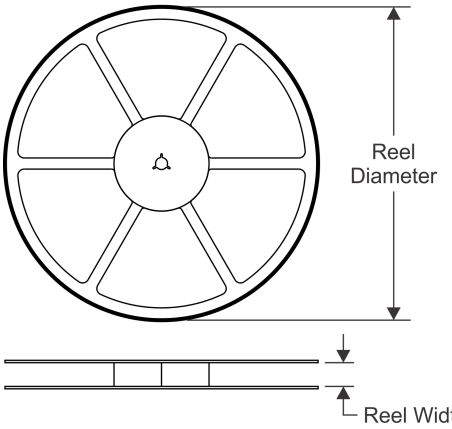
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

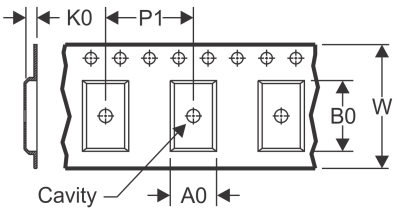
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

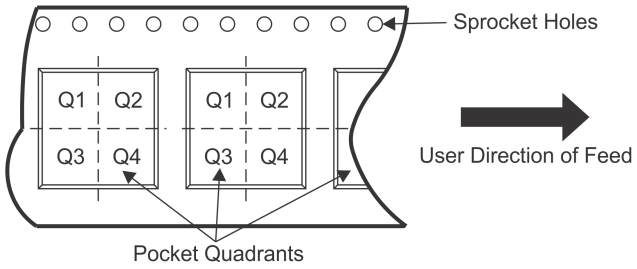


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

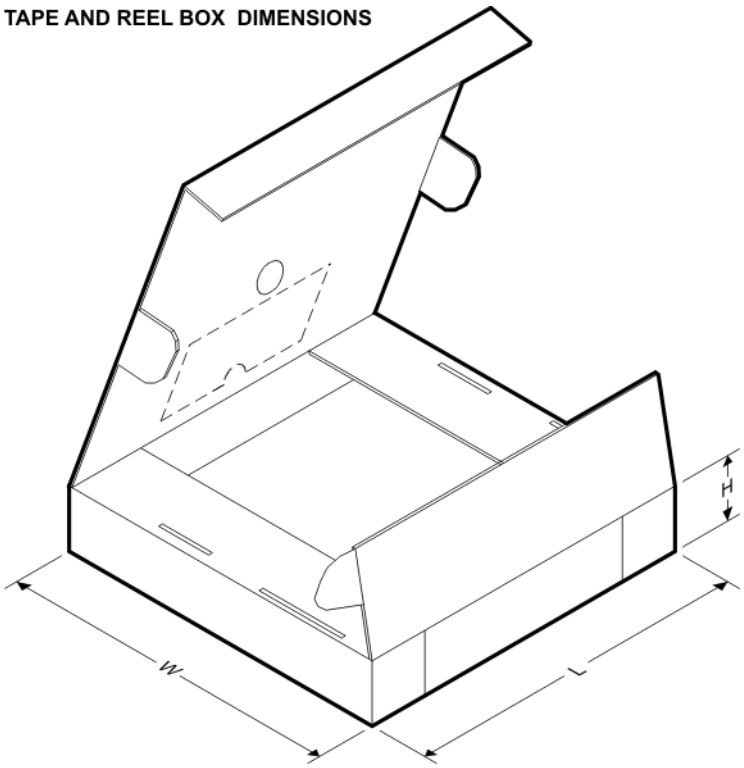
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0204QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

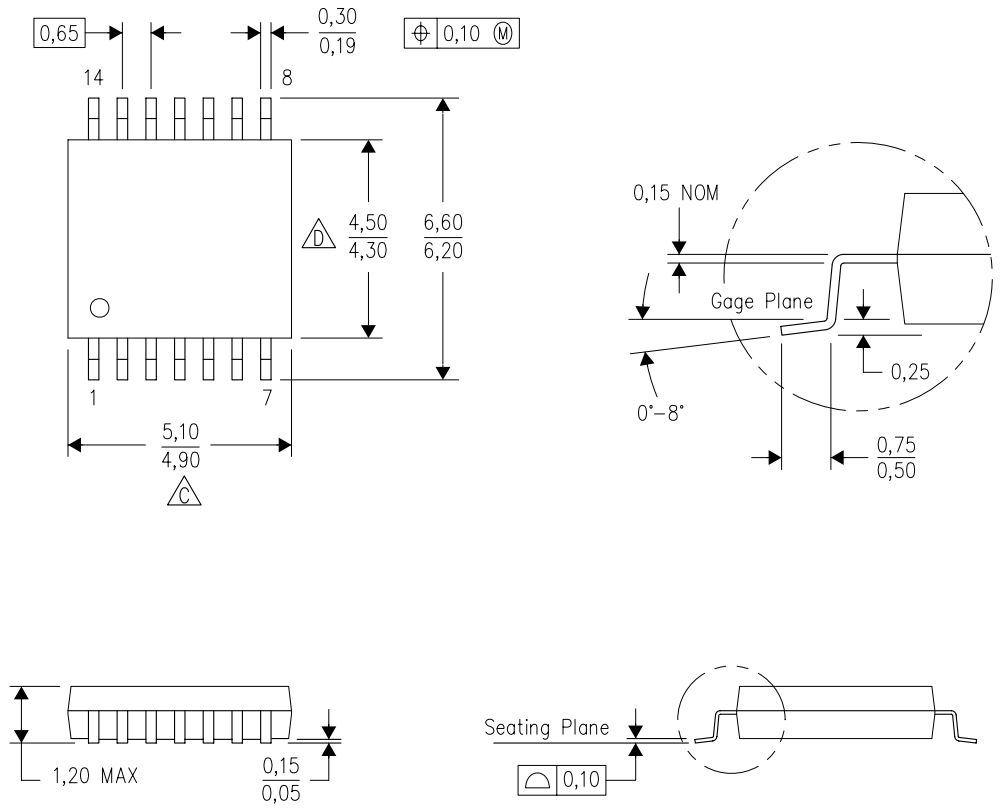
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0204QPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

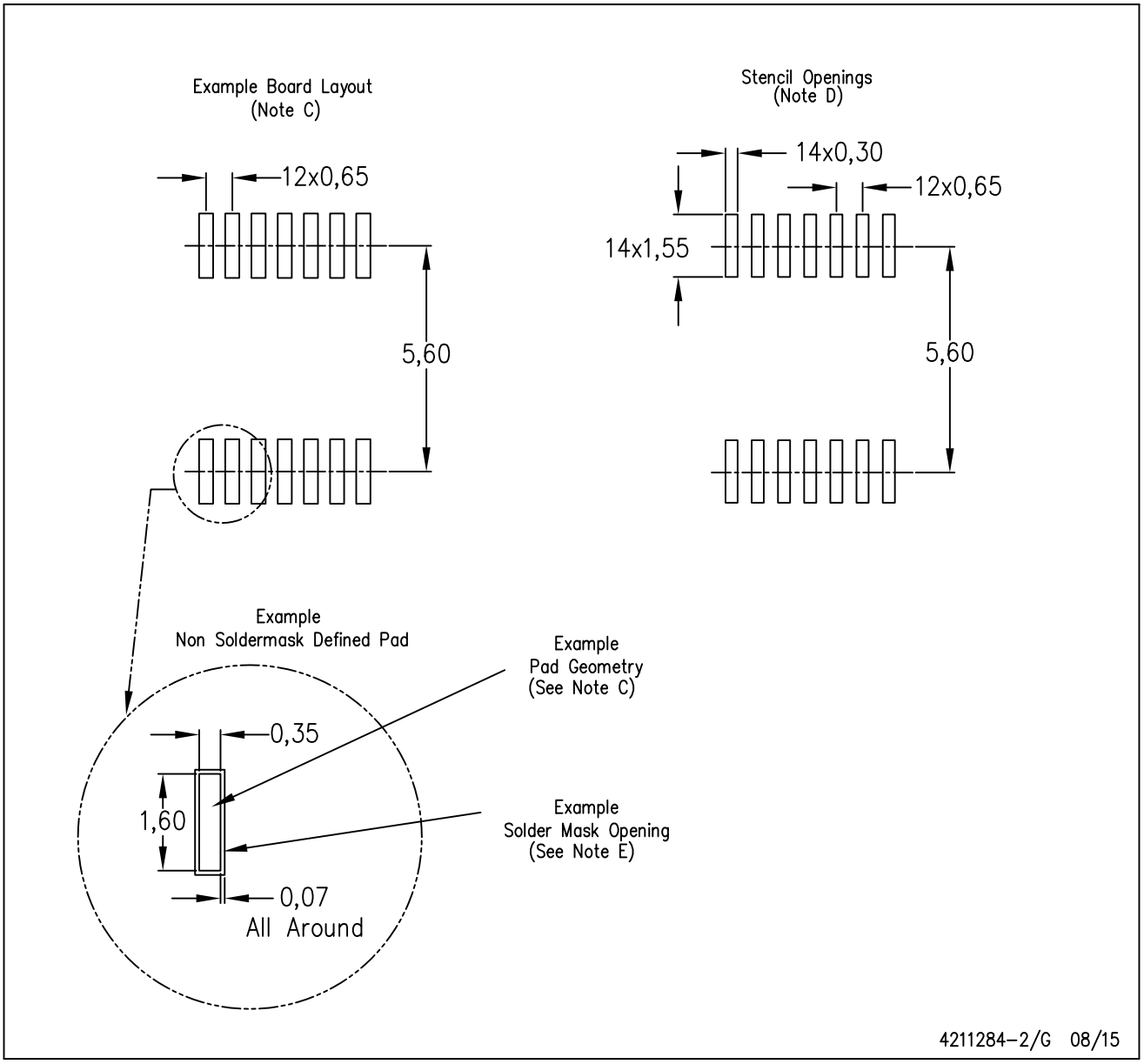
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122