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**DLPC3437**

ZHCSHH9C –JANUARY 2017–REVISED JUNE 2019

# DLPC3437 显示控制器

## 1 特性

- 适用于 DLP3310 (0.33 1080p) TRP DMD 的显示控制器
  - 用于驱动 DLP3310 DMD 的专用 2xDLPC3437 控制器
  - 最高支持 1080p 的输入图像大小
  - 支持接口训练的低功耗 DMD 接口
- 24 位输入像素接口支持：
  - 并行接口
  - 高达 150MHz 的像素时钟
- 双路 FPD-link 输入像素接口支持：
  - LVDS 接口
  - 有效像素时钟高达 150MHz
- 像素数据处理：
  - IntelliBright™图像处理算法套件
    - 内容自适应照明控制
    - 局部亮度增强
  - 色彩坐标调整
  - 可编程 degamma
  - 主动电源管理处理
- 封装：
  - 201 引脚、13mm × 13mm、0.8mm 间距、NFBGA
- 支持外部闪存
- 与 DLPA3000 PMIC/LED 驱动器兼容
- 断电时自动 DMD 停止
- 嵌入式帧存储器 (eDRAM)
- 系统 功能：
  - 器件配置的 I²C 控制
  - 可编程启动界面
  - 可编程 LED 电流控制
  - 一帧延迟

## 2 应用

- 移动智能电视
- 无屏电视
- 游戏显示器
- 数字标牌
- 可穿戴显示器
- Pico 投影仪
- 交互式显示器
- 超便携显示器
- 智能家居显示器
- 3D 机器视觉
- 3D 打印机

## 3 说明

DLPC3437 数字控制器是 DLP3310 (.33 1080p) 芯片组的组成部分，用于支持 DLP3310 数字微镜器件 (DMD) 的可靠运行。DLP3310 芯片组可用于各种小尺寸、低功耗和高分辨率全高清显示。

### 器件信息[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
| --- | --- | --- |
| DLPC3437 | NFBGA (201) | 13.00mm x 13.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 简化原理图

# 目录

# 4 修订历史记录

**Changes from Revision B (January 2018) to Revision C**                     **Page**

• Changed normal park time from 500 μs to 20 ms

**Changes from Revision A (February 2017) to Revision B**                   **Page**

• Clarified that GPIO_12 FPGA_RDY and GPIO_11 ACT_SYNC connect to Slave ASIC in Pin Functions – GPIO Peripheral Interface

• Removed 3.3 V from V$_{CC\_INTF}$ in Pin Functions-Power and Ground

• Removed 2.5-V and 3.3-V options from the subscripts 5, 7, 9, and 11 in Table 1

• Removed 2.5-V and 3.3-V references from V$_{(VCC\_INTF)}$ in *Absolute Maximum Ratings$^{(1)}$*

• Removed Host I/O Power from V$_{(VCC\_INTF)}$ in *Absolute Maximum Ratings$^{(1)}$*

• Removed 3.3 V value from V$_{(VCC\_INTF)}$ in *Recommended Operating Conditions*

• Removed 3.3-V reference from I$_{(VCC\_INTF)}$ in *Electrical Characteristics Over Recommended Operating Conditions*

• Removed I/O types 5, 9, and 11 from V$_{OH}$ and V$_{OL}$ 2.5-V and 3.3-V LVTTL entries in *Electrical Characteristics*

• Removed I/O type "9" from 2.5-V LVTTL / 8 mA entry line, I/O types "5, 9, 11," from 2.5-V LVTTL / 24 mA entry line, and I/O type "9" from 3.3-V LVTTL / 8 mA entry line for I$_{OH}$ in *Electrical Characteristics*

• Removed 2.5-V Iand 3.3-V LVTTL I/O type 5 from I$_{OH}$ in *Electrical Characteristics*

• Removed I/O type "9" from 2.5-V LVTTL / 8 mA entry line, I/O types "5, 9, 11," from 2.5-V LVTTL / 24 mA entry line, and I/O type "9" from 3.3-V LVTTL / 8 mA entry line for I$_{OL}$ in *Electrical Characteristics*

• Removed 2.5-V Iand 3.3-V LVTTL I/O type 5 from I$_{OL}$ in *Electrical Characteristics*

• Updated Table 9 column titles and added second option for DLPC3437 ASIC 8 lane DMD routing

## Changes from Original (January 2017) to Revision A                                       Page

# 5 Pin Configuration and Functions

**ZEZ Package**
**201-Pin NFBGA**
**Bottom View**
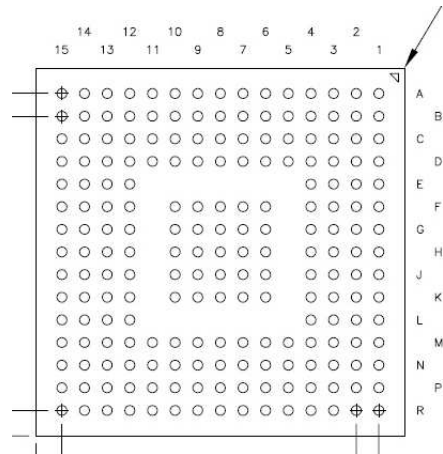
|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| A | DMD_LS_CLK | DMD_LS_WDATA | DMD_HS_WDATAH_P | DMD_HS_WDATAG_P | DMD_HS_WDATAF_P | DMD_HS_WDATAE_P | DMD_HS_CLK_P | DMD_HS_WDATAD_P | DMD_HS_WDATAC_P | DMD_HS_WDATAB_P | DMD_HS_WDATAA_P | CMP_OUT | SPI0_CLK | SPI0_CSZ0 | CMP_PWM |
| B | DMD_DEN_ARSTZ | DMD_LS_RDATA | DMD_HS_WDATAH_N | DMD_HS_WDATAG_N | DMD_HS_WDATAF_N | DMD_HS_WDATAE_N | DMD_HS_CLK_N | DMD_HS_WDATAD_N | DMD_HS_WDATAC_N | DMD_HS_WDATAB_N | DMD_HS_WDATAA_N | SPI0_DIN | SPI0_DOUT | LED_SEL_1 | LED_SEL_0 |
| C | NC | NC | VDDLP12 | VSS | VDD | VSS | VCC | VSS | VCC | HWTEST_EN | RESETZ | SPI0_CSZ1 | PARKZ | GPIO_00 | GPIO_01 |
| D | NC | NC | VDD | VCC | VDD | VSS | VDD | VSS | VDD | VSS | VCC_FLSH | VDD | VDD | GPIO_02 | GPIO_03 |
| E | NC | NC | VDD | VSS |  |  |  |  |  |  |  | VCC | VSS | GPIO_04 | GPIO_05 |
| F | NC | NC | RREF | VSS |  | VSS | VSS | VSS | VSS | VSS |  | VCC | VDD | GPIO_06 | GPIO_07 |
| G | NC | NC | VSS_PLLM | VSS |  | VSS | VSS | VSS | VSS | VSS |  | VSS | VSS | GPIO_08 | GPIO_09 |
| H | PLL_REFCLK_I | VDD_PLLM | VSS_PLLD | VSS |  | VSS | VSS | VSS | VSS | VSS |  | VSS | VDD | GPIO_10 | GPIO_11 |
| J | PLL_REFCLK_O | VDD_PLLD | VSS | VDD |  | VSS | VSS | VSS | VSS | VSS |  | VDD | VSS | GPIO_12 | GPIO_13 |
| K | PDATA_1 | PDATA_0 | VDD | VSS |  | VSS | VSS | VSS | VSS | VSS |  | VSS | VCC | GPIO_14 | GPIO_15 |
| L | PDATA_3 | PDATA_2 | VSS | VDD |  |  |  |  |  |  |  | VDD | VDD | GPIO_16 | GPIO_17 |
| M | PDATA_5 | PDATA_4 | VCC_INTF | VSS | VSS | VDD | VCC_INTF | VSS | VDD | VDD | VCC | VSS | JTAGTMS1 | GPIO_18 | GPIO_19 |
| N | PDATA_7 | PDATA_6 | VCC_INTF | PDM_CVS_TE | HSYNC_CS | 3DR | VCC_INTF | HOST_IRQ | IIC0_SDA | IIC0_SCL | JTAGTMS2 | JTAGTDO2 | JTAGTDO1 | TSTPT_6 | TSTPT_7 |
| P | VSYNC_WE | DATEN_CMD | PCLK | PDATA_11 | PDATA_13 | PDATA_15 | PDATA_17 | PDATA_19 | PDATA_21 | PDATA_23 | JTAGTRSTZ | JTAGTCK | JTAGTDI | TSTPT_4 | TSTPT_5 |
| R | PDATA_8 | PDATA_9 | PDATA_10 | PDATA_12 | PDATA_14 | PDATA_16 | PDATA_18 | PDATA_20 | PDATA_22 | IIC1_SDA | IIC1_SCL | TSTPT_0 | TSTPT_1 | TSTPT_2 | TSTPT_3 |

**Figure 1.  13 mm × 13 mm Package – VF Ball Grid Array**

## Pin Functions – Board Level Test, Debug, and Initialization

| PIN | | I/O | DESCRIPTION |
|-----|-----|-----|-------------|
| NAME | NUMBER | | |
| HWTEST_EN | C10 | $I_6$ | Manufacturing test enable signal. This signal should be connected directly to ground on the PCB for normal operation. |
| PARKZ | C13 | $I_6$ | DMD fast PARK control (active low Input) (hysteresis buffer). PARKZ must be set high to enable normal operation. PARKZ should be set high prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input). PARKZ should be set low for a minimum of 32 µs before any power is removed from the DLPC3437 such that the fast DMD PARK operation can be completed. Note for PARKZ, fast PARK control should only be used when loss of power is eminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with the fast PARK operation. The longest lifetime is achieved with a normal PARK operation. Because of this, PARKZ is typically used in conjunction with a normal PARK request control input through GPIO_08. The difference being that when the host sets PROJ_ON low, which connects to both GPIO_08 and the DLPA3000 PMIC chip, the DLPC3437 takes much longer than 40 µs to park the mirrors. The DLPA3000 holds on all power supplies, and keep RESETZ high, until the longer mirror parking has completed. This longer mirror parking time, of up to 20 ms, ensures the longest DMD lifetime and reliability.<br>The DLPA3000 monitors power to the DLPC3437 and detects an eminent power loss condition and drives the PARKZ signal accordingly. |
| Reserved | P12 | $I_6$ | TI internal use. Should be left unconnected. |
| Reserved | P13 | $I_6$ | TI internal use. Should be left unconnected. |
| Reserved | N13[1] | $O_1$ | TI internal use. Should be left unconnected. |
| Reserved | N12[1] | $O_1$ | TI internal use. Should be left unconnected. |
| Reserved | M13 | $I_6$ | TI internal use. Should be left unconnected. |
| Reserved | N11 | $I_6$ | TI internal use. Should be left unconnected. |
| Reserved | P11 | $I_6$ | TI internal use<br>This pin must be tied to ground, through an external resistor of 8 kΩ, or less, resistor for normal operation. Failure to tie this pin low during normal operation will cause startup and initialization problems. |
| RESETZ | C11 | $I_6$ | DLPC3437 power-on reset (active low input) (hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All ASIC power and clocks must be stable before this reset is de-asserted. Note that the following signals will be tri-stated while RESETZ is asserted:<br>• SPI0_CLK, SPI0_DOUT, SPI0_CSZ0,<br>• SPI0_CSZ1, and GPIO(19:00)<br>External pullups or downs (as appropriate) should be added to all tri-stated output signals listed (including bidirectional signals to be configured as outputs) to avoid floating ASIC outputs during reset if connected to devices on the PCB that can malfunction. For SPI, at a minimum, any chip selects connected to the devices should have a pullup.<br>Unused bidirectional signals can be functionally configured as outputs to avoid floating ASIC inputs after RESETZ is set high.<br>The following signals are forced to a logic low state while RESETZ is asserted and corresponding I/O power is applied:<br>• LED_SEL_0, LED_SEL_1 and DMD_DEN_ARSTZ<br>No signals will be in their active state while RESETZ is asserted.<br>Note that no I²C activity is permitted for a minimum of 500 ms after RESETZ (and PARKZ) are set high. |

(1)  If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

## Pin Functions – Board Level Test, Debug, and Initialization (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| TSTPT_0 | R12 | B$_1$ | Test pin 0 (includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ, and then driven as an output. Normal use: Reserved for test output. Should be left open or unconnected for normal use. Note: An external pullup should not be applied to this pin to avoid putting the DLPC3437 in a test mode.<br><br>Without external pullup [2]          With external pullup[3]<br>Feeds TMSEL(0)                          Feeds TMSEL(0) |
| TSTPT_1 | R13 | B$_1$ | Test pin 1 (includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for test output. Should be left open or unconnected for normal use. Note: An external pullup should not be applied to this pin to avoid putting the DLPC3437 in a test mode.<br><br>Without external pullup[2]          With external pullup[3]<br>Feeds TMSEL(1)                          Feeds TMSEL(1) |
| TSTPT_2 | R14 | B$_1$ | Test pin 2 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for test output. Should be left open or unconnected for normal use. Note: An external pullup should not be applied to this pin to avoid putting the DLPC3437 in a test mode.<br><br>Without external pullup[2]          With external pullup[3]<br>Feeds TMSEL(2)                          Feeds TMSEL(2) |
| TSTPT_3 | R15 | B$_1$ | Test pin 3 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for for test output. Should be left open or unconnected for normal use. |
| TSTPT_4 | P14 | B$_1$ | Test pin 4 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for for test output. Should be left open or unconnected for normal use. |
| TSTPT_5 | P15 | B$_1$ | Test pin 5 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for test output. Should be left open or unconnected for normal use. |
| TSTPT_6 | N14 | B$_1$ | Test pin 6 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for test output. Should be left open or unconnected for normal use. Alternative use: none. External logic shall not unintentionally pull this pin high to avoid putting the DLPC3437 in a test mode. |
| TSTPT_7 | N15 | B$_1$ | Test pin 7 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: Reserved for test output. Should be left open or unconnected for normal use. |

(2)   External pullup resistor must be 8 kΩ, or less, for pins with internal pullup or down resistors.
(3)   If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then the TSTPT I/O can be left open/ unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

**Pin Functions – Parallel Port Input Data and Control** [(1)]

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | PARALLEL RGB MODE |
| PCLK | P3 | $I_{11}$ | Pixel clock[(2)] |
| PDM_CVS_TE | N4 | $B_5$ | Parallel data mask[(3)] |
| VSYNC_WE | P1 | $I_{11}$ | Vsync[(4)] |
| HSYNC_CS | N5 | $I_{11}$ | Hsync[(4)] |
| DATAEN_CMD | P2 | $I_{11}$ | Data Valid[(4)] |
| PDATA_0<br>PDATA_1<br>PDATA_2<br>PDATA_3<br>PDATA_4<br>PDATA_5<br>PDATA_6<br>PDATA_7 | K2<br>K1<br>L2<br>L1<br>M2<br>M1<br>N2<br>N1 | $I_{11}$ | **(RGB 888)**<br><br>Blue (bit weight 1)<br>Blue (bit weight 2)<br>Blue (bit weight 4)<br>Blue (bit weight 8)<br>Blue (bit weight 16)<br>Blue (bit weight 32)<br>Blue (bit weight 64)<br>Blue (bit weight 128) |
| PDATA_8<br>PDATA_9<br>PDATA_10<br>PDATA_11<br>PDATA_12<br>PDATA_13<br>PDATA_14<br>PDATA_15 | R1<br>R2<br>R3<br>P4<br>R4<br>P5<br>R5<br>P6 | $I_{11}$ | **(RGB 888)**<br><br>Green (bit weight 1)<br>Green (bit weight 2)<br>Green (bit weight 4)<br>Green (bit weight 8)<br>Green (bit weight 16)<br>Green (bit weight 32)<br>Green (bit weight 64)<br>Green (bit weight 128) |
| PDATA_16<br>PDATA_17<br>PDATA_18<br>PDATA_19<br>PDATA_20<br>PDATA_21<br>PDATA_22<br>PDATA_23 | R6<br>P7<br>R7<br>P8<br>R8<br>P9<br>R9<br>P10 | $I_{11}$ | **(RGB 888)**<br><br>Red (bit weight 1)<br>Red (bit weight 2)<br>Red (bit weight 4)<br>Red (bit weight 8)<br>Red (bit weight 16)<br>Red (bit weight 32)<br>Red (bit weight 64)<br>Red (bit weight 128) |
| 3DR | N6 | | 3D reference<br>• For 3D applications: Left or right 3D reference (left = 1, right = 0). To be provided by the host when a 3D command is not provided. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC).<br>• If a 3D application is not used, then this input should be pulled low through an external resistor. |

(1)  PDM_CVS_TE is optional for parallel interface operation. If unused, inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(2)  Pixel clock capture edge is software programmable.
(3)  The parallel data mask signal input is optional for parallel interface operations. If unused, inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(4)  VSYNC, HSYNC, and DATAEN polarity is software programmable.

## Pin Functions – DMD Reset and Bias Control

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| DMD_DEN_ARSTZ | B1 | $O_2$ | DMD driver enable (active high)/DMD reset (active low). Assuming the corresponding I/O power is supplied, this signal will be driven low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC3437 is independent of the 1.8-V power to the DMD, then TI recommends a weak, external pulldown resistor to hold the signal low in the event DLPC3437 power is inactive while DMD power is applied. |
| DMD_LS_CLK | A1 | $O_3$ | DMD, low speed interface clock |
| DMD_LS_WDATA | A2 | $O_3$ | DMD, low speed serial write data |
| DMD_LS_RDATA | B2 | $I_6$ | DMD, low speed serial read data |

## Pin Functions – DMD Sub-LVDS Interface

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| DMD_HS_CLK_P<br>DMD_HS_CLK_N | A7<br>B7 | $O_4$ | DMD high speed interface |
| DMD_HS_WDATA_H_P<br>DMD_HS_WDATA_H_N<br>DMD_HS_WDATA_G_P<br>DMD_HS_WDATA_G_N<br>DMD_HS_WDATA_F_P<br>DMD_HS_WDATA_F_N<br>DMD_HS_WDATA_E_P<br>DMD_HS_WDATA_E_N<br>DMD_HS_WDATA_D_P<br>DMD_HS_WDATA_D_N<br>DMD_HS_WDATA_C_P<br>DMD_HS_WDATA_C_N<br>DMD_HS_WDATA_B_P<br>DMD_HS_WDATA_B_N<br>DMD_HS_WDATA_A_P<br>DMD_HS_WDATA_A_N | A3<br>B3<br>A4<br>B4<br>A5<br>B5<br>A6<br>B6<br>A8<br>B8<br>A9<br>B9<br>A10<br>B10<br>A11<br>B11 | $O_4$ | DMD high speed interface lanes, write data bits: The true numbering and application of the DMD_HS_DATA pins are software configuration dependent |

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## Pin Functions – Peripheral Interface[1]

| PIN NAME | PIN NUMBER | I/O | DESCRIPTION |
|---|---|---|---|
| CMP_OUT | A12 | $I_6$ | Successive approximation ADC comparator output (DLPC3437 Input). Assumes a successive approximation ADC is implemented with a WPC light sensor and/or a thermistor feeding one input of an external comparator and the other side of the comparator is driven from the ASIC's CMP_PWM pin. Should be pulled-down to ground if this function is not used (hysteresis buffer). |
| CMP_PWM | A15 | $O_1$ | Successive approximation comparator pulse-duration modulation (output). Supplies a PWM signal to drive the successive approximation ADC comparator used in WPC light-to-voltage sensor applications. Should be left unconnected if this function is not used. |
| HOST_IRQ[2] | N8 | $O_9$ | Host interrupt (output)<br>HOST_IRQ indicates when the DLPC3437 auto-initialization is in progress and most importantly when it completes.<br>The DLPC3437 tri-states this output during reset and assumes that an external pullup is in place to drive this signal to its inactive state. |
| IIC0_SCL | N10 | $B_7$ | I2C slave (port 0) SCL (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (1.8 V). External I2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the $V_{IH}$ specification of the slave I2C input buffers). |
| IIC1_SCL | R11 | $B_8$ | I2C master (Port 1) SCL (bidirectional, open-drain signal with input hysteresis): An external pull-up is required. The Master I2C I/Os are 3.6-V tolerant (High-volt-input tolerant) but are powered by the fixed 1.8-V $V_{CC18}$ supply. Thus even though its supply is fixed at 1.8 V, the external I2C pull-ups can be connected to 1.8-V, 2.5-V, or 3.3-V supplies; However this is **only** valid if the external slave I2C device satisfies the DLPC3437 $V_{IH}$ input requirement at the fixed 1.8-V level. $V_{IH}$ is specified at 1.17 V, thus assuming $V_{CC18}$ = 1.64 V, $V_{IH}$ = 0.486 V. |
| IIC1_SDA | R10 | $B_8$ | I2C Master (Port 1) SDA (bidirectional, open-drain signal with input hysteresis): An external pull-up is required. The Master I2C I/Os are 3.6-V tolerant (High-volt-input tolerant) but are powered by the fixed 1.8-V $V_{CC18}$ supply. Thus even though its supply is fixed at 1.8 V, the external I2C pull-ups can be connected to 1.8-V, 2.5-V, or 3.3-V supplies; However this is **only** valid if the external Slave I2C device satisfies the DLPC3437 $V_{IH}$ input requirement at the fixed 1.8-V level. $V_{IH}$ is specified at 1.17 V, thus assuming $V_{CC18}$ = 1.64 V, $V_{IH}$ = 0.486 V. |
| Reserved | R11 | $B_8$ | TI internal use. TI recommends an external pullup resistor. |
| IIC0_SDA | N9 | $B_7$ | I2C slave (port 0) SDA (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I2C port is the control port of ASIC. The slave I2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by $V_{CC\_INTF}$ (1.8 V). External I2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the $V_{IH}$ specification of the slave I2C input buffers). |
| Reserved | R10 | $B_8$ | TI internal use. TI recommends an external pullup resistor. |
| LED_SEL_0 | B15 | $O_1$ | LED enable select. Controlled by programmable DMD sequence.<br><br>Timing        Enabled LED<br>LED_SEL(1:0)   DLPA3000 application<br>00          None<br>01          Red<br>10          Green<br>11          Blue |
| LED_SEL_1 | B14 | $O_1$ | These signals will be driven low when RESETZ is asserted and the corresponding I/O power is supplied. They will continue to be driven low throughout the auto-initialization process. A weak, external pulldown resistor is still recommended to ensure that the LEDs are disabled when I/O power is not applied. |
| SPI0_CLK | A13 | $O_{13}$ | Synchronous serial port 0, clock |
| SPI0_CSZ0 | A14 | $O_{13}$ | SPI port 1, chip select 0 (active low output)<br>TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion. |
| SPI0_CSZ1 | C12 | $O_{13}$ | SPI port 1, chip select 1 (active low output)<br>TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion. |
| SPI0_DIN | B12 | $I_{12}$ | Synchronous serial port 0, receive data in |
| SPI0_DOUT | B13 | $O_{13}$ | Synchronous serial port 0, transmit data out |

(1) External pullup resistor must be 8 kΩ or less.
(2) For more information about usage, see *HOST_IRQ Usage Model*.

## Pin Functions – GPIO Peripheral Interface[1]

| PIN | | I/O | DESCRIPTION[2] |
|---|---|---|---|
| NAME | NUMBER | | |
| GPIO_19 | M15 | B₁ | HBT_ODAT (Output): Required connection for Dual ASIC Applications. Connect this to alternate ASICs HBT_IDAT Input pin. |
| GPIO_18 | M14 | B₁ | HBT_OCLK (Output): Required connection for Dual ASIC Applications. Connect this to alternate ASICs HBT_ICLK Input pin. |
| GPIO_17 | L15 | B₁ | HBT_IDAT (Input): Required connection for Dual ASIC Applications. Connect this to alternate ASICs HBT_ODAT Output pin. |
| GPIO_16 | L14 | B₁ | HBT_ICLK (Input): Required connection for Dual ASIC Applications. Connect this to alternate ASICs HBT_OCLK Output pin. |
| GPIO_15 | K15 | B₁ | DA_SYNC (BiDir): Required to be connected between ASICs on this same pin for Dual ASIC Applications. |
| GPIO_14 | K14 | B₁ | SEQ_SYNC (BiDir): Required to be connected between ASICs on this same pin, with an external pull-up resistor, for Dual ASIC Applications. |
| GPIO_13 | J15 | B₁ | General purpose I/O 13 (hysteresis buffer). Options: 1. CAL_PWR (output): Intended to feed the calibration control of the successive approximation ADC light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_12 | J14 | B₁ | General purpose I/O 12 (hysteresis buffer). Master ASIC Options: 1. (Output) power enable control for LABB light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). Slave ASIC: 1. FPGA_RDY (input): Input from FPGA, indicating when the FPGA initialization process is complete. |
| GPIO_11 | H15 | B₁ | General purpose I/O 11 (hysteresis buffer). Master ASIC Options: 1. (Output): Thermistor power enable. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). Slave ASIC: 1. ACT_SYNC (output): Output to FPGA, used for synchronizing the actuator position with the ASIC data processing. |
| GPIO_10 | H14 | B₁ | General Purpose I/O 10 (hysteresis buffer). Master ASIC Options: 1. RC_CHARGE (output): Intended to feed the RC charge circuit of the successive approximation ADC used to control the light sensor comparator. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). Slave ASIC: 1. SUB_FRAME (input): Input from FPGA, signaling sub-frames. |
| GPIO_09 | G15 | B₁ | General purpose I/O 09 (hysteresis buffer). Options: 1. LS_PWR (active high output): Intended to feed the power control signal of the successive approximation ADC light sensor. 2. 3D Glasses Control (Output): Intended to be used to control the shutters on 3D Glasses (Left = 1, Right = 0). 3. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_08 | G14 | B₁ | General purpose I/O 08 (hysteresis buffer). Options: 1. (All) Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal will cause the DLPC3437 to PARK the DMD, but it will not power down the DMD (the DLPA3000 does that instead). The minimum high time is 200 ms. The minimum low time is also 200 ms. |

(1) GPIO signals must be configured through software for input, output, bidirectional, or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO is as an input signal. An external pullup is required for each signal configured as open-drain.
(2) DLPC3437 general purpose I/O. These GPIO are software configurable.

## Pin Functions – GPIO Peripheral Interface[1] (continued)

| PIN NAME | PIN NUMBER | I/O | DESCRIPTION[2] |
|---|---|---|---|
| GPIO_07 | F15 | B$_1$ | General purpose I/O 07 (hysteresis buffer). Options:<br>1. (Output): LABB output sample and hold sensor control signal.<br>2. (All) GPIO (bidirectional): Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_06 | F14 | B$_1$ | General purpose I/O 06 (hysteresis buffer). Option:<br>1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used. An external pulldown resistor is required to deactivate this signal during reset and auto-initialization processes. |
| GPIO_05 | E15 | B$_1$ | General purpose I/O 05 (hysteresis buffer). Options:<br>1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_04 | E14 | B$_1$ | MST_SLVZ (Input): Master/Slave ASIC identifier strap (Master = 1, Slave = 0). |
| GPIO_03 | D15 | B$_1$ | General purpose I/O 03 (hysteresis buffer). Options:<br>1. SPI1_CSZ0 (active low output): Optional SPI1 chip select 0 signal. An external pullup resistor is required to deactivate this signal during reset and auto-initialization processes.<br>2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_02 | D14 | B$_1$ | General purpose I/O 02 (hysteresis buffer). Options:<br>1. SPI1_DOUT (output): Optional SPI1 data output signal.<br>2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_01 | C15 | B$_1$ | General purpose I/O 01 (hysteresis buffer). Options:<br>1. SPI1_CLK (output): Optional SPI1 clock signal.<br>2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |
| GPIO_00 | C14 | B$_1$ | General purpose I/O 00 (hysteresis buffer). Options:<br>1. SPI1_DIN (input): Optional SPI1 data input signal.<br>2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). |

## Pin Functions – Clock and PLL Support

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| PLL_REFCLK_I | H1 | $I_{11}$ | Reference clock crystal input. If an external oscillator is used in place of a crystal, then this pin should be used as the oscillator input. |
| PLL_REFCLK_O | J1 | $O_5$ | Reference clock crystal return. If an external oscillator is used in place of a crystal, then this pin should be left unconnected (that is floating with no added capacitive load). |

## Pin Functions – Power and Ground[(1)]

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| $V_{DD}$ | C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3 | PWR | Core power 1.1 V (main 1.1 V) |
| $V_{DDLP12}$ | C3 | PWR | Core power 1.1 V |
| $V_{SS}$ | C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8 F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10 | GND | Core ground (eDRAM, I/O ground, thermal ground) |
| $V_{CC18}$ | C7, C9, D4, E12, F12, K13, M11 | PWR | All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins) |
| $V_{CC\_INTF}$ | M3, M7, N3, N7 | PWR | Host or parallel interface I/O power: 1.8 (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins) |
| $V_{CC\_FLSH}$ | D11 | PWR | Flash interface I/O power: 1.8 V to 3.3 V (Dedicated SPI0 power pin) |
| $V_{DD\_PLLM}$ | H2 | PWR | MCG PLL 1.1-V power |
| $V_{SS\_PLLM}$ | G3 | RTN | MCG PLL return |
| $V_{DD\_PLLD}$ | J2 | PWR | DCG PLL 1.1-V power |
| $V_{SS\_PLLD}$ | H3 | RTN | DCG PLL return |

(1)  The only power sequencing restrictions are:
    (a)  The $V_{DDLP12}$ supply must be powered-on at exactly the same time or after the $V_{DD11}$ supply.
    (b)  The $V_{DD11}$ supply should ramp up with a 1-ms minimum rise time.
    (c) The reverse is needed at power down.

**Table 1. I/O Type Subscript Definition**

| I/O | | SUPPLY REFERENCE | ESD STRUCTURE |
|---|---|---|---|
| SUBSCRIPT | DESCRIPTION | | |
| 1 | 1.8-V LVCMOS I/O buffer with 8-mA drive | $V_{CC18}$ | ESD diode to GND and supply rail |
| 2 | 1.8-V LVCMOS I/O buffer with 4-mA drive | $V_{CC18}$ | ESD diode to GND and supply rail |
| 3 | 1.8-V LVCMOS I/O buffer with 24-mA drive | $V_{CC18}$ | ESD diode to GND and supply rail |
| 4 | 1.8-V sub-LVDS output with 4-mA drive | $V_{CC18}$ | ESD diode to GND and supply rail |
| 5 | 1.8-V LVCMOS with 4-mA drive | $V_{CC\_INTF}$ | ESD diode to GND and supply rail |
| 6 | 1.8-V LVCMOS input | $V_{CC18}$ | ESD diode to GND and supply rail |
| 7 | 1.8-V I$^2$C with 3-mA drive | $V_{CC\_INTF}$ | ESD diode to GND and supply rail |
| 8 | 1.8-V I$^2$C with 3-mA drive | $V_{CC18}$ | ESD diode to GND and supply rail |
| 9 | 1.8-V LVCMOS with 8-mA drive | $V_{CC\_INTF}$ | ESD diode to GND and supply rail |
| 11 | 1.8-V LVCMOS input | $V_{CC\_INTF}$ | ESD diode to GND and supply rail |
| 12 | 1.8-, 2.5-, 3.3-V LVCMOS input | $V_{CC\_FLSH}$ | ESD diode to GND and supply rail |
| 13 | 1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive | $V_{CC\_FLSH}$ | ESD diode to GND and supply rail |

**Table 2. Internal Pullup and Pulldown Characteristics[1][2]**

| INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS | $V_{CCIO}$ | MIN | MAX | UNIT |
|---|---|---|---|---|
| Weak pullup resistance | 3.3 V | 29 | 63 | kΩ |
| | 2.5 V | 38 | 90 | kΩ |
| | 1.8 V | 56 | 148 | kΩ |
| Weak pulldown resistance | 3.3 V | 30 | 72 | kΩ |
| | 2.5 V | 36 | 101 | kΩ |
| | 1.8 V | 52 | 167 | kΩ |

(1) The resistance is dependent on the supply voltage level applied to the I/O.
(2) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

over operating free-air temperature (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **SUPPLY VOLTAGE**[2][3] | | | | |
| $V_{(VDD)}$ (core) | | –0.3 | 1.21 | V |
| $V_{(VDDLP12)}$ (core) | | –0.3 | 1.32 | V |
| Power + sub-LVDS | | –0.3 | 1.96 | V |
| $V_{(VCC\_INTF)}$ | 1.8-V power | –0.3 | 1.99 | V |
| $V_{(VCC\_FLSH)}$ | Flash I/O power | –0.3 | 3.60 | V |
| | If 1.8-V power used | –0.3 | 1.96 | |
| | If 2.5-V power used | –0.3 | 2.72 | |
| | If 3.3-V power used | –0.3 | 3.58 | |
| $V_{(VDD\_PLLM)}$ (MCG PLL) | | –0.3 | 1.21 | V |
| $V_{(VDD\_PLLD)}$ (1DCG PLL) | | –0.3 | 1.21 | V |
| **GENERAL** | | | | |
| $T_J$ | Operating junction temperature | –30 | 125 | °C |
| $T_{stg}$ | Storage temperature | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$[1] | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[3] | ±500 | |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(VDD)}$ | Core power 1.1 V (main 1.1 V) | ±5% tolerance | 1.045 | 1.1 | 1.155 | V |
| $V_{(VDDLP12)}$ | Core power 1.1 V (supplemental 1.1 V) | ±5% tolerance | 1.045 | 1.1 | 1.155 | V |
| $V_{(VCC18)}$ | All 1.8-V I/O power:<br>(1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins.) | ±8.5% tolerance | 1.64 | 1.8 | 1.96 | V |
| $V_{(VCC\_INTF)}$ | Host or parallel interface I/O power: 1.8 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins) | ±8.5% tolerance | 1.64 | 1.8 | 1.96 | V |
| $V_{(VCC\_FLSH)}$ | Flash interface I/O power: 1.8 V to 3.3 V | ±8.5% tolerance See [1] | 1.64 | 1.8 | 1.96 | V |
| | | | 2.28 | 2.5 | 2.72 | |
| | | | 3.02 | 3.3 | 3.58 | |
| $V_{(VDD\_PLLM)}$ | MCG PLL 1.1-V power | ±9.1% tolerance See [2] | 1.025 | 1.1 | 1.155 | V |
| $V_{(VDD\_PLLD)}$ | DCG PLL 1.1-V power | ±9.1% tolerance See [2] | 1.025 | 1.1 | 1.155 | V |
| $T_A$ | Operating ambient temperature range[3] | | –30 | | 85 | °C |
| $T_J$ | Operating junction temperature | | –30 | | 105 | °C |

(1) These supplies have multiple valid ranges corresponding to the possible nominal voltages 1.8 V, 2.5 V, or 3.3 V.
(2) These I/O supply ranges are wider to facilitate additional filtering.
(3) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which will impact $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
   (a) $T_{a\_min} = T_{j\_min} - (P_{d\_min} \times R_{\theta JA}) = -30°C - (0.0\ W \times 30.3°C/W) = -30°C$
   (b) $T_{a\_max} = T_{j\_max} - (P_{d\_max} \times R_{\theta JA}) = 105°C - (0.348\ W \times 30.3°C/W) = 94.4°C$

## 6.4 Thermal Information

| THERMAL METRIC[1] | | | DLPC3437 | UNIT |
|---|---|---|---|---|
| | | | ZEZ (NFBGA) | |
| | | | 201 PINS | |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | 10.1 | °C/W |
| $R_{\theta JA}$[2] | Junction-to-air thermal resistance | At 0 m/s of forced airflow | 28.8 | °C/W |
| | | At 1 m/s of forced airflow | 25.3 | |
| | | At 2 m/s of forced airflow | 24.4 | |
| $\psi_{JT}$[3] | Temperature variance from junction to package top center temperature, per unit power dissipation | | 0.23 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC3437 test PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2°C/W) ≈ 1.00°C temperature rise.

## 6.5 Electrical Characteristics Over Recommended Operating Conditions

see [1][2][3][4]

| PARAMETER | | TEST CONDITIONS[5][6] | MIN | TYP[7] | MAX[8] | UNIT |
|---|---|---|---|---|---|---|
| $I_{(VDD)}$ | Core current 1.1 V (main 1.1 V) | IDLE disabled, 1920 × 1080, 60 Hz | | 188 | 334 | mA |
| $I_{(VDD\_PLLM)}$ | MCG PLL 1.1-V current | IDLE disabled, 1920 × 1080, 60 Hz | | 4 | 7 | mA |
| $I_{(VDD\_PLLD)}$ | DCG PLL 1.1-V current | IDLE disabled, 1920 × 1080, 60 Hz | | 4 | 7 | mA |
| $I_{(VDD)}$ + $I_{(VDD\_PLLM)}$ + $I_{(VDD\_PLLD)}$ | Core Current 1.1 V + MCG PLL 1.1-V current + DCG PLL 1.1-V current | IDLE disabled, 1920 × 1080, 60 Hz | | 196 | 348 | mA |
| $I_{(VCC18)}$ | Main 1.8-V I/O current: 1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes sub-LVDS DMD I/O , RESETZ, PARKZ, LED_SEL, CMP, GPIO, IIC1, TSTPT and JTAG pins | IDLE disabled, 1920 × 1080, 60 Hz | | | 62 | mA |
| $I_{(VCC\_INTF)}$ | Host or parallel interface I/O current: 1.8 V ( includes IIC0, PDATA, video syncs, and HOST_IRQ pins) | IDLE disabled, 1920 × 1080, 60 Hz | | | 3 | mA |
| $I_{(VCC\_FLSH)}$ | Flash Interface I/O current: 1.8 V to 3.3 V | IDLE disabled, 1920 × 1080, 60 Hz | | 1 | 1.5 | mA |
| $I_{(VCC18)}$ + $I_{(VCC\_INTF)}$ + $I_{(VCC\_FLSH)}$ | Main 1.8 V I/O current + $V_{CC\_INTF}$ current + $V_{CC\_FLSH}$ current | IDLE disabled, 1920 × 1080, 60 Hz | | 30 | 66.5 | mA |

(1) Assumes 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT or HVT cells.
(2) Programmable host and flash I/O are at minimum voltage (that is 1.8 V) for this typical scenario.
(3) Max currents column use typical motion video as the input. The typical currents column uses SMPTE color bars as the input.
(4) Some applications may be forced to use 1-oz. copper to manage ASIC package heat.
(5) Chipset input image is 1920 × 1080 (1080p) 24-bits on the FPGA parallel interface at the frame rate shown with a 0.33-inch 1080p DMD.
(6) In normal operation while displaying an image with CAIC enabled.
(7) Assumes typical case power PVT condition = nominal process, typical voltage, typical temperature (55°C junction), a 0.33-inch 1080p DMD.
(8) Assumes worse case power PVT condition = corner process, high voltage, high temperature (105°C junction), a 0.33-inch 1080p DMD.

## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) [1] [2]

| PARAMETER[3] | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input threshold voltage | I²C buffer (I/O type 7) | | $0.7 \times V_{CC\_INTF}$ | | [1] | V |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | | 1.17 | | 3.6 | |
| | | 1.8-V LVTTL (I/O type 1, 6) identified below: [2] CMP_OUT; PARKZ; RESETZ; GPIO 0 →19 | | 1.3 | | 3.6 | |
| | | 2.5-V LVTTL (I/O type 5, 9, 11, 12, 13) | | 1.7 | | 3.6 | |
| | | 3.3-V LVTTL (I/O type 5, 9, 11, 12, 13) | | 2 | | 3.6 | |
| $V_{IL}$ | Low-level input threshold voltage | I²C buffer (I/O type 7) | | −0.5 | | $0.3 \times V_{CC\_INTF}$ | V |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | | −0.3 | | 0.63 | |
| | | 1.8-V LVTTL (I/O type 1, 6) identified below: [2] CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19 | | −0.3 | | 0.5 | |
| | | 2.5-V LVTTL (I/O type 5, 9, 11, 12, 13) | | −0.3 | | 0.7 | |
| | | 3.3-V LVTTL (I/O type 5, 9, 11, 12, 13) | | −0.3 | | 0.8 | |
| $V_{CM}$ | Steady-state common mode voltage | 1.8-V sub-LVDS (DMD high speed) (I/O type 4) | | 0.8 | 0.9 | 1 | mV |
| |$V_{OD}$| | Differential output magnitude | 1.8-V sub-LVDS (DMD high speed) (I/O type 4) | | | 200 | | mV |
| $V_{OH}$ | High-level output voltage | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | | 1.35 | | | V |
| | | 2.5-V LVTTL (I/O type 12, 13) | | 1.7 | | | |
| | | 3.3-V LVTTL (I/O type 12, 13) | | 2.4 | | | |
| | | 1.8-V sub-LVDS – DMD high speed (I/O type 4) | | | 1 | | |
| $V_{OL}$ | Low-level output voltage | I²C buffer (I/O type 7) | $V_{CC\_INTF} > 2$ V | | | 0.4 | V |
| | | I²C buffer (I/O type 7) | $V_{CC\_INTF} < 2$ V | | | $0.2 \times V_{CC\_INTF}$ | |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | | | | 0.45 | |
| | | 2.5 V LVTTL (I/O type 12, 13) | | | | 0.7 | |
| | | 3.3 V LVTTL (I/O type 12, 13) | | | | 0.4 | |
| | | 1.8-V sub-LVDS – DMD high speed (I/O type 4) | | | 0.8 | | |

(1) I/O is high voltage tolerant; that is, if $V_{CC} = 1.8$ V, the input is 3.3-V tolerant, and if $V_{CC} = 3.3$ V, the input is 5-V tolerant.
(2) ASIC pins: CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19 have slightly varied $V_{IH}$ and $V_{IL}$ range from other 1.8-V I/O.
(3) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)[1][2]

| PARAMETER[3] | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OH}$ | High-level output current | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | 4 mA | 2 | | mA |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | 8 mA | 3.5 | | |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | 24 mA | 10.6 | | |
| | | 2.5-V LVTTL (I/O type 13) | 8 mA | 10.8 | | |
| | | 2.5-V LVTTL (I/O type 12, 13) | 24 mA | 28.7 | | |
| | | 3.3-V LVTTL (I/O type 13) | 8 mA | 15 | | |
| $I_{OL}$ | Low-level output current | I²C buffer (I/O type 7) | | 3 | | mA |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | 4 mA | 2.3 | | |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | 8 mA | 4.6 | | |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | 24 mA | 13.9 | | |
| | | 2.5-V LVTTL (I/O type 13) | 8 mA | 10.4 | | |
| | | 2.5-V LVTTL (I/O type 12, 13) | 24 mA | 31.1 | | |
| | | 3.3-V LVTTL (I/O type 13) | 8 mA | 8.9 | | |
| $I_{OZ}$ | High-impedance leakage current | I²C buffer (I/O type 7) | $0.1 \times V_{CC\_INTF} < V_I$ $< 0.9 \times V_{CC\_INTF}$ | −10 | | 10 | µA |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | | −10 | | 10 |
| | | 2.5-V LVTTL (I/O type 5, 9, 11, 12, 13) | | −10 | | 10 |
| | | 3.3-V LVTTL (I/O type 5, 9, 11, 12, 13) | | −10 | | 10 |
| $C_I$ | Input capacitance (including package) | I²C buffer (I/O type 7) | | | | 5 | pF |
| | | 1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13) | | 2.6 | | 3.5 |
| | | 2.5-V LVTTL (I/O type 5, 9, 11, 12, 13) | | 2.6 | | 3.5 |
| | | 3.3-V LVTTL (I/O type 5, 9, 11, 12, 13) | | 2.6 | | 3.5 |
| | | 1.8-V sub-LVDS – DMD high speed (I/O type 4) | | | | 3 |

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## 6.7 High-Speed Sub-LVDS Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CM}$ | Steady-state common mode voltage | 0.8 | 0.9 | 1.0 | V |
| $V_{CM}$ ($\Delta$pp)[1] | $V_{CM}$ change peak-to-peak (during switching) | | | 75 | mV |
| $V_{CM}$ ($\Delta$ss)[1] | $V_{CM}$ change steady state | −10 | | 10 | mV |
| $|V_{OD}|$[2] | Differential output voltage magnitude | | 200 | | mV |
| $V_{OD}$ ($\Delta$) | $V_{OD}$ change (between logic states) | −10 | | 10 | mV |
| $V_{OH}$ | Single-ended output voltage high | | 1.00 | | V |
| $V_{OL}$ | Single-ended output voltage low | | 0.80 | | V |
| $t_R$[2] | Differential output rise time | | | 250 | ps |
| $t_F$[2] | Differential output fall time | | | 250 | ps |
| $t_{MAX}$ | Max switching rate | | | 1200 | Mbps |
| $DC_{out}$ | Output duty cycle | 45% | 50% | 55% | |
| $Tx_{term}$[1] | Internal differential termination | 80 | 100 | 120 | Ω |
| $Tx_{load}$ | 100-Ω differential PCB trace (50-Ω transmission lines) | 0.5 | | 6 | inches |

(1) For the definition of $V_{CM}$ changes, see Figure 2.
(2) Note that $V_{OD}$ is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of this voltage swing relative to 0. Rise and fall times are defined for the differential $V_{OD}$ signal as follows in Figure 3.

## 6.8 Low-Speed SDR Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | ID | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Operating voltage | $V_{CC18}$ (all signal groups) | | 1.64 | 1.96 | V |
| DC input high voltage | $V_{IHD(DC)}$ Signal group 1 | All | $0.7 \times V_{CC18}$ | $V_{CC18} + 0.5$ | V |
| DC input low voltage[1] | $V_{ILD(DC)}$ Signal group 1 | All | –0.50 | $0.3 \times V_{CC18}$ | V |
| AC input high voltage[2] | $V_{IHD(AC)}$ Signal group 1 | All | $0.8 \times V_{CC18}$ | $V_{CC18} + 0.5$ | V |
| AC input low voltage | $V_{ILD(AC)}$ Signal group 1 | All | –0.5 | $0.2 \times V_{CC18}$ | V |
| Slew rate [3][4][5][6] | Signal group 1 | | 1 | 3.0 | V/ns |
| | Signal group 2 | | 0.25 | | |
| | Signal group 3 | | 0.5 | | |

(1)   $V_{ILD(AC)}$ min applies to undershoot.
(2)   $V_{IHD(AC)}$ max applies to overshoot.
(3)   Signal group 1 output slew rate for rising edge is measured between $V_{ILD(DC)}$ to $V_{IHD(AC)}$.
(4)   Signal group 1 output slew rate for falling edge is measured between $V_{IHD(DC)}$ to $V_{ILD(AC)}$.
(5)   Signal group 1: See Figure 4.
(6)   Signal groups 2 and 3 output slew rate for rising edge is measured between $V_{ILD(AC)}$ to $V_{IHD(AC)}$.

## 6.9 System Oscillators Timing Requirements

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, MOSC[1] | Option 1: 24-MHz oscillator | 23.998 | 24.002 | MHz |
| $t_c$ | Cycle time, MOSC[1] | Option 1: 24-MHz oscillator | 41.670 | 41.663 | ns |
| $t_{w(H)}$ | Pulse duration, MOSC, high | 50% to 50% reference points (signal) | | 40 $t_c$% | |
| $t_{w(L)}$ | Pulse duration, MOSC, low | 50% to 50% reference points (signal) | | 40 $t_c$% | |
| $t_t$ | Transition time, MOSC, $t_t = t_f / t_r$ | 20% to 80% reference points (signal) | | 10 | ns |
| $t_{jp}$ | Long-term, peak-to-peak, period jitter[2], MOSC (that is the deviation in period from ideal period due solely to high frequency jitter) | | | 2% | |

(1) The frequency accuracy for MOSC is ±200 PPM. This includes impact to accuracy due to aging, temperature, and trim sensitivity.
(2) The MOSC input cannot support spread spectrum clock spreading.

## 6.10 Power-Up and Reset Timing Requirements

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(L)}$ | Pulse duration, inactive low, RESETZ | 50% to 50% reference points (signal) | 1.25 | | µs |
| $t_t$ | Transition time, RESETZ[1], $t_t = t_f / t_r$ | 20% to 80% reference points (signal) | | 0.5 | µs |

(1) For more information on RESETZ, see *Pin Configuration and Functions*.

## 6.11 Parallel Interface Frame Timing Requirements

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{p\_vsw}$ | Pulse duration – VSYNC_WE high | 50% reference points | 1 | | lines |
| $t_{p\_vbp}$ | Vertical back porch (VBP) – time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line (see [1]) | 50% reference points | 2 | | lines |
| $t_{p\_vfp}$ | Vertical front porch (VFP) – time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE (see [1]) | 50% reference points | 1 | | lines |
| $t_{p\_tvb}$ | Total vertical blanking – time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame (This is equal to the sum of VBP ($t_{p\_vbp}$) + VFP ($t_{p\_vfp}$)). | 50% reference points | See [1] | | lines |
| $t_{p\_hsw}$ | Pulse duration – HSYNC_CS high | 50% reference points | 4 | 128 | PCLKs |
| $t_{p\_hbp}$ | Horizontal back porch – time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD | 50% reference points | 4 | | PCLKs |
| $t_{p\_hfp}$ | Horizontal front porch – time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS | 50% reference points | 8 | | PCLKs |
| $t_{p\_thb}$ | Total horizontal blanking – sum of horizontal front and back porches | 50% reference points | See [2] | | PCLKs |

(1) The minimum total vertical blanking is defined by the following equation: $t_{p\_tvb}(min) = 6 + [8 \times Max(1, Source\_ALPF/ DMD\_ALPF)]$ lines
where:
(a) SOURCE_ALPF = Input source active lines per frame.
(b) DMD_ALPF = Actual DMD used lines per frame supported.
(2) Total horizontal blanking is driven by the max line rate for a given source which will be a function of resolution and orientation. The following equation can be applied for this: $t_{p\_thb} = Roundup[(1000 \times f_{clock})/ LR] – APPL$
where:
(a) $f_{clock}$ = Pixel clock rate in MHz.
(b) LR = Line rate in kHz.
(c) APPL is the number of active pixels per (horizontal) line.
(d) If $t_{p\_thb}$ is calculated to be less than $t_{p\_hbp} + t_{p\_hfp}$ then the pixel clock rate is too low or the line rate is too high, and one or both must be adjusted.

## 6.12 Parallel Interface General Timing Requirements[1]

see [2]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, PCLK | | 1.0 | 150.0 | MHz |
| $t_{p\_clkper}$ | Clock period, PCLK | 50% reference points | 6.66 | 1000 | ns |
| $t_{p\_clkjit}$ | Clock jitter, PCLK | Max $f_{clock}$ | See [3] | See [3] | |
| $t_{p\_wh}$ | Pulse duration low, PCLK | 50% reference points | 2.43 | | ns |
| $t_{p\_wl}$ | Pulse duration high, PCLK | 50% reference points | 2.43 | | ns |
| $t_{p\_su}$ | Setup time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid before the active edge of PCLK | 50% reference points | 0.9 | | ns |
| $t_{p\_h}$ | Hold time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid after the active edge of PCLK | 50% reference points | 0.9 | | ns |
| $t_t$ | Transition time – all signals | 20% to 80% reference points | 0.2 | 2.0 | ns |

(1)    The active (capture) edge of PCLK for HSYNC_CS, DATEN_CMD and PDATA(23:0) is software programmable, but defaults to the rising edge.
(2)    The I/O pin TSTPT_6 must be left open for 24-MHz timing to work properly inside the DLPC3437.
(3)    Clock jitter (in ns) should be calculated using this formula: Jitter = [1 / $f_{clock}$ – 5.76 ns]. Setup and hold times must be met during clock jitter.

## 6.13  Flash Interface Timing Requirements

The DLPC3437 ASIC flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC3437 can support 1- to 64-Mb flash memories. [1] [2]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, SPI_CLK | See [3] | 1.42 | 36.0 | MHz |
| $t_{p\_clkper}$ | Clock period, SPI_CLK | 50% reference points | 704 | 27.7 | ns |
| $t_{p\_wh}$ | Pulse duration low, SPI_CLK | 50% reference points | 352 | | ns |
| $t_{p\_wl}$ | Pulse duration high, SPI_CLK | 50% reference points | 352 | | ns |
| $t_t$ | Transition time – all signals | 20% to 80% reference points | 0.2 | 3.0 | ns |
| $t_{p\_su}$ | Setup time – SPI_DIN valid before SPI_CLK falling edge | 50% reference points | 10.0 | | ns |
| $t_{p\_h}$ | Hold time – SPI_DIN valid after SPI_CLK falling edge | 50% reference points | 0.0 | | ns |
| $t_{p\_clqv}$ | SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ | 50% reference points | | 1.0 | ns |
| $t_{p\_clqx}$ | SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ | 50% reference points | –3.0 | 3.0 | ns |

(1)  Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC3437 does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC3437 hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2)  With the above output timing, DLPC3437 provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
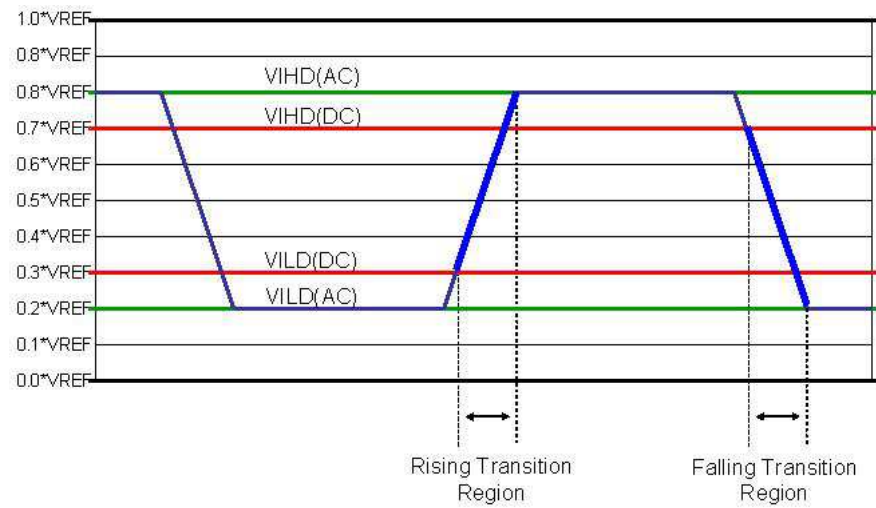(3)  This range includes the 200 ppm of the external oscillator (but no jitter).
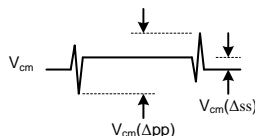


**Figure 2.  Definition of V$_{CM}$ Changes**
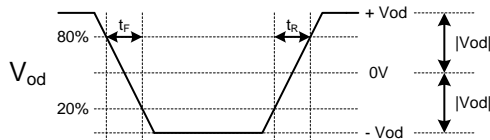

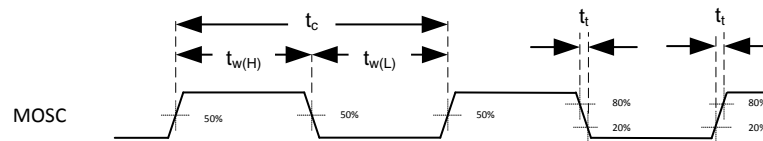
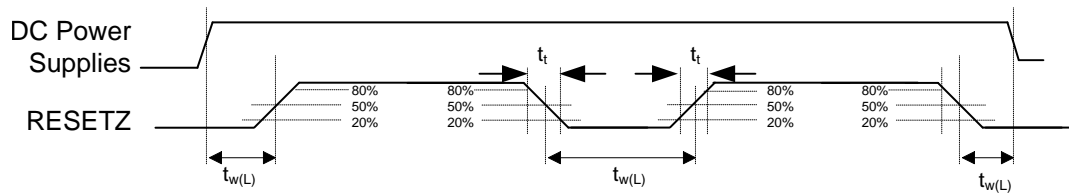NOTE:  V$_{CM}$ is removed when the signals are viewed differentially.

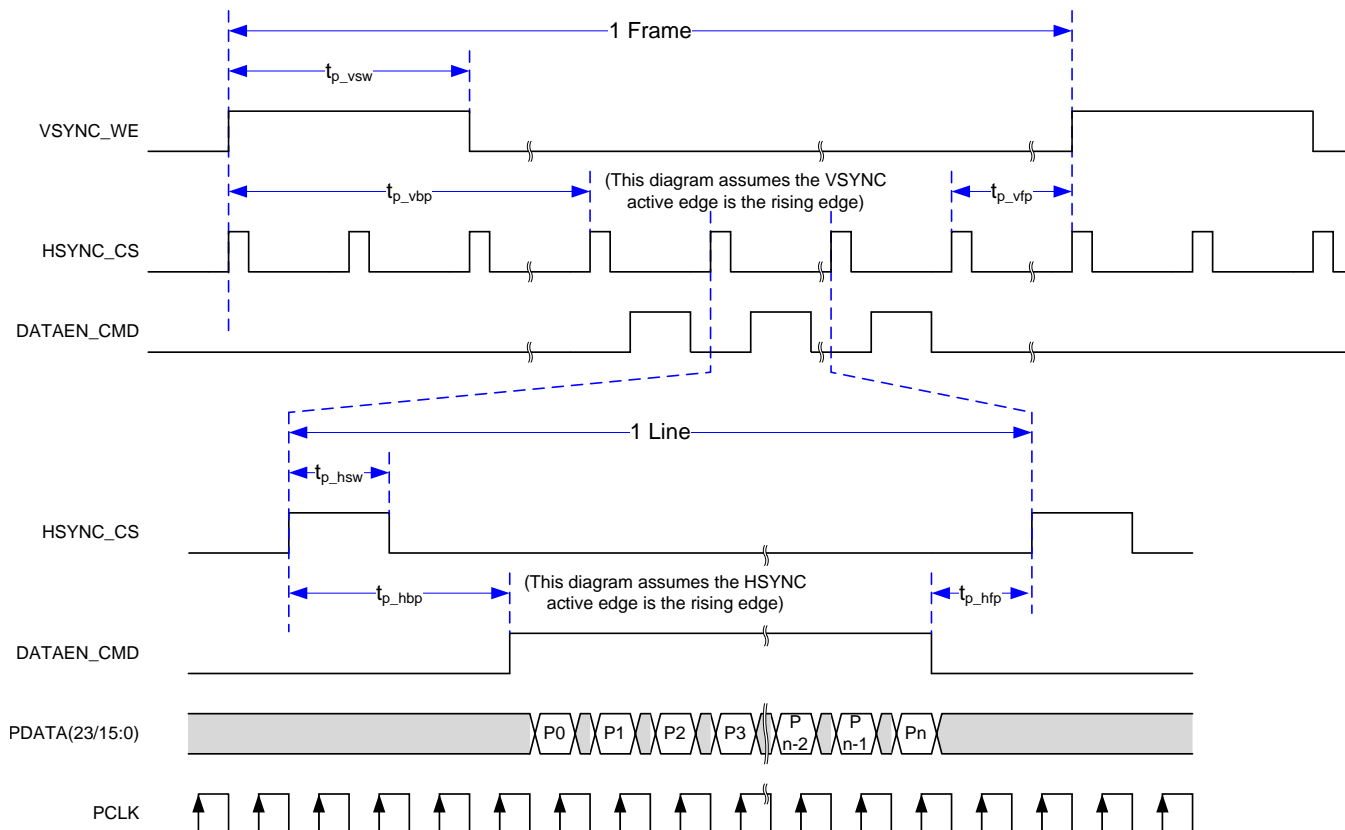**Figure 3.  Differential Output Signal**

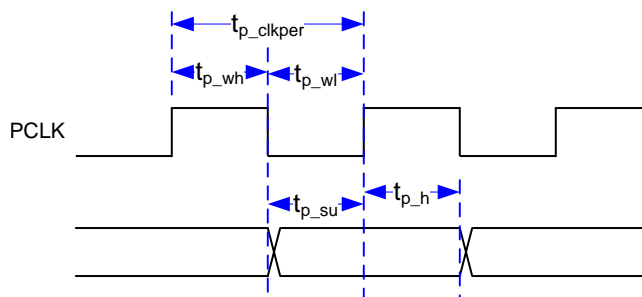**Figure 4. Low Speed (LS) I/O Input Thresholds**



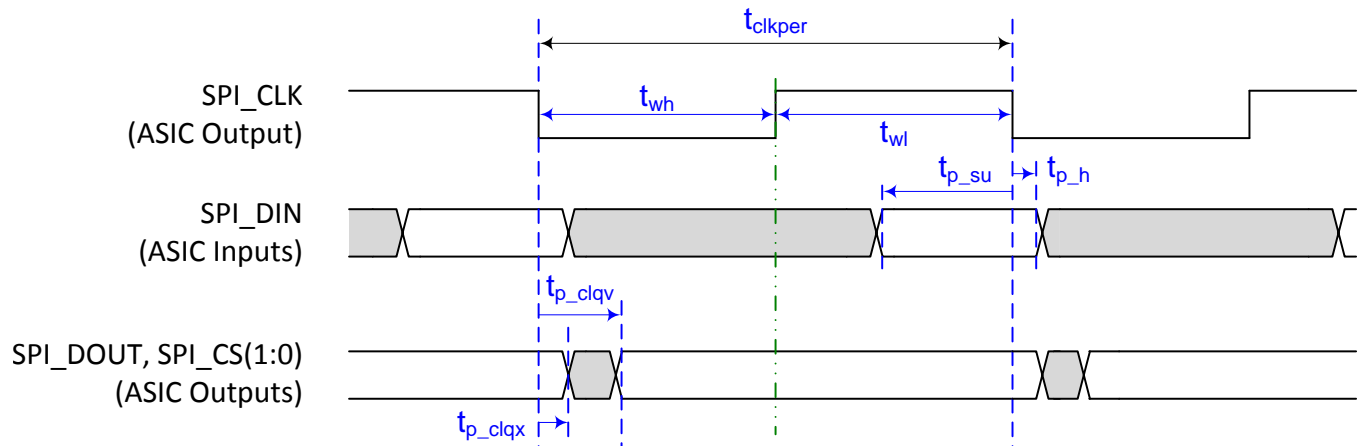**Figure 5. System Oscillators**



**Figure 6. Power-Up and Power-Down RESETZ Timing**

**Figure 7. Parallel Interface Frame Timing**



**Figure 8. Parallel Interface General Timing**

**Figure 9. Flash Interface Timing**

# 7 Parameter Measurement Information

## 7.1 HOST_IRQ Usage Model

- While reset is applied, HOST_IRQ will reset to tri-state (an external pullup pulls the line high).
- HOST_IRQ will remain tri-state (pulled high externally) until the microprocessor boot completes. While the signal is pulled high, this indicates that the DLPC3437 is performing boot-up and auto-initialization.
- As soon as possible after boot-up, the microprocessor will drive HOST_IRQ to a logic high state to indicate that the DLPC3437 is continuing to perform auto-initialization (no real state change occurs on the external signal).
- Upon completion of the chip set auto-initialization, software will set HOST_IRQ to a logic low state to indicate the completion of auto-initialization. (At the falling edge, the system is said to enter the INIT_DONE state).
- The 500-ms max shown from the rising edge of RESETZ to the falling edge of HOST_IRQ may become longer than 500 ms if many commands are added to the autoinit batch file in flash which automatically runs at power up.
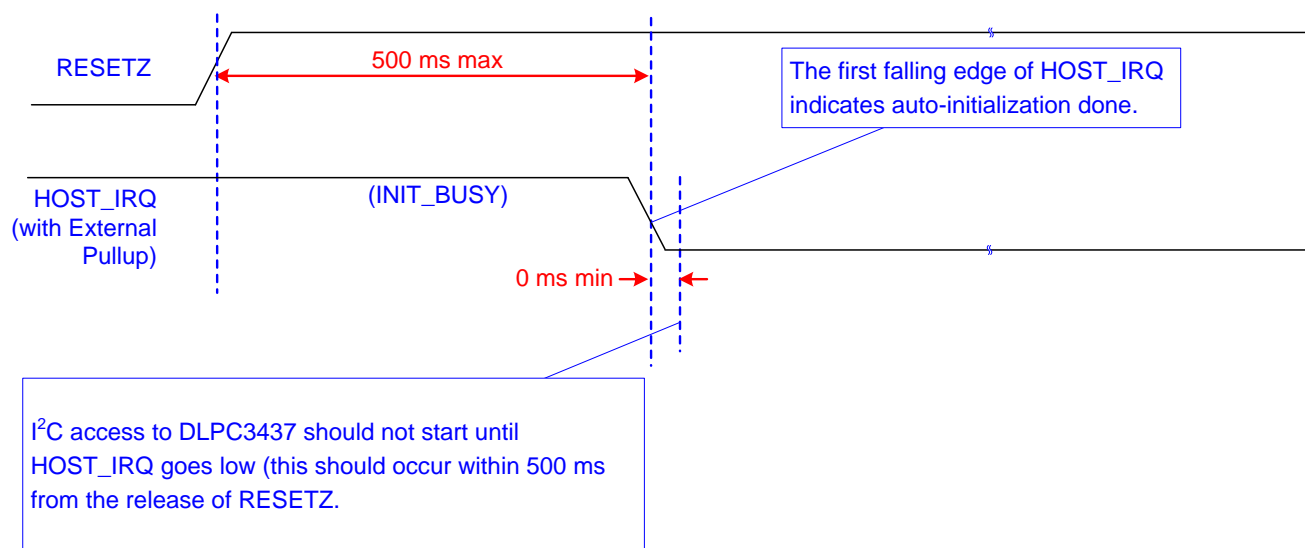


**Figure 10. Host IRQ Timing**

## 7.2   Input Source - Frame Rates and 3-D Display Operation

### Table 3. Supported Input Source Ranges[1][2][3][4]

| INTERFACE | BITS / PIXEL [5] | IMAGE TYPE | SOURCE RESOLUTION RANGE[6] | | | | FRAME RATE RANGE |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | | HORIZONTAL | | VERTICAL | | |
| | | | Landscape | Portrait | Landscape | Portrait | |
| Parallel | 24 | 2D - 1080p | 1920 | N/A | 1080 | N/A | 50 ± 2 Hz, 60 ± 2 Hz |
| Parallel | 24 | 2D - WXGA | 1366 | N/A | 768 | N/A | 50 ± 2 Hz, 60 ± 2 Hz |
| Parallel | 24 | 2D - 720p | 1280 | N/A | 720 | N/A | 50 ± 2 Hz, 60 ± 2 Hz |
| Parallel | 24 | 3D - 1080p[7] | 1920 | N/A | 1080 | N/A | 48 ± 2 Hz |
| Parallel | 24 | 3D - 720p[7] | 1280 | N/A | 720 | N/A | 100 ± 2 Hz, 120 ± 2 Hz |

(1)   The user must stay within specifications for all source interface parameters such as max clock rate and max line rate.
(2)   The max DMD size for all rows in the table is 1366 x 768.
(3)   To achieve the ranges stated, the composer-created firmware used must be defined to support the source parameters used.
(4)   These interfaces are supported with the DMD sequencer sync mode command (3Bh) set to auto.
(5)   Bits / Pixel does not necessarily equal the number of data pins used on the DLPC343x. Fewer pins are used if multiple clocks are used per pixel transfer.
(6)   The DLPC3437 only supports Landscape orientation.
(7)   Formatted as Frame Sequential.

The DLPC3437 will support both 2D and 3D sources on the parallel interface. The frame and sub-frame timing for 2D sources is shown in Figure 11 while the frame and sub-frame timing for 3D sources is shown in Figure 12.
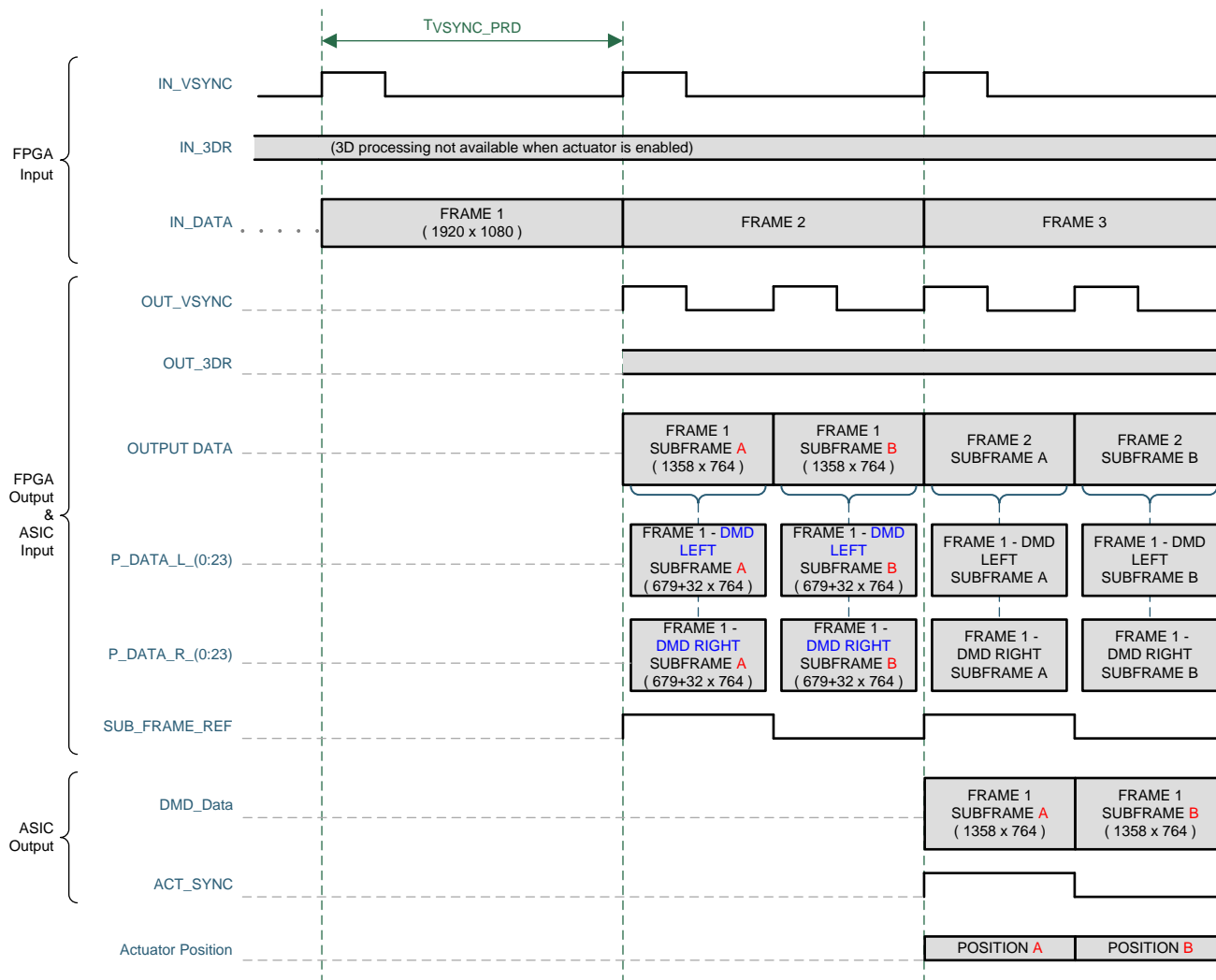


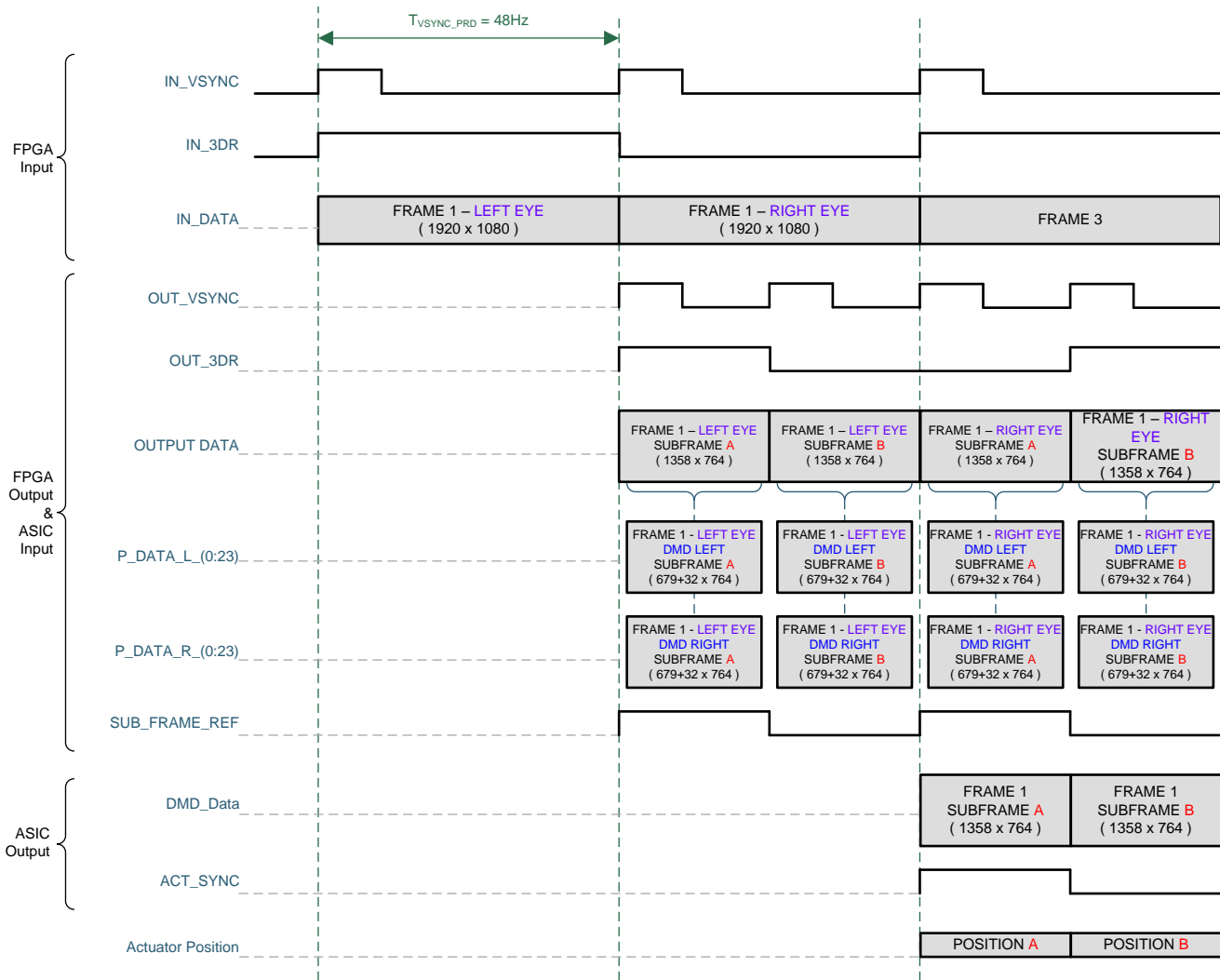**Figure 11.  DLPC3437 2D Actuator Frame and Signal Timing**

**Figure 12. DLPC3437 3D Frame and Signal Timing**

### 7.2.1 Parallel Interface Data Transfer Format

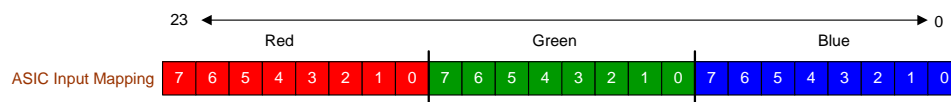The data format on the PDATA(23:0) bus between the 0.33 1080p FPGA and the DLPC3439 is always RGB888, as shown in Figure 13.



**Figure 13. RGB-888 I/O Mapping**

# 8 Detailed Description

## 8.1 Overview

The DLPC3437 is the display controller for the DLP3310 (0.33 1080p) DMD. The DLPC3437 is part of the chipset comprising the DLPC3437 controller, the DLP3310 (0.33 1080p) DMD, and the DLPA3000 PMIC/LED driver. All three components of the chipset must be used in conjunction with each other, along with the XC7Z020-1CLG484I4493 FPGA, for reliable operation of the DLP3310 (0.33 1080p) DMD. The DLPC3437 display controller provides data/image processing functions that are optimized for small form factor and power-constrained display applications. Applications include pico projectors, wearable displays, and digital signage. Standalone projectors must include a separate front-end chip to interface to the outside world (for example, video decoder, HDMI receiver, triple ADC, or USB I/F chip).

## 8.2 Functional Block Diagram
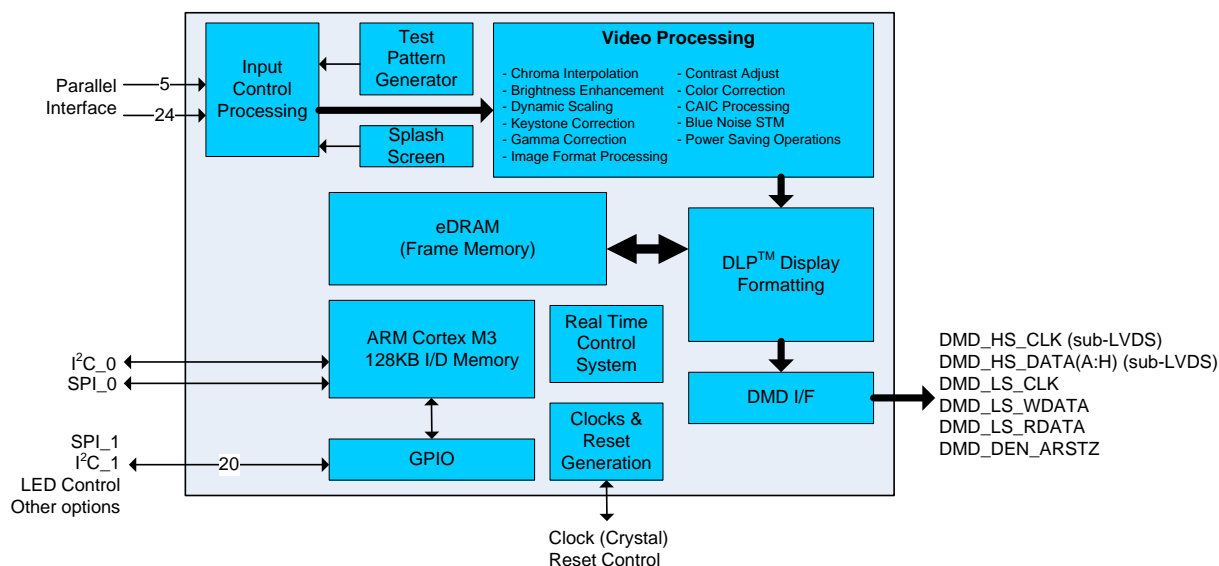


## 8.3 Feature Description

### 8.3.1 Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC3437 ASIC.

#### 8.3.1.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, with the addition of the SUB_FRAME signal (which is a necessary output from the XC7Z020-1CLG484I4493 FPGA). The standard graphics interface protocol includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs and the active edge of the clock are programmable. Figure 7 shows the relationship of these signals.

> **NOTE**
> VSYNC_WE must remain active at all times (in lock-to-VSYNC mode) or the display sequencer will stop and cause the LEDs to be turned off.

### 8.3.2 Serial Flash Interface

DLPC3437 uses an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported is 64 Mb.

## Feature Description (continued)

For access to flash, the DLPC3437 uses a single SPI interface operating at a programmable frequency complying to industry standard SPI flash protocol. The programmable SPI frequency is defined to be equal to 180 MHz/N, where N is a programmable value between 5 to 127 providing a range from 36.0 to 1.41732 MHz. Note that this results in a relatively large frequency step size in the upper range (for example, 36 MHz, 30 MHz, 25.7 MHz, 22.5 MHz, and so forth) and thus this must be taken into account when choosing a flash device.

The DLPC3437 supports two independent SPI chip selects; however, the flash must be connected to SPI chip select zero (SPI0_CSZ0) because the boot routine is only executed from the device connected to chip select zero (SPI0_CSZ0). The boot routine uploads program code from flash to program memory, then transfers control to an auto-initialization routine within program memory. The DLPC3437 asserts the HOST_IRQ output signal high while auto-initialization is in progress, then drives it low to signal its completion to the host processor. Only after auto-initialization is complete will the DLPC3437 be ready to receive commands through I$^2$C.

The DLPC3437 should support any flash device that is compatible with the modes of operation, features, and performance as defined in Table 4 and Table 5.

**Table 4. SPI Flash Required Features or Modes of Operation**

| Feature | DLPC3437 Requirement |
|---|---|
| SPI interface width | Single |
| SPI protocol | SPI mode 0 |
| Fast READ addressing | Auto-incrementing |
| Programming mode | Page mode |
| Page size | 256 B |
| Sector size | 4 kB sector |
| Block size | Any |
| Block protection bits | 0 = Disabled |
| Status register bit(0) | Write in progress (WIP), also called flash busy |
| Status register bit(1) | Write enable latch (WEN) |
| Status register bits(6:2) | A value of 0 disables programming protection |
| Status register bit(7) | Status register write protect (SRWP) |
| Status register bits(15:8) (that is expansion status byte) | The DLPC3437 only supports single-byte status register R/W command execution, and thus may not be compatible with flash devices that contain an expansion status byte. However, as long as expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the device should be compatible with DLPC3437. |

To support flash devices with program protection defaults of either enabled or disabled, the DLPC3437 always assumes the device default is enabled and goes through the process of disabling protection as part of the boot-up process. This process consists of:

- A write enable (WREN) instruction executed to request write enable, followed by
- A read status register (RDSR) instruction is then executed (repeatedly as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction is executed that writes 0 to all 8-bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC3437 issues:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction is executed
- Note the flash automatically clears the write enable status after each program and erase instruction

The specific instruction OpCode and timing compatibility requirements are listed in Table 6 and Table 7. Note however that DLPC3437 does not read the flash's electronic signature ID and thus cannot automatically adapt protocol and clock rate based on the ID.

**Table 5. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements**

| SPI Flash Command | First Byte (OPCODE) | Second Byte | Third Byte | Fourth Byte | Fifth Byte | Sixth Byte |
|---|---|---|---|---|---|---|
| Fast READ (1 Output) | 0x0B | ADDRS(0) | ADDRS(1) | ADDRS(2) | dummy | DATA(0)[1] |
| Read status | 0x05 | N/A | N/A | STATUS(0) | | |
| Write status | 0x01 | STATUS(0) | [2] | | | |
| Write enable | 0x06 | | | | | |
| Page program | 0x02 | ADDRS(0) | ADDRS(1) | ADDRS(2) | DATA(0)[1] | |
| Sector erase (4 kB) | 0x20 | ADDRS(0) | ADDRS(1) | ADDRS(2) | | |
| Chip erase | 0xC7 | | | | | |

(1)   Only the first data byte is show, data continues.
(2)   DLPC3437 does not support access to a second/expansion Write Status byte.

The specific and timing compatibility requirements for a DLPC3437 compatible flash are listed in Table 6 and Table 7.

**Table 6. SPI Flash Key Timing Parameter Compatibility Requirements[1][2]**

| SYMBOL | ALTERNATE SYMBOL | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_R$ | $f_C$ | Access frequency (all commands) | ≤ 1.42 | | MHz |
| $t_{SHSL}$ | $t_{CSH}$ | Chip select high time (also called chip select deselect time) | ≤ 200 | | ns |
| $t_{CLQX}$ | $t_{HO}$ | Output hold time | ≥ 0 | | ns |
| $t_{CLQV}$ | $t_V$ | Clock low to output valid time | | ≤ 11 | ns |
| $t_{DVCH}$ | $t_{DSU}$ | Data in set-up time | ≤ 5 | | ns |
| $t_{CHDX}$ | $t_{DH}$ | Data in hold time | ≤ 5 | | ns |

(1)   The timing values are related to the specification of the flash device itself, not the DLPC3437.
(2)   The DLPC3437 does not drive the HOLD or WP (active low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB through an external pullup.

The DLPC3437 supports 1.8-, 2.5-, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 7 contains a list of 1.8-, 2.5-, and 3.3-V compatible SPI serial flash devices supported by DLPC3437.

### 8.3.3 Tested Flash Devices

**Table 7. DLPC3437 Compatible SPI Flash Device Options (3.3-V Compatible Devices)[1] [2]**

| DVT[3] | DENSITY (Mb) | VENDOR | PART NUMBER | PACKAGE SIZE |
|---|---|---|---|---|
| Yes | 32 Mb | Winbond | W25Q32FVSSIG | 5.2 mm x 7.9 mm, 8-pin SOIC |
| Yes | 64 Mb | Winbond | W25Q64FVSSIG | 5.2 mm x 7.9 mm, 8-pin SOIC |

(1)    The flash supply voltage must match VCC_FLSH on the DLPC3437. Special attention needs to be paid when ordering devices to be sure the desired supply voltage is attained as multiple voltage options are often available under the same base part number.
(2)    Beware when considering Numonyx (Micron) serial flash devices as they typically do not have the 4 kB sector size needed to be DLPC3437 compatible.
(3)    All of the flash devices shown are compatible with the DLPC3437, but only those marked with yes in the DVT column have been validated during TI Validation testing using a TI reference design. Those marked with no can be used at the ODM's own risk. Other parts than those shown can be used if the timing conditions in *Serial Flash Interface* are met.

### 8.3.4 Serial Flash Programming

Note that the flash can be programmed through the DLPC3437 over I$^2$C or by driving the SPI pins of the flash directly while the DLPC3437 I/O are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the DLPC3437. Note that SPI0_CSZ1 is not tri-stated by this same action.

### 8.3.5 SPI Signal Routing

The DLPC3437 is designed to support two SPI slave devices on the SPI0 interface, specifically, a serial flash and the DLPA3000. This requires routing associated SPI signals to two locations while attempting to operate up to 36 MHz. Take special care to ensure that reflections do not compromise signal integrity. To this end, the following recommendations are provided:

• The SPI0_CLK PCB signal trace from the DLPC3437 source to each slave device should be split into separate routes as close to the DLPC3437 as possible. In addition, the SPI0_CLK trace length to each device should be equal in total length.
• The SPI0_DOUT PCB signal trace from the DLPC3437 source to each slave device should be split into separate routes as close to the DLPC3437 as possible. In addition, the SPI0_DOUT trace length to each device should be equal in total length(use the same strategy as SPI0_CLK).
• The SPI0_DIN PCB signal trace from each slave device to the point where they intersect on their way back to the DLPC3437 should be made equal in length and as short as possible. They should then share a common trace back to the DLPC3437.
• SPI0_CSZ0 and SPI0_CSZ1 need no special treatment because they are dedicated signals which drive only one device.

### 8.3.6 I$^2$C Interface Performance

Both DLPC3437 I$^2$C interface ports support 100-kHz baud rate. By definition, I$^2$C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

### 8.3.7 Content-Adaptive Illumination Control

Content-adaptive illumination control (CAIC) is an image processing algorithm that takes advantage of the fact that in common real-world image content most pixels in the images are well below full scale for the for the R, G, and B digital channels being input to the DLPC3437. As a result of this the average picture level (APL) for the overall image is also well below full scale, and the system's dynamic range for the collective set of pixel values is not fully utilized. CAIC takes advantage of this headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images frame by frame and derives three unique digital gains, one for each of the R, G, and B color channels. During CAIC image processing, each gain is applied to all pixels in the associated color channel. CAIC derives each color channel's gain that is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. Figure 14 and Figure 15 show an example of the application of CAIC for one color channel.
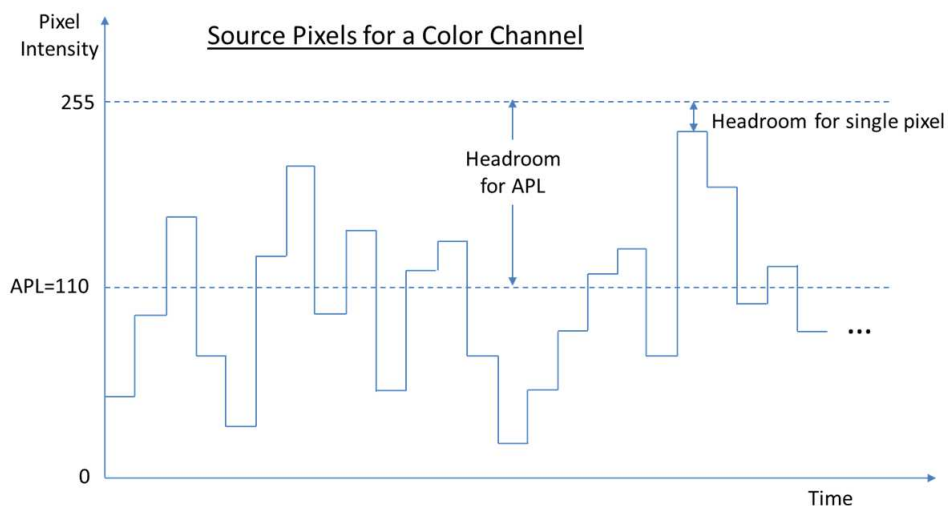
**Figure 14. Input Pixels Example**
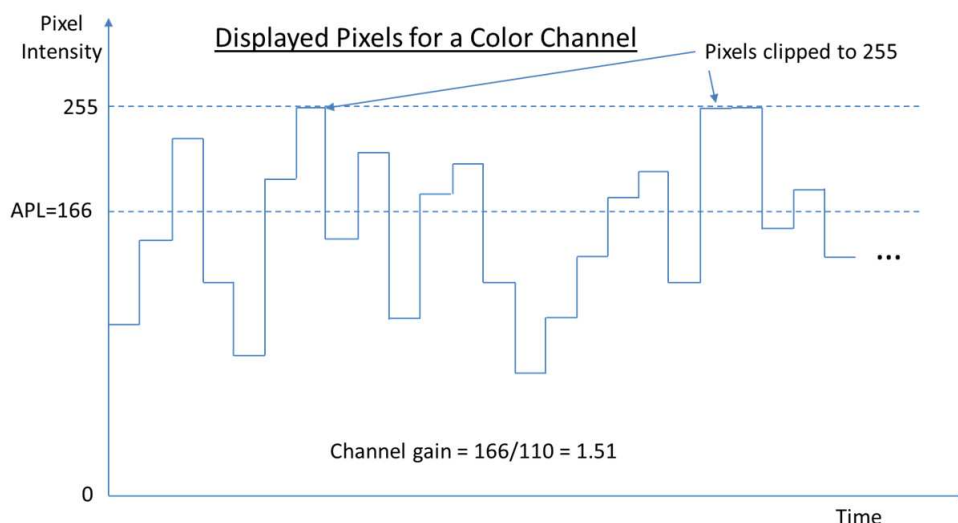


**Figure 15. Displayed Pixels After CAIC Processing**

Figure 15 shows the gain that is applied to a color processing channel inside the DLPC3437. CAIC will also adjust the power for the R, G, and B LED. For each color channel of an individual frame, CAIC will intelligently determine the optimal combination of digital gain and LED power. The decision regarding how much digital gain to apply to a color channel and how much to adjust the LED power for that color is heavily influenced by the software command settings sent to the DLPC3437 for configuring CAIC.

As CAIC applies a digital gain to each color channel independently, and adjusts each LED's power independently, CAIC also makes sure that the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

Since the R, G, and B channels can be gained up by CAIC inside the DLPC3437, the LED power can be turned down for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. Figure 16 shows an example of LED power reduction by CAIC for an image where the R and B LEDs can be turned down in power.

CAIC can alternatively be used to increase the overall brightness of an image while holding the total power for all LEDs constant. In summary, when CAIC is enabled CAIC can operate in one of two distinct modes:

- Power Reduction Mode – holds overall image brightness constant while reducing LED power
- Enhanced Brightness Mode – holds overall LED power constant while enhancing image brightness
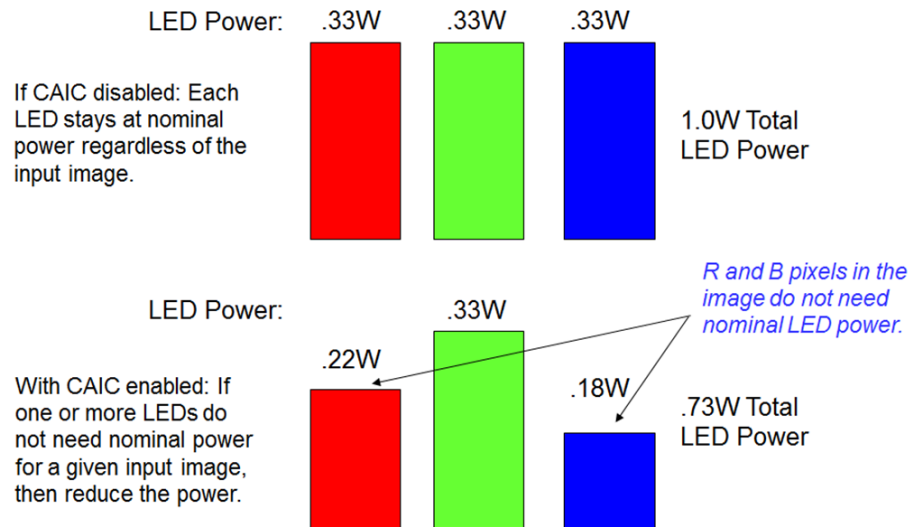


**Figure 16. CAIC Power Reduction Mode (for Constant Brightness)**

### 8.3.8 Local Area Brightness Boost (LABB)

LABB is an image processing algorithm that adaptively gains up regions of an image that are dim relative to the average picture level. Some regions of the image will have significant gain applied, and some regions will have little or no gain applied. LABB evaluates images frame by frame and derives the local area gains to be used uniquely for each image. Since many images have a net overall boost in gain even if some parts of the image get no gain, the overall perceived brightness of the image is boosted.

Figure 17 shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.
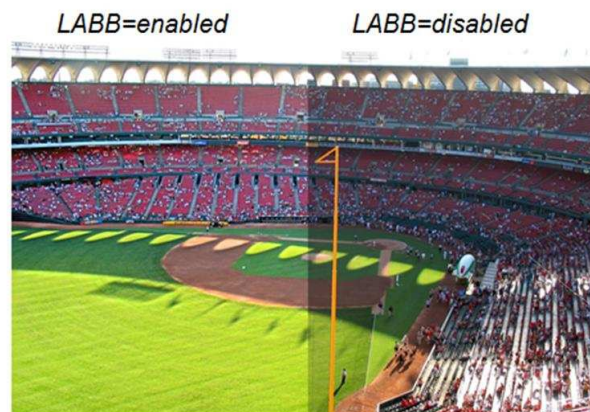


**Figure 17. Boosting Brightness in Local Areas of an Image**

LABB works best when the decision about the strength of gains used is determined by ambient light conditions. For this reason, an ambient light sensor can be read by an external processor each frame. Based on the sensor readings, the external processor can send LABB strength commands to apply higher gains for bright rooms to help overcome any washing out of images. LABB will receive commands to apply lower gains in dark rooms to prevent over-punching of images.

### 8.3.9  3-D Glasses Operation

For supporting 3D glasses, the DLPC3437-based chip set outputs sync information to synchronize the Left eye/Right eye shuttering in the glasses with the displayed DMD image frames.

Two different types of glasses are often used to achieve synchronization. One relies on an IR transmitter on the system PCB to send an IR sync signal to an IR receiver in the glasses. In this case DLPC3437 output signal GPIO_09 can be used to cause the IR transmitter to send an IR sync signal to the glasses. The timing for signal GPIO_09 is shown in Figure 18.

The second type of glasses relies on sync information that is encoded into the light being output from the projection lens. This is referred to as the DLP Link approach for 3D, and many 3D glasses from different suppliers have been built using this method. This demonstrates that the DLP Link method can work reliability. The advantage of the DLP Link approach is that it takes advantage of existing projector hardware to transmit the sync information to the glasses. This can save cost, size, and power in the projector.

For generating the DLP Link sync information, one light pulse per DMD frame is output from the projection lens while the glasses have both shutters closed. To achieve this, the DLPC3437 signals the DLPA3000 when to turn on the illumination source (typically LEDs or lasers) so that an encoded light pulse is output once per DMD frame. Since the shutters in the glasses are both off when the DLP Link pulse is sent, the projector illumination source will also be off except for the when light is sent to create the DLP Link pulse. The timing for the light pulses for DLP Link 3D operation is shown in Figure 18 and Figure 19.
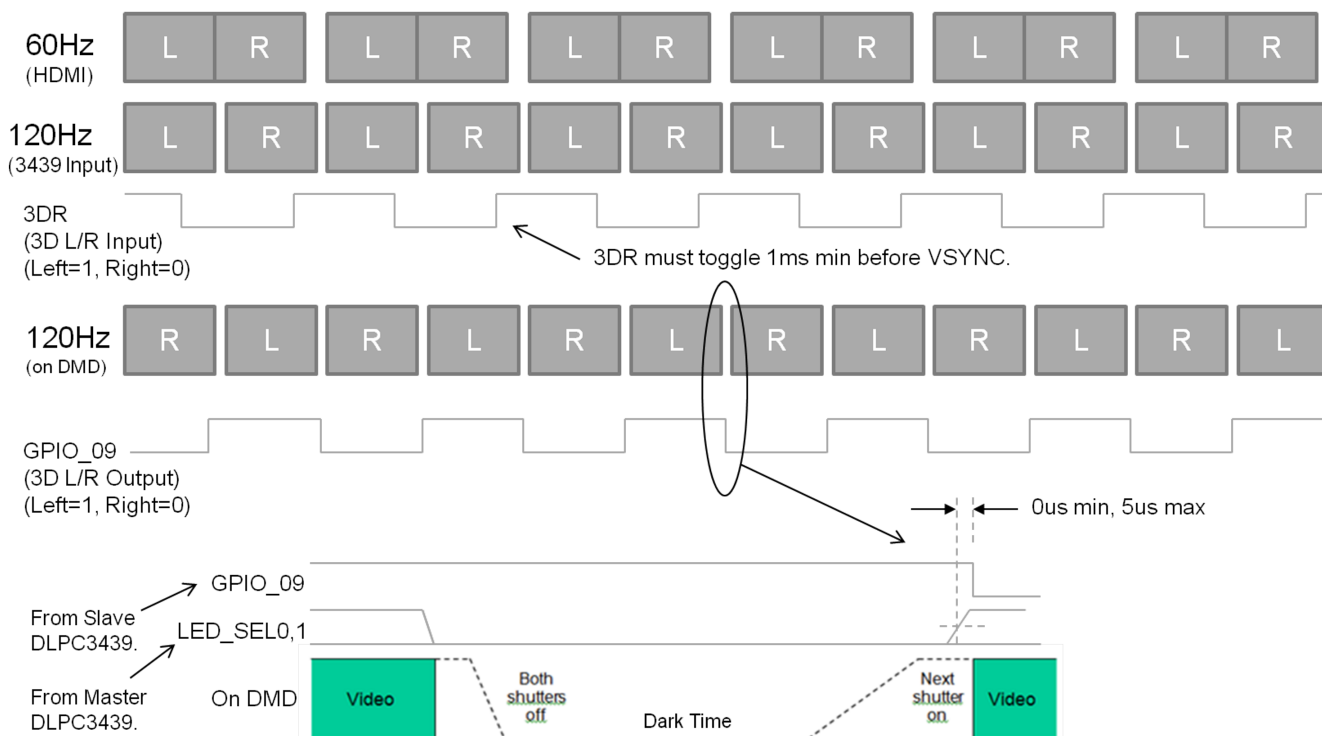


**Figure 18.  DLPC3437 L/R Timing for DLP Link**

**Figure 19. 3D DLP Link Pulse Timing**
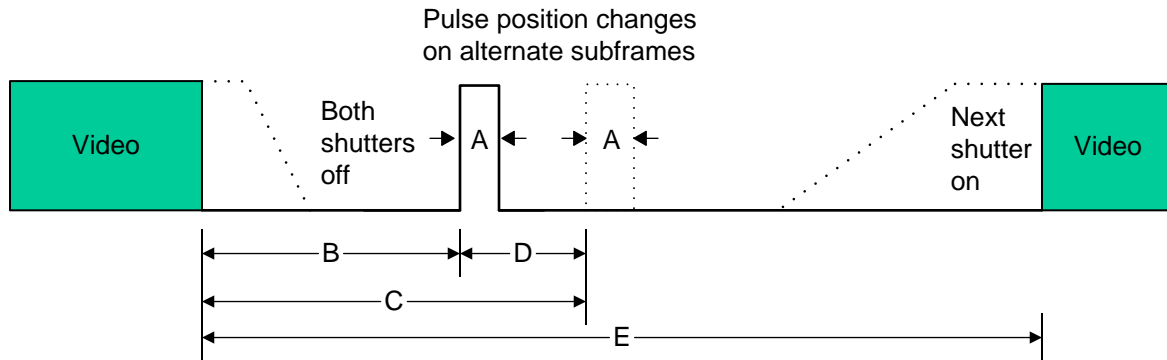
NOTE: The period between DLPLink pulses alternates between the subframe period + D and the subframe period – D, where D is the delta period.

**Table 8. 3D Link Nominal Timing Table**

| HDMI SOURCE REFERENCE (Hz) | 3D DMD SEQUENCE RATE (Hz) | A (μs) | B (μs) | C (μs) | D (μs) | E (μs) |
|---|---|---|---|---|---|---|
| 23.6 | 94.5 | 25 | 500 | 628 | 128 | > 2000 |
| 24.0 | 96 | 25 | 500 | 628 | 128 | > 2000 |
| 49.0 | 98 | 25 | 500 | 628 | 128 | > 2000 |
| 50.0 | 100 | 25 | 500 | 628 | 128 | > 2000 |
| 51.0 | 102 | 25 | 500 | 628 | 128 | > 2000 |
| 59.0 | 118 | 25 | 500 | 628 | 128 | > 2000 |
| 60.0 | 120 | 25 | 500 | 628 | 128 | > 2000 |
| 61.0 | 122 | 25 | 500 | 628 | 128 | > 2000 |

### 8.3.10 DMD (Sub-LVDS) Interface

The DLPC3437 ASIC DMD interface consists of a HS 1.8-V sub-LVDS output only interface with a maximum clock speed of 600-MHz DDR and a LS SDR (1.8-V LVCMOS) interface with a fixed clock speed of 120 MHz. Table 9 shows how the 8 sub-LVDS lanes are configured for the DLP3310 (.33 1080p) DMD.

**Table 9. DLP3310 (.33 1080p) DMD – ASIC to 8-Lane DMD Pin Mapping**

| DLPC3437 ASIC 8 LANE DMD ROUTING OPTION #1 | | |
|---|---|---|
| MASTER DLPC3437 PINS | SLAVE DLPC3437 PINS | DMD PINS |
| HS_WDATA_D_P<br>HS_WDATA_D_N | HS_WDATA_E_P<br>HS_WDATA_E_N | Input DATA_p_0<br>Input DATA_n_0 |
| HS_WDATA_C_P<br>HS_WDATA_C_N | HS_WDATA_F_P<br>HS_WDATA_F_N | Input DATA_p_1<br>Input DATA_n_1 |
| HS_WDATA_B_P<br>HS_WDATA_B_N | HS_WDATA_G_P<br>HS_WDATA_G_N | Input DATA_p_2<br>Input DATA_n_2 |
| HS_WDATA_A_P<br>HS_WDATA_A_N | HS_WDATA_H_P<br>HS_WDATA_H_N | Input DATA_p_3<br>Input DATA_n_3 |
| HS_WDATA_H_P<br>HS_WDATA_H_N | HS_WDATA_A_P<br>HS_WDATA_A_N | Input DATA_p_4<br>Input DATA_n_4 |
| HS_WDATA_G_P<br>HS_WDATA_G_N | HS_WDATA_B_P<br>HS_WDATA_B_N | Input DATA_p_5<br>Input DATA_n_5 |
| HS_WDATA_F_P<br>HS_WDATA_F_N | HS_WDATA_C_P<br>HS_WDATA_C_N | Input DATA_p_6<br>Input DATA_n_6 |
| HS_WDATA_E_P<br>HS_WDATA_E_N | HS_WDATA_D_P<br>HS_WDATA_D_N | Input DATA_p_7<br>Input DATA_n_7 |
| DLPC3437 ASIC 8 LANE DMD ROUTING OPTION #2 | | |
| MASTER DLPC3437 PINS | SLAVE DLPC3437 PINS | DMD PINS |
| HS_WDATA_E_P<br>HS_WDATA_E_N | HS_WDATA_D_P<br>HS_WDATA_D_N | Input DATA_p_0<br>Input DATA_n_0 |
| HS_WDATA_F_P<br>HS_WDATA_F_N | HS_WDATA_C_P<br>HS_WDATA_C_N | Input DATA_p_1<br>Input DATA_n_1 |
| HS_WDATA_G_P<br>HS_WDATA_G_N | HS_WDATA_B_P<br>HS_WDATA_B_N | Input DATA_p_2<br>Input DATA_n_2 |
| HS_WDATA_H_P<br>HS_WDATA_H_N | HS_WDATA_A_P<br>HS_WDATA_A_N | Input DATA_p_3<br>Input DATA_n_3 |
| HS_WDATA_A_P<br>HS_WDATA_A_N | HS_WDATA_H_P<br>HS_WDATA_H_N | Input DATA_p_4<br>Input DATA_n_4 |
| HS_WDATA_B_P<br>HS_WDATA_B_N | HS_WDATA_G_P<br>HS_WDATA_G_N | Input DATA_p_5<br>Input DATA_n_5 |
| HS_WDATA_C_P<br>HS_WDATA_C_N | HS_WDATA_F_P<br>HS_WDATA_F_N | Input DATA_p_6<br>Input DATA_n_6 |
| HS_WDATA_D_P<br>HS_WDATA_D_N | HS_WDATA_E_P<br>HS_WDATA_E_N | Input DATA_p_7<br>Input DATA_n_7 |

### 8.3.11 Calibration and Debug Support

The DLPC3437 contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pulldown resistor, thus external pullups must be used to modify the default test configuration. The default configuration (x000) corresponds to the TSTPT_(7:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pullup is recommended for TSTPT_(2:0). Pullups on TSTPT_(6:3) are used to configure the ASIC for a specific mode or option. TI does not recommend adding pullups to TSTPT_(7:3) because this has adverse affects for normal operation. This external pullup is only sampled upon a 0-to-1 transition on the RESETZ input, thus changing their configuration after reset is released will not have any effect until the next time reset is asserted and released. Table 10 defines the test mode selection for one programmable scenario defined by TSTPT(2:0).

**Table 10. Test Mode Selection Scenario Defined by TSTPT(2:0)[1]**

| TSTPT(2:0) CAPTURE VALUE | NO SWITCHING ACTIVITY x000 | CLOCK DEBUG OUTPUT x010 |
|---|---|---|
| TSTPT(0) | HI-Z | 60 MHz |
| TSTPT(1) | HI-Z | N/A |
| TSTPT(2) | HI-Z | 0.7 to 22.5 MHz |
| TSTPT(3) | HI-Z | HIGH |
| TSTPT(4) | HI-Z | LOW |
| TSTPT(5) | HI-Z | HIGH |
| TSTPT(6) | HI-Z | HIGH |
| TSTPT(7) | HI-Z | 7.5 MHz |

(1) These are only the default output selections. Software can reprogram the selection at any time.

### 8.3.12 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3437 ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

Setup Margin = (DLPC3437 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)   (1)

Hold-time Margin = (DLPC3437 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where PCB SI degradation is signal integrity degradation due to PCB affects which includes such things as Simultaneously Switching Output (SSO) noise, cross-talk and Inter-symbol Interference (ISI) noise.   (2)

DLPC3437 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that will satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.
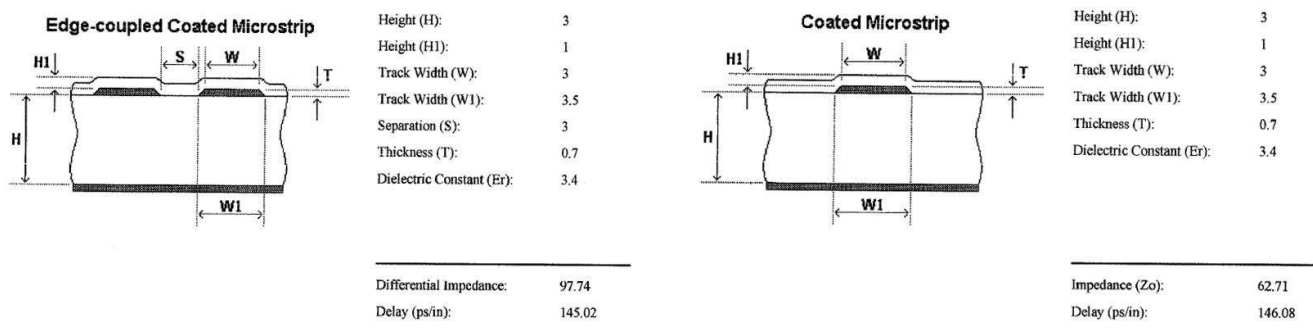


LEFT: DMD_HS Differential Signals                    RIGHT: DMD_LS Signals

**Figure 20. DMD Interface Board Stack-Up Details**

## 8.4 Device Functional Modes

DLPC3437 has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the projector automatically powers up and an image is projected from the DMD.
- When pin PROJ_ON is set low, the projector automatically powers down and only microwatts of power are consumed.

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The DLPC3437 controller is required to be coupled with DLP3310 (0.33 1080p) DMD to provide a reliable display solution for various data and video display applications. DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the chipset. Applications of interest include mobile smart TV, screenless TV, gaining displays, digital signage, wearable displays, pico projectors, interactive displays, ultra mobile displays, and smart home displays.

## 9.2 Typical Application

A common application when using a DLPC3437 controller with DLP3310 DMD and DLPA3000 PMIC/LED driver is for creating an accessory Pico projector. A functional block diagram of a typical Pico projector is shown in Figure 21.
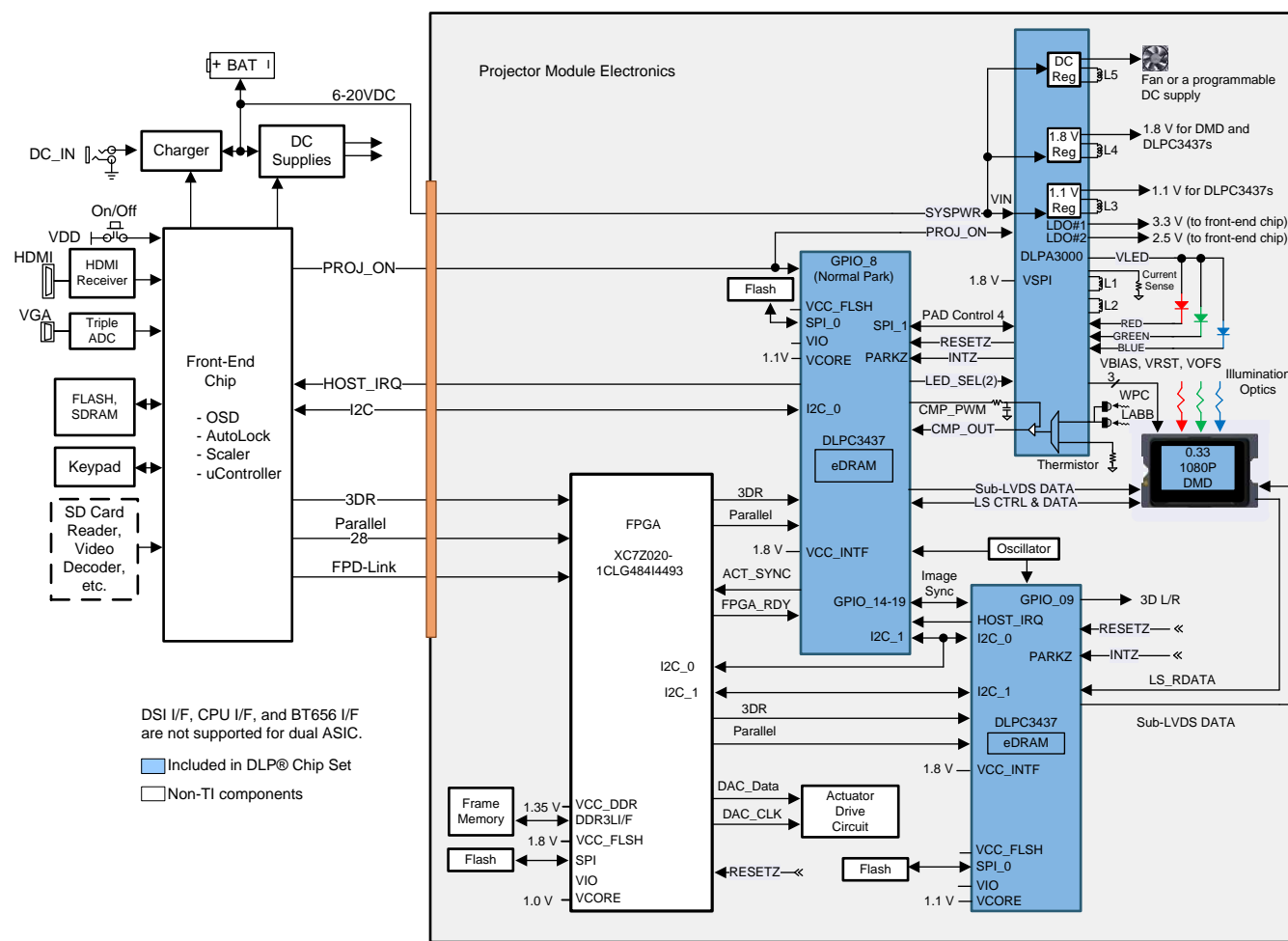


**Figure 21. Typical Application Diagram**

### 9.2.1 Design Requirements

A Pico projector is created by using a DLP chipset comprised of DLP3310 (.33 1080p) DMD, 2xDLPC3437 controller, a XC7Z020-1CLG484I4493 FPGA, and DLPA3000 PMIC/LED driver. The DLPC3437 and FPGA do the digital image processing, the DLPA3000 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image.

In addition to the four DLP chips in the chipset, other chips may be needed. At a minimum, flash memories are needed to store the software and firmware to control the two DLPC3437s and the FPGA.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8-V supply can continue to be left at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the DLPA3000 will not draw current on the 1.8-V supply.

## Typical Application  (continued)

### 9.2.2  Detailed Design Procedure

For connecting together the DLP3310 (.33 1080p) DMD, 2xDLPC3437 controller, XC7Z020-1CLG484I4493 FPGA, and DLPA3000 PMIC/LED driver, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Follow the layout guidelines to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

### 9.2.3  Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 22 when using the DLPA3000. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.
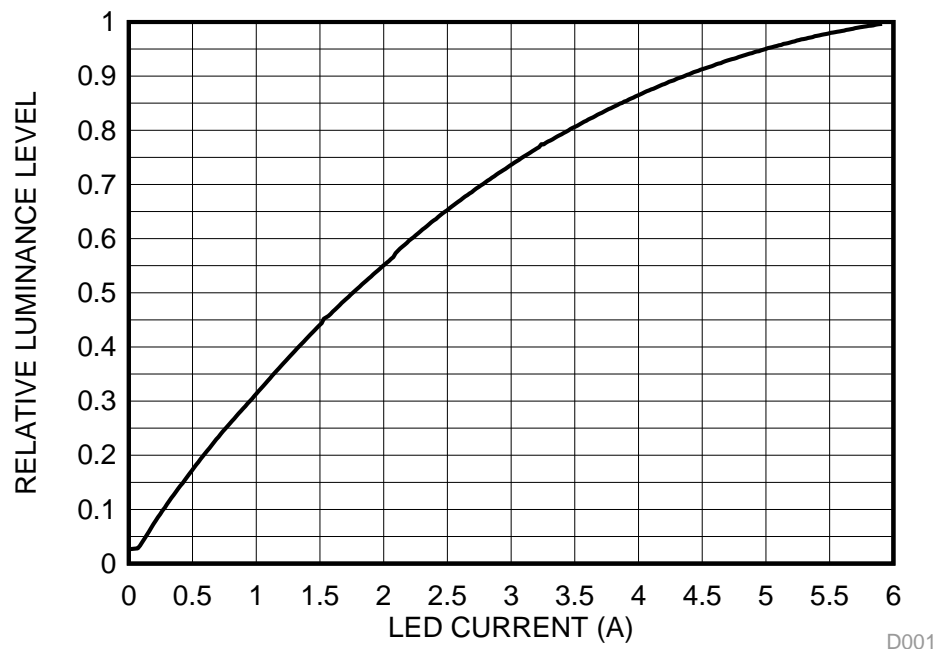


**Figure 22. Luminance vs Current**

# 10   Power Supply Recommendations

## 10.1   DLPC3437 System Design Consideration

System power regulation: It is acceptable for $V_{DD\_PLLD}$ and $V_{DD\_PLLM}$ to be derived from the same regulator as the core $V_{DD}$, but to minimize the AC noise component they should be filtered as recommended in the *PCB Layout Guidelines for Internal ASIC PLL Power*.

## 10.2   System Power-Up and Power-Down Sequence

Although the DLPC3437 requires an array of power supply voltages, (for example, $V_{DD}$, $V_{DDLP12}$, $V_{DD\_PLLM/D}$, $V_{CC18}$, $V_{CC\_FLSH}$, $V_{CC\_INTF}$), since $V_{DDLP12}$ is tied to the 1.1-V $V_{DD}$ supply, then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC3437 (This is true for both power-up and power-down scenarios). Similarly, there is no minimum time between powering-up or powering-down the different supplies if $V_{DDLP12}$ is tied to the 1.1-V $V_{DD}$ supply.

Although there is no risk of damaging the DLPC3437 if the above power sequencing rules are followed, the following additional power sequencing recommendations must be considered to ensure proper system operation.

- To ensure that DLPC3437 output signal states behave as expected, all DLPC3437 I/O supplies should remain applied while $V_{DD}$ core power is applied. If $V_{DD}$ core power is removed while the I/O supply ($V_{CC\_INTF}$) is applied, then the output signal state associated with the inactive I/O supply will go to a high impedance state.
- Additional power sequencing rules may exist for devices that share the supplies with the DLPC3437, and thus these devices may force additional system power sequencing requirements.

Note that when $V_{DD}$ core power is applied, but I/O power is not applied, additional leakage current may be drawn. This added leakage does not affect normal DLPC3437 operation or reliability.
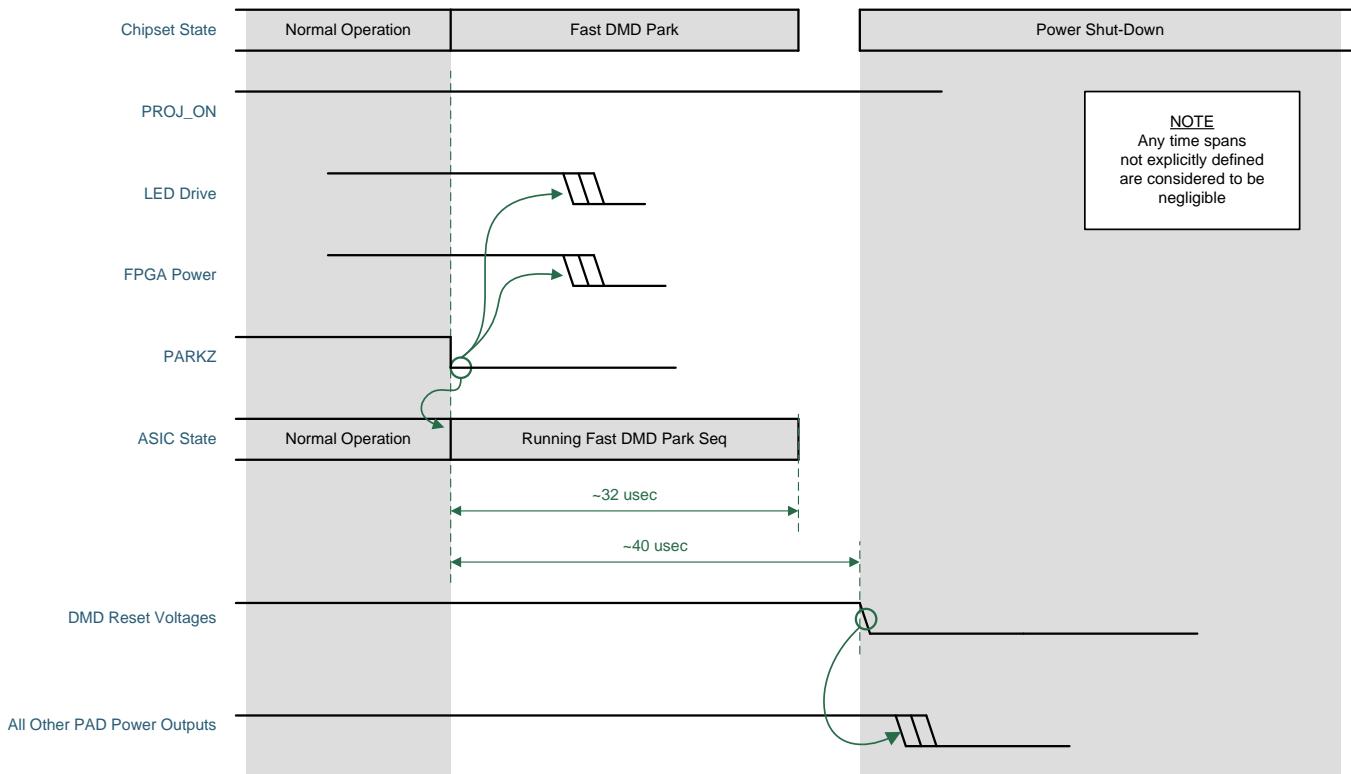
Figure 23 and Figure 24 show the DLPC3437 power-up and power-down sequence for both the normal PARK and fast PARK operations of the DLPC3437 ASIC.
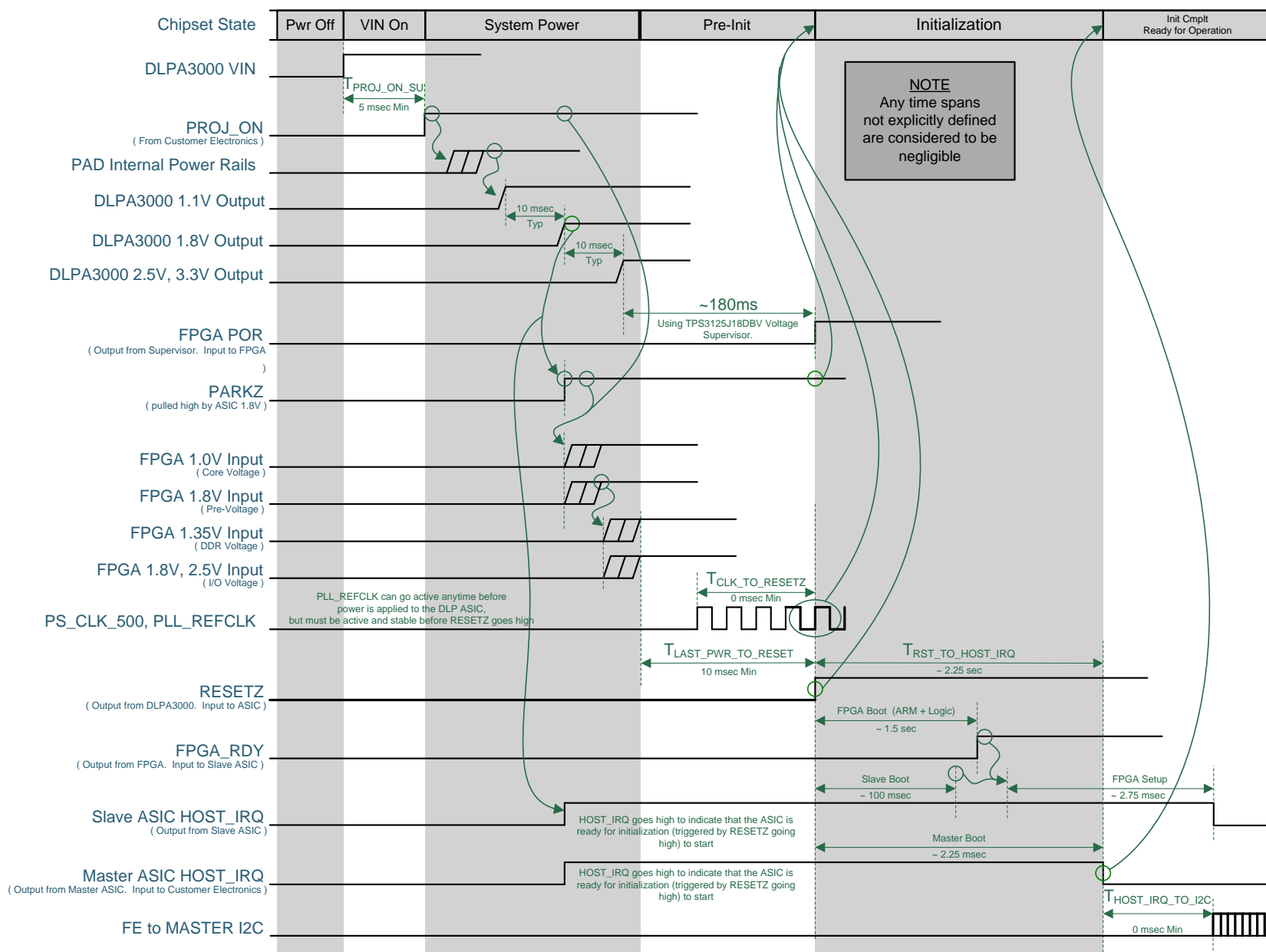
**Figure 23. DLPC3437 Power-Up Timing**
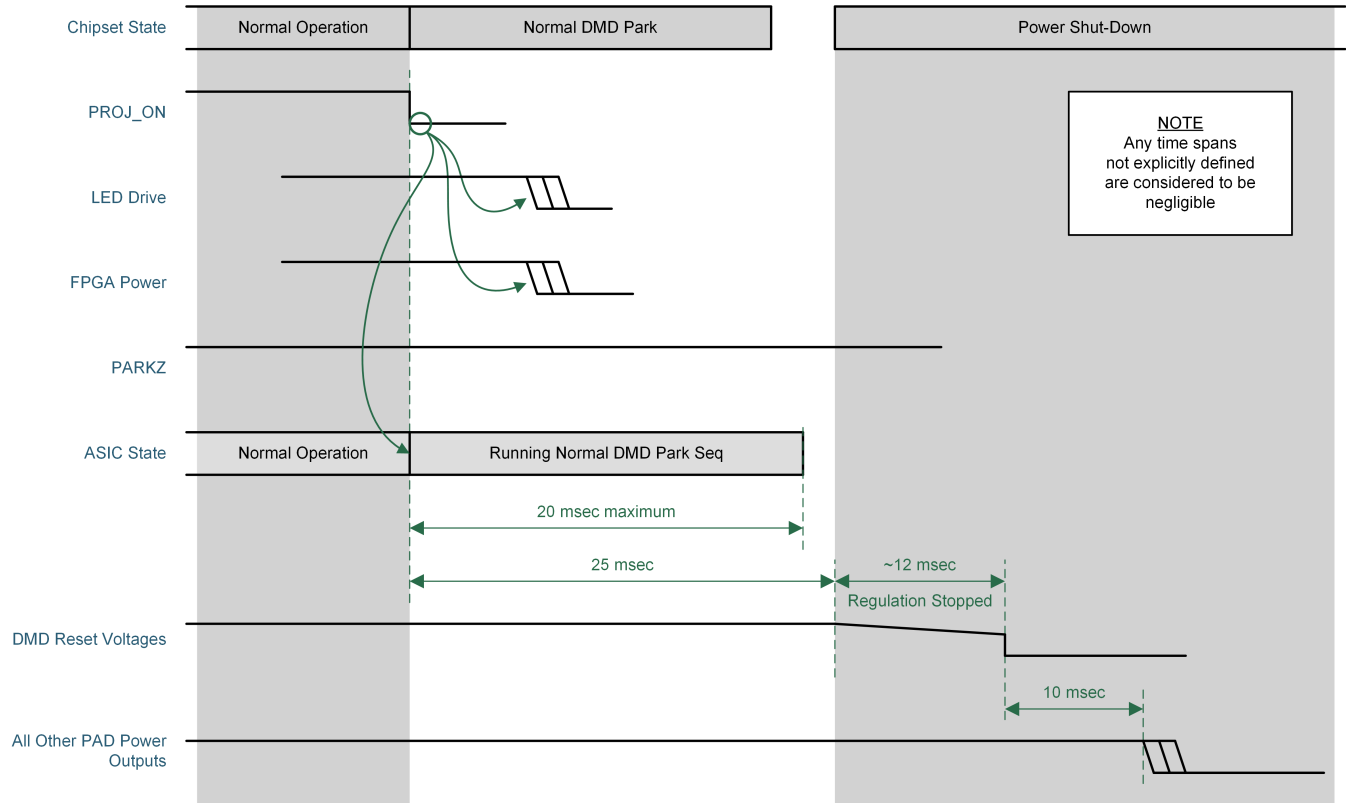
**Figure 24. DLPC3437 Normal Power-Down**



**Figure 25. DLPC3437 Fast Power-Down**

## 10.3 DLPC3437 Power-Up Initialization Sequence

It is assumed that an external power monitor will hold the DLPC3437 in system reset during power-up. It must do this by driving RESETZ to a logic low state. It should continue to assert system reset until all ASIC voltages have reached minimum specified voltage levels, PARKZ is asserted high, and input clocks are stable. During this time, most ASIC outputs will be driven to an inactive state and all bidirectional signals will be configured as inputs to avoid contention. ASIC outputs that are not driven to an inactive state are tri-stated. These include LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0 (see RESETZ pin description for full signal descriptions in *Pin Configuration and Functions*. After power is stable and the PLL_REFCLK_I clock input to the DLPC3437 is stable, then RESETZ should be deactivated (set to a logic high). The DLPC3437 then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ all DLPC3437 I/Os will become active. Immediately following the release of RESETZ, the HOST_IRQ signal will be driven high to indicate that the auto initialization routine is in progress. However, since a pullup resistor is connected to signal HOST_IRQ, this signal will have already gone high before the DLPC3437 actively drives it high. Upon completion of the chipset auto-initialization routine, the master DLPC3437 will drive HOST_IRQ low to indicate the initialization done state of the DLPC3437 has been reached.

Note that the host processor must wait for HOST_IRQ to go low before initiating I$^2$C commands.

## 10.4 DMD Fast PARK Control (PARKZ)

The PARKZ signal is defined to be an early warning signal that should alert the ASIC 40 µs before DC supply voltages have dropped below specifications in fast PARK operation. This allows the ASIC time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and RESETZ should remain deactivated for at least 40 µs after PARKZ has been deactivated (set to a logic low) to allow the park operation to complete.

## 10.5 Hot Plug Usage

The DLPC3437 provides fail-safe I/O on all host interface signals (signals powered by V$_{CC\_INTF}$). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the DLPC3437 will not load the input signal nor draw excessive current that could degrade ASIC reliability. For example, the I$^2$C bus from the host to other components would not be affected by powering off V$_{CC\_INTF}$ to the DLPC3437. TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

If the I/O supply (V$_{CC\_INTF}$) is powered off, but the core supply (V$_{DD}$) is powered on, then the corresponding input buffer may experience added leakage current, but this does not damage the DLPC3437.

## 10.6 Maximum Signal Transition Time

Unless otherwise noted, 10 ns is the maximum recommended 20% to 80% rise or fall time to avoid input buffer oscillation. This applies to all DLPC3437 input signals. However, the PARKZ input signal includes an additional small digital filter that ignores any input buffer transitions caused by a slower rise or fall time for up to 150 ns.
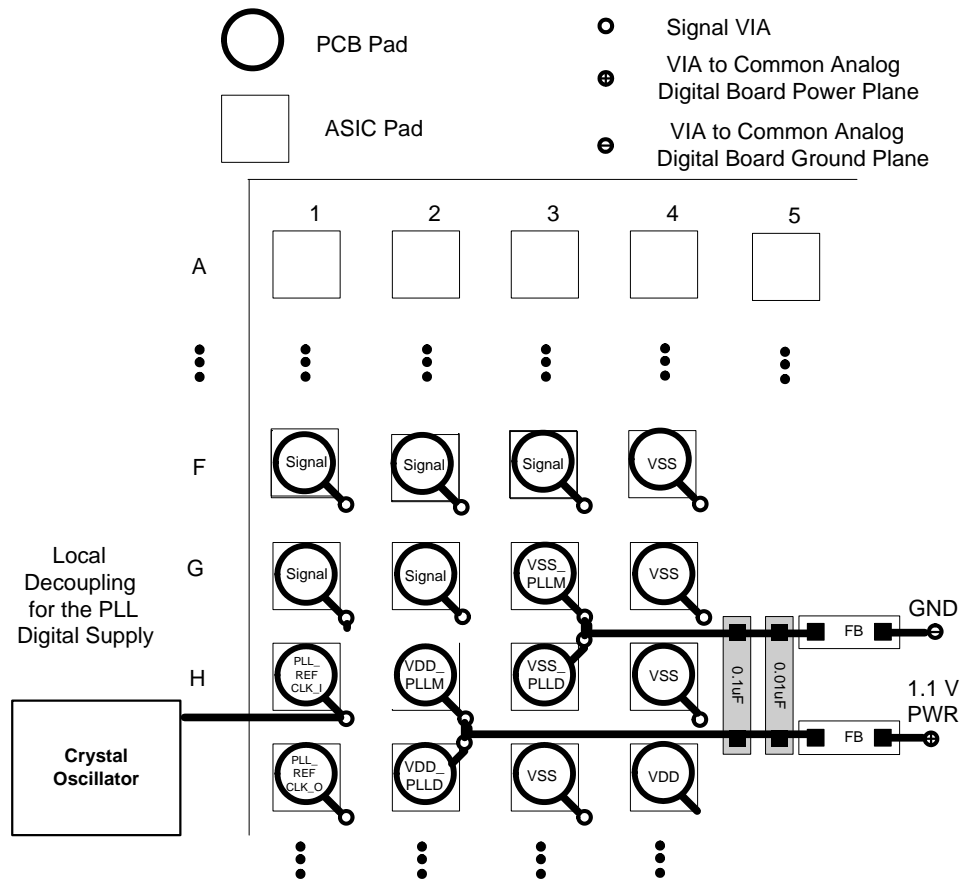
# 11 Layout

## 11.1 Layout Guidelines

### 11.1.1 PCB Layout Guidelines for Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. Each DLPC3437 contains 2 internal PLLs which have dedicated analog supplies ($V_{DD\_PLLM}$, $V_{SS\_PLLM}$, $V_{DD\_PLLD}$, $V_{SS\_PLLD}$). As a minimum, $V_{DD\_PLLx}$ power and $V_{SS\_PLLx}$ ground pins should be isolated using a simple passive filter consisting of two series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. All four components should be placed as close to the ASIC as possible but it's especially important to keep the leads of the high frequency capacitors as short as possible. Note that both capacitors should be connected across $V_{DD\_PLLM}$ and $V_{SS\_PLLM}$ / $V_{DD\_PLLD}$ and $V_{SS\_PLLD}$ respectfully on the ASIC side of the ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 $\Omega$
- Impedance at 10 MHz equal to or greater than 180 $\Omega$
- Impedance at 100 MHz equal to or greater than 600 $\Omega$

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, $V_{DD\_PLLM}$ and $V_{DD\_PLLD}$ must be a single trace from each DLPC3437 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.



**Figure 26. PLL Filter Layout**

## Layout Guidelines (continued)

### 11.1.2 DLPC3437 Reference Clock

The DLPC3437 requires an external reference clock to feed its internal PLL. A crystal oscillator can supply this reference. For flexibility, the DLPC3437 accepts either of two reference clock frequencies, but both must have a maximum frequency variation of ±200 ppm (including aging, temperature, and trim component variation).

The two DLPC3437 devices require a single dedicated oscillator where the oscillator output drives both DLPC3437 devices. The oscillator must drive the PLL_REFCLK_I pin on each DLPC3437 and the PLL_REFCLK_O pins should be left unconnected.

The external oscillator must be able to drive at least a 15-pF load. Routing length from the oscillator to each DLPC3437 should be closely matched.

### 11.1.3 General PCB Recommendations

TI recommends 1-oz. copper planes in the PCB design to achieve needed thermal connectivity.

### 11.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with an internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC3437 implements very few internal resistors and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Unused output-only pins should never be tied directly to power or ground, but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

## Layout Guidelines (continued)

### 11.1.5   Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

**Table 11. Max Pin-to-Pin PCB Interconnect Recommendations[1][2]**

| DMD BUS SIGNAL | SIGNAL INTERCONNECT TOPOLOGY | | UNIT |
| --- | --- | --- | --- |
| | SINGLE BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH | |
| DMD_HS_CLK_P DMD_HS_CLK_N | 6.0 152.4 | See [3] | inch (mm) |
| DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N | 6.0 152.4 | See [3] | inch (mm) |
| DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N | | | |
| DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N | | | |
| DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N | | | |
| DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N | | | |
| DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N | | | |
| DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N | | | |
| DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N | | | |
| DMD_LS_CLK | 6.5 165.1 | See [3] | inch (mm) |
| DMD_LS_WDATA | 6.5 165.1 | See [3] | inch (mm) |
| DMD_LS_RDATA | 6.5 165.1 | See [3] | inch (mm) |
| DMD_DEN_ARSTZ | 7.0 177.8 | See [3] | inch (mm) |

(1)   Max signal routing length includes escape routing.
(2)   Multi-board DMD routing length is more restricted due to the impact of the connector.
(3)   Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

#### Table 12. High Speed PCB Signal Routing Matching Requirements[1][2][3][4]

| SIGNAL GROUP LENGTH MATCHING | | | | |
|---|---|---|---|---|
| INTERFACE | SIGNAL GROUP | REFERENCE SIGNAL | MAX MISMATCH[5] | UNIT |
| DMD | DMD_HS_WDATA_A_P<br>DMD_HS_WDATA_A_N<br><br>DMD_HS_WDATA_B_P<br>DMD_HS_WDATA_B_N<br><br>DMD_HS_WDATA_C_P<br>DMD_HS_WDATA_C_N<br><br>DMD_HS_WDATA_D_P<br>DMD_HS_WDATA_D_N<br><br>DMD_HS_WDATA_E_P<br>DMD_HS_WDATA_E_N<br><br>DMD_HS_WDATA_F_P<br>DMD_HS_WDATA_F_N<br><br>DMD_HS_WDATA_G_P<br>DMD_HS_WDATA_G_N<br><br>DMD_HS_WDATA_H_P<br>DMD_HS_WDATA_H_N | DMD_HS_CLK_P<br>DMD_HS_CLK_N | ±1.0<br>(±25.4) | inch<br>(mm) |
| DMD | DMD_LS_WDATA<br>DMD_LS_RDATA | DMD_LS_CLK | ±0.2<br>(±5.08) | inch<br>(mm) |
| DMD | DMD_DEN_ARSTZ | N/A | N/A | inch<br>(mm) |

(1)  These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC3437, the DMD.
(2)  DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3)  Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4)  DMD LS signals are single ended.
(5)  Mismatch variance applies to high-speed data pairs. For all high-speed data pairs, the maximum mismatch between pairs should be 1 mm or less.

#### 11.1.6  Number of Layer Changes

• Single-ended signals: Minimize the number of layer changes.
• Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.

#### 11.1.7  Stubs

Stubs should be avoided.

#### 11.1.8  Terminations

• No external termination resistors are required on DMD_HS differential signals.
• The DMD_LS_CLK and DMD_LS_WDATA signal paths should include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
• The DMD_LS_RDATA signal path should include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
• DMD_DEN_ARSTZ does not require a series resistor.

#### 11.1.9  Routing Vias

• The number of vias on DMD_HS signals should be minimized and should not exceed two.
• Any and all vias on DMD_HS signals should be located as close to the ASIC as possible.
• The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be minimized and not exceed two.
• Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be located as close to the ASIC as possible.
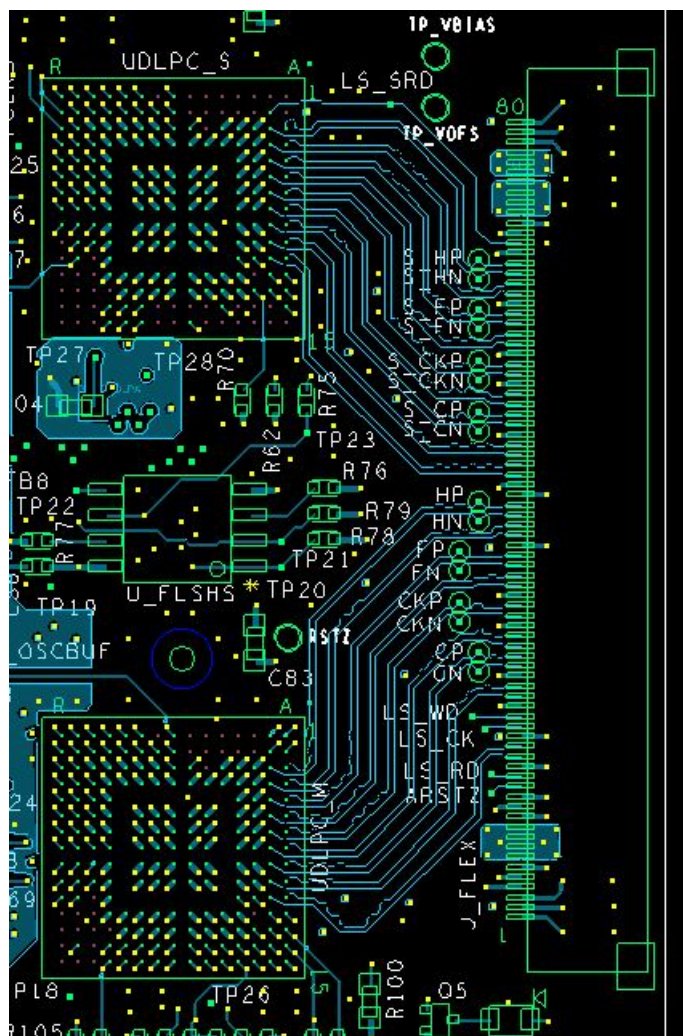
## 11.2 Layout Example



**Figure 27. Board Layout**

## 11.3 Thermal Considerations

The underlying thermal limitation for the DLPC3437 is that the maximum operating junction temperature ($T_J$) not be exceeded (this is defined in the *Recommended Operating Conditions*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC3437, and power dissipation of surrounding components. The DLPC3437's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature ($T_A$) is provided primarily as a design target and is based on maximum DLPC3437 power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a glater test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the DLPC3437 PCB; the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommended that thermal performance be measured and validated.

## Thermal Considerations (接下页)

To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validated not to exceed the maximum recommended case temperature ($T_C$). This specification is based on the measured $\varphi_{JT}$ for the DLPC3437 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

#### 12.1.2 器件命名规则

##### 12.1.2.1 器件标记
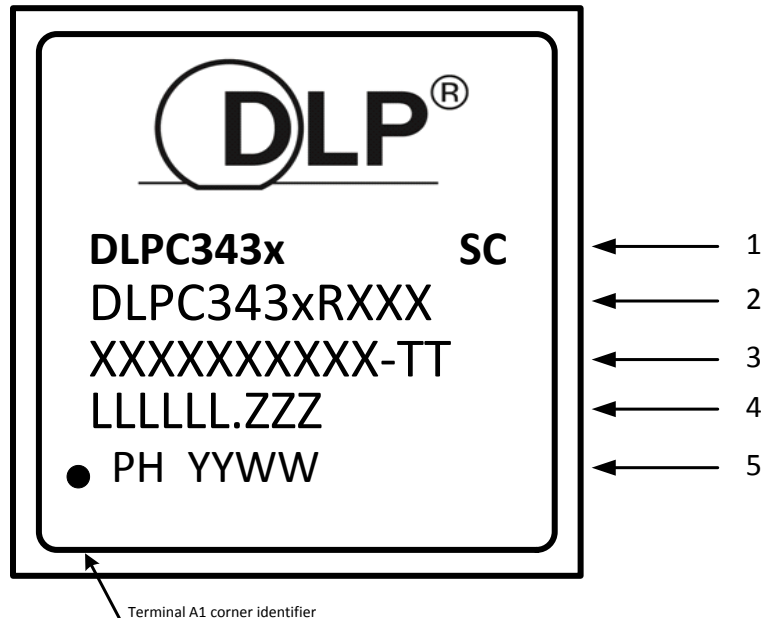


标记定义：

第 1 行：     DLP® 器件名称：DLPC343x，本器件的 **x** 是"7"。
              SC：焊锡球成分
                e1：表示含 SnAgCu 的无铅焊锡球
                G8：表示含 SnAgCu 的无铅焊锡球，其中银含量
                小于等于 1.5%，模压混合物满足德州仪器 (TI) 的绿色定义。

第 2 行：     TI 器件编号
              DLP® 器件名称：DLPC343x = 本器件的 **x** 是"7"。
              **R** 对应于 TI 器件版本字母，例如 A、B 或 C
              **XXX** 对应于器件封装标识符。

第 3 行：     XXXXXXXXXX-TT 制造商器件号

第 4 行：     LLLLLL.ZZZ 半导体晶圆的铸造批次代码
              LLLLLL：生产批次代码
              ZZZ：分批编号

第 5 行：     PH YYWW ES：封装组件信息
              PH：制造工厂
              YYWW：日期代码（YY = 年 :: WW = 周）

器件支持 **(**接下页**)**

<div align="center">注</div>

1. 工程原型样品则在 TI 部件号之后加 **X** 后缀表示。例如：2512737-0001X。

2. 请参阅Table 3，了解 DLPC3437 在每个 DMD 支持的器件型号上的分辨率。

### 12.1.3  视频时序参数定义

每帧有效扫描行数 **(ALPF)** 定义一帧中包含可显示数据的行数：ALPF 是每帧总行数 (TLPF) 的子集。

每行有效像素 **(APPL)** 定义包含可显示数据的一行中的像素时钟数：APPL 是每行总像素 (TPPL) 的子集。

水平后沿 **(HBP)** 消隐 水平同步之后，第一个有效像素之前的消隐像素时钟数量。注意：HBP 时间参考各自同步信号的前缘（有效）边沿。

水平前沿 **(HFP)** 消隐 最后一个有效时钟之后，水平同步之前的消隐像素时钟的数量。

水平同步 **(HS)** 定义水平间隔（行）开始的时序基准点。绝对基准点由 HS 信号的有效边沿定义。有效边沿（源定义的上升沿或下降沿）是测量所有水平消隐参数的基准。

每帧总行数 **(TLPF)** 以行数定义垂直扫描时间（帧时间）：TLPF = 每帧总行数（有效和无效行）。

每行总像素 **(TPPL)** 以像素时钟数定义水平行扫描时间：TPPL = 每行总像素时钟数（有效和无效像素时钟）。

垂直同步 **(VS)** 定义垂直间隔（帧）开始的时序基准点。这个绝对基准点由 VS 信号的有效边沿定义。有效边沿（源定义的上升沿或下降沿）是测量所有垂直消隐参数的基准。

垂直后沿 **(VBP)** 消隐 垂直同步的前沿之后，第一个有效行之前的消隐行的数量。

垂直前沿 **(VFP)** 消隐 最后一个有效行之后，垂直同步的前沿之前的消隐行的数量。
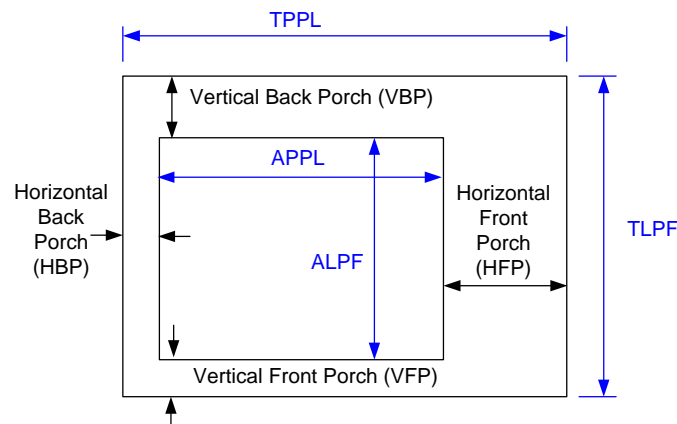


<div align="center">图 28. 时序参数图</div>

## 12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **13.** 相关链接

| 器件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持和社区 |
|---|---|---|---|---|---|
| DLPC3437 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| DLP3310 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| DLPA3000 | 单击此处 | 单击此处 | 单击此处 | 单击此处 | 单击此处 |

## 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 商标

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## 12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## 13.1 Package Option Addendum

### 13.1.1 Packaging Information

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] | Op Temp (°C) | Device Marking[4][5] |
|---|---|---|---|---|---|---|---|---|---|---|
| DLPC3437CZEZ | ACTIVE | NFBGA | ZEZ | 201 | 160 | TBD | Call TI | Level-3-260C-168 HRS | –30 to 85°C | |

(1) The marketing status values are defined as follows:
   **ACTIVE:** Product device recommended for new designs.
   **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   **PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
   **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
   **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
   **TBD:** The Pb-Free/Green conversion plan has not been defined.
   **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
   **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and the leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
   **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## 重要声明和免责声明

A
13.1
12.9
B

BALL A1 CORNER

13.1
12.9

1 MAX

C

SEATING PLANE

0.31
0.21 TYP

BALL TYP

⬙ 0.1 C

11.2 TYP

SYMM
₵

(0.9) TYP

R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

SYMM
₵

(0.9) TYP

11.2
TYP

201X ⌀ 0.4
0.3

⌖ ⌀ 0.15 Ⓜ C AⓈ BⓈ
⌀ 0.08 Ⓜ C

0.8 TYP

1  2  3  4  5  6  7  8  9  10 11 12 13 14 15

BALL A1 CORNER

0.8 TYP

4221521/A  03/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## ZEZ0201A

201X (⌀0.4)

(0.8) TYP

(0.8) TYP

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

A B C D E F G H J K L M N P R

SYMM ₵

SYMM ₵

**LAND PATTERN EXAMPLE**
SCALE:8X

0.05 MAX

(⌀0.4)
METAL

SOLDER MASK
OPENING

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL UNDER
SOLDER MASK

(⌀0.4)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**
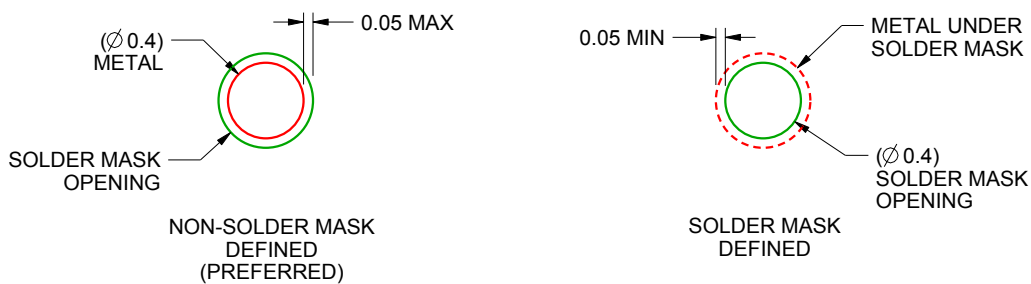
**SOLDER MASK DETAILS**
NOT TO SCALE

4221521/A   03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

## ZEZ0201A

### NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X
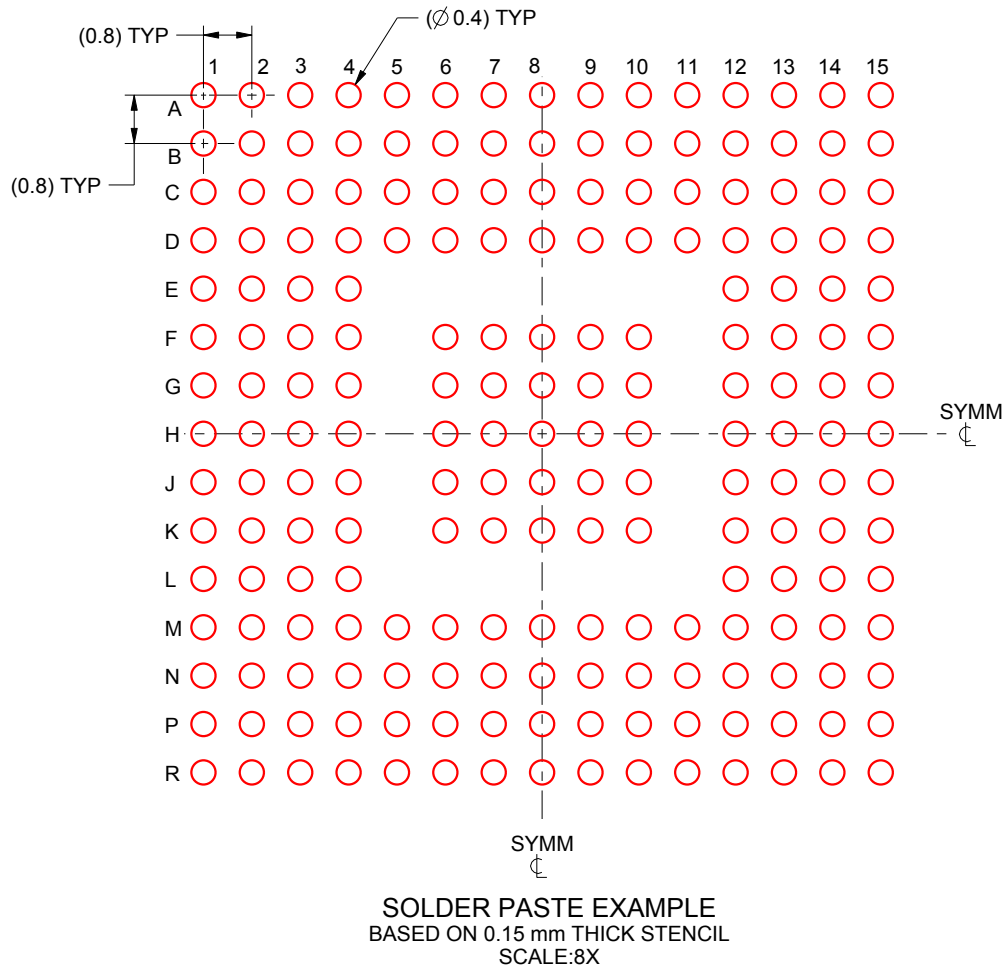
4221521/A   03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## 重要声明和免责声明