ADS8860 16 位、1MSPS、串行接口、微功耗、微型、单端输入、SAR 模数转换器

1 特性

- 采样率：1MHz
- 无延迟输出
- 单极单端输入电压范围：0V 至 $+V_{REF}$
- SPI™- 兼容串行接口，此接口具有菊链式选项
- 出色的交流和直流性能：
  - SNR：93dB，THD：–108dB
  - INL：±1.0LSB（典型值），±2.0 LSB（最大值）
  - DNL：±1.0LSB（最大值）、16 位 NMC
- 宽工作电压范围：
  - AVDD：2.7V 至 3.6V
  - DVDD：1.65V 至 3.6V（不受 AVDD 影响）
  - REF：2.5V 至 5V（不受 AVDD 影响）
  - 工作温度：-40°C 至 +85°C
- 低功率耗散：
  - 1MSPS 时为 5.5mW
  - 100kSPS 时为 0.55mW
  - 10kSPS 时为 55µW
- 关断电流 (AVDD)：50nA
- 满标度步进趋稳至 16 位：290ns
- 封装：VSSOP-10 和 VSON-10

2 应用

- 自动测试设备 (ATE)
- 仪器和流程控制
- 精密医疗设备
- 低功耗电池供电的仪器

3 说明

ADS8860 是一款 16 位、1MSPS 单端输入模数转换器 (ADC)。此器件以 2.5V 至 5V 的外部基准运行，从而在无需额外的信号调节情况下提供宽信号范围。此基准电压设置独立于，并且可超过，模拟电源电压 (AVDD)。

该器件提供一个兼容的 SPI 串口。该串口也支持菊花链操作以实现多个器件级联。一个可选的繁忙指示器位可轻松实现与数字主机的同步。

此器件支持 -0.1V 至 V_{REF} + 0.1V 范围的单极单端模拟输入。

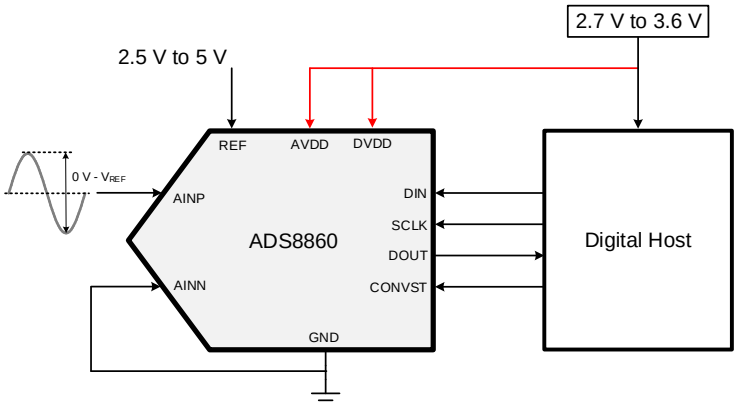
器件运行针对极低功耗运行进行了优化。功耗直接与速度成比例。此特性使得 ADS8860 非常适合较低速度的应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS8860	VSSOP (10)	3.00mm × 3.00mm
	VSON (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

ADC 电源无需独立的 LDO



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2013) to Revision B **Page**

- 已添加 添加了*器件信息* 表、*ESD 额定值* 表、*建议运行条件* 表、*参数测量信息* 部分、*特性* *说明*部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 已更改 通篇将模拟输入从*伪差分*更改为*单端* ... 1
- 已更改 在*特性* 部分中将 DVDD 值从 2.7V 至 3.6V 更改为 1.65V 至 3.6V ... 1
- 已更改 通篇将 MSOP 更改为 VSSOP ... 1
- Changed title of *Device Comparison Table* from *Family Information* ... 4
- Changed footnotes of *Family Information* table ... 4
- Changed LSB footnote in *Electrical Characteristics* table to include how to convert LSB to ppm ... 6
- Added more information about validity of data on SCLK edges in all interface modes ... 22
- Changed diagrams and text for better explanation of the daisy-chain feature in the *Daisy-Chain Mode* section ... 27
- Changed Equation 1 and Equation 2 ... 31
- Changed *Charge-Kickback Filter* section title and functionality description ... 32

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- 已更改 更改了*交流和直流性能* 特性 项目中的子项目 ... 1
- 已更改 *更改了满标度步进趋稳* 特性 项目 ... 1
- 已删除 删除了最后两个 应用 项目 ... 1
- 已更改 *说明* 部分 ... 1
- 已更改 首页图 ... 1
- Added *Family Information*, *Absolute Maximum Ratings*, and *Thermal Information* tables ... 4
- Added *Pin Configurations* section ... 4
- Added *Electrical Characteristics* table ... 6
- Added *Timing Characteristics* section ... 8

- Added *Typical Characteristics* section 11

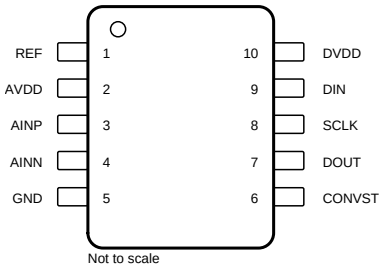
5 Device Comparison Table

THROUGHPUT	18-BIT, TRUE-DIFFERENTIAL	16-BIT, SINGLE-ENDED	16-BIT, TRUE-DIFFERENTIAL
100 kSPS	ADS8887	ADS8866	ADS8867
250 kSPS	—	ADS8339(1)	—
400 kSPS	ADS8885	ADS8864	ADS8865
500 kSPS	—	ADS8319(1)	ADS8318(1)(2)
680 kSPS	ADS8883	ADS8862	ADS8863
1 MSPS	ADS8881	ADS8860	ADS8861

(1) Pin-to-pin compatible device with AVDD = 5 V.
(2) Supports standard for fully-differential input.

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



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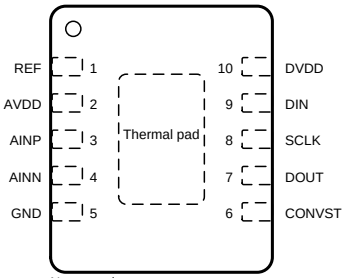
DRC Package
10-Pin VSON
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AINN	4	Analog input	Inverting analog signal input
AINP	3	Analog input	Noninverting analog signal input
AVDD	2	Analog	Analog power supply. This pin must be decoupled to GND with a 1-µF capacitor.
CONVST	6	Digital input	Convert input. This pin also functions as the $\overline{CS}$ input in 3-wire interface mode; see the *Description* and *Timing Requirements* sections for more details.
DIN	9	Digital input	Serial data input. The DIN level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). This pin also serves as the $\overline{CS}$ input in 4-wire interface mode; see the *Description* and *Timing Requirements* sections for more details.
DOUT	7	Digital output	Serial data output
DVDD	10	Power supply	Digital interface power supply. This pin must be decoupled to GND with a 1-µF capacitor.
GND	5	Analog, digital	Device ground. Note that this pin is a common ground pin for both the analog power supply (AVDD) and digital I/O supply (DVDD). The reference return line is also internally connected to this pin.
REF	1	Analog	Positive reference input. This pin must be decoupled with a 10-µF or larger capacitor.
SCLK	8	Digital input	Clock input for serial interface. Data output (on DOUT) are synchronized with this clock.
Thermal pad		—	Exposed thermal pad **(only for the DRC package option)**. Texas Instruments recommends connecting the thermal pad to the printed circuit board (PCB) ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AINP to GND or AINN to GND	–0.3	REF + 0.3	V
AVDD to GND or DVDD to GND	–0.3	4	V
REF to GND	–0.3	5.7	V
Digital input voltage to GND	–0.3	DVDD + 0.3	V
Digital output to GND	–0.3	DVDD + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Operating temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply		3		V
DVDD	Digital power supply		3		V
V_{REF}	Reference voltage		5		V

7.4 Thermal Information

THERMAL METRIC(1)		ADS8860		UNIT
		DGS (VSSOP)	DRC (VSON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.9	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	45.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.9	45.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

all minimum and maximum specifications are at AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS over the operating free-air temperature range (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 3 V, and DVDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span(1)	AINP – AINN	0		V_{REF}	V
	Operating input range(1)	AINP	–0.1		V_{REF} + 0.1	V
		AINN	–0.1		+ 0.1	
C_I	Input capacitance	AINP and AINN terminal to GND		59		pF
	Input leakage current	During acquisition for dc input		5		nA
EXTERNAL REFERENCE INPUT						
V_{REF}	Input range		2.5		5	V
	Reference input current	During conversion, 1-MHz sample rate, mid-code		300		µA
	Reference leakage current			250		nA
C_{REF}	Decoupling capacitor at the REF input		10	22		µF
SYSTEM PERFORMANCE						
	Resolution			16		Bits
NMC	No missing codes		16			Bits
DNL	Differential linearity		–0.99	±0.6	1	LSB(2)
INL	Integral linearity(3)		–2	±0.8	2	LSB(2)
E_O	Offset error(4)		–4	±1	4	mV
	Offset error drift with temperature			±1.5		µV/°C
E_G	Gain error		–0.01	±0.005	0.01	%FSR
	Gain error drift with temperature			±0.15		ppm/°C
CMRR	Common-mode rejection ratio	With common-mode input signal = 5 V_{PP} at dc	90	100		dB
PSRR	Power-supply rejection ratio	At mid-code		80		dB
	Transition noise			0.5		LSB
SAMPLING DYNAMICS						
t_{conv}	Conversion time		500		710	ns
t_{ACQ}	Acquisition time		290			ns
	Maximum throughput rate with or without latency				1000	kHz
	Aperture delay			4		ns
	Aperture jitter, RMS			5		ps
	Step response	Settling to 16-bit accuracy		290		ns
	Overvoltage recovery	Settling to 16-bit accuracy		290		ns

(1) Ideal input span, does not include gain or offset error.
(2) LSB = least significant bit. 1 LSB at 16-bits is approximately 15.26 ppm.
(3) This parameter is the endpoint INL, not best-fit.
(4) Measured relative to actual measured reference.

Electrical Characteristics (continued)

all minimum and maximum specifications are at AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS over the operating free-air temperature range (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 3 V, and DVDD = 3 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
SINAD	Signal-to-noise + distortion(5)		At 1 kHz, V_{REF} = 5 V	90.5	92.9		dB
			At 10 kHz, V_{REF} = 5 V		92.9		
			At 100 kHz, V_{REF} = 5 V		88.2		
SNR	Signal-to-noise ratio(5)		At 1 kHz, V_{REF} = 5 V	92	93		dB
			At 10 kHz, V_{REF} = 5 V		93		
			At 100 kHz, V_{REF} = 5 V		88.5		
THD	Total harmonic distortion(5)(6)		At 1 kHz, V_{REF} = 5 V		–108		dB
			At 10 kHz, V_{REF} = 5 V		–108		
			At , V_{REF} = 5 V		–101		
SFDR	Spurious-free dynamic range(5)		At 1 kHz, V_{REF} = 5 V		108		dB
			At 10 kHz, V_{REF} = 5 V		108		
			At 100 kHz, V_{REF} = 5 V		101		
$BW_{–3dB}$	–3-dB small-signal bandwidth				30		MHz
POWER-SUPPLY REQUIREMENTS							
	Power-supply voltage	AVDD	Analog supply	2.7	3	3.6	V
		DVDD	Digital supply range for SCLK > 40 MHz	2.7	3	3.6	
			Digital supply range for SCLK < 40 MHz	1.65	1.8	3.6	
	Supply current	AVDD	1-MHz sample rate, AVDD = 3 V		1.8	2.4	mA
P_{VA}	Power dissipation		1-MHz sample rate, AVDD = 3 V		5.5	7.2	mW
			100-kHz sample rate, AVDD = 3 V		0.55		
			10-kHz sample rate, AVDD = 3 V		55		µW
IA_{PD}	Device power-down current(7)				50		nA
DIGITAL INPUTS: LOGIC FAMILY (CMOS)							
V_{IH}	High-level input voltage		1.65 V < DVDD < 2.3 V	0.8 × DVDD		DVDD + 0.3	V
			2.3 V < DVDD < 3.6 V	0.7 × DVDD		DVDD + 0.3	
V_{IL}	Low-level input voltage		1.65 V < DVDD < 2.3 V	–0.3		0.2 × DVDD	V
			2.3 V < DVDD < 3.6 V	–0.3		0.3 × DVDD	
I_{LK}	Digital input leakage current				±10	±100	nA
DIGITAL OUTPUTS: LOGIC FAMILY (CMOS)							
V_{OH}	High-level output voltage		I_O = 500-µA source, C_{LOAD} = 20 pF	0.8 × DVDD		DVDD	V
V_{OL}	Low-level output voltage		I_O = 500-µA sink, C_{LOAD} = 20 pF	0		0.2 × DVDD	V
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		85	°C

(5) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(6) Calculated on the first nine harmonics of the input frequency.
(7) The device automatically enters a power-down state at the end of every conversion, and remains in power-down during the acquisition phase.

7.6 Timing Requirements: 3-Wire Operation

all specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns
$1/f_{sample}$	Time between conversions	1000			ns
t_{wh-CNV}	Pulse duration: CONVST high	10			ns
f_{SCLK}	SCLK frequency			66.6	MHz
t_{SCLK}	SCLK period	15			ns
t_{clkl}	SCLK low time	0.45		0.55	t_{SCLK}
t_{clkh}	SCLK high time	0.45		0.55	t_{SCLK}
$t_{h-CK-DO}$	SCLK falling edge to current data invalid	3			ns
$t_{d-CK-DO}$	SCLK falling edge to next data valid delay			13.4	ns
$t_{d-CNV-DO}$	Enable time: CONVST low to MSB valid			12.3	ns
$t_{d-CNV-DOhz}$	Disable time: CONVST high or last SCLK falling edge to DOUT 3-state ($\overline{CS}$ mode)			13.2	ns
t_{quiet}	Quiet time	20			ns

7.7 Timing Requirements: 4-Wire Operation

all specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns
$1/f_{sample}$	Time between conversions	1000			ns
t_{wh-DI}	Pulse duration: DIN high	10			ns
t_{wl-CNV}	Pulse width: CONVST low	20			ns
$t_{d-DI-DO}$	Delay time: DIN low to MSB valid			12.3	ns
$t_{d-DI-DOhz}$	Delay time: DIN high or last SCLK falling edge to DOUT 3-state			13.2	ns
$t_{su-DI-CNV}$	Setup time: DIN high to CONVST rising edge	7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN high from CONVST rising edge (see Figure 61)	0			ns

7.8 Timing Requirements: Daisy-Chain

all specifications are at AVDD = 3 V, DVDD = 3 V, and over the operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns
$1/f_{sample}$	Time between conversions	1000			ns
$t_{su-CK-CNV}$	Setup time: SCLK valid to CONVST rising edge	5			ns
$t_{h-CK-CNV}$	Hold time: SCLK valid from CONVST rising edge	5			ns
$t_{su-DI-CNV}$	Setup time: DIN low to CONVST rising edge (see Figure 2)	7.5			ns
$t_{h-DI-CNV}$	Hold time: DIN low from CONVST rising edge (see Figure 61)	0			ns
$t_{su-DI-CK}$	Setup time: DIN valid to SCLK falling edge	1.5			ns

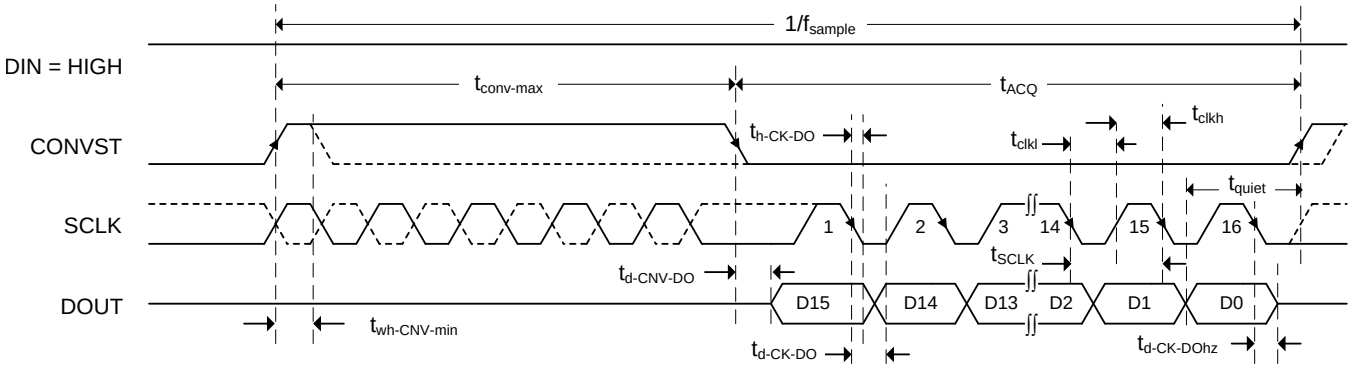

Figure 1. 3-Wire Operation: CONVST Functions as Chip Select

NOTE: Figure 1 shows the timing diagram for the *3-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in *Timing Requirements: 3-Wire Operation* table are also applicable for the *3-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

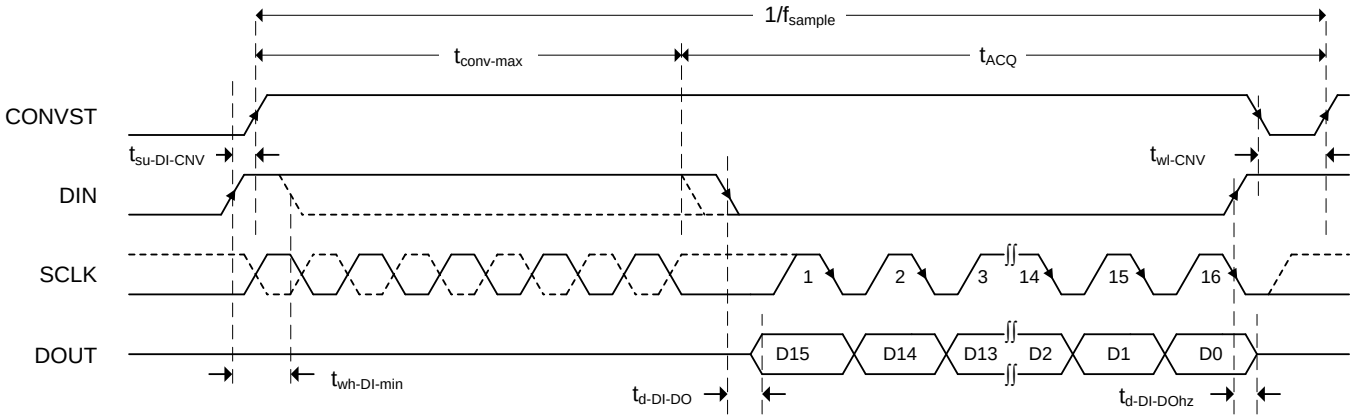

Figure 2. 4-Wire Operation: DIN Functions as Chip Select

NOTE: Figure 2 shows the timing diagram for the *4-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in *Timing Requirements: 4-Wire Operation* table are also applicable for the *4-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

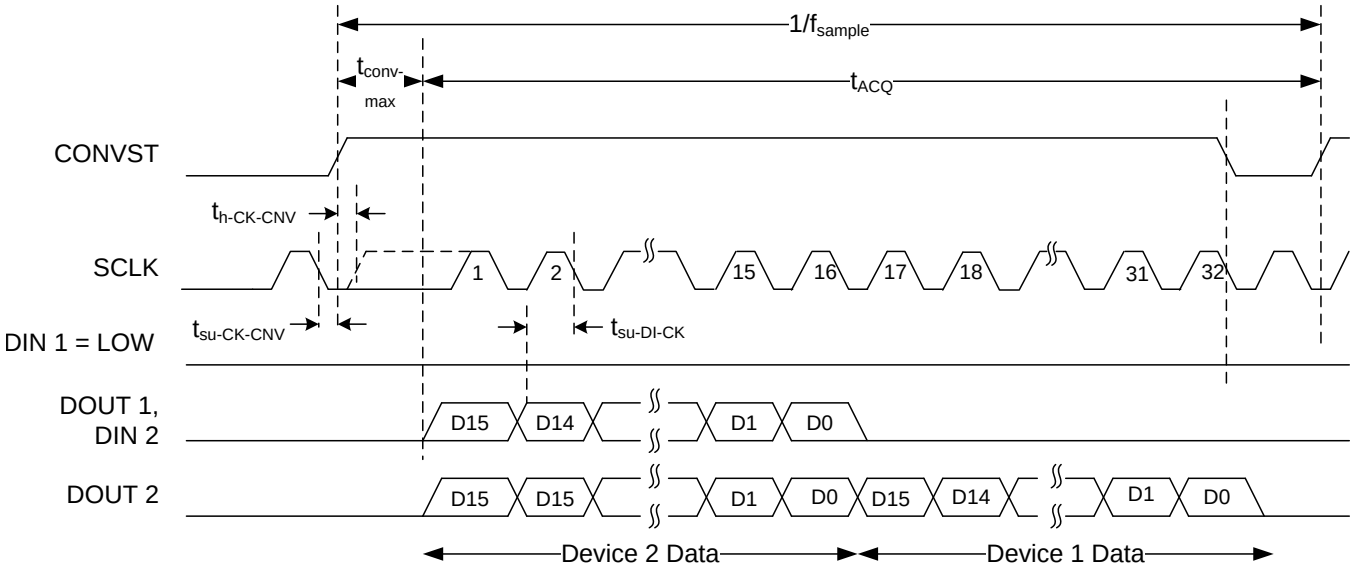

Figure 3. Daisy-Chain Operation: Two Devices

NOTE: Figure 3 shows the timing diagram for the *Daisy-Chain Mode Without a Busy Indicator* interface option. However, the timing parameters specified in *Timing Requirements: Daisy-Chain* table are also applicable for the *Daisy-Chain Mode With a Busy Indicator* interface option, unless otherwise specified; see the *Device Functional Modes* section for specific details for each interface option.

7.9 Typical Characteristics

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

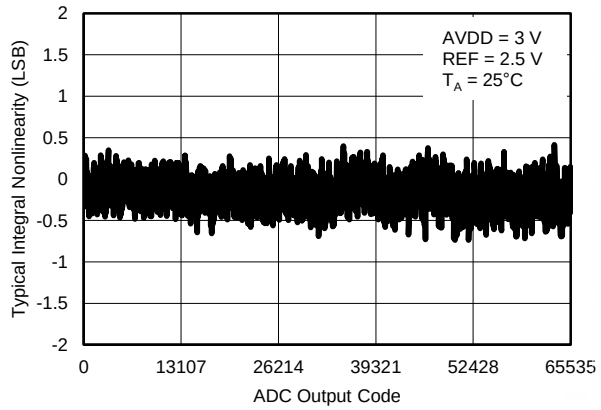

Figure 4. Typical INL (V_{REF} = 2.5 V)

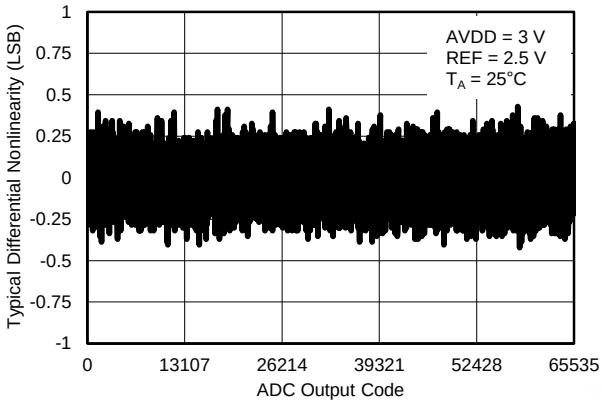

Figure 5. Typical DNL (V_{REF} = 2.5 V)

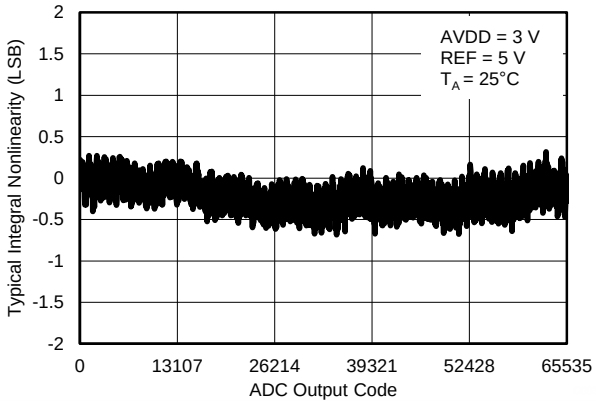

Figure 6. Typical INL (V_{REF} = 5 V)

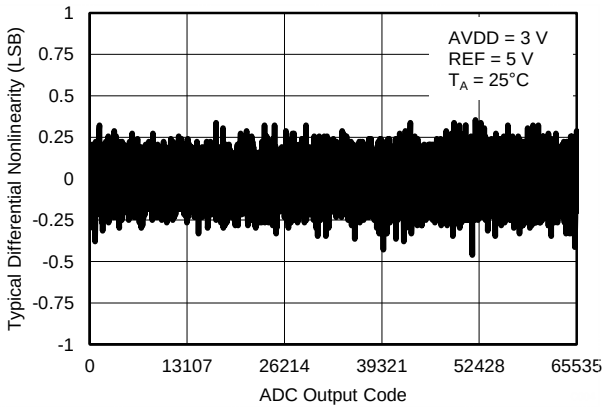

Figure 7. Typical DNL (V_{REF} = 5 V)

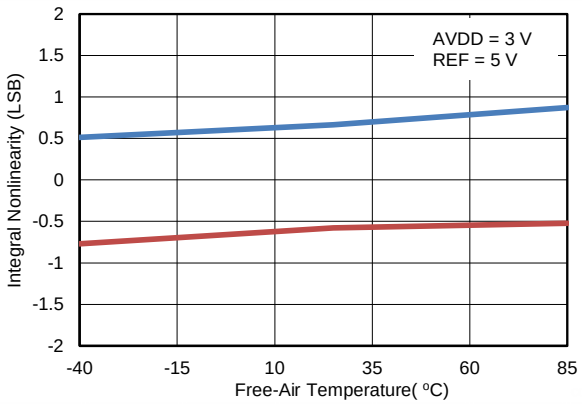

Figure 8. INL vs Temperature

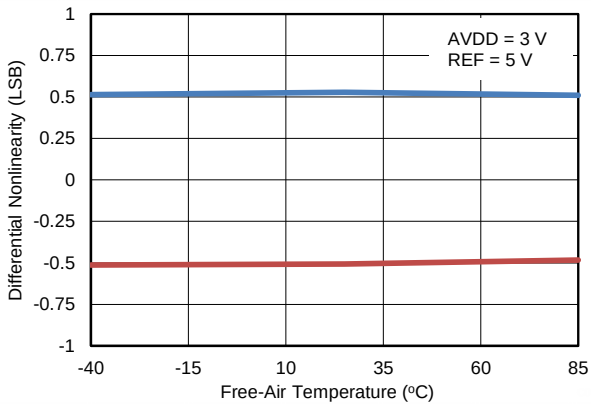

Figure 9. DNL vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

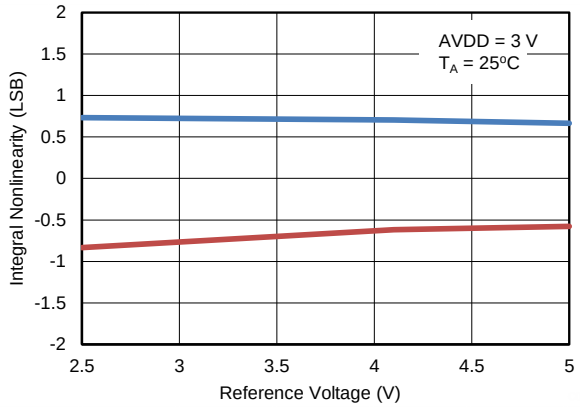

Figure 10. INL vs Reference Voltage

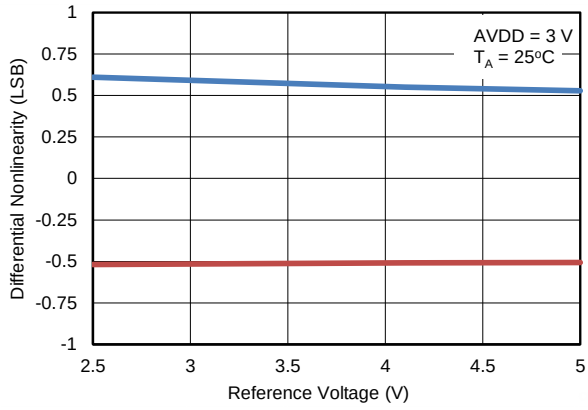

Figure 11. DNL vs Reference Voltage

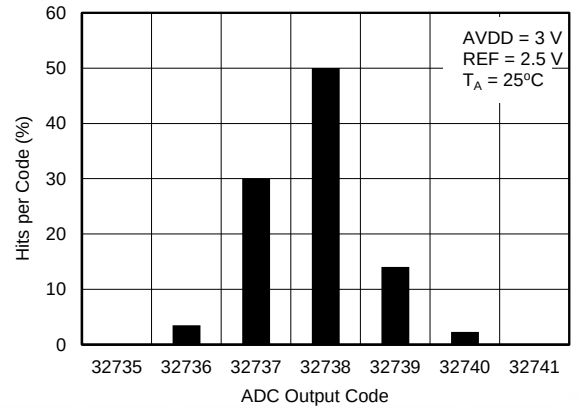

Figure 12. DC Input Histogram (V_{REF} = 2.5 V)

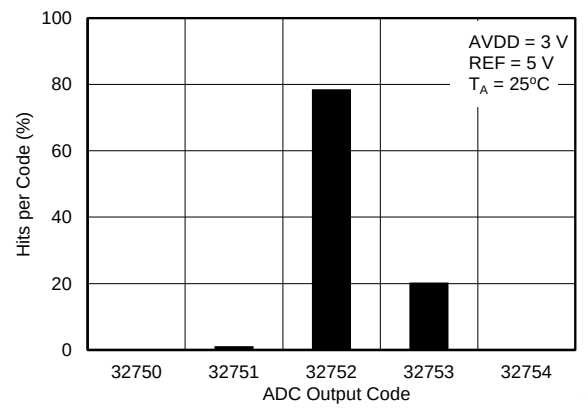

Figure 13. DC Input Histogram (V_{REF} = 5 V)

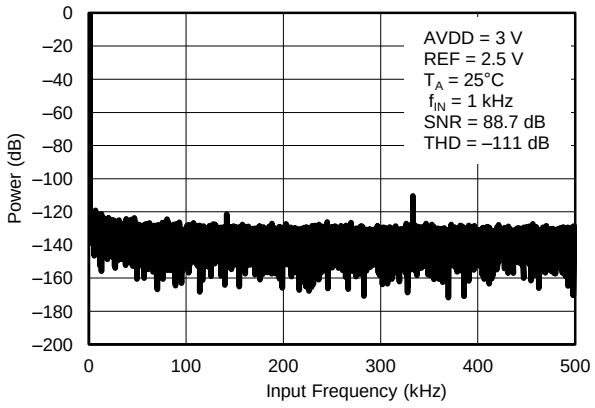

Figure 14. Typical FFT (V_{REF} = 2.5 V)

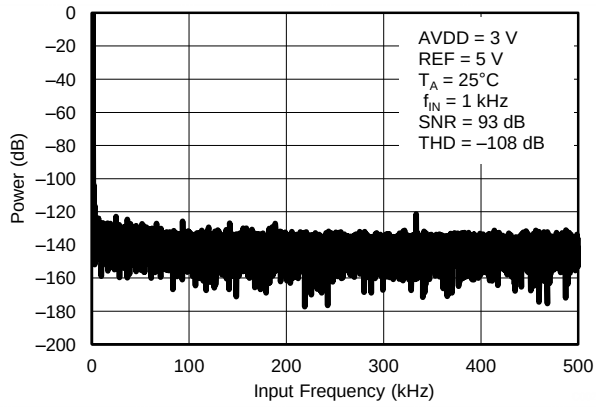

Figure 15. Typical FFT (V_{REF} = 5 V)

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

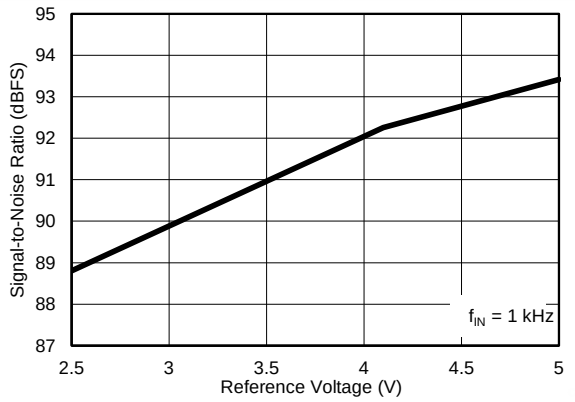

Figure 16. SNR vs Reference Voltage

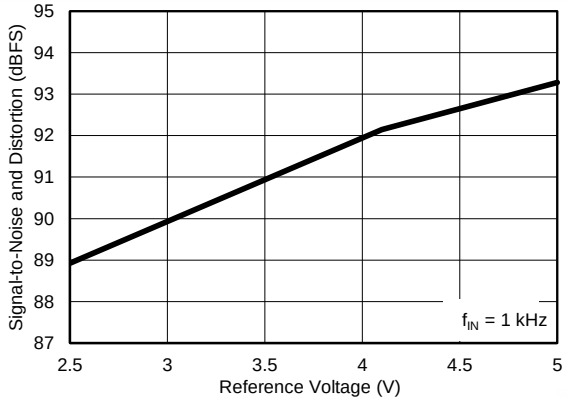

Figure 17. SINAD vs Reference Voltage

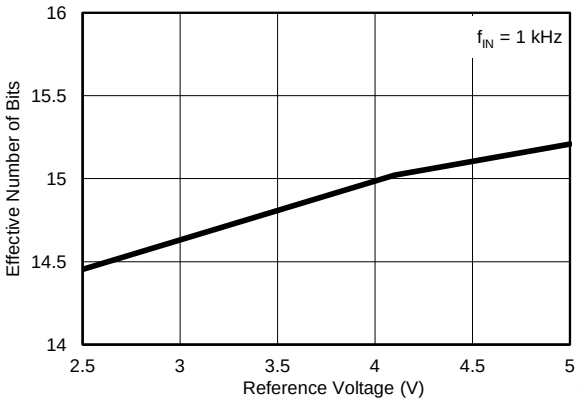

Figure 18. ENOB vs Reference Voltage

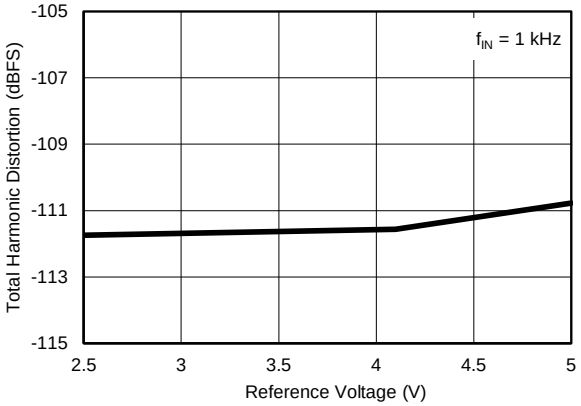

Figure 19. THD vs Reference Voltage

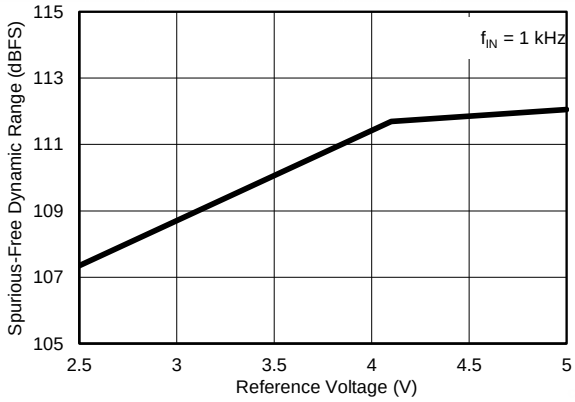

Figure 20. SFDR vs Reference Voltage

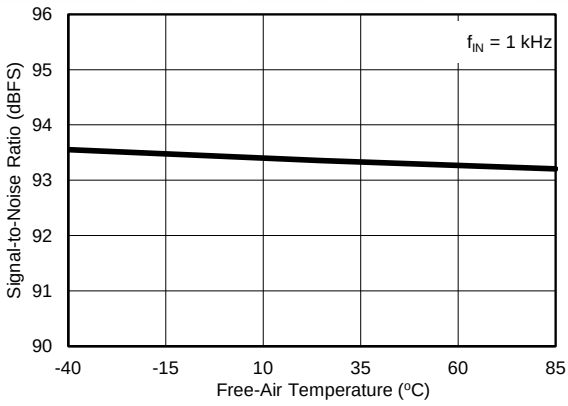

Figure 21. SNR vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

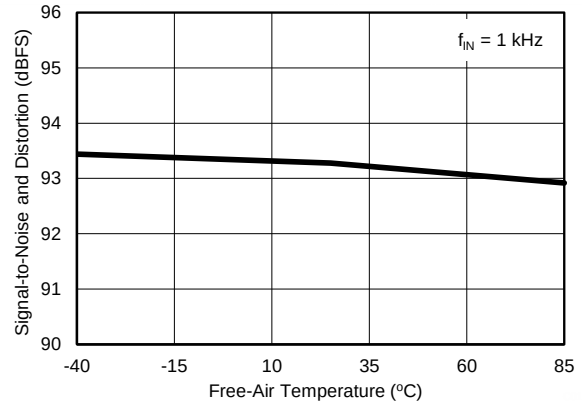

Figure 22. SINAD vs Temperature

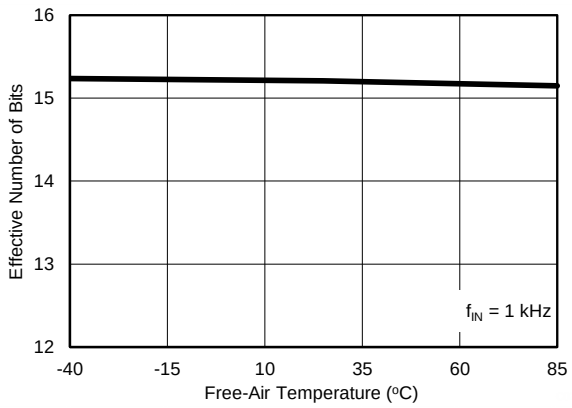

Figure 23. ENOB vs Temperature

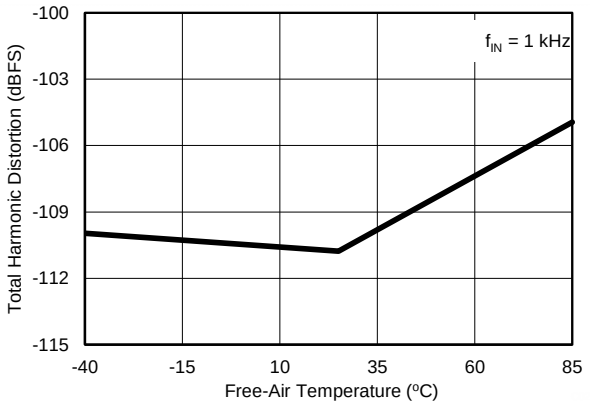

Figure 24. THD vs Temperature

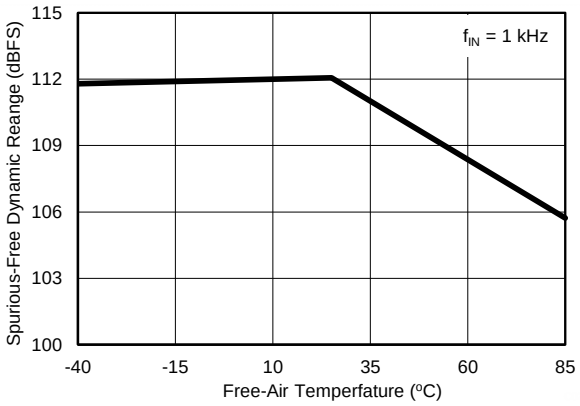

Figure 25. SFDR vs Temperature

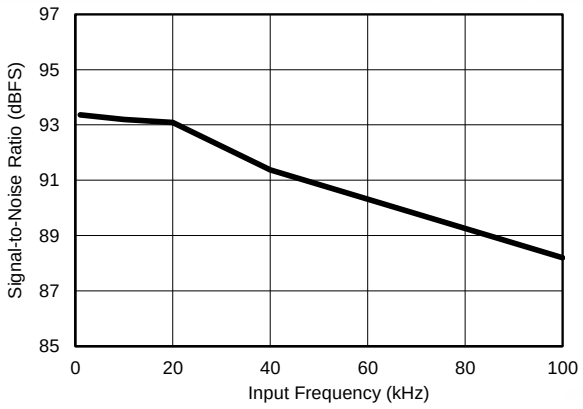

Figure 26. SNR vs Input Frequency

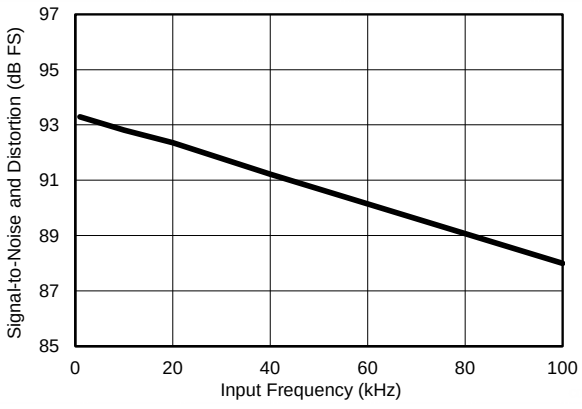

Figure 27. SINAD vs Input Frequency

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

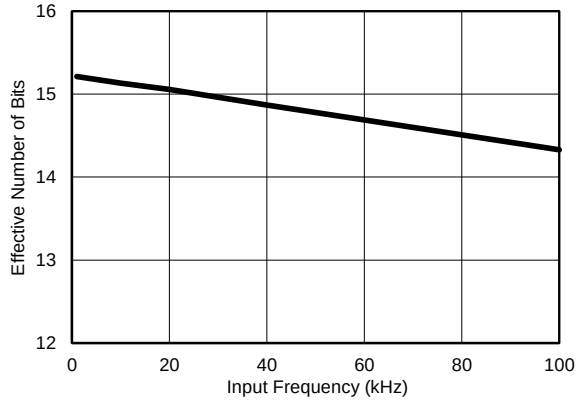

Figure 28. ENOB vs Input Frequency

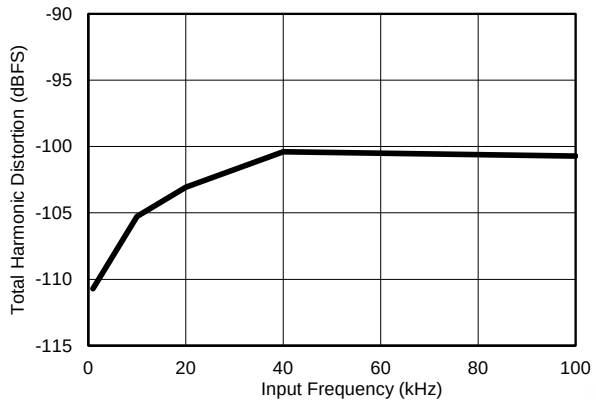

Figure 29. THD vs Input Frequency

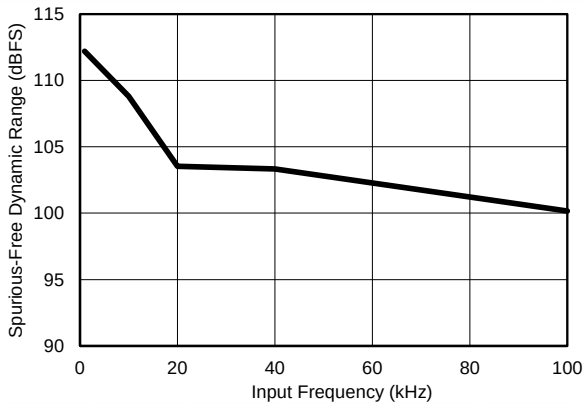

Figure 30. SFDR vs Input Frequency

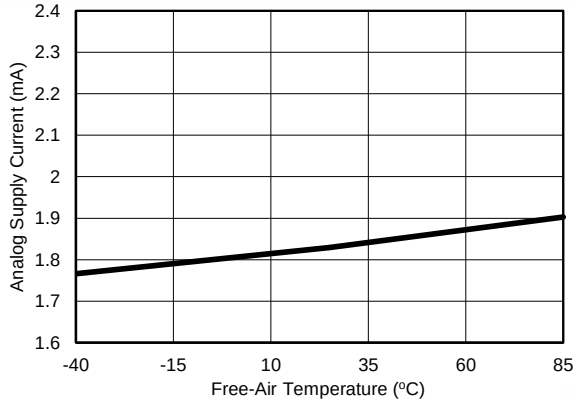

Figure 31. Supply Current vs Temperature

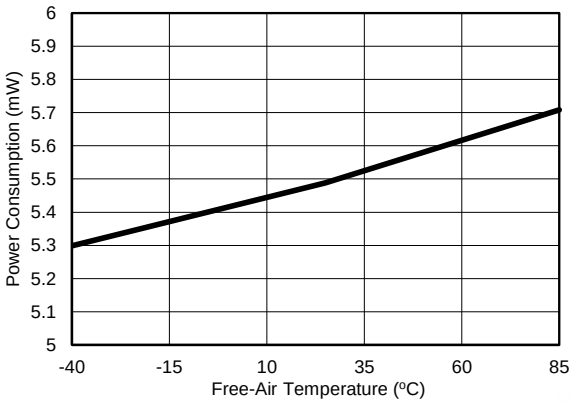

Figure 32. Power Consumption vs Temperature

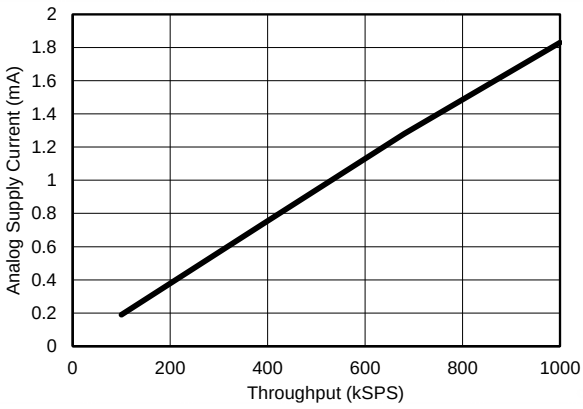

Figure 33. Supply Current vs Throughput

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

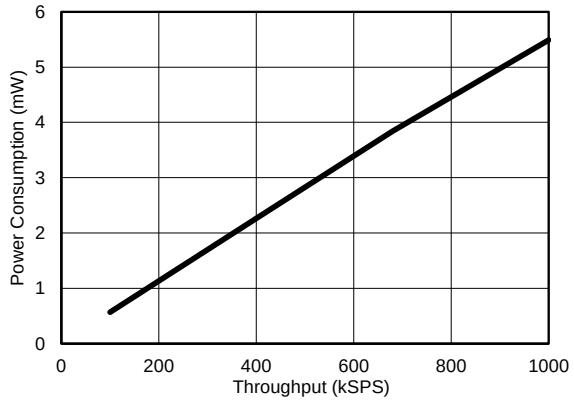

Figure 34. Power Consumption vs Throughput

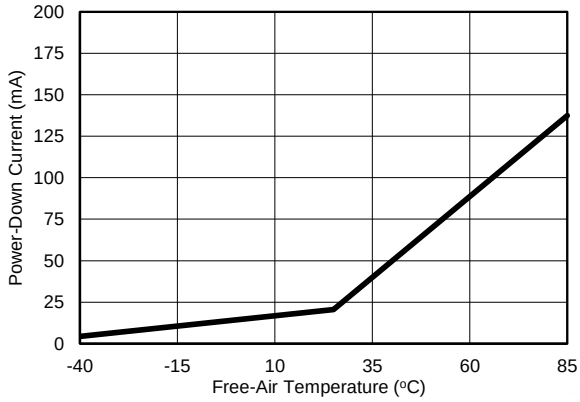

Figure 35. Power-Down Current vs Temperature

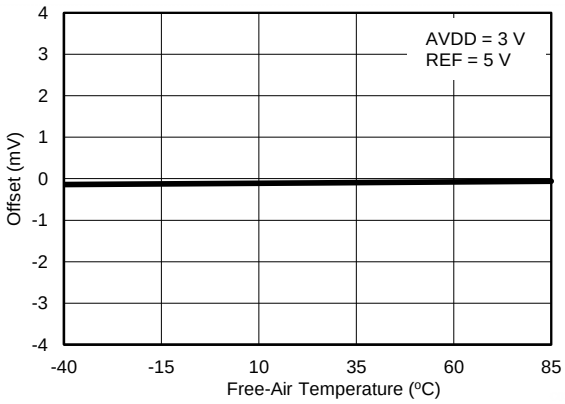

Figure 36. Offset vs Temperature

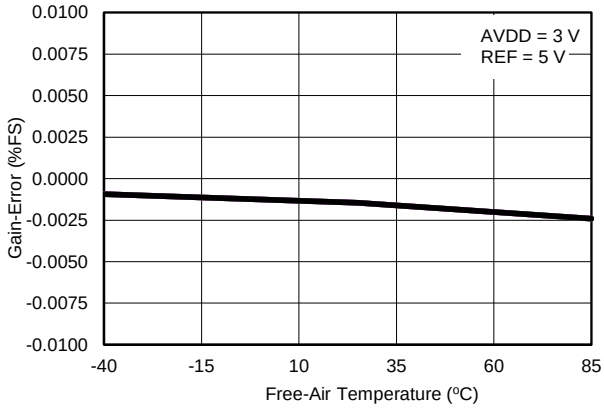

Figure 37. Gain Error vs Temperature

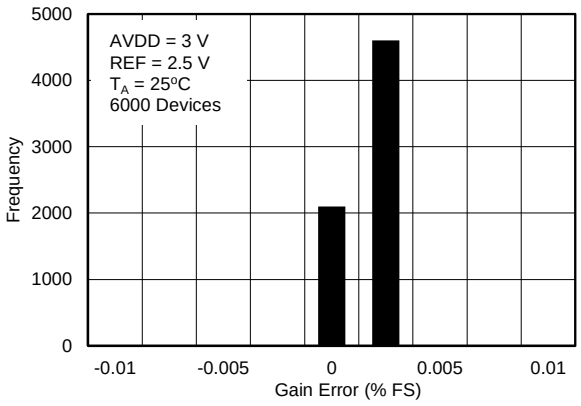

Figure 38. Typical Distribution of Gain Error

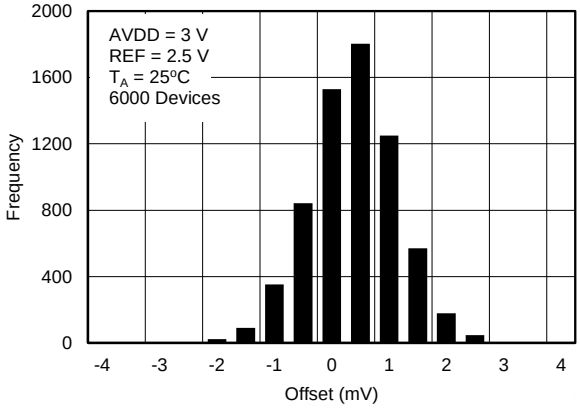

Figure 39. Typical Distribution of Offset Error

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)

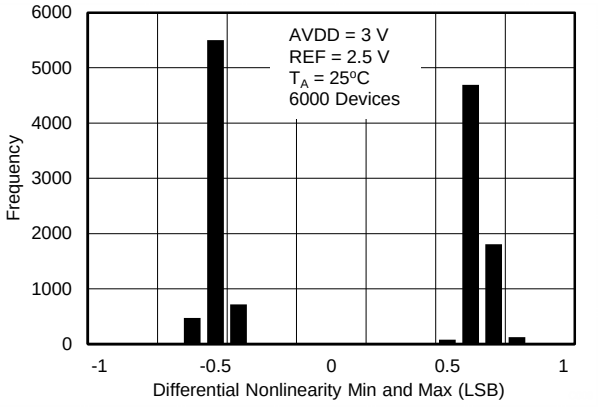

Figure 40. Typical Distribution of Differential Nonlinearity (Minimum and Maximum)

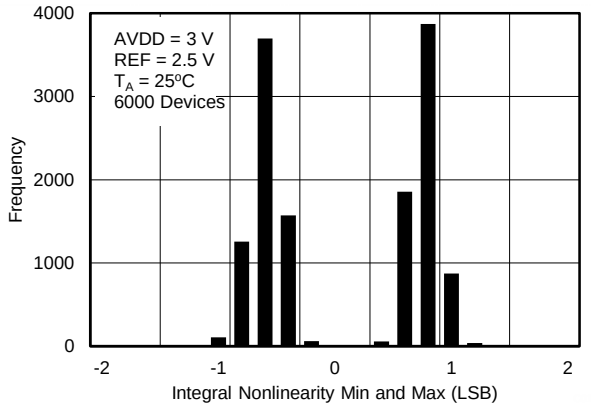

Figure 41. Typical Distribution of Integral Nonlinearity (Minimum and Maximum)

8 Parameter Measurement Information

8.1 Equivalent Circuits

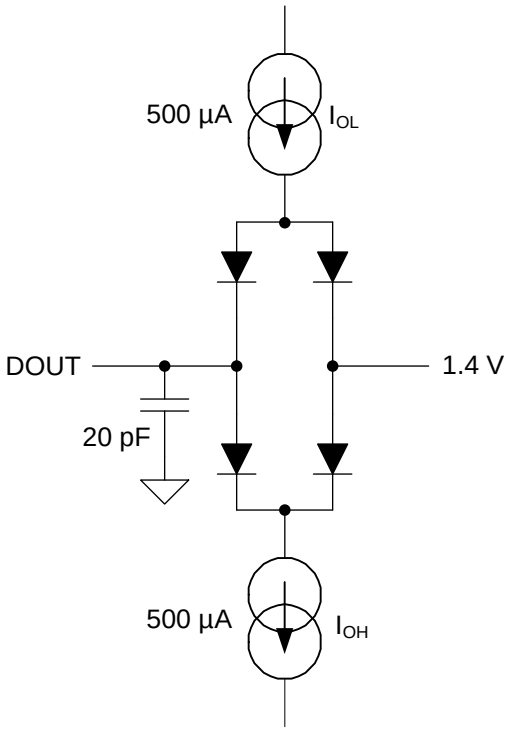

Figure 42. Load Circuit for Digital Interface Timing

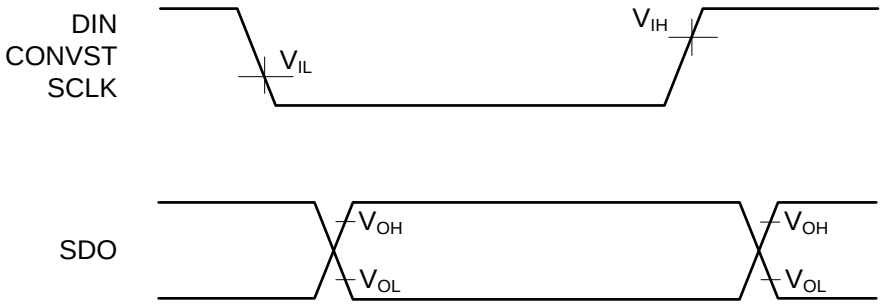

Figure 43. Voltage Levels for Timing

9 Detailed Description

9.1 Overview

The ADS8860 is a high-speed, successive approximation register (SAR), analog-to-digital converter (ADC) from a 16- and 18-bit device family. This compact device features high performance. Power consumption is inherently low and scales linearly with sampling speed. The architecture is based on charge redistribution that inherently includes a sample-and-hold (S/H) function.

The ADS8860 supports a single-ended analog input across two pins (INP and INN). When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both the INP and INN inputs are disconnected from the internal circuit.

The ADS8860 uses an internal clock to perform conversions. The device reconnects the sampling capacitors to the INP and INN pins after conversion and then enters an acquisition phase. During the acquisition phase, the device is powered down and the conversion result can be read.

The device digital output is available in SPI-compatible format, thus making interfacing with microprocessors, digital signal processors (DSPs), or field-programmable gate arrays (FPGAs) easy.

9.2 Functional Block Diagram

Figure 44 shows the detailed functional block diagram for the device.

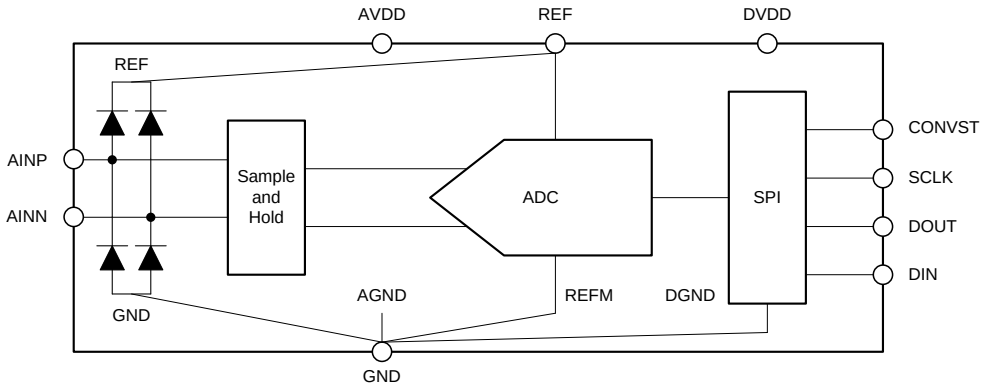

Figure 44. Detailed Block Diagram

9.3 Feature Description

9.3.1 Analog Input

As shown in Figure 44, the device features a single-ended analog input. AINP can swing from GND – 0.1 V to V_{REF} + 0.1 V and AINN can swing from GND – 0.1 V to GND + 0.1 V. Both positive and negative inputs are individually sampled on 55-pF sampling capacitors and the device converts for the voltage difference between the two sampled values: $V_{INP} – V_{INN}$. The single-ended signal range is 0 V to V_{REF}.

Feature Description (continued)

Figure 45 shows an equivalent circuit of the input sampling stage. The sampling switch is represented by a 96-Ω resistance in series with the ideal switch; see the *ADC Input Driver* section for more details on the recommended driving circuits.

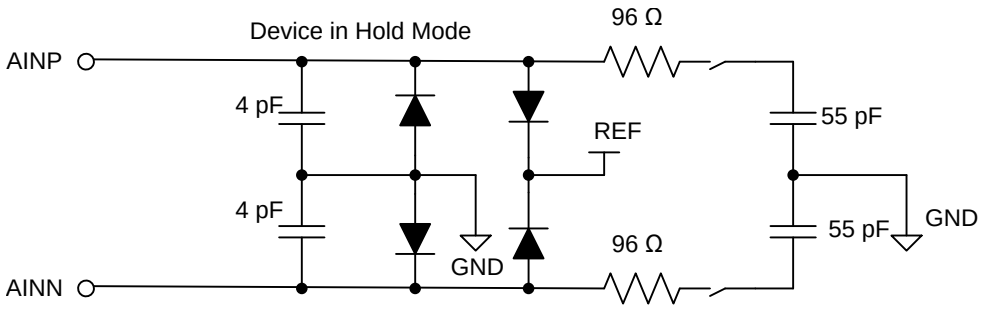

Figure 45. Input Sampling Stage Equivalent Circuit

Figure 44 and Figure 45 illustrate electrostatic discharge (ESD) protection diodes to REF and GND from both analog inputs. Make sure that these diodes do not turn on by keeping the analog inputs within the specified range.

9.3.2 Reference

The device operates with an external reference voltage and switches binary-weighted capacitors onto the reference terminal (REF pin) during the conversion process. The switching frequency is proportional to the internal conversion clock frequency but the dynamic charge requirements are a function of the absolute value of the input voltage and reference voltage. This dynamic load must be supported by a reference driver circuit without degrading the noise and linearity performance of the device. During the acquisition process, the device automatically powers down and does not take any dynamic current from the external reference source. The basic circuit diagram for such a reference driver circuit for precision ADCs is shown in Figure 46; see the *ADC Reference Driver* section for more details on the application circuits.

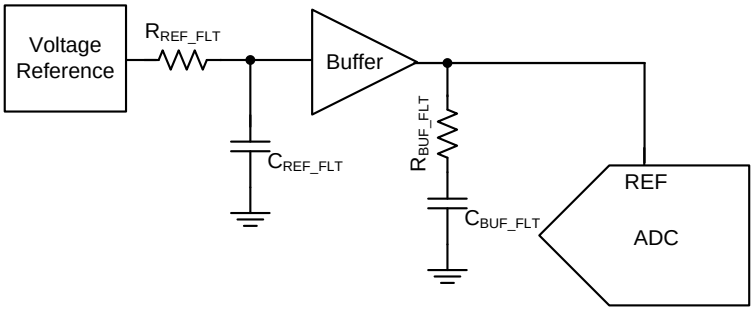

Figure 46. Reference Driver Schematic

9.3.3 Clock

The device uses an internal clock for conversion. Conversion duration may vary but is bounded by the minimum and maximum value of t_{conv}, as specified in the *Timing Requirements* section. An external SCLK is only used for a serial data read operation. Data are read after a conversion completes and when the device is in acquisition phase for the next sample.

Feature Description (continued)

9.3.4 ADC Transfer Function

The ADS8860 is a unipolar, single-ended input device. The device output is in straight binary format.

Figure 47 shows ideal characteristics for the device. The full-scale range for the ADC input (AINP – AINN) is equal to the reference input voltage to the ADC (V_{REF}). One LSB is equal to [(V_{REF} / 2^{16})].

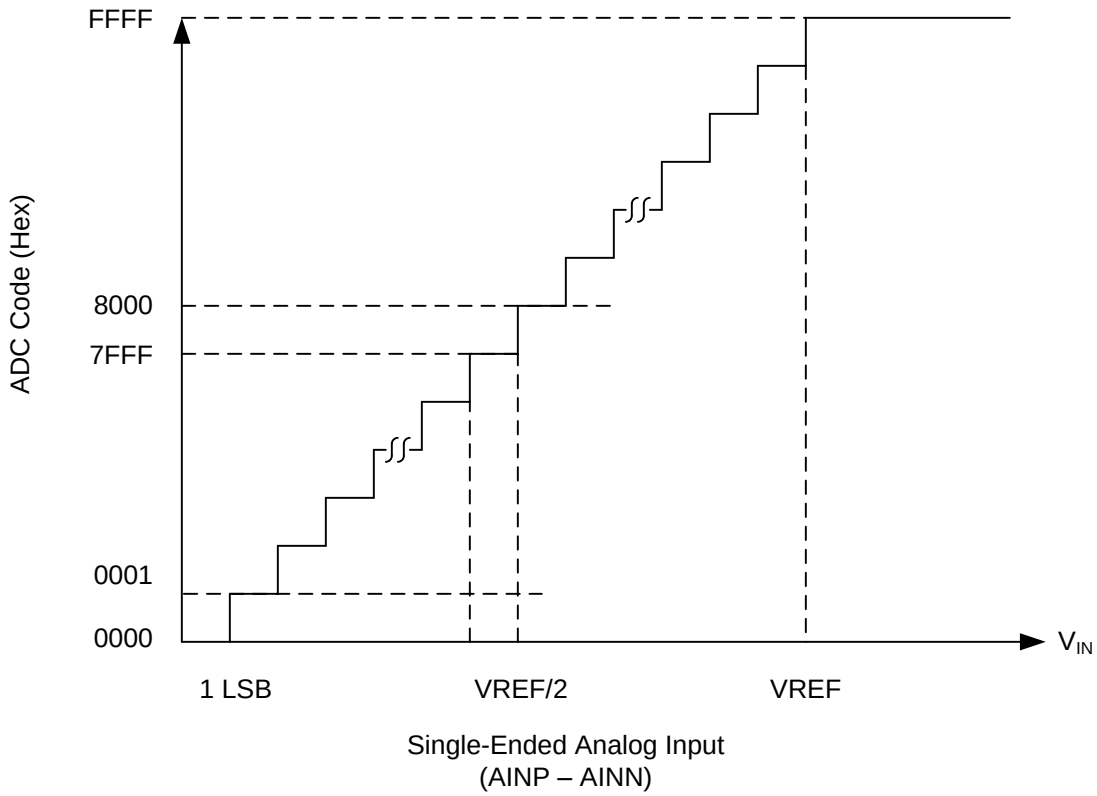

Figure 47. Single-Ended Transfer Characteristics

9.4 Device Functional Modes

The ADS8860 is a low pin-count device. However, the device offers six different options for interfacing with the digital host.

These options can be broadly classified as being either *$\overline{CS}$ mode* (in either a 3- or 4-wire interface) or *daisy-chain mode*. The device operates in $\overline{CS}$ mode if DIN is high at the CONVST rising edge. If DIN is low at the CONVST rising edge, or if DIN and CONVST are connected together, the device operates in daisy-chain mode. In both modes, the device can either operate with or without a *busy indicator*, where the busy indicator is a bit preceding the output data bits that can be used to interrupt the digital host and trigger the data transfer.

The 3-wire interface in $\overline{CS}$ mode is useful for applications that need galvanic isolation on-board. The 4-wire interface in $\overline{CS}$ mode allows the user to sample the analog input independent of the serial interface timing and, therefore, allows easier control of an individual device while having multiple, similar devices on-board. The daisy-chain mode is provided to hook multiple devices in a chain similar to a shift register and is useful in reducing component count and the number of signal traces on the board.

9.4.1 $\overline{CS}$ Mode

$\overline{CS}$ mode is selected if DIN is high at the CONVST rising edge. There are six different interface options available in this mode: 3-wire $\overline{CS}$ mode without a busy indicator, 3-wire $\overline{CS}$ mode with a busy indicator, 4-wire $\overline{CS}$ mode without a busy indicator, and 4-wire $\overline{CS}$ mode with a busy indicator. The following sections discuss these interface options in detail.

Device Functional Modes (continued)

9.4.1.1 3-Wire $\overline{CS}$ Mode Without a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host. In this interface option, DIN can be connected to DVDD and CONVST functions as $\overline{CS}$ (as shown in Figure 48). As shown in Figure 49, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must return high before the minimum conversion time ($t_{conv-min}$) elapses and is held high until the maximum possible conversion time ($t_{conv-max}$) elapses. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

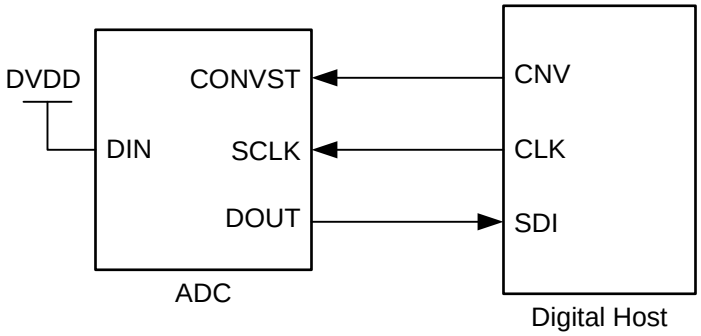

Figure 48. Connection Diagram: 3-Wire $\overline{CS}$ Mode Without a Busy Indicator (DIN = 1)

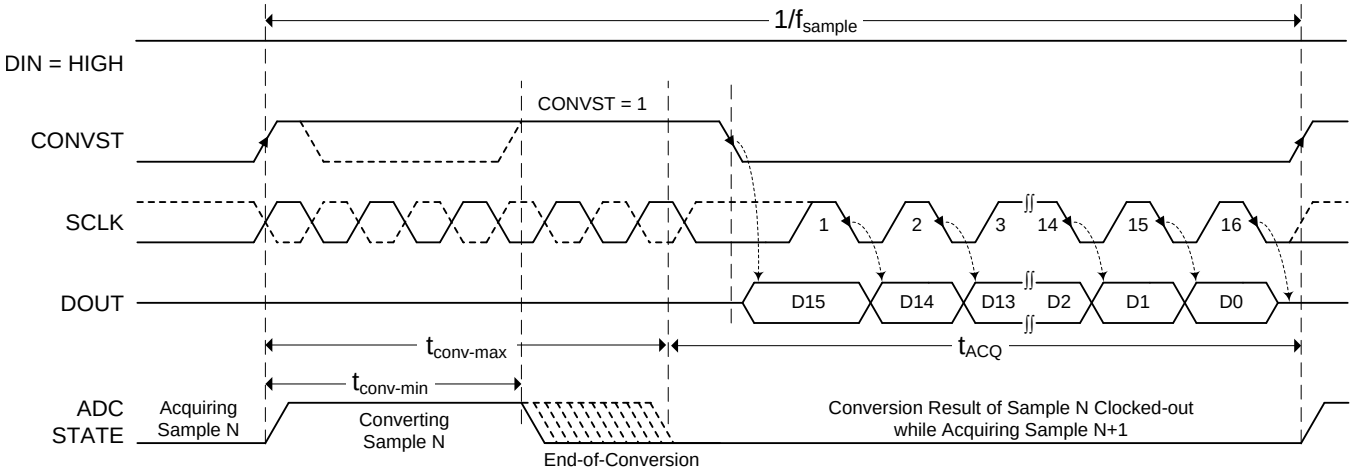

Figure 49. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode Without a Busy Indicator (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down. CONVST (functioning as $\overline{CS}$) can be brought low after the maximum conversion time ($t_{conv-max}$) elapses. On the CONVST falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h\_CK\_DO-min}$ time frame. DOUT goes to 3-state after the 16th SCLK falling edge or when CONVST goes high, whichever occurs first.

Device Functional Modes (continued)

9.4.1.2 3-Wire $\overline{CS}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, DIN can be connected to DVDD and CONVST functions as $\overline{CS}$ (as shown in Figure 50). The pull-up resistor on the DOUT pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 51, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must be pulled low before the minimum conversion time ($t_{conv-min}$) elapses and must remain low until the maximum possible conversion time ($t_{conv-max}$) elapses. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator.

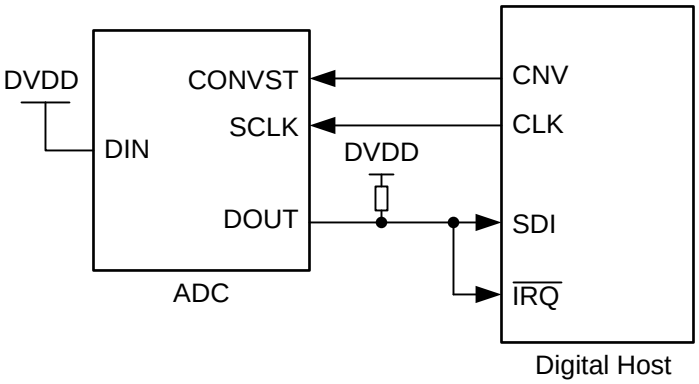

Figure 50. Connection Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator

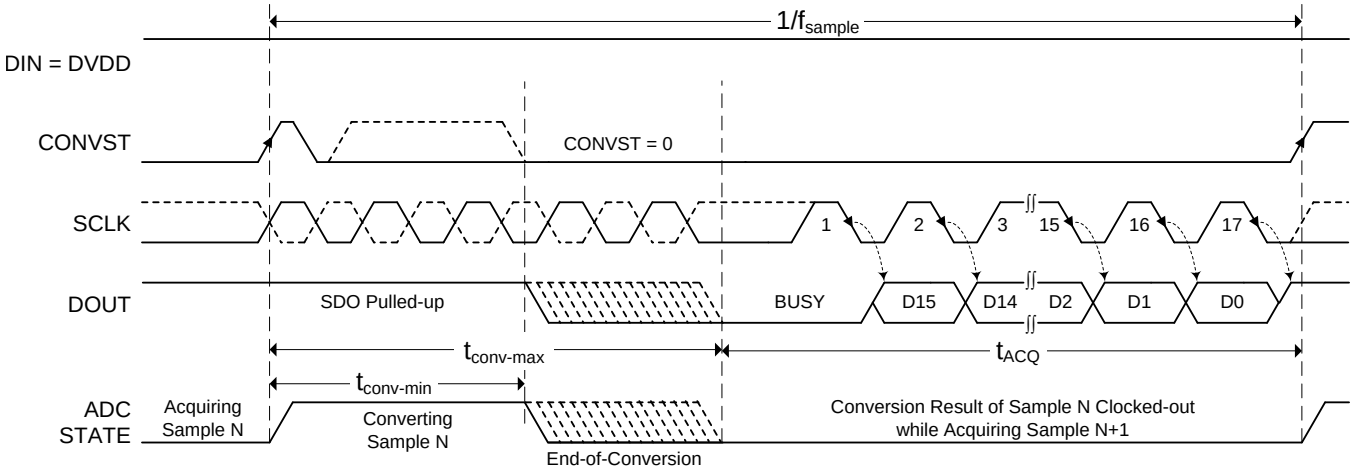

Figure 51. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h\_CK\_DO-min}$ time frame. DOUT goes to 3-state after the 17th SCLK falling edge or when CONVST goes high, whichever occurs first.

Device Functional Modes (continued)

9.4.1.3 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

This interface option is useful when one or more ADCs are connected to an SPI-compatible digital host. Figure 52 shows the connection diagram for single ADC; see Figure 54 for the connection diagram for two ADCs.

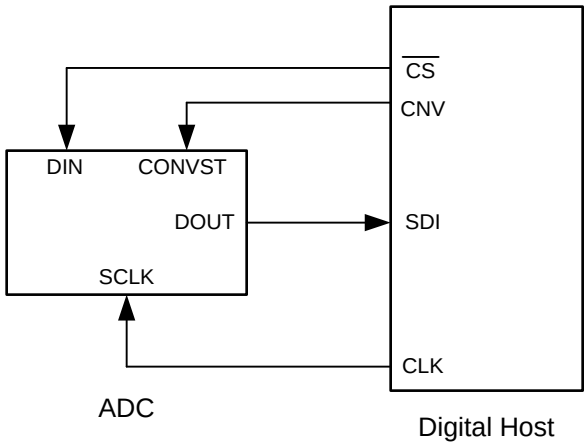

Figure 52. Connection Diagram: Single ADC With 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

In this interface option, DIN is controlled by the digital host and functions as $\overline{CS}$. As shown in Figure 53, with DIN high, a CONVST rising edge selects $\overline{CS}$ mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (functioning as $\overline{CS}$) can be pulled low to select other devices on the board. However, DIN must be pulled high before the minimum conversion time ($t_{conv-min}$) elapses and remains high until the maximum possible conversion time ($t_{conv-max}$) elapses. A high level on DIN at the end of the conversion ensures the device does not generate a busy indicator.

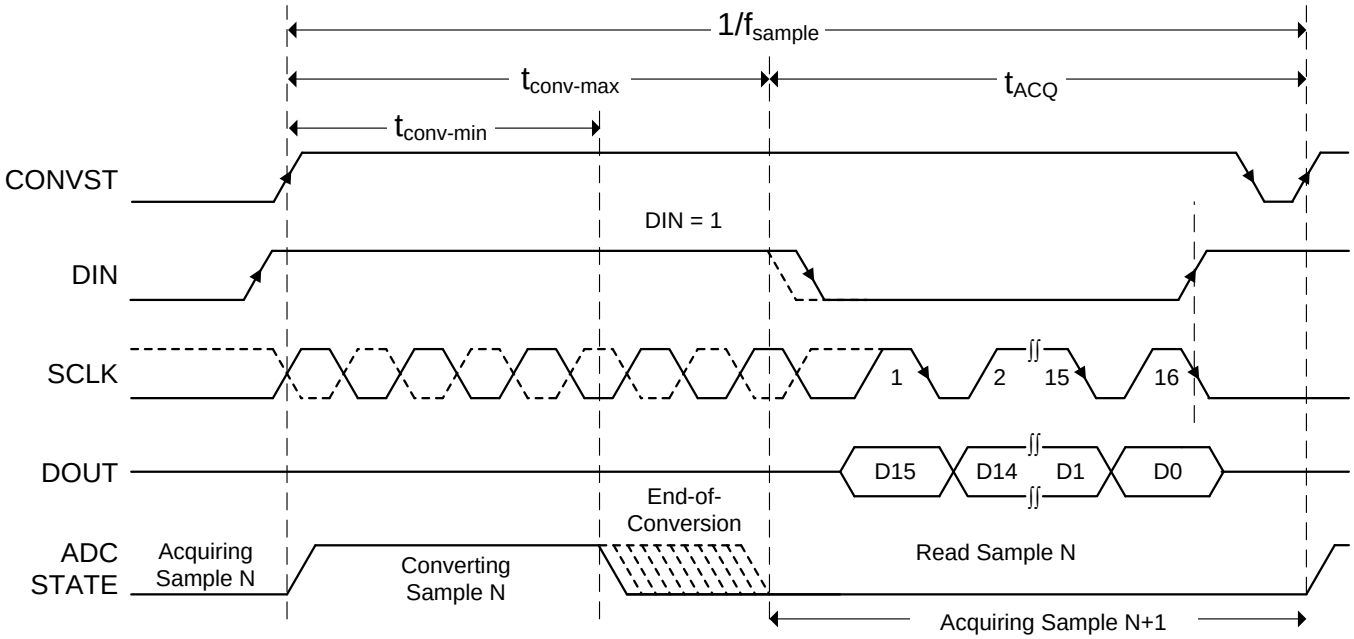

Figure 53. Interface Timing Diagram: Single ADC With 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

Device Functional Modes (continued)

When conversion is complete, the device enters acquisition phase and powers down. DIN (functioning as $\overline{CS}$) can be brought low after the maximum conversion time ($t_{conv-max}$) elapses. On the DIN falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h\_CK\_DO-min}$ time frame. DOUT goes to 3-state after the 16th SCLK falling edge or when DIN goes high, whichever occurs first.

As shown in Figure 54, multiple devices can be hooked together on the same data bus. In this case, as shown in Figure 55, the DIN of the second device (functioning as $\overline{CS}$ for the second device) can go low after the first device data are read and the DOUT of the first device is in 3-state.

Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

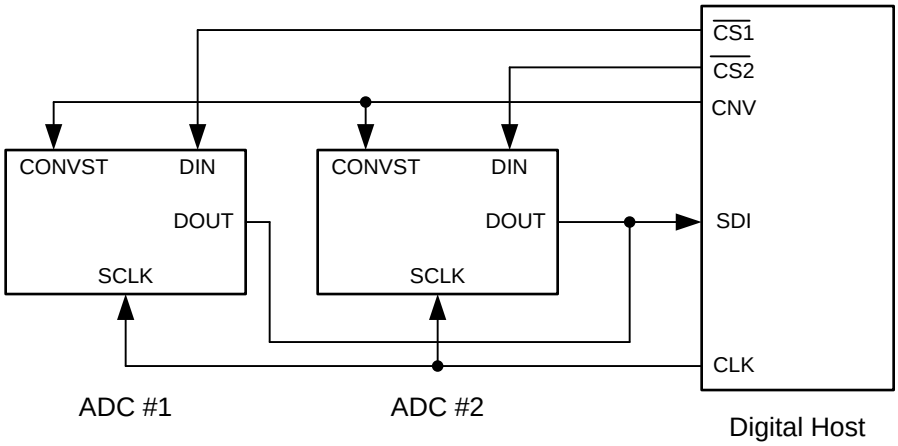

Figure 54. Connection Diagram: Two ADCs With 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

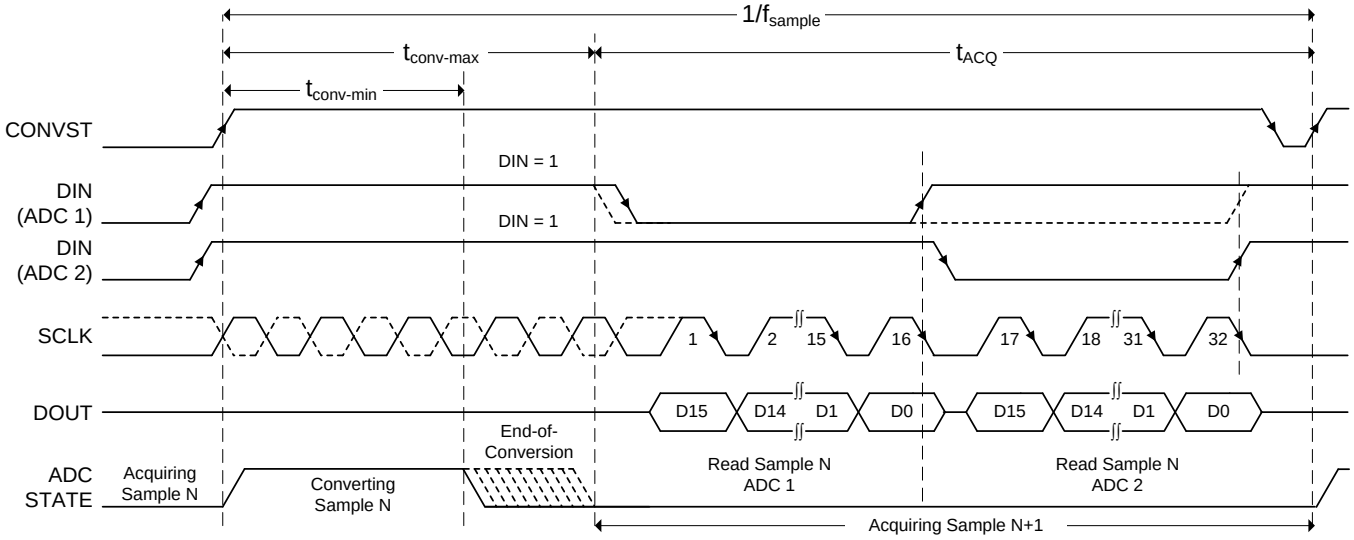

Figure 55. Interface Timing Diagram: Two ADCs With 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

Device Functional Modes (continued)

9.4.1.4 4-Wire $\overline{CS}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, the analog sample is least affected by clock jitter because the CONVST signal (used to sample the input) is independent of the data read operation. In this interface option, DIN is controlled by the digital host and functions as $\overline{CS}$ (as shown in Figure 56). The pull-up resistor on the DOUT pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 57, when DIN is high, a CONVST rising edge selects $\overline{CS}$ mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held high from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (acting as $\overline{CS}$) can be pulled low to select other devices on the board. However, DIN must be pulled low before the minimum conversion time ($t_{conv-min}$) elapses and remains low until the maximum possible conversion time ($t_{conv-max}$) elapses. A low level on the DIN input at the end of a conversion ensures the device generates a busy indicator.

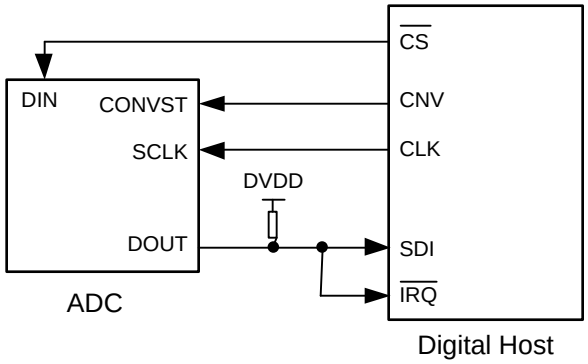

Figure 56. Connection Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

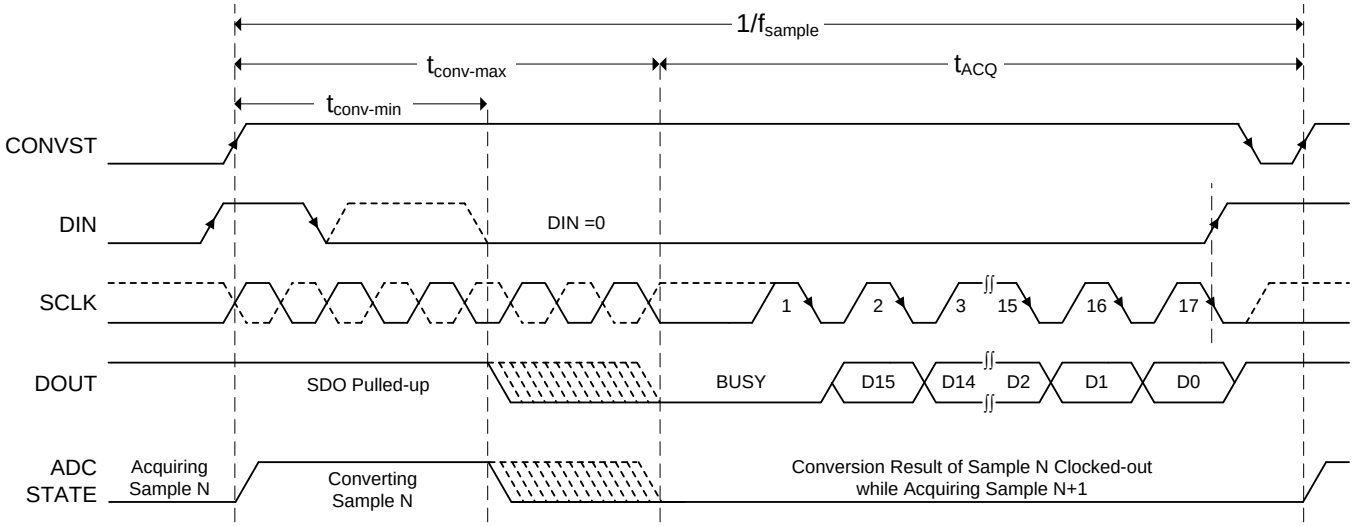

Figure 57. Interface Timing Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

Device Functional Modes (continued)

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h\_CK\_DO\text{-}min}$ time frame. DOUT goes to 3-state after the 17th SCLK falling edge or when DIN goes high, whichever occurs first. Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

9.4.2 Daisy-Chain Mode

Daisy-chain mode is selected if DIN is low at the time of a CONVST rising edge or if DIN and CONVST are connected together. Similar to $\overline{CS}$ mode, this mode features operation with or without a busy indicator. The following sections discuss these interface modes in detail.

9.4.2.1 Daisy-Chain Mode Without a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability. Figure 58 shows a connection diagram with *N* ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 (DIN-1) is connected to GND. The DOUT pin of ADC 1 (DOUT-1) is connected to the DIN pin of ADC 2 (DIN-2), and so on. The DOUT pin of the last ADC in the chain (DOUT-N) is connected to the SDI pin of the digital host.

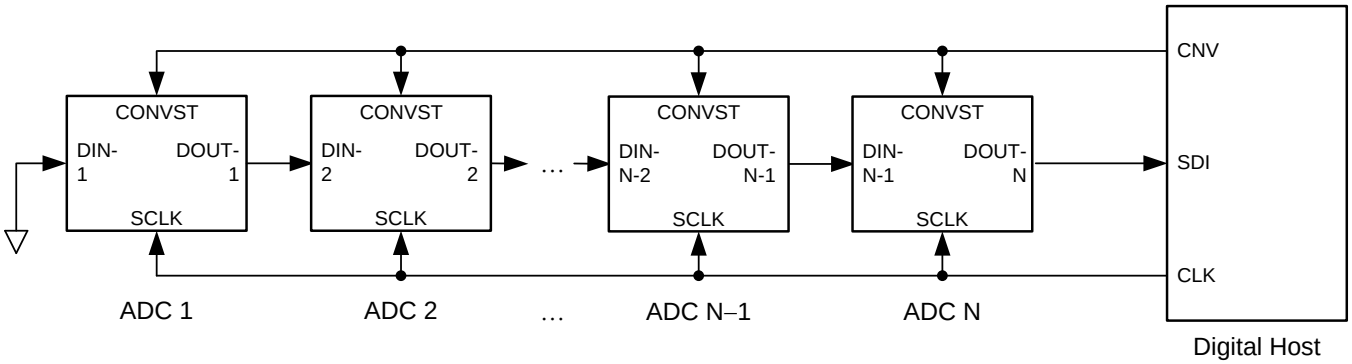

Figure 58. Connection Diagram: Daisy-Chain Mode Without a Busy Indicator (DIN = 0)

Device Functional Modes (continued)

As shown in Figure 59, the device DOUT pin is driven low when DIN and CONVST are low together. With DIN low, a CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be low at the CONVST rising edge so that the device does not generate a busy indicator at the end of the conversion.

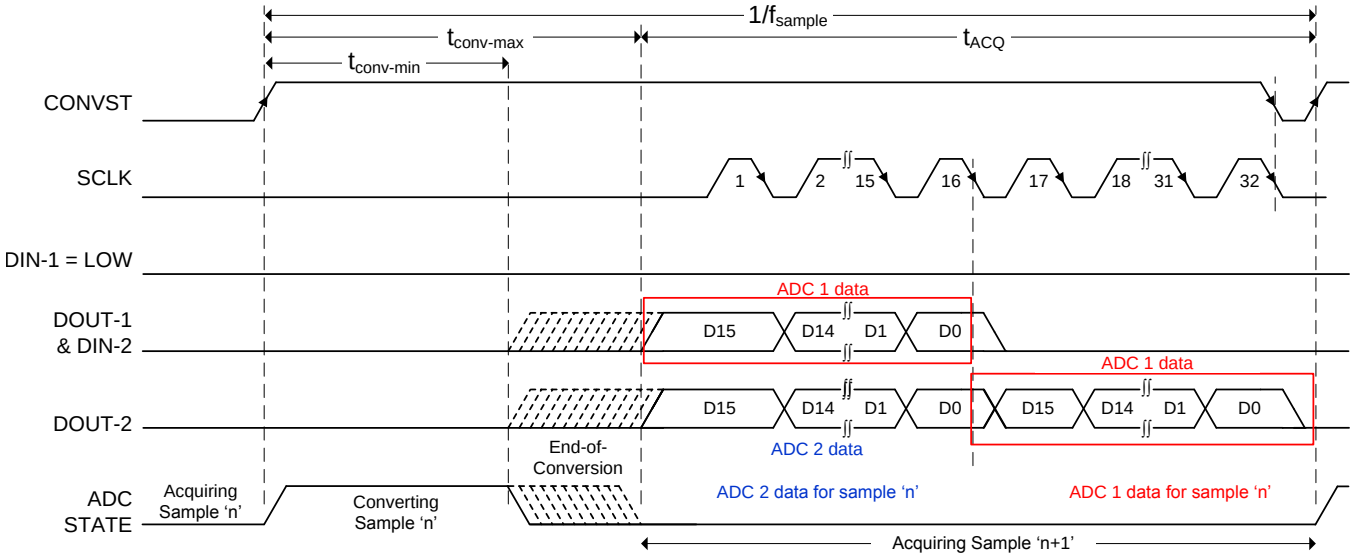

Figure 59. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode Without a Busy Indicator

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 16-bit, shift register and also outputs the MSB bit of this conversion result on its own DOUT pin. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the data of ADC N, followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of 16 x *N* SCLK falling edges are required to capture the outputs of all *N* devices in the chain. Fast sampling rates require high frequency SCLK and data must be read at SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. Note that with any SCLK frequency, reading data at SCLK falling edge requires the digital host to clock in the data during the $t_{h\_CK\_DO\text{-}min}$ time frame.

Device Functional Modes (continued)

9.4.2.2 Daisy-Chain Mode With a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability and an interrupt-driven data transfer is desired. Figure 60 shows a connection diagram with *N* ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 (DIN-1) is connected to its CONVST. The DOUT pin of ADC 1 (DOUT-1) is connected to the DIN pin of ADC 2 (DIN-2), and so on. The DOUT pin of the last ADC in the chain (DOUT-N) is connected to the SDI and IRQ pins of the digital host.

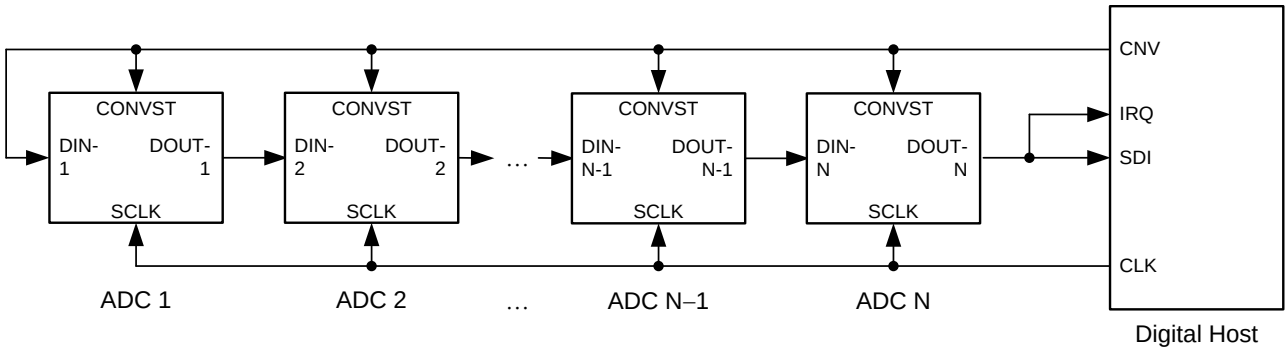

Figure 60. Connection Diagram: Daisy-Chain Mode With a Busy Indicator (DIN = 0)

Device Functional Modes (continued)

As shown in Figure 61, the device DOUT pin is driven low when DIN and CONVST are low together. A CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be high at the CONVST rising edge so that the device generates a busy indicator at the end of the conversion.

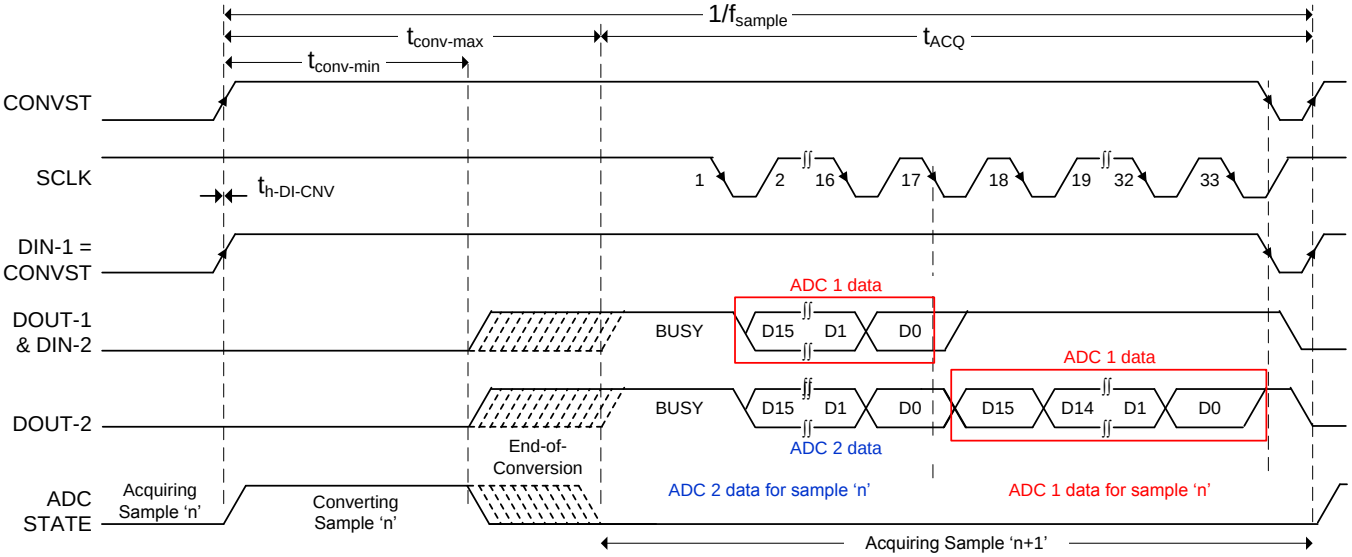

Figure 61. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode With a Busy Indicator

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 16-bit, shift register and also forces its DOUT pin high, thereby providing a low-to-high transition on the IRQ pin of the digital host. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the interrupt signal followed by the data of ADC N followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of (16 × N) + 1 SCLK falling edges are required to capture the outputs of all *N* devices in the chain. Fast sampling rates require a high-frequency SCLK and data must be read at the SCLK falling edges. For slow sampling rates and SCLK frequency ≤ 36 MHz, data can be read at either SCLK falling or rising edges. With any SCLK frequency, reading data at the SCLK falling edge requires the digital host to clock in the data during the $t_{h\_CK\_DO-min}$ time frame. The busy indicator bits of ADC 1 to ADC N–1 do not propagate to the next device in the chain.

NOTE

For SCLK ≤ 36 MHz, SPI mode-3 (CPOL = 1, CPHA = 1) allows reading the conversion results of N ADCs in 18 × N SCLK cycles because the busy indicator bit is not clocked in by the host.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, followed by some application circuits designed using the ADS8860.

10.1.1 ADC Reference Driver

The external reference source to the ADS8860 must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few hundred μV_{RMS}. Therefore, to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz.

After band-limiting the noise of the reference circuit, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. The reference buffer must regulate the voltage at the reference pin such that the value of V_{REF} stays within the 1-LSB error at the start of each conversion. This condition necessitates the use of a large capacitor, C_{BUF_FLT} (see Figure 46) for regulating the voltage at the reference input of the ADC. The amplifier selected to drive the reference pin must have an extremely low offset and temperature drift with a low output impedance to drive the capacitor at the ADC reference pin without any stability issues.

10.1.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision, 16-bit ADC such as the ADS8860.

10.1.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (see the *Antialiasing Filter* section) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, select the amplifier bandwidth as described in Equation 1:

$$Unity-Gain\ Bandwidth \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (1)$$

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in Equation 2.

Application Information (continued)

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \quad \leq \quad \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)}$$

where:

- $V_{1\ /\ f\_AMP\_PP}$ is the peak-to-peak flicker noise in µV,
- e_{n_RMS} is the amplifier broadband noise density in nV/√Hz,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration. (2)

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as shown in Equation 3.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \tag{3}$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within an 16-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, always verify the settling behavior of the input driver by TINA™-SPICE simulations before selecting the amplifier.

10.1.2.2 Charge-Kickback Filter

The charge-kickback filter is an RC filter at the input pins of the ADC that filters the broadband noise from the front-end drive circuitry and attenuates the sampling charge injection from the switched-capacitor input stage of the ADC. As shown in Figure 62, a filter capacitor (C_{FLT}) is connected from each input pin of the ADC to ground. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For the ADS8860, the input sampling capacitance is equal to 59 pF; therefore, for optimal performance, keep C_{FLT} greater than 590 pF. This capacitor must be a COG- or NPO-type. The type of dielectric used in COG or NPO ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

Driving capacitive loads can degrade the phase margin of the input amplifier, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} helps with amplifier stability, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability of the driver amplifier and distortion performance of the design. Always verify the stability and settling behavior of the driving amplifier and charge-kickback filter by a TINA-TI™ SPICE simulation. Keep the tolerance of the selected resistors less than 1% to keep the inputs balanced.

$$f_{-3dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

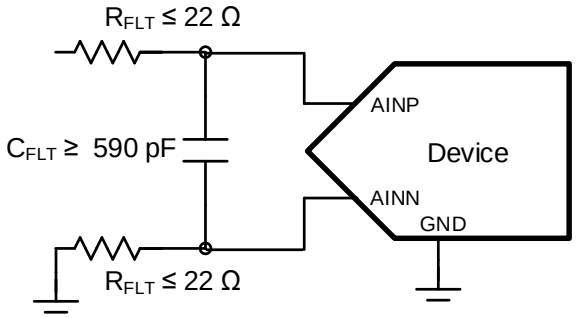

Figure 62. Charge-Kickback Filter

Application Information (continued)

This section describes some common application circuits using the ADS8860. These data acquisition (DAQ) blocks are optimized for specific input types and performance requirements of the system. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; see the *Power-Supply Decoupling* section for suggested guidelines.

10.2 Typical Applications

10.2.1 DAQ Circuit for a 1-µs, Full-Scale Step Response

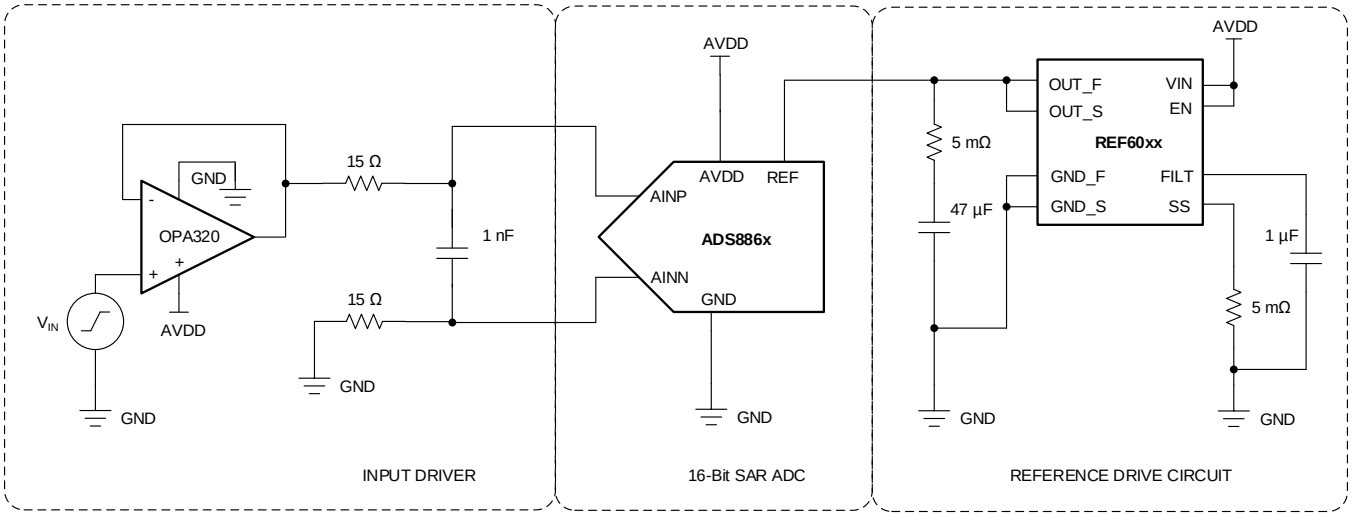

Figure 63. DAQ Circuit for a 1-µs, Full-Scale Step Response

10.2.1.1 Design Requirements

Step input signals are common in multiplexed applications when switching between different channels. In the worst-case scenario, one channel is at the negative full-scale (NFS) and the other channel is at the positive full-scale (PFS) voltage, in which case the step size is the full-scale range (FSR) of the ADC when the MUX channel is switched.

Design an application circuit optimized for using the ADS8860 to achieve

- Full-scale step input settling to 16-bit accuracy and
- INL of < ±2 LSB and
- Maximum specified throughput of 1 MSPS

10.2.1.2 Detailed Design Procedure

The application circuit is shown in Figure 63.

In such applications, the primary design requirement is to ensure that the full-scale step input signal settles to 16-bit accuracy at the ADC inputs. This condition is critical to achieve the excellent linearity specifications of the ADC. Therefore, the bandwidth of the charge-kickback RC filter must be large enough to allow optimal settling of the input signal during the ADC acquisition time. The filter capacitor helps reduce the sampling charge injection at the ADC inputs, but degrades the phase margin of the driving amplifier, thereby leading to stability issues. Amplifier stability is maintained by the series isolation resistor.

During the conversion process, binary-weighted capacitors are switched onto the REF pin. In order to support this dynamic load the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer.

The REF60xx family of voltage references are able to maintain an output voltage within 1 LSB (16-bit) with minimal droop, even during the first conversion while driving the REF pin of the ADS8860. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems.

Typical Applications (continued)

For the input driving amplifiers, key specifications include rail-to-rail input and output swing, high bandwidth, high slew rate, and fast settling time. The CMOS amplifier meets all these specification requirements for this circuit with a single-supply and low quiescent current. The component values of the antialiasing filter are selected to meet the settling requirements of the system as well as to maintain the stability of the input driving amplifiers.

10.2.2 DAQ Circuit for Lowest Distortion and Noise Performance at 1 MSPS

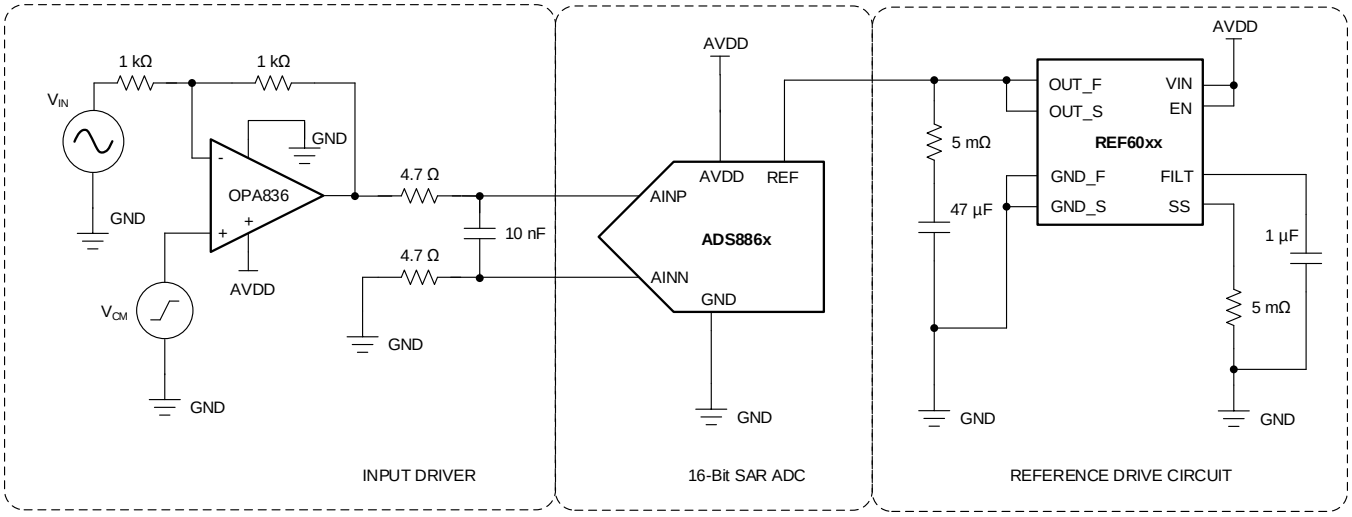

Figure 64. DAQ Circuit for Lowest Distortion and Noise at 1 MSPS

10.2.2.1 Design Requirements

Design an application circuit optimized for using the ADS8860 to achieve

- > 94.5-dB SNR, < –110-dB THD and
- ± 1-LSB linearity and
- maximum specified throughput of 1 MSPS

10.2.2.2 Detailed Design Procedure

This section describes an application circuit (as shown in Figure 64) optimized for using the ADS8860 with lowest distortion and noise performance at a throughput of 1 MSPS. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADC.

As a rule of thumb, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the input of the amplifier. Therefore, the circuit uses the low-power OPA836 as an input driver, which provides exceptional ac performance because of its extremely low-distortion, high-bandwidth specifications.

In addition, the components of the charge-kickback filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

Typical Applications (continued)

10.2.3 Ultralow-Power DAQ Circuit at 10 kSPS

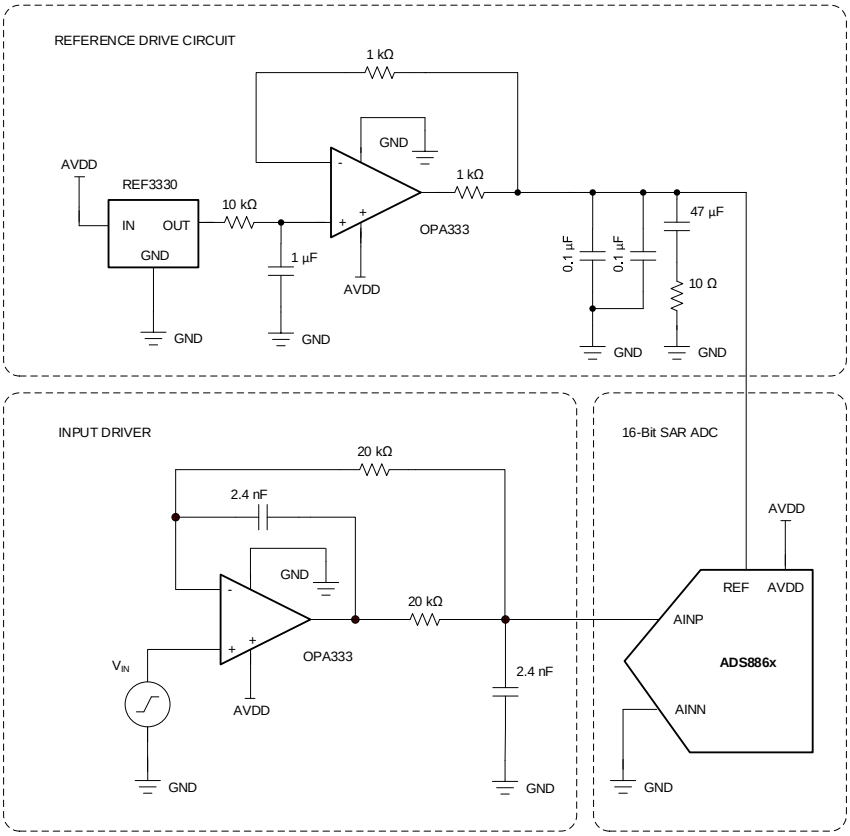

Figure 65. Ultralow-Power DAQ Circuit at 10 kSPS

10.2.3.1 Design Requirements

Portable and battery-powered applications require ultralow-power consumption and do not need very high throughput from the ADC.

Design a single-supply, data acquisition circuit optimized for using the ADS8860 to achieve

- ENOB > 14.5 bits and
- Ultralow-power consumption of < 1 mW at throughput of 10 kSPS

10.2.3.2 Detailed Design Procedure

The data acquisition circuit shown in Figure 65 is optimized for using the ADS8860 at a reduced throughput of 10 kSPS

In order to save power, this circuit is operated on a single 3.3-V supply. The circuit uses the OPA333 with a maximum quiescent current of 28 µA in order to drive the ADC input. The input amplifier is configured in a modified unity-gain buffer configuration. The filter capacitor at the ADC inputs attenuates the sampling charge injection noise from the ADC but effects the stability of the input amplifiers by degrading the phase margin. This attenuation requires a series isolation resistor to maintain amplifier stability. The value of the series resistor is directly proportional to the open-loop output impedance of the driving amplifier to maintain stability, which is high (in the order of kΩ) in the case of low-power amplifiers such as the OPA333. Therefore, a high value of 1 kΩ is selected for the series resistor at the ADC inputs. However, this series resistor creates an additional voltage drop in the signal path, thereby leading to linearity and distortion issues. The dual-feedback configuration used in Figure 65 corrects for this additional voltage drop and maintains system performance at ultralow-power consumption.

11 Power Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range. During normal operation, if the voltage on the AVDD supply drops below the AVDD minimum specification, then TI recommends ramping the AVDD supply down to ≤ 0.7 V before power up. Also, during power-up, AVDD must monotonously rise to the desired operating voltage above the minimum AVDD specification.

11.1 Power-Supply Decoupling

Decouple the AVDD and DVDD pins with GND, using individual 1-µF decoupling capacitors placed in close proximity to the pin, as shown in 图 66.

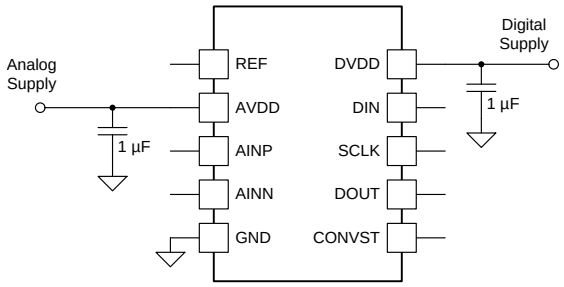

图 66. Supply Decoupling

11.2 Power Saving

The device has an auto power-down feature that powers down the internal circuitry at the end of every conversion. Referring to 图 67, the input signal is acquired on the sampling capacitors when the device is in a power-down state (t_{acq}); at the same time, the result for the previous conversion is available for reading. The device powers up on the start of the next conversion. During conversion phase (t_{conv}), the device also consumes current from the reference source (connected to the REF pin).

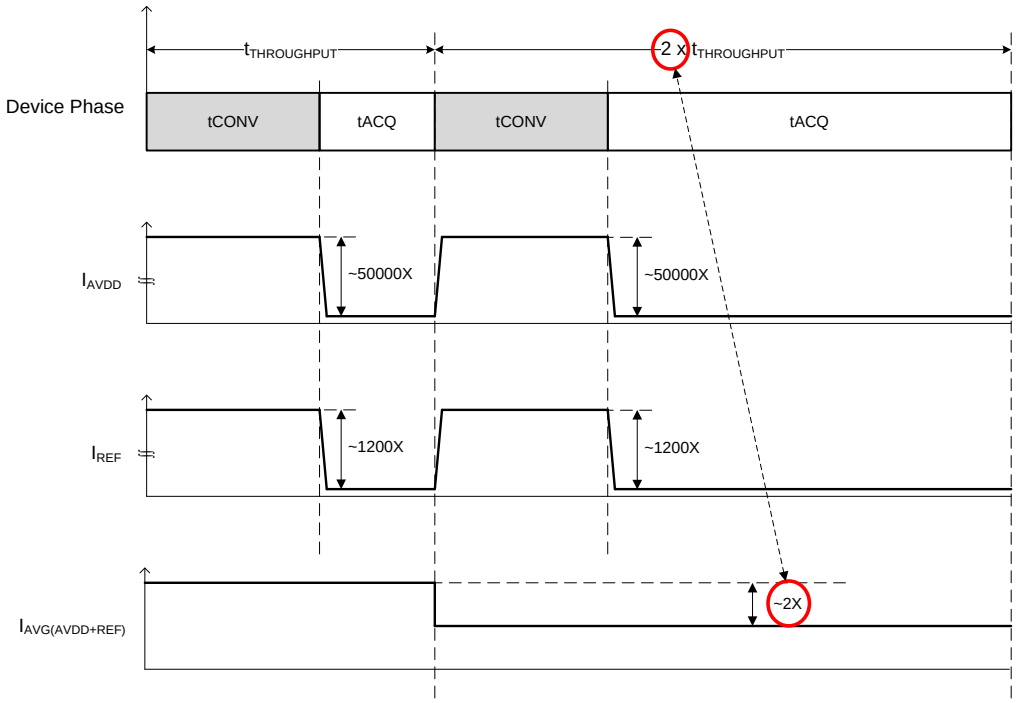

图 67. Power Scaling With Throughput

The conversion time, t_{conv}, is independent of the SCLK frequency. When operating the device at speeds lower than the maximum rated throughput, the conversion time, t_{conv}, does not change; the device spends more time in power-down state. Therefore, as shown in 图 68, the device power consumption from the AVDD supply and the external reference source is directly proportional to the speed of operation. Extremely low AVDD power-down current (50 nA, typical) and extremely low external reference leakage current (250 nA, typical), make this device ideal for very low throughput applications (such as pulsed measurements).

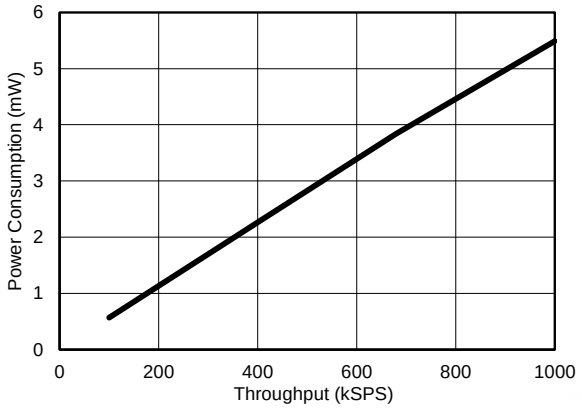

图 68. Power Scaling With Throughput

12 Layout

12.1 Layout Guidelines

图 69 shows a board layout example for the device. Appropriate layout that interconnects accompanying capacitors and converters with low inductance is critical for achieving optimum performance. Thus, a PCB board with at least four layers is recommended to keep all critical components on the top layer and interconnected to a solid (low inductance) analog ground plane at the subsequent inner layer using 15-mil vias. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in 图 69, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

As a result of dynamic currents during conversion and data transfer, each supply pin (AVDD and DVDD) must have a decoupling capacitor to keep the supply voltage stable. To maximize decoupling capabilities, inductance between each supply capacitor and the supply pin of the converter is kept less than 5 nH by placing the capacitor within 0.2-inches from the pin and connecting it with 20-mil traces and a 15-mil grounding via, as shown in 图 69. TI recommends using one 1-μF ceramic capacitor at each supply pin. Avoid placing vias between the supply pin and its decoupling capacitor.

Dynamic currents are also present at the REF pin during the conversion phase and very good decoupling is critical to achieve optimum performance. The inductance between the reference capacitor and the REF pin is kept less than 2 nH by placing the capacitor within 0.1-inches from the pin and connecting it with 20-mil traces and multiple 15-mil grounding vias, as shown in 图 69. A single, 10-μF, X7R-grade, 0805-size, ceramic capacitor with at least a 10-V rating is recommended for good performance over the rated temperature range. Avoid using additional lower value capacitors because the interactions between multiple capacitors may affect the ADC performance at higher sampling rates. A small, 0.1-Ω to 0.47-Ω, 0603-size resistor placed in series with the reference capacitor (as shown in 图 69) keeps the overall impedance low and constant, especially at very high frequencies.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

12.2 Layout Example

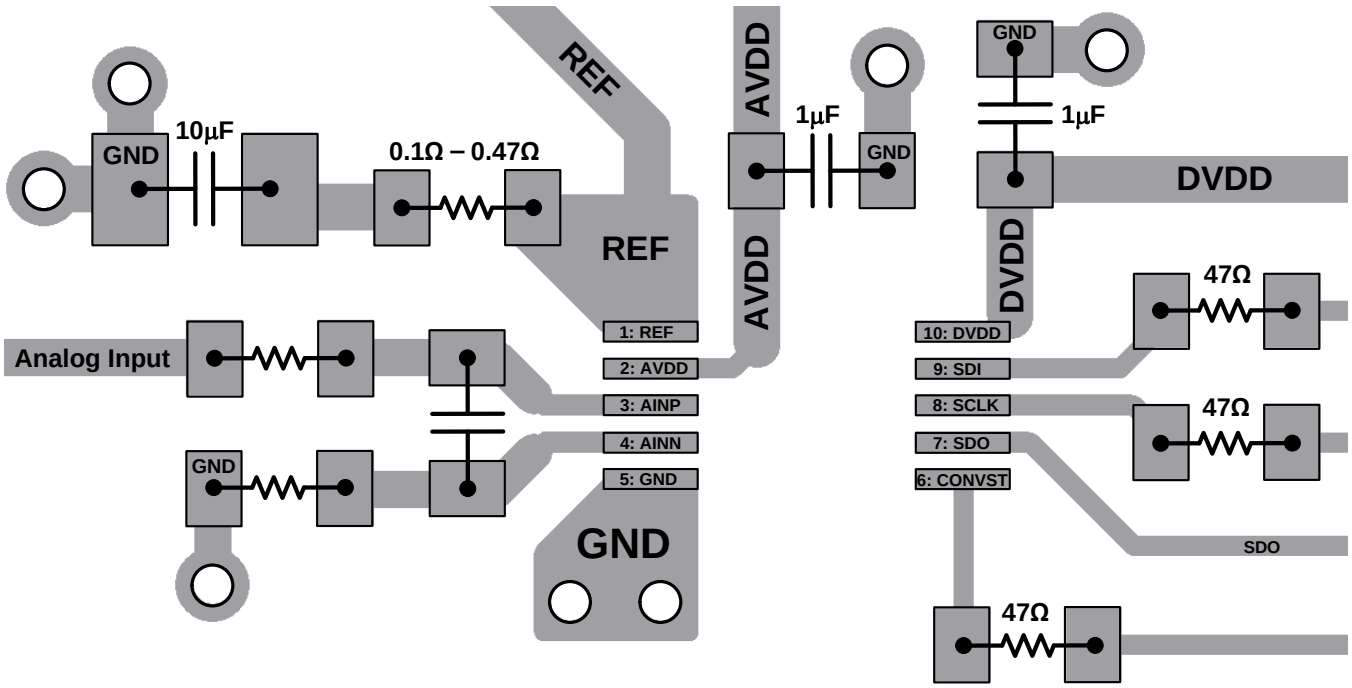

图 69. Recommended Layout

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《OPAx333 1.8V、微功耗 CMOS 运算放大器零漂移系列》数据表*
- 德州仪器 (TI)，*《THS452x 极低功耗、负轨输入、轨至轨输出、全差分放大器》数据表*
- 德州仪器 (TI)，*《THS4281 极低功耗、高速、轨至轨输入和输出电压反馈运算放大器》数据表*
- 德州仪器 (TI)，*《1MHz、微功耗、低噪声、RRIO、1.8V CMOS 运算放大器精密超值系列》数据表*
- 德州仪器 (TI)，*《OPAx350 高速单电源轨至轨运算放大器微型放大器系列》数据表*
- 德州仪器 (TI)，*《1.8V、7MHz、90dB CMRR、单电源轨至轨 I/O 运算放大器》数据表*
- 德州仪器 (TI)，*《经优化可实现 1µs 满标度步进响应的 16 位数据采集 (DAQ) 块》参考指南*
- 德州仪器 (TI)，*《经优化可实现最低功耗的 18 位、1MSPS 数据采集 (DAQ) 块》参考指南*
- 德州仪器 (TI)，*《经优化可实现超低功耗 (<1mW) 的 18 位、10kSPS 数据采集 (DAQ) 块》参考指南*
- 德州仪器 (TI)，*《经优化可实现最低失真和噪声的 18 位、1MSPS 数据采集块 (DAQ)》参考指南*
- 德州仪器 (TI)，*《超低功耗 18 位高精度 ECG 数据采集系统》参考指南*

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8860IDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8860	Samples
ADS8860IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8860	Samples
ADS8860IDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8860	Samples
ADS8860IDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8860	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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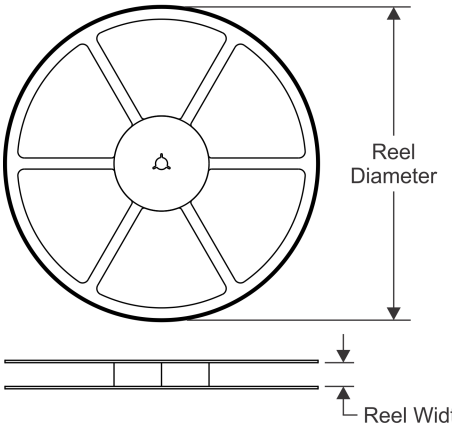
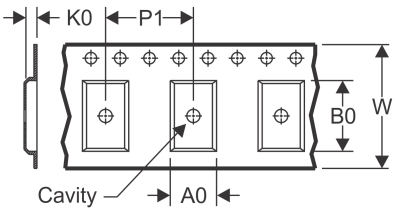
TAPE AND REEL INFORMATION

REEL DIMENSIONS

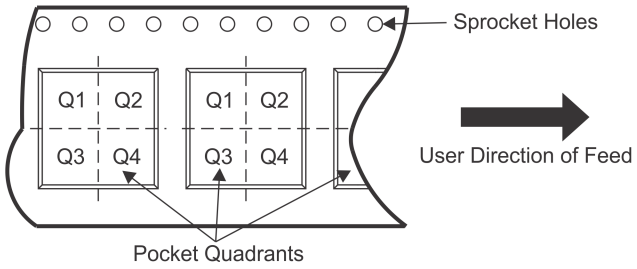


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

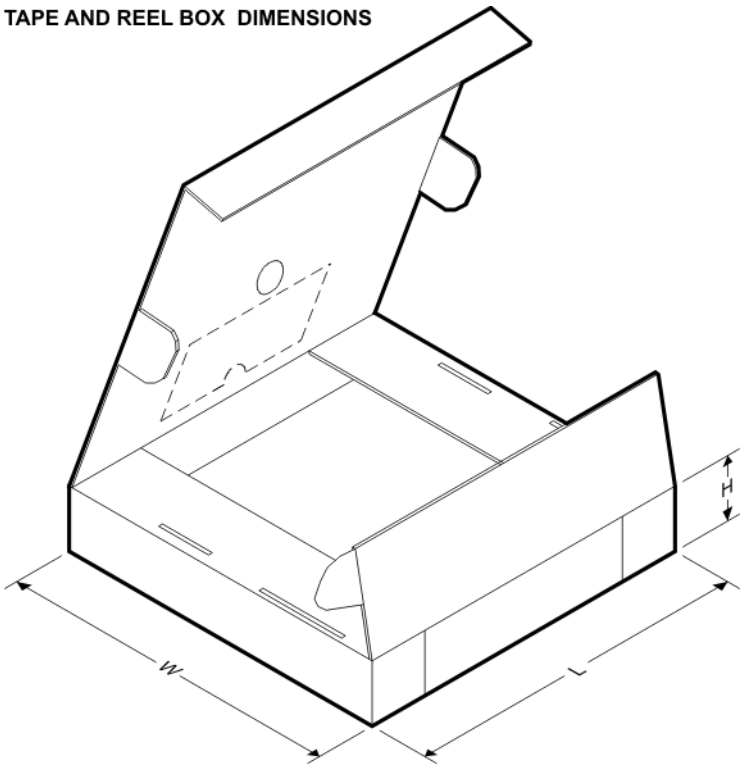
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8860IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8860IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8860IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

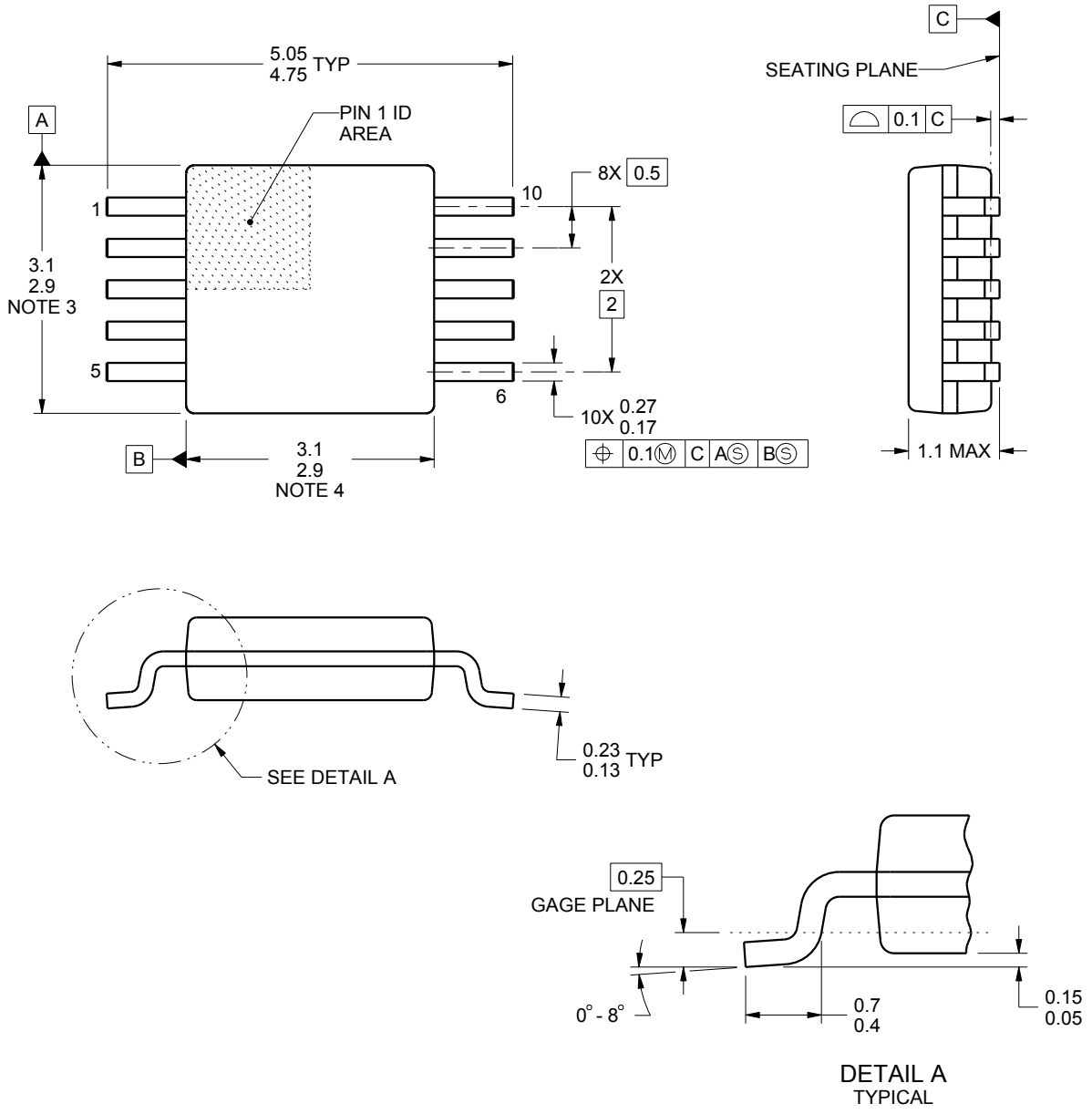
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8860IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8860IDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8860IDRCT	VSON	DRC	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

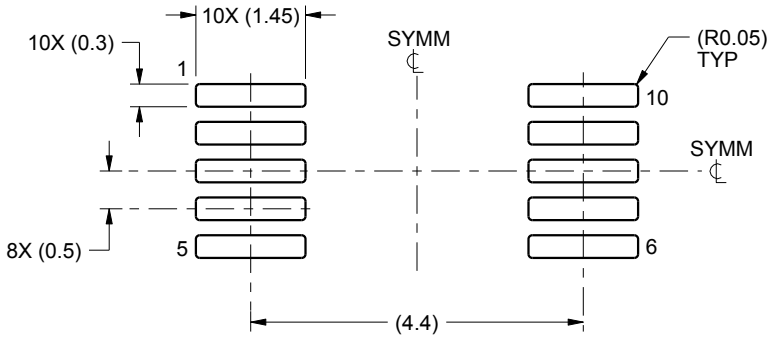
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

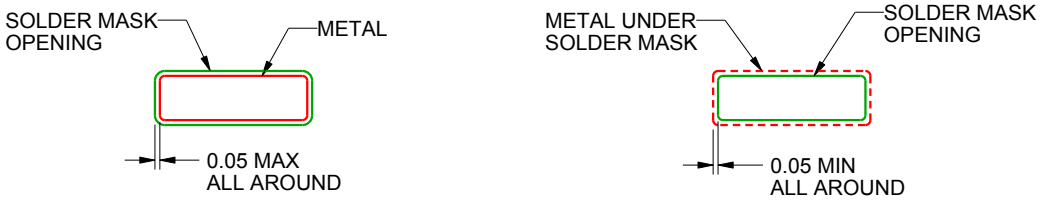


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

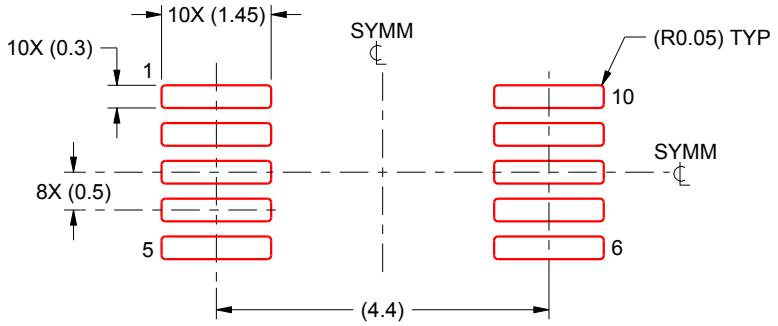


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

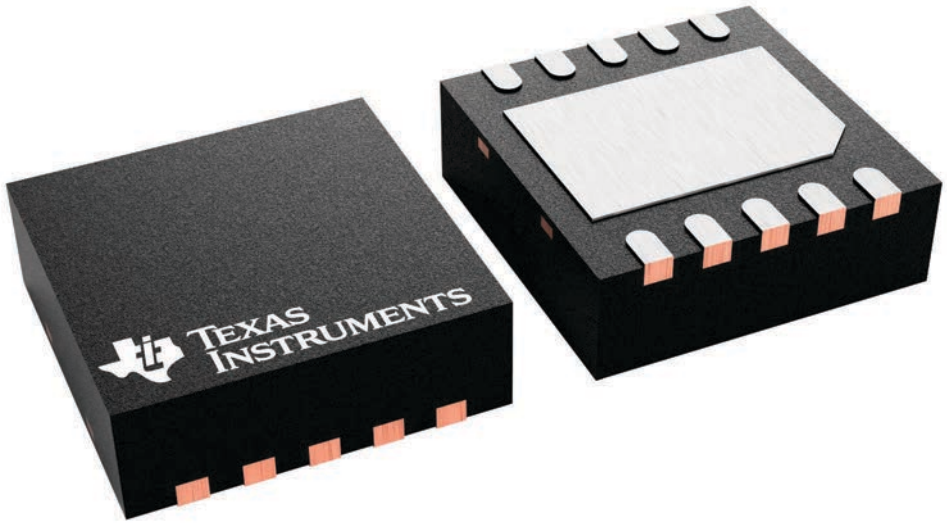
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



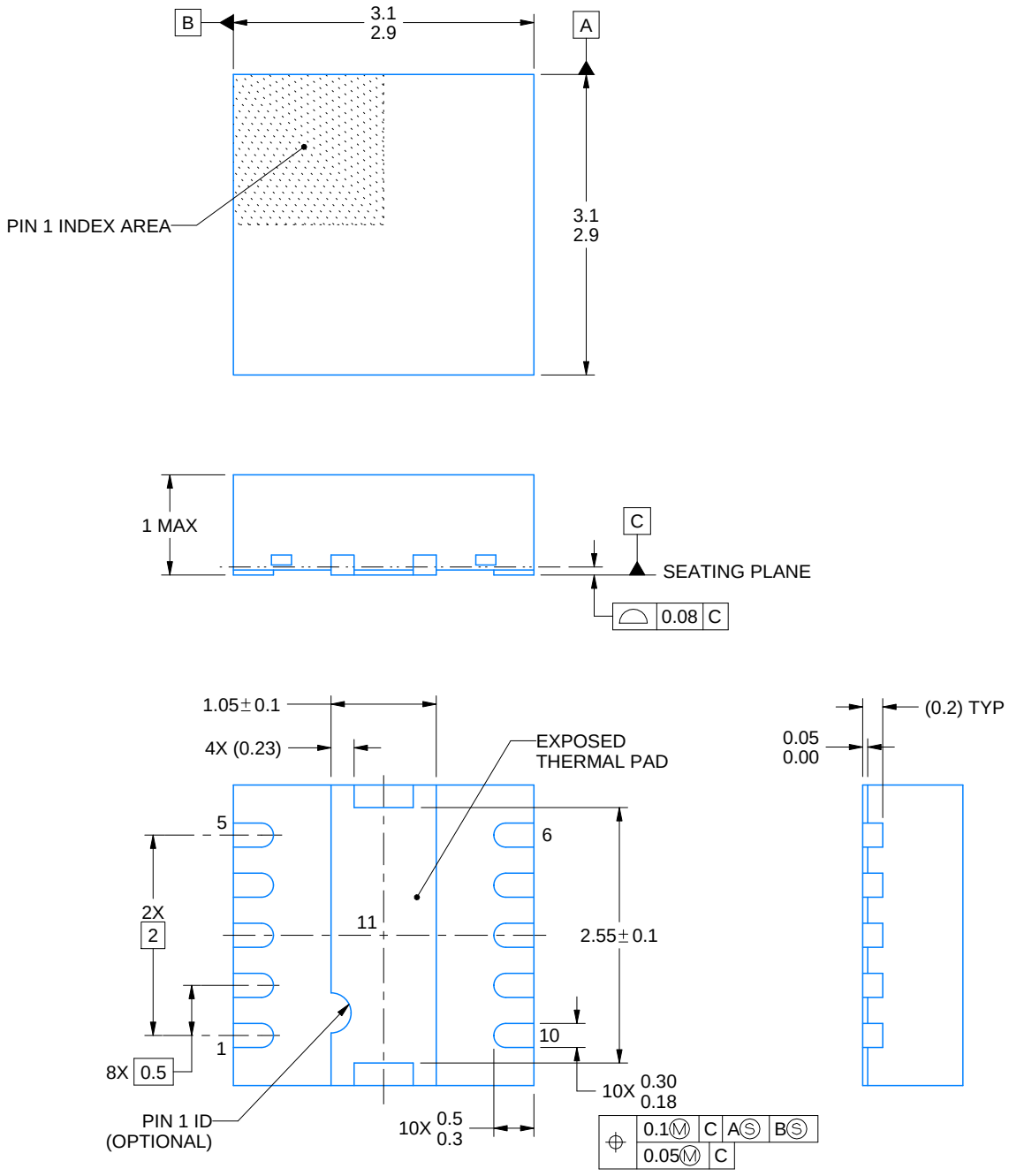
4226193/A

PACKAGE OUTLINE

DRC0010D

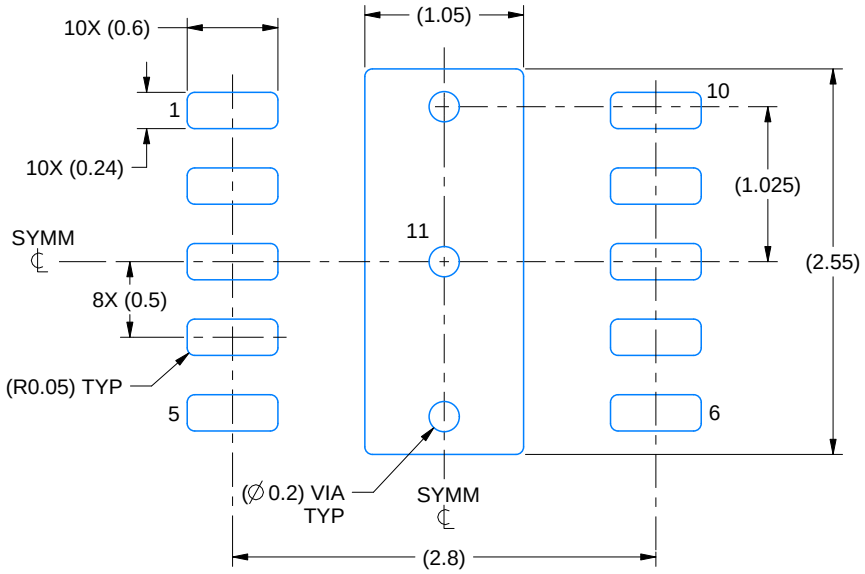
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

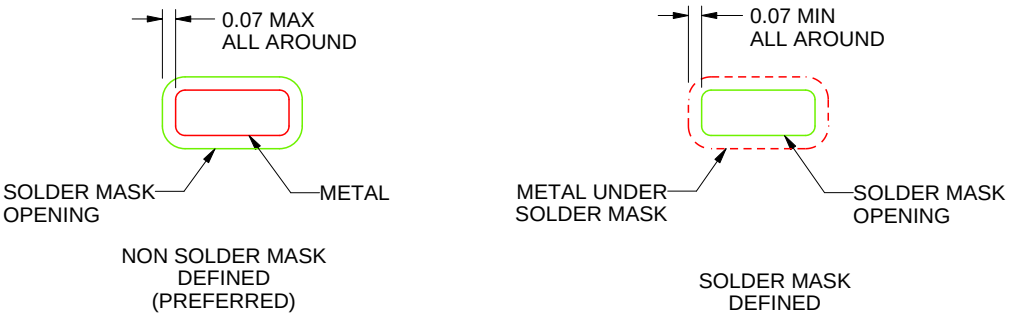


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

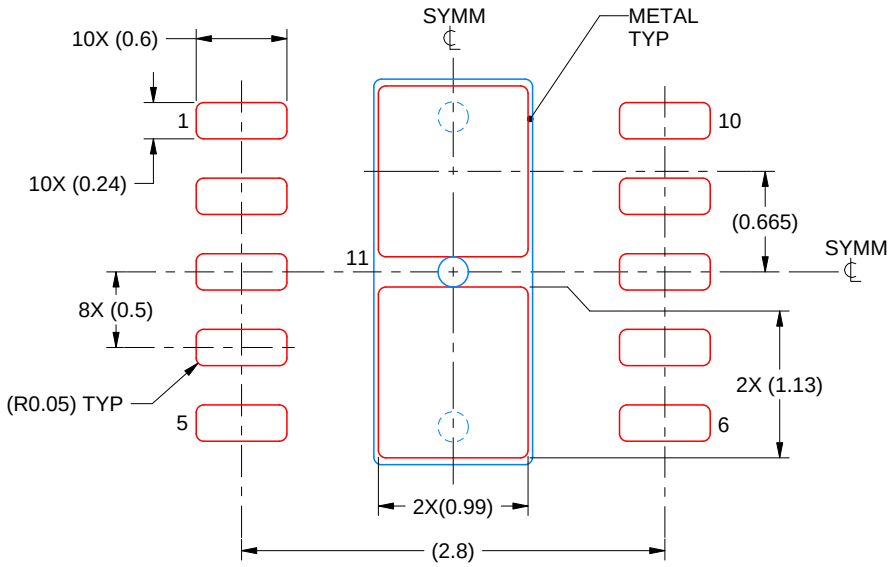


SOLDER MASK DETAILS

4218880/A 10/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4218880/A 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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