

Dual-Channel, 16-BIT, 1.25 GSPS Digital-to-Analog Converter (DAC)

Check for Samples: [DAC3482](#)

FEATURES

- **Very Low Power: 900 mW at 1.25 GSPS, Full Operating Conditions**
- **Multi-DAC Synchronization**
- **Selectable 2x, 4x, 8x, 16x Interpolation Filter**
 - **Stop-Band Attenuation > 90 dBc**
- **Flexible On-Chip Complex Mixing**
 - **Fine Mixer with 32-bit NCO**
 - **Power Saving Coarse Mixer: $\pm n \times F_s/8$**
- **High Performance, Low Jitter Clock Multiplying PLL**
- **Digital I and Q Correction**
 - **Gain, Phase, Offset, and Group Delay Correction**
- **Digital Inverse Sinc Filter**
- **Flexible LVDS Input Data Bus**
 - **Word- or Byte-Wide Interface**
 - **8 Sample Input FIFO**
 - **Data Pattern Checker**
 - **Parity Check**
- **Temperature Sensor**
- **Differential Scalable Output: 10mA to 30mA**
- **Multiple Package Options: 88-pin 9x9mm WQFN and 196-ball 12mmx12mm BGA (GREEN / Pb-Free)**

DESCRIPTION

The DAC3482 is a very low power, high dynamic range, dual-channel, 16-bit digital-to-analog converter (DAC) with a sample rate as high as 1.25 GSPS.

The device includes features that simplify the design of complex transmit architectures: 2x to 16x digital interpolation filters with over 90 dB of stop-band attenuation simplify the data interface and reconstruction filters. A complex mixer allows flexible carrier placement. A high-performance low jitter clock multiplier simplifies clocking of the device without significant impact on the dynamic range. The digital Quadrature Modulator Correction (QMC) enables complete IQ compensation for gain, offset, phase, and group delay between channels in direct up-conversion applications.

Digital data is input to the device through a flexible LVDS data bus with on-chip termination. Data can be input either word-wide or byte-wide. The device includes a FIFO, data pattern checker and parity test to ease the input interface. The interface also allows full synchronization of multiple devices.

The device is characterized for operation over the entire industrial temperature range of -40°C to 85°C and is available in a very-small 88-pin 9x9mm WQFN package.

The DAC3482 very low power, small size, superior crosstalk, high dynamic range and features are an ideal fit for today's communication systems.

APPLICATIONS

- **Cellular Base Stations**
- **Diversity Transmit**
- **Wideband Communications**

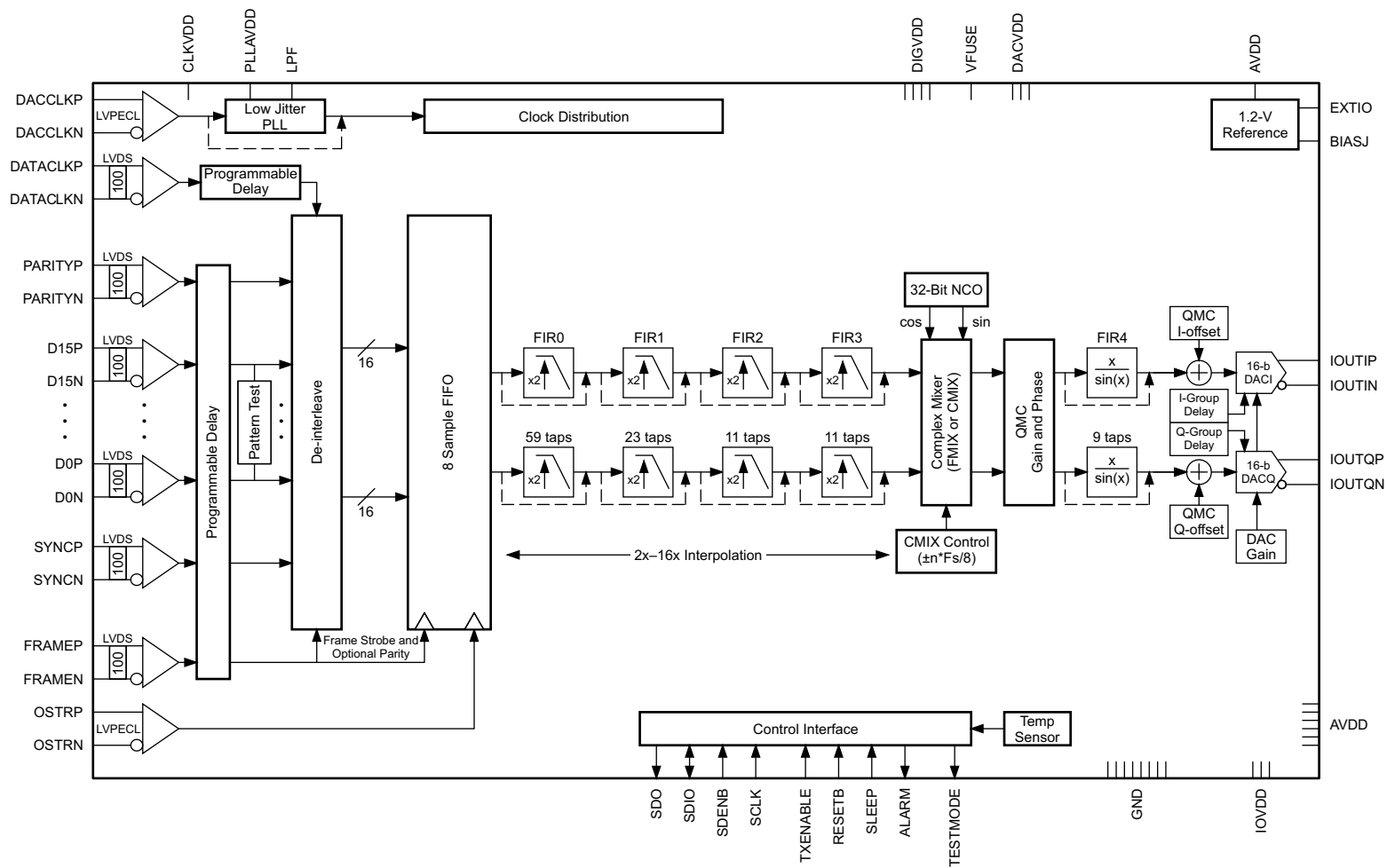


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

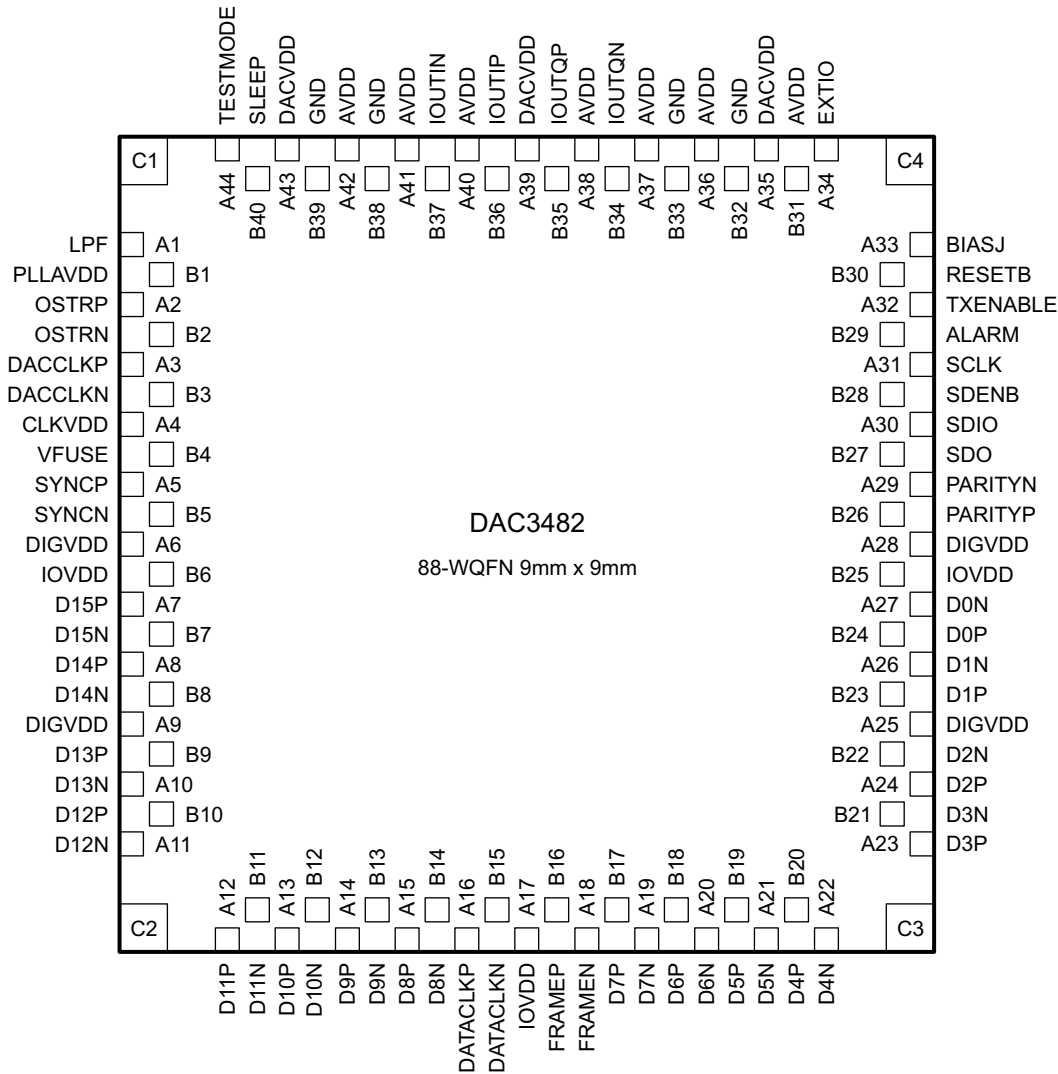
FUNCTIONAL BLOCK DIAGRAM



B0450-01

DEVICE INFORMATION

PINOUT RKD Package (Top View)



P0133-01

PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|--------|-----------------------------------|-----|--|
| NAME | NO. | | |
| AVDD | A36, A37, A38, A40, A41, A42, B31 | I | Analog supply voltage. (3.3 V) |
| ALARM | B29 | O | CMOS output for ALARM condition. The ALARM output functionality is defined through the config7 register. Default polarity is active high, but can be changed to active low via <i>config0 alarm_out_pol</i> control bit. |
| BIASJ | A33 | O | Full-scale output current bias. For 30mA full-scale output current, connect 1.28kΩ to ground. Change the full-scale output current through <i>coarse_dac(3:0)</i> in <i>config3, bit<15:12></i> |
| CLKVDD | A4 | I | Internal clock buffer supply voltage. (1.2 V) It is recommended to isolate this supply from DIGVDD and DACVDD. |

PIN FUNCTIONS (continued)

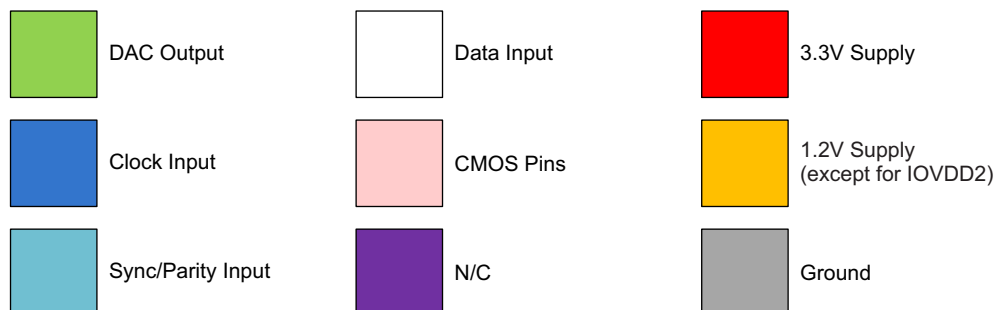
| PIN | | I/O | DESCRIPTION |
|-----------|--|-----|--|
| NAME | NO. | | |
| D[15..0]P | A7, A8, B9, B10, A12, A13, A14, A15, B17, B18, B19, B20, A23, A24, B23, B24 | I | <p>LVDS positive input data bits 0 through 15. Internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR) and can be transferred in either byte-wide or word-wide mode. In byte-wide mode the unused pins can be left unconnected.</p> <p>D15P is most significant data bit (MSB) in word-wide mode D7P is most significant data bit (MSB) in byte-wide mode D0P is least significant data bit (LSB)</p> <p>The order of the bus can be reversed via <i>config2 revbus</i> bit.</p> |
| D[15..0]N | B7, B8, A10, A11, B11, B12, B13, B14, A19, A20, A21, A22, B21, B22, A26, A27 | I | LVDS negative input data bits 0 through 15. (See D[15:0]P description above) |
| DACCLKP | A3 | I | Positive external LVPECL clock input for DAC core with a self-bias. |
| DACCLKN | B3 | I | Complementary external LVPECL clock input for DAC core. (see the DACCLKP description) |
| DACVDD | A35, A39, A43 | I | DAC core supply voltage. (1.2 V). It is recommended to isolate this supply from CLKVDD and DIGVDD. |
| DATACLKP | A16 | I | LVDS positive input data clock. Internal 100 Ω termination resistor. Input data D[15:0]P/N is latched on both edges of DATACLKP/N (Double Data Rate). |
| DATACLKN | B15 | I | LVDS negative input data clock. (See DATACLKP description) |
| DIGVDD | A6, A9, A25, A28 | I | Digital supply voltage. (1.2 V). It is recommended to isolate this supply from CLKVDD and DACVDD. |
| EXTIO | A34 | I/O | Used as external reference input when internal reference is disabled through <i>config27 extref_ena</i> = '1'. Used as internal reference output when <i>config27 extref_ena</i> = '0' (default). Requires a 0.1 μ F decoupling capacitor to AGND when used as reference output. |
| FRAMEP | B16 | I | LVDS frame indicator positive input. Internal 100 Ω termination resistor. The main functions of this input are to reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP/N. The signal captured by the falling edge of DATACLKP/N can be used as a block parity bit. The FRAMEP/N signal should be edge-aligned with D[15:0]P/N. |
| FRAMEN | A18 | I | LVDS frame indicator negative input. (See the FRAMEP description) |
| GND | C1, C2, C3, C4, B32, B33, B38, B39, Thermal Pad | I | These pins are ground for all supplies. |
| IOUTIP | B36 | O | I-Channel DAC current output. Connect directly to ground if unused. |
| IOUTIN | B37 | O | I-Channel DAC complementary current output. Connect directly to ground if unused. |
| IOUTQP | B35 | O | Q-Channel DAC current output. Connect directly to ground if unused. |
| IOUTQN | B34 | O | Q-Channel DAC complementary current output. Connect directly to ground if unused. |
| IOVDD | B6, A17, B25 | I | Supply voltage for all digital I/O. (3.3 V) |
| LPF | A1 | I/O | PLL loop filter connection. If not using the clock multiplying PLL, the LPF pin can be left unconnected. |
| OSTRP | A2 | I | LVPECL output strobe positive input. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used to sync the divided-down clocks and FIFO output pointer in Dual Sync Sources Mode. If unused it can be left unconnected. |
| OSTRN | B2 | I | LVPECL output strobe negative input. (See the OSTRP description) |
| PARITYP | B26 | I | Optional LVDS positive input parity bit. The PARITYP/N LVDS pair has an internal 100 Ω termination resistor. If unused it can be left unconnected. |
| PARITYN | A29 | I | Optional LVDS negative input parity bit. |
| PLLAVDD | B1 | I | PLL analog supply voltage. (3.3 V) |
| SCLK | A31 | I | Serial interface clock. Internal pull-down. |
| SDENB | B28 | I | Active low serial data enable, always an input to the DAC3482. Internal pull-up. |
| SDIO | A30 | I/O | Serial interface data. Bi-directional in 3-pin mode (default) and uni-directional in 4-pin mode. Internal pull-down. |

PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|----------|-----|-----|---|
| NAME | NO. | | |
| SDO | B27 | O | Uni-directional serial interface data in 4-pin mode. The SDO pin is tri-stated in 3-pin interface mode (default). |
| SLEEP | B40 | I | Active high asynchronous hardware power-down input. Internal pull-down. |
| SYNCP | A5 | I | Optional LVDS SYNC positive input. The SYNCP/N LVDS pair has an internal 100 Ω termination resistor. If unused it can be left unconnected. |
| SYNCN | B5 | I | Optional LVDS SYNC negative input. |
| RESETB | B30 | I | Active low input for chip RESET, which resets all the programming registers to their default state. Internal pull-up. |
| TXENABLE | A32 | I | Transmit enable active high input. Internal pull-down. To enable analog output data transmission, set <i>sif_txenable</i> in register <i>config3</i> to "1" or pull CMOS TXENABLE pin to high. To disable analog output, set <i>sif_txenable</i> to "0" and pull CMOS TXENABLE pin to low. The digital logic section is forced to all 0, and any input data is ignored. |
| TESTMODE | A44 | I | This pin is used for factory testing. Internal pull-down. Leave unconnected for normal operation. |
| VFUSE | B4 | I | Digital supply voltage. This supply pin is also used for factory fuse programming. Connect to DACVDD for normal operation. |

**ZAY Package
(Top View)**

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P |
|----|-----------|--------|----------|----------|----------|----------|-----------|---------|----------|----------|---------|-----|-----------|----------|
| 14 | GND | GND | GND | GND | IOOUT IN | IOOUT IP | GND | GND | IOOUT QP | IOOUT QN | GND | GND | GND | GND |
| 13 | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| 12 | DAC CLKP | GND | CLK VDD | LPF | GND | GND | EXTIO | BIASJ | GND | N/C | N/C | GND | ALARM | SDO |
| 11 | DAC CLKN | GND | PLL AVDD | PLL AVDD | AVDD | AVDD | AVDD | AVDD | AVDD | AVDD | N/C | GND | N/C | SDIO |
| 10 | GND | GND | GND | AVDD | DAC VDD | DAC VDD | DAC VDD | DAC VDD | DAC VDD | DAC VDD | AVDD | GND | RESET B | SDENB |
| 9 | OS TRP | OS TRN | GND | DAC VDD | DAC VDD | GND | GND | GND | GND | DAC VDD | DAC VDD | GND | TX ENABLE | SCLK |
| 8 | TEST MODE | SLEEP | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | N/C | N/C |
| 7 | N/C | N/C | GND | VFUSE | DIG VDD | GND | GND | GND | GND | DIG VDD | N/C | GND | N/C | N/C |
| 6 | N/C | N/C | GND | IO VDD | DIG VDD | GND | GND | GND | GND | DIG VDD | IO VDD | GND | N/C | N/C |
| 5 | SYNCP | SYNCPN | GND | IO VDD | DIG VDD | DIG VDD | IO VDD | IO VDD | DIG VDD | DIG VDD | IO VDD | GND | PARITY P | PARITY N |
| 4 | D15P | D15N | N/C | N/C | N/C | N/C | N/C | N/C | N/C | N/C | N/C | N/C | D0P | D0N |
| 3 | D14P | D14N | N/C | N/C | N/C | N/C | N/C | N/C | N/C | N/C | N/C | N/C | D1P | D1N |
| 2 | D13P | D13N | D11P | D10P | D9P | D8P | DATA CLKP | FRAME P | D7P | D6P | D5P | D4P | D2P | D2N |
| 1 | D12P | D12N | D11N | D10N | D9N | D8N | DATA CLKN | FRAME N | D7N | D6N | D5N | D4N | D3P | D3N |



P0134-02

PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|-----------|--|-----|--|
| NAME | NO. | | |
| AVDD | D10, E11, F11, G11, H11, J11, K11, L10 | I | Analog supply voltage. (3.3 V) |
| ALARM | N12 | O | CMOS output for ALARM condition. The ALARM output functionality is defined through the <i>config7</i> register. Default polarity is active low, but can be changed to active high via <i>config0 alarm_out_pol</i> control bit. |
| BIASJ | H12 | O | Full-scale output current bias. For 30mA full-scale output current, connect 1.28k Ω to ground. Change the full-scale output current through <i>coarse_dac(3:0)</i> in <i>config3, bit<15:12></i> |
| CLKVDD | C12 | I | Internal clock buffer supply voltage. (1.2 V) It is recommended to isolate this supply from DIGVDD and DACVDD. |
| D[15..0]P | N4, N3, N2, N1, M2, L2, K2, J2, F2, E2, D2, C2, A1, A2, A3, A4 | I | LVDS positive input data bits 0 through 15. Internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR). D15P is most significant data bit (MSB) D0P is least significant data bit (LSB) The order of the bus can be reversed via <i>config2 revbus</i> bit. |
| D[15..0]N | P4, P3, P2, P1, M1, L1, K1, J1, F1, E1, D1, C1, B1, B2, B3, B4 | I | LVDS negative input data bits 0 through 15. (See D[15:0]P description above) |
| DACCLKP | A12 | I | Positive external LVPECL clock input for DAC core with a self-bias. |
| DACCLKN | A11 | I | Complementary external LVPECL clock input for DAC core. (see the DACCLKP description) |
| DACVDD | D9, E9, E10, F10, G10, H10, J10, K9, K10, L9 | I | DAC core supply voltage. (1.2 V). It is recommended to isolate this supply from CLKVDD and DIGVDD. |
| DATACLKP | G2 | I | LVDS positive input data clock. Internal 100 Ω termination resistor. Input data D[15:0]P/N is latched on both edges of DATACLKP/N (Double Data Rate). |
| DATACLKN | G1 | I | LVDS negative input data clock. (See DATACLKP description) |
| DIGVDD | E5, E6, E7, F5, J5, K5, K6, K7 | I | Digital supply voltage. (1.2 V). It is recommended to isolate this supply from CLKVDD and DACVDD. |
| EXTIO | G12 | I/O | Used as external reference input when internal reference is disabled through <i>config27 extref_ena</i> = '1'. Used as internal reference output when <i>config27 extref_ena</i> = '0' (default). Requires a 0.1 μ F decoupling capacitor to AGND when used as reference output. |
| FRAMEP | H2 | I | LVDS frame indicator positive input. Internal 100 Ω termination resistor. The main functions of this input are to reset the FIFO pointer or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP/N. The signal captured by the falling edge of DATACLKP/N can be used as a block parity bit. The FRAMEP/N signal should be edge-aligned with D[15:0]P/N. Additionally it is used to indicate the beginning of the frame. |
| FRAMEN | H1 | I | LVDS frame indicator negative input. (See the FRAMEP description) |

PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|----------|---|-----|--|
| NAME | NO. | | |
| GND | A10, A13, A14, B10, B11, B12, B13, B14, C5, C6, C7, C8, C9, C10, C13, C14, D8, D13, D14, E8, E12, E13, F6, F7, F8, F9, F12, F13, G6, G7, G8, G9, G13, G14, H6, H7, H8, H9, H13, H14, J6, J7, J8, J9, J12, J13, K8, K13, L8, L13, L14, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, N13, N14, P13, P14 | I | These pins are ground for all supplies. |
| IOUTIP | F14 | O | I-Channel DAC current output. |
| IOUTIN | E14 | O | I-Channel DAC complementary current output. |
| IOUTQP | J14 | O | Q-Channel DAC current output. |
| IOUTQN | K14 | O | Q-Channel DAC complementary current output. |
| IOVDD | D5, D6, G5, H5, L5, L6 | I | Supply voltage for all digital I/O. (3.3 V) |
| LPF | D12 | I | PLL loop filter connection. If not using the clock multiplying PLL, the LPF pin can be left unconnected. |
| OSTRP | A9 | I | LVPECL output strobe positive input. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used for multiple DAC synchronization. If unused it can be left unconnected. |
| OSTRN | B9 | I | LVPECL output strobe negative input. (See the OSTRP description) |
| PARITYP | N5 | I | Optional LVDS positive input parity bit. The PARITYP/N LVDS pair has an internal 100 Ω termination resistor. If unused it can be left unconnected. |
| PARITYN | P5 | I | Optional LVDS negative input parity bit. |
| PLLAVDD | C11, D11 | I | PLL analog supply voltage. (3.3 V) |
| SCLK | P9 | I | Serial interface clock. Internal pull-down. |
| SDENB | P10 | I | Active low serial data enable, always an input to the DAC3482. Internal pull-up. |
| SDIO | P11 | I/O | Serial interface data. Bi-directional in 3-pin mode (default) and 4-pin mode. Internal pull-down. |
| SDO | P12 | O | Uni-directional serial interface data in 4-pin mode. The SDO pin is three-stated in 3-pin interface mode (default). |
| SLEEP | B8 | I | Active high asynchronous hardware power-down input. Internal pull-down. |
| SYNCP | A5 | I | Optional LVDS SYNC positive input. The SYNCP/N LVDS pair has an internal 100 Ω termination resistor. If unused it can be left unconnected. |
| SYNCN | B5 | I | LVDS SYNC negative input. |
| RESETB | N10 | I | Active low input for chip RESET, which resets all the programming registers to their default state. Internal pull-up. |
| TXENABLE | N9 | I | Transmit enable active high input. Internal pull-down. To enable analog output data transmission, set <i>sif_txenable</i> in register <i>config3</i> to "1" or pull CMOS TXENABLE pin to high. To disable analog output, set <i>sif_txenable</i> to "0" and pull CMOS TXENABLE pin to low. The DAC output is forced to midscale. |
| TESTMODE | A8 | O | This pin is used for factory testing. Internal pull-down. Leave unconnected for normal operation. |
| VFUSE | D7 | I | Digital supply voltage. This supply pin is also used for factory fuse programming. Connect to DACVDD for normal operation. |

ORDERING INFORMATION⁽¹⁾

| T _A | ORDER CODE | PACKAGE DRAWING/TYPE ⁽²⁾⁽³⁾ | TRANSPORT MEDIA | QUANTITY |
|----------------|--------------|--|-----------------|----------|
| –40°C to 85°C | DAC3482IRKDT | RKD, 88 WQFN Quad Flatpack No-Lead | Tape and Reel | 250 |
| | DAC3482IRKDR | | | 2000 |
| | DAC3482IZAY | ZAY, 196 NFBGA | | 160 |
| | DAC3482IZAYR | | | 1000 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Thermal Pad Size: 6.4 mm x 6.4 mm
(3) MSL Peak Temperature: Level-3-260C-168 HR

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE | | UNIT |
|--|--|-------|---------------|------|
| | | MIN | MAX | |
| Supply voltage range ⁽²⁾ | DACVDD, DIGVDD, CLKVDD | –0.5 | 1.5 | V |
| | VFUSE | –0.5 | 1.5 | V |
| | IOVDD | –0.5 | 4 | V |
| | AVDD, PLLAVDD | –0.5 | 4 | V |
| Pin voltage range ⁽²⁾ | D[15..0]P/N, DATACLKP/N, FRAMEP/N, PARITYP/N, SYNCNCP/N | –0.5 | IOVDD + 0.5 | V |
| | DACCLKP/N, OSTRP/N | –0.5 | CLKVDD + 0.5 | V |
| | ALARM, SDO, SDIO, SCLK, SDENB, SLEEP, RESETB, TESTMODE, TXENABLE | –0.5 | IOVDD + 0.5 | V |
| | IOUTIP/N, IOUTQP/N | –1.0 | AVDD + 0.5 | V |
| | EXTIO, BIASJ | –0.5 | AVDD + 0.5 | V |
| | LPF | 0.5 | PLLA VDD+0.5V | V |
| Peak input current (any input) | | | 20 | mA |
| Peak total input current (all inputs) | | | –30 | mA |
| Operating free-air temperature range, T _A : DAC3482 | | –40 | 85 | °C |
| Absolute maximum junction temperature, T _J | | | 150 | °C |
| Storage temperature range | | –65 | 150 | °C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | DAC3482 | | UNITS |
|-------------------------------|---|-------------|-------------|-------|
| | | RKD PACKAGE | ZAY PACKAGE | |
| | | (88) PINS | (196) BALL | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 22.1 | 37.6 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 7.1 | 6.8 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance ⁽⁴⁾ | 0.6 | N/A | |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁵⁾ | 4.7 | 16.8 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁶⁾ | 0.1 | 0.2 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁷⁾ | 4.6 | 16.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(6) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-------|---|-----|-----|-----|------|
| T_J | Recommended operating junction temperature | | | 105 | °C |
| | Maximum rated operating junction temperature ⁽¹⁾ | 125 | | | |
| T_A | Recommended free-air temperature | –40 | 25 | 85 | °C |

(1) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

ELECTRICAL CHARACTERISTICS – DC SPECIFICATIONS⁽¹⁾

over recommended operating free-air temperature range, nominal supplies, $I_{OUT_{FS}} = 20\text{mA}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|---|--------|-----|------|--------|
| Resolution | | | 16 | | | Bits |
| DC ACCURACY | | | | | | |
| DNL | Differential nonlinearity | 1 LSB = IOUT _{FS} /2 ¹⁶ | ±2 | | | LSB |
| INL | Integral nonlinearity | | ±4 | | | LSB |
| ANALOG OUTPUT | | | | | | |
| | Coarse gain linearity | | ±0.04 | | | LSB |
| | Offset error | Mid code offset | ±0.001 | | | %FSR |
| | Gain error | With external reference | ±2 | | | %FSR |
| | | With internal reference | ±2 | | | %FSR |
| | Gain mismatch | With internal reference | ±2 | | | %FSR |
| | Full scale output current | | 10 | 20 | 30 | mA |
| | Output compliance range | | −0.5 | | 0.6 | V |
| | Output resistance | | 300 | | | kΩ |
| | Output capacitance | | 5 | | | pF |
| REFERENCE OUTPUT | | | | | | |
| V _{REF} | Reference output voltage | | 1.2 | | | V |
| | Reference output current ⁽²⁾ | | 100 | | | nA |
| REFERENCE INPUT | | | | | | |
| V _{EXTIO} | Input voltage range | External Reference Mode | 0.6 | 1.2 | 1.25 | V |
| | Input resistance | | 1 | | | MΩ |
| | Small signal bandwidth | | 472 | | | kHz |
| | Input capacitance | | 100 | | | pF |
| TEMPERATURE COEFFICIENTS | | | | | | |
| | Offset drift | | ±1 | | | ppm/°C |
| | Gain drift | With external reference | ±15 | | | ppm/°C |
| | | With internal reference | ±30 | | | ppm/°C |
| | Reference voltage drift | | ±8 | | | ppm/°C |

(1) Measured differentially across IOU_{TP}/N with 25 Ω each to GND.

(2) Use an external buffer amplifier with high impedance input to drive any external load.

ELECTRICAL CHARACTERISTICS – DC SPECIFICATIONS⁽¹⁾ (continued)

over recommended operating free-air temperature range, nominal supplies, $I_{OUT_{FS}} = 20\text{mA}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--------------------------------------|--|------|------|------|--------|
| POWER SUPPLY ⁽³⁾ | | | | | | |
| AVDD, IOVDD, PLLAVDD | | All conditions | 3.14 | 3.3 | 3.46 | V |
| DIGVDD | | All conditions | 1.14 | 1.2 | 1.32 | |
| CLKVDD, DACVDD ⁽⁴⁾ | | F _{DAC} Sample Rate ≤ 1.25GSPS, PLL OFF | 1.14 | 1.2 | 1.32 | V |
| | | F _{DAC} Sample Rate ≤ 1GSPS, PLL ON | 1.14 | 1.2 | 1.32 | |
| | | F _{DAC} Sample Rate ≥ 1GSPS, PLL ON | 1.25 | 1.29 | 1.32 | |
| PSRR | Power supply rejection ratio | DC tested | ±0.2 | | | %FSR/V |
| POWER CONSUMPTION | | | | | | |
| I _(AVDD) | Analog supply current ⁽⁵⁾ | MODE 1 f _{DAC} = 1.25GSPS, 2x interpolation, Mixer on, QMC on, invsinc on, PLL enabled, 20mA FS output, IF = 200MHz | 80 | 85 | mA | |
| I _(DIGVDD) | Digital supply current | | 390 | 450 | mA | |
| I _(DACVDD) | DAC supply current | | 30 | 50 | mA | |
| I _(CLKVDD) | Clock supply current | | 95 | 110 | mA | |
| P | Power dissipation | | 882 | 980 | mW | |
| I _(AVDD) | Analog supply current ⁽⁵⁾ | MODE 2 f _{DAC} = 1.25GSPS, 2x interpolation, Mixer on, QMC on, invsinc on, PLL disabled, 20mA FS output, IF = 200MHz | 65 | | mA | |
| I _(DIGVDD) | Digital supply current | | 385 | | mA | |
| I _(DACVDD) | DAC supply current | | 30 | | mA | |
| I _(CLKVDD) | Clock supply current | | 70 | | mA | |
| P | Power dissipation | | 800 | | mW | |
| I _(AVDD) | Analog supply current ⁽⁵⁾ | MODE 3 f _{DAC} = 625MSPS, 2x interpolation, Mixer on, QMC on, invsinc off, PLL disabled, 20mA FS output, IF = 200MHz | 65 | | mA | |
| I _(DIGVDD) | Digital supply current | | 190 | | mA | |
| I _(DACVDD) | DAC supply current | | 15 | | mA | |
| I _(CLKVDD) | Clock supply current | | 45 | | mA | |
| P | Power dissipation | | 515 | | mW | |
| I _(AVDD) | Analog supply current ⁽⁵⁾ | MODE 4 f _{DAC} = 1.25GSPS, 2x interpolation, Mixer on, QMC on, invsinc on, PLL enabled, I/Q output sleep, IF = 200MHz, | 35 | | mA | |
| I _(DIGVDD) | Digital supply current | | 395 | | mA | |
| I _(DACVDD) | DAC supply current | | 30 | | mA | |
| I _(CLKVDD) | Clock supply current | | 95 | | mA | |
| P | Power dissipation | | 740 | | mW | |
| I _(AVDD) | Analog supply current ⁽⁵⁾ | Mode 5 Power-Down mode: No clock, DAC on sleep mode (clock receiver sleep), I/Q output sleep, static data pattern | 20 | | mA | |
| I _(DIGVDD) | Digital supply current | | 10 | | mA | |
| I _(DACVDD) | DAC supply current | | 4 | | mA | |
| I _(CLKVDD) | Clock supply current | | 10 | | mA | |
| P | Power dissipation | | 95 | | mW | |
| I _(AVDD) | Analog supply current ⁽⁴⁾ | Mode 6 f _{DAC} = 1GSPS, 2x interpolation, Mixer off, QMC off, invsinc off, PLL enabled, 20mA FS output, IF = 200MHz | 80 | | mA | |
| I _(DIGVDD) | Digital supply current | | 200 | | mA | |
| I _(DACVDD) | DAC supply current | | 25 | | mA | |
| I _(CLKVDD) | Clock supply current | | 85 | | mA | |
| P | Power dissipation | | 636 | | mW | |

(3) To ensure power supply accuracy and to account for power supply filter network loss at operating conditions, the use of the ATEST function in register config27 to check the internal power supply nodes is recommended.

(4) Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details.

(5) Includes AVDD, PLLAVDD, and IOVDD.

ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|---|--|------------------------------------|-----|-----|------|----|
| LVDS INPUTS: D[15:0]P/N, DATACLKP/N, FRAMEP/N, SYNCN/P/N, PARITYP/N ⁽¹⁾ | | | | | | | |
| V _{A,B+} | Logic high differential input voltage threshold | | 200 | | | mV | |
| V _{A,B–} | Logic low differential input voltage threshold | | –200 | | | mV | |
| V _{COM} | Input common mode | | 1.0 | 1.2 | 1.6 | V | |
| Z _T | Internal termination | | 85 | 110 | 135 | Ω | |
| C _L | LVDS Input capacitance | | 2 | | | pF | |
| f _{INTERL} | Interleaved LVDS data transfer rate | | 1250 | | | MSPS | |
| f _{DATA} | Input data rate | Word-wide interface mode | 625 | | | MSPS | |
| | | Byte-wide interface mode | 312.5 | | | | |
| CLOCK INPUT (DACCLKP/N) | | | | | | | |
| | Duty cycle | | 40% | | 60% | | |
| | Differential voltage ⁽²⁾ | DACCLKP - DACCLKN | 0.4 | 0.8 | | V | |
| | Internally biased common-mode voltage | | 0.2 | | | V | |
| | Single-ended swing level | | –0.4 | | | V | |
| | DACCLKP/N input frequency | | 1250 | | | MHz | |
| OUTPUT STROBE (OSTRP/N) | | | | | | | |
| f _{OSTR} | Frequency | f _{OSTR} = f _{DACCLK} / (n x 8 x Interp) where n is any positive integer, f _{DACCLK} is DACCLK frequency in MHz | f _{DACCLK} / (8 x interp) | | | MHz | |
| | Duty cycle | | 50% | | | | |
| | Differential voltage | OSTRP – OSTRN | 0.4 | 0.8 | | V | |
| | Internally biased common-mode voltage | | 0.2 | | | V | |
| | Single-ended swing level | | –0.4 | | | V | |
| CMOS INTERFACE: ALARM, SDO, SDIO, SCLK, SDENB, SLEEP, RESETB, TXENABLE | | | | | | | |
| V _{IH} | High-level input voltage | | 2 | | | V | |
| V _{IL} | Low-level input voltage | | 0.8 | | | V | |
| I _{IH} | High-level input current | | –40 | | | 40 | μA |
| I _{IL} | Low-level input current | | –40 | | | 40 | μA |
| C _I | CMOS input capacitance | | 2 | | | pF | |
| V _{OH} | ALARM, SDO, SDIO | I _{load} = –100 μA | IOVDD – 0.2 | | | V | |
| | | I _{load} = –2 mA | 0.8 x IOVDD | | | V | |
| V _{OL} | ALARM, SDO, SDIO | I _{load} = 100 μA | 0.2 | | | V | |
| | | I _{load} = 2 mA | 0.5 | | | V | |

(1) See LVDS INPUTS section for terminology.

(2) Standard high swing LVPECL clock signal should be applied for best performance.

ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|--------|------------------|------|
| DIGITAL INPUT TIMING SPECIFICATIONS | | | | | |
| Timing LVDS inputs: D[15:0]P/N, FRAMEP/N, SYNCN/P, PARITYP/N, <i>double edge latching</i> | | | | | |
| $t_{s(DATA)}$ | Setup time, D[15:0]P/N, FRAMEP/N, SYNCN/P and PARITYP/N, valid to either edge of DATACLKP/N | Config36 Setting | | ps | |
| | | datadly | clkdly | | |
| | | 0 | 0 | | |
| | | 0 | 1 | | |
| | | 0 | 2 | | |
| | | 0 | 3 | | |
| | | 0 | 4 | | |
| | | 0 | 5 | | |
| | | 0 | 6 | | |
| | | 0 | 7 | | |
| | | 1 | 0 | | |
| | | 2 | 0 | | |
| | | 3 | 0 | | |
| | | 4 | 0 | | |
| | | 5 | 0 | | |
| | | 6 | 0 | | |
| | | 7 | 0 | | |
| $t_{h(DATA)}$ | Hold time, D[15:0]P/N, FRAMEP/N, SYNCN/P and PARITYP/N, valid after either edge of DATACLKP/N | Config36 Setting | | ps | |
| | | datadly | clkdly | | |
| | | 0 | 0 | | |
| | | 0 | 1 | | |
| | | 0 | 2 | | |
| | | 0 | 3 | | |
| | | 0 | 4 | | |
| | | 0 | 5 | | |
| | | 0 | 6 | | |
| | | 0 | 7 | | |
| | | 1 | 0 | | |
| | | 2 | 0 | | |
| | | 3 | 0 | | |
| | | 4 | 0 | | |
| | | 5 | 0 | | |
| | | 6 | 0 | | |
| | | 7 | 0 | | |
| $t_{(FRAME_SYNC)}$ | FRAMEP/N and SYNCN/P pulse width | $f_{DATACLK}$ is DATACLK frequency in MHz | | $1/2f_{DATACLK}$ | ns |

ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|-----|-----|------|
| TIMING OUTPUT STROBE INPUT: DACCLKP/N rising edge LATCHING ⁽³⁾ | | | | | |
| $t_{s(OSTR)}$ | Setup time, OSTRP/N valid to rising edge of DACCLKP/N | 0 | | | ps |
| $t_{h(OSTR)}$ | Hold time, OSTRP/N valid after rising edge of DACCLKP/N | 300 | | | ps |
| TIMING SYNC INPUT: DACCLKP/N rising edge LATCHING ⁽⁴⁾ | | | | | |
| $t_{s(SYNC_PLL)}$ | Setup time, SYNC/N valid to rising edge of DACCLKP/N | | 200 | | ps |
| $t_{h(SYNC_PLL)}$ | Hold time, SYNC/N valid after rising edge of DACCLKP/N | | 300 | | ps |
| TIMING SERIAL PORT | | | | | |
| $t_{s(SDENB)}$ | Setup time, SDENB to rising edge of SCLK | 20 | | | ns |
| $t_{s(SDIO)}$ | Setup time, SDIO valid to rising edge of SCLK | 10 | | | ns |
| $t_{h(SDIO)}$ | Hold time, SDIO valid to rising edge of SCLK | 5 | | | ns |
| $t_{(SCLK)}$ | Period of SCLK | Register <i>config6</i> read (temperature sensor read) | | 1 | μs |
| | | All other registers | | 100 | ns |
| $t_{d(Data)}$ | Data output delay after falling edge of SCLK | | 10 | | ns |
| t_{RESET} | Minimum RESETB pulse width | | 25 | | ns |

- (3) OSTR is required in Dual Sync Sources mode. In order to minimize the skew it is recommended to use the same clock distribution device such as Texas Instruments CDCE62005 to provide the DACCLK and OSTR signals to all the DAC3482 devices in the system. Swap the polarity of the DACCLK outputs with respect to the OSTR ones to establish proper phase relationship.
- (4) SYNC is required to synchronize the PLL circuit in multiple devices. The SYNC signal must meet the timing relationship with respect to the reference clock (DACCLKP/N) of the on-chip PLL circuit.

ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS

over recommended operating free-air temperature range, nominal supplies, $I_{OUT_{FS}} = 20\text{mA}$ (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS / COMMENTS | | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|--|----|------|-----|------------------|------|
| ANALOG OUTPUT ⁽¹⁾ | | | | | | | | |
| f _{DAC} | Maximum DAC rate ⁽²⁾ | PLL OFF | | | 1250 | | MSPS | |
| | | PLL ON - devices without enhanced test coverage | | | 1000 | | | |
| | | PLL ON - devices with enhanced test coverage | | | 1250 | | | |
| t _{s(DAC)} | Output settling time to 0.1% | Transition: Code 0x0000 to 0xFFFF | | | 10 | | ns | |
| t _{pd} | Output propagation delay | DAC outputs are updated on the falling edge of DAC clock. Does not include Digital Latency (see below). | | | 2 | | ns | |
| t _{r(IOUT)} | Output rise time 10% to 90% | | | | 220 | | ps | |
| t _{f(IOUT)} | Output fall time 90% to 10% | | | | 220 | | ps | |
| Digital latency | | 8-bit interface | No interpolation, FIFO enabled, Mixer off, QMC off, Inverse sinc off | | 250 | | DAC clock cycles | |
| | | | 2x Interpolation | | 212 | | | |
| | | | 4x Interpolation | | 372 | | | |
| | | | 8x Interpolation | | 723 | | | |
| | | | 16x Interpolation | | 1440 | | | |
| | | 16-bit interface | No interpolation, FIFO enabled, Mixer off, QMC off, Inverse sinc off | | 140 | | | |
| | | | 2x Interpolation | | 228 | | | |
| | | | 4x Interpolation | | 417 | | | |
| | | | 8x Interpolation | | 817 | | | |
| | | | 16x Interpolation | | 1630 | | | |
| | | Fine mixer | | 24 | | | | |
| | | QMC | | 32 | | | | |
| | | Inverse sinc | | 36 | | | | |
| Power-up Time | DAC wake-up time | IOUT current settling to 1% of IOUT _{FS} from output sleep | | | 2 | | μs | |
| | DAC sleep time | IOUT current settling to less than 1% of IOUT _{FS} in output sleep | | | 2 | | | |
| AC PERFORMANCE ⁽³⁾ | | | | | | | | |
| SFDR | Spurious free dynamic range (0 to f _{DAC} /2) tone at 0 dBFS | f _{DAC} = 1.25 GSPS, f _{OUT} = 20 MHz | | | 82 | | dBc | |
| | | f _{DAC} = 1.25 GSPS, f _{OUT} = 50 MHz | | | 77 | | | |
| | | f _{DAC} = 1.25 GSPS, f _{OUT} = 70 MHz | | | 72 | | | |
| IMD3 | Third-order two-tone intermodulation distortion Each tone at –12 dBFS | f _{DAC} = 1.25 MSPS, f _{OUT} = 30 ± 0.5 MHz | | | 81 | | dBc | |
| | | f _{DAC} = 1.25 GSPS, f _{OUT} = 50 ± 0.5 MHz | | | 79 | | | |
| | | f _{DAC} = 1.25 GSPS, f _{OUT} = 100 ± 0.5 MHz | | | 77.5 | | | |
| NSD | Noise spectral density Tone at 0dBFS | f _{DAC} = 1.25 GSPS, f _{OUT} = 10 MHz | | | 160 | | dBc/Hz | |
| | | f _{DAC} = 1.25 GSPS, f _{OUT} = 80 MHz | | | 155 | | | |
| ACLR ⁽⁴⁾ | Adjacent channel leakage ratio, single carrier | f _{DAC} = 1.2288 GSPS, f _{OUT} = 30.72 MHz | | | 77 | | dBc | |
| | | f _{DAC} = 1.2288 GSPS, f _{OUT} = 153.6 MHz | | | 74 | | | |
| | Alternate channel leakage ratio, single carrier | f _{DAC} = 1.2288 GSPS, f _{OUT} = 30.72 MHz | | | 82 | | | |
| | | f _{DAC} = 1.2288 GSPS, f _{OUT} = 153.6 MHz | | | 80 | | | |
| | Channel isolation | f _{DAC} = 1.25 GSPS, f _{OUT} = 10 MHz | | | 84 | | dBc | |

(1) Measured single ended into 50 Ω load.

(2) Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details.

(3) 4:1 transformer output termination, 50 Ω doubly terminated load.

(4) Single carrier, W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF, PAR = 12dB. TESTMODEL 1, 10 ms

ELECTRICAL CHARACTERISTICS - PHASE-LOCKED LOOP SPECIFICATIONS

over operating free-air temperature range (unless otherwise noted)

| pll_vco(5:0) in CONFIG26 BINARY VALUE / DECIMAL VALUE | ON-CHIP VCO RANGE | | |
|--|--------------------|------|------|
| | MIN | MAX | UNIT |
| b111111 / 63 | 3900 | 4000 | MHz |
| b111010 / 58 | 3850 | 3950 | MHz |
| b110110 / 54 | 3800 | 3900 | MHz |
| b110010 / 50 | 3770 | 3840 | MHz |
| b101110 / 46 | 3730 | 3790 | MHz |
| b101010 / 42 | 3690 | 3750 | MHz |
| b100110 / 38 | 3650 | 3700 | MHz |
| b100010 / 34 | 3600 | 3650 | MHz |
| b011110 / 30 | 3580 | 3600 | MHz |
| b010111 / 23 | Tested at 3500 MHz | | |

Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification

In 2013, TI has enhanced production test coverage for the on-chip phase-locked loop. The purpose of the production test coverage enhancement is to increase the DAC operating speed and allow the phase-locked loop to stay locked throughout the recommended range over the operating free-air temperature specification using only one pll_vco(5:0) setting instead of possible adjustments over temperature. This new specification reduces alarm checking and pll_vco(5:0) adjustment overhead if the phase-locked loop is used in the end application.

The tested devices will have updated date code. For the RKD package option, the tested devices will have date code that start 36 or later. For the ZAY package option, the tested devices will have date code that start 3B or later. Refer to [Figure 1](#) for the location of the date code for the respective packages.

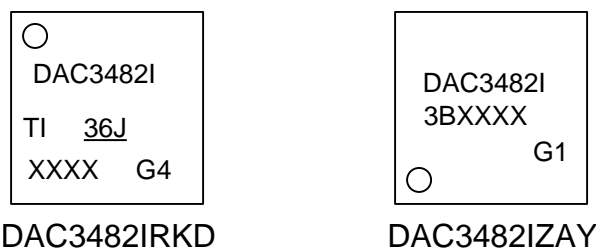


Figure 1. Date Code Location for RKD Package Option and ZAY Package Option

TYPICAL CHARACTERISTICS

All plots are at 25°C, nominal supply voltage, $f_{\text{DAC}} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

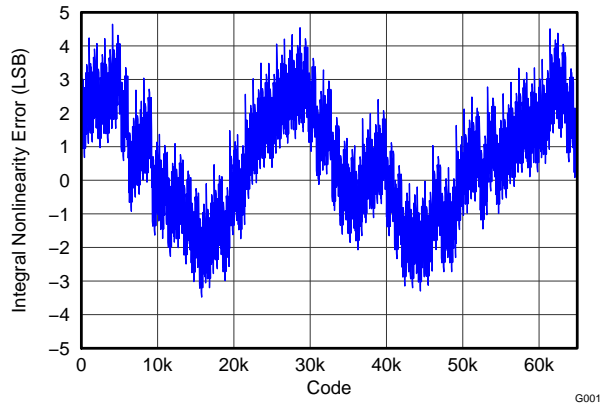


Figure 2. Integral Nonlinearity

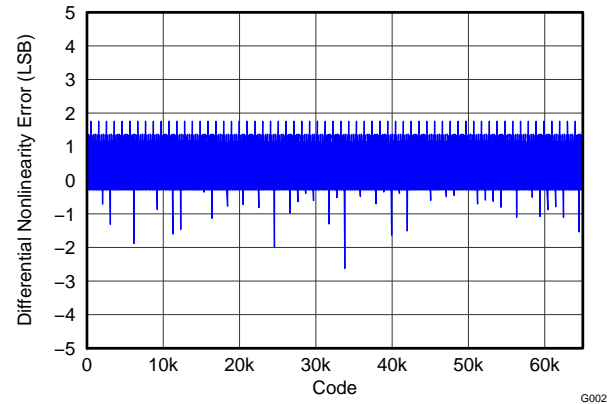


Figure 3. Differential Nonlinearity

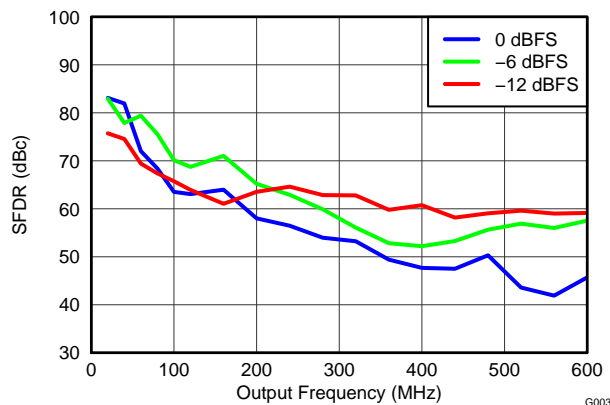


Figure 4. SFDR vs Output Frequency Over Input Scale

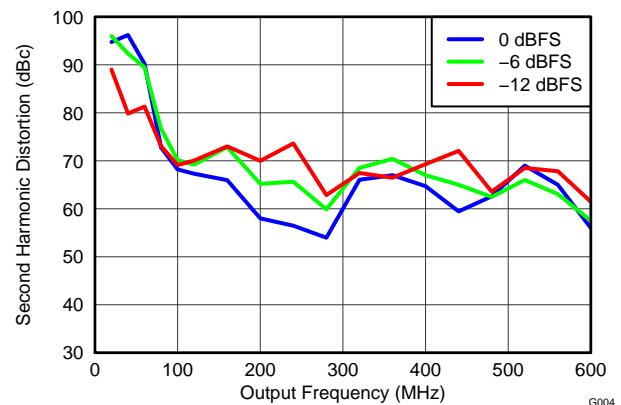


Figure 5. Second Harmonic Distortion vs Output Frequency Over Input Scale

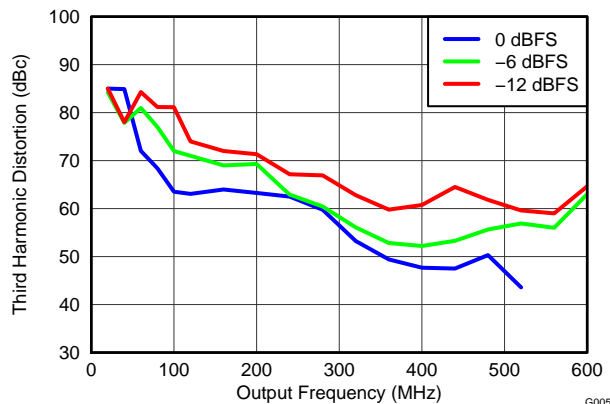


Figure 6. Third Harmonic Distortion vs Output Frequency Over Input Scale

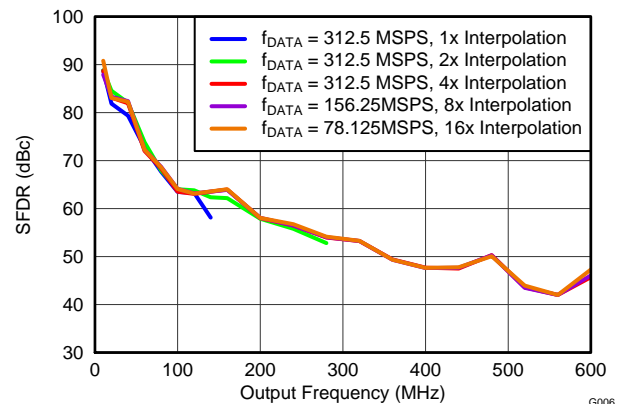


Figure 7. SFDR vs Output Frequency Over Interpolation

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

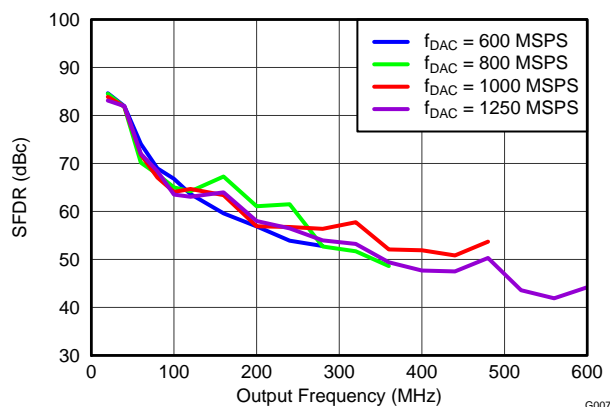


Figure 8. SFDR vs Output Frequency Over f_{DAC}

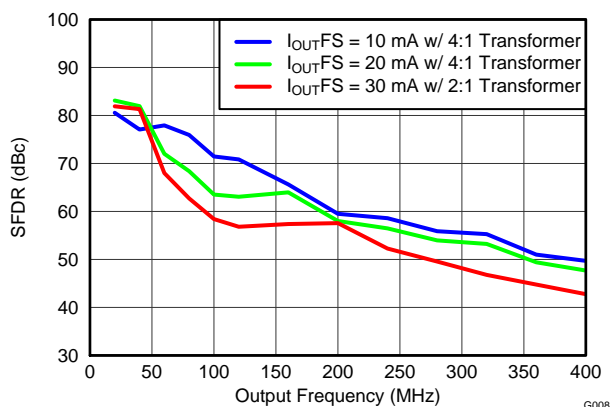


Figure 9. SFDR vs Output Frequency Over I_{OUTFS}

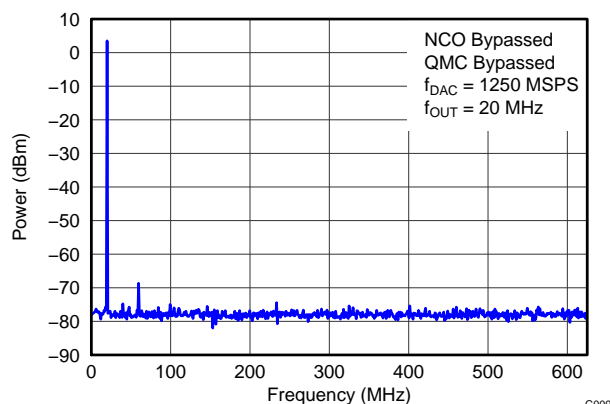


Figure 10. Single Tone Spectral Plot

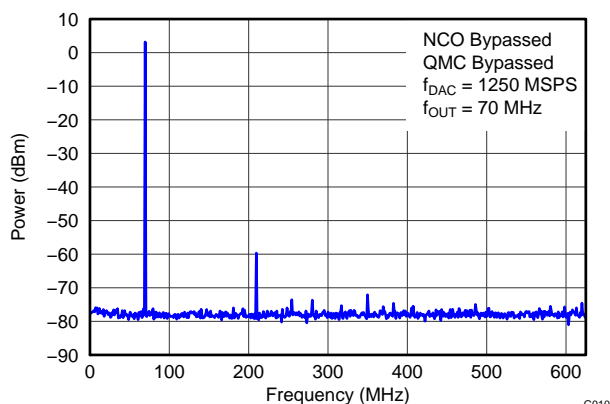


Figure 11. Single Tone Spectral Plot

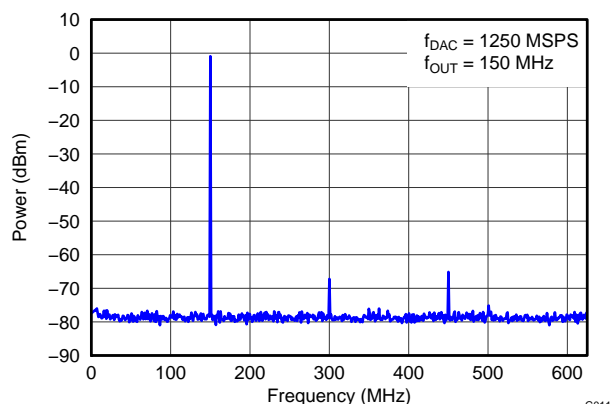


Figure 12. Single Tone Spectral Plot

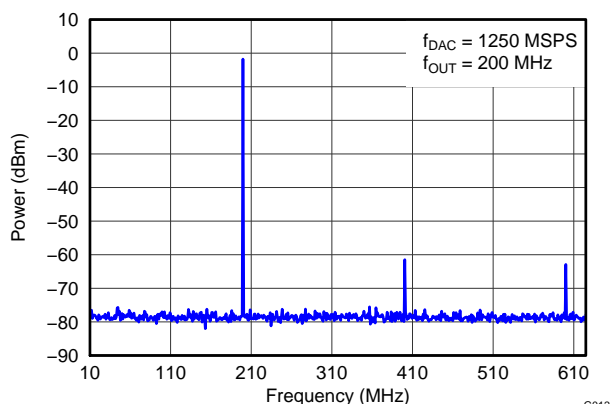


Figure 13. Single Tone Spectral Plot

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

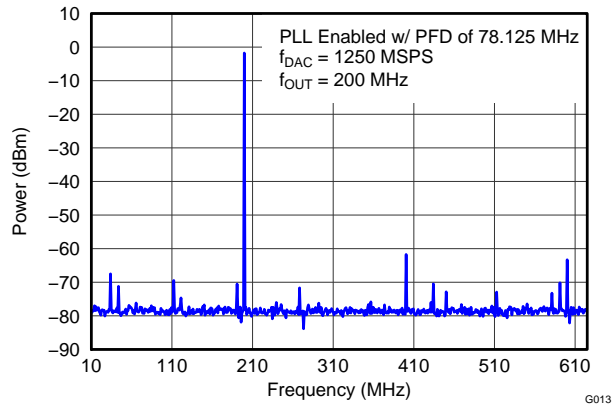


Figure 14. Single Tone Spectral Plot

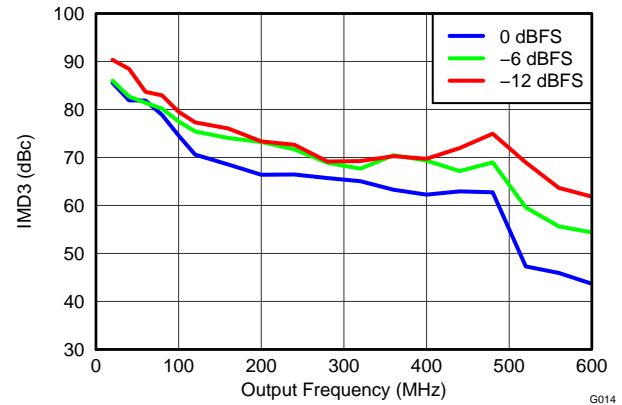


Figure 15. IMD3 vs Output Frequency Over Input Scale

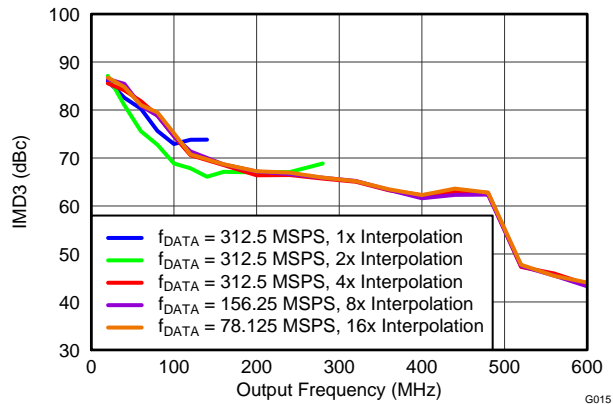


Figure 16. IMD3 vs Output Frequency Over Interpolation

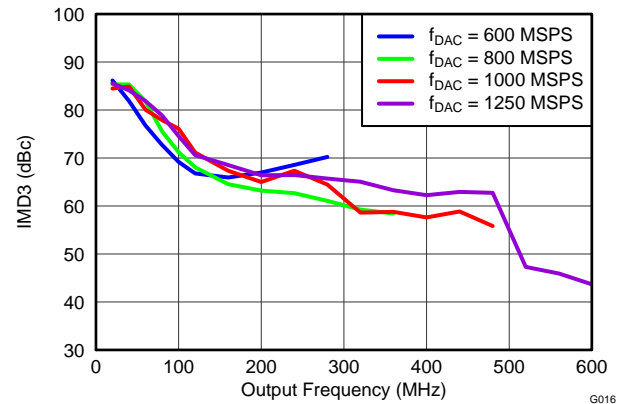
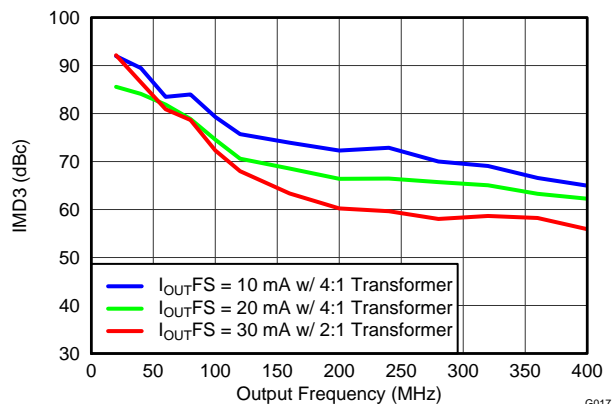
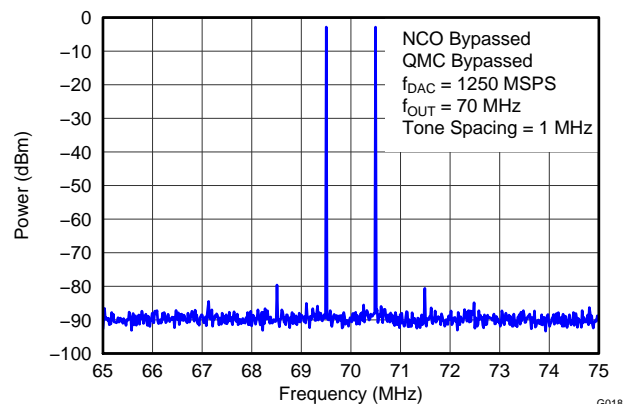
Figure 17. IMD3 vs Output Frequency Over f_{DAC} Figure 18. IMD3 vs Output Frequency Over I_{OUTFS} 

Figure 19. Two Tone Spectral Plot

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

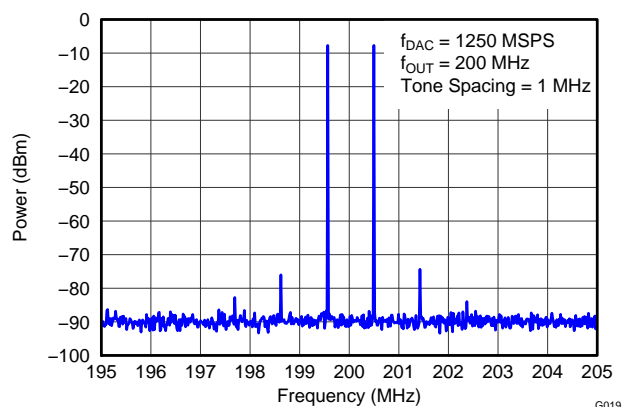


Figure 20. Two Tone Spectral Plot

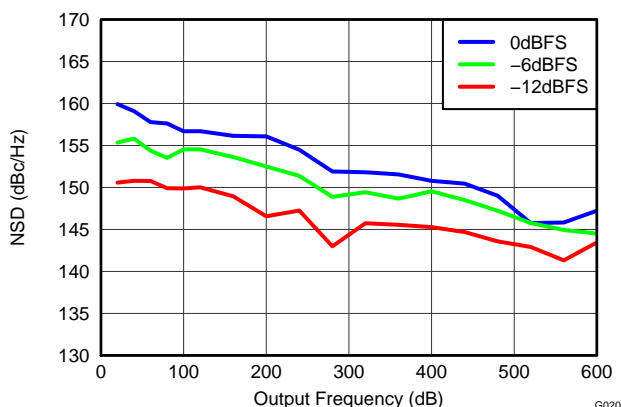


Figure 21. NSD vs Output Frequency Over Input Scale

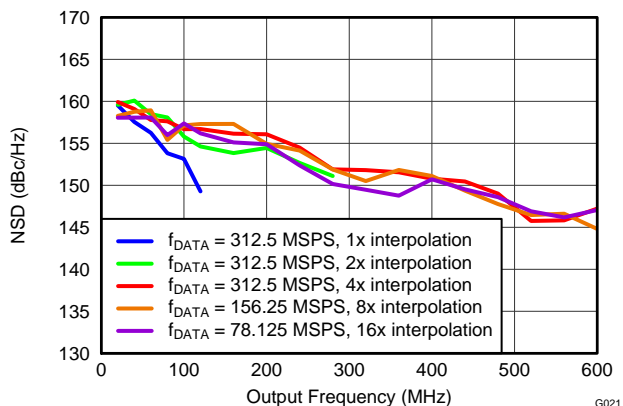


Figure 22. NSD vs Output Frequency Over Interpolation

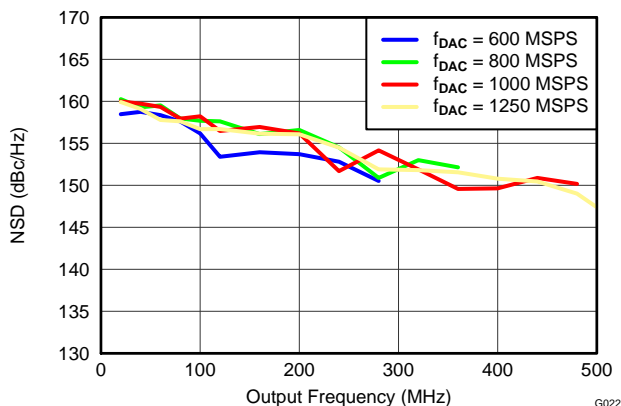


Figure 23. NSD vs Output Frequency Over f_{DAC}

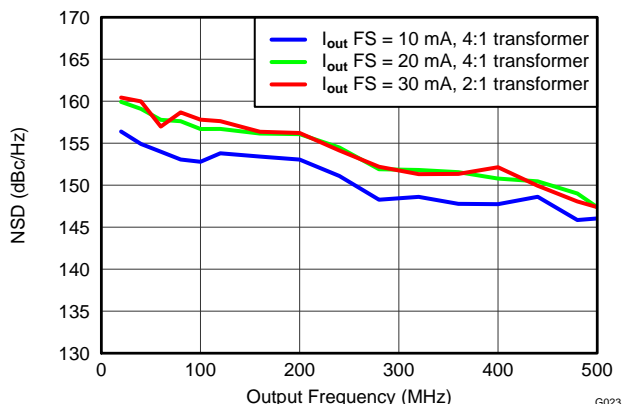


Figure 24. NSD vs Output Frequency Over I_{OUTFS}

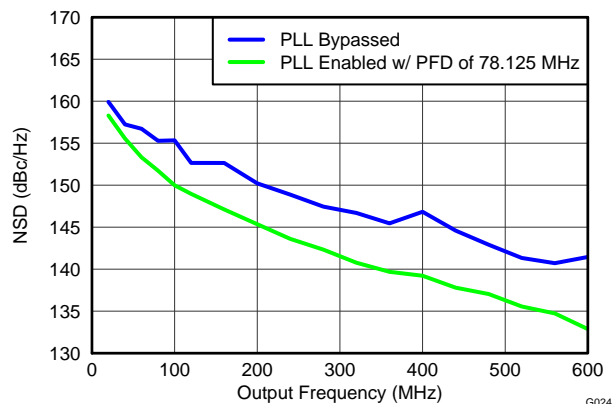


Figure 25. NSD vs Output Frequency Over Clocking Options

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

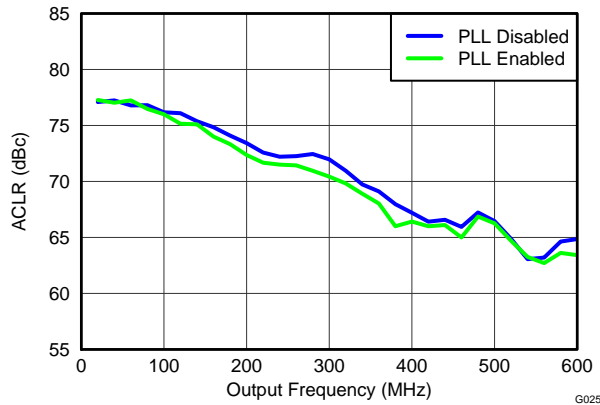


Figure 26. Single Carrier WCDMA ACLR (Adjacent) vs Output Frequency Over Clocking Options

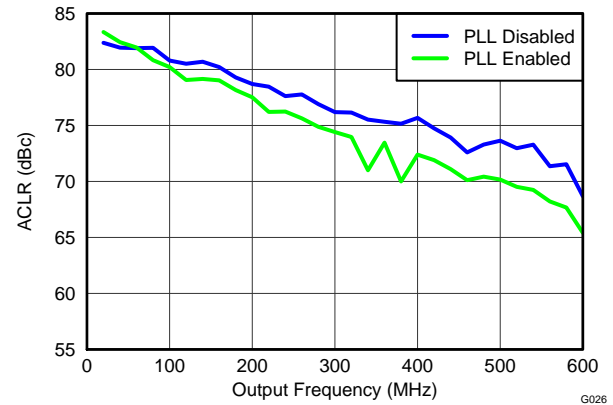


Figure 27. Single Carrier WCDMA ACLR (Alternate) vs Output Frequency Over Clocking Options

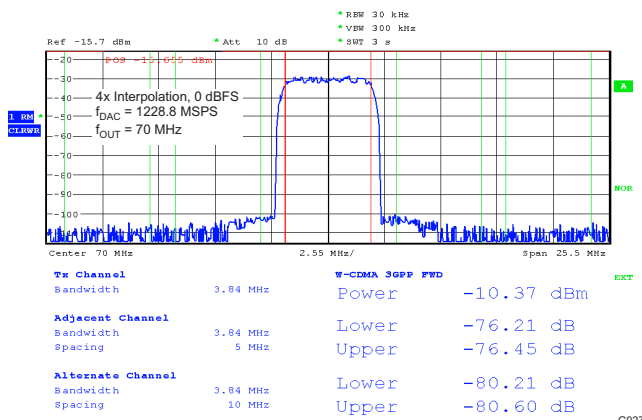


Figure 28. Single Carrier W-CDMA Test Model 1

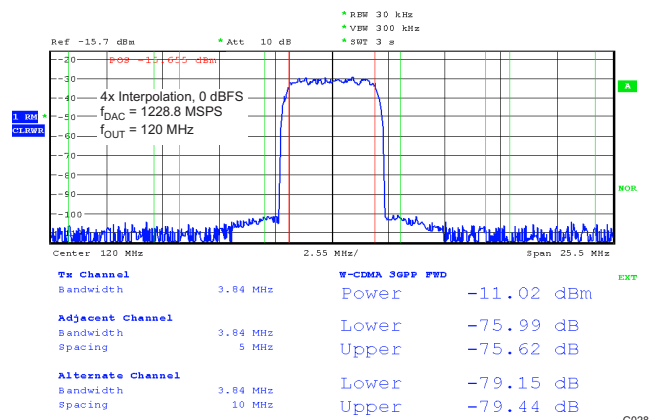


Figure 29. Single Carrier W-CDMA Test Model 1

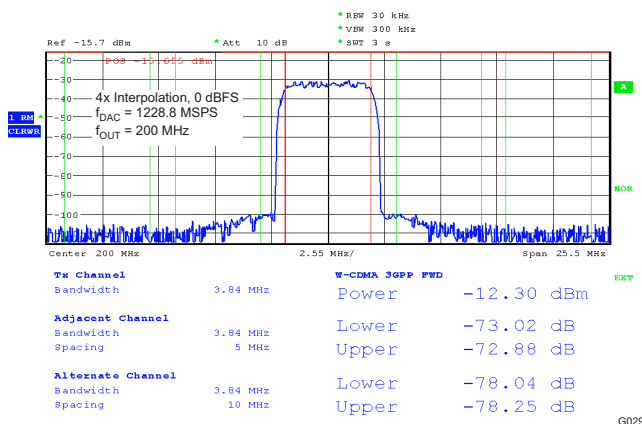


Figure 30. Single Carrier W-CDMA Test Model 1

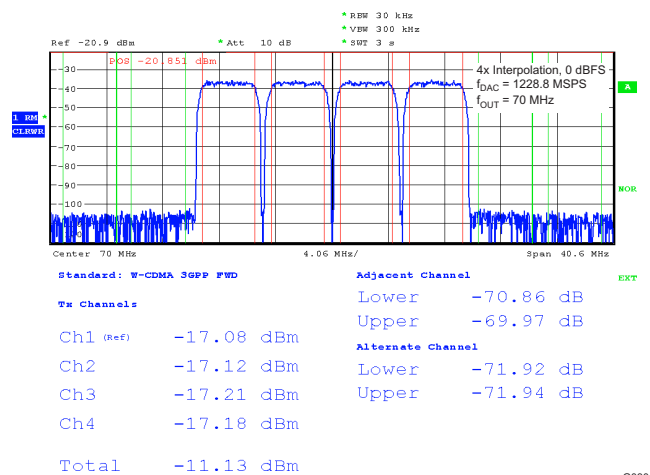


Figure 31. Four Carrier W-CDMA Test Model 1

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

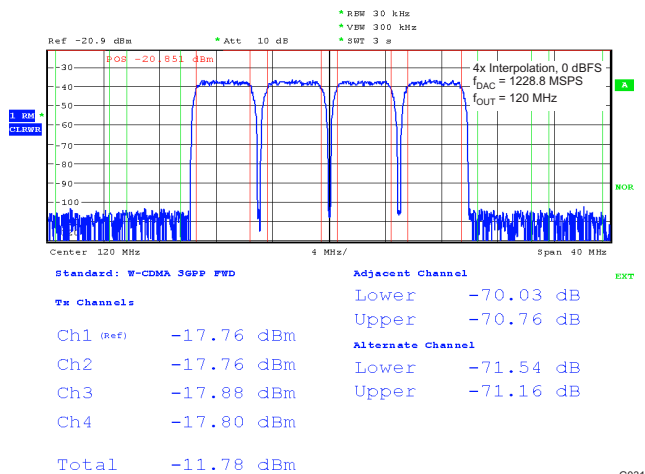


Figure 32. Four Carrier W-CDMA Test Model 1

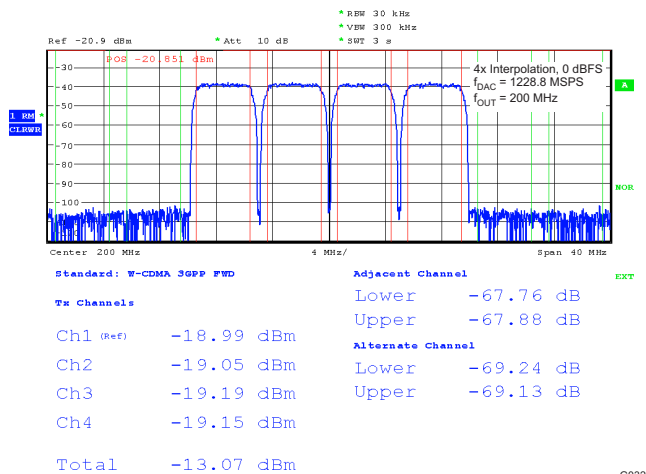


Figure 33. Four Carrier W-CDMA Test Model 1

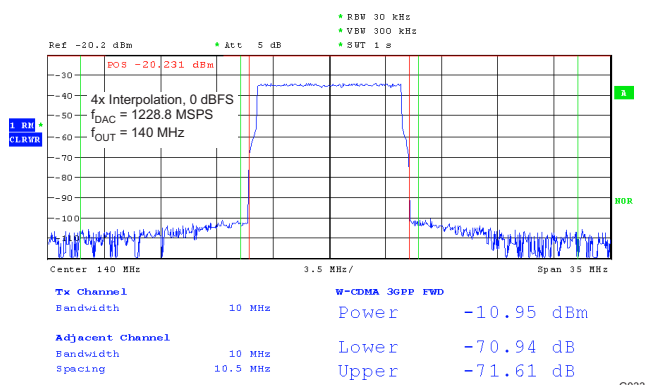


Figure 34. 10 MHz Single Carrier LTE Test Model 3.1

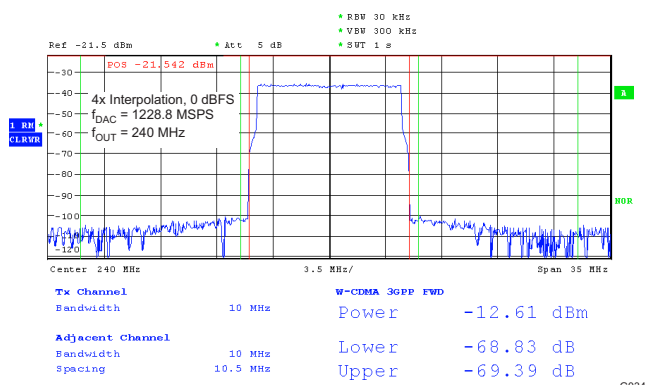


Figure 35. 10 MHz Single Carrier LTE Test Model 3.1

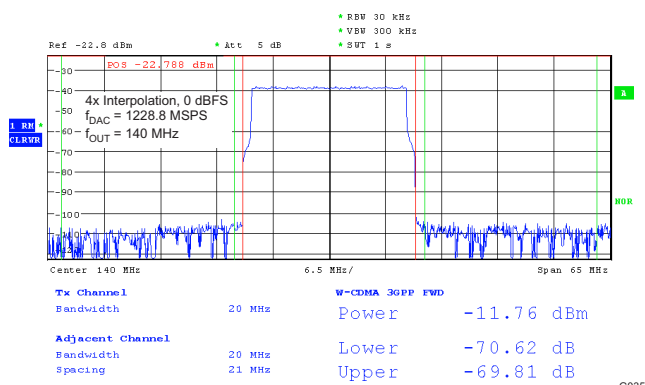


Figure 36. 20 MHz Single Carrier LTE Test Model 3.1

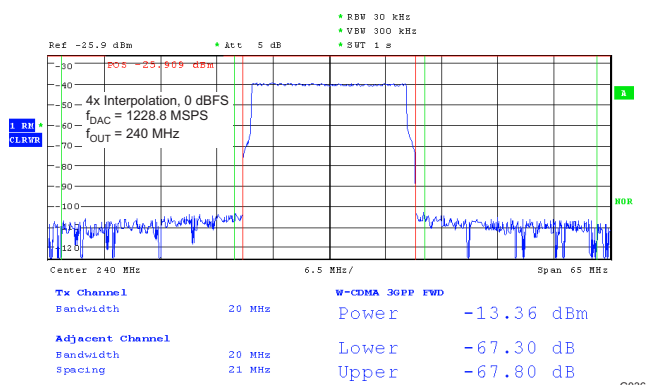


Figure 37. 20 MHz Single Carrier LTE Test Model 3.1

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

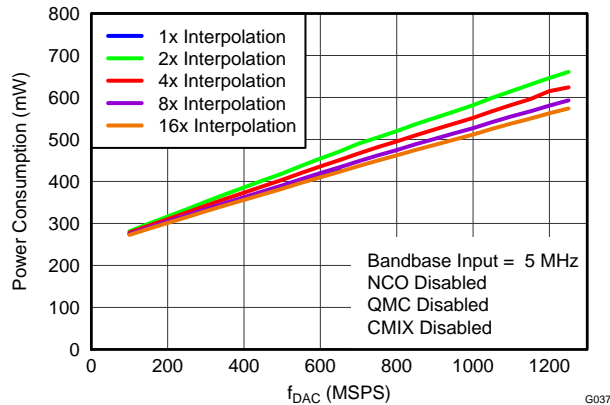


Figure 38. Power Consumption vs f_{DAC} Over Interpolation

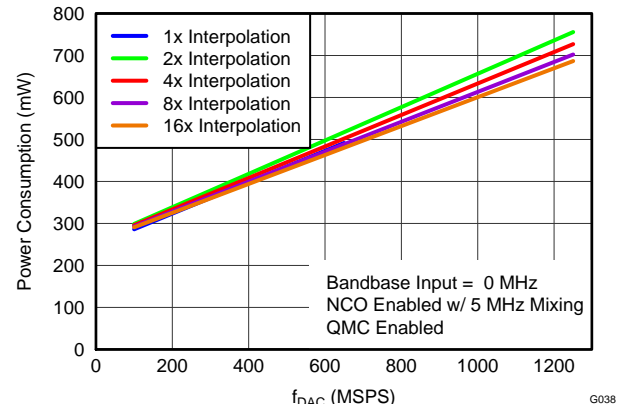


Figure 39. Power Consumption vs f_{DAC} Over Interpolation

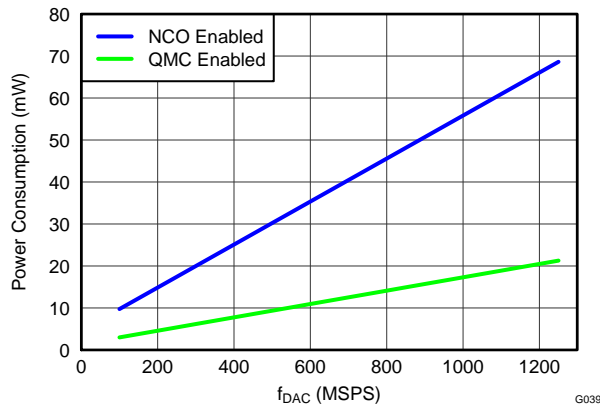


Figure 40. Power Consumption vs f_{DAC} Over Digital Processing Functions

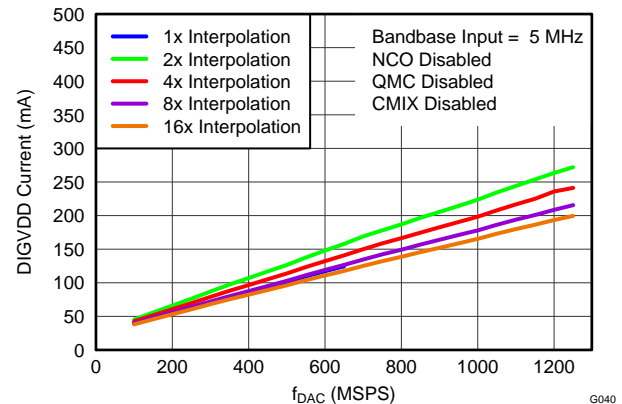


Figure 41. DIGVDD Current vs f_{DAC} Over Interpolation

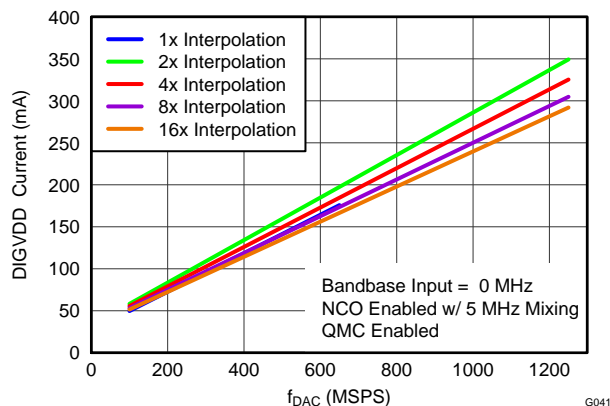


Figure 42. DIGVDD Current vs f_{DAC} Over Interpolation

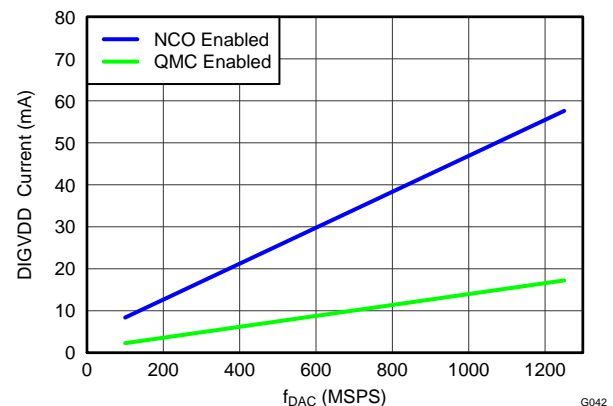


Figure 43. DIGVDD Current vs f_{DAC} Over Digital Processing Functions

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltage, $f_{DAC} = 1250$ MSPS, 4x interpolation, NCO enabled, Mixer Gain disabled, QMC enabled with gain set at 1446 for both I/Q channels, 0 dBFS digital input, 20 mA full-scale output current with 4:1 transformer (unless otherwise noted)

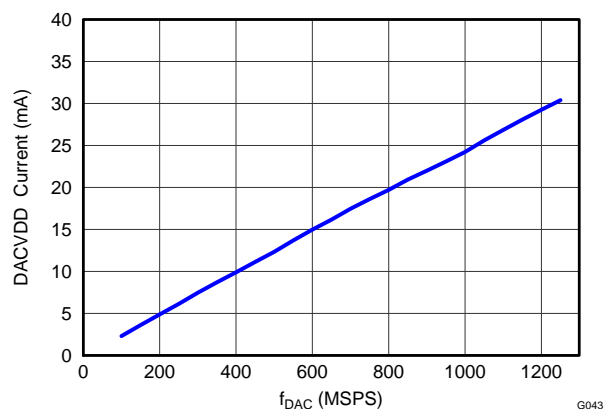


Figure 44. DACVDD Current vs f_{DAC}

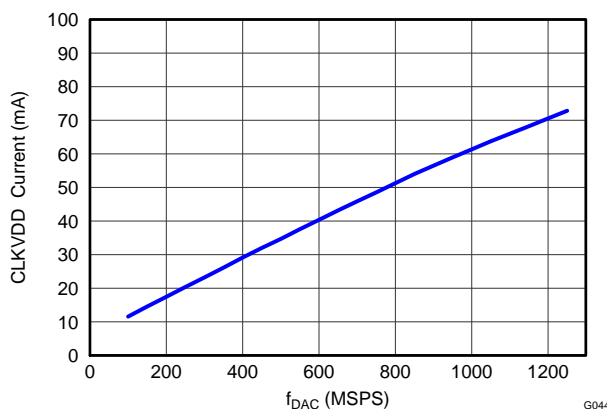


Figure 45. CLKVDD Current vs f_{DAC}

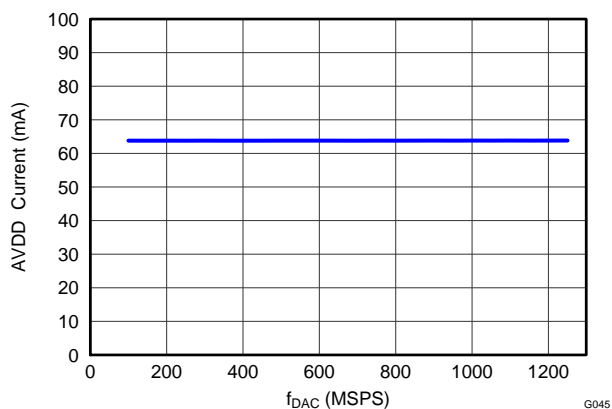


Figure 46. AVDD Current vs f_{DAC}

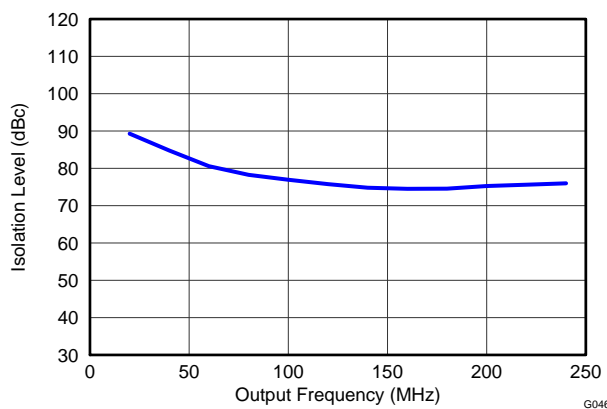


Figure 47. Isolation Level vs Output Frequency

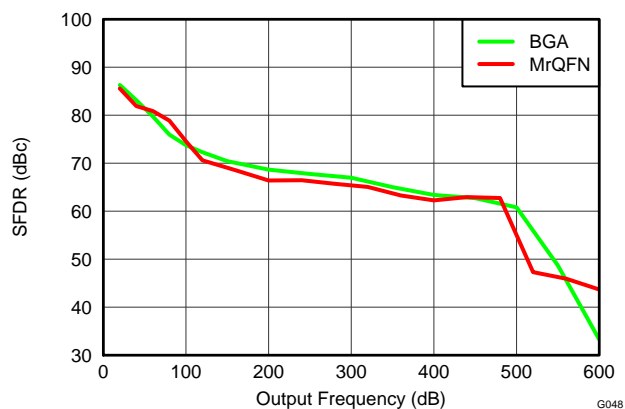


Figure 48. SFDR vs Output Frequency

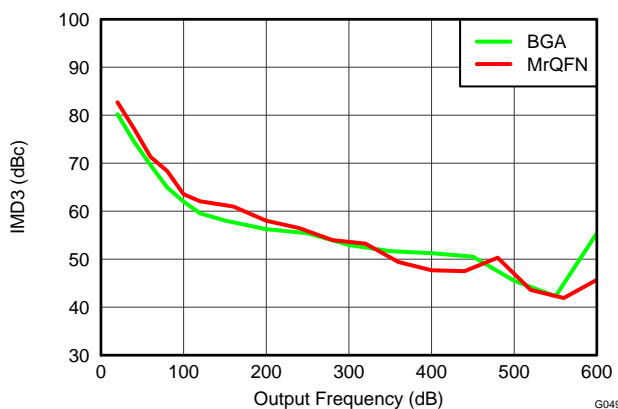


Figure 49. IMD3 vs Output Frequency

DEFINITION OF SPECIFICATIONS

Adjacent Carrier Leakage Ratio (ACLR): Defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3): The two-tone IMD3 is defined as the ratio (in dBc) of the 3rd-order intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal within the first Nyquist zone.

Noise Spectral Density (NSD): Defined as the difference of power (in dBc) between the output tone signal power and the noise floor of 1Hz bandwidth within the first Nyquist zone.

SERIAL INTERFACE

The serial port of the DAC3482 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC3482. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by *sif4_ena* in register *config2*. In both configurations, SCLK is the serial interface input clock and SDENB is serial interface enable. For 3 pin configuration, SDIO is a bidirectional pin for both data in and data out. For 4 pin configuration, SDIO is data in only and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK.

Each read/write operation is framed by signal SDENB (Serial Data Enable Bar) asserted low. The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write as well as the 7-bit address to be accessed. Table 1 below indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. The data transfer cycle consists of two bytes.

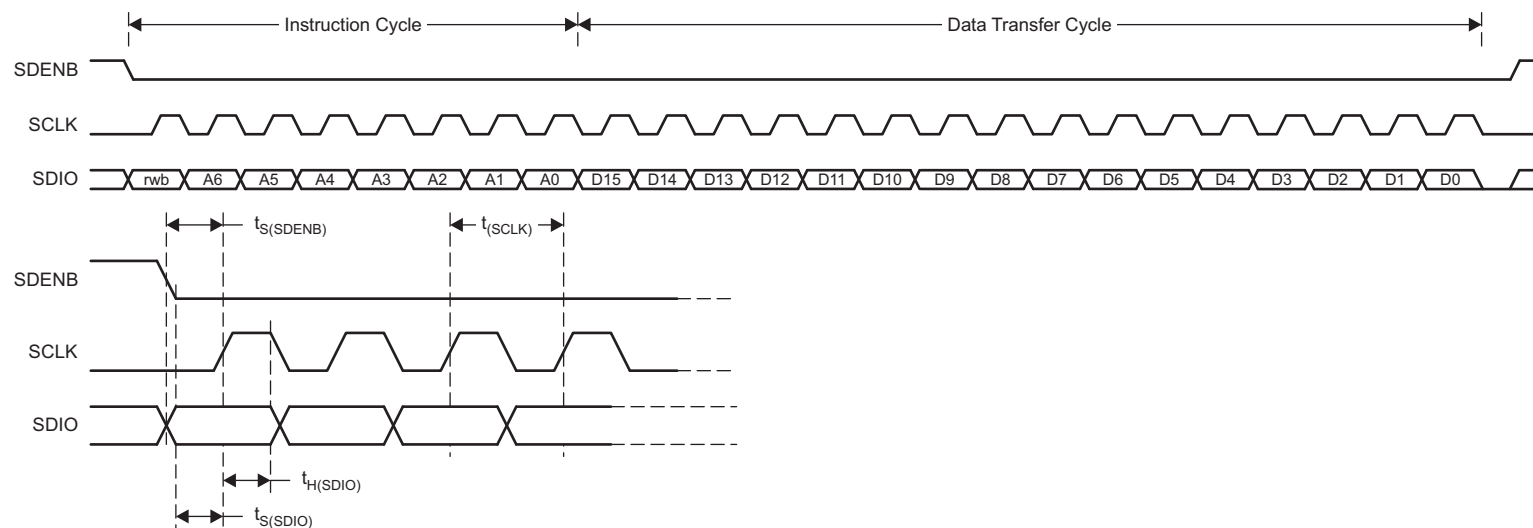
Table 1. Instruction Byte of the Serial Interface

| | MSB | | | | | | | LSB |
|-------------|-----|----|----|----|----|----|----|-----|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Description | R/W | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC3482 and a low indicates a write operation to DAC3482.

[A6 : A0] Identifies the address of the register to be accessed during the read or write operation.

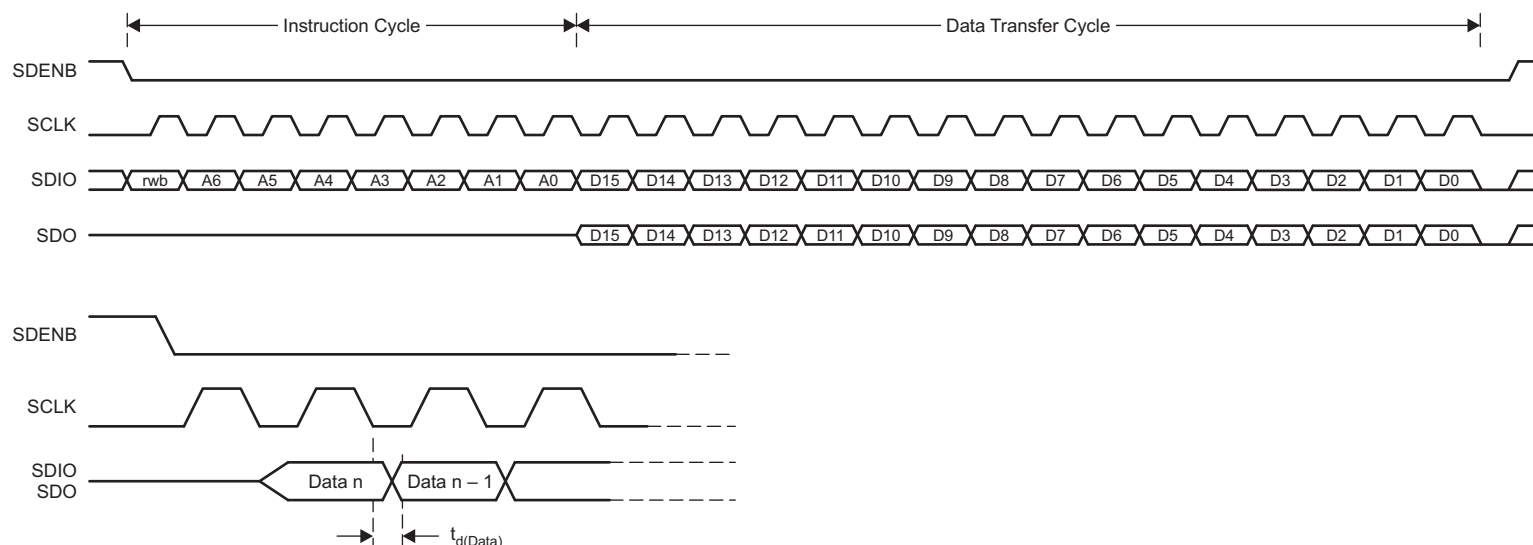
Figure 50 shows the serial interface timing diagram for a DAC3482 write operation. SCLK is the serial interface clock input to DAC3482. Serial data enable SDENB is an active low input to DAC3482. SDIO is serial data in. Input data to DAC3482 is clocked on the rising edges of SCLK.



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Figure 50. Serial Interface Write Timing Diagram

Figure 51 shows the serial interface timing diagram for a DAC3482 read operation. SCLK is the serial interface clock input to DAC3482. Serial data enable SDENB is an active low input to DAC3482. SDIO is serial data in during the instruction cycle, while SDO is in a high-impedance state. In 3 pin configuration, SDIO is data out from the DAC3482 during the data transfer cycle, while SDO is in a high-impedance state. In 4 pin configuration, SDO is data out from the DAC3482 during the data transfer cycle. At the end of the data transfer, SDIO and SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when they will 3-state.



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Figure 51. Serial Interface Read Timing Diagram

Table 2. Register Map⁽¹⁾

| Name | Address | Default | (MSB) Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 | |
|----------|---------|---------|-----------------------|-----------------|-----------------------|--------------------|------------------|-------------------|--------------------|-------------------|---------------------|-----------------|-----------------|---------------|-------------------|--------------------|---------------------|----------------|----------|
| config0 | 0x00 | 0x049C | qmc_offset_ena | reserved | qmc_corr_ena | reserved | interp(3:0) | | | | fifo_ena | reserved | reserved | alarm_out_ena | alarm_out_pol | clkdiv_sync_ena | invsinc_ena | reserved | |
| config1 | 0x01 | 0x050E | iotest_ena | reserved | reserved | 64cnt_ena | oddeven_parity | word_parity_ena | frame_parity_ena | reserved | reserved | dacI_complement | dacQ_complement | reserved | alarm_2away_ena | alarm_1away_ena | alarm_collision_ena | reserved | |
| config2 | 0x02 | 0x7000 | 16bit_in | dacclk_gone_ena | dataclk_gone_ena | collision_gone_ena | resreved | reserved | reserved | reserved | sif4_ena | mixer_ena | mixer_gain | nco_ena | revbus | reserved | twos | reserved | |
| config3 | 0x03 | 0xF000 | coarse_dac(3:0) | | | | reserved | | | | reserved | | | | | | | sif_txenable | |
| config4 | 0x04 | NA | iotest_results(15:0) | | | | | | | | | | | | | | | | |
| config5 | 0x05 | NA | alarm_from_zerochk | reserved | alarms_from_fifo(2:0) | | | alarm_dacclk_gone | alarm_dataclk_gone | alarm_output_gone | alarm_from_iotest | reserved | alarm_from_pll | alarm_rparity | alarm_fparity | alarm_frame_parity | reserved | reserved | |
| config6 | 0x06 | NA | tempdata(7:0) | | | | | | | | reserved | | | | | | | reserved | reserved |
| config7 | 0x07 | 0xFFFF | alarms_mask(15:0) | | | | | | | | | | | | | | | | |
| config8 | 0x08 | 0x0000 | reserved | reserved | reserved | qmc_offsetI(12:0) | | | | | | | | | | | | | |
| config9 | 0x09 | 0x8000 | fifo_offset(2:0) | | | qmc_offsetQ(12:0) | | | | | | | | | | | | | |
| config10 | 0x0A | 0x0000 | reserved | reserved | reserved | reserved | | | | | | | | | | | | | |
| config11 | 0x0B | 0x0000 | reserved | reserved | reserved | reserved | | | | | | | | | | | | | |
| config12 | 0x0C | 0x0400 | reserved | reserved | reserved | reserved | reserved | qmc_gainI(10:0) | | | | | | | | | | | |
| config13 | 0x0D | 0x0400 | cmix(3:0) | | | | reserved | qmc_gainQ(10:0) | | | | | | | | | | | |
| config14 | 0x0E | 0x0400 | reserved | reserved | reserved | reserved | reserved | reserved | | | | | | | | | | | |
| config15 | 0x0F | 0x0400 | output_delay(1:0) | | reserved | | reserved | reserved | | | | | | | | | | | |
| config16 | 0x10 | 0x0000 | reserved | reserved | reserved | reserved | qmc_phase(11:0) | | | | | | | | | | | | |
| config17 | 0x11 | 0x0000 | reserved | reserved | reserved | reserved | reserved | | | | | | | | | | | | |
| config18 | 0x12 | 0x0000 | phase_offset(15:0) | | | | | | | | | | | | | | | | |
| config19 | 0x13 | 0x0000 | reserved | | | | | | | | | | | | | | | | |
| config20 | 0x14 | 0x0000 | phase_add(15:0) | | | | | | | | | | | | | | | | |
| config21 | 0x15 | 0x0000 | phase_add(31:16) | | | | | | | | | | | | | | | | |
| config22 | 0x16 | 0x0000 | reserved | | | | | | | | | | | | | | | | |
| config23 | 0x17 | 0x0000 | reserved | | | | | | | | | | | | | | | | |
| config24 | 0x18 | NA | reserved | | | pll_reset | pll_ndivsync_ena | pll_ena | reserved | | pll_cp(1:0) | | pll_p(2:0) | | | pll_lfvolt(2:0) | | | |
| config25 | 0x19 | 0x0440 | pll_m(7:0) | | | | | | | | pll_n(3:0) | | | | pll_vcoitune(2:0) | | reserved | | |
| config26 | 0x1A | 0x0020 | pll_vco(5:0) | | | | | | reserved | reserved | bias_sleep | tsense_sleep | pll_sleep | clkrecv_sleep | reserved | reserved | reserved | reserved | |
| config27 | 0x1B | 0x0000 | extref_ena | reserved | reserved | reserved | fuse_sleep | reserved | reserved | reserved | reserved | reserved | reserved | | | | | | |
| config28 | 0x1C | 0x0000 | reserved | | | | | | | | reserved | | | | | | | | |
| config29 | 0x1D | 0x0000 | reserved | | | | | | | | reserved | | | | | | | | |
| config30 | 0x1E | 0x1111 | syncsel_qmoffset(3:0) | | | | reserved | | | | syncsel_qmcorr(3:0) | | | | reserved | | | | |

(1) Unless otherwise noted, all reserved registers should be programmed to default values.

Table 2. Register Map⁽¹⁾ (continued)

| Name | Address | Default | (MSB) Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 |
|----------|---------|---------|---------------------|---------------|----------|-------------|----------------------|--------|----------|----------|------------------|----------|----------|---------------|-----------------------|----------------|----------|-----------------|
| config31 | 0x1F | 0x1140 | syncsel_mixer(3:0) | | | | reserved | | | | syncsel_nco(3:0) | | | | syncsel_dataformatter | | sif_sync | reserved |
| config32 | 0x20 | 0x2400 | syncsel_fifoIn(3:0) | | | | syncsel_fifoout(3:0) | | | | reserved | | | | | | | clkdiv_sync_sel |
| config33 | 0x21 | 0x0000 | reserved | | | | | | | | | | | | | | | |
| config34 | 0x22 | 0x1B1B | reserved | | reserved | | reserved | | reserved | | reserved | | reserved | | reserved | | reserved | |
| config35 | 0x23 | 0xFFFF | sleep_cntl(15:0) | | | | | | | | | | | | | | | |
| config36 | 0x24 | 0x0000 | datadly(2:0) | | | clkdly(2:0) | | | reserved | | | | | | | | | |
| config37 | 0x25 | 0x7A7A | iostest_pattern0 | | | | | | | | | | | | | | | |
| config38 | 0x26 | 0xB6B6 | iostest_pattern1 | | | | | | | | | | | | | | | |
| config39 | 0x27 | 0xEAEA | iostest_pattern2 | | | | | | | | | | | | | | | |
| config40 | 0x28 | 0x4545 | iostest_pattern3 | | | | | | | | | | | | | | | |
| config41 | 0x29 | 0x1A1A | iostest_pattern4 | | | | | | | | | | | | | | | |
| config42 | 0x2A | 0x1616 | iostest_pattern5 | | | | | | | | | | | | | | | |
| config43 | 0x2B | 0xAAAA | iostest_pattern6 | | | | | | | | | | | | | | | |
| config44 | 0x2C | 0xC6C6 | iostest_pattern7 | | | | | | | | | | | | | | | |
| config45 | 0x2D | 0x0004 | reserved | ostrtodig_sel | ramp_ena | reserved | | | | | | | | | | | | sifdac_ena |
| config46 | 0x2E | 0x0000 | reserved | | | | | | | | grp_delayl(7:0) | | | | | | | |
| config47 | 0x2F | 0x0000 | grp_delayQ(7:0) | | | | | | | | reserved | | | | | | | |
| config48 | 0x30 | 0x0000 | sifdac(15:0) | | | | | | | | | | | | | | | |
| version | 0x7F | 0x540C | reserved | | | | | | reserved | reserved | | reserved | | deviceid(1:0) | | versionid(2:0) | | |

REGISTER DESCRIPTIONS

Register name: config0 – Address: 0x00, Default: 0x049C

| Register Name | Address | Bit | Name | Function | Default Value | |
|---------------|-----------------|--|----------------|--|----------------------|------|
| config0 | 0x00 | 15 | qmc_offset_ena | When set, the digital Quadrature Modulator Correction (QMC) offset correction is enabled. | 0 | |
| | | 14 | Reserved | Reserved for factory use. | 0 | |
| | | 13 | qmc_corr_ena | When set, the QMC phase and gain correction circuitry is enabled. | 0 | |
| | | 12 | Reserved | Reserved for factory use. | 0 | |
| | | 11:8 | interp(3:0) | These bits define the interpolation factor | | 0100 |
| | | | | interp | Interpolation Factor | |
| | | | | 0000 | 1x | |
| | | | | 0001 | 2x | |
| | | | | 0010 | 4x | |
| | | | | 0100 | 8x | |
| | | | | 1000 | 16x | |
| | | 7 | fifo_ena | When set, the FIFO is enabled. When the FIFO is disabled DACCCLKP/N and DATACLKP/N must be aligned (not recommended). | 1 | |
| | | 6 | Reserved | Reserved for factory use. | 0 | |
| | | 5 | Reserved | Reserved for factory use. | 0 | |
| | | 4 | alarm_out_ena | When set, the ALARM pin becomes an output. When cleared, the ALARM pin is 3-stated. | 1 | |
| | | 3 | alarm_out_pol | This bit changes the polarity of the ALARM signal. 0: Negative logic 1: Positive logic | 1 | |
| 2 | clkdiv_sync_ena | When set, enables the syncing of the clock divider using the sync source selected by register <i>config32</i> . The internal divided-down clocks will be phase aligned after syncing. See the Power-Up Sequence section for more detail. | 1 | | | |
| 1 | invsinc_ena | When set, the inverse sinc filter is enabled. | 0 | | | |
| 0 | Reserved | Reserved for factory use. | 0 | | | |

Register name: config1 – Address: 0x01, Default: 0x050E

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-----|---------------------|--|---------------|
| config1 | 0x01 | 15 | iotest_ena | When set, enables the data pattern checker test. <i>The outputs are deactivated regardless of the state of TXENABLE and sif_txenable.</i> | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12 | 64cnt_ena | When set, enables resetting of the alarms after 64 good samples with the goal of removing unnecessary errors. For instance, when checking setup/hold through the pattern checker test, there may initially be errors. Setting this bit removes the need for a SIF write to clear the alarm register. | 0 |
| | | 11 | oddeven_parity | Selects between odd and even parity check 0: Even parity 1: Odd parity | 0 |
| | | 10 | word_parity_ena | When set, enables parity checking of each input word using the PARITYP/N parity input. It should match the oddeven_parity register setting. | 1 |
| | | 9 | frame_parity_ena | When set, enables parity checking using the FRAME signal to source the parity bit. | 0 |
| | | 8 | Reserved | Reserved for factory use. Note: Default value is '1'. Must be set to '0' for proper operation | 1 |
| | | 7 | Reserved | Reserved for factory use. | 0 |
| | | 6 | dacI_complement | When set, the DACI output is complemented. This allows to effectively change the + and – designations of the LVDS data lines. | 0 |
| | | 5 | dacQ_complement | When set, the DACQ output is complemented. This allows to effectively change the + and – designations of the LVDS data lines. | 0 |
| | | 4 | Reserved | Reserved for factory use. | 0 |
| | | 3 | alarm_2away_ena | When set, the alarm from the FIFO indicating the write and read pointers being 2 away is enabled. | 1 |
| | | 2 | alarm_1away_ena | When set, the alarm from the FIFO indicating the write and read pointers being 1 away is enabled. | 1 |
| | | 1 | alarm_collision_ena | When set, the alarm from the FIFO indicating a collision between the write and read pointers is enabled. | 1 |
| | | 0 | Reserved | Reserved for factory use. | 0 |

Register name: config2 – Address: 0x02, Default: 0x7000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-----|-------------------|---|---------------|
| config2 | 0x02 | 15 | 16bit_in | When set, the input interface is set to word-wide mode. When cleared, the input interface is set to byte-wide mode. | 0 |
| | | 14 | dacclkgone_ena | When set, the DACCLK-gone signal from the clock monitor circuit can be used to shut off the DAC outputs. The corresponding alarms, <i>alarm_dacclk_gone</i> and <i>alarm_output_gone</i> , must not be masked (i.e.Config7, bit <10> and bit <8> must set to "0"). | 1 |
| | | 13 | dataclkgone_ena | When set, the DATACLK-gone signal from the clock monitor circuit can be used to shut off the DAC outputs. The corresponding alarms, <i>alarm_dataclk_gone</i> and <i>alarm_output_gone</i> , must not be masked (i.e.Config7, bit <9> and bit <8> must set to "0"). | 1 |
| | | 12 | collisiongone_ena | When set, the FIFO collision alarms can be used to shut off the DAC outputs. The corresponding alarms, <i>alarm_fifo_collision</i> and <i>alarm_output_gone</i> , must not be masked (i.e.Config7, bit <13> and bit <8> must set to "0"). | 1 |
| | | 11 | Reserved | Reserved for factory use. | 0 |
| | | 10 | Reserved | Reserved for factory use. | 0 |
| | | 9 | Reserved | Reserved for factory use. | 0 |
| | | 8 | Reserved | Reserved for factory use. | 0 |
| | | 7 | sif4_ena | When set, the serial interface (SIF) is a 4 bit interface, otherwise it is a 3 bit interface. | 0 |
| | | 6 | mixer_ena | When set, the mixer block is enabled. | 0 |
| | | 5 | mixer_gain | When set, a 6dB gain is added to the mixer output. | 0 |
| | | 4 | nco_ena | When set, the NCO is enabled. This is not required for coarse mixing. | 0 |
| | | 3 | revbus | When set, the input bits for the data bus are reversed. MSB becomes LSB. | 0 |
| | | 2 | Reserved | Reserved for factory use. | 0 |
| | | 1 | twos | When set, the input data format is expected to be 2's complement. When cleared, the input is expected to be offset-binary. | 0 |
| | | 0 | Reserved | Reserved for factory use. | 0 |

Register name: config3 – Address: 0x03, Default: 0xF000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-----------------|---|---------------|
| config3 | 0x03 | 15:12 | coarse_dac(3:0) | Scales the output current in 16 equal steps. $I_{FS} = \frac{V_{EXTIO}}{R_{BIAS}} \times 2 \times (\text{coarse_dac} + 1)$ | 1111 |
| | | 11:8 | Reserved | Reserved for factory use. | 0000 |
| | | 7:1 | Reserved | Reserved for factory use. | 0000000 |
| | | 0 | sif_txenable | When set, the internal value of TXENABLE is set to "1". To enable analog output data transmission, set <i>sif_txenable</i> to "1" or pull CMOS TXENABLE pin (A32) to high. To disable analog output, set <i>sif_txenable</i> to "0" and pull CMOS TXENABLE pin (A32) to low. | 0 |

Register name: config4 – Address: 0x04, Default: No RESET Value (WRITE TO CLEAR)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------------------|--|----------------|
| config4 | 0x04 | 15:0 | iotest_results(15:0) | <p>This register is used with pattern checker test enabled (<i>iotest_ena</i> in <i>config1</i>, <i>bit<15></i> set to "1"). It does not have a default RESET value.</p> <p>The values of these bits tell which bit in the word failed during the pattern checker test. <i>iotest_results</i>(15:8) correspond to the data bits on D[15:8] and <i>iotest_results</i>(7:0) correspond to the data bits on D[7:0].</p> | No RESET Value |

Register name: config5 – Address: 0x05, Default: Setup and Power-Up Conditions Dependent (WRITE TO CLEAR)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-----------------------|--|---------------|
| config5 | 0x05 | 15 | alarm_from_zerochk | This alarm indicates the 8-bit FIFO write pointer address has an all zeros patterns. Due to pointer address being a shift register, this is not a valid address and will cause the write pointer to be stuck until the next sync. This error is typically caused by timing error or improper power start-up sequence. If this alarm is asserted, resynchronization of FIFO is necessary. Refer to the Power-Up Sequence section for more detail. | NA |
| | | 14 | Reserved | Reserved for factory use. | NA |
| | | 13:11 | alarms_from_fifo(2:0) | <p>Alarm indicating FIFO pointer collisions and nearness:</p> <p>000: All fine 001: Pointers are 2 away 01x: Pointers are 1 away 1xx: FIFO pointer collision</p> <p>If the FIFO pointer collision alarm is set when <i>collisiongone_ena</i> is enabled, the FIFO must be re-synchronized and the bits must be cleared to resume normal operation.</p> | NA |
| | | 10 | alarm_dacclk_gone | Alarm indicating the DACCLK has been stopped. If the bit is set when <i>dacclkgone_ena</i> is enabled, the DACCLK must resume and the bit must be cleared to resume normal operation. | NA |
| | | 9 | alarm_dataclk_gone | Alarm indicating the DATACLK has been stopped. If the bit is set when <i>dataclkgone_ena</i> is enabled, the DATACLK must resume and the bit must be cleared to resume normal operation. | NA |
| | | 8 | alarm_output_gone | Alarm indicating either <i>alarm_dacclk_gone</i> , <i>alarm_dataclk_gone</i> , or <i>alarm_fifo_collision</i> are asserted. It controls the output. When high it will output "0x8000" for each output connected to the DAC. If the bit is set when <i>dacclkgone_ena</i> , <i>dataclkgone_ena</i> , or <i>collisiongone_ena</i> are enabled, then the corresponding errors must be fixed and the bits must be cleared to resume normal operation. | NA |
| | | 7 | alarm_from_iotest | Alarm indicating the input data pattern does not match the pattern in the <i>iotest_pattern</i> registers. When data pattern checker mode is enabled, this alarm in register config5, bit7 is the only valid alarm. Other alarms in register config5 are not valid and can be disregarded. | NA |
| | | 6 | Reserved | Reserved for factory use. | NA |
| | | 5 | alarm_from_pll | Alarm indicating the PLL has lost lock. For version ID "100" or earlier, <i>alarm_from_PLL</i> may not indicate the correct status of the PLL. Refer to <i>pll_ifvlt(2:0)</i> in register config24 for proper PLL lock indication. | NA |
| | | 4 | alarm_rparity | Alarm indicating a parity error on data captured on the rising edge of DATACLKP/N. | NA |
| | | 3 | alarm_fparity | Alarm indicating a parity error on data captured on the falling edge of DATACLKP/N. | NA |
| | | 2 | alarm_frame_parity | Alarm indicating a parity error when using the FRAME as parity bit. | NA |
| | | 1 | Reserved | Reserved for factory use. | NA |
| | | 0 | Reserved | Reserved for factory use. | NA |

Register name: config6 – Address: 0x06, Default: No RESET Value (READ ONLY)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|---------------|--|----------------|
| config6 | 0x06 | 15:8 | tempdata(7:0) | This is the output from the chip temperature sensor. The value of this register in two's complement format represents the temperature in degrees Celsius. This register must be read with a minimum SCLK period of 1µs. | No RESET Value |
| | | 7:2 | Reserved | Reserved for factory use. | 000000 |
| | | 1 | Reserved | Reserved for factory use. | 0 |
| | | 0 | Reserved | Reserved for factory use. | 0 |

Register name: config7 – Address: 0x07, Default: 0xFFFF

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-------------------|---|---------------|
| config7 | 0x07 | 15:0 | alarms_mask(15:0) | These bits control the masking of the alarms. (0=not masked, 1= masked) | 0xFFFF |
| | | | | alarm_mask | |
| | | | | Alarm that is Masked | |
| | | | | 15 | |
| | | | | alarm_from_zerock | |
| | | | | 14 | |
| | | | | not used | |
| | | | | 13 | |
| | | | | alarm_fifo_collision | |
| | | | | 12 | |
| | | | | alarm_fifo_1away | |
| | | | | 11 | |
| | | | | alarm_fifo_2away | |
| | | | | 10 | |
| | | | | alarm_dacclk_gone | |
| | | | | 9 | |
| | | | | alarm_dataclk_gone | |
| | | | | 8 | |
| | | | | alarm_output_gone | |
| | | | | 7 | |
| | | | | alarm_from_iotest | |
| | | | | 6 | |
| | | | | not used | |
| | | | | 5 | |
| | | | | alarm_from_pll | |
| | | | | 4 | |
| | | | | alarm_rparity | |
| | | | | 3 | |
| | | | | alarm_lparity | |
| | | | | 2 | |
| | | | | alarm_frame_parity | |
| | | | | 1 | |
| | | | | not used | |
| | | | | 0 | |
| | | | | not used | |

Register name: config8 – Address: 0x08, Default: 0x0000 (CAUSES AUTO-SYNC)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|------------------|---|---------------|
| config8 | 0x08 | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12:0 | qmc_offset(12:0) | DACI offset correction. The offset is measured in DAC LSBs. If enabled in config30 writing to this register causes an auto-sync to be generated. This loads the values of the QMC offset registers (config8-config9) into the offset block at the same time. When updating the offset values config8 should be written last. Programming config9 will not affect the offset setting. | All zeros |

Register name: config9 – Address: 0x09, Default: 0x8000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-------------------|---|---------------|
| config9 | 0x09 | 15:13 | fifo_offset(2:0) | When the sync to the FIFO occurs, this is the value loaded into the FIFO read pointer. With this value the initial difference between write and read pointers can be controlled. This may be helpful in syncing multiple chips or controlling the delay through the device. | 100 |
| | | 12:0 | qmc_offsetQ(12:0) | DACQ offset correction. The offset is measured in DAC LSBs. | All zeros |

Register name: config10 – Address: 0x0A, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config10 | 0x0A | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12:0 | Reserved | Reserved for factory use. | All zeros |

Register name: config11 – Address: 0x0B, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config10 | 0x0A | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12:0 | Reserved | Reserved for factory use. | All zeros |

Register name: config12 – Address: 0x0C, Default: 0x0400

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|-----------------|
| config12 | 0x0C | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12 | Reserved | Reserved for factory use. | 0 |
| | | 11 | Reserved | Reserved for factory use. | 0 |
| | | 10:0 | qmc_gainl(10:0) | QMC gain for DACI. The full 11-bit qmc_gainl(10:0) word is formatted as UNSIGNED with a range of 0 to 1.9990. The implied decimal point for the multiplication is between bit 9 and bit 10. | 10000000 000 |

Register name: config13 – Address: 0x0D, Default: 0x0400

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|-----------------|
| config13 | 0x0D | 15 | cmix_mode(3:0) | Sets the mixing function of the coarse mixer. Bit 15: Fs/8 mixer Bit 14: Fs/4 mixer Bit 13: Fs/2 mixer Bit 12: -Fs/4 mixer The various mixers can be combined together to obtain a $\pm n \times F_s/8$ total mixing factor. | 0000 |
| | | 11 | Reserved | Reserved for factory use. | 0 |
| | | 10:0 | qmc_gainQ(10:0) | QMC gain for DACQ. The full 11-bit qmc_gainb(10:0) word is formatted as UNSIGNED with a range of 0 to 1.9990. The implied decimal point for the multiplication is between bit 9 and bit 10. | 10000000 000 |

Register name: config14 – Address: 0x0E, Default: 0x0400

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|-----------------|
| config14 | 0x0E | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12 | Reserved | Reserved for factory use. | 0 |
| | | 11 | Reserved | Reserved for factory use. | 0 |
| | | 10:0 | Reserved | Reserved for factory use. | 10000000 000 |

Register name: config15 – Address: 0x0F, Default: 0x0400

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-------------------|--|-----------------|
| config15 | 0x0F | 15:14 | output_delay(1:0) | Delays the DAC outputs from 0 to 3 DAC clock cycles. | 00 |
| | | 13:12 | Reserved | Reserved for factory use. | 00 |
| | | 11 | Reserved | Reserved for factory use. | 0 |
| | | 10:0 | Reserved | Reserved for factory use. | 10000000 000 |

Register name: config16 – Address: 0x10, Default: 0x0000 (CAUSES AUTO-SYNC)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config16 | 0x10 | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. Note: Default value is '0'. Must be set to '1' for proper operation | 0 |
| | | 12 | Reserved | Reserved for factory use. Note: Default value is '0'. Must be set to '1' for proper operation | 0 |
| | | 11:0 | qmc_phase(11:0) | QMC correction phase. The 12-bit qmc_phase(11:0) word is formatted as two's complement and scaled to occupy a range of -0.5 to 0.49975 and a default phase correction of 0.00. To accomplish QMC phase correction, this value is multiplied by the current B sample, then summed into the A sample. If enabled in config30 writing to this register causes an auto-sync to be generated. This loads the values of the QMC offset registers (config12, config13, and config16) into the QMC block at the same time. When updating the QMC values config16 should be written last. Programming config12 and config13 will not affect the QMC settings. | All zeros |

Register name: config17 – Address: 0x11, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config17 | 0x11 | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | Reserved | Reserved for factory use. | 0 |
| | | 13 | Reserved | Reserved for factory use. | 0 |
| | | 12 | Reserved | Reserved for factory use. | 0 |
| | | 11:0 | Reserved | Reserved for factory use. | All zeros |

Register name: config18 – Address: 0x12, Default: 0x0000 (CAUSES AUTO-SYNC)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|--------------------|---|---------------|
| config18 | 0x12 | 15:0 | phase_offset(15:0) | Phase offset added to the NCO accumulator before the generation of the SIN and COS values. The phase offset is added to the upper 16 bits of the NCO accumulator results and these 16 bits are used in the sin/cos lookup tables. If enabled in config31 writing to this register causes an auto-sync to be generated. This loads the values of the Qfine mixer block registers (config18, config20, and config21) at the same time. When updating the mixer values the config18 should be written last. Programming config20 and config21 will not affect the mixer settings. | 0x0000 |

Register name: config19 – Address: 0x13, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config19 | 0x13 | 15:0 | Reserved | Reserved for factory use. | 0x0000 |

Register name: config20 – Address: 0x14, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|--|---------------|
| config20 | 0x14 | 15:0 | phase_add(15:0) | The phase_add(15:0) value is used to determine the NCO frequency. The two's complement formatted value can be positive or negative. Each LSB represents $F_s/(2^{32})$ frequency step. | 0x0000 |

Register name: config21 – Address: 0x15, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|------------------|----------------------------|---------------|
| config21 | 0x15 | 15:0 | phase_add(31:16) | See <i>config20</i> above. | 0x0000 |

Register name: config22 – Address: 0x16, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config22 | 0x16 | 15:0 | Reserved | Reserved for factory use. | 0x0000 |

Register name: config23 – Address: 0x17, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config23 | 0x17 | 15:0 | Reserved | Reserved for factory use. | 0x0000 |

Register name: config24 – Address: 0x18, Default: NA

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|------------------|---|---------------|
| config24 | 0x18 | 15:13 | Reserved | Reserved for factory use. | 001 |
| | | 12 | pll_reset | When set, the PLL loop filter (LPF) is pulled down to 0V. Toggle from '1' to '0' to restart the PLL if an over-speed lock-up occurs. Over-speed can happen when the process is fast, the supplies are higher than nominal, etc. resulting in the feedback dividers missing a clock. | 0 |
| | | 11 | pll_ndivsync_ena | When set, the LVDS SYNC input is used to sync the PLL N dividers. | 1 |
| | | 10 | pll_ena | When set, the PLL is enabled. When cleared, the PLL is bypassed. | 0 |
| | | 9:8 | Reserved | Reserved for factory use. | 00 |
| | | 7:6 | pll_cp(1:0) | PLL pump charge select 00: No charge pump 01: Single pump charge 10: Not used 11: Dual pump charge | 00 |
| | | 5:3 | pll_p(2:0) | PLL pre-scaler dividing module control. 010: 2 011: 3 100: 4 101: 5 110: 6 111: 7 000: 8 | 001 |
| | | 2:0 | pll_lfvolt(2:0) | PLL loop filter voltage. This three bit read-only indicator has step size of 0.4125V. The entire range covers from 0V to 3.3V. The optimal lock range of the PLL will be from 010 to 101 (i.e. 0.825V to 2.063V). Adjust pll_vco(5:0) for optimal lock range. | NA |

Register name: config25 – Address: 0x19, Default: 0x0440

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-------------------|--|---------------|
| config25 | 0x19 | 15:8 | pll_m(7:0) | M portion of the M/N divider of the PLL. If pll_m<7> = 0, the M divider value has the range of pll_m<6:0>, spanning from 4 to 127. (i.e. 0, 1, 2, and 3 are not valid.) If pll_m<7> = 1, the M divider value has the range of 2 × pll_m<6:0>, spanning from 8 to 254. (i.e. 0, 2, 4, and 6 are not valid. M divider has even values only.) | 00000100 |
| | | 7:4 | pll_n(3:0) | N portion of the M/N divider of the PLL. 0000: 1 0001: 2 0010: 3 0011: 4 0100: 5 0101: 6 0110: 7 0111: 8 1000: 9 1001: 10 1010: 11 1011: 12 1100: 13 1101: 14 1110: 15 1111: 16 | 0100 |
| | | 3:2 | pll_vcoitune(1:0) | PLL VCO bias tuning bits. Set to "01" for normal PLL operation. | 00 |
| | | 1:0 | Reserved | Reserved for factory use. | 00 |

Register name: config26 – Address: 0x1A, Default: 0x0020

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|---------------|--|---------------|
| config26 | 0x1A | 15:10 | pll_vco(5:0) | VCO frequency coarse tuning bits. | 000000 |
| | | 9 | Reserved | Reserved for factory use. | 0 |
| | | 8 | Reserved | Reserved for factory use. | 0 |
| | | 7 | bias_sleep | When set, the bias amplifier is put into sleep mode. | 0 |
| | | 6 | tsense_sleep | Turns off the temperature sensor when asserted. | 0 |
| | | 5 | pll_sleep | When set, the PLL is put into sleep mode. | 1 |
| | | 4 | clkrecv_sleep | When asserted the clock input receiver gets put into sleep mode. This affects the OSTR receiver as well. | 0 |
| | | 3 | Reserved | Reserved for factory use. | 0 |
| | | 2 | Reserved | Reserved for factory use. | 0 |
| | | 1 | Reserved | Reserved for factory use. | 0 |
| | | 0 | Reserved | Reserved for factory use. | 0 |

Register name: config27 – Address: 0x1B, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value | | |
|---------------|---------|---------------------------------|------------|---|--------------------|---------------------------------|--------|
| config27 | 0x1B | 15 | extref_ena | Allows the device to use an external reference or the internal reference. 0: Internal reference 1: External reference | 0 | | |
| | | 14 | Reserved | Reserved for factory use. | 0 | | |
| | | 13 | Reserved | Reserved for factory use. | 0 | | |
| | | 12 | Reserved | Reserved for factory use. | 0 | | |
| | | 11 | fuse_sleep | Puts the fuses to sleep when set high. Note: Default value is '0'. Must be set to '1' for proper operation | 0 | | |
| | | 10 | Reserved | Reserved for factory use. | 0 | | |
| | | 9 | Reserved | Reserved for factory use. | 0 | | |
| | | 8 | Reserved | Reserved for factory use. | 0 | | |
| | | 7 | Reserved | Reserved for factory use. | 0 | | |
| | | 6 | Reserved | Reserved for factory use. | 0 | | |
| | | 5:0 | atest | ATEST mode allows the user to check for the internal die voltages to ensure the supply voltages are within the range. When ATEST mode is programmed, the internal die voltages can be measured at the TXENABLE pin. The TXENABLE pin (A32 for DAC3482IRKD and N9 for DAC3482IZAY) must be floating without any pull-up or pull-down resistors. In ATEST mode, the TXENABLE and sif_txenable logics are bypassed, and output will be active at all time. | | | 000000 |
| | | Config27, bit<5:0> | | | Description | Expected Nominal Voltage | |
| | | 001110 | | | DACA AVSS | 0V | |
| | | 001111 | | | DACA DVDD | 1.2V | |
| | | 010000 | | | DACA AVDD | 3.3V | |
| | | 010110 | | | DACB AVSS | 0V | |
| | | 010111 | | | DACB DVDD | 1.2V | |
| | | 011000 | | | DACB AVDD | 3.3V | |
| | | 011110 | | | DACC AVSS | 0V | |
| | | 011111 | | | DACC DVDD | 1.2V | |
| 100000 | | | DACC AVDD | 3.3V | | | |
| 100110 | | | DACD AVSS | 0V | | | |
| 100111 | | | DACD DVDD | 1.2V | | | |
| 101000 | | | DACD AVDD | 3.3V | | | |
| 110000 | | | 1.2VDIG | 1.2V | | | |
| 000101 | | | 1.2VCLK | 1.2V | | | |

Register name: config28 – Address: 0x1C, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config28 | 0x1C | 15:8 | Reserved | Reserved for factory use. | 0x00 |
| | | 7:0 | Reserved | Reserved for factory use. | 0x00 |

Register name: config29 – Address: 0x1D, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config29 | 0x1D | 15:8 | Reserved | Reserved for factory use. | 0x00 |
| | | 7:0 | Reserved | Reserved for factory use. | 0x00 |

Register name: config30 – Address: 0x1E, Default: 0x1111

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-----------------------|--|---------------|
| config30 | 0x1E | 15:12 | syncsel_qmoffset(3:0) | Selects the syncing source(s) of the double buffered QMC offset registers. A '1' in the bit enables the signal as a sync source. More than one sync source is permitted. Bit 15: sif_sync (via config31) Bit 14: SYNC Bit 13: OSTR Bit 12: Auto-sync from register write | 0001 |
| | | 11:8 | Reserved | Reserved for factory use. | 0001 |
| | | 7:4 | syncsel_qmcorr(3:0) | Selects the syncing source(s) of the double buffered QMC correction registers. A '1' in the bit enables the signal as a sync source. More than one sync source is permitted. Bit 7: sif_sync (via config31) Bit 6: SYNC Bit 5: OSTR Bit 4: Auto-sync from register write | 0001 |
| | | 3:0 | Reserved | Reserved for factory use. | 0001 |

Register name: config31 – Address: 0x1F, Default: 0x1140

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-----------------------|---|---------------|
| config31 | 0x1F | 15:12 | syncsel_mixer(3:0) | Selects the syncing source(s) of the double buffered mixer registers. A '1' in the bit enables the signal as a sync source. More than one sync source is permitted. Bit 15: sif_sync (via config31) Bit 14: SYNC Bit 13: OSTR Bit 12: Auto-sync from register write | 0001 |
| | | 11:8 | Reserved | Reserved for factory use. | 0001 |
| | | 7:4 | syncsel_nco(3:0) | Selects the syncing source(s) of the two NCO accumulators. A '1' in the bit enables the signal as a sync source. More than one sync source is permitted. Bit 7: sif_sync (via config31) Bit 6: SYNC Bit 5: OSTR Bit 4: FRAME | 0100 |
| | | 3:2 | syncsel_dataformatter | Selects the syncing source of the data formatter. Unlike the other syncs only one sync source is allowed. 00: FRAME 01: SYNC 10: No sync 11: No sync | 00 |
| | | 1 | sif_sync | SIF created sync signal. Set to '1' to cause a sync and then clear to '0' to remove it. | 0 |
| | | 0 | Reserved | Reserved for factory use. | 0 |

Register name: config32 – Address: 0x20, Default: 0x2400

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|-----------------------|---|---------------|
| config32 | 0x20 | 15:12 | syncsel_fifo_in(3:0) | Selects the syncing source(s) of the FIFO input side. A '1' in the bit enables the signal as a sync source. More than one sync source is permitted. Bit 15: sif_sync (via <i>config31</i>) Bit 14: Always zero Bit 13: FRAME Bit 12: SYNC | 0010 |
| | | 11:8 | syncsel_fifo_out(3:0) | Selects the syncing source(s) of the FIFO output side. A '1' in the bit enables the signal as a sync source. More than one sync source is permitted. Bit 11: sif_sync (via <i>config31</i>) Bit 10: OSTR – Dual Sync Sources Mode Bit 9: FRAME – Single Sync Source mode Bit 8: SYNC – Single Sync Source mode | 0100 |
| | | 7:1 | Reserved | Reserved for factory use. | 0000 |
| | | 0 | clkdiv_sync_sel | Selects the signal source for clock divider synchronization. | 0 |
| | | | | clkdiv_sync_sel | |
| | | | | 0 | |
| | | | | 1 | |
| | | | | FRAME, SYNC, or SIF SYNC based on syncsel_fifo_in source selection (<i>config32</i> , bit<15:12>) | |

Register name: config33 – Address: 0x21, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|----------|---------------------------|---------------|
| config33 | 0x21 | 15:0 | Reserved | Reserved for factory use. | 0x0000 |

Register name: config34 – Address: 0x22, Default: 0x1B1B

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|----------|---------------------------|---------------|
| config34 | 0x22 | 15:14 | Reserved | Reserved for factory use. | 00 |
| | | 13:12 | Reserved | Reserved for factory use. | 01 |
| | | 11:10 | Reserved | Reserved for factory use. | 10 |
| | | 9:8 | Reserved | Reserved for factory use. | 11 |
| | | 7:6 | Reserved | Reserved for factory use. | 00 |
| | | 5:4 | Reserved | Reserved for factory use. | 01 |
| | | 3:2 | Reserved | Reserved for factory use. | 10 |
| | | 1:0 | Reserved | Reserved for factory use. | 11 |

Register name: config35 – Address: 0x23, Default: 0xFFFF

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|------------------|--|---------------|
| config35 | 0x23 | 15:0 | sleep_cntl(15:0) | Controls the routing of the CMOS SLEEP signal (pin B40) to different blocks. When a 0xFFFF bit in this register is set, the SLEEP signal will be sent to the corresponding block. The block will only be disabled when the SLEEP is logic HIGH and the correspond bit is set to "1". These bits do not override SIF bits in register <i>config26</i> that control the same sleep function. | 0xFFFF |
| | | | | sleep_cntl(bit) | |
| | | | | 15 | |
| | | | | 14 | |
| | | | | 13 | |
| | | | | 12 | |
| | | | | 11 | |
| | | | | 10 | |
| | | | | 9 | |
| | | | | 8 | |
| | | | | 7 | |
| | | | | 6 | |
| | | | | 5 | |
| | | | | All others | |
| | | | | reserved | |
| | | | | DACI sleep | |
| | | | | DACQ sleep | |
| | | | | reserved | |
| | | | | Clock receiver sleep | |
| | | | | PLL sleep | |
| | | | | LVDS data sleep | |
| | | | | LVDS control sleep | |
| | | | | Temp sensor sleep | |
| | | | | reserved | |
| | | | | Bias amplifier sleep | |
| | | | | not used | |

Register name: config36 – Address: 0x24, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|--------------|---|---------------|
| config36 | 0x24 | 15:13 | datadly(2:0) | Controls the delay of the data inputs through the LVDS receivers. Each LSB adds approximately 50 ps 0: Minimum | 000 |
| | | 12:10 | clkdlly(2:0) | Controls the delay of the data clock through the LVDS receivers. Each LSB adds approximately 50 ps 0: Minimum | 000 |
| | | 9:0 | Reserved | Reserved for factory use. | 0x000 |

Register name: config37 – Address: 0x25, Default: 0x7A7A

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config37 | 0x25 | 15:0 | iotest_pattern0 | Dataword0 in the IO test pattern. It is used with the seven other words to test the input data. At the start of the IO test pattern, this word should be aligned with rising edge of FRAME or SYNC signal to indicate sample 0. | 0x7A7A |

Register name: config38 – Address: 0x26, Default: 0xB6B6

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config38 | 0x26 | 15:0 | iotest_pattern1 | Dataword1 in the IO test pattern. It is used with the seven other words to test the input data. | 0xB6B6 |

Register name: config39 – Address: 0x27, Default: 0xEAEA

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config39 | 0x27 | 15:0 | iotest_pattern2 | Dataword2 in the IO test pattern. It is used with the seven other words to test the input data. | 0xEAEA |

Register name: config40 – Address: 0x28, Default: 0x4545

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config40 | 0x28 | 15:0 | iotest_pattern3 | Dataword3 in the IO test pattern. It is used with the seven other words to test the input data. | 0x4545 |

Register name: config41 – Address: 0x29, Default: 0x1A1A

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config41 | 0x29 | 15:0 | iotest_pattern4 | Dataword4 in the IO test pattern. It is used with the seven other words to test the input data. | 0x1A1A |

Register name: config42 – Address: 0x2A, Default: 0x1616

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config42 | 0x2A | 15:0 | iotest_pattern5 | Dataword5 in the IO test pattern. It is used with the seven other words to test the input data. | 0x1616 |

Register name: config43 – Address: 0x2B, Default: 0xAAAA

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config43 | 0x2B | 15:0 | iotest_pattern6 | Dataword6 in the IO test pattern. It is used with the seven other words to test the input data. | 0xAAAA |

Register name: config44 – Address: 0x2C, Default: 0xC6C6

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|---|---------------|
| config44 | 0x2C | 15:0 | iotest_pattern7 | Dataword7 in the IO test pattern. It is used with the seven other words to test the input data. | 0xC6C6 |

Register name: config45 – Address: 0x2D, Default: 0x0004

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|---------------|--|----------------------|
| config45 | 0x2D | 15 | Reserved | Reserved for factory use. | 0 |
| | | 14 | ostrtodig_sel | When set, the OSTR signal is passed directly to the digital block. This is the signal that is used to clock the dividers. | 0 |
| | | 13 | ramp_ena | When set, a ramp signal is inserted in the input data at the FIFO input. | 0 |
| | | 12:1 | Reserved | Reserved for factory use. | 0000 0000 0010 |
| | | 0 | sifdac_ena | When set, the DAC output is set to the value in sifdac(15:0) in register config48. In this mode, sif_txena in config3 and TXENABLE inputs are ignored. | 0 |

Register name: config46 – Address: 0x2E, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|--|---------------|
| config46 | 0x2E | 15:8 | Reserved | Reserved for factory use. | 0x00 |
| | | 7:0 | grp_delayl(7:0) | Sets the group delay function for DACI. The maximum delay ranges from 30ps to 100ps and is dependent on DAC sample clock. Contact TI for specific application information. | 0x00 |

Register name: config47 – Address: 0x2F, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|-----------------|--|---------------|
| config47 | 0x2F | 15:8 | grp_delayQ(7:0) | Sets the group delay function for DACQ. The maximum delay ranges from 30ps to 100ps and is dependent on DAC sample clock. Contact T1 for specific application information. | 0x00 |
| | | 7:0 | Reserved | Reserved for factory use. | 0x00 |

Register name: config48 – Address: 0x30, Default: 0x0000

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|------|--------------|---|---------------|
| config48 | 0x30 | 15:0 | sifdac(15:0) | Value sent to the DACs when <i>sifdac_ena</i> is asserted. DATACLK must be running to latch this value into the DACs. The format would be based on <i>twos</i> in register <i>config2</i> . | 0x0000 |

Register name: version– Address: 0x7F, Default: 0x540C (READ ONLY)

| Register Name | Address | Bit | Name | Function | Default Value |
|---------------|---------|-------|----------------|---|---------------|
| version | 0x7F | 15:10 | Reserved | Reserved for factory use. | 010101 |
| | | 9 | Reserved | Reserved for factory use. | 0 |
| | | 8:7 | Reserved | Reserved for factory use. | 00 |
| | | 6:5 | Reserved | Reserved for factory use. | 00 |
| | | 4:3 | deviceid(1:0) | Returns '01' for DAC3482. | 01 |
| | | 2:0 | versionid(2:0) | A hardwired register that contains the version of the chip. | 100 |

DATA INTERFACE

The DAC3482 has a 16-bit LVDS bus that accepts 16-bit I and Q data in either word-wide or byte-wide formats. In word-wide mode data is sent through a 16-bit bus while in byte-wide mode an 8-bit bus is used. The selection between the two modes is done through *16bit_in* in the *config2* register. The LVDS bus inputs in each mode are shown in Table 3.

Table 3. LVDS Bus Input Assignment

| Input Mode | Pins |
|--------------------------|----------|
| Word-wide | D[15..0] |
| Byte-wide ⁽¹⁾ | D[7..0] |

(1) The unused pins can be left floating. For word-by-word parity and IO pattern checker functionality, the pins need to have known logic values for valid functionality.

Data is sampled by the LVDS double data rate (DDR) clock DATACLK. Setup and hold requirements must be met for proper sampling.

For both input bus modes, a sync signal, either FRAME or SYNC, can sync the FIFO read and/or write pointers. In byte-wide mode the sync source is needed to establish the correct sample boundaries.

The sync signal, either FRAME or SYNC, can be either a pulse or a periodic signal where the sync period corresponds to multiples of 8 samples. FRAME or SYNC is sampled by a rising edge in DATACLK. The pulse-width ($t_{\text{FRAME_SYNC}}$) needs to be at least equal to $\frac{1}{2}$ of the DATACLK period.

For both input bus mode, the value in FRAME sampled by the next falling edge in DATACLK can be used as a block parity value. This feature is enabled by setting *frame_parity_ena* in register *config1* to "1". Refer to "Parity Check Test" section for more detail

WORD-WIDE FORMAT

The word-wide format is selected by setting *16bit_in* to "1" in the *config2* register. In this mode the 16-bit data for channels I and Q is word-wide interleaved in the form $I_0, Q_0, I_1, Q_1, \dots$ into the D[15:0] 16-bit bus. Data into the DAC3482 is formatted according to the diagram shown in Figure 52 where index 0 is the data LSB and index 15 is the data MSB.

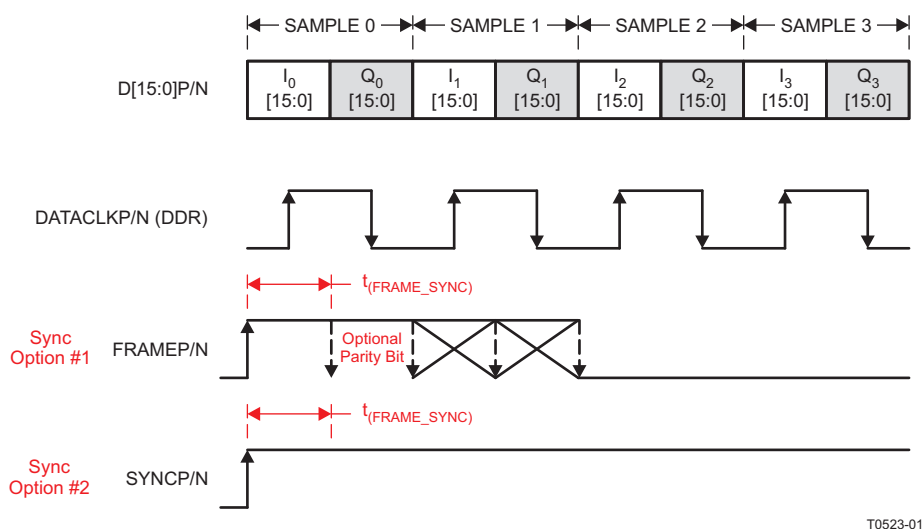


Figure 52. Word-Wide Data Transmission Format

For word-wide format only. The FIFO read and write pointers can also be synced by SIF SYNC as the third option if multi-device synchronization is not needed. In this sync mode, *syncsel_data_formatter(1:0)* in register *config32* can be set to "10" or "11". The *syncsel_fifoin(3:0)* and *syncsel_fifoout(3:0)* in register *config32* need to be both set to "1000" for the SIF SYNC option.

BYTE-WIDE FORMAT

The byte-wide format is selected by setting *16bit_in* to “0” in the *config2* register. In this mode the 16-bit data for channels I and Q is byte-wide interleaved in the form $I_0[15:8]$, $I_0[7:0]$, $Q_0[15:8]$, $Q_0[7:0]$, $I_1[15:8]$, $I_1[7:0]$, $Q_1[15:8]$, $Q_1[7:0]$... into the D[7:0] 8-bit bus. Data into the DAC3482 is formatted according to the diagram shown in Figure 53 where index 0 is the data LSB and index 15 is the data MSB. A rising edge transition of the sync signal, either FRAME or SYNC, is used to establish the correct sample boundaries.

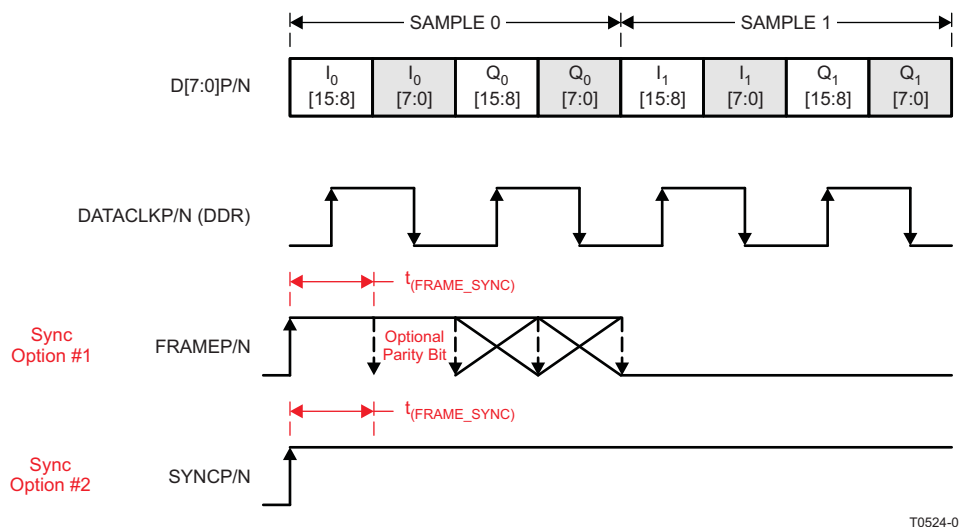
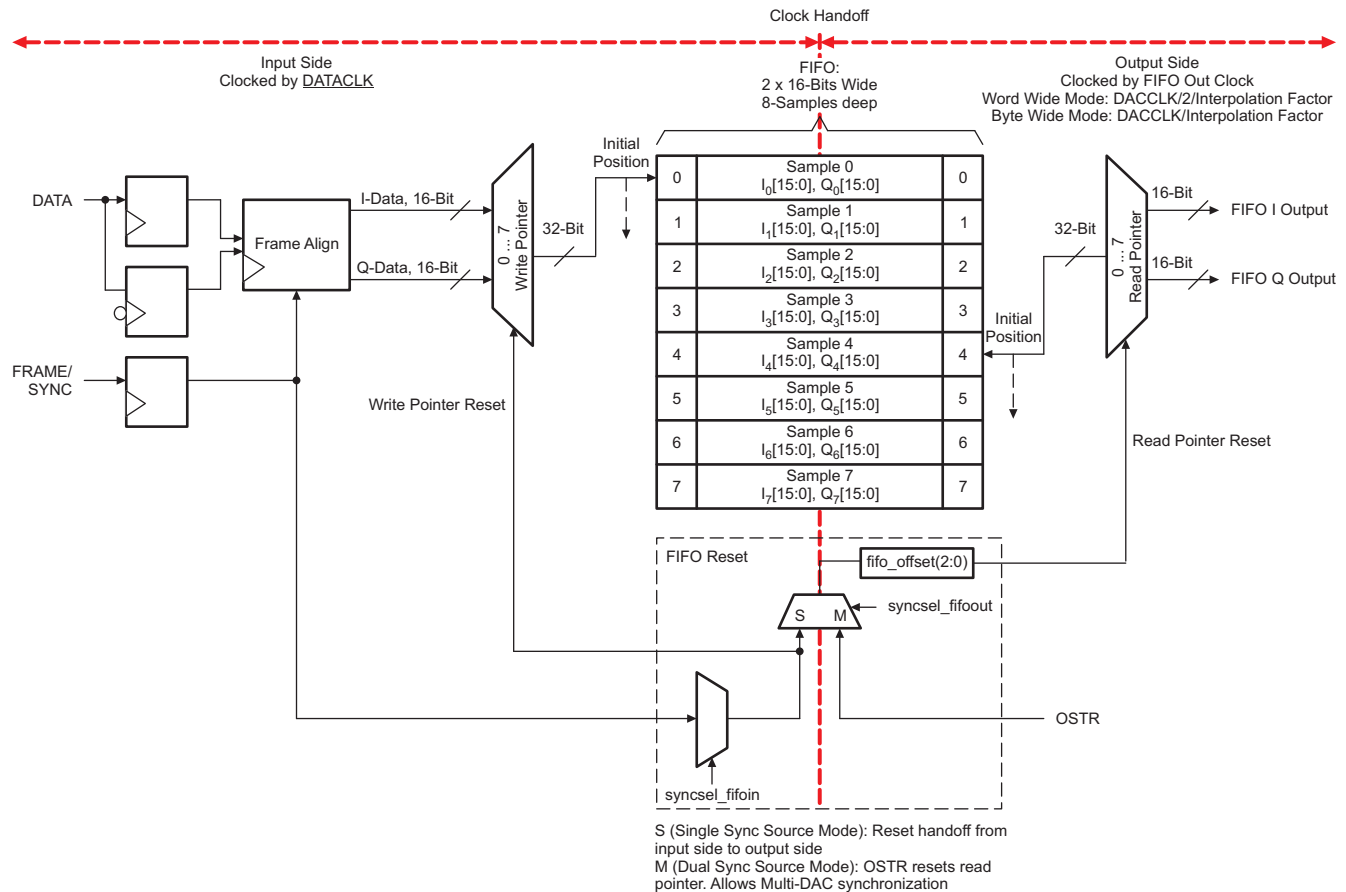


Figure 53. Byte-Wide Data Transmission Format

INPUT FIFO

The DAC3482 includes a 2-channel, 16-bits wide and 8-samples deep input FIFO which acts as an elastic buffer. The purpose of the FIFO is to absorb any timing variations between the input data and the internal DAC data rate clock such as the ones resulting from clock-to-data variations from the data source.

Figure 54 shows a simplified block diagram of the FIFO.



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Figure 54. DAC3482 FIFO Block Diagram

Data is written to the device on the rising and falling edges of DATACLK. Each 32-bit wide sample (16-bit I-data and 16-bit Q-data) is written into the FIFO at the address indicated by the write pointer. Similarly, data from the FIFO is read by the FIFO Out Clock 32-bits at a time from the address indicated by the read pointer. The FIFO Out Clock is generated internally from the DACCLK signal. Its rate is equal to DACCLK/2/Interpolation for word-wide data transmission, or DACCLK/Interpolation for byte-wide data transmission. Each time a FIFO write or FIFO read is done the corresponding pointer moves to the next address.

The reset position for the FIFO read and write pointers is set by default to addresses 0 and 4 as shown in Figure 54. This offset gives optimal margin within the FIFO. The default read pointer location can be set to another value using `fifo_offset(2:0)` in register `config9` (address 4 by default). Under normal conditions data is written-to and read-from the FIFO at the same rate and consequently the write and read pointer gap remains constant. If the FIFO write and read rates are different, the corresponding pointers will be cycling at different speeds which could result in pointer collision. Under this condition the FIFO attempts to read and write data from the same address at the same time which will result in errors and thus must be avoided.

The write pointer sync source is selected by `syncsel_fifoin(3:0)` in register `config32`. In most applications either FRAME or SYNC is used to reset the write pointer. Unlike DATA, the sync signal is latched only on the rising edges of DATACLK. A rising edge on the sync signal source causes the pointer to return to its original position.

Similarly, the read pointer sync source is selected by `syncsel_fifoout(3:0)`. The write pointer sync source can be set to reset the read pointer as well. In this case, the FIFO Out clock will recapture the write pointer sync signal to reset the read pointer. This clock domain transfer (DATACLK to FIFO Out Clock) results in phase ambiguity of the reset signal, and will create latency variation based on the capture edge of the FIFO Out Clock. Since the reset signal also synchronizes the clock divider circuit for the FIFO Out clock generation, the latency variation also includes the capture edge of the DACCLK cycle in the clock divider stage. Ultimately, the variation in capture edge of both the FIFO Out clock and the DACCLK limits the precise control of the output timing latency. The full latency control of the DAC will be difficult and is not recommended in this setup.

NOTE

For full latency control of the DAC, refer to the Dual Sync Source Mode section of the datasheet.

To alleviate this, the device offers the alternative of resetting the FIFO read pointer independently of the write pointer by using the OSTR signal. The OSTR signal is sampled by DACCLK and must satisfy the timing requirements in the specifications table. In order to minimize the skew it is recommended to use the same clock distribution device such as Texas Instruments CDCE62005 to provide the DACCLK and OSTR signals to all the DAC3482 devices in the system. Swapping the polarity of the DACCLK outputs with respect to the OSTR ones establishes proper phase relationship.

The FIFO pointers reset procedure can be done periodically or only once during initialization as the pointers automatically return to the initial position when the FIFO has been filled. To reset the FIFO periodically, the signals to sync the FIFO read and write pointer can repeat at multiples of 8 FIFO samples when the data interface is byte-wide format. When the data interface is word-wide format, the signal to sync the FIFO read and write pointer can repeat at multiples of 16 FIFO samples.

The frequency limitation for FRAME and SYNC signals are the following:

$$f_{\text{sync}} = f_{\text{DATACLK}} / (n \times 16) \text{ where } n = 1, 2, \dots \text{ can repeat multiples of 8 FIFO samples for Byte-Wide Mode}$$

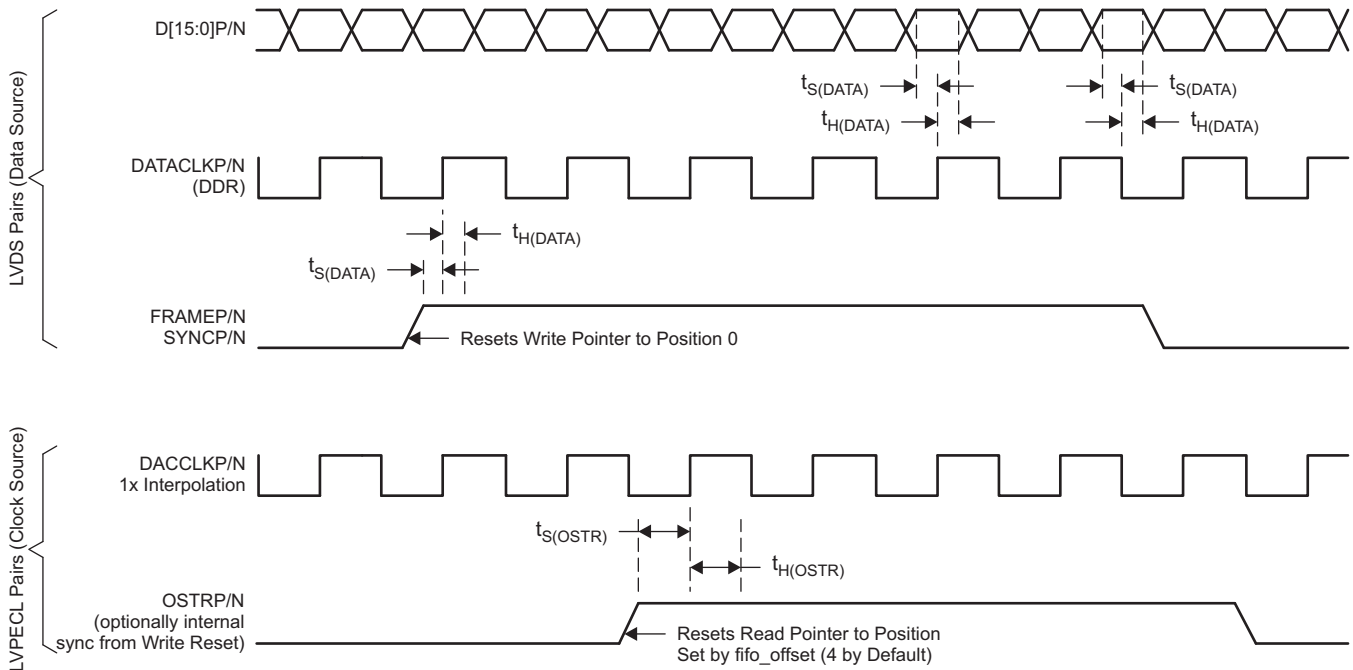
$$f_{\text{sync}} = f_{\text{DATACLK}} / (n \times 16) \text{ where } n = 1, 2, \dots \text{ can repeat multiples of 16 FIFO samples for Word-Wide Mode}$$

The frequency limitation for the OSTR signal is the following:

$$f_{\text{OSTR}} = f_{\text{DAC}} / (n \times \text{interpolation} \times 8) \text{ where } n = 1, 2, \dots \text{ can repeat multiples of 8 FIFO samples for Byte-Wide Mode}$$

$$f_{\text{OSTR}} = f_{\text{DAC}} / (n \times \text{interpolation} \times 16) \text{ where } n = 1, 2, \dots \text{ can repeat multiples of 16 FIFO samples for Word-Wide Mode}$$

The frequencies above are at maximum when $n = 1$. This is when the FRAME, SYNC, or OSTR have a rising edge transition every 8 or 16 FIFO samples. The occurrence can be made less frequent by setting $n > 1$, for example, every $n \times 8$ or $n \times 16$ FIFO samples.



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Figure 55. FIFO Write and Read Descriptions (Example shown with Word-Wide Mode)

FIFO MODES OF OPERATION

The DAC3482 input FIFO can be completely bypassed through registers *config0* and *config32*. The register configuration for each mode is described in [Table 4](#).

| Register | Control Bits |
|-----------------|------------------------------|
| <i>config0</i> | <i>fifo_ena</i> |
| <i>config32</i> | <i>syncsel_fifoout</i> (3:0) |

Table 4. FIFO Operation Modes

| FIFO Mode | config0 and config32 FIFO Bits | | | | |
|--------------------|--------------------------------|------------------------|--------------------|-----------------------------------|-----------------------------------|
| | fifo_ena | syncsel_fifoout | | | |
| | | Bit 3: <i>sif_sync</i> | Bit 2: <i>OSTR</i> | Bit 1: <i>FRAME</i> | Bit 0: <i>SYNC</i> |
| Dual Sync Sources | 1 | 0 | 1 | 0 | 0 |
| Single Sync Source | 1 | 0 | 0 | 1 or 0 Depends on the sync source | 1 or 0 Depends on the sync source |
| Bypass | 0 | X | X | X | X |

DUAL SYNC SOURCES MODE

This is the recommended mode of operation for those applications that require precise control of the output timing. In Dual Sync Sources mode, the FIFO write and read pointers are reset independently. The FIFO write pointer is reset using the LVDS FRAME or SYNC signal, and the FIFO read pointer is reset using the LVPECL OSTR signal. This allows LVPECL OSTR signal to control the phase of the output for either a single chip or multiple chips. Multiple devices can be fully synchronized in this mode.

SINGLE SYNC SOURCE MODE

In Single Sync Source mode, the FIFO write and read pointers are reset from the same source, either LVDS FRAME or LVDS SYNC signal. As described in the “Input FIFO” section, this mode has latency variations in both the FIFO Out clock and DAC clock between the multiple DAC devices. Applications requiring exact output latency control will need Dual Sync Sources mode instead of Single Sync Source mode. A single rising edge for FIFO and clock divider is recommended in this mode. Periodic sync signal is not recommended due to non-deterministic latency of the sync signal through the clock domain transfer.

In this mode, there is a chance for FIFO pointers 2 away alarm (or possibly 1 away alarm) to occur at initial setup/syncing. This is the result of Single Sync Source mode having 0 to 3 address location slip, which is caused by the asynchronous handoff of the sync signal occurring between the DATACLK zone and DACCLK zone. The asynchronous relationship between the clock domains means there could be a slip (from nominal) in the READ and Write pointers at initial syncing. For example, with the default programming of FIFO Offset of 4, the actual FIFO Offset may be 3, 2, or in some instances, 1. Please note that in this mode, the nominal address location slip is 0 with the possibility getting less for each increase in slip amount. Also, the slip does not continue to occur as the device functions, but the READ/WRITE pointers may not be at optimal settings.

In situation of alarm occurrence:

1. Adjust the FIFO offset accordingly and resynchronize the FIFO, data formatter, etc such that there are no alarm reported or at least only 2 away alarm is reported
2. The FIFO collision alarm is a warning of the system since the read and write processes occur at the same pointer. However, the FIFO 1 away or 2 away alarms are informational for the system designer. The important thing for these two alarms is that the alarm should not get closer to collision during normal operation. If 1 away alarm and alarm collision starts to occur, it is a warning to check for system errors. The system should have an interrupt or algorithm to fix the error and resynchronize the alarm appropriately.

BYPASS MODE

In FIFO bypass mode, the FIFO block is not used. As a result the input data is handed off from the DATACLK to the DACCLK domain without any compensation. In this mode the relationship between DATACLK and DACCLK is critical and used as a synchronizing mechanism for the internal logic. Due to this constraint this mode is not recommended. The effects of bypassing the FIFO are the following:

1. The FIFO pointers have no effect on the data path or handoff.
2. The FIFO will not be able to pass the controls signals from the LVDS FRAME and LVDS SYNC to digital circuits after the FIFO. These digital circuits mainly are quadrature modulation correction circuits, complex mixer circuit, and numerical controlled oscillator circuits.

CLOCKING MODES

The DAC3482 has a dual clock setup in which a DAC clock signal is used to clock the DAC cores and internal digital logic and a separate DATA clock is used to clock the input LVDS receivers and FIFO input. The DAC3482 DAC clock signal can be sourced directly or generated through an on-chip low-jitter phase-locked loop (PLL).

In those applications requiring extremely low noise it is recommended to bypass the PLL and source the DAC clock directly from a high-quality external clock to the DACCLK input. In most applications system clocking can be simplified by using the on-chip PLL to generate the DAC core clock while still satisfying performance requirements. In this case the DACCLK pins are used as the reference frequency input to the PLL.

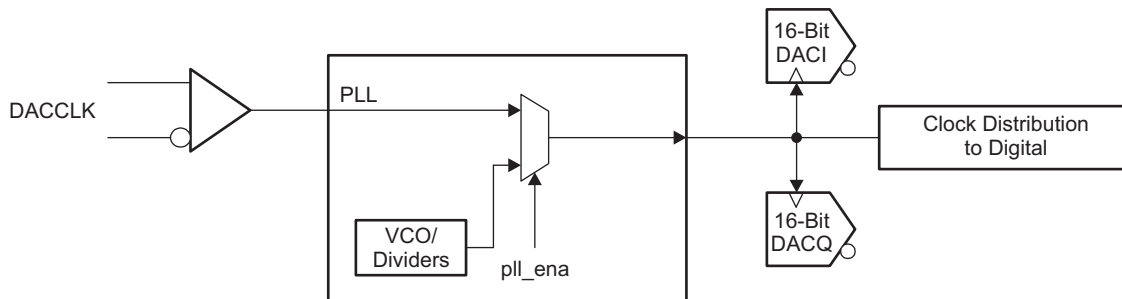


Figure 56. Top Level Clock Diagram

PLL BYPASS MODE

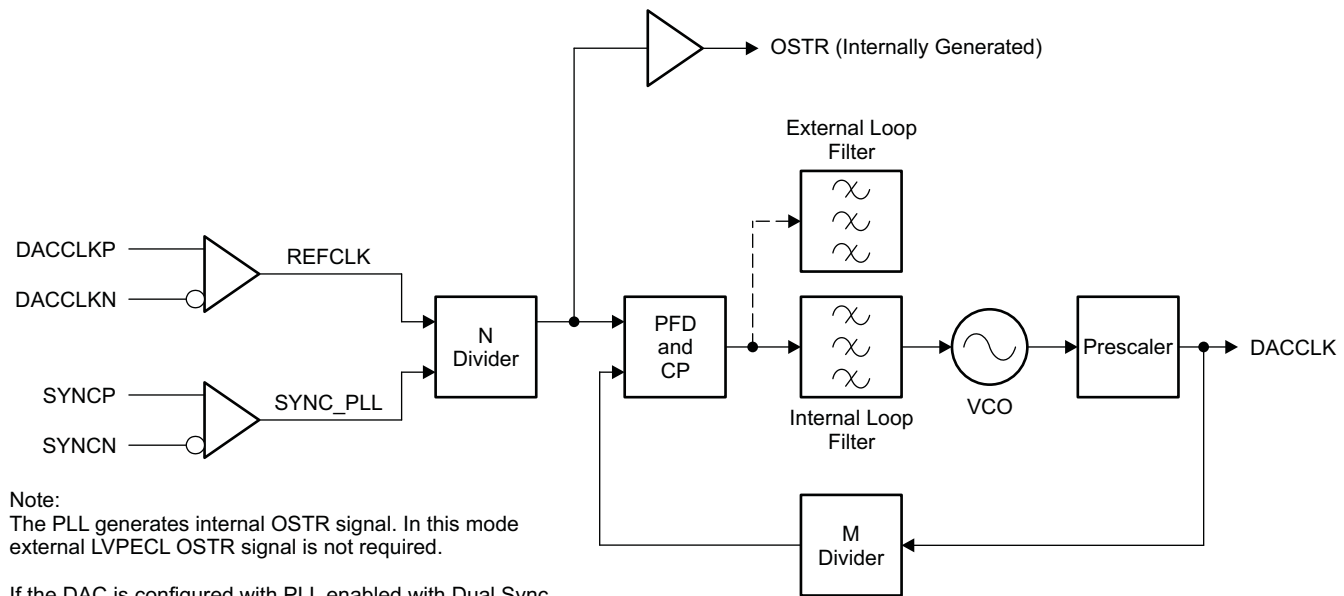
In PLL bypass mode a very high quality clock is sourced to the DACCLK inputs. This clock is used to directly clock the DAC3482 DAC sample rate clock. This mode gives the device best performance and is recommended for extremely demanding applications.

The bypass mode is selected by setting the following:

1. *pll_ena* bit in register *config24* to "0" to bypass the PLL circuitry.
2. *pll_sleep* bit in register *config26* to "1" to put the PLL and VCO into sleep mode.

PLL MODE

In this mode the clock at the DACCLK input functions as a reference clock source to the on-chip PLL. The on-chip PLL will then multiply this reference clock to supply a higher frequency DAC sample rate clock. Figure 57 shows the block diagram of the PLL circuit.



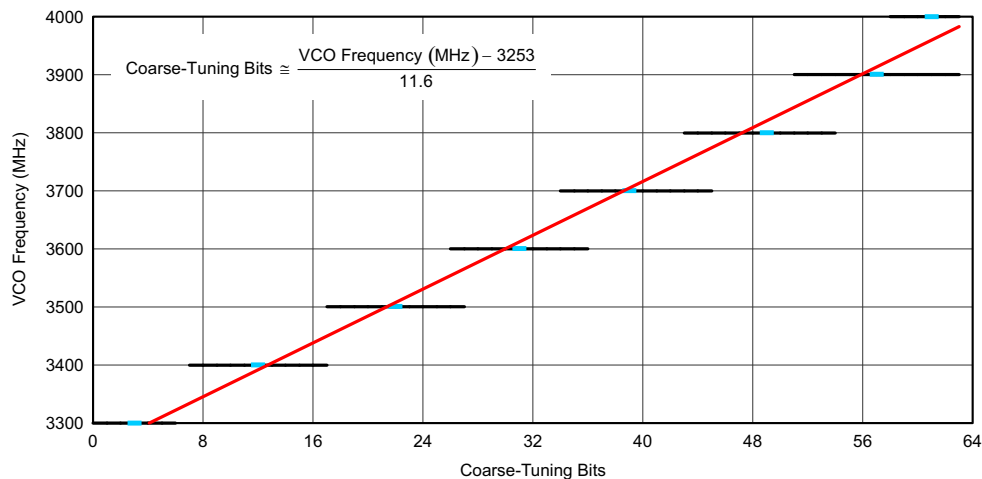
B0453-01

Figure 57. PLL Block Diagram

The DAC3482 PLL mode is selected by setting the following:

1. *pll_ena* bit in register *config24* to "1" to route to the PLL clock path.
2. *pll_sleep* bit in register *config26* to "0" to enable the PLL and VCO.

The output frequency of the VCO is designed to be in the range from 3.3GHz to 4.0GHz. The prescaler value, *pll_p(2:0)* in register *config24*, should be chosen such that the product of the prescaler value and DAC sample rate clock is within the VCO range. To maintain optimal PLL loop, the coarse tune bits, *pll_vco(5:0)* in register *config26*, can adjust the center frequency of the VCO towards the product of the prescaler value and DAC sample rate clock. Figure 58 shows a typical relationship between coarse tune bits and VCO center frequency. For the recommended *pll_vco(5:0)* setting over free-air temperature, refer to Electrical Characteristic – Phased-Locked Loop Specification table for detail.

**Figure 58. Typical PLL/VCO Lock Range vs Coarse Tuning Bits**

If the corresponding pll_vco(5:0) setting and the VCO frequency of interest are not in the Phase-Locked Loop Specification table, TI recommends the use of the typical pll_vco(5:0) value found in [Figure 58](#) along with implementation of PLL lock status check over temperature. The PLL lock status can be read back in pll_lfvolt(2:0) register of config24. If the PLL is out of range, adjust pll_vco(5:0) in config26 accordingly. The example PLL lock status and adjustment algorithm can be found in [Figure 59](#).

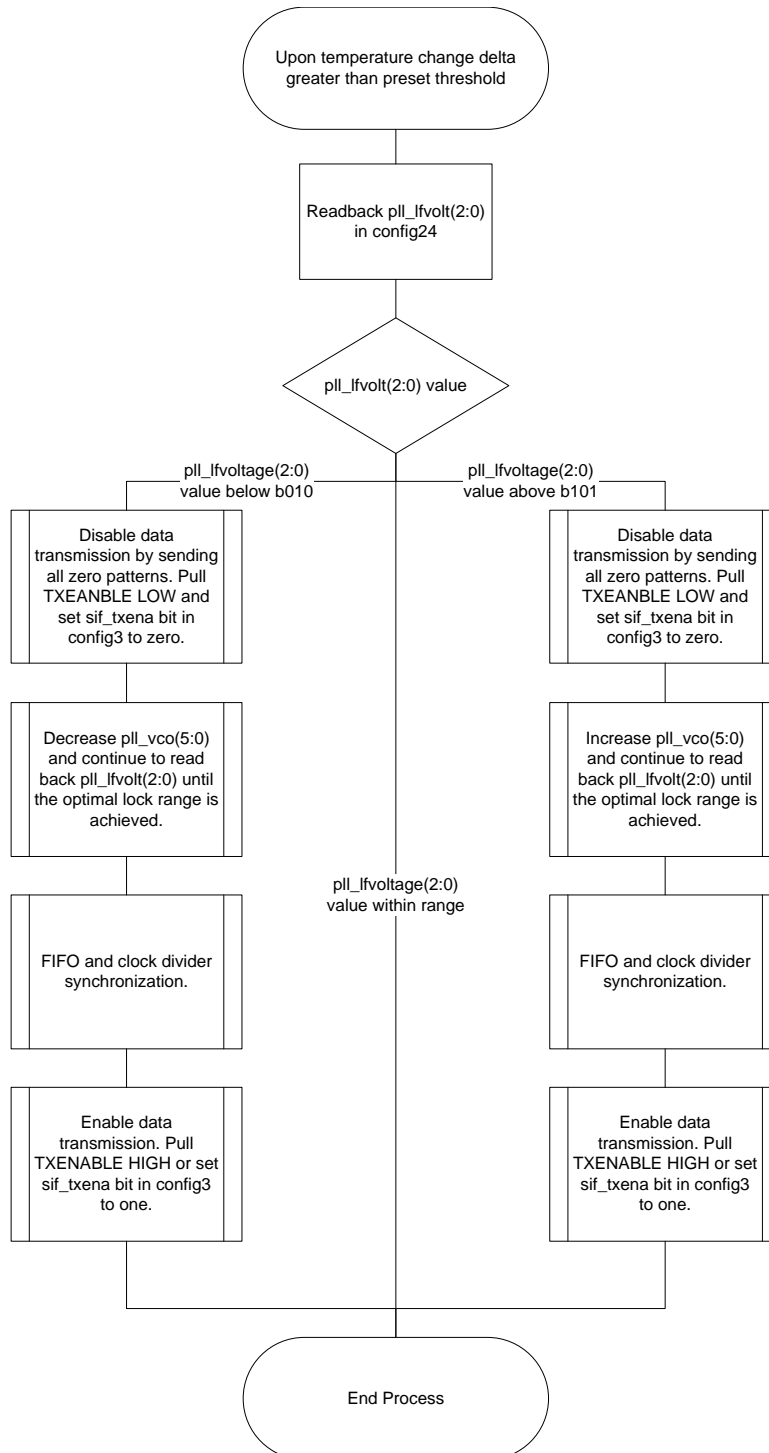


Figure 59. Example PLL Lock Status and Adjustment Algorithm

Common wireless infrastructure frequencies (614.4MHz, 737.28MHz, 983.04MHz, etc.) are generated from this VCO frequency in conjunction with the pre-scaler setting as shown in Table 5.

Table 5. VCO Operation

| VCO Frequency (MHz) | Pre-Scale Divider | Desired DACCLK (MHz) | pll_p(2:0) |
|---------------------|-------------------|----------------------|------------|
| 3932.16 | 8 | 491.52 | 111 |
| 3686.4 | 6 | 614.4 | 110 |
| 3686.4 | 5 | 737.28 | 101 |
| 3932.16 | 4 | 983.04 | 100 |

The M divider is used to determine the phase-frequency-detector (PFD) and charge-pump (CP) frequency.

Table 6. PFD and CP Operation

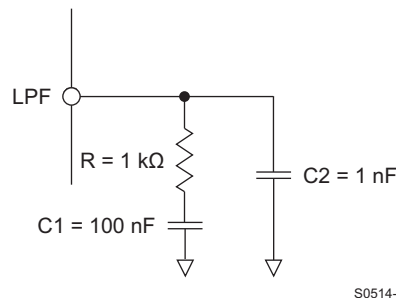
| DACCLK Frequency (MHz) | M Divider | PDF Update Rate (MHz) | pll_m(7:0) |
|------------------------|-----------|-----------------------|------------|
| 491.52 | 4 | 122.88 | 00000100 |
| 491.52 | 8 | 61.44 | 00001000 |
| 491.52 | 16 | 30.72 | 00010000 |
| 491.52 | 32 | 15.36 | 00100000 |

The N divider in the loop allows the PFD to operate at a lower frequency than the reference clock. Both M and N dividers can keep the PFD frequency below 155 MHz for peak operation.

The overall divide ratio inside the loop is the product of the Pre-Scale and M dividers ($P * M$) and the following guidelines should be followed:

- The overall divide ratio range is from 24 to 480
- When the overall divide ratio is less than 120, the internal loop filter can guarantee a stable loop
- When the overall divide ratio is greater than 120, an external loop filter or double charge pump is required to ensure loop stability

The single- and double-charge-pump current option are selected by setting *pll_cp* in register *config24* to 01 and 11, respectively. When using the double-charge-pump setting, an external loop filter is not required. If an external filter is required, the following filter should be connected to the LPF pin (A1):

**Figure 60. Recommended External Loop Filter**

The PLL will generate an internal OSTR signal and does not require the external LVPECL OSTR signal. The OSTR signal is buffered from the N-divider output in the PLL block, and the frequency of the signal is the same as the PFD frequency. Therefore, using PLL with Dual Sync Sources mode requires the PFD frequency to be the pre-defined OSTR frequency listed in Input FIFO section. This will allow the FIFO to be synced correctly by the internal OSTR.

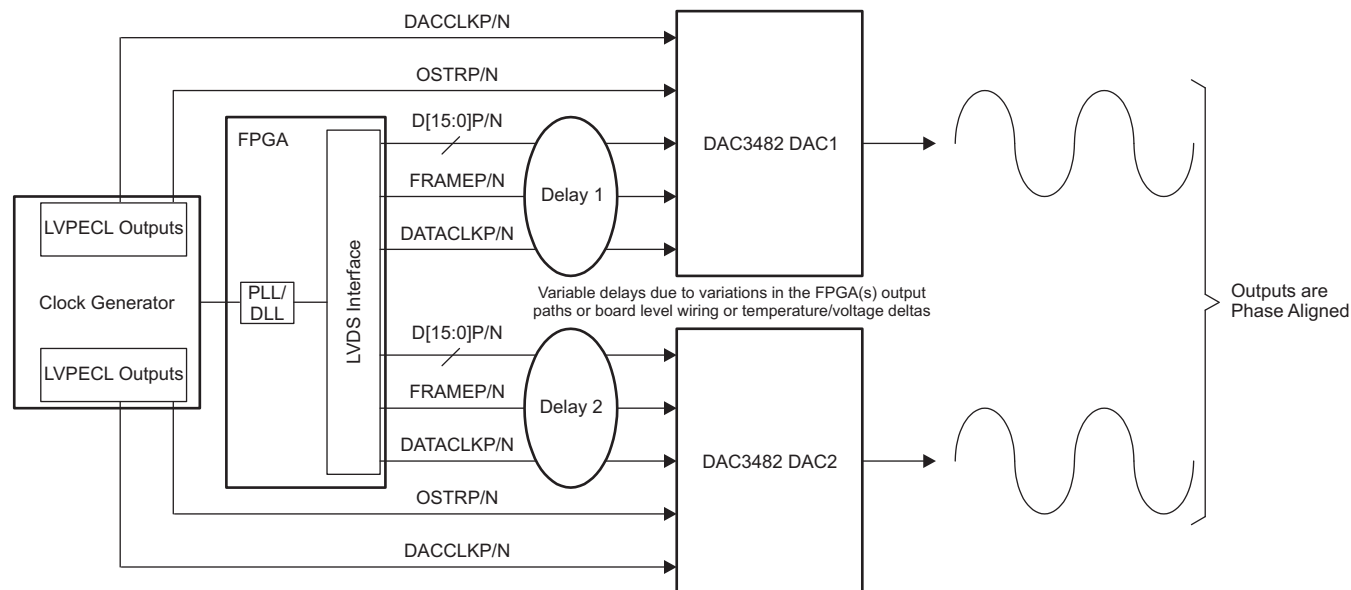
MULTI-DEVICE SYNCHRONIZATION

In various applications, such as multi antenna systems where the various transmit channels information is correlated, it is required that multiple DAC devices are completely synchronized such that their outputs are phase aligned. The DAC3482 architecture supports this mode of operation.

MULTI-DEVICE SYNCHRONIZATION: PLL BYPASSED WITH DUAL SYNC SOURCES MODE

For single or multi-device synchronization it is important that delay differences in the data are absorbed by the device so that latency through the device remains the same. Furthermore, to guarantee that the outputs from each DAC are phase aligned it is necessary that data is read from the FIFO of each device simultaneously. In the DAC3482 this is accomplished by operating the multiple devices in Dual Sync Sources mode. In this mode the additional OSTR signal is required by each DAC3482 to be synchronized.

Data into the device is input as LVDS signals from one or multiple baseband ASICs or FPGAs. Data into the multiple DAC devices can experience different delays due to variations in the digital source output paths or board level wiring. These different delays can be effectively absorbed by the DAC3482 FIFO so that all outputs are phase aligned correctly.

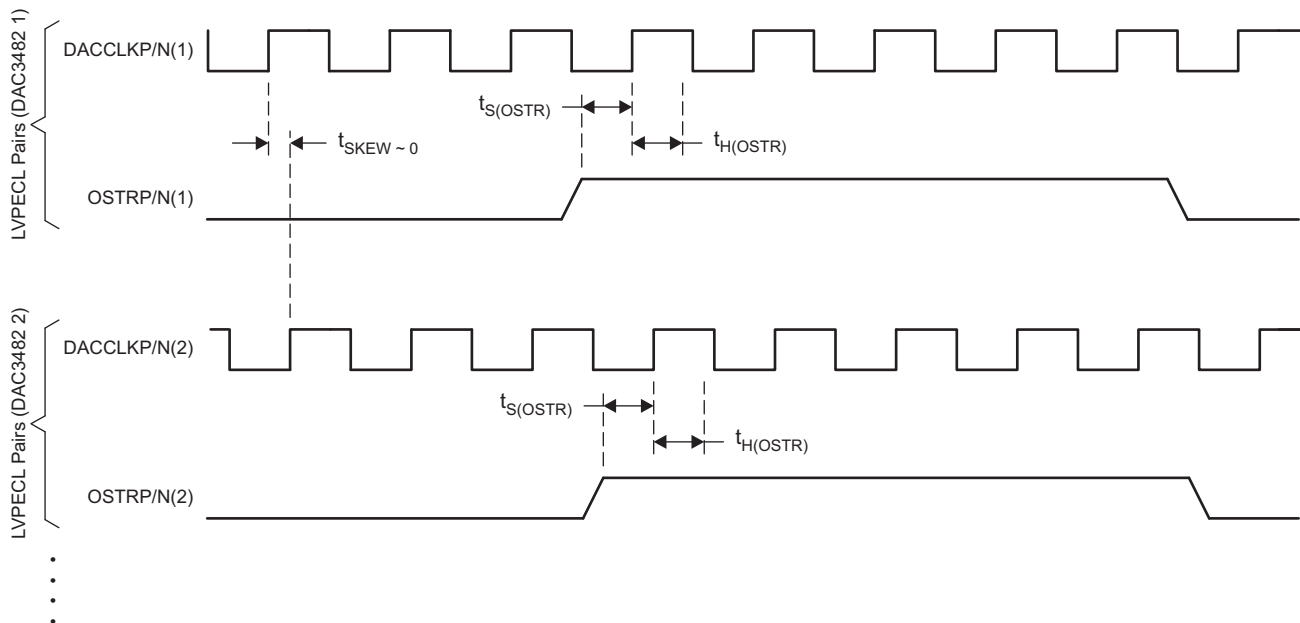


B0454-01

Figure 61. Synchronization System in Dual Sync Sources Mode with PLL Bypassed

For correct operation both OSTR and DACCLK must be generated from the same clock domain. The OSTR signal is sampled by DACCLK and must satisfy the timing requirements in the specifications table. If the clock generator does not have the ability to delay the DACCLK to meet the OSTR timing requirement, the polarity of the DACCLK outputs can be swapped with respect to the OSTR ones to create 180 degree phase delay of the DACCLK. This may help establish proper setup and hold time requirement of the OSTR signal.

Careful board layout planning must be done to ensure that the DACCLK and OSTR signals are distributed from device to device with the lowest skew possible as this will affect the synchronization process. In order to minimize the skew across devices it is recommended to use the same clock distribution device to provide the DACCLK and OSTR signals to all the DAC devices in the system.



T0526-01

Figure 62. Timing Diagram for LVPECL Synchronization Signals

The following steps are required to ensure the devices are fully synchronized. The procedure assumes all the DAC3482 devices have a DACCLK and OSTR signal and must be carried out on each device.

1. Start-up the device as described in the power-up sequence. Set the DAC3482 in Dual Sync Sources mode and select OSTR as the clock divider sync source (*clkdiv_sync_sel* in register *config32*).
2. Sync the clock divider and FIFO pointers.
3. Verify there are no FIFO alarms either through register *config5* or through the ALARM pin.
4. Disable clock divider sync by setting *clkdiv_sync_ena* to "0" in register *config0*.

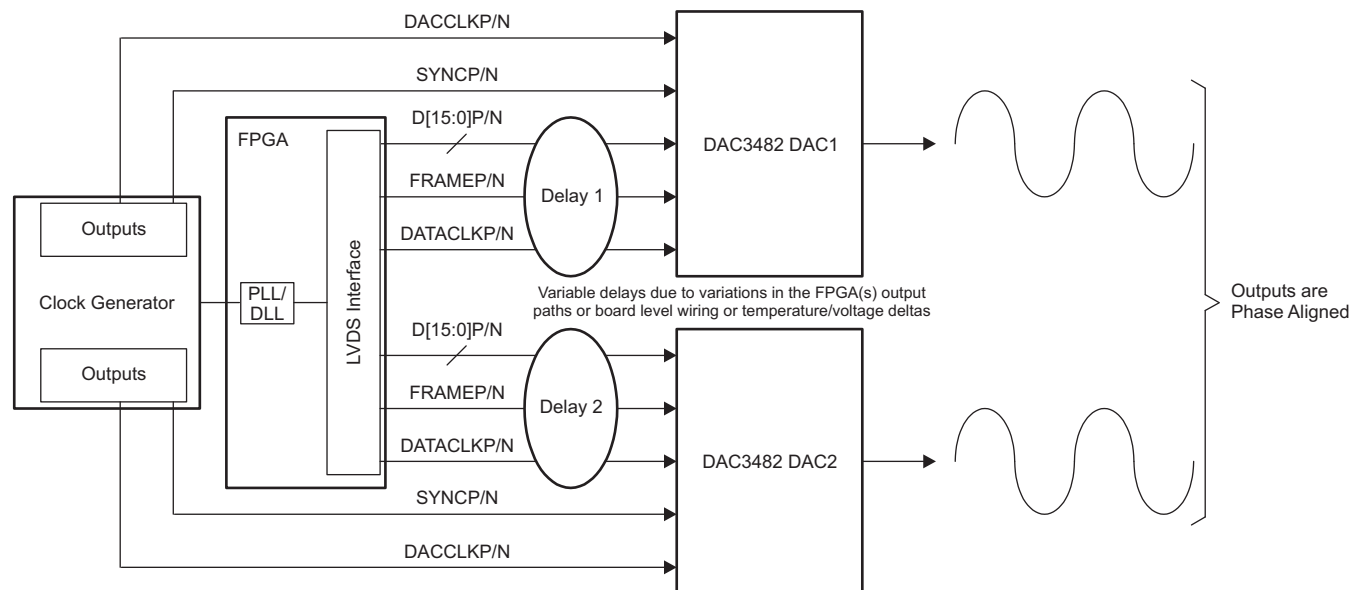
After these steps all the DAC3482 outputs will be synchronized.

MULTI-DEVICE SYNCHRONIZATION: PLL ENABLED WITH DUAL SYNC SOURCES MODE

The DAC3482 allows exact phase alignment between multiple devices even when operating with the internal PLL clock multiplier. In PLL clock mode, the PLL generates the DAC clock and an internal OSTR signal from the reference clock applied to the DACCLK inputs so there is no need to supply an additional LVPECL OSTR signal.

For this method to operate properly the SYNC signal should be set to reset the PLL N dividers to a known state by setting *pll_ndivsync_ena* in register *config24* to "1". The SYNC signal resets the PLL N dividers with a rising edge, and the timing relationship $t_{s(\text{SYNC_PLL})}$ and $t_{h(\text{SYNC_PLL})}$ are relative to the reference clock presented on the DACCLK pin.

Both SYNC and DACCLK can be set as low frequency signals to greatly simplifying trace routing (SYNC can be just a pulse as a single rising edge is required, if using a periodic signal it is recommended to clear the *pll_ndivsync_ena* bit after resetting the PLL dividers). Besides the $t_{s(\text{SYNC_PLL})}$ requirement between SYNC and DACCLK, there is no additional required timing relationship between the SYNC and FRAME signals or between DACCLK and DATACLK. The only restriction as in the PLL disabled case is that the DACCLK and SYNC signals are distributed from device to device with the lowest skew possible.



B0455-01

Figure 63. Synchronization System in Dual Sync Sources Mode with PLL Enabled

The following steps are required to ensure the devices are fully synchronized. The procedure assumes all the DAC3482 devices have a DACCLK and OSTR signal and must be carried out on each device.

1. Start-up the device as described in the power-up sequence. Set the DAC3482 in Dual Sync Sources mode and enable SYNC to reset the PLL dividers (set *pll_ndivsync_ena* in register *config24* to "1").
2. Reset the PLL dividers with a rising edge on SYNC.
3. Disable PLL dividers resetting.
4. Sync the clock divider and FIFO pointers.
5. Verify there are no FIFO alarms either through register *config5* or through the ALARM pin.
6. Disable clock divider sync by setting *clkdiv_sync_ena* to "0" in register *config0*.

After these steps all the DAC3482 outputs will be synchronized.

MULTI-DEVICE OPERATION: SINGLE SYNC SOURCE MODE

In Single Sync Source mode the FIFO read pointer reset is handoff between the two clock domains (DATACLK and FIFO Out clock) by simply re-sampling the write pointer reset. Since the two clocks are asynchronous there is a small but distinct possibility of a meta-stable situation during the pointer handoff. As described in the "Input FIFO" section, this meta-stable situation can change the latency of the multiple DAC devices by both the FIFO Out clock cycles and DAC clock cycles.

When the PLL is enabled with Single Sync Source mode, the FIFO read pointer is not synchronized by the OSTR signal. Therefore, there is no restriction on the PLL PFD frequency as described in the previous section.

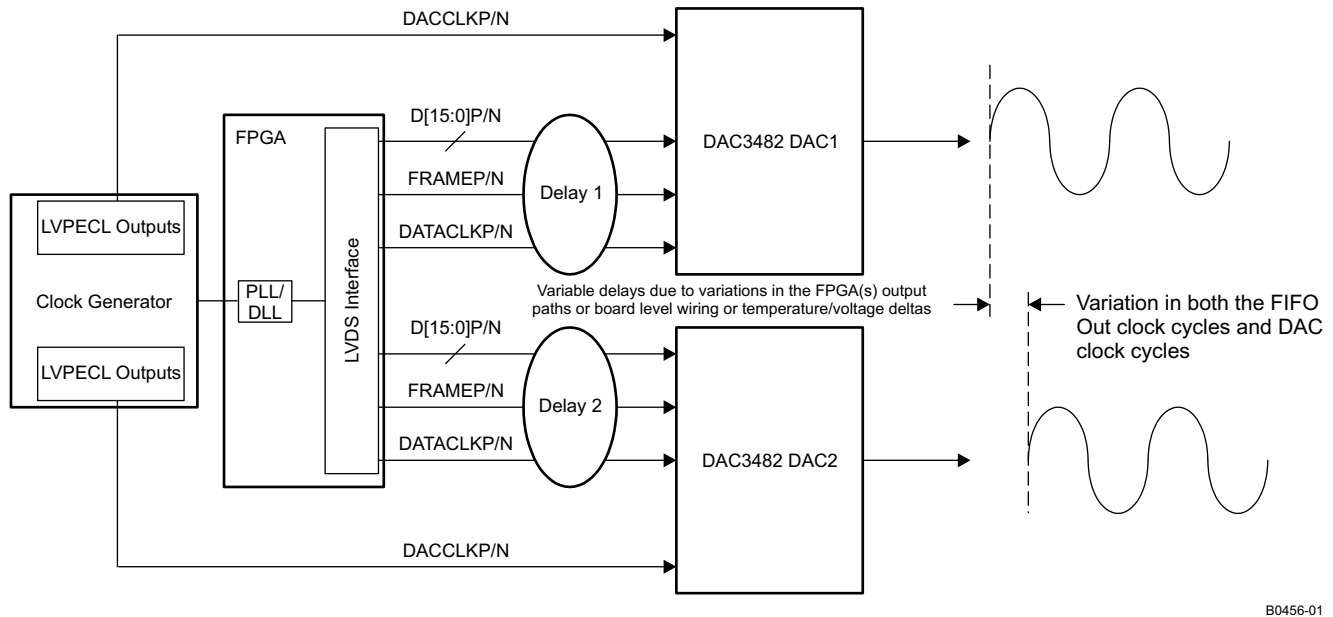


Figure 64. Multi-Device Operation in Single Sync Source Mode

B0456-01

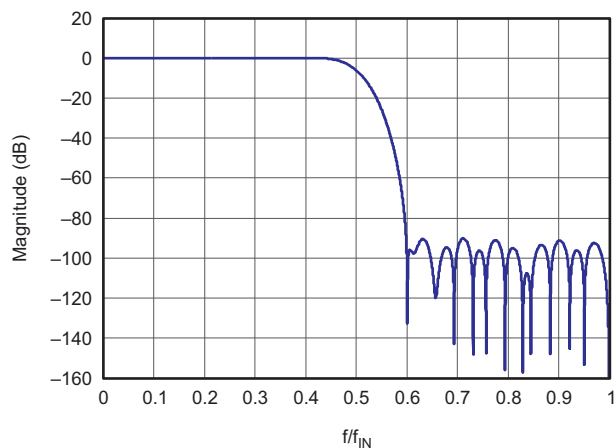
FIR FILTERS

Figure 65 through Figure 68 show the magnitude spectrum response for the FIR0, FIR1, FIR2 and FIR3 interpolating filters where f_{IN} is the input data rate to the FIR filter. Figure 69 to Figure 72 show the composite filter response for 2x, 4x, 8x and 16x interpolation. The transition band for all interpolation settings is from 0.4 to $0.6 \times f_{DATA}$ (the input data rate to the device) with $< 0.001\text{dB}$ of pass-band ripple and $> 90\text{ dB}$ stop-band attenuation.

The DAC3482 also has a 9-tap inverse sinc filter (FIR4) that runs at the DAC update rate (f_{DAC}) that can be used to flatten the frequency response of the sample-and-hold output. The DAC sample-and-hold output sets the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well-known $\sin(x)/x$ or $\text{sinc}(x)$ frequency response (Figure 15, red line). The inverse sinc filter response (Figure 66, blue line) has the opposite frequency response from 0 to $0.4 \times f_{DAC}$, resulting in the combined response (Figure 66, green line). Between 0 to $0.4 \times f_{DAC}$, the inverse sinc filter compensates the sample-and-hold roll-off with less than 0.03 dB error.

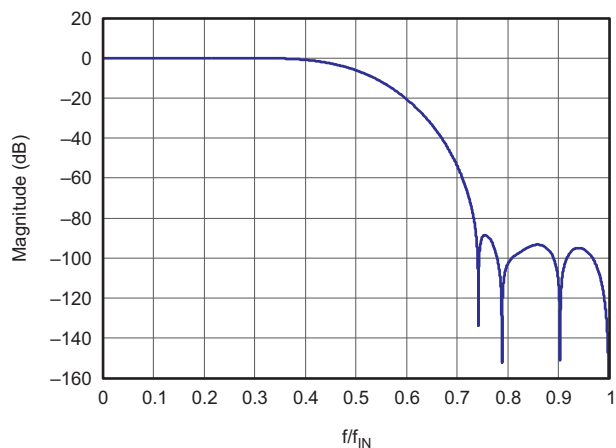
The inverse sinc filter has a gain > 1 at all frequencies. Therefore, the signal input to FIR4 must be reduced from full scale to prevent saturation in the filter. The amount of back-off required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to FIR4 is at $0.25 \times f_{DAC}$, the response of FIR4 is 0.9 dB, and the signal must be backed off from full scale by 0.9 dB to avoid saturation. The gain function in the QMC blocks can be used to reduce the amplitude of the input signal. The advantage of FIR4 having a positive gain at all frequencies is that the user is then able to optimize the back-off of the signal based on its frequency.

The filter taps for all digital filters are listed in Table 4. Note that the loss of signal amplitude may result in lower SNR due to decrease in signal amplitude.



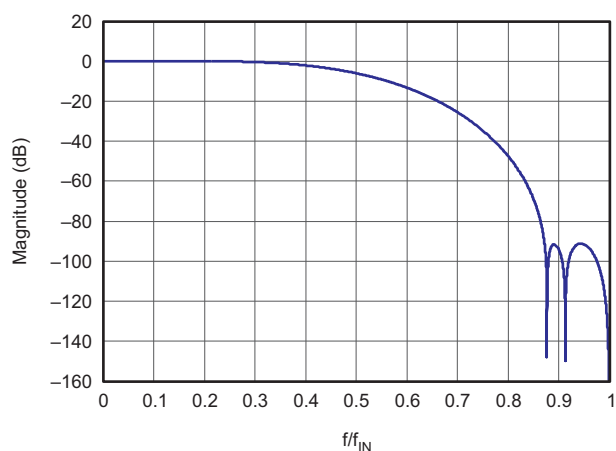
G048

Figure 65. Magnitude Spectrum for FIR0



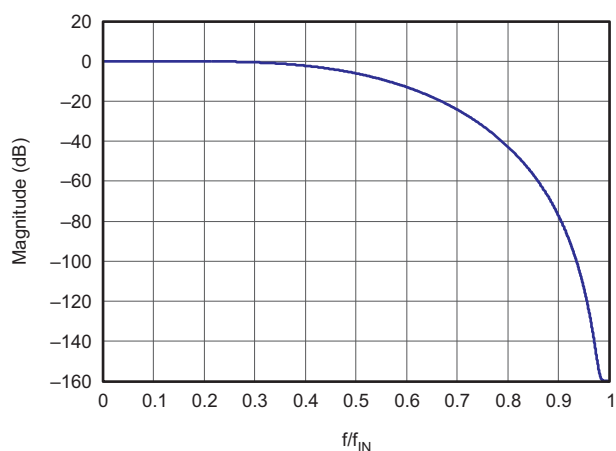
G049

Figure 66. Magnitude Spectrum for FIR1



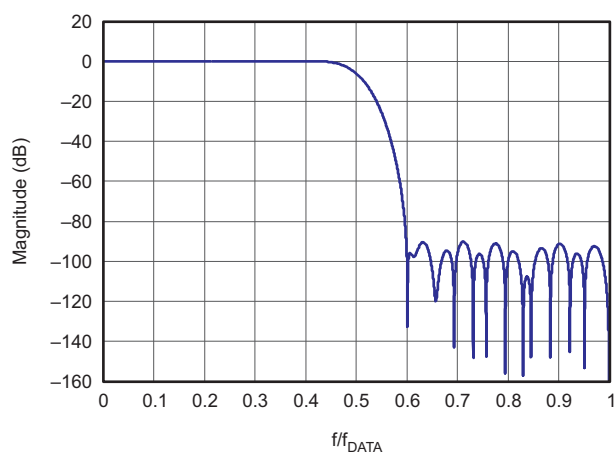
G050

Figure 67. Magnitude Spectrum for FIR2



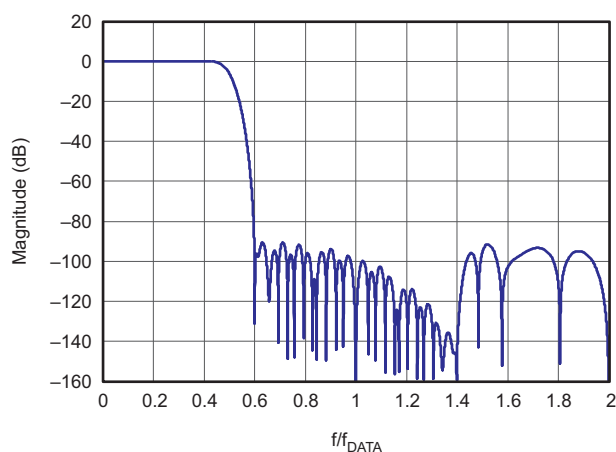
G051

Figure 68. Magnitude Spectrum for FIR3



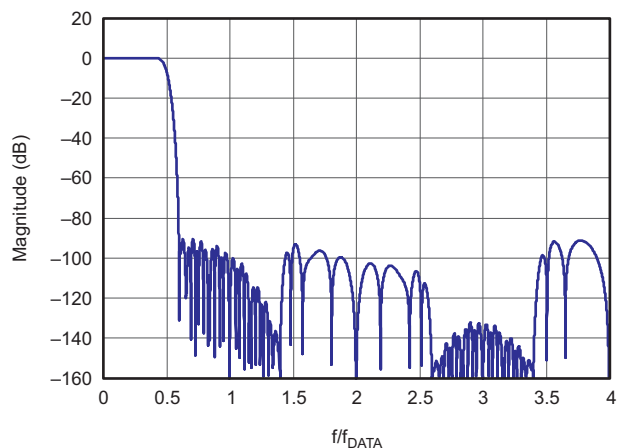
G052

Figure 69. 2x Interpolation Composite Response



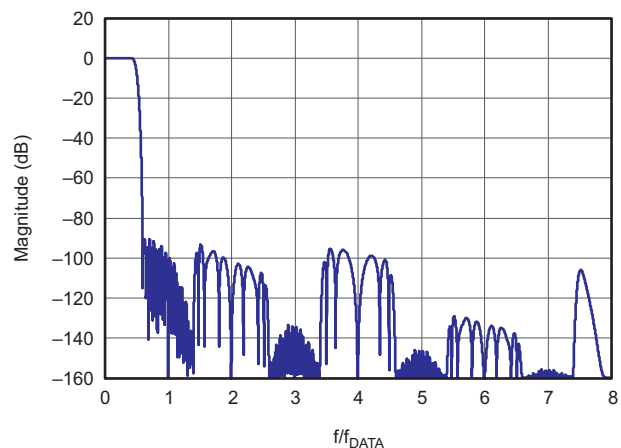
G053

Figure 70. 4x Interpolation Composite Response



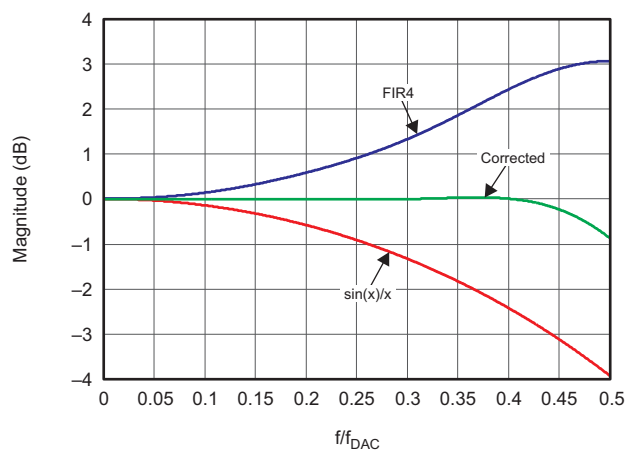
G054

Figure 71. 8x Interpolation Composite Response



G055

Figure 72. 16x Interpolation Composite Response



G056

Figure 73. Magnitude Spectrum for Inverse Sinc Filter

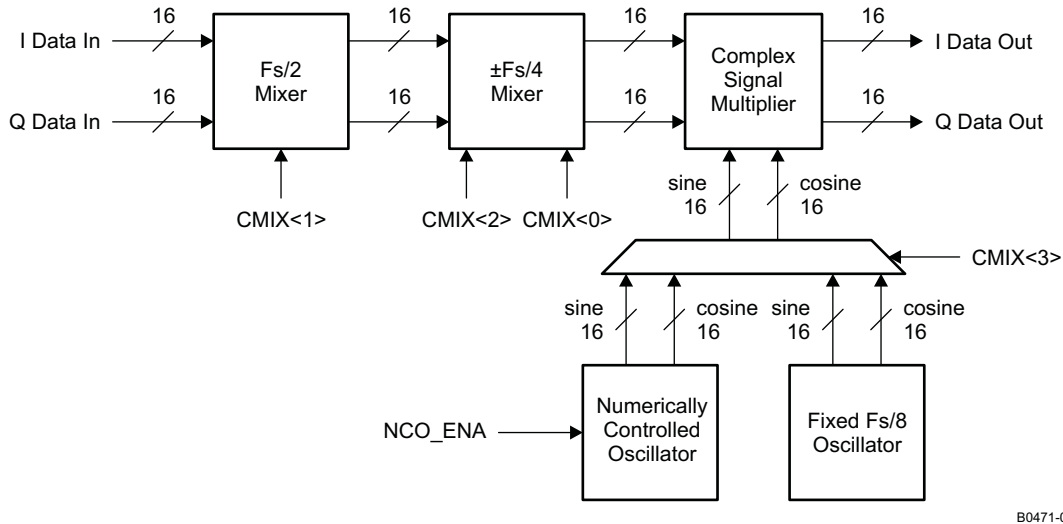
Table 7. FIR Filter Coefficients

| Interpolating Half-band Filters | | | | | | | | Non-Interpolating Inverse-SINC Filter | |
|---------------------------------|--------|----------------------------|-------|---------------------------|------|--------------------------|-----|---------------------------------------|-----|
| FIR0 | | FIR1 | | FIR2 | | FIR3 | | FIR4 | |
| 59 Taps | | 23 Taps | | 11 Taps | | 11 Taps | | 9 Taps | |
| 6 | 6 | -12 | -12 | 29 | 29 | 3 | 3 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -4 | -4 |
| -19 | -19 | 84 | 84 | -214 | -214 | -25 | -25 | 13 | 13 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -50 | -50 |
| 47 | 47 | -336 | -336 | 1209 | 1209 | 150 | 150 | 592⁽¹⁾ | |
| 0 | 0 | 0 | 0 | 2048⁽¹⁾ | | 256⁽¹⁾ | | | |
| -100 | -100 | 1006 | 1006 | | | | | | |
| 0 | 0 | 0 | 0 | | | | | | |
| 192 | 192 | -2691 | -2691 | | | | | | |
| 0 | 0 | 0 | 0 | | | | | | |
| -342 | -342 | 10141 | 10141 | | | | | | |
| 0 | 0 | 16384⁽¹⁾ | | | | | | | |
| 572 | 572 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| -914 | -914 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| 1409 | 1409 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| -2119 | -2119 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| 3152 | 3152 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| -4729 | -4729 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| 7420 | 7420 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| -13334 | -13334 | | | | | | | | |
| 0 | 0 | | | | | | | | |
| 41527 | 41527 | | | | | | | | |
| 65536⁽¹⁾ | | | | | | | | | |

(1) Center taps are highlighted in BOLD

COMPLEX SIGNAL MIXER

The DAC3482 has two paths of complex signal mixer blocks that contain two full complex mixer (FMIX) blocks and power saving coarse mixer (CMIX) blocks. The signal path is shown in Figure 74.

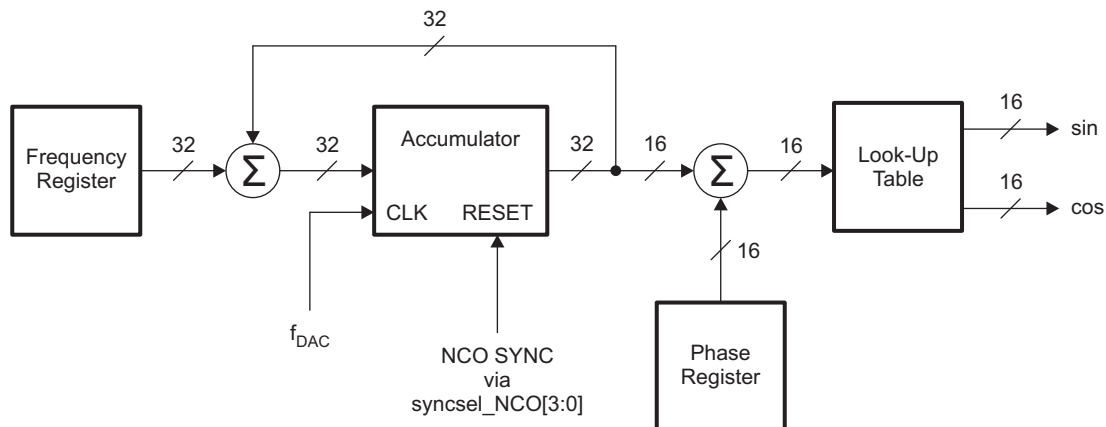


B0471-01

Figure 74. Path of Complex Signal Mixer

FULL COMPLEX MIXER

The DAC3482 has a full complex mixer (FMIX) block with a Numerically Controlled Oscillators (NCO) that enables flexible frequency placement without imposing additional limitations in the signal bandwidth. The NCO has a 32-bit frequency registers (*phaseadd(31:0)*) and a 16-bit phase register (*phaseoffset(15:0)*) that generate the sine and cosine terms for the complex mixing. The NCO block diagram is shown below in Figure 75.



B0026-03

Figure 75. NCO Block Diagram

Synchronization of the NCOs occurs by resetting the NCO accumulators to zero. The synchronization source is selected by *syncsel_NCO(3:0)* in *config31*. The frequency word in the *phaseadd(31:0)* register is added to the accumulators every clock cycle, f_{DAC} . The output frequency of the NCO is:

$$f_{NCO} = \frac{freq \times f_{NCO_CLK}}{2^{32}} \quad (1)$$

With the complex mixer enabled, the two channels in the mixer path are treated as complex vectors of the form $I_{IN}(t) + j Q_{IN}(t)$. The complex signal multiplier (shown in Figure 76) will multiply the complex channels with the sine and cosine terms generated by the NCO. The resulting output, $I_{OUT}(t) + j Q_{OUT}(t)$, of the complex signal multiplier is:

$$I_{OUT}(t) = (I_{IN}(t)\cos(2\pi f_{NCO}t + \delta) - Q_{IN}(t)\sin(2\pi f_{NCO}t + \delta)) \times 2^{(mixer_gain - 1)}$$

$$Q_{OUT}(t) = (I_{IN}(t)\sin(2\pi f_{NCO}t + \delta) + Q_{IN}(t)\cos(2\pi f_{NCO}t + \delta)) \times 2^{(mixer_gain - 1)}$$

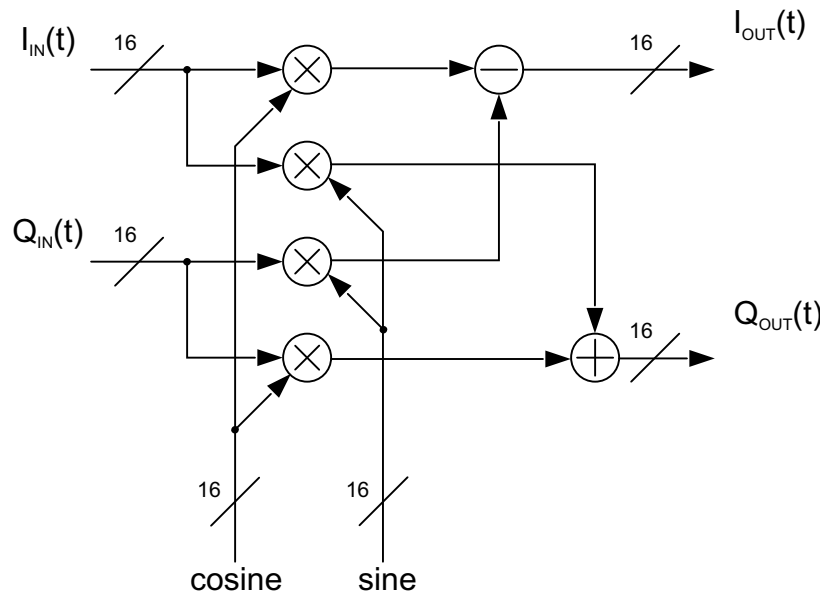


Figure 76. Complex Signal Multiplier

where t is the time since the last resetting of the NCO accumulator, δ is the phase offset value and $mixer_gain$ is either 0 or 1. δ is given by:

$$\delta = 2\pi \times phase_offset(15:0)/2^{16}$$

The $mixer_gain$ option allows the output signals of the multiplier to reduce by half (6dB). See Mixer Gain Section for detail.

COARSE COMPLEX MIXER

In addition to the full complex mixer, the DAC3482 also has a coarse mixer block capable of shifting the input signal spectrum by the fixed mixing frequencies $\pm n \times f_s/8$. Using the coarse mixer instead of the full mixer lowers power consumption.

The output of the $f_s/2$, $f_s/4$, and $-f_s/4$ mixer block is:

$$I_{OUT}(t) = I(t)\cos(2\pi f_{CMIX}t) - Q(t)\sin(2\pi f_{CMIX}t)$$

$$Q_{OUT}(t) = I(t)\sin(2\pi f_{CMIX}t) + Q(t)\cos(2\pi f_{CMIX}t)$$

Since the sine and the cosine terms are a function of $f_s/2$, $f_s/4$, or $-f_s/4$ mixing frequencies, the possible resulting value of the terms will only be 1, -1, or 0. The simplified mathematics allows the complex signal multiplier to be bypassed in any one of the modes, thus mixer gain is not available. The $f_s/2$, $f_s/4$, and $-f_s/4$ mixer blocks performs mixing through negating and swapping of I/Q channel on certain sequence of samples. Table 8 shows the algorithm used for those mixer blocks.

Table 8. Fs/2, Fs/4, and –Fs/4 Mixing Sequence

| MODE | MIXING SEQUENCE |
|-------------------------|---------------------------------------|
| Normal (mixer bypassed) | $I_{out} = \{+I1, +I2, +I3, +I4...\}$ |
| | $Q_{out} = \{+Q1, +Q2, +Q3, +Q4...\}$ |
| fs/2 | $I_{out} = \{+I1, -I2, +I3, -I4...\}$ |
| | $Q_{out} = \{+Q1, -Q2, +Q3, -Q4...\}$ |
| fs/4 | $I_{out} = \{+I1, -Q2, -I3, +Q4...\}$ |
| | $Q_{out} = \{+Q1, +I2, -Q3, -I4...\}$ |
| -fs/4 | $I_{out} = \{+I1, +Q2, -I3, -Q4...\}$ |
| | $Q_{out} = \{+Q1, -I2, -Q3, +I4...\}$ |

The fs/8 mixer can be enabled along with various combinations of fs/2, fs/4, and –fs/4 mixer. Since the fs/8 mixer uses the complex signal multiplier block with fixed fs/8 sine and cosine term, the output of the multiplier is:

$$I_{OUT}(t) = (I_{IN}(t)\cos(2\pi f_{NCO}t + \delta) - Q_{IN}(t)\sin(2\pi f_{NCO}t + \delta)) \times 2^{(mixer_gain - 1)}$$

$$Q_{OUT}(t) = (I_{IN}(t)\sin(2\pi f_{NCO}t + \delta) + Q_{IN}(t)\cos(2\pi f_{NCO}t + \delta)) \times 2^{(mixer_gain - 1)}$$

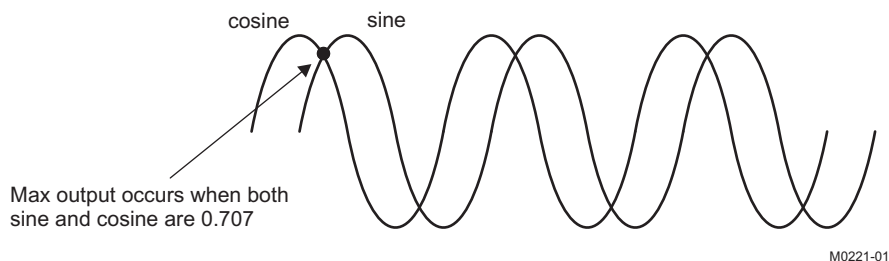
where f_{CMIX} is the fixed mixing frequency selected by *cmix*(3:0). The mixing combinations are described in Table 9. The *mixer_gain* option allows the output signals of the multiplier to reduce by half (6dB). See Mixer Gain section for detail.

Table 9. Coarse Mixer Combinations

| cmix(3:0) | Fs/8 Mixer cmix(3) | Fs/4 Mixer cmix(2) | Fs/2 Mixer cmix(1) | –Fs/4 Mixer cmix(0) | Mixing Mode |
|------------|-----------------------|-----------------------|-----------------------|------------------------|-----------------|
| 0000 | Disabled | Disabled | Disabled | Disabled | No mixing |
| 0001 | Disabled | Disabled | Disabled | Enabled | –Fs/4 |
| 0010 | Disabled | Disabled | Enabled | Disabled | Fs/2 |
| 0100 | Disabled | Enabled | Disabled | Disabled | +Fs/4 |
| 1000 | Enabled | Disabled | Disabled | Disabled | +Fs/8 |
| 1010 | Enabled | Disabled | Enabled | Disabled | –3Fs/8 |
| 1100 | Enabled | Enabled | Disabled | Disabled | +3Fs/8 |
| 1110 | Enabled | Enabled | Enabled | Disabled | –Fs/8 |
| All others | – | – | – | – | Not recommended |

MIXER GAIN

The maximum output amplitude out of the complex signal multiplier (i.e., FMIX mode or CMIX mode with fs/8 mixer enabled) occurs if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously full scale amplitude and the sine and cosine arguments are equal to $2\pi \times f_{MIX}t + \delta \ (2N-1) \times \pi/4$, where $N = 1, 2, 3$, etc....

**Figure 77. Maximum Output of the Complex Signal Multiplier**

With *mixer_gain* = 1 and both $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously full scale amplitude, the maximum output possible out of the complex signal multiplier is $0.707 + 0.707 = 1.414$ (or 3dB). This configuration can cause clipping of the signal and should therefore be used with caution.

With *mixer_gain* = 0 in *config2*, the maximum output possible out of the complex signal multiplier is $0.5 \times (0.707 + 0.707) = 0.707$ (or -3dB). This loss in signal power is in most cases undesirable, and it is recommended that the gain function of the QMC block be used to increase the signal by 3 dB to compensate.

REAL CHANNEL UPCONVERSION

The mixer in the DAC3482 treats the I and Q inputs as complex input data and produces a complex output for most mixing frequencies. The real input data for each channel can be isolated only when the mixing frequency is set to normal mode or $f_s/2$ mode. Refer to [Table 8](#) for details.

QUADRATURE MODULATION CORRECTION (QMC)

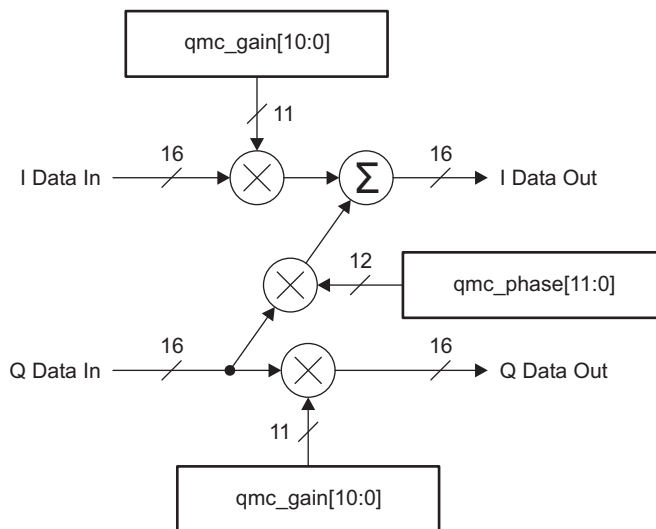
GAIN AND PHASE CORRECTION

The DAC3482 includes a Quadrature Modulator Correction (QMC) block. The QMC blocks provide a mean for changing the gain and phase of the complex signals to compensate for any I and Q imbalances present in an analog quadrature modulator. The block diagram for the QMC block is shown in [Figure 78](#). The QMC block contains 3 programmable parameters.

Register *qmc_gain*(10:0) controls the I and Q path gains and is an 11-bit unsigned value with a range of 0 to 1.9990 and the default gain is 1.0000. The implied decimal point for the multiplication is between bit 9 and bit 10.

Register *qmc_phase*(11:0) control the phase imbalance between I and Q and is a 12-bit values with a range of -0.5 to approximately 0.49975. The QMC phase term is not a direct phase rotation but a constant that is multiplied by each "Q" sample then summed into the "I" sample path. This is an approximation of a true phase rotation in order to keep the implementation simple. The corresponding phase rotation corresponds to approximately +26.5 to -26.5 degrees in 4096 steps.

LO feed-through can be minimized by adjusting the DAC offset feature described below.



B0164-02

Figure 78. QMC Block Diagram

OFFSET CORRECTION

Registers *qmc_offsetI*(12:0) and *qmc_offsetQ*(12:0) can be used to independently adjust the DC offsets of each channel. The offset values are represented in 2s-complement format with a range from -4096 to 4095.

The offset value adds a digital offset to the digital data before digital-to-analog conversion. Since the offset is added directly to the data it may be necessary to back off the signal to prevent saturation. Both data and offset values are LSB aligned.

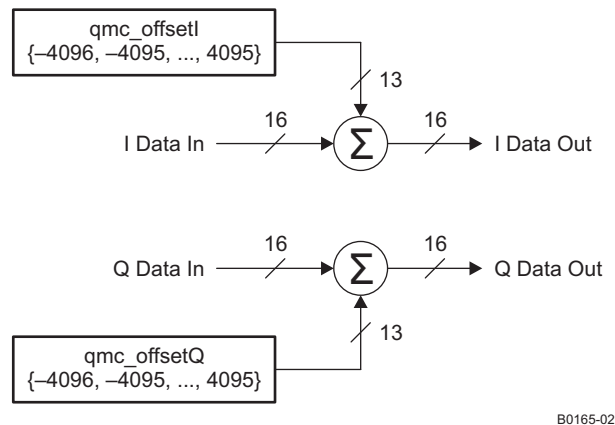


Figure 79. Digital Offset Block Diagram

GROUP DELAY CORRECTION

A complex transmitter system typically is consisted of a DAC, reconstruction filter network, and I/Q modulator. Besides the gain and phase mismatch contribution, there could also be timing mismatch contribution from each components. For instance, the timing mismatch could come from the PCB trace length variation between the I and Q channels and the group delay variation from the reconstruction filter.

This timing mismatch in the complex transmitter system creates phase mismatch that varies linearly with respect to frequency. To compensate for the I/Q imbalances due to this mismatch, the DAC3482 has group delay correction block for each DAC channel. Each DAC channel can adjust its delay through *grp_delayI(7:0)* and *grp_delayQ(7:0)* in register *config46* and *config47*, respectively. The maximum delay ranges from 30ps to 100ps and is dependent on DAC sample clock. Contact TI for specific application information. The group delay correction, along with gain/phase correction, can be useful for correcting imbalances in wide-band transmitter system.

TEMPERATURE SENSOR

The DAC3482 incorporates a temperature sensor block which monitors the temperature by measuring the voltage across 2 transistors. The voltage is converted to an 8-bit digital word using a successive-approximation (SAR) analog to digital conversion process. The result is scaled, limited and formatted as a twos complement value representing the temperature in degrees Celsius.

The sampling is controlled by the serial interface signals SDENB and SCLK. If the temperature sensor is enabled (*tsense_sleep* = 0 in register *config26*) a conversion takes place each time the serial port is written or read. The data is only read and sent out by the digital block when the temperature sensor is read in *tempdata(7:0)* in *config6*. The conversion uses the first eight clocks of the serial clock as the capture and conversion clock, the data is valid on the falling eighth SCLK. The data is then clocked out of the chip on the rising edge of the ninth SCLK. No other clocks to the chip are necessary for the temperature sensor operation. As a result the temperature sensor is enabled even when the device is in sleep mode.

In order for the process described above to operate properly, the serial port read from *config6* must be done with an SCLK period of at least 1 μ s. If this is not satisfied the temperature sensor accuracy is greatly reduced.

DATA PATTERN CHECKER

The DAC3482 incorporates a simple pattern checker test in order to determine errors in the data interface. The main cause of failures is setup/hold timing issues. The test mode is enabled by asserting *iotest_ena* in register *config1*. In test mode the analog outputs are deactivated regardless of the state of TXENABLE or *sif_textnable* in register *config3*.

The data pattern key used for the test is 8 words long and is specified by the contents of *iotest_pattern[0:7]* in registers *config37* through *config44*. The data pattern key can be modified by changing the contents of these registers.

The first word in the test frame is determined by a rising edge transition in FRAME or SYNC, depending on the *syncsel_fifo(3:0)* setting in *config32*. At this transition, the *pattern0* word should be input to the data pins. Patterns 1 through 7 should follow sequentially on each edge of DATACLK (rising and falling). The sequence should be repeated until the pattern checker test is disabled by setting *iotest_ena* back to 0. It is not necessary to have a rising FRAME or SYNC edge aligned with every *pattern0* word, just the first one to mark the beginning of the series.

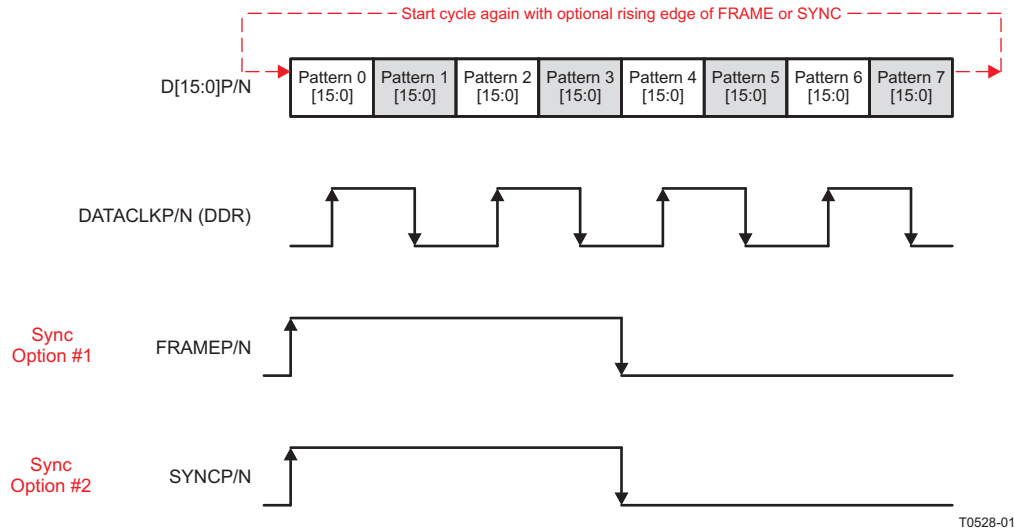


Figure 80. IO Pattern Checker Data Transmission Format

The test mode determines if the 16-bit LVDS data D[15:0]P/N of all the patterns were received correctly by comparing the received data against the data pattern key. If any of the 16-bit data D[15:0]P/N were received incorrectly, the corresponding bits in *iotest_results(15:0)* in register *config4* will be set to “1” to indicate bit error location. Furthermore, the error condition will trigger the *alarm_from_iotest* bit in register *config5* to indicate a general error in the data interface. When data pattern checker mode is enabled, this alarm in register *config5*, bit 7 is the only valid alarm. Other alarms in register *config5* are not valid and can be disregarded.

For instance, *pattern0* is programmed to the default of 0x7A7A. If the received Pattern 0 is 0x7A7B, then bit 0 in *iotest_results(15:0)* will be set to “1” to indicate an error in bit 0 location. The *alarm_from_iotest* will also be set to “1” to report the data transfer error. The user can then narrow down the error from the *alarm_from_iotest* bit location information and implement the fix accordingly.

The alarms can be cleared by writing 0x0000 to *iotest_results(15:0)* and “0” to *alarm_from_iotest* through the serial interface. The serial interface will read back 0s if there are no errors or if the errors are cleared. The corresponding alarm bit will remain a “1” if the errors remain. Based on the pattern test result, the user can adjust the data source output timing, PCB traces delay, or DAC3482 CONFIG36 LVDS Programmable delay to help optimize the setup and hold time of the transmitter system.

Note that unless the unused data pins in byte-wide input format are forced to a known value the data pattern checker is only available for the word-wide input data format. In byte-wide input format, the first 8-bits of the *iotest_pattern[0:7]* in registers *config37* through *config44* will either need to be 0s or 1s for valid data pattern checking.

It is recommended to enable the pattern checker and then run the pattern sequence for 100 or more complete cycles before clearing the *iotest_results(15:0)* and *alarm_from_iotest*. This will eliminate the possibility of false alarms generated during the setup sequence.

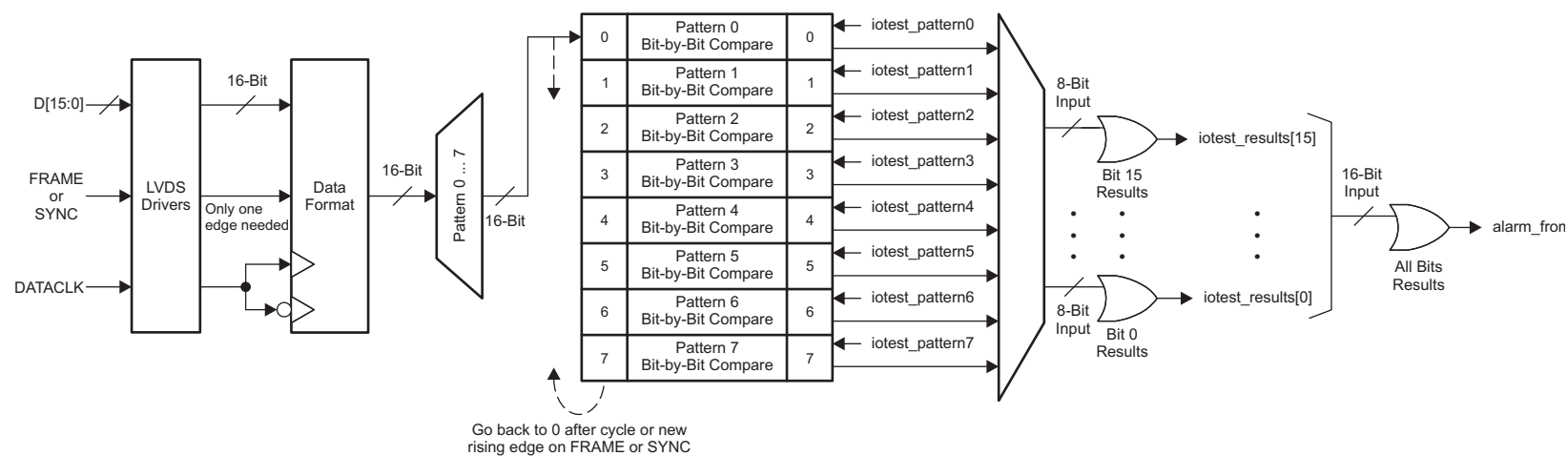


Figure 81. DAC3482 Pattern Check Block Diagram

PARITY CHECK TEST

The DAC3482 has a parity check test that enables continuous validity monitoring of the data received by the DAC. Parity check testing in combination with the data pattern checker offer an excellent solution for detecting board assembly issues due to missing pad connections.

For the parity check test, an extra parity bit is added to the data bits to ensure that the total number of set bits (bits with logic value of “1”) is even or odd. This simple scheme is used to detect data transfer errors. Parity testing is implemented in the DAC3482 in two ways: word-by-word parity and block parity.

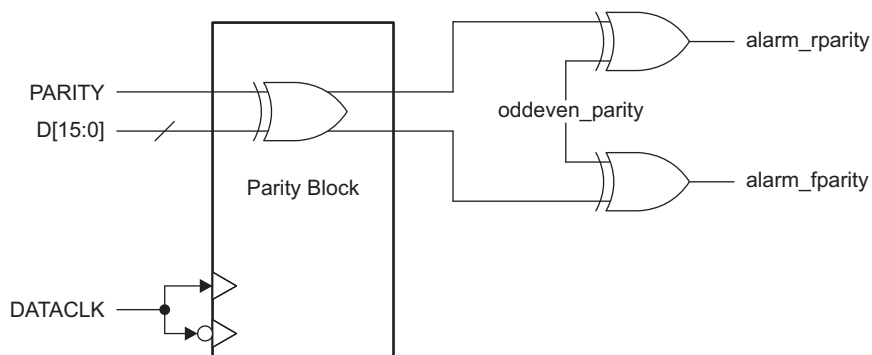
WORD-BY-WORD PARITY

Word-by-word parity is the easiest mode to implement. In this mode the additional parity bit is sourced to the parity input (PARITYP/N) for each data word transfer into the D[15:0]P/N inputs. This mode is enabled by setting the *word_parity_ena* bit. The input parity value is defined to be the total number of logic 1s on the 17-bit data bus, the D[15:0]P/N inputs and the PARITYP/N input. This value, the total number of logic 1s, must match the parity test selected in the *oddeven_parity* bit in register *config1*.

For example, if the *oddeven_parity* bit is set to “1” for odd parity, then the number of 1s on the 17-bit data bus should be odd. The DAC will check the data transfer through the parity input. If the data received has odd number of 1s, then the parity is correct. If the data received has even number of 1s, then the parity is incorrect. The corresponding alarm for parity error will be set accordingly.

Note that unless the unused data pins in byte-wide input format are forced to a known value the word-by-word parity is only available for the word-wide input data format.

Figure 82 shows the simple XOR structure used to check word parity. Parity is tested independently for data captured on both rising and falling edges of DATACLK (*alarm_rparity* and *alarm_fparity*, respectively). Testing on both edges helps in determining a possible setup/hold issue. Both alarms are captured individually in register *config5*.



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Figure 82. DAC3482 Word-by-Word Parity Check

BLOCK PARITY

The block parity method uses the FRAME signal to determine the boundaries of the data block to compute parity. This mode is enabled by setting the *frame_parity_ena* bit in register *config1*.

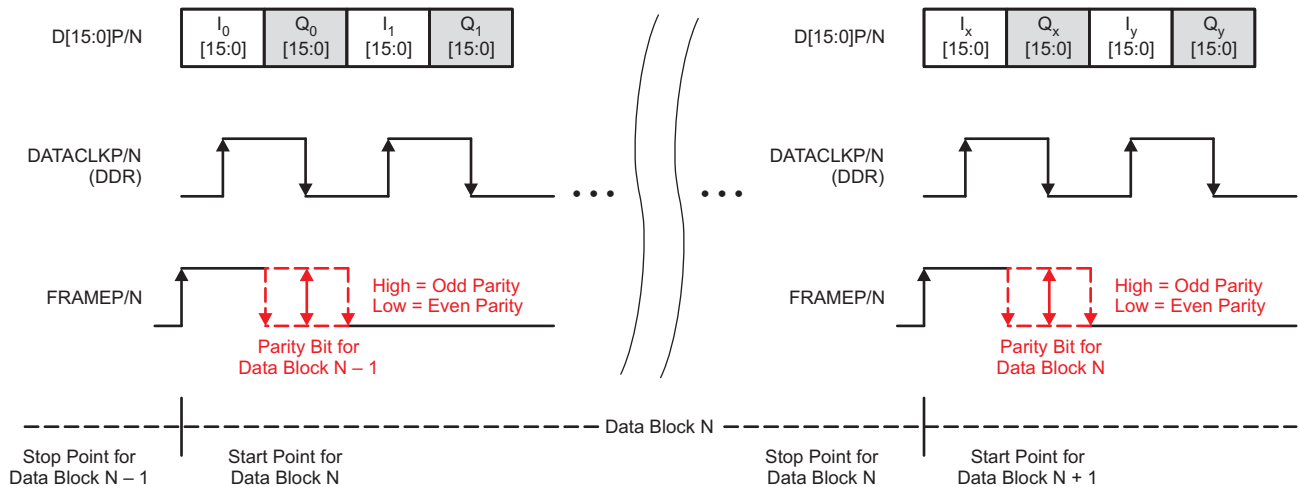
A low-to-high transition of FRAME captured with the DATACLK rising edge determines the end point of the parity block and the beginning of the next one. In this method the parity bit of the completed block corresponds to the FRAME value captured on the DATACLK falling edge right after the STOP/START point.

The input parity value is defined to be the total number of logic 1s in the data block. A logic HIGH captured on the falling edge of DATACLK indicates odd parity or odd number of logic 1s, while a logic LOW indicates even parity or even number of logic 1s. If the expected parity does not match the number of logic 1s in the received data, then *alarm_frame_parity* in register *config5* will be set to “1”. The main advantage of the block parity mode is that there is no need for an additional parity LVDS input.

Since the FRAME signal is used for parity testing in addition to FIFO syncing and frame boundary assignment, it is mandatory to take some extra steps to avoid device malfunction. If FRAME is used to reset the FIFO pointers continuously, the block size must be a multiple of 8 samples (each sample corresponding to 16-bits I and 16-bits Q). In addition since FRAME is used in byte-wide input data mode to establish the frame boundary, the parity block must be aligned with the data frame boundaries.

In addition, the use of block parity in byte-wide input data mode requires the following steps:

1. Since FRAME is used to establish FRAME boundary, the parity block must be aligned with the data frame boundaries.
2. Unused data pins need to have known logic value for block parity to function correctly.



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Notes: Rising edge of FRAMEP/N indicates the beginning of data block.

Parity bit for the current data block is latched on falling edge of DATACLK after the start point for next data block.

Figure 83. DAC3482 Block Parity Check (Example shown with Word-Wide Mode)

DAC3482 ALARM MONITORING

The DAC3482 includes a flexible set of alarm monitoring that can be used to alert of a possible malfunction scenario. All the alarm events can be accessed either through the config5 register or through the ALARM pin. Once an alarm is set, the corresponding alarm bit in register config5 must be reset through the serial interface to allow further testing. The set of alarms includes the following conditions

Zero check alarm

- *Alarm_from_zerock*. Occurs when the FIFO write pointer has an all zeros pattern. Since the write pointer is a shift register, all zeros will cause the input point to be stuck until the next sync event. When this happens a sync to the FIFO block is required.

FIFO alarms

- *alarm_from_fifo*. Occurs when there is a collision in the FIFO pointers or a collision event is close.
 - *alarm_fifo_2away*. Pointers are within two addresses of each other.
 - *alarm_fifo_1away*. Pointers are within one address of each other.
 - *alarm_fifo_collision*. Pointers are equal to each other.

Clock alarms

- *clock_gone*. Occurs when either the DACCLK or DATALOCK have been stopped.
 - *alarm_dacclk_gone*. Occurs when the DACCLK has been stopped.
 - *alarm_dataclk_gone*. Occurs when the DATACLK has been stopped.

Pattern checker alarm

- *alarm_from_iotest*. Occurs when the input data pattern does not match the pattern key.

PLL alarm

- *alarm_from_pll*. Occurs when the PLL is out of lock.

Parity alarms

- *alarm_rparity*. Occurs when there is a parity error in the data captured by the rising edge of DATACLKP/N. The PARITYP/N input is the parity bit (word-by-word parity test).
- *alarm_fparity*. Occurs when there is a parity error in the data captured by the falling edge of DATACLKP/N. The PARITYP/N input is the parity bit (word-by-word parity test).
- *alarm_frame_parity_err*. Occurs when there is a frame parity error when using the FRAME as the parity bit (block parity test).

To prevent unexpected DAC outputs from propagating into the transmit channel chain, the clock and alarm_fifo_collision alarms can be set in *config2* to shut-off the DAC output automatically regardless of the state of TXENABLE or *sif_txenable*.

Alarm monitoring is implemented as follows:

- Power up the device using the recommended power-up sequence.
- Clear all the alarms in *config5* by setting them to 0.
- Unmask those alarms that will generate a hardware interrupt through the ALARM pin in *config7*.
- Enable automatic DAC shut-off in register *config2* if required.
- In the case of an alarm event, the ALARM pin will trigger. If automatic DAC shut-off has been enabled the DAC outputs will be disabled.
- Read registers *config5* to determine which alarm triggered the ALARM pin.
- Correct the error condition and re-synchronize the FIFO.
- Clear the alarms in *config5*.
- Re-read *config5* to ensure the alarm event has been corrected.
- Keep clearing and reading *config5* until no error is reported.

POWER-UP SEQUENCE

The following startup sequence is recommended to power-up the DAC3482:

1. Set TXENABLE low
2. Supply all 1.2V voltages (DACVDD, DIGVDD, CLKVDD and VFUSE) and all 3.3V voltages (AVDD, IOVDD, and PLLAVDD). The 1.2V and 3.3V supplies can be powered up simultaneously or in any order. There are no specific requirements on the ramp rate for the supplies.
3. Provide all LVPECL inputs: DACCLKP/N and the optional OSTRP/N. These inputs can also be provided after the SIF register programming.
4. Toggle the RESETB pin for a minimum 25 ns active low pulse width.
5. Program the SIF registers.
6. Program *config1*, bit <8> = "0" and *config16*, bit <13:12> = "11".
7. Program *fuse_sleep* (*config27*, Bit <11>) to put internal fuses to sleep.
8. FIFO configuration needed for synchronization:
 - (a) Program *syncsel_fifoin*(3:0) (*config32*, bit<15:12>) to select the FIFO input pointer sync source.
 - (b) Program *syncsel_fifoout*(3:0) (*config32*, bit<11:8>) to select the FIFO output pointer sync source.
 - (c) Program *syncsel_dataformatter*(1:0) (*config31*, bit<3:2>) to select the FIFO Data Formatter sync source.
9. Clock divider configuration needed for synchronization:
 - (a) Program *clkdiv_sync_sel* (*config32*, bit<0>) to select the clock divider sync source.
 - (b) Program *clkdiv_sync_ena* (*config0*, bit<2>) to "1" to enable clock divider sync.
 - (c) For multi-DAC synchronization in PLL mode, program *pll_ndivsync_ena* (*config24*, bit<11>) to "1" to synchronize the PLL N-divider.
10. Provide all LVDS inputs (D[15:0]P/N, DATACLKP/N, FRAMEP/N, SYNCN/P and PARITYP/N) simultaneously. Synchronize the FIFO and clock divider by providing the pulse or periodic signals needed.
 - (a) For Single Sync Source Mode where either FRAMEP/N or SYNCN/P is used to sync the FIFO, a single rising edge for FIFO, FIFO data formatter, and clock divider sync is recommended. Periodic sync signal

is not recommended due to the non-deterministic latency of the sync signal through the clock domain transfer.

- (b) For Dual Sync Sources Mode, both single pulse or periodic sync signals can be used.
 - (c) For multi-DAC synchronization in PLL mode, the LVDS SYNC/N signal is used to sync the PLL N-divider and can be sourced from either the FPGA/ASIC pattern generator or clock distribution circuit as long as the $t_{\text{SYNC_PLL}}$ setup and hold timing requirement is met with respect to the reference clock source at DACCLKP/N pins. The LVDS SYNC/N signal can be provided at this point.
11. FIFO and clock divider configurations after all the sync signals have provided the initial sync pulses needed for synchronization:
- (a) For Single Sync Source Mode where the clock divider sync source is either FRAMEP/N or SYNC/N, clock divider syncing may be disabled after DAC3482 initialization and before the data transmission by setting *clkdiv_sync_ena* (config0, bit 2) to "0". This is to prevent accidental syncing of the clock divider or when sending FRAMEP/N or SYNC/N pulse to other digital blocks.
 - (b) For Dual Sync Sources Mode, where the clock divider sync source is from the OSTR signal (either from external OSTRP/N or internal PLL N divider output), the clock divider syncing may be enabled at all time.
 - (c) Optionally, to prevent accidental syncing of the FIFO and FIFO data formatter when sending the FRAMEP/N or SYNC/N pulse to other digital blocks such as NCO, QMC, etc, disable FIFO syncing by setting *syncsel_fifo_in(3:0)* and *syncsel_fifo_out(3:0)* to "0000" after the FIFO input and output pointers are initialized. Also Disable the FIFO data formatter by setting *syncsel_dataformatter(1:0)* to "10" or "11". If the FIFO and FIFO data formatter sync remain enabled after initialization, the FRAMEP/N or SYNC/N pulse must occur in ways to not disturb the FIFO operation. Refer to the INPUT FIFO section for detail.
 - (d) Disable PLL N-divider syncing by setting *pll_ndivsync_ena* (config24, bit<11>) to "0".
12. Enable transmit of data by asserting the TXENABLE pin or *set_sif_txenable* to "1".
13. At any time, if any of the clocks (i.e DATACLK or DACCLK) is lost or a FIFO collision alarm is detected, a complete resynchronization of the DAC is necessary. Set TXENABLE low and repeat steps 8 through 12. Program the FIFO configuration and clock divider configuration per steps 8 and 9 appropriately to accept the new sync pulse or pulses for the synchronization.

EXAMPLE START-UP ROUTINE

DEVICE CONFIGURATION

$f_{\text{DATA}} = 491.52\text{MSPS}$, 16-bit word wide interface
 Interpolation = 2x
 Input data = baseband data
 $f_{\text{OUT}} = 122.88\text{MHz}$
 PLL = Enabled
 Full Mixer = Enabled
 Dual Sync Sources Mode

PLL CONFIGURATION

$f_{\text{REFCLK}} = 491.52\text{MHz}$ at the DACCLKP/N LVPECL pins
 $f_{\text{DACCLK}} = f_{\text{DATA}} \times \text{Interpolation} = 983.04\text{MHz}$
 $f_{\text{VCO}} = 4 \times f_{\text{DACCLK}} = 3932.16\text{MHz}$ (keep f_{VCO} between 3.3GHz to 4GHz)
 $\text{PFD} = f_{\text{OSTR}} = 30.72\text{MHz}$
 $N = 16$, $M = 32$, $P = 3$, single charge pump
 $\text{pll_vco}(5:0) = "100100"$ (36)

NCO CONFIGURATION

$$f_{\text{NCO}} = 122.88\text{MHz}$$

$$f_{\text{NCO_CLK}} = 983.04\text{MHz}$$

$$\text{freq} = f_{\text{NCO}} \times 2^{32} / 983.04 = 536870912 = 0x20000000$$

$$\text{phaseaddAB}(31:0) \text{ or } \text{phaseaddCD}(31:0) = 0x20000000$$

NCO SYNC = rising edge of SYNC

EXAMPLE START-UP SEQUENCE

Table 10. Example Start-Up Sequence Description

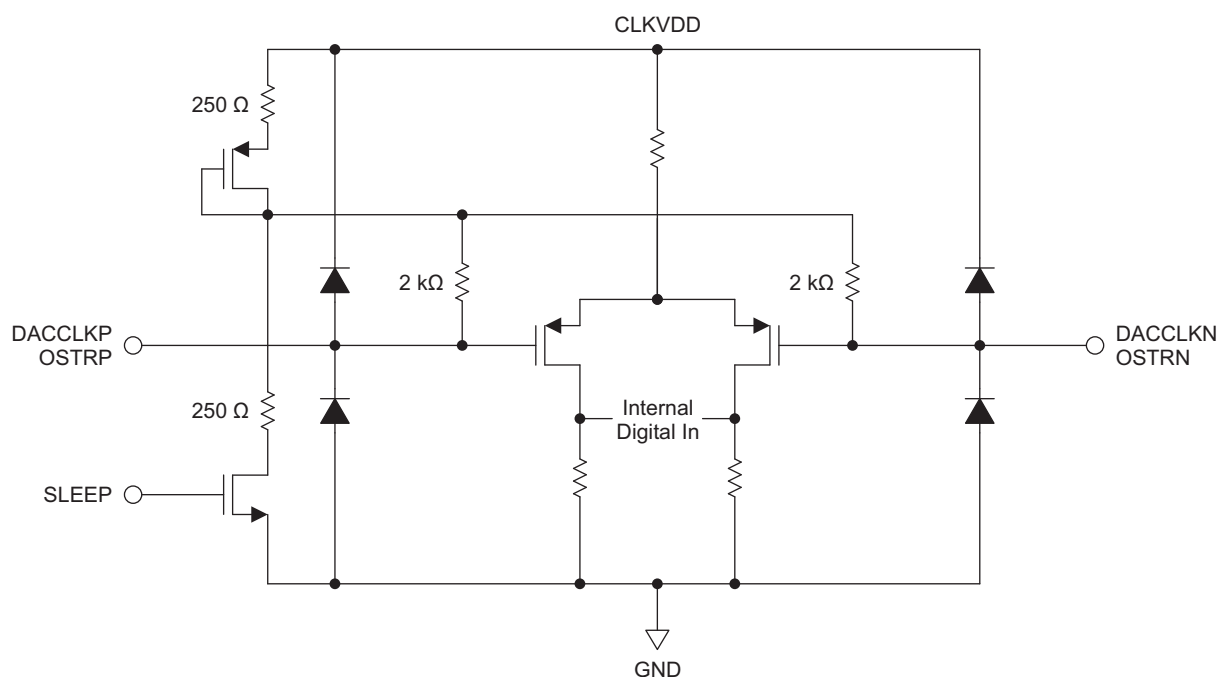
| STEP | READ/WRITE | ADDRESS | VALUE | DESCRIPTION |
|------|------------|---------|--------|--|
| 1 | N/A | N/A | N/A | Set TXENABLE Low |
| 2 | N/A | N/A | N/A | Power-up the device |
| 3 | N/A | N/A | N/A | Apply LVPECL DACCLKP/N for PLL reference clock |
| 4 | N/A | N/A | N/A | Toggle RESETB pin |
| 5 | Write | 0x00 | 0xA19E | QMC offset and correction enabled, 2x int, FIFO enabled, Alarm enabled, clock divider sync enabled, inverse sinc filter enabled. |
| 6 | Write | 0x01 | 0x040E | Single parity enabled, FIFO alarms enabled (2 away, 1 away, and collision). Note: bit8 = '0' |
| 7 | Write | 0x02 | 0xF052 | Output shut-off when DACCLK gone, DATACLK gone, and FIFO collision. Mixer block with NCO enabled, twos complement. Word wide interface. |
| 8 | Write | 0x03 | 0xA000 | Output current set to 20mAFS with internal reference and 1.28kohm R _{BIAS} resistor. |
| 9 | Write | 0x07 | 0xD8FF | Un-mask FIFO collision, DACCLK-gone, and DATACLK-gone alarms to the Alarm output. |
| 10 | Write | 0x08 | N/A | Program the desired channel I QMC offset value. (Causes Auto-Sync for QMC Offset Block) |
| 11 | Write | 0x09 | N/A | Program the desired FIFO offset value and channel Q QMC offset value. |
| 12 | Write | 0x0C | N/A | Program the desired channel I QMC gain value. |
| 13 | Write | 0x0D | N/A | Coarse mixer mode not used. Program the desired channel Q QMC gain value. |
| 14 | Write | 0x10 | N/A | Program the desired channel IQ QMC phase value. (Causes Auto-Sync QMC Correction Block) Note : bit13 and bit12 = '1' |
| 15 | Write | 0x12 | N/A | Program the desired channel IQ NCO phase offset value. (Causes Auto-Sync for Channel IQ NCO Mixer) |
| 16 | Write | 0x14 | 0x2000 | Program the desired channel IQ NCO frequency value |
| 17 | Write | 0x15 | 0x0000 | Program the desired channel IQ NCO frequency value |
| 18 | Write | 0x18 | 0x2C67 | PLL enabled, PLL N-dividers sync enabled, single charge pump, prescaler = 4. |
| 19 | Write | 0x19 | 0x20F4 | M = 32, N = 16, PLL VCO bias tune = "01" |
| 20 | Write | 0x1A | 0xEC00 | PLL VCO coarse tune = 59 |
| 21 | Write | 0x1B | 0x0800 | Internal reference |
| 22 | Write | 0x1E | 0x9191 | QMC offset IQ and QMC correction IQ can be synced by <code>sif_sync</code> or <code>auto-sync</code> from register write |
| 23 | Write | 0x1F | 0x4140 | Mixer IQ values synced by <code>SYNCP/N</code> . NCO accumulator synced by <code>SYNCP/N</code> . FIFO data formatter synced by <code>FRAMEP/N</code> . |
| 24 | Write | 0x20 | 0x2400 | FIFO Input Pointer Sync Source = FRAME FIFO Output Pointer Sync Source = OSTR (from PLL N-divider output) Clock Divider Sync Source = OSTR |
| 25 | N/A | N/A | N/A | Provide all the LVDS DATA and DATACLK Provide rising edge <code>FRAMEP/N</code> and rising edge <code>SYNCP/N</code> to sync the FIFO input pointer and PLL N-dividers. |

Table 10. Example Start-Up Sequence Description (continued)

| STEP | READ/WRITE | ADDRESS | VALUE | DESCRIPTION |
|------|------------|---------|--------|--|
| 26 | Read | 0x18 | N/A | Read back pll_lfvolt(2:0). If the value is not optimal, adjust pll_vco(5:0) in 0x1A. |
| 27 | Write | 0x05 | 0x0000 | Clear all alarms in 0x05. |
| 28 | Read | 0x05 | N/A | Read back all alarms in 0x05. Check for PLL lock, FIFO collision, DACCLK-gone, DATACLK-gone, etc. Fix the error appropriately. Repeat step 26 and 27 as necessary. |
| 29 | Write | 0x1F | 0x4142 | Sync all the QMC blocks using <code>sif_sync</code> . These blocks can also be synced via auto-sync through appropriate register writes. |
| 30 | Write | 0x00 | 0xA19A | Disable clock divider sync. |
| 31 | Write | 0x1F | 0x4148 | Disable FIFO data formatter sync. Set <code>sif_sync</code> to "0" for the next <code>sif_sync</code> event. |
| 32 | Write | 0x20 | 0x0000 | Disable FIFO input and output pointer sync. |
| 33 | Write | 0x18 | 0x2467 | Disable PLL N-dividers sync. |
| 34 | N/A | N/A | N/A | Set TXENABLE high. Enable data transmission. |

LVPECL INPUTS

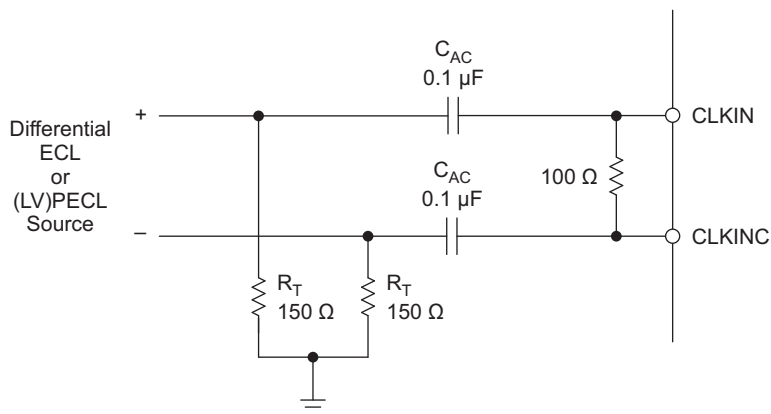
Figure 84 shows an equivalent circuit for the DAC input clock (DACCLKP/N) and the output strobe clock (OSTRP/N).



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Figure 84. DACCLKP/N and OSTRP/N Equivalent Input Circuit

Figure 85 shows the preferred configuration for driving the CLKIN/CLKINC input clock with a differential ECL/PECL source.

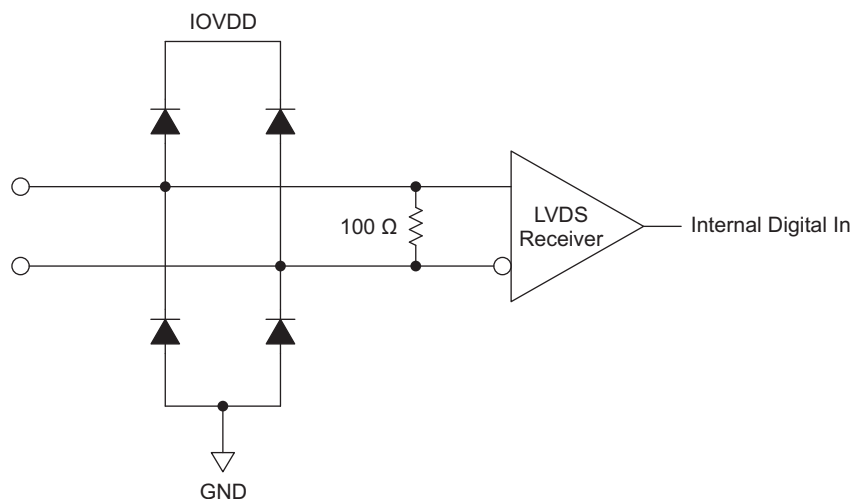


S0029-02

Figure 85. Preferred Clock Input Configuration with a Differential ECL/PECL Clock Source

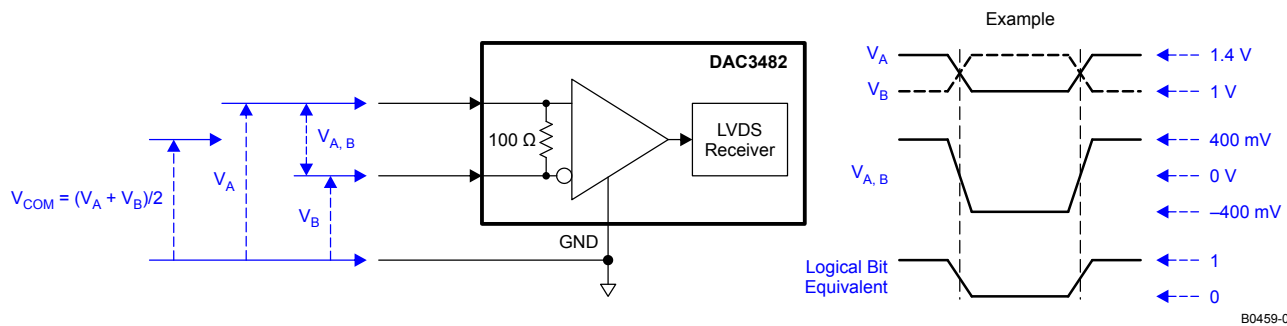
LVDS INPUTS

The D[15:0]P/N, DATACLKP/N, SYNCNP/N, PARITYP/N and FRAMEP/N LVDS pairs have the input configuration shown in Figure 86. Figure 87 shows the typical input levels and common-mode voltage used to drive these inputs.



S0516-01

Figure 86. D[15:0]P/N, DATACLKP/N, FRAMEP/N, SYNCNP/N and PARITYP/N LVDS Input Configuration



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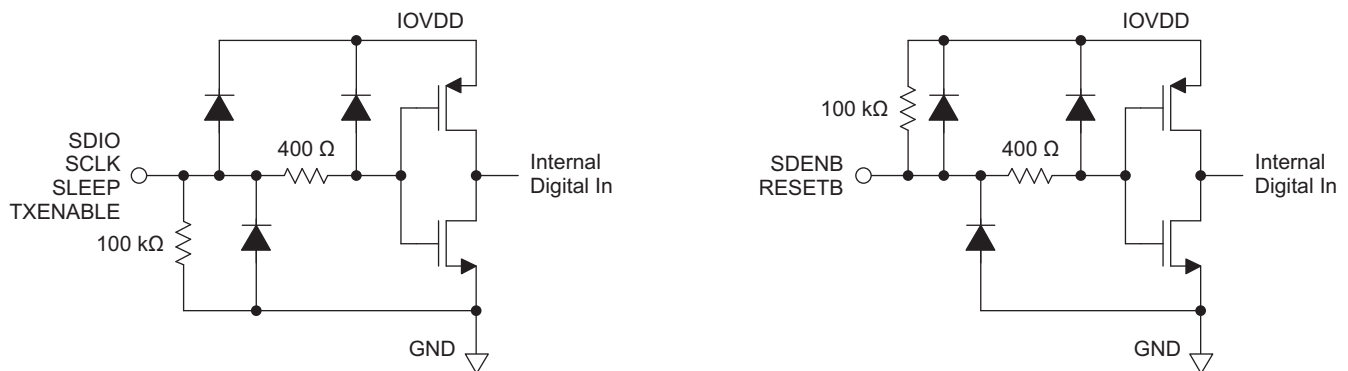
Figure 87. LVDS Data Input Levels

Table 11. Example LVDS Data Input Levels

| Applied Voltages | | Resulting Differential Voltage | Resulting Common-Mode Voltage | Logical Bit Binary Equivalent |
|------------------|----------------|--------------------------------|-------------------------------|-------------------------------|
| V _A | V _B | V _{A,B} | V _{COM} | |
| 1.4 V | 1.0 V | 400 mV | 1.2 V | 1 |
| 1.0 V | 1.4 V | -400 mV | | 0 |
| 1.2 V | 0.8 V | 400 mV | 1.0 V | 1 |
| 0.8 V | 1.2 V | -400 mV | | 0 |

CMOS DIGITAL INPUTS

Figure 88 shows a schematic of the equivalent CMOS digital inputs of the DAC3482. SDIO, SCLK, SLEEP and TXENABLE have pull-down resistors while SDENB and RESETB have pull-up resistors internal to the DAC3482. See the specification table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 100kΩ.



S0027-03

Figure 88. CMOS Digital Equivalent Input

REFERENCE OPERATION

The DAC3482 uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 64 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 64 \times I_{BIAS} = 64 \times (V_{EXTIO} / R_{BIAS}) / 2$$

The DAC3482 has a 4-bit coarse gain control *coarse_dac(3:0)* in the *config3* register. Using gain control, the $IOUT_{FS}$ can be expressed as:

$$IOUT_{FS} = (coarse_dac + 1) / 16 \times I_{BIAS} \times 64 = (coarse_dac + 1) / 16 \times (V_{EXTIO} / R_{BIAS}) / 2 \times 64$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2V. This reference is active when *extref_ena* = '0' in *config27*. An external decoupling capacitor C_{EXT} of 0.1 μF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by setting the *extref_ena* control bit. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 30 mA down to 10 mA by varying resistor R_{BIAS} , programming *coarse_dac(3:0)*, or changing the externally applied reference voltage.

NOTE

With internal reference, the minimum R_{bias} resistor value is 1.28k Ω . Resistor value below 1.28k Ω is not recommended since it will program the full-scale current to go above 30mA and potentially damages the device.

DAC TRANSFER FUNCTION

The CMOS DAC's consist of a segmented array of PMOS current sources, capable of sourcing a full-scale output current up to 30 mA. Differential current switches direct the current to either one of the complementary output nodes IOUTP or IOUTN. Complementary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (+1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 64 times I_{BIAS} .

The relation between IOUTP and IOUTN can be expressed as:

$$IOUT_{\text{FS}} = IOUTP + IOUTN$$

We will denote current flowing into a node as – current and current flowing out of a node as + current. Since the output stage is a current source the current flows from the IOUTP and IOUTN pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUTP = IOUT_{\text{FS}} \times \text{CODE} / 65536$$

$$IOUTN = IOUT_{\text{FS}} \times (65535 - \text{CODE}) / 65536$$

where CODE is the decimal representation of the DAC data input word

For the case where IOUTP and IOUTN drive resistor loads R_L directly, this translates into single ended voltages at IOUTP and IOUTN:

$$VOUTP = IOUT1 \times R_L$$

$$VOUTN = IOUT2 \times R_L$$

Assuming that the data is full scale (65535 in offset binary notation) and the R_L is 25 Ω , the differential voltage between pins IOUTP and IOUTN can be expressed as:

$$VOUTP = 20\text{mA} \times 25 \Omega = 0.5 \text{ V}$$

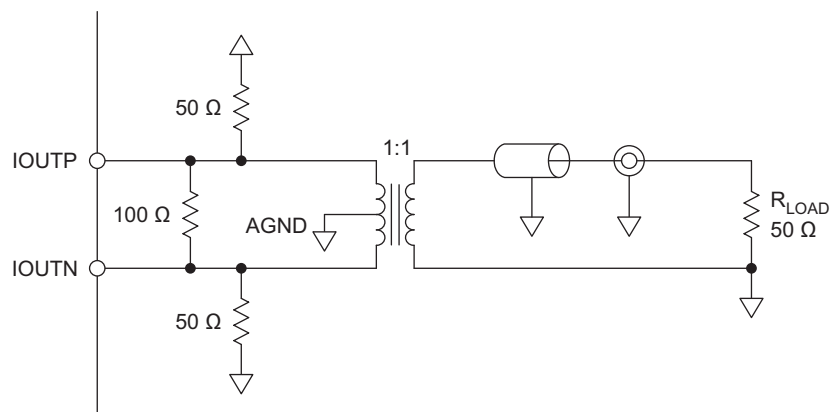
$$VOUTN = 0\text{mA} \times 25 \Omega = 0 \text{ V}$$

$$V_{\text{DIFF}} = VOUTP - VOUTN = 0.5\text{V}$$

Note that care should be taken not to exceed the compliance voltages at node IOUTP and IOUTN, which would lead to increased signal distortion.

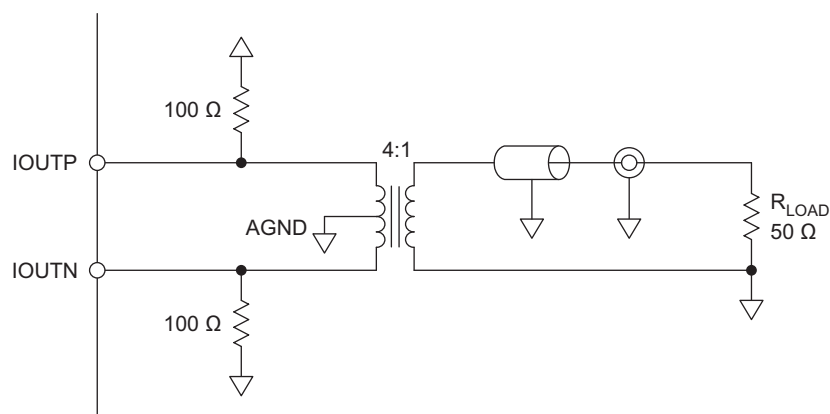
ANALOG CURRENT OUTPUTS

The DAC3482 can be easily configured to drive a doubly terminated 50 Ω cable using a properly selected RF transformer. [Figure 89](#) and [Figure 90](#) show the 50 Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a DC current flow. Applying a 20 mA full-scale output current would lead to a 0.5 Vpp for a 1:1 transformer and a 1 Vpp output for a 4:1 transformer. The low dc-impedance between IOUTP or IOUTN and the transformer center tap sets the center of the ac-signal to GND, so the 1 Vpp output for the 4:1 transformer results in an output between –0.5 V and +0.5 V.



S0517-01

Figure 89. Driving a Doubly Terminated 50 Ω Cable Using a 1:1 Impedance Ratio Transformer



S0518-01

Figure 90. Driving a Doubly Terminated 50 Ω Cable Using a 4:1 Impedance Ratio Transformer

REVISION HISTORY

Changes from Original (March 2011) to Revision A Page

- Changed from PRODUCT PREVIEW to PRODUCTION DATA 1

Changes from Revision A (March 2011) to Revision B Page

- Changed ALARM description 3
- Added notes to ELECTRICAL CHARACTERISTICS – DC SPECIFICATIONS 11
- Deleted TYP and MAX values from $V_{A,B+}$ 13
- Changed V_{COM} MIN value from 1.075V to 1.0V 13
- Added MIN and MAX values for Z_T 13
- Added f_{DAC} PLL ON MIN of 1000MSPS in ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS 16
- Changed config5 default value from 0x0000 to NA in Register Map 30
- Changed register version default value from 0x5409 to 0x540C in Register Map 31
- Added SIF SYNC to register config32 description 43
- Changed register config35 description 44
- Changed register config36 description from 40ps to 50ps 44
- Changed register version default value from 0x5409 to 0x540C 46
- Added information to SINGLE SYNC SOURCE MODE section to clarify the latency limitation of Single Sync Source Mode 52
- Changed 1.2288GHz to 983.04MHz in PLL MODE description 56
- Changed data in [Table 5](#) 56
- Deleted 2x in [Table 7](#) 63
- Changed config32 to config 31 in POWER-UP SEQUENCE description 73
- Changed EXAMPLE START-UP ROUTINE information 74
- Changed [Table 10](#) 75

Changes from Revision B (September 2011) to Revision C Page

- Changed Package options in FEATURES 1
- Added ZAY package 6
- Added ZAY pin functions 7
- Added ZAY package to ORDERING INFORMATION section 9
- Added ZAY package to THERMAL INFORMATION section 10
- Added Input Common Mode max value of 1.6V 13
- Added information to CLOCK INPUT (DACCLKP/N) in ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS 13
- Added information to OUTPUT STROBE (OSTRP/N) in ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS 13
- Changed ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS AC PERFORMANCE information 16
- Changed [Figure 21](#) 20
- Changed [Figure 22](#) 21
- Changed [Figure 23](#) 21
- Changed [Figure 24](#) 21
- Added [Figure 48](#) 25
- Added [Figure 49](#) 25
- Changed config3 to config9 in INPUT FIFO section 49

| | |
|---|----|
| • Added information for double-charge-pump current to PLL MODE section | 56 |
| • Changed Figure 76 | 65 |
| • Changed +3.75 to –3.75 degrees in 1024 steps to +26.5 to –26.5 degrees in 4096 steps in GAIN AND PHASE CORRECTION section | 67 |

| Changes from Revision C (June 2012) to Revision D | Page |
|---|-------------|
| • Added thermal information to the Absolute Maximum Ratings table | 9 |
| • Deleted T _J row from top of thermal table | 10 |
| • Added Recommended Operating Conditions table | 10 |
| • Deleted OPERATING RANGE section from bottom of Electrical Characteristics – DC Specifications table | 11 |

| Changes from Revision D (August 2012) to Revision E | Page |
|---|-------------|
| • Changed Power Supply Specification Table under Electrical Specification. This specification depends on the enhanced production test coverage and is specific to devices with certain date code. Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details | 12 |
| • Deleted Note (5) in Power Consumption Specification to reflect the latest DAC3482 speed specification. | 12 |
| • Changed DACCLKP/N typical clock swing specification to reflect commonly used LVPECL driver | 13 |
| • Changed DACCLKP/N typical clock swing specification to reflect commonly used LVPECL driver | 13 |
| • Changed DACCLK driver requirement to reflect actual device performance under commonly used LVPECL drivers | 13 |
| • Changed Analog Output Specification Table under Electrical Specification. This specification depends on the enhanced production test coverage and is specific to devices with certain date code. Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details | 16 |
| • Changed Digital Latency Specification for QMC to reflect the actual DAC3482 parameter | 16 |
| • Changed Digital Latency Specification for Inverse Sinc to reflect the actual DAC3482 parameter | 16 |
| • Added Phase-Locked Loop Specification Table under Electrical Specification. This specification depends on the enhanced production test coverage and is specific to devices with certain date code. Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details | 17 |
| • Changed pll_vco(6:0) to pll_vco(5:0) to reflect actual bit width in the register | 40 |
| • Changed config45, bit12:1 default value to reflect the actual default register value | 45 |
| • Changed config45, bit0 description to clarify additional DAC3482 behavior | 45 |
| • Changed syncsel_fifoout(3:0) description to clarify the FIFO read pointer reset capture method and limitation | 50 |
| • Changed information to SINGLE SYNC SOURCE MODE section to clarify the latency limitation of Single Sync Source Mode | 52 |
| • Added "the effect of bypassing the FIFO" in the Bypass Mode section to clarify the operation of FIFO, LVDS FRAME, and LVDS SYNC in FIFO Bypass Mode | 53 |
| • Changed PLL Mode section with additional operating recommendations for the DAC3482 on-chip PLL | 55 |
| • Changed information to MULTI-DEVICE OPERATION: SINGLE SYNC SOURCE MODE section to clarify the latency limitation of Single Sync Source Mode | 59 |
| • Changed Figure 64 to clarify the latency limitation of Single Sync Source Mode | 60 |
| • Changed Data Pattern Checker section with additional operating recommendations | 69 |
| • Added additional requirements for Block Parity section when byte wide input data mode is selected | 72 |
| • Changed the NCO setting description in the Example Start-up Sequence Section to reflect the example register writes | 75 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DAC3482IRKDR | ACTIVE | WQFN-MR | RKD | 88 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC3482I | Samples |
| DAC3482IRKDT | ACTIVE | WQFN-MR | RKD | 88 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC3482I | Samples |
| DAC3482IZAY | ACTIVE | NFBGA | ZAY | 196 | 160 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | DAC3482I | Samples |
| DAC3482IZAYR | ACTIVE | NFBGA | ZAY | 196 | 1000 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | DAC3482I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

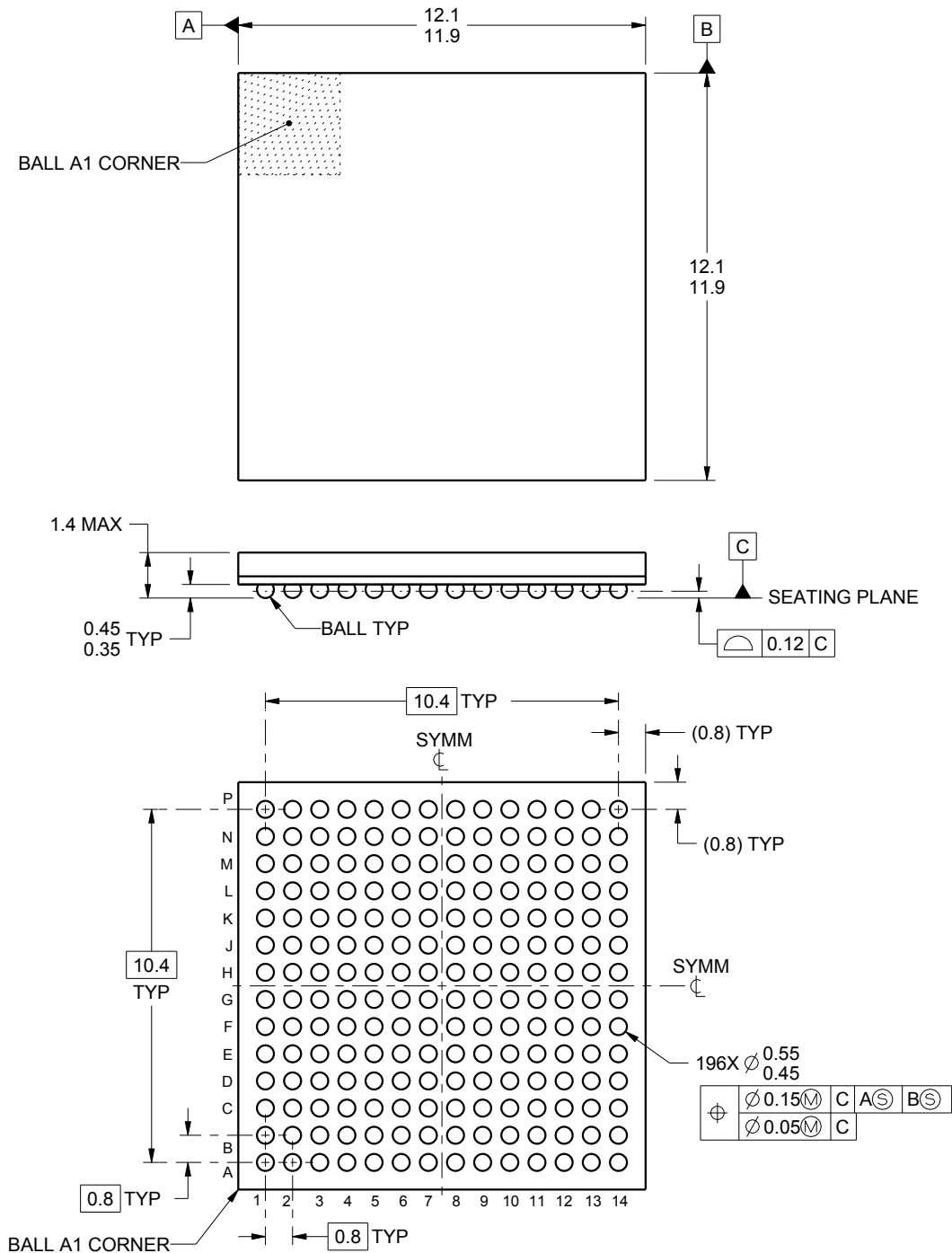
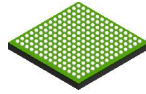
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC3482IRKDR | WQFN-MR | RKD | 88 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| DAC3482IRKDT | WQFN-MR | RKD | 88 | 250 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC3482IRKDR | WQFN-MR | RKD | 88 | 2000 | 336.6 | 336.6 | 28.6 |
| DAC3482IRKDT | WQFN-MR | RKD | 88 | 250 | 367.0 | 367.0 | 38.0 |



4219823/A 09/2015

NOTES:

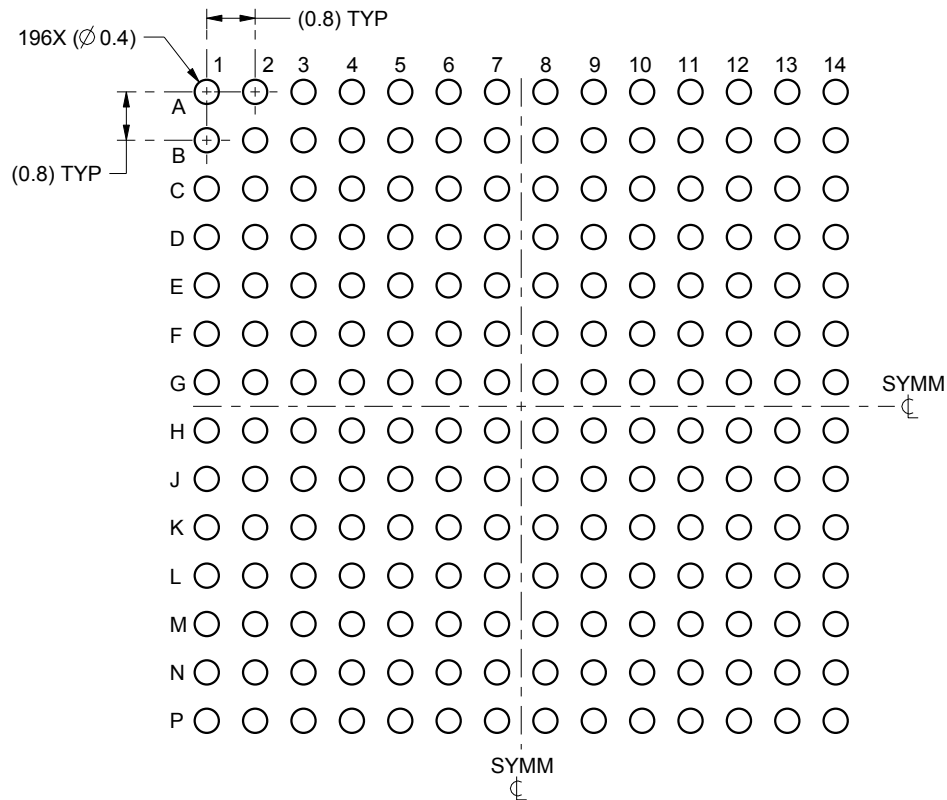
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

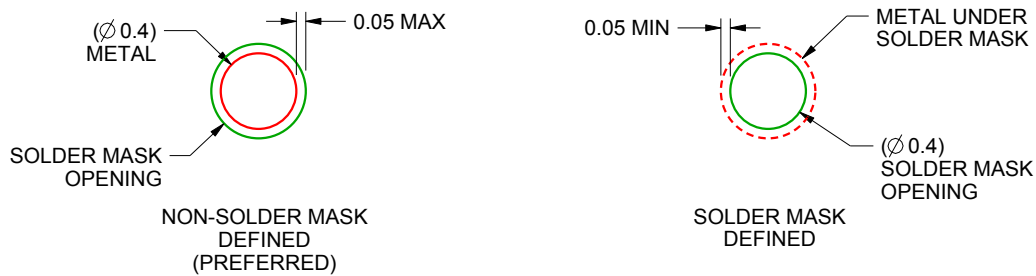
ZAY0196A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4219823/A 09/2015

NOTES: (continued)

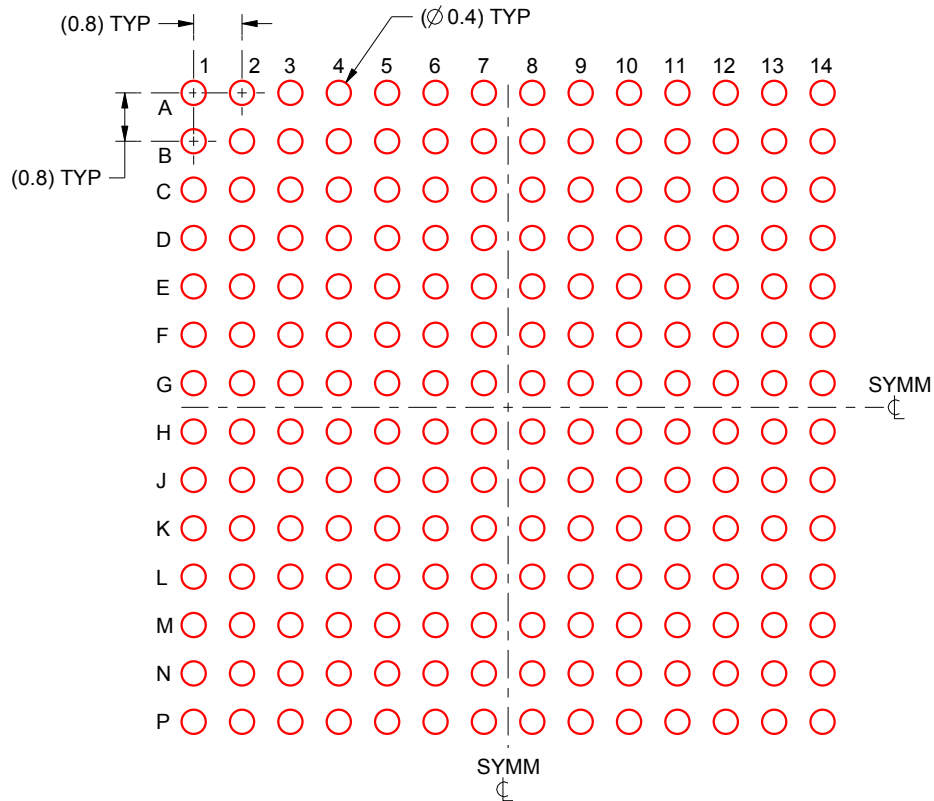
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZAY0196A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

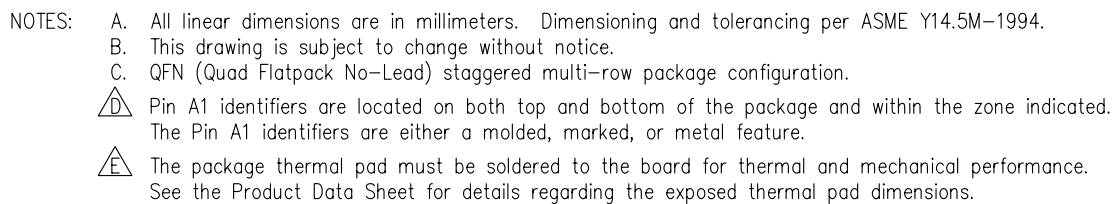


SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219823/A 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



RKD (S-MRQFN-N88)

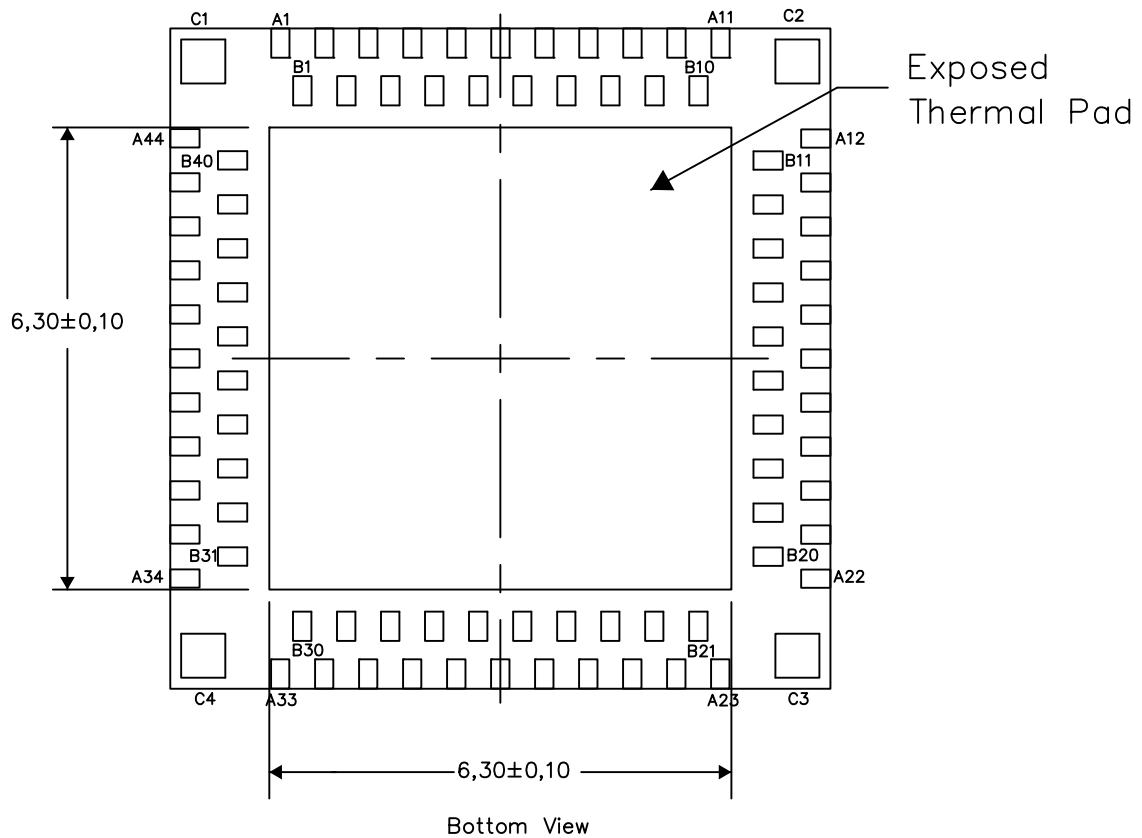
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



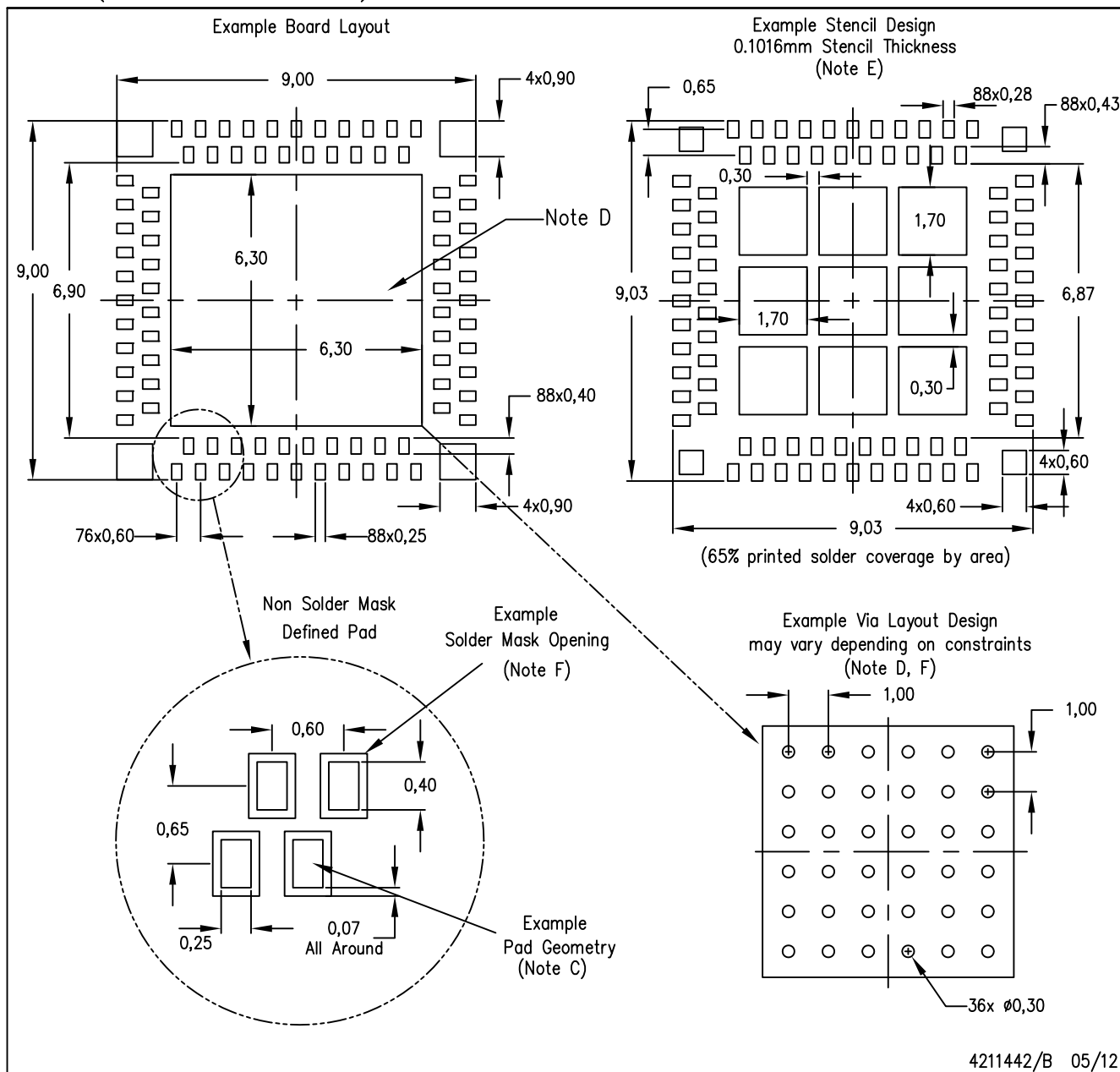
Exposed Thermal Pad Dimensions

4210259/C 11/13

NOTE: All linear dimensions are in millimeters

RKD (S-MRQFN-N88)

PLASTIC QUAD FLATPACK NO-LEAD



4211442/B 05/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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