BURR-BROWN®

DAC811

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Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: Double-Buffered Latch
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS

DESCRIPTION

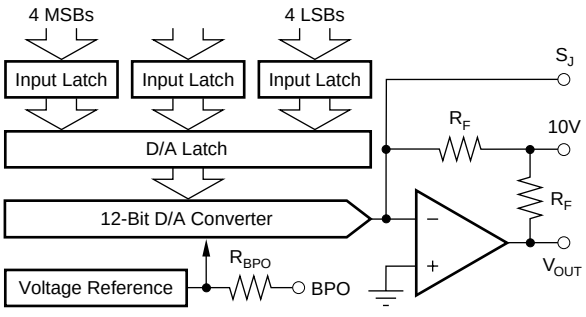
The DAC811 is a complete, single-chip integrated-circuit, microprocessor-compatible, 12-bit digital-to-analog converter. The chip combines a precision voltage reference, microcomputer interface logic, and double-buffered latch, in a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nibbles to permit interfacing to 4-, 8-, 12-, or 16-bit buses and to handle right-or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nibble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B and K grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in six performance grades and three package types. DAC811J and K are specified over the temperature ranges of 0°C to +70°C; DAC811A and B are specified over –25°C to +85°C; DAC811J and K are packaged in a reliable 28-pin plastic DIP or plastic SO package, while DAC811A and B are available in a 28-pin 0.6" wide dual-inline hermetically sealed ceramic side-brazed package (H package).



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SPECIFICATIONS

At T_A = +25°C. $\pm V_{CC}$ = 12V or 15V, unless otherwise noted.

PARAMETER	DAC811AH, JP, JU			DAC811BH, KP, KU			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT							
Resolution			12			*	Bits
Codes[1]		USB, BOB			*		
Digital Inputs Over Temperature Range[2]							
V_{IH}	+2		+15	*		*	VDC
V_{IL}	0		+0.8	*		*	VDC
I_{IH}, V_I = +2.7V			+10			*	µA
I_{IL}, V_I = +0.4V			±20			*	µA
Digital Interface Timing Over Temperature Range							
t_{WP}, $\overline{WR}$ Pulse Width	50			*			ns
t_{AW}1, $\overline{N_X}$ and $\overline{LDAC}$ Valid to End of $\overline{WR}$	50			*			ns
t_{DW}, Data Valid to End of $\overline{WR}$	80			*			ns
t_{DH}, Data Valid Hold Time	0			*			ns
ACCURACY							
Linearity Error		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]		±0.1	±0.2		*	*	%
Offset Error[3, 4]		±0.05	±0.15		*	*	% of FSR[5]
Monotonicity		Guaranteed			*		
Power Supply Sensitivity: $+V_{CC}$		±0.001	±0.003		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.002	±0.006		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		*	*	% of FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)							
Gain		±10	±30		±10	±20	ppm/°C
Unipolar Offset		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			*		
SETTLING TIME[6] (to within ±0.01% of FSR of Final Value; 2kΩ load)							
For Full Scale Range Change, 20V Range		3	4		*	*	µs
10V Range		3	4		*	*	µs
For 1LSB Change at Major Carry[7]		1			*		µs
Slew Rate[6]	8	12		*	*		V/µs
ANALOG OUTPUT							
Voltage Range ($\pm V_{CC}$ = 15V)[8]: Unipolar		0 to +10			*		V
Bipolar		±5, ±10			*		V
Output Current	±5			*			mA
Output Impedance (at DC)		0.2			*		Ω
Short Circuit to Common Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+6.2	+6.3	+6.4	*	*	*	V
Source Current Available for External Loads	+2			*			mA
Temperature Coefficient		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	VDC
V_{DD}	+4.5	+5	+5.5	*	*	*	VDC
Current (no load): $+V_{CC}$		+16	+25		*	*	mA
$-V_{CC}$		–23	–35		*	*	mA
V_{DD}		+8	+15		*	*	mA
Potential at DCOM with Respect to ACOM[9]		±0.5			*		V
Power Dissipation		625	800		*	*	mW
TEMPERATURE RANGE							
Specification: J, K	0		+70	*		*	°C
A, B	–25		+85	*		*	°C
R, S	–65		+150	*		*	°C
							°C
Storage: J, K	–60		+100	*		*	°C
A, B, R, S	–65		+150	*		*	°C

* Specification same as DAC811AH, JP, JU.

NOTES: (1) USB = unipolar straight binary; BOB = bipolar offset binary. (2) TTL, LSTTL and 54/74 HC compatible. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means full scale range and is 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least –8V to +8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	$+V_{DD}$	Logic supply, +5V.
2	$\overline{WR}$	Write, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	Load D/A converter, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	Nibble A, enables $\overline{WR}$ to load input latch A (the most significant nibble). Logic low enables.
5	$\overline{N_B}$	Nibble B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	Nibble C, enables $\overline{WR}$ to load input latch C (the least significant nibble). Logic low enables.
7	D_{11}	Data bit 12, MSB, positive true.
8	D_{10}	Data bit 11.
9	D_9	Data bit 10.
10	D_8	Data bit 9.
11	D_7	Data bit 8.
12	D_6	Data bit 7.
13	D_5	Data bit 6.
14	D_4	Data bit 5.
15	DCOM	Digital common, V_{DD} supply return.
16	D_0	Data bit 1, LSB.
17	D_1	Data bit 2.
18	D_2	Data bit 3.
19	D_3	Data bit 4.
20	$+V_{CC}$	Analog supply input, +15V or +12V.
21	$-V_{CC}$	Analog supply input, –15V or –12V.
22	Gain Adj	To externally adjust gain.
23	ACOM	Analog common, $\pm V_{CC}$ supply return.
24	V_{OUT}	D/A converter voltage output.
25	10V Range	Connect to pin 24 for 10V range.
26	SJ	Summing junction of output amplifier.
27	BPO	Bipolar offset. Connect to pin 26 for bipolar operation.
28	Ref Out	6.3V reference output.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (Pins 2–14, 16–19) to DCOM	–0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
Ref Out	Indefinite Short to ACOM
External Voltage Applied to DAC Output	–5V to +5V
Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, θ_{J-A}: Plastic DIP and SOIC	100°C/W
Ceramic DIP	65°C/W

NOTE: Stresses above those listed above may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

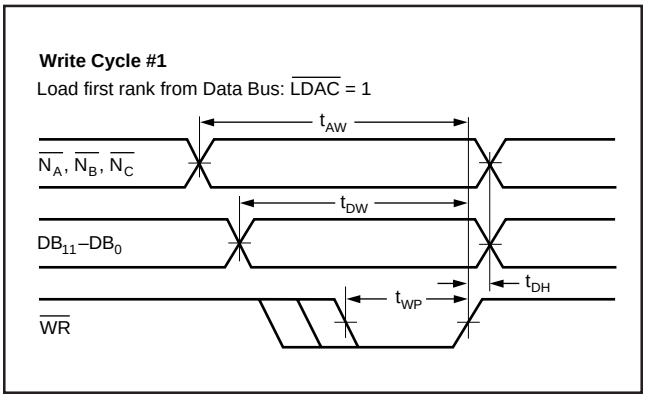
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

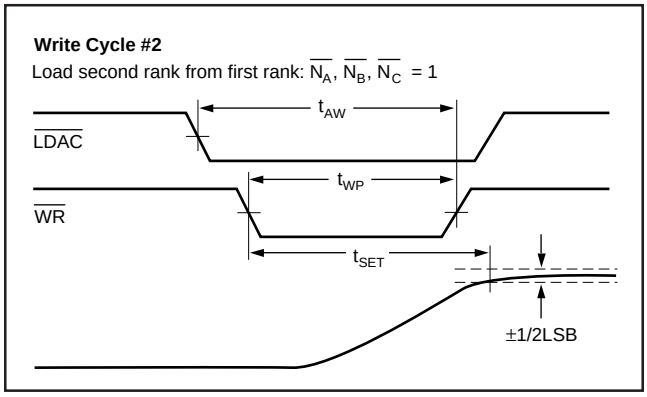
PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL LINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC811AH	±1/2 LSB	3/4	CERDIP-28	149	–25°C to +85°C	DAC811AH	Rails
DAC811JP	±1/2 LSB	3/4	DIP-28	215	0°C to +70°C	DAC811JP	Rails
DAC811JU	±1/2 LSB	3/4	SO-28	217	0°C to +70°C	DAC811JU	Rails
"	"	"	"	"	"	DAC811JU/1K	Tape and Reel
DAC811KP	±1/4 LSB	1/2	DIP-28	215	0°C to +70°C	DAC811KP	Rails
DAC811KU	±1/4 LSB	1/2	SO-28	217	0°C to +70°C	DAC811KU	Rails

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC811JU/1K" will get a single 1000-piece Tape and Reel.

TIMING DIAGRAMS





DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive-true binary input codes. DAC811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC(1) Binary Two's Complement
111111111111	+ Full Scale	+ Full Scale	–1LSB
100000000000	+ 1/2 Full Scale	Zero	– Full Scale
011111111111	+ 1/2 Full Scale – 1LSB	–1LSB	+ Full Scale
000000000000	Zero	– Full Scale	Zero

NOTE: (1) Invert MSB of the BOB code with external inverter to obtain BTC code.

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all 1s and all 0s). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for B and K grades, and ±1/2LSB (max) for A and J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC811 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range (FSR) output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full scale range value (e.g., +FS minus –FS) at high temperature, +25°C, and low temperature, calculating the error with respect to the +25°C value, and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0s on the input over the specification temperature range. Offset is measured at high temperature, +25°C, and low temperature. The offset drift is the maximum change in offset referred to the +25°C value, divided by the temperature change. It is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.1V. The reference output may be used to drive external loads, sourcing at least 2mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

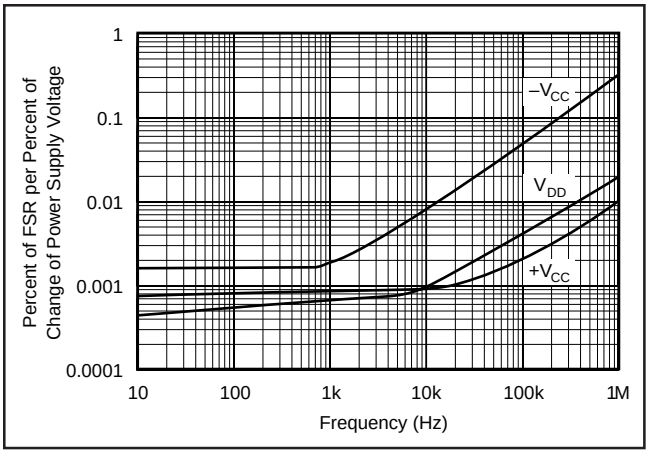


FIGURE 1. Power Supply Rejection vs Power Supply Ripple Frequency.

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$, and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic 0. When either $\overline{N_A}$, ($\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic 1, the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic 0.

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic 0. When either $\overline{LDAC}$ or $\overline{WR}$ are at logic 1, the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic 0.

All latches are level-triggered. Data present when the control signals are logic 0 will enter the latch. When any one of the control signals returns to logic 1, the data is latched. Table II is a truth table for all latches.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No operation
0	0	1	1	1	Enables input latch 4MSBs
0	1	0	1	1	Enables input latch 4 middle bits
0	1	1	0	1	Enables input latch 4LSBs
0	1	1	1	0	Loads D/A latch from input latches
0	0	0	0	0	Makes all latches transparent

"X" = Don't care.

TABLE II. DAC813 Interface Logic Truth Table.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output, and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

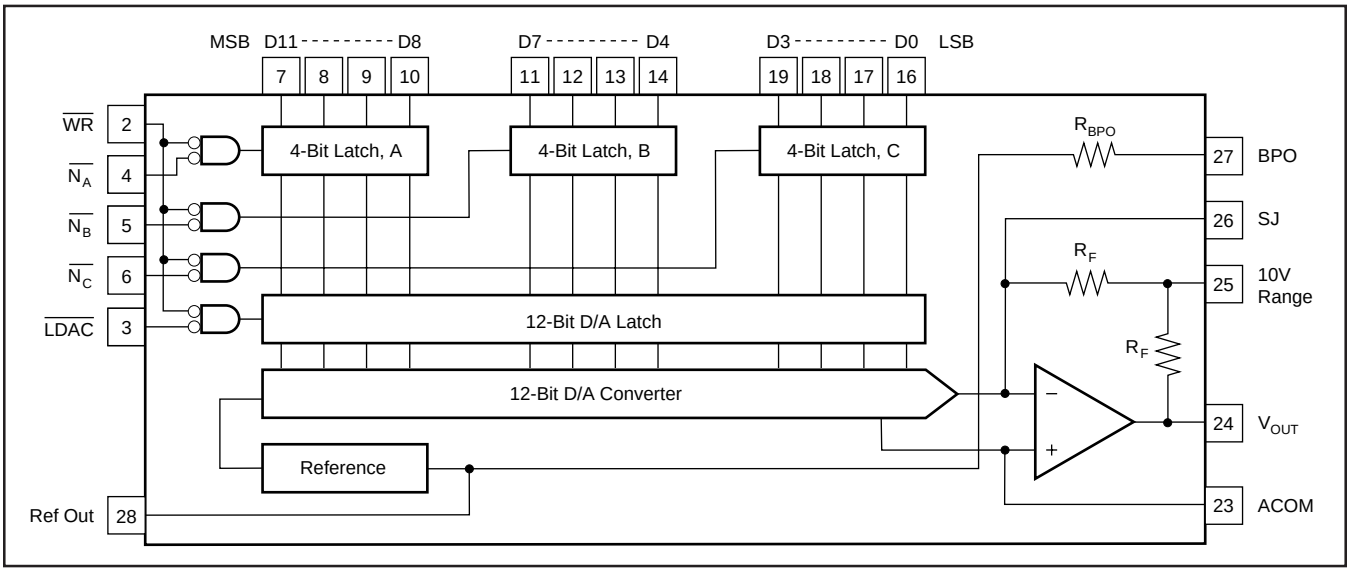


FIGURE 2. DAC811 Block Diagram.

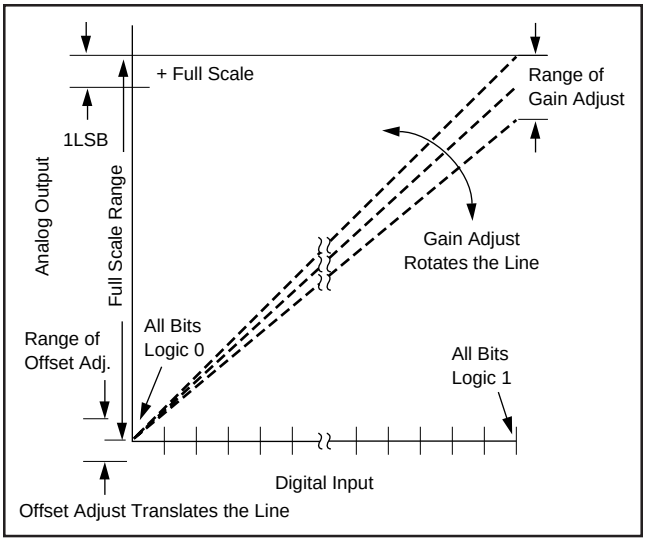


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

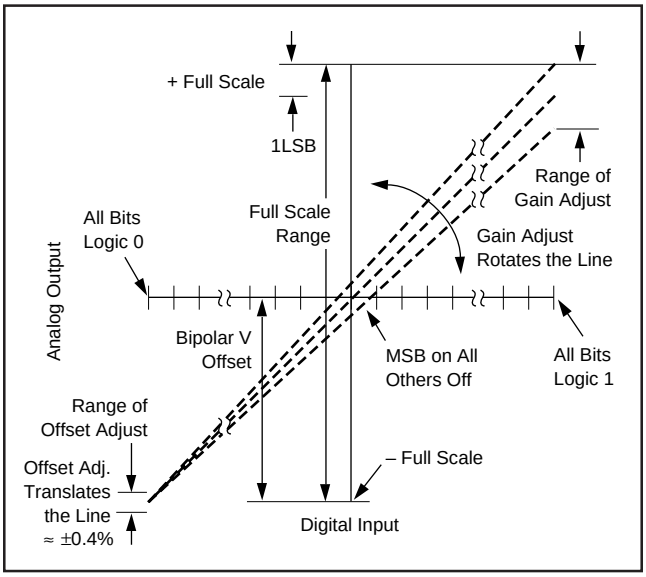


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT		
	0 to +10V	±5V	±10V
MSB LSB ↓ ↓			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5V	0V	0V
011111111111	+4.9976V	–0.0024V	–0.0049V
000000000000	0V	–5V	–10V
LSB	2.4mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12VB supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TLL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B and 54/74C CMOS devices.

Resistors of 47Ω should be placed in series with D0 through D11, $\overline{WR}$, $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ if edges are <10ns or if the logic input is driven below ground by undershoot.

INSTALLATION

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in Figure 5.

These capacitors (1µF tantalum recommended) should be located close to the DAC811.

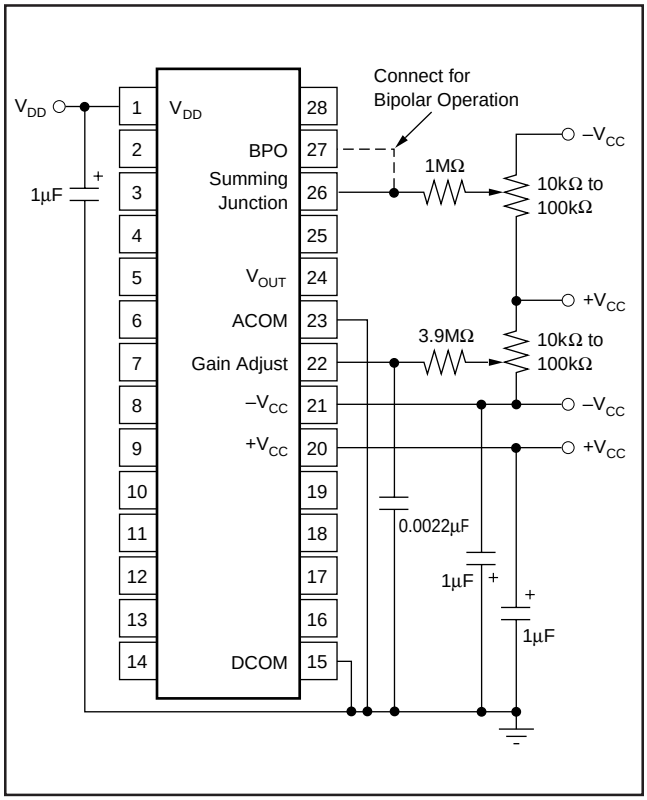


FIGURE 5. Power Supply, Gain, and Offset Potentiometer Connections.

DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The analog common (pin 23) and digital common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiometers should be 100ppm/°C or less. The 1MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001µF to 0.01µF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment. Excessive capacitance on the Gain Adjust or Offset Adjust pin may affect slew rate and settling time.

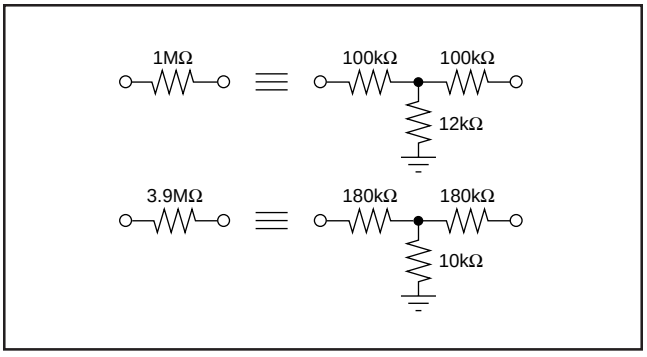


FIGURE 6. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or a unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.

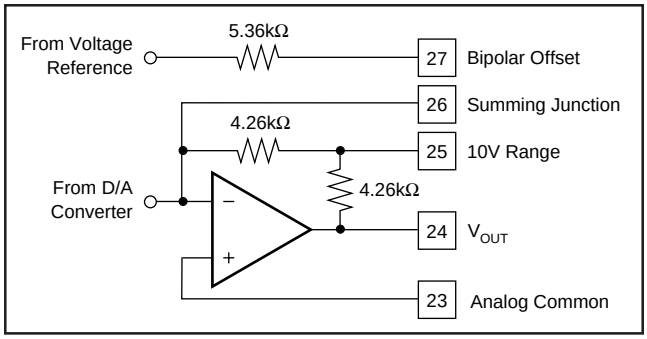


FIGURE 7. Output Amplifier Voltage Range Scaling Circuit.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 25 TO	CONNECT PIN 27 TO
0 to +10V	USB	24	23
±5	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

TABLE IV. Output Range Connections.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface to microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether. For instance, if half the memory space is unused, address line A15 of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each DAC811 occupies four address locations. A 74LS139 provides the two-to-four decoder and selects it with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. An 8205 decoder is an alternative to the 74LS139.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right-justified data formats, as illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 10 and 11 show an addressing scheme for right-justified and left-justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right-justified case, $X10_{16}$ loads the 8LSBs, and $X01_{16}$ loads the 4MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

Left-justified data is handled in a similar manner, shown in Figure 11. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.

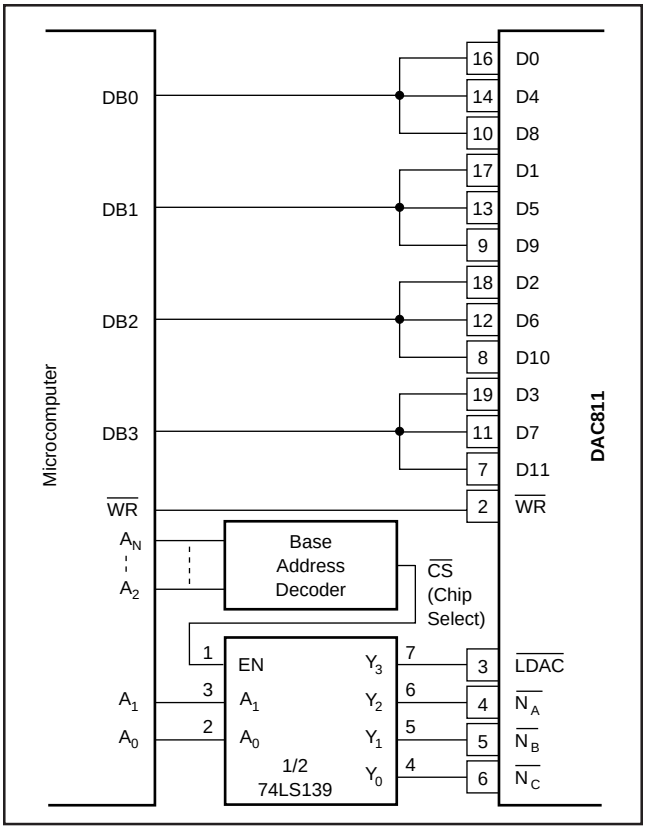


FIGURE 8. Addressing and Control for 4-Bit Microcomputer Interface.

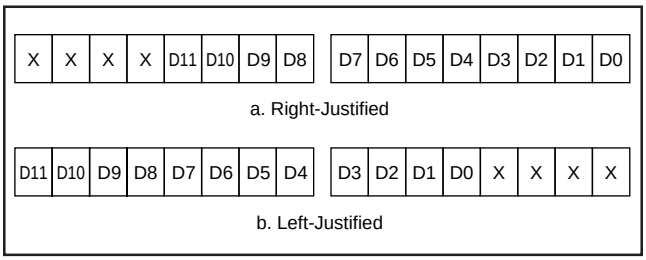


FIGURE 9. 12-Bit Data Format for 8-Bit Systems.

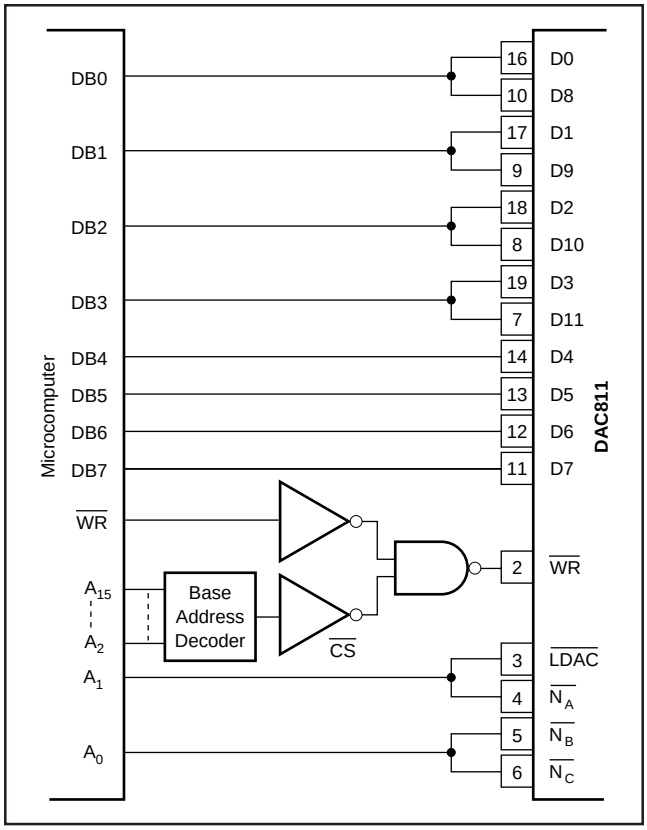


FIGURE 10. Right-Justified Data Bus Interface.

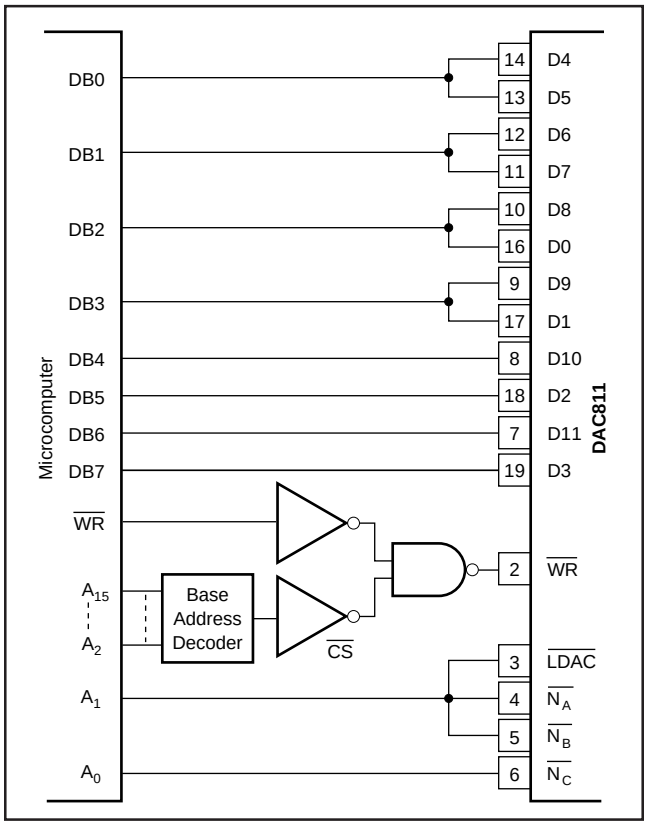


FIGURE 11. Left-Justified Data Bus Interface.

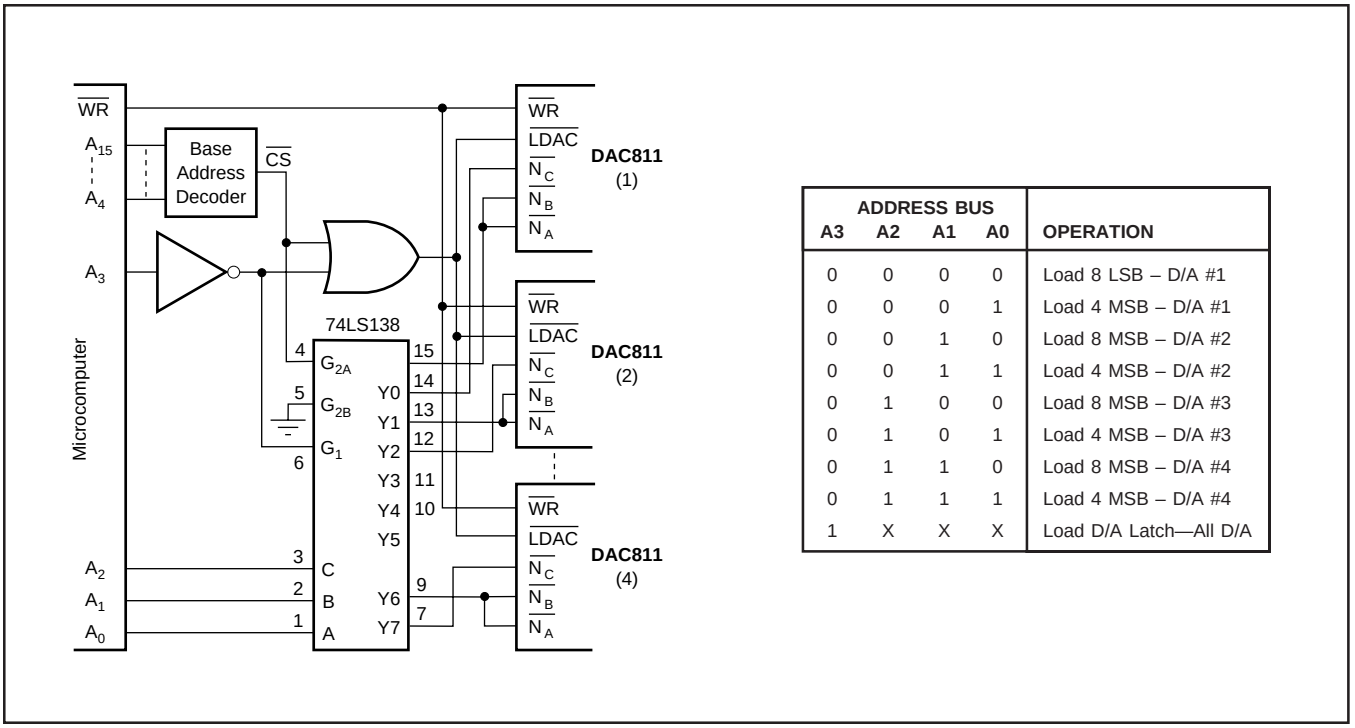
INTERFACING MULTIPLE DAC811s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 12 uses a 74LS138 decoder to decode a set of eight adjacent addresses, to load the input latches of four DAC811s. The example shows a right-justified data format.

A ninth address using A_3 causes all DAC811s to be updated simultaneously. If a particular DAC811 is always loaded last—for instance, D/A #4—A_3 is not needed, thus saving eight address spaces for other uses. Incorporate A_3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application, the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$ and $\overline{N_C}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC811, is selected by the address decoder and strobed by $\overline{WR}$.



ADDRESS BUS A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 MSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 MSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 MSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 12. Interfacing Multiple DAC811s to an 8-Bit Bus.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC811BH	ACTIVE	CDIP SB	JD	28	1	RoHS & Green	AU	N / A for Pkg Type	-25 to 85	DAC811BH	Samples
DAC811JU	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	DAC811JU	Samples
DAC811JU/1K	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	DAC811JU	Samples
DAC811JUG4	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	DAC811JU	Samples
DAC811KU	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	DAC811KU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

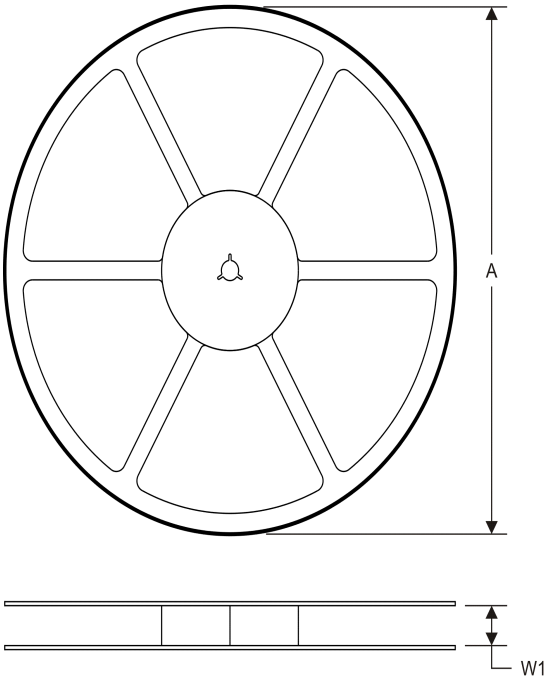
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

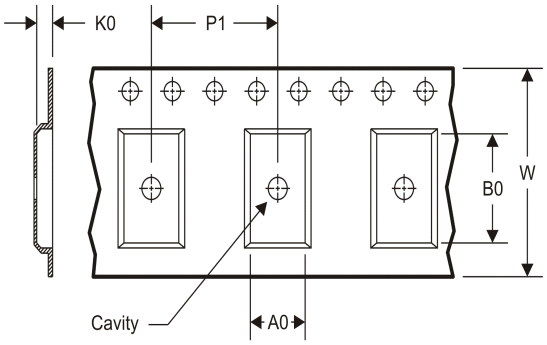
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



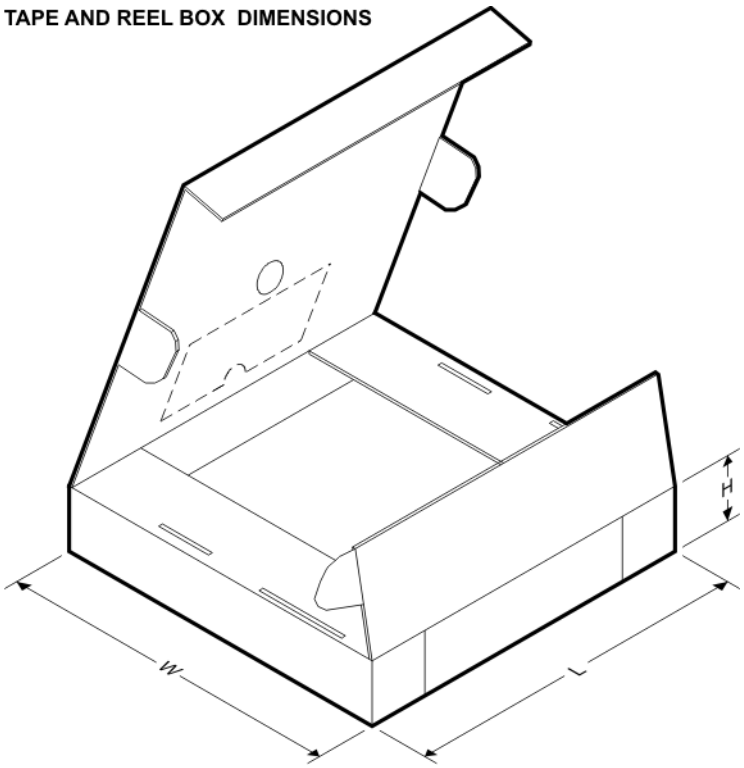
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC811JU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC811JU/1K	SOIC	DW	28	1000	367.0	367.0	55.0

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