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AMC7836 12 位高密度模拟监视和控制解决方案,具有多通道模数转换器 (ADC)、双极数模转换器 (DAC)、温度传感器和通用输入输出 (GPIO) 端口

Technical

Documents

- 1 特性
- 16 个单调性 12 位 DAC
 - 可选范围: -10V 至 0V、-5V 至 0V、0V 至 5V、0V 至 10V
 - 高电流驱动能力: 高达 ±15mA
 - 自动范围检测器
 - 可选钳位电压
- 12 位逐次逼近寄存器 (SAR) ADC
 - 21 个外部模拟输入
 - 16 个双极输入: -12.5V 至 12.5V
 - 5 个高精度输入: 0V 至 5V
 - 可编程超限报警
- 2.5V 内部电压基准
- 内部温度传感器
 - 运行温度范围: -40℃ 至 +125℃
 - **±2.5°C**精度
- 8 个通用 I/O 端口 (GPIO)
- 兼容串行外设接口 (SPI) 的低功耗串行接口
 4 线制模式,运行电压为 1.8V 至 5.5V
- 工作温度范围: -40°C 至 +125°C
- 采用 64 引脚耐热增强型薄型四方扁平 (HTQFP) 封装 PowerPAD™IC 封装
- 2 应用
- 通信基础设施:
 - 蜂窝基站
 - 微波回程
 - 光纤网络
- 通用监视器和控制
- 数据采集系统

3 说明

🥭 Tools &

Software

AMC7836 是一款高度集成的低功耗、模拟监视和控制 解决方案。该器件包含一个 21 通道 12 位模数转换器 (ADC)、16 个具有可编程输出范围的 12 位数模转换器 (DAC)、8 个 GPIO、一个内部基准电压以及一个本地 温度传感器通道。该器件的高度集成特性显著减少组件 数量,同时简化了闭环系统设计,因此非常适合 对电 路板空间、尺寸和低功耗严格要求的多通道应用。

该器件具有低功耗、超高集成度和宽工作温度范围等诸 多优势,因此适合用作多通道射频 (RF) 通信系统中功 率放大器 (PA) 的一体化、低成本偏置控制电路。凭借 灵活的 DAC 输出范围,该器件可用作适用于多种晶体 管技术(例如 LDMOS、GaA 和 GaN)的偏置解决方 案。AMC7836 功能集对通用监视器和控制系统而言同 样有益。

为满足 各类应用 对不同通道数、 附加特性、或转换器 分辨率的需求, 德州仪器 (TI) 提供了完备的模拟监视 和控制 (AMC) 产品系列。更多信息, 敬请访问 www.ti.com.cn/amc。

器件信息⁽¹⁾

器件型号	封装	封装尺寸(标称值)	
AMC7836	HTQFP (64)	10.00mm x 10.00mm	

(1) 如需了解所有可用封装,请参阅产品说明书末尾的可订购产品 附录。







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4 修订历史记录

注: 之前版本的页码可能与当前版本有所不同。

Changes from Revision C (April 2016) to Revision D

•	Changed 4.5 V to 4.7 V in AV _{DD} description in Pin Functions	. 4
•	Changed 4.5 V to 4.7 V in DV _{DD} description in Pin Functions	. 5
•	Changed Supply voltage, AV_{DD} MIN value from 4.5 V to 4.7 V \ldots	. 7
•	Changed Supply voltage, DV _{DD} MIN value from 4.5 V to 4.7 V	. 7
•	Changed Supply voltage, AV _{CC} MIN value from 4.5 V to 4.7 V \ldots	. 7
•	Changed $AV_{DD} = DV_{DD} = 4.5$ to 5.5 V to $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V in Electrical Characteristics: DAC conditions	. 8
•	Changed $AV_{DD} = DV_{DD} = 4.5$ to 5.5 V to $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V in Electrical Characteristics: ADC and Temperature Sensor conditions	10
•	Changed $AV_{DD} = DV_{DD} = 4.5$ to 5.5 V to $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V in Electrical Characteristics: General conditions	11
•	Changed $AV_{DD} = DV_{DD} = 4.5$ to 5.5 V to $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V in Timing Requirements conditions	12
•	Added paragraph and Figure 59 to Internal Reference section	37
•	Changed 4.5 V to 4.7 V in All-Negative DAC Range Mode section	40
•	已添加 paragraph to Power Supply Recommendations section	77
•	已添加 paragraph to Power Supply Recommendations section	78

Changes from Revision B (February 2015) to Revision C

•	Changed Figure 117; corrected pins 63 and 64	74
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Changes from Revision A (November 2014) to Revision B

•	件状态"产品预览"至"量产数据"

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5 Pin Configuration and Functions



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INSTRUMENTS

Texas

	Pin Functions				
PIN	l		DESCRIPTION		
NAME	NO.	I/O	DESCRIPTION		
ADC_0	47	I			
ADC_1	46	I	Bipolar analog inputs. These pins are typically used to monitor the DAC group-C outputs. The		
ADC_2	45	I	input range of these channels is -12.5 to 12.5 V.		
ADC_3	44	I			
ADC_4	43	I			
ADC_5	42	I	Bipolar analog inputs. These pins are typically used to monitor the DAC group-D outputs. The		
ADC_6	41	I	input range of these channels is -12.5 to 12.5 V.		
ADC_7	40	I			
ADC_8	34	I			
ADC_9	33	I	Bipolar analog inputs. These pins are typically used to monitor the DAC group-B outputs. The		
ADC_10	32	I	input range of these channels is -12.5 to 12.5 V.		
ADC_11	31	I			
ADC_12	30	I			
ADC_13	29	I	Bipolar analog inputs These pips are typically used to monitor the DAC group-A outputs. The		
ADC_14	28	I	input range of these channels is -12.5 to 12.5 V.		
ADC_15	27	I			
AGND1	21	I	Analog ground. These pins are the ground reference point for all analog circuitry on the device.		
AGND2	48	1	Connect the AGND1, AGND2, and AGND3 pins to the same potential (AGND). Ideally, the		
AGND3	56	I	analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3 V.		
			Positive analog power for DAC groups A and B. The AV _{CC_AB} and AV _{CC_CD} pins must be connected to the same potential (AV _{CC}).		
AV _{CC_AB}	20	1			
AV _{CC_CD}	57	I	Positive analog power for DAC groups C and D. The AV _{CC_AB} and AV _{CC_CD} pins must be connected to the same potential (AV _{CC}).		
AV _{DD}	50	I	Analog supply voltage (4.7 V to 5.5 V). This pin must have the same value as the DV_{DD} pin.		
AV _{EE}	17	I	Lowest potential in the system. This pin is typically tied to a negative supply voltage but if all DACs are set in a positive output range, this pin can be connected to the analog ground. This pin also acts as the negative analog supply for DAC group A. This pin sets the power-on-reset and clamp voltage values for the DAC group A.		
AV _{SSB}	24	I	Negative analog supply for DAC group B. This pin sets the power-on-reset and clamp voltage values for the DAC group B. This pin is typically tied to the AV_{EE} pin for the negative output ranges or AGND for the positive output ranges.		
AV _{SSC}	53	I	Negative analog supply for DAC group C. This pin sets the power-on-reset and clamp voltage values for the DAC group C. This pin is typically tied to the AV_{EE} pin for the negative output ranges or AGND for the positive output ranges.		
AV _{SSD}	60	I	Negative analog supply for DAC group D. This pin sets the power-on-reset and clamp voltage values for the DAC group D. This pin is typically tied to the AV_{EE} pin for the negative output ranges or AGND for the positive output ranges.		
CS	6	I	Active-low serial-data enable. This input is the frame-synchronization signal for the serial data. When this signal goes low, it enables the serial interface input shift register.		
DAC_A0	15	0			
DAC_A1	16	0	DAC group A. These DAC channels share the same range and clamp voltage. If any of the		
DAC_A2	18	0	voltage range as well.		
DAC_A3	19	0			
DAC_B4	22	0			
DAC_B5	23	0			
DAC_B6	25	0	DAG group b. These DAG channels share the same range and clamp voltage.		
DAC_B7	26	0			





Pin Functions (continued)

PIN			DESCRIPTION	
NAME	NO.	I/O	DESCRIPTION	
DAC_C8	51	0		
DAC_C9	52	0	DAC group C. Those DAC channels share the same range and clamp voltage	
DAC_C10	54	0	DAG group C. These DAG channels share the same range and clamp voltage.	
DAC_C11	55	0		
DAC_D12	58	0		
DAC_D13	59	0	DAC group D. These DAC channels share the same range and clamp voltage	
DAC_D14	61	0	bao group D. These bao champers share the same range and clamp voltage.	
DAC_D15	62	0		
DGND	64	I	Digital ground. This pin is the ground reference point for all digital circuitry on the device. Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ± 0.3 V.	
DV _{DD}	63	I	Digital supply voltage (4.7 V to 5.5 V). This pin must have the same value as the ${\rm AV}_{\rm DD}$ pin.	
GPIO0/ALARMIN	7	I/O	General-purpose digital I/O 0 (default). This pin is a bidirectional digital input/output (I/O) with an internal 48-k Ω pullup resistor to the IOV _{DD} pin. Alternatively the pin can be set to operate as the digital input ALARMIN which is an active-low alarm-control signal. If unused this pin can be left floating.	
GPIO0/ALARMOUT	8	I/O	General purpose digital I/O 1 (default). This pin is a bidirectional digital I/O with an internal 48- k Ω pullup resistor to the IOV _{DD} pin. Alternatively the pin can be set to operate as ALARMOUT which is an open drain global alarm output. This pin goes low (active) when an alarm event is detected. If unused this pin can be left floating.	
GPIO2/ADCTRIG	9	I/O	General purpose digital I/O 2 (default). This pin is a bidirectional digital I/O with internal 48-k Ω pullup resistor to the IOV _{DD} pin. Alternatively the pin can be set to operate as ADCTRIG which is an active-low external conversion trigger. The falling edge of this pin begins the sampling and conversion of the ADC. If unused this pin can be left floating.	
GPIO3/DAV	10	I/O	General purpose digital I/O 3 (default). This pin is a bidirectional digital I/O with internal 48-k Ω pullup resistor to the IOV _{DD} pin. Alternatively the pin can be set to operate as DAV which is an active-low data-available indicator output. In direct mode, the DAV pin goes low (active) when the conversion ends. In auto mode, a 1-µs pulse (active low) appears on this pin when a conversion cycle finishes. The DAV pin remains high when deactivated. If unused this pin can be left floating.	
GPIO4	11	I/O		
GPIO5	12	I/O	General purpose digital I/O. These pins are bidirectional digital I/Os with an internal 48-k Ω	
GPIO6	13	I/O	pullup resistor to the IOV _{DD} pin. If unused these pins can be left floating.	
GPIO7	14	I/O		
IOV _{DD}	1	I	I/O supply voltage (1.8 V to 5.5 V). This pin sets the I/O operating voltage and threshold levels. The voltage on this pin must not be greater than the value of the DV_{DD} pin.	
LV_ADC16	39	I		
LV_ADC17	38	I		
LV_ADC18	37	I	General purpose analog inputs. These channels are used for general monitoring. The input range of these pins is 0 to 2 x V_{rot} .	
LV_ADC19	36	I		
LV_ADC20	35	I		
REF_CMP	49	0	Internal-reference compensation-capacitor connection. Connect a 4.7- μF capacitor between this pin and the AGND2 pin.	
RESET	2	I	Active-low reset input. Logic low on this pin causes the device to perform a hardware reset.	
SCLK	5	I	Serial interface clock.	
SDI	4	I	Serial-interface data input. Data is clocked into the input shift register on each rising edge of the SCLK pin.	
SDO	3	0	Serial-interface data output. The SDO pin is in high impedance when the \overline{CS} pin is high. Data is clocked out of the input shift register on each falling edge of the SCLK pin.	
Thermal Pad	_	I	The thermal pad is located on the bottom-side of the device package. The thermal pad should be tied to the same potential as the AV_{EE} pin or left disconnected.	

Specifications 6

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	МАХ	UNIT		
	AV _{DD} to GND	-0.3	6			
	DV _{DD} to GND	ND -0.3 6				
	IOV _{DD} to GND	-0.3	6			
	AV _{CC} to GND	-0.3	18			
Supply Voltage	AV _{EE} to GND	-13	0.3	V		
	$AV_{SSB}, AV_{SSC}, AV_{SSD}$ to AV_{EE}	-0.3	13			
	AV_{CC} to AV_{SSB} , AV_{SSC} , or AV_{SSD}	-0.3	26			
	AV _{CC} to AV _{EE}	-0.3	26			
	DGND to AGND	-0.3	0.3			
	ADC_[0-15] analog input voltage to GND	-13	13	V		
	LV_ADC[16-20] analog input voltage to GND	-0.3	AV _{DD} + 0.3			
	DAC_A[0-3] outputs to GND	AV _{EE} – 0.3	AV _{CC} + 0.3			
	DAC_B[4-7] outputs to GND	AV _{SSB} – 0.3	AV _{CC} + 0.3			
	DAC_C[8-11] outputs to GND	$AV_{SSC} - 0.3$	$AV_{CC} + 0.3$			
Pin voltage	DAC_D[12-15] outputs to GND	$AV_{SSD} - 0.3$	$AV_{CC} + 0.3$	v		
	REF_CMP to GND	-0.3	AV _{DD} + 0.3			
	CS, SCLK, SDI and RESET to GND	-0.3	IOV _{DD} + 0.3			
	SDO to GND	-0.3	$IOV_{DD} + 0.3$			
	GPIO[0-7] to GND	-0.3	$IOV_{DD} + 0.3$			
	ADC_[0:15] analog input current	-10	10			
Pin Current	LV_ADC[16:20] analog input current	-10	10	mA		
	GPIO[0:7] sinking current		5			
Operating temperature		-40	125	°C		
Junction temperature, T	Г _J max	-40	150	°C		
Storage temperature, T	age temperature, T _{stg} -40 150		°C			

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 $^{\left(2\right) }$	±250	V

JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
 JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	AV _{DD}	4.7	5	5.5	V
	DV _{DD} ⁽¹⁾	4.7	5	5.5	
Supply voltage	IOV _{DD} ⁽²⁾	1.8		5.5	
	AV _{CC}	4.7	12	12.5	
	AV _{EE}	-12.5	-12	0	
	AV _{SSB} , AV _{SSC} , AV _{SSD}	AV _{EE}		0	
Specified operating temperature		-40	25	105	°C
Operating temperature		-40	25	125	°C

(1)

The value of the DV_{DD} pin must be equal to that of the AV_{DD} pin. The value of the IOV_{DD} pin must be less than or equal to that of the DV_{DD} pin. (2)

6.4 Thermal Information

		AMC7836	
	THERMAL METRIC ⁽¹⁾	PAP (HTQFP)	UNIT
		64 PINS	
R_{\thetaJA}	Junction-to-ambient thermal resistance	26.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ΨJT	Junction-to-top characterization parameter	0.2	°C/W
Ψјв	Junction-to-board characterization parameter	9	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

TEXAS INSTRUMENTS

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6.5 Electrical Characteristics: DAC

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V, $AV_{CC} = 12$ V, $IOV_{DD} = 1.8$ to 5.5 V, AGND = DGND = 0 V, $AV_{EE} = AV_{SSE} = AV_{SSC} = AV_{SSD} = -12$ V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0 to 10 V for all groups, no load on the DACs, $T_A = -40^{\circ}$ C to 105°C

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
DAC D	C ACCURACY				
	Resolution		12		Bits
		Measured by line passing through codes 020h and FFFh. 0 to 10 V and -10 to 0 V ranges	±0.3	±1	
INL	Relative accuracy	Measured by line passing through codes 040h and FFFh. 0 to 5 V and –5 to 0 V ranges	±0.5	±1.5	LSB
	Differential and in a site	Specified monotonic. Measured by line passing through codes 020h and FFFh. 0 to 10 V and -10 to 0 V ranges	±0.03	±1	
DINL	Direferitiar nonlinearity	Specified monotonic. Measured by line passing through codes 020h and FFFh. 0 to 5 V and -5 to 0 V ranges	±0.06	±1	LSB
		T _A = 25°C, 0 to 10 V range	±2.5	±20	
TUE	Total upodivisted error ⁽¹⁾	$T_A = 25^{\circ}C$, -10 to 0 V range	±2.5	±20	
TUE	I otal unadjusted error	$T_A = 25^{\circ}C$, 0 to 5 V range	±1.5	±15	mv
		$T_A = 25^{\circ}C, -5 \text{ to } 0 \text{ V range}$	±1.5	±15	
	Offset error	$T_{\rm A}$ = 25°C, Measured by line passing through codes 020h and FFFh. 0 to 10 V range	±0.25	±5	mV
		$T_{\rm A}$ = 25°C, Measured by line passing through codes 040h and FFFh. 0 to 5 V range	±0.25	±5	
	Zana anda anna	T _A = 25°C, Code 000h, -10 to 0 V range	±1	±25	mV
	Zero-code error	$T_A = 25^{\circ}C$, Code 000h, -5 to 0 V range	±1	±25	
		$T_{\rm A}$ = 25°C, Measured by line passing through codes 020h and FFFh, 0 to 10 V range	±0.01	±0.2	%FSR
	- (1)	T_A = 25°C, Measured by line passing through codes 020h and FFFh, –10 to 0 V range	±0.01	±0.2	
	Gain error "	T_{A} = 25°C, Measured by line passing through codes 040h and FFFh, 0 to 5 V range	±0.01	±0.2	
		$T_{\rm A}$ = 25°C, Measured by line passing through codes 040h and FFFh, –5 to 0 V range	±0.01	±0.2	
	Offeret terrereture en filisient	0 to 10 V range	±1		/0 O
	Onset temperature coefficient	0 to 5 V range	±1		ppm/°C
	7	-10 to 0 V range	±2		/0 O
	Zero-code temperature coefficient	-5 to 0 V range	±2		ppm/°C
		0 to 10 V range	±2.5		
	Coin tomporature coefficient $^{(1)}$	-10 to 0 V range	±2.5		ppm/°C
	Gain temperature coefficient."	0 to 5 V range	±2.5		
		–5 to 0 V range	±2.5		

(1) The internal reference contribution not included.



Electrical Characteristics: DAC (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V, $AV_{CC} = 12$ V, $IOV_{DD} = 1.8$ to 5.5 V, AGND = DGND = 0 V, $AV_{EE} = AV_{SSB} = AV_{SSC} = AV_{SSD} = -12$ V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0 to 10 V for all groups, no load on the DACs, $T_A = -40^{\circ}$ C to 105°C

PARAMETER	TEST CONDITIONS MIN TYP MAX			MAX	UNIT	
DAC OUTPUT CHARACTERISTICS						
Full-scale output voltage range ⁽²⁾	Set at power-up or reset through auto-range detection. The output range can be modified after power-up or reset through the DAC range registers (address 0x1E through 0x1F). DAC-RANGE = 100b	-10		0		
	The output range can be modified after power-up or reset through the DAC range registers (address 0x1E through 0x1F). DAC-RANGE = 101b-5Set at power-up or reset through auto-range detection. The output range can be modified after power-up or reset through the DAC range registers (address 0x1E through 0x1F). DAC-RANGE = 111b0			0	M	
			5	V		
	The output range can be modified after power-up or reset through the DAC range registers (address 0x1E through 0x1F). DAC-RANGE = 110b	0		10		
Output voltage pottling time	Transition: Code 400h to C00h to within ½ LSB, R _L = 2 kΩ, C _L = 200 pF. 0 to 10 V and –10 to 0 V ranges		10			
Output voltage settling time	Transition: Code 400h to C00h to within ½ LSB, R _L = 2 k Ω , C _L = 200 pF. 0 to 5 V and –5 to 0 V ranges		10		μs	
Slew rate	Transition: Code 400h to C00h, 10% to 90%, R_L = 2 $k\Omega$, C_L = 200 pF. 0 to 10 V and –10 to 0 V ranges		1.25		V/µs	
	Transition: Code 400h to C00h, 10% to 90%, R_L = 2 k\Omega, C_L = 200 pF. 0 to 5 V and –5 to 0 V ranges		1.25			
Short circuit current	Short circuit current Full-scale current shorted to the DAC group AV _{SS} or AV _{CC} voltage ±45			mA		
	Source or sink with 1-V headroom from the DAC group AV_{CC} or AV_{SS} voltage, voltage drop < 25 mV	±15			0	
Load current.	Source or sink with 300-mV headroom from the DAC group AV_{CC} or AV_{SS} voltage, voltage drop < 25 mV	±10			mA	
Maximum capacitive load ⁽⁴⁾	R _L = ∞	0		10	nF	
DC output impedance	Code set to 800h, ±15mA		1		Ω	
Power-on overshoot	$AV_{EE} = AV_{SSB} = AV_{SSC} = AV_{SSD} = AGND, AV_{CC} = 0$ to 12 V, 2-ms ramp		10		mV	
Glitch energy	Transition: Code 7FFh to 800h; 800h to 7FFh		1		nV-s	
Output noise	$T_A = 25^{\circ}C$, 1 kHz, code 800h, includes internal reference noise		520		nV/√Hz	
	$T_A = 25^{\circ}$ C, integrated noise from 0.1 Hz to 10 Hz, code 800h, includes internal reference noise		20		μV _{PP}	
CLAMP OUTPUTS				·		
	DAC output range: 0 to 10 V, AV _{SS} = AGND		0			
	DAC output range: 0 to 5 V, AV _{SS} = AGND		0			
	DAC output range: -10 to 0 V, AV _{SS} = -12 V		AV _{SS} + 2		V	
	DAC output range: -5 to 0 V, AV _{SS} = -6 V		AV _{SS} + 1			
Clamp output impedance			8		kΩ	

(2) The output voltage of each DAC group must not be greater than that of the corresponding AV_{CC} pin (AV_{CC_AB} or AV_{CC_CD}) or lower than that of the corresponding AV_{SS} pin (AV_{EE}, AV_{SSB}, AV_{SSC} or AV_{SSD}). See the *DAC Output Range and Clamp Configuration* section for more details.

(3) If all channels are simultaneously loaded, care must be taken to ensure the thermal conditions for the device are not exceeded.

(4) To be sampled during initial release to ensure compliance; not subject to production testing.

(5) No DAC load to the DAC group AV_{SS} pin.



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6.6 Electrical Characteristics: ADC and Temperature Sensor

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V, $AV_{CC} = 12$ V, $IOV_{DD} = 1.8$ to 5.5 V, AGND = DGND = 0 V, $AV_{EE} = AV_{SSE} = AV_{SSC} = AV_{SSD} = -12$ V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0 to 10 V for all groups, no load on the DACs, $T_A = -40^{\circ}$ C to 105°C

PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT	
Resolution		12			Bits	
	Unipolar input channels		±0.5	±1	LSB	
Integral nonlinearity	Bipolar input channels		±0.5	±1.5		
Differential nonlinearity	Specified monotonic. All input channels		±0.5	±1	LSB	
UNIPOLAR ANALOG INPUTS: LV_ADC16	o LV_ADC20					
Absolute input voltage range		AGND - 0.2		$AV_{DD} + 0.2$	V	
Full scale input range	V _{ref} measured at REF_CMP pin	0		$2 \times V_{ref}$	V	
Input capacitance			34		pF	
DC input leakage current	Unselected ADC input			±10	μA	
Offset error			±1	±5	LSB	
Offset error match			±0.5		LSB	
Gain error ⁽¹⁾			±0.5	±5	LSB	
Gain error match			±1		LSB	
Update time	Single unipolar input, temperature sensor disabled		11.5		μs	
BIPOLAR ANALOG INPUTS: ADC_0 to AD	C_15					
Absolute input voltage range		-13		13	V	
Full scale input range		-12.5		12.5	V	
Input resistance			175		kΩ	
Offset error			±0.25	±5	LSB	
Gain error ⁽¹⁾			±0.5	±5	LSB	
Update time	Single bipolar input, temperature sensor disabled		34.5		μs	
TEMPERATURE SENSOR						
Operating range		-40		125	°C	
Accuracy	$T_A = -40$ °C to 125°C, AV _{DD} = 5 V		±1.25	±2.5	°C	
Resolution	LSB size		0.25		°C	
Update time	All ADC input channels disabled		256		μs	
ADC UPDATE TIME						
Internal oscillator frequency		3.7	4	4.3	MHz	
ADC update time	All 21 ADC inputs enabled, temperature sensor disabled.		609.5		μs	
	All 21 ADC inputs enabled, temperature sensor enabled.		865.5		μs	
INTERNAL REFERENCE (INTERNAL REFERENCE NOT ACCESSIBLE)						
Initial accuracy	$T_A = 25^{\circ}C$	2.4925	2.5	2.5075	V	
Reference temperature coefficient			12	35	ppm/°C	
INTERNAL ADC REFERENCE BUFFER						
Reference buffer offset	$T_A = 25^{\circ}C$			±5	mV	

(1) Internal reference contribution not included.



6.7 Electrical Characteristics: General

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V, $AV_{CC} = 12$ V, $IOV_{VDD} = 1.8$ to 5.5 V, AGND = DGND = 0 V, $AV_{EE} = AV_{SSE} = AV_{SSC} = AV_{SSD} = -12$ V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0 to 10 V for all groups, no load on the DACs, $T_A = -40^{\circ}$ C to 105°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
AV _{SS} DET	ECTOR						
	AV_{SS} threshold detector (AV _{SSTH})		-3.5		-1.5	V	
DIGITAL L	-OGIC: GPIO		L				
	High-level input voltage	IOV _{DD} = 1.8 to 5.5 V	$0.7 \times IOV_{DD}$			V	
		IOV _{DD} = 1.8 V	0.45		0.45		
Low-level input voltage	IOV _{DD} = 2.7 to 5.5 V			$0.3 \times IOV_{DD}$	v		
		IOV _{DD} = 1.8 V, I _(LOAD) = -2 mA	(0.4	V	
	Low-level output voltage	$IOV_{DD} = 5.5 \text{ V}, I_{(LOAD)} = -5 \text{ mA}$			0.4	V	
	Input impedance	To IOV _{DD}	48			kΩ	
DIGITAL L	OGIC: ALL EXCEPT GPIO				÷		
	High-level input voltage	IOV _{DD} = 1.8 to 5.5 V	$0.7 \times IOV_{DD}$			V	
		IOV _{DD} = 1.8 V			0.45	V	
	Low-level input voltage	IOV _{DD} = 2.7 to 5.5 V		($0.3 \times IOV_{DD}$	V	
	High-level output voltage	$I_{(LOAD)} = -1 \text{ mA}$	$IOV_{DD} - 0.4$			V	
	Low-level output voltage	I _(LOAD) = 1 mA			0.4	V	
	High impedance leakage				±5	μA	
	High impedance output capacitance			10		pF	
POWER REQUIREMENTS							
I _{AVDD}	AV _{DD} supply current			6	13.5		
I _{AVCC}	AV _{CC} supply current			7.5	13.5		
I _{AVSS}	AV _{SS} supply current		-13.5	5		mA	
I _{AVEE}	AV _{EE} supply current	No DAC load, all DACs at 800h code and ADC at the fastest auto conversion rate	-3.5	-1.75			
I _{DVDD}	DV _{DD} supply current			1	3		
I _{IOVDD}	IOV _{DD} supply current			1.5	15	μA	
	Power consumption			215		mW	
I _{AVDD}	AV _{DD} supply current			2.5	5		
I _{AVCC}	AV _{CC} supply current			1	2.5		
I _{AVSS}	AV _{SS} supply current		-5	-3		mA	
I _{AVEE}	AV _{EE} supply current	Power-down mode	-3	-1.75			
I _{DVDD}	DV _{DD} supply current			0.75	1.5		
IIOVDD	IOV _{DD} supply current			1.5	15	μA	
	Power consumption			90		mW	

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6.8 Timing Requirements

 $AV_{DD} = DV_{DD} = 4.7$ to 5.5 V, $AV_{CC} = 12$ V, $AV_{EE} = -12$ V, $AGND = DGND = AV_{SSB} = AV_{SSC} = AV_{SSD} = 0$ V, DAC output range = 0 to 10 V for all groups, no load on the DACs, $T_A = -40^{\circ}$ C to 105°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT	
SERIAL II	NTERFACE ⁽¹⁾						
$f_{(\mathrm{SCLK})}$		IOV _{DD} = 1.8 to 2.7 V			15	MHz	
	SULK frequency	IOV _{DD} = 2.7 to 5.5 V			20		
	SCI K pariad ⁽²⁾	IOV _{DD} = 1.8 to 2.7 V	66.67			ns	
ι _p	SOLK period	IOV _{DD} = 2.7 to 5.5 V	50				
t _{PH}	CCLK pulses width high (2)	IOV _{DD} = 1.8 to 2.7 V	30			ns	
	SCLK pulse width high	IOV _{DD} = 2.7 to 5.5 V	23				
	SCI K pulso width $low^{(2)}$	IOV _{DD} = 1.8 to 2.7 V	30			22	
ι _{ΡL}	SOLK pulse width low	IOV _{DD} = 2.7 to 5.5 V	23			ns	
	CDI actum (2)	IOV _{DD} = 1.8 to 2.7 V	10			20	
ι _{su}	SDI selup	IOV _{DD} = 2.7 to 5.5 V	10			ns	
	CDL hald ⁽²⁾	IOV _{DD} = 1.8 to 2.7 V	10			ns	
ι _h	SDI nola	IOV _{DD} = 2.7 to 5.5 V	10				
	SDO driven to tri-	IOV _{DD} = 1.8 to 2.7 V	0		15		
t _(ODZ)	state ⁽³⁾⁽⁴⁾	IOV _{DD} = 2.7 to 5.5 V	0		9	ns	
	SDO tri-state to	IOV _{DD} = 1.8 to 2.7 V	0		23	-	
t(OZD)	driven ⁽³⁾⁽⁴⁾	IOV _{DD} = 2.7 to 5.5 V	0		15	ns	
	CDO sutsut delaw ⁽³⁾⁽⁴⁾	IOV _{DD} = 1.8 to 2.7 V	0		23		
t _(OD)	SDO output delay	IOV _{DD} = 2.7 to 5.5 V	0		15	ns	
	CS setup ⁽²⁾	IOV _{DD} = 1.8 to 2.7 V	5			ns	
t _{su(CS)}		IOV _{DD} = 2.7 to 5.5 V	5				
	$\overline{\mathbf{OO}}$ hold ⁽²⁾	IOV _{DD} = 1.8 to 2.7 V	20				
ι _{h(CS)}		IOV _{DD} = 2.7 to 5.5 V	20			ns	
	later (2)	IOV _{DD} = 1.8 to 2.7 V	10				
t(IAG)	Inter-access gap	IOV _{DD} = 2.7 to 5.5 V	10			ns	
DIGITAL I	LOGIC						
Reset delay; delay-to-normal operation from reset				100	250	μs	
Power-down recovery time					70	μs	
Clamp shutdown delay			100		μs		
Convert pulse width		20			ns		
	Reset pulse width		20			ns	
ADC WAIT state ⁽⁵⁾ ; the wait time from when the ADC enters the IDLE state to when the ADC is ready for trigger			2			μs	

Specified by design and characterization. Not tested during production. (1)

See Figure 1 and Figure 2.

(2) (3) SDO loaded with 10 pF load capacitance for SDO timing specifications.

See Figure 2.

(4) (5) Specified by design; not subject to production testing. See the ADC Sequencing section for more details.





Figure 1. Serial Interface Write Timing Diagram



Figure 2. Serial Interface Read Timing Diagram



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6.9 Typical Characteristics: DAC

At $T_A = 25^{\circ}C$ (unless otherwise noted)































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6.10 Typical Characteristics: ADC

At $T_A = 25^{\circ}C$ (unless otherwise noted)









6.11 Typical Characteristics: Reference

At $T_A = 25^{\circ}C$ (unless otherwise noted)



6.12 Typical Characteristics: Temperature Sensor

At $T_A = 25^{\circ}C$ (unless otherwise noted)





7 Detailed Description

7.1 Overview

The AMC7836 device is a highly-integrated analog-monitoring and control solution capable of voltage and temperature supervision. The AMC7836 device includes the following features:

- Sixteen 12-bit digital-to-analog converters (DACs) with adjustable output ranges
- Output ranges: -10 to 0 V, -5 to 0 V, 0 to 5 V, and 0 to 10 V
- Auto-range detector on device power-up and reset events
- The DACs power-on and clamp voltages can be pin-selected between AGND and a negative voltage
- The DACs can be configured to clamp automatically upon detection of an alarm event
- A multi-channel, 12-bit analog-to-digital converter (ADC) for voltage and temperature sensing
 - Sixteen bipolar inputs: -12.5 to 12.5 V input range
 - Five precision inputs with programmable threshold detectors: 0 to 5 V input range
 - Internal temperature sensor
- Internal 2.5 V precision reference
- Eight general purpose I/O (GPIO) ports
- Communication with the device occurs through a 4-wire SPI-compatible interface supporting 1.8 to 5.5 V operation

The AMC7836 device is characterized for operation over the temperature range of -40° C to 125° C which makes the device suitable for harsh-condition applications. The device is available in a 10-mm × 10-mm 64-pin HTQFP PowerPAD IC package.

The very high-integration of the AMC7836 device makes it an ideal all-in-one, low-cost, bias-control circuit for the power amplifiers (PAs) found in multi-channel RF-communication systems. The flexible DAC output ranges allow the device to be used as a biasing solution for a large variety of transistor technologies such as LDMOS, GaAs, and GaN. The AMC7836 feature set is similarly beneficial in general-purpose monitor and control systems.



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7.2 Functional Block Diagram





7.3 Feature Description

7.3.1 Digital-to-Analog Converters (DACs)

The AMC7836 device features an analog-control system centered on sixteen 12-bit DACs that operate from the internal reference of the device. Each DAC core consists of a string DAC and output-voltage buffer.

The resistor-string structure consists of a series of resistors, each with a value of R. The code loaded to the DAC determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier (see Figure 48). This architecture has inherent monotonicity, voltage output, and low glitch. This architecture is also linear because all the resistors are of equal value.



Figure 48. DAC Resistor String

7.3.1.1 DAC Output Range and Clamp Configuration

The 16 DACs are split into four groups, each with four DACs. All of the DACs in a given group share the same output range and clamp voltage value, however, these settings can be set independently for each DAC group. After power-on or a reset event the following actions take place: the DAC outputs are directed automatically to the corresponding clamp value; the DAC groups output ranges are set by the auto-range detector and; all DAC data registers and data latches are set to the default values. Figure 49 shows a high level block diagram of each DAC in the AMC7836 device.

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Feature Description (continued)



Figure 49. DAC Block Diagram

7.3.1.1.1 Auto-Range Detection

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present in the corresponding AV_{SS} pin (AV_{EE} , AV_{SSB} , AV_{SSC} or AV_{SSD}). When the AV_{SS} voltage of a DAC group is lower than the threshold value, AV_{SSTH} , the output for that DAC group is automatically configured to the –10 to 0 V range. Conversely, if the DAC group AV_{SS} voltage is higher than AV_{SSTH} , the DAC group output is automatically set to the 0 to 5 V range. The auto-range detector results for each DAC group are stored in the general status register (address 0x72).

In addition to a power-on or reset event, the auto-range detector is also enabled by a register write to the DAC power down registers (address 0xB2 through 0xB3) or the device configuration register (address 0x02).

Although the initial output-range setting is determined by the auto-range detector, the output range for each DAC-group can be afterwards configured to any of the available output ranges (-10 to 0 V, -5 to 0 V, 0 to 5 V, or 0 to 10 V) through the DAC range registers (address 0x1E through 0x1F).

NOTE

The power-on-reset and clamp-voltage value of each DAC group is set by the corresponding AV_{SS} pin and is independent of the DAC output range. In some applications, matching the clamp-voltage setting to the operating voltage range is imperative. For those applications, the recommended connections for the AV_{SS} pin are: AGND for the positive output ranges, in which case the clamp voltage is 0 V; a negative supply voltage with a lower value than the minimum DAC output voltage (-5 V or -10 V) for the selected negative output range, in which case the unloaded clamp voltage is determined by the value of the negative supply voltage (see Figure 50).

Although not a recommended operating condition, the device allows a DAC group to operate in a positive output range even if its clamp voltage is negative (AV_{SS} connected to a negative supply voltage).



Feature Description (continued)



Figure 50. DAC Clamp Output vs AV_{SS}

A special distinction must be made for DAC group A as the AV_{SS} pin of this group is the dual-function AV_{EE} pin. Aside from setting the clamp voltage and default output range for the DAC group A, the AV_{EE} pin is also the lowest potential in the device. As a consequence the AV_{EE} voltage is dependent on the other AV_{SS} pin connections. The AV_{EE} pin can only be connected to the analog ground if all the other AV_{SS} pins are also connected to the analog ground. If any of the AV_{SS} pins is connected to a negative voltage, the AV_{EE} pin must also be connected to that voltage (see Table 1).

The full-scale output range for each DAC group is limited by the corresponding AV_{CC} and AV_{SS} values. The maximum and minimum outputs cannot exceed the AV_{CC} voltage or be lower than the AV_{SS} voltage, respectively.

AUTO-RANGE AV _{EE}		AV _{EE} = 2	AGND	$AV_{EE} = V_{NEG}$			
DAC GROUP	DAC	AND CLAMP AC VOLTAGE SELECTION (AV _{SS})	OUTPUT RANGE	CLAMP VOLTAGE CONNECTION	OUTPUT RANGE	CLAMP VOLTAGE CONNECTION	
	DAC_A0			AGND	–5 to 0 V or –10 to 0 V	V _{NEG}	
Δ	DAC_A1	A\/					
~	DAC_A2	AVEE	0103 010101010				
	DAC_A3						
	DAC_B4	AV _{SSB}				$5 \pm 0 \times cr$ 10 $\pm 0 \times c$	
DAC_B5	DAC_B5		0 to 5 V or 0 to 10 V		-5 10 0 7 01 -10 10 0 7	VNEG = AVSSB = 0 V	
D	DAC_B6				AGND	0 to $E V$ or 0 to $10 V$	
	DAC_B7					AGND	
	DAC_C8						
<u> </u>	DAC_C9	A)/				$V_{NEG} \ge AV_{SSC} \ge -5 V$	
C	DAC_C10	AVSSC		AGND			
	DAC_C11					AGND	
	DAC_D12						
	DAC_D13		D 0 to 5 V or 0 to 10 V	AGND	-5 10 0 v of -10 to 0 v	$v_{NEG} \le AV_{SSD} \le -5 V$	
U	DAC_D14	AVSSD				ACNID	
	DAC_D15					AGND	

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7.3.1.2 DAC Register Structure

The input data of the DACs is written to the individual DAC data registers (address 0x50 through 0x6F) in straight binary format for all output ranges (see Table 2).

	DAC OUTPUT VOLTAGE (V)				
DIGITAL CODE	0 to 5 V RANGE	0 to 10 V RANGE	-5 to 0 V RANGE	-10 to 0 V RANGE	
0000 0000 0000	0	0	-5	-10	
0000 0000 0001	0.00122	0.00244	-4.99878	-9.99756	
1000 0000 0000	2.5	5	-2.5	-5	
1111 1111 1110	4.99756	9.99512	-0.00244	-0.00488	
1111 1111 1111	4.99878	9.99756	-0.00122	-0.00244	

Table 2. DAC Data Format

Data written to the DAC data registers is initially stored in the DAC buffer registers. The transfer of data from the DAC buffer registers to the active registers is initiated by an update command in the register update register (address 0x0F). When the active registers are updated, the DAC outputs change to the new values.

The host has the option to read from either the buffer registers or the active registers when accessing the DAC data registers. The DAC read back option is configured by the READBACK bit in the interface configuration 1 register (address 0x01).

7.3.1.3 DAC Clear Operation

Each DAC can be set to a CLEAR state using either hardware or software. When a DAC goes to CLEAR state, it is loaded with a zero-code input and the output voltage is set according to the auto-range detector output range. The DAC buffer or active registers do not change when the DACs enter the CLEAR state which makes it possible to return to the same voltage output before the clear event was issued. Even though the contents of the active register do not change while a DAC is in CLEAR state, a data-register read operation from the active registers while in this state returns zero-code. This functionality enables the ability to determine the DAC output voltage regardless of the operating state (CLEAR or NORMAL).

NOTE

The DAC buffer and active registers can be updated while the DACs are in CLEAR state allowing the DACs to output new values upon return to normal operation. When the DACs exit the CLEAR state, the DACs are immediately loaded with the data in the DAC active registers and the output is set back to the corresponding level to restore operation.

The DAC clear registers (address 0xB0 through 0xB1) enable independent control of each DAC CLEAR state through software. The DACs can also be forced to enter a CLEAR state through hardware using the ALARMIN pin. See the *Programmable Out-of-Range Alarms* section for a detailed description of this method.

The ALARMIN-controlled clear mechanism is just a special case of the device capability to force the DACs into the CLEAR state as a response to an alarm event. To enable this function, the alarm events must first be enabled as DAC-clear alarm sources in the DAC clear source registers (address 0x1A through 0x1B). The DAC outputs to be cleared by the selected alarm events must also be specified in the DAC clear enable registers (address 0x18 through 0x19).

An alarm event sets the corresponding alarm bit in the alarm status registers. In addition all the DACs set to clear in response to the alarm event in the DAC clear enable registers enter a CLEAR state. Once the alarm bit is cleared, as long as no other CLEAR-state controlling alarm events have been triggered, the DACs are reloaded with the contents of the DAC active registers and the outputs update accordingly.



7.3.2 Analog-to-Digital Converter (ADC)

The AMC7836 features a monitoring system centered on a 12-bit SAR (successive approximation register) ADC fronted by a 22-channel multiplexer and an on-chip track-and-hold circuit. The monitoring systems is capable of sensing up to 16 external bipolar inputs (–12.5 to 12.5 V range), five external unipolar inputs (0 to 5 V range), and an internal analog temperature sensor.

The ADC operates from an internal 2.5 V reference (V_{ref} , measured at the REF_CMP pin) and the input range is 0 V to 2 × V_{ref} . The external bipolar inputs to the ADC are internally mapped to this range. The ADC timing signals are derived from an on-chip temperature-compensated oscillator. The conversion results can be accessed through the device serial interface.

7.3.2.1 Analog Inputs

The AMC7836 has 21 analog inputs for external voltage sensing. Sixteen of these inputs (ADC_0 through ADC_15) are bipolar and the other five (LV_ADC16 through LV_ADC20) are unipolar. Figure 51 shows the equivalent circuit for the external analog-input pins. All switches are open while the ADC is in the IDLE state.



Figure 51. ADC External Inputs Equivalent Circuit

To achieve the specified performance, especially at higher input frequencies, driving each analog input pin with a low impedance source is recommended. An external amplifier can also be used to drive the input pins.



7.3.2.1.1 Bipolar Analog Inputs

The AMC7836 can support up to 16 bipolar analog inputs. The analog input range for these channels is –12.5 to 12.5 V. The bipolar signal is scaled internally through a resistor divider so that it maps to the native input range of the ADC (0 V to 2 × V_{ref}). The input resistance of the scaling network is 175 k Ω .

The bipolar analog input conversion values are stored in straight binary format in the ADC data registers (address 0x20 through 0x49). The LSB (least-significant bit) size for these channels is $25 \times V_{ref}$ / 4096. With the internal reference equal to 2.5 V, the input voltage is calculated by Equation 1.

$$Voltage = 5\left(\frac{CODE \times 5}{4096} - 2.5\right)$$
(1)

A typical application for the bipolar channels is monitoring of the 16 DAC outputs in the device. In this application the bipolar inputs can be driven directly. However, in applications where the signal source has high impedance, buffering the analog input is recommended. When driven from a low impedance source such as the AMC7836 DAC outputs, the network is designed to settle before the start of conversion. Additional impedance can affect the settling and divider accuracy of this network.

7.3.2.1.2 Unipolar Analog Inputs

In addition to the bipolar input channels, the AMC7836 device includes five unipolar analog inputs. The analog input range for these channels is 0 V to 2 × V_{ref} and the LSB size for these channels is 2 × V_{ref} / 4096.

The unipolar analog input conversion values are stored in straight binary format in the ADC-Data registers (address 0x40 through 0x49). With the internal reference equal to 2.5 V, the input voltage is calculated by Equation 2.

$$Voltage = \frac{CODE \times 5}{4096}$$

(2)

In applications where the signal source has high impedance, externally buffering the unipolar analog input is recommended.

7.3.2.2 ADC Sequencing

The AMC7836 ADC conversion sequence is shown in Figure 52. The ADC supports direct mode and auto mode conversion. The conversion method is selected in the ADC configuration register (address 0x10). The default conversion method is direct mode.

In both methods, the single channel or sequence of channels to be converted by the ADC must be first configured in the ADC MUX configuration registers (address 0x13 through 0x15). The input channels to the ADC include 16 external bipolar inputs, five external unipolar inputs, and the internal temperature sensor.

In direct-mode conversion, the selected ADC input channels are converted on demand by issuing an ADC trigger signal. After the last enabled channel is converted, the ADC enters IDLE state and waits for a new trigger.

In auto-mode conversion, the selected ADC input channels are converted continuously. The conversion cycle is initiated by issuing an ADC trigger. Upon completion of the first conversion sequence another sequence is automatically started. Conversion of the selected channels occurs repeatedly until the auto-mode conversion is stopped by issuing a second trigger signal.





Figure 52. ADC Conversion Sequence

Regardless of the selected conversion method, the following ADC registers should only be updated while the ADC is in IDLE state:

- ADC configuration register (address 0x10)
- False alarm configuration register (address 0x11)
- ADC MUX configuration registers (address 0x13 through 0x15)
- Threshold registers (0x80 through 0x97)
- Hysteresis register (0xA0 through 0xA5)

NOTE

After updating any of the ADC registers listed above, a minimum 2 μs wait time should be implemented before issuing an ADC trigger.



7.3.2.3 ADC Synchronization

A trigger signal must occur for the ADC to enter and exit the IDLE state. The ADC trigger can be generated either through software (ICONV bit in the ADC trigger register, 0xC0) or hardware (GPIO2/ADCTRIG, pin 9). To use the GPIO2/ADCTRIG pin as an ADC trigger, the pin must be configured accordingly in the GPIO configuration register (address 0x12). When the pin is configured as a trigger, a falling edge on it begins the sampling and conversion of the ADC.

In auto mode the ADC and temperature data registers (0x20 through 0x4B) are accessed by first issuing an ADC UPDATE command in the register update register (address 0x0F). The ADC UPDATE command ensures the latest available data for each input channel can be accessed without the need for complex synchronization schemes between the AMC7836 device and the host controller. A single ADC UPDATE command updates all ADC and temperature data registers. Therefore issuing multiple UPDATE commands is not necessary when reading more than one ADC data register.

NOTE

The ADC UPDATE command and accessing of the ADC and Temperature data registers does not interfere with the conversion process which ensures continuous ADC operation.

In direct mode the ADC and temperature data registers (0x20 through 0x4B) should only be accessed while the ADC is in the IDLE state (see Figure 53). Although the total update time can be easily calculated, the device provides a data-available indicator signal to track the ADC status. Failure to satisfy the synchronization requirements could lead to erroneous data reads.

The data-available indicator signal is output through the GPIO3/DAV pin and as a data-available flag that is accessible through the serial interface (DAVF bit in the general status register, 0x72). The GPIO3/DAV pin must be configured in the GPIO configuration register (address 0x12) as an interrupt. After a direct-mode conversion is complete and the ADC returns to the IDLE state, the DAVF bit is immediately set to 1 and the DAV pin is active (low) which indicates that new data is available. The pin and flag are cleared automatically when a new conversion begins or one of the ADC data or temperature data registers is accessed.



a) Direct Mode, Software Trigger

Figure 53. ADC Direct-Mode Trigger Synchronization



7.3.2.4 Programmable Out-of-Range Alarms

The AMC7836 device is capable of continuously analyzing the five external unipolar inputs and internal temperature sensor conversion results for normal operation.

Normal operation is established through the lower and upper threshold registers (address 0x80 through 0x97). When any of the monitored inputs is out of the specified range, an alarm event is issued and the global alarm bit, GALR in the general status register (0x72), is set (see Figure 54). Use the alarm status registers (0x70 through 0x71) to determine the source of the alarm event.



Figure 54. Alarm Status Register

The ALARM-LATCH-DIS bit in the ALARMOUT source 1 register (address 0x1D) sets the latching behavior for all alarms (except for the ALARMIN alarm which is always unlatched). When the ALARM-LATCH-DIS bit is cleared to 0 the alarm bits in the alarm status registers are latched. The alarm bits are referred to as being latched because they remain set until read by software. This design ensures that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the alarm status registers, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted. When the ALARM-LATCH-DIS bit is set to 1, the alarm bits are not latched. The alarm bits in the alarm status registers are set to 0 when the error condition subsides, regardless of whether the bit is read or not.

All of the alarms can be set to activate the ALARMOUT pin. To enable this functionality, the GPIO1/ALARMOUT pin must be configured accordingly in the GPIO configuration register (address 0x12). The ALARMOUT pin works as an interrupt to the host so that it can query the alarm status registers to determine the alarm source. Any alarm event can activate the pin as long as the alarm is not masked in the ALARMOUT source registers (address 0x1C through 0x1D). When an alarm event is masked, the occurrence of the event sets the corresponding status bit in the alarm status registers, but does not activate the ALARMOUT pin.

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7.3.2.4.1 Unipolar Inputs Out-of-Range Alarms

The AMC7836 device provides out-of-range detection for the five external unipolar ADC inputs (LV_ADC16 through LV_ADC20, pins 35 through 39). Figure 55 shows the out-of-range detection block. When the measurement is out-of-range, the corresponding alarm bit in the alarm status 0 register (address 0x70) is set to 1 to flag the out-of-range condition. The values in the ADC upper and lower Threshold registers (address 0x80 through 0x93) define the upper and lower bound thresholds for all five inputs.



Figure 55. Unipolar Inputs Out-of-Range Alarms

7.3.2.4.2 Unipolar Inputs Out-of-Range Alarms

The AMC7836 includes high-limit and low-limit detection for the internal temperature sensor. Figure 56 shows the temperature detection block. The values in the LT upper and lower threshold registers (address 0x94 through 0x97) set the limits for the temperature sensor. The temperature sensor detector can issue either a high-alarm (LT-HIGH-ALR bit) or a low-alarm (LT-LOW-ALR bit) in the alarm status 1 register (address 0x71) depending on whether the high or low thresholds were exceeded. To implement single, upper-bound threshold detection for the temperature sensor, the host processor can set the upper-bound threshold to the desired value and the lower-bound threshold to the default value. For lower-bound threshold detection, the host processor can set the upper-bound threshold to the default value.

In addition to the programmable threshold alarms the temperature sensor detection circuit also includes a die thermal-alarm flag which continuously monitors the die temperature. When the die temperatures exceeds 150°C the die thermal alarm flag (THERM-ALR bit) in the alarm status 1 register (address 0x71) is set. The internal temperature sensor must be enabled for this alarm to be functional.



Figure 56. Internal Temperature Out-of-Range Alarms



7.3.2.4.3 ALARMIN Alarm

The AMC7836 device offers the option of using an external interrupt signal, such as the output of a comparator as an alarm event. The GPIO0/ALARMIN pin is used as the alarm input and must be configured accordingly in the GPIO configuration register (address 0x12). The pin is active low when configured as an alarm input.

A typical application for ALARMIN pin is to use it as a hardware interrupt that is responsible for forcing one or more DACs to a CLEAR state. The DAC is loaded with a zero-code input and the output voltage is set according to the operating output range, however the DAC buffer or active registers do not change (see the *Digital-to-Analog Converters (DACs)* section for more details). To enable this functionality the ALARMIN pin must be enabled as a DAC clear-alarm source in the DAC clear source 1 register (address 0x1B). Additionally the DAC outputs to be cleared by the ALARMIN pin must be specified in the DAC clear enable registers (address 0x18 through 0x19).

In this application when the ALARMIN pin goes low, all the DACs that are set to clear in response to the ALARMIN alarm in the DAC-clear enable registers enter a CLEAR state. When the ALARMIN pin goes back high the DACs are reloaded with the contents of the DAC active registers which allows the DAC outputs to return to the previous operating point without any additional commands.

7.3.2.4.4 Hysteresis

If a monitored signal is out of range and the alarm is enabled, the corresponding alarm bit is set to 1. However, the alarm condition is cleared only when the conversion result returns either a value lower than the high threshold register setting or higher than the low threshold register setting by the number of codes specified in the hysteresis setting (see Figure 57). The ADC and LT hysteresis registers (address 0xA0 through 0xA4) store the hysteresis value for the external unipolar inputs and internal temperature sensor programmable alarms. The hysteresis is a programmable value between 0 LSB to 127 LSB for the unipolar inputs alarms and 0°C to 31°C for the internal temperature-sensor alarms. The die thermal alarm hysteresis is fixed at 8°C.



Figure 57. Device Hysteresis

7.3.2.4.5 False-Alarm Protection

To prevent false alarms, an alarm event is only registered when the monitored signal is out of range for an *N* number of consecutive conversions. If the monitored signal returns to the normal range before N consecutive conversions, an alarm event is not issued. The false alarm factor, N, for the unipolar input and local temperature sensor out-of-range alarms can be configured in the false alarm configuration register (address 0x11).

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7.3.3 Internal Temperature Sensor

The AMC7836 device has an on-chip temperature sensor that measures the device die temperature. The normal operating temperature range for the internal temperature sensor is limited by the operating temperature range of the device (-40°C to 125°C).

The temperature sensor results are converted by the device ADC at a lower speed than the analog input channels. The temperature can be monitored either continuously or as a single-time conversion depending on whether the ADC is configured in auto mode or direct mode (see the *Analog-to-Digital Converter (ADC)* section for more details). If the temperature sensor is not needed, it can be disabled in the ADC MUX configuration 2 register (address 0x15). When disabled, the temperature sensor output is not converted by the ADC.

The temperature sensor provides 0.25°C resolution over the operating temperature range. The temperature value is stored in 12-bit two's complement format in the temperature data registers (address 0x78 through 0x79).

TEMPERATURE (°C)	DIGITAL CODE
-40	1111 0110 0000
-25	1111 1001 1100
-10	1111 1101 1000
-0.25	1111 1111 1111
0	0000 0000 0000
0.25	0000 0000 0001
10	0000 0010 1000
25	0000 0110 0100
50	0000 1100 1000
75	0001 0010 1100
100	0001 1001 0000
105	0001 1010 0100
125	0001 1111 0100

Table 3. Temperature Sensor Data Format

Use Equation 3 and Equation 4 to calculate the positive or negative temperature according to the polarity of the temperature data MSB (0 - positive, 1 - negative).

Positive Temperature (°C) =
$$\frac{ADC_Code}{4}$$

Negative Temperature (°C) = $\frac{4096 - ADC_Code}{4}$

(4)



(3)


7.3.4 Internal Reference

The AMC7836 device includes a high-performance internal reference for the on-chip ADC and 16 DACs (see Figure 58). The internal reference is a 2.5 V, bipolar transistor-based, precision bandgap reference. A compensation capacitor (4.7 μ F, typical) should be connected between the REF_CMP pin and the AGND2 pin.

The AMC7836 device includes a buffer to drive the ADC and should not be used to drive any external circuitry. The ADC reference buffer is powered down by default and should be enabled in the ADC configuration register (address 0x10) during device initialization.



Figure 58. AMC7836 Internal Reference

The internal reference is typically established after power-up in less than 5 ms at $T_A = 25^{\circ}C$ however the reference settling time is highly dependent on temperature. Figure 59 shows typical reference settling time as a function of temperature.







7.3.5 General Purpose I/Os

The AMC7836 device includes eight GPIO pins, each with an internal 48-k Ω pullup resistor to the IOV_{DD} pin. The GPIO[0:3] pins have dual functionality and can be programmed as either bidirectional digital I/O pins or interrupt signals in the GPIO configuration register (address 0x12). The GPIO[4:7] pins are dedicated GPIOs. Table 4 lists the dual function of the GPIO[0:3] pins.

PIN	DEFAULT PIN NAME ALTERNATIVE PIN NAME		ALTERNATIVE FUNCTIONALITY
7	GPIO0	ALARMIN	DAC clear control signal.
8	GPIO1	ALARMOUT	Global alarm output.
9	GPIO2	ADCTRIG	External ADC conversion trigger.
10	GPIO3	DAV	ADC data available indicator.

The GPIOs can receive an input or produce an output. When the GPIOn pin acts as an output, the status of the pin is determined by the corresponding GPIO bit in the GPIO register (address 0x7A).

To use a GPIOn pin as an input, the corresponding GPIO bit in the GPIO register must be set to 1. When a GPIOn pin acts as input, the digital value on the pin is acquired by reading the corresponding GPIO bit. After a power-on reset (POR) or any forced reset, all GPIO bits are set to 1, and the GPIOn pins have a $48 \cdot k\Omega$ input impedance to the IOV_{DD} pin (see Figure 60). The unused GPIO pins can be left floating.



Figure 60. AMC7836 GPIO Pin



7.4 Device Functional Modes

The sixteen DACs in the AMC7836 device are split into four groups, each with four DACs. The output range and clamp voltage for each DAC group is set independently which enables the device to operate in one of the following modes:

- All-positive DAC range mode
- All-negative DAC range mode
- Mixed DAC range mode

7.4.1 All-Positive DAC Range Mode

In the AMC7836 all-positive DAC range mode, each of the four DAC groups is set to a positive voltage output range (0 to 5 V or 0 to 10 V).

Because the maximum DAC output for each group cannot exceed the common AV_{CC} voltage for the device $(AV_{CC} = AV_{CC_AB} = AV_{CC_CD})$, a DAC group in the 0 to 10 V output range forces the AV_{CC} voltage to a value greater or equal to 10 V even if the remaining DAC groups are set in the 0 to 5 V range. If all DAC groups are set in the 0 to 5 V range the AV_{CC} voltage can be set to a value as low as 5 V.

The minimum DAC output for each group cannot be lower than the AV_{SS} voltage but because the minimum DAC output is 0 V in the all-positive DAC range mode, all of the AV_{SS} pins (AV_{EE}, AV_{SSB}, AV_{SSC}, and AV_{SSD}) as well as the device thermal pad can be tied to AGND thus simplifying the board design. Table 5 lists the typical configurations for this mode.

PIN	NOTES	TYPICAL CONNECTION
AV _{DD}		5 V
DV _{DD}	DV_{DD} must be equal to AV_{DD} .	5 V
IOV _{DD}	IOV_DD must be equal to or less than $DV_DD.$	1.8 V to 5 V
AV _{CC_AB} , AV _{CC_CD}	The AV _{CC_AB} and AV _{CC_CD} pins must be tied to the same potential (AV _{CC}). AV _{CC} must be greater or equal than the maximum possible output voltage for any of the sixteen DACs.	AV _{CC} ≥ 5 V AV _{CC} ≥ 10 V
AV _{EE}		AGND
AV _{SSB} , AV _{SSC} , AV _{SSD}		AGND
Thermal Pad		AGND

Table 5. All-positive DAC Range Mode Typical Configuration

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present on the corresponding AV_{SS} pin. In the all-positive DAC range mode all AV_{SS} pins are connected to AGND and consequently all four DAC groups will initialize by default to the 0 to 5 V range. The output for any of the DAC groups can be modified to the 0 to 10 V range after initialization by setting the corresponding DAC range register (address 0x1E to 0x1F) to 110b.

In addition to setting the default output range, the AV_{SS} pins also set the clamp voltage for each DAC group. Because the clamp voltage is only dependent on the voltage in the AV_{SS} pin, changes to the DAC range registers do not affect the clamp setting. With the AV_{SS} pins connected to AGND, the clamp voltage for all sixteen DACs is 0 V.



7.4.2 All-Negative DAC Range Mode

In the AMC7836 all-negative DAC range mode, each of the four DAC groups is set to a negative voltage output range (-5 to 0 V or -10 to 0 V).

Although the maximum DAC output does not exceed 0 V, the common AV_{CC} voltage ($AV_{CC} = AV_{CC_{AB}} = AV_{CC_{CD}}$) must still satisfy a minimum voltage of 4.7 V to comply with the device operating conditions. In this case a recommended approach is to tie the AV_{CC} , AV_{DD} , and DV_{DD} supply pins to a common potential.

The minimum DAC output for each group cannot be lower than the voltage on the corresponding AV_{SS} pins (AV_{EE} , AV_{SSB} , AV_{SSC} , and AV_{SSD}). The AV_{SS} pins are not required to be tied to the same potential and typically the negative voltage at each AV_{SS} pin is dictated by the desired operating DAC negative output range. One exception is the AV_{EE} pin which must be the lowest potential in the device. The thermal pad should be either tied to the same potential as the AV_{EE} pin or left disconnected. Table 6 lists the typical configurations for this mode.

PIN	NOTES	TYPICAL CONNECTION
AV _{DD}		5 V
DV _{DD}	DV_{DD} must be equal to AV_{DD} .	5 V
IOV _{DD}	IOV_DD must be equal to or less than $DV_DD.$	1.8 V to 5 V
AV _{CC_AB} , AV _{CC_CD}	The AV _{CC_AB} and AV _{CC_CD} pins must be tied to the same potential (AV _{CC}).	5 V
AV _{EE}	AV_{EE} must be the lowest potential in the device. AV_{EE} must be less than or equal to the minimum possible output voltage for DAC group A.	AV _{EE} ≤ –5 V AV _{EE} ≤ –10 V
AV _{SSB} , AV _{SSC} , AV _{SSD}	AV_{SSn} must be less than or equal to the minimum possible output voltage for DAC group n (n = B, C, D).	$AV_{EE} \le AV_{SSn} \le -5 V$ $AV_{EE} \le AV_{SSn} \le -10 V$
Thermal Pad		AV _{EE} or, Floating

Table 6. All-Negative DAC Range Mode Typical Configuration

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present in the corresponding AV_{SS} pin. In the all-negative DAC range mode all AV_{SS} pins should be connected to a voltage lower than AV_{SSTH} . If this condition is satisfied, all four DAC groups will initialize by default to the –10- to 0-V range. Because the negative clamp voltage is only dependent on the voltage in the AV_{SS} pin, the default –10- to 0-V output range presents no risk even when the AV_{SS} voltage is greater than –10 V. In this case the DAC group output should be modified to the –5 to 0 V range after initialization by setting the corresponding DAC range register (address 0x1E to 0x1F) to 101b.



7.4.3 Mixed DAC Range Mode

In the AMC7836 mixed DAC range mode, a combination of DAC groups is set to a negative voltage output range (-5 to 0 V or -10 to 0 V) and a positive voltage output range (0 to 5 V or 0 to 10 V).

Because the maximum DAC output for each group cannot exceed the common AV_{CC} voltage for the device $(AV_{CC} = AV_{CC_AB} = AV_{CC_CD})$, a DAC group in the 0 to 10 V output range forces the AV_{CC} voltage to a value greater or equal to 10 V. If all positive DAC groups are in the 0 to 5 V range the AV_{CC} voltage can be set to a value as low as 5 V.

The minimum DAC output for each group cannot be lower than the voltage on the corresponding AV_{SS} pins (AV_{EE} , AV_{SSB} , AV_{SSC} and AV_{SSD}). The AV_{SS} pins are not required to be tied to the same potential and typically the negative voltage at each AV_{SS} pin is dictated by the desired operating DAC negative output range. One exception is the AV_{EE} pin which must be the lowest potential in the device. The implication of this requirement is that if either DAC group B, C or D is set to a negative output range, DAC group A must also be set to a negative range. The thermal pad should be either tied to the same potential as the AV_{EE} pin or left disconnected. Table 7 lists the typical configurations for this mode.

PIN	NOTES	TYPICAL CONNECTION	
AV _{DD}		5 V	
DV _{DD}	DV_{DD} must be equal to AV_{DD} .	5 V	
IOV _{DD}	IOV_{DD} must be equal to or less than DV_{DD} .	1.8 V to 5 V	
AV _{CC_AB} , AV _{CC_CD}	The AV _{CC_AB} and AV _{CC_CD} pins must be tied to the same potential (AV _{CC}). AV _{CC} must be greater or equal to the maximum possible output voltage for any of the positive output range DACs.	AV _{CC} ≥ 5 V AV _{CC} ≥ 10 V	
AV _{EE}	AVEE must be the lowest potential in the device. AV_{EE} must be less than or equal to the minimum possible output voltage for DAC group A.	AVEE ≤ -5 V AVEE ≤ -10 V	
AV_{SSB} , AV_{SSC} , AV_{SSD} AV_{SSD} AV_{SSB} AV_{SSB} AV_{SSB} , AV_{SSC} , AV_{SSD} AV_{S		Negative Range	$\begin{array}{l} {\rm AV}_{\rm EE} \leq {\rm AV}_{\rm SSn} \leq -5 \ {\rm V} \\ {\rm AV}_{\rm EE} \leq {\rm AV}_{\rm SSn} \leq -10 \ {\rm V} \end{array}$
	D).	Positive Range	AGND
Thermal Pad		AV _{EE} or, Floating	

Table 7. Mixed DAC Range Mode Typical Configuration

After power-on or a reset event the output range for each DAC group is set automatically by the voltage present in the corresponding AV_{SS} pin. When the AV_{SS} voltage of a DAC group is lower than the threshold value, AV_{SSTH} , the output for that DAC group is automatically configured to the –10 to 0 V range. Conversely, if the AV_{SS} voltage of the DAC group is higher than AV_{SSTH} , the DAC-group output is automatically set to the 0 to 5 V range. The output for any of the DAC groups can be modified after initialization by setting the corresponding DAC range register (address 0x1E to 0x1F).

In addition to setting the default output range, the AV_{SS} pins also set the clamp voltage for each DAC group. Because the clamp voltage is only dependent on the voltage in the AV_{SS} pin, changes to the DAC range registers do not affect the clamp setting.

NOTE

Although not a recommended operating condition, the device allows a DAC group to operate in a positive output range even if the clamp voltage is negative (AV_{SS} connected to a negative supply voltage).



7.5 Programming

The AMC7836 device is controlled through a flexible four-wire serial interface that is compatible with SPI-type interfaces used on many microcontrollers and DSP controllers. The interface provides read and write (R/W) access to all registers of the AMC7836 device.

Each serial-interface access cycle is exactly (N + 2) bytes long, where N is the number of data bytes. Asserting the \overline{CS} pin low initiates a frame. The frame ends when the \overline{CS} pin is deasserted high. In MSB-first mode, the first bit transferred is the R/W bit. The next 15 bits are the register address (32768 addressable registers), and the remaining bits are data. For all writes, data is committed in bytes as the eight data bit of a data field that is clocked in on the rising edge of SCLK. If the write access is not an even multiple of 8 clocks, the trailing data bits are not committed. On a read access, data is clocked out on the falling edge of the serial interface clock, SCLK, on the SDO pin.

Figure 61 and Figure 62 show the access protocol used by the interface.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 SCLK	
SDI R/W A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0	
SDO	
Figure 61. Serial Interface Write Bus Cycle	
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 SCLK	
SDIR/W A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	
SDO D7 D6 D5 D4 D3 D2 D1 D0 -	

Figure 62. Serial Interface Read Bus Cycle

Streaming mode is supported for operations that require large amounts of data to be passed to or from the AMC7836. In streaming mode multiple bytes of data can be written to or read from the AMC7836 with<u>out</u> specifically providing instructions for each byte. Streaming mode is implemented by continually holding the CS pin active and continuing to shift new data in or old data out of the device.

The instruction phase includes the starting address. The AMC7836 device begins reading or writing data to this address and continues as long as the CS pin is asserted and single byte writes have not been enabled in the interface configuration 1 register (address 0x01). The AMC7836 device automatically increments or decrements the address depending on the setting of the address ascension bit in the interface configuration 0 register (address 0x00).

If the address is decrementing and address 0x0000 is reached, the next address used is 0x7FFF. If the address is incrementing and address 0x7FFF is reached, the next address used is 0x0000. Care should be taken when writing to address 0x0000 and 0x0001 as writing to these addresses may change the configuration of the serial interface. Therefore address 0x0010 should be the first (ascending) or last (descending) address accessed in streaming mode.

Figure 63 and Figure 64 show the access protocol used in streaming mode.



Programming (continued)





7.6 Register Maps

ADDRESS	TYPE	DEFAULT	REGISTER NAME
0x00	R/W	30	Interface Configuration 0
0x01	R/W	00	Interface Configuration 1
0x02	R/W	03	Device Configuration
0x03	R	08	Chip Type
0x04	R	36	Chip ID (Low Byte)
0x05	R	0C	Chip ID (High Byte)
0x06	R	00	Chip Version
0x07 – 0x0B	-	_	Reserved
0x0C	R	51	Manufacturer ID (Low Byte)
0x0D	R	04	Manufacturer ID (High Byte)
0x0E	-	_	Reserved
0x0F	R/W	00	Register Update
0x10	R/W	00	ADC Configuration
0x11	R/W	70	False Alarm Configuration
0x12	R/W	00	GPIO Configuration
0x13	R/W	00	ADC MUX Configuration 0
0x14	R/W	00	ADC MUX Configuration 1
0x15	R/W	00	ADC MUX Configuration 2
0x16	-	_	Reserved
0x17	-	_	Reserved
0x18	R/W	00	DAC Clear Enable 0
0x19	R/W	00	DAC Clear Enable 1
0x1A	R/W	00	DAC Clear Source 0
0x1B	R/W	00	DAC Clear Source 1
0x1C	R/W	00	ALARMOUT Source0
0x1D	R/W	00	ALARMOUT Source1
0x1E	R/W	00	DAC Range 0
0x1F	R/W	00	DAC Range 1
0x20	R	00	ADC0-Data (Low Byte)
0x21	R	00	ADC0-Data (High Byte)
0x22	R	00	ADC1-Data (Low Byte)
0x23	R	00	ADC1-Data (High Byte)
0x24	R	00	ADC2-Data (Low Byte)
0x25	R	00	ADC2-Data (High Byte)
0x26	R	00	ADC3-Data (Low Byte)
0x27	R	00	ADC3-Data (High Byte)
0x28	R	00	ADC4-Data (Low Byte)
0x29	R	00	ADC4-Data (High Byte)
0x2A	R	00	ADC5-Data (Low Byte)
0x2B	R	00	ADC5-Data (High Byte)
0x2C	R	00	ADC6-Data (Low Byte)
0x2D	R	00	ADC6-Data (High Byte)
0x2E	R	00	ADC7-Data (Low Byte)
0x2F	R	00	ADC7-Data (High Byte)
0x30	R	00	ADC8-Data (Low Byte)

Table 8. Register Map

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Table	8.	Register	Map	(continued))
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ADDRESS	TYPE	DEFAULT	REGISTER NAME
0x31	R	00	ADC8-Data (High Byte)
0x32	R	00	ADC9-Data (Low Byte)
0x33	R	00	ADC9-Data (High Byte)
0x34	R	00	ADC10-Data (Low Byte)
0x35	R	00	ADC10-Data (High Byte)
0x36	R	00	ADC11-Data (Low Byte)
0x37	R	00	ADC11-Data (High Byte)
0x38	R	00	ADC12-Data (Low Byte)
0x39	R	00	ADC12-Data (High Byte)
0x3A	R	00	ADC13-Data (Low Byte)
0x3B	R	00	ADC13-Data (High Byte)
0x3C	R	00	ADC14-Data (Low Byte)
0x3D	R	00	ADC14-Data (High Byte)
0x3E	R	00	ADC15-Data (Low Byte)
0x3F	R	00	ADC15-Data (High Byte)
0x40	R	00	ADC16-Data (Low Byte)
0x41	R	00	ADC16-Data (High Byte)
0x42	R	00	ADC17-Data (Low Byte)
0x43	R	00	ADC17-Data (High Byte)
0x44	R	00	ADC18-Data (Low Byte)
0x45	R	00	ADC18-Data (High Byte)
0x46	R	00	ADC19-Data (Low Byte)
0x47	R	00	ADC19-Data (High Byte)
0x48	R	00	ADC20-Data (Low Byte)
0x49	R	00	ADC20-Data (High Byte)
0x4A	R	00	Temperature Data (Low Byte)
0x4B	R	00	Temperature Data (High Byte)
0x4C - 0x4F	_	_	Reserved
0x50	R/W	00	DACA0-Data (Low Byte)
0x51	R/W	00	DACA0-Data (High Byte)
0x52	R/W	00	DACA1-Data (Low Byte)
0x53	R/W	00	DACA1-Data (High Byte)
0x54	R/W	00	DACA2-Data (Low Byte)
0x55	R/W	00	DACA2-Data (High Byte)
0x56	R/W	00	DACA3-Data (Low Byte)
0x57	R/W	00	DACA3-Data (High Byte)
0x58	R/W	00	DACB4-Data (Low Byte)
0x59	R/W	00	DACB4-Data (High Byte)
0x5A	R/W	00	DACB5-Data (Low Byte)
0x5B	R/W	00	DACB5-Data (High Byte)
0x5C	R/W	00	DACB6-Data (Low Byte)
0x5D	R/W	00	DACB6-Data (High Byte)
0x5E	R/W	00	DACB7-Data (Low Byte)
0x5F	R/W	00	DACB7-Data (High Byte)
0x60	R/W	00	DACC8-Data (Low Byte)
0x61	R/W	00	DACC8-Data (High Byte)
0x62	R/W	00	DACC9-Data (Low Byte)



Table 8. Register Map (continued)

ADDRESS	TYPE	DEFAULT	REGISTER NAME
0x63	R/W	00	DACC9-Data (High Byte)
0x64	R/W	00	DACC10-Data (Low Byte)
0x65	R/W	00	DACC10-Data (High Byte)
0x66	R/W	00	DACC11-Data (Low Byte)
0x67	R/W	00	DACC11-Data (High Byte)
0x68	R/W	00	DACD12-Data (Low Byte)
0x69	R/W	00	DACD12-Data (High Byte)
0x6A	R/W	00	DACD13-Data (Low Byte)
0x6B	R/W	00	DACD13-Data (High Byte)
0x6C	R/W	00	DACD14-Data (Low Byte)
0x6D	R/W	00	DACD14-Data (High Byte)
0x6E	R/W	00	DACD15-Data (Low Byte)
0x6F	R/W	00	DACD15-Data (High Byte)
0x70	R	00	Alarm Status 0
0x71	R	00	Alarm Status 1
0x72	R	0C	General Status
0x73 - 0x79	—	—	Reserved
0x7A	R/W	FF	GPIO
0x7B - 0x7F	_	_	Reserved
0x80	R/W	FF	ADC16-Upper-Thresh (Low Byte)
0x81	R/W	0F	ADC16-Upper-Thresh (High Byte)
0x82	R/W	00	ADC16-Lower-Thresh (Low Byte)
0x83	R/W	00	ADC16-Lower-Thresh (High Byte)
0x84	R/W	FF	ADC17-Upper-Thresh (Low Byte)
0x85	R/W	0F	ADC17-Upper-Thresh (High Byte)
0x86	R/W	00	ADC17-Lower-Thresh (Low Byte)
0x87	R/W	00	ADC17-Lower-Thresh (High Byte)
0x88	R/W	FF	ADC18-Upper-Thresh (Low Byte)
0x89	R/W	0F	ADC18-Upper-Thresh (High Byte)
0x8A	R/W	00	ADC18-Lower-Thresh (Low Byte)
0x8B	R/W	00	ADC18-Lower-Thresh (High Byte)
0x8C	R/W	FF	ADC19-Upper-Thresh (Low Byte)
0x8D	R/W	0F	ADC19-Upper-Thresh (High Byte)
0x8E	R/W	00	ADC19-Lower-Thresh (Low Byte)
0x8F	R/W	00	ADC19-Lower-Thresh (High Byte)
0x90	R/W	FF	ADC20-Upper-Thresh (Low Byte)
0x91	R/W	0F	ADC20-Upper-Thresh (High Byte)
0x92	R/W	00	ADC20-Lower-Thresh (Low Byte)
0x93	R/W	00	ADC20-Lower-Thresh (High Byte)
0x94	R/W	FF	LT-Upper-Thresh (Low Byte)
0x95	R/W	07	LT-Upper-Thresh (High Byte)
0x96	R/W	00	LT-Lower-Thresh (Low Byte)
0x97	R/W	08	LT-Lower-Thresh (High Byte)
0x98 - 0x9F		—	Reserved
0xA0	R/W	08	ADC16-Hysteresis
0xA1	R/W	08	ADC17-Hysteresis
0xA2	R/W	08	ADC18-Hysteresis



Table 8. Register Map (continued)

ADDRESS	TYPE	DEFAULT	REGISTER NAME
0xA3	R/W	08	ADC19-Hysteresis
0xA4	R/W	08	ADC20-Hysteresis
0xA5	R/W	08	LT-Hysteresis
0xA6 - 0xAF	_	—	Reserved
0xB0	R/W	00	DAC Clear 0
0xB1	R/W	00	DAC Clear 1
0xB2	R/W	00	Power-Down 0
0xB3	R/W	00	Power-Down 1
0xB4	R/W	00	Power-Down 2
0xB5 - 0xBF	_	—	Reserved
0xC0	R/W	00	ADC Trigger

7.6.1 Interface Configuration: Address 0x00 – 0x02

7.6.1.1 Interface Configuration 0 Register (address = 0x00) [reset = 0x30]

Figure 65. Interface Configuration 0 (Interface Config 0) Register (R/W)

7	6	5	4	3	2	1	0
SOFT-RESET	Reserved	ADDR- ASCEND	Reserved		Rese	rved	
R/W-0	R/W-0	R/W-1	R/W-1		R/W-AI	l zeros	

Table 9. Interface Config 0 Register Field Descriptions (R/W)

Bit	Field	Туре	Reset	Description
7	SOFT-RESET	R/W	0	Soft reset (self-clearing)
				0: no action
				1: reset - resets everything except address 0x00, 0x01
6	Reserved	R/W	0	Reserved for factory use
5	ADDR-ASCEND	R/W	1	Address Ascend
				0: Descend – decrements address while streaming (address wrap from 0x0000 to 0x7FFF)
				1: Ascend – increments address while streaming (address wrap from 0x7FFF to 0x0000)
4	Reserved	R/W	1	Reserved for factory use
3-0	Reserved	R/W	All zeros	Reserved for factory use



7.6.1.2 Interface Configuration 1 Register (address = 0x01) [reset = 0x00]

Figure 66. Interface Configuration 1 (Interface Config 1) Register (R/W)

7	6	5	4	3	2	1	0
SINGLE-INSTR	Reserved	READBACK			Reserved		
R/W-0 R/W-0 R/W-0 R/W-All zeros							
Table 10 Interface Config 1 Register Field Descriptions							

Table 10. Interface Config 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	SINGLE-INSTR	R/W	0	Single instruction enable
				0: streaming mode (default)
				1: single instruction
6	Reserved	R/W	0	Reserved for factory use
5	READBACK	R/W	0	Read back
				0: DAC read back from active registers (default)
				1: DAC read back from buffer registers
4-0	Reserved	R/W	All zeros	Reserved for factory use

7.6.1.3 Device Configuration Register (address = 0x02) [reset = 0x03]

Figure 67. Device Configuration (Device Config) Register (R/W)

7	6	5	4	3	2	1	0
	Reserved					POWER	R-MODE
		R/W-A		R/V	V-11		

Table 11. Device Config Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	Reserved	R/W	All zeros	Reserved for factory use
1-0	POWER-MODE	R/W	11	Mode: 00: Normal operation – full power and full performance 11: Power Down – lowest power, non-operational except SPI
				One time overwrite of the power-down registers (0xB2 and 0xB3)

7.6.2 Device Identification: Address 0x03 – 0x0D

7.6.2.1 Chip Type Register (address = 0x03) [reset = 0x08]

Figure 68. Chip Type Register (R)

7	6	5	4	3	2	1	0	
	Rese	erved		CHIP-TYPE				
	R-(0x0			R-0)x8		

Table 12. Chip Type Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R	0x0	Reserved for factory use
3-0	CHIP-TYPE	R	0x8	Identifies the device as a precision analog monitor and control

7.6.2.2 Chip ID Low Byte Register (address = 0x04) [reset = 0x36]

7	6	5	4	3	2	1	0	
CHIPID-LOW								
R-0x36								
	Table 12 Chin ID Low Byte Register Field Descriptions							

Figure 69. Chip ID Low Byte Register (R)

Table 13. Chip ID Low Byte Register Field Descriptions Bit Field Type Reset Description 7-0 CHIPID-LOW R 0x36 Chip ID. Low byte

7.6.2.3 Chip ID High Byte Register (address = 0x05) [reset = 0x0C]

Figure 70. Chip ID High Byte Register (R)

7	6	5	4	3	2	1	0
			CHIPIE	D-HIGH			
			R-0	x0C			

Table 14. Chip ID High Byte Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	CHIPID-HIGH	R	0x0C	Chip ID. High byte

7.6.2.4 Version ID Register (address = 0x06) [reset = 0x00]

Figure 71. Version ID Register (R)

7	6	5	4	3	2	1	0
			VERS	IONID			
R-0x00							

Table 15. Version ID Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	VERSIONID	R	0x00	AMC7836 version ID. Subject to change

7.6.2.5 Manufacturer ID Low Byte Register (address = 0x0C) [reset = 0x51]

Figure 72. Manufacturer ID Low Byte Register (R)

7	6	5	4	3	2	1	0	
VENDORID-LOW								
R-0x51								

Table 16. Manufacturer ID Low Byte Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	VENDORID-LOW	R	0x51	Manufacturer ID. Low byte



7.6.2.6 Manufacturer ID High Byte Register (address = 0x0D) [reset = 0x04]

7 6	5	4	3	2	1	0		
VENDORID-HIGH								
R-0x04								

Figure 73. Manufacturer ID High Byte Register

Table 17. Manufacturer ID High Byte Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	VENDORID-HIGH	R	0x04	Manufacturer ID. High byte

7.6.3 Register Update (Buffered Registers): Address 0x0F

7.6.3.1 Register Update Register (address = 0x0F) [reset = 0x00]

Figure 74. Register Update Register (Self Clearing) [R/W]

7	6	5	4	3	2	1	0
	Reserved		ADC-UPDATE	Reserved			UPDATE
	R/W-All Zeros		R/W-0		R/W-All Zeros		R/W-0

Table 18. Register Update Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4	ADC-UPDATE	R/W	0	When set transfers the latest ADC and temperature conversion data to the ADC and Temperature Data registers. This function is needed when operating the ADC in auto-cycle mode
3-1	Reserved	R/W	All zeros	Reserved for factory use
0	DAC-UPDATE	R/W	0	DAC update (self clearing) 0: disabled
				1: enabled – transfers data from buffers to active registers (DAC registers only)

7.6.4 General Device Configuration: Address 0x10 through 0x17

7.6.4.1 ADC Configuration Register (address = 0x10) [reset = 0x00]

Figure 75. ADC Configuration Register (R/W)

7	6	5	4	3	2	1	0		
CMODE	CONV-R	ATE[1:0]	ADC-REF- BUFF		Reserved				
R/W-0	R/W	-00	R/W-0		R/W-A	ll zeros			

Reset Description Bit Field Туре CMODE R/W 0 7 ADC Conversion Mode Bit. This bit selects the ADC conversion mode. 0: Direct mode. The analog inputs specified in the ADC channel registers are converted sequentially one time. When one set of conversions is complete, the ADC is idle and waits for a new trigger. 1: Auto mode. The analog inputs specified in the AMC channel registers are converted sequentially and repeatedly. When one set of conversions is complete, the ADC multiplexer returns to the first channel and repeats the process. The ADC-UPDATE bit in register 0x0F must be used to initiate the transfer of the latest conversion data to the ADC Data registers. R/W 00 6-5 CONV-RATE[1:0] ADC Conversion rate. See Table 20 to configure this setting. 4 ADC-REF-BUFF R/W 0 ADC Reference Buffer bit. This bit must be set to 1 after device power-up to enable the internal reference buffer driving the ADC. 0: ADC reference buffer is disabled. 1: ADC reference buffer is enabled. R/W 3-0 Reserved All zeros Reserved for factory use

Table 19. ADC Configuration Register Field Descriptions

Table 20. CONV-RATE[1:0] Bit Configuration

CONV-RATE[1:0]	Unipolar Channel Sample Time (µs)	Bipolar Channel Sample Time (µs)
00	11.5	34.5
01	23	34.5
10	34.5	34.5
11	69	69



7.6.4.2 False Alarm Configuration Register (address = 0x11) [reset = 0x70]

7	6	5	4	4	3	2	1	0	
CH-FALR-CT[2:0]			TEMP-FALR-CT[1:0]			Reserved			
	R/W-011			R/W–10)		R/W-All zeros		
	Table 21. False Alarm Configuration Register Field Descriptions								
Bit	Field	Т	уре	Reset	Description				
7-5	CH-FALR-CT[2:0]	R	R/W	011	False alarm configure thi	n protection for is bit.	ADC channels.	See Table 22 to	
4-3	TEMP-FALR-CT[1:0]	R	R/W	10	False alarm configure thi	protection for te s bit.	mperature sensor	. See Table 23 to	
2-0	Reserved	R	R/W	All zeros	Reserved fo	r factory use			

Figure 76. False Alarm Configuration Register (R/W)

Table 22. CH-FALR-CT Bit Configuration

CH-FALR-CT	N Consecutive Samples Before Alarm is Set
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 23. TEMP-FALR-CT Bit Configuration

TEMP-FALR-CT	N Consecutive Samples Before Alarm is Set
00	1
01	2
10	4
11	8

7.6.4.3 GPIO Configuration Register (address = 0x12) [reset = 0x00]

7	6	5	4	ļ	3	2	1	0
	Reserved			rved	EN-DAV	EN-ADCTRIG	EN- ALARMOUT	EN-ALARMIN
	R/W-All zeros		R/V	V-0	R/W-0	R/W-0	R/W-0	R/W-0
	Tab	le 24. GPIO	Config	uration I	Register Fie	eld Description	ns	
Bit	Field	٦	Гуре	Reset	Description	I		
7-5	Reserved	F	R/W	All zeros	Reserved fo	r factory use		
4	Reserved	F	R/W	0	Reserved fo	r factory use		
3	EN-DAV	F	R/W	0	DAV pin enable 0: GPIO3 operation (default) 1: DAV operation			
2	EN-ADCTRIG	F	R/W	0	ADCTRIG p 0: GPIC 1: ADC	ADCTRIG pin enable 0: GPIO2 operation (default) 1: ADCTRIG operation		
1	EN-ALARMOUT	F	R/W	0	ALARMOUT pin enable 0: GPIO1 operation (default) 1: ALARMOUT operation			
0	EN-ALARMIN	F	R/W	0	ALARMIN pi 0: GPIC 1: ALAI	in enable D0 operation (defa RMIN operation	ult)	

Figure 77. GPIO Configuration Register (R/W)

7.6.4.4 ADC MUX Configuration 0 Register (address = 0x13) [reset = 0x00]

Figure 78. ADC MUX Configuration 0 Register (R/W)

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
R/W-0							

Table 25. ADC MUX Configuration 0 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	CH7	R/W	0	When set to 1 the corresponding analog input channel ADC n is
6	CH6	R/W	0	accessed during an ADC conversion cycle.
5	CH5	R/W	0	When cleared to 0 the corresponding input channel ADC_n is
4	CH4	R/W	0	ignored during an ADC conversion cycle.
3	СНЗ	R/W	0	
2	CH2	R/W	0	
1	CH1	R/W	0	
0	СН0	R/W	0	



7.6.4.5 ADC MUX Configuration 1 Register (address = 0x14) [reset = 0x00]

7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
R/W-0							

Figure 79. ADC MUX Configuration 1 Register (R/W)

Table 26. ADC MUX Configuration 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	CH15	R/W	0	When set to 1 the corresponding analog input channel ADC n is
6	CH14	R/W	0	accessed during an ADC conversion cycle.
5	CH13	R/W	0	When cleared to 0 the corresponding input channel ADC_n is
4	CH12	R/W	0	ignored during an ADC conversion cycle.
3	CH11	R/W	0	
2	CH10	R/W	0	
1	СН9	R/W	0	
0	CH8	R/W	0	

7.6.4.6 ADC MUX Configuration 2 Register (address = 0x15) [reset = 0x00]

Figure 80. ADC MUX Configuration 2 Register (R/W)

7	6	5	4	3	2	1	0
Resei	ved	TEMP-CH	CH20	CH19	CH18	CH17	CH16
R/W-All	Zeros	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 27. ADC MUX Configuration 2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	Reserved	R/W	All Zeros	Reserved for factory use
5	TEMP-CH	R/W	0	When set to 1 the local temperature sensor is enabled for ADC conversion. When cleared to 0 the local temperature sensor is ignored.
4	CH20	R/W	0	When set to 1 the corresponding analog input channel ADC n is
3	CH19	R/W	0	accessed during an ADC conversion cycle.
2	CH18	R/W	0	When cleared to 0 the corresponding input channel ADC_n is
1	CH17	R/W	0	Ignored during an ADC conversion cycle.
0	CH16	R/W	0	

7.6.4.7 DAC Clear Enable 0 Register (address = 0x18) [reset = 0x00]

7	6	5	4	l i	3	2	1	0		
CLREN-E	B7 CLREN-B6	CLREN-B5	CLRE	N-B4	CLREN-A3	CLREN-A2	CLREN-A1	CLREN-A0		
R/W-0	R/W-0	R/W-0	R/V	V-0	R/W-0	R/W-0	R/W-0	R/W-0		
	Та	able 28. DAC	Register Fie	d Descriptio	ns					
Bit	Field		Туре	Reset	Description					
7	CLREN-B7		R/W	0	This register	determines which	n DACs ao into cl	ear state when a		
6	CLREN-B6		R/W	0	clear event	ear event is detected as configured in the DAC-CLEAR				
5	CLREN-B5		R/W	0	SOURCE re	SOURCE registers. If CLRENn = 1, DAC_n is forced into a clear state with a clear event.				
4	CLREN-B4		R/W	0	If CLRE					
3	CLREN-A3		R/W	0						
2	CLREN-A2		R/W	0	DAC n	$\sin n = 0$, a clear	event does not a	nect the state of		
1	CLREN-A1		R/W	0		•				
0	CLREN-A0		R/W	0						

Figure 81. DAC Clear Enable 0 Register (R/W)

7.6.4.8 DAC Clear Enable 1 Register (address = 0x19) [reset = 0x00]

Figure 82. DAC Clear Enable 1 Register (R/W)

7	6	5	4	3	2	1	0
CLREN-D15	CLREN-D14	CLREN-D13	CLREN-D12	CLREN-C11	CLREN-C10	CLREN-C9	CLREN-C8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 29. DAC Clear Enable 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	CLREN-D15	R/W	0	This register determines which DACs go into clear state when a
6	CLREN-D14	R/W	0	clear event is detected as configured in the DAC-CLEAR-
5	CLREN-D13	R/W	0	SOURCE registers.
4	CLREN-D12	R/W	0	If CLRENn = 1, DAC_n is forced into a clear state with a
3	CLREN-C11	R/W	0	the CIDENIA of a clear overthe data and effect the state of
2	CLREN-C10	R/W	0	IT CLREINN = 0, a clear event does not affect the state of DAC. n
1	CLREN-C9	R/W	0	
0	CLREN-C8	R/W	0	



7.6.5 DAC Clear and ALARMOUT Source Select: Address 0x1A through 0x1D

7.6.5.1 DAC Clear Source 0 Register (address = 0x1A) [reset = 0x00]

Figure 83. DAC Clear Source 0 Register (R/W)

7	6	5	4	3	2	1	0
	Reserved		ADC20-ALR- CLR	ADC19-ALR- CLR	ADC18-ALR- CLR	ADC17-ALR- CLR	ADC16-ALR- CLR
	R/W-All zeros		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 30. DAC Clear Source 0 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4	ADC20-ALR-CLR	R/W	0	This register selects which alarm forces DACs into a clear state.
3	ADC19-ALR-CLR	R/W	0	regardless of which DAC operation mode is active, auto or
2	ADC18-ALR-CLR	R/W	0	manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC Clear Enable registers.
1	ADC17-ALR-CLR	R/W	0	
0	ADC16-ALR-CLR	R/W	0	

7.6.5.2 DAC Clear Source 1 Register (address = 0x1B) [reset = 0x00]

Figure 84. DAC Clear Source 1 Register (R/W)

7	6	5	4	3	2	1	0
	Rese	erved		ALARMIN-ALR	THERM-ALR	LT-HIGH-ALR	LT-LOW-ALR
R/W-All zeros				R/W-0	R/W-0	R/W-0	R/W-0

Table 31. DAC Clear Source 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use
3	ALARMIN-ALR	R/W	0	This register selects which alarm forces DACs into a clear state.
2	THERM-ALR	R/W	0	regardless of which DAC operation mode is active, auto or
1	LT-HIGH-ALR	R/W	0	manual. In order for DAC_n to go into clear mode, it must be enabled in the DAC Clear Enable registers.
0	LT-LOW-ALR	R/W	0	

7.6.5.3 ALARMOUT Source 0 Register (address = 0x1c) [reset = 0x00]

Figure 85. ALARMOUT Source 0 Register (R/W)

7	6	5	4	3	2	1	0
	Reserved		ADC20-ALR- OUT	ADC19-ALR- OUT	ADC18-ALR- OUT	ADC17-ALR- OUT	ADC16-ALR- OUT
	R/W-All zeros		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 32. ALARMOUT Source 0 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4	ADC20-ALR-OUT	R/W	0	This register selects which alarms can activate the ALARMOUT
3	ADC19-ALR-OUT	R/W	0	pin. The ALARMOUT must be enabled for this function to take
2	ADC18-ALR-OUT	R/W	0	effect.
1	ADC17-ALR-OUT	R/W	0	
0	ADC16-ALR-OUT	R/W	0	

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7.6.5.4 ALARMOUT Source 1 Register (address = 0x1D) [reset = 0x00]

7	6	5	4	3	2	1	0
	Reserved		ALARM- LATCH-DIS	ALRIN-ALR- OUT	THERM-ALR- OUT	LT-HIGH-ALR- OUT	LT-LOW-ALR- OUT
	R/W-All zeros		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Figure 86. ALARMOUT Source 1 Register (R/W)

Table 33. ALARMOUT Source 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use
4	ALARM-LATCH-DIS	R/W	0	Alarm latch disable bit. When cleared to 0 the alarm bits are latched. When an alarm occurs, the corresponding alarm bit is set to "1". The alarm bit remains until the error condition subsides and the alarm register is read. Before reading, the alarm bit is not cleared even if the alarm condition disappears. When set to 1 the alarm bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the alarm bits have been read or not.
3	ALRIN-ALR-OUT	R/W	0	This register selects which alarms can activate the ALARMOUT
2	THERM-ALR-OUT	R/W	0	pin. The ALARMOUT must be enabled for this function to take
1	LT-HIGH-ALR-OUT	R/W	0	effect.
0	LT-LOW-ALR-OUT	R/W	0	

7.6.6 DAC Range: Address 0x1E

7.6.6.1 DAC Range Register (address = 0x1E) [reset = 0x00]

Figure 87. DAC Range Register (R/W)

7	6	5	4	3	2	1	0
Reserved		DAC-RANGEB[2:0)]	Reserved		DAC-RANGEA[2	:0]
R/W-0		R/W-All zeros		R/W-0		R/W-All zeros	

Table 34. DAC Range Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved for factory use
6-4	DAC-RANGEB[2:0]	R/W	All zeros	DAC group B output voltage selection. Overrides output range set by the auto-range detection circuit. See Table 35 to configure this setting.
3	Reserved	R/W	0	Reserved for factory use
2	DAC-RANGEA[2:0]	R/W	All zeros	DAC group A output voltage selection. Overrides output range set by the auto-range detection circuit. See Table 35 to configure this setting.

Table 35. DAC-RANGEx Bit Configuration

DAC-RANGEx[2:0]	DAC Group x Output Voltage Range
0xx	Range set by auto-range detection circuit
100	-10 to 0 V
101	-5 to 0 V
110	0 to 10 V
111	0 to 5 V



7.6.6.2 DAC Range 1 Register (address = 0x1F) [reset = 0x00]

7	6	5	4	3	2	1	0
Reserved		DAC-RANGED[2:0]	Reserved		DAC-RANGEC[2:(0]
R/W-0		R/W-All zeros		R/W-0		R/W-All zeros	

Figure 88. DAC Range 1 Register (R/W)

R/W-All zeros R/W-0

Table 36. DAC Range 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved for factory use
6-4	DAC-RANGED[2:0]	R/W	All zeros	DAC group D output voltage selection. Overrides output range set by the auto-range detection circuit. See Table 35 to configure this setting.
3	Reserved	R/W	0	Reserved for factory use
2	DAC-RANGEC[2:0]	R/W	All zeros	DAC group C output voltage selection. Overrides output range set by the auto-range detection circuit. See Table 35 to configure this setting.

7.6.7 ADC and Temperature Data: Address 0x20 through 0x4B

7.6.7.1 ADCn-Data (Low Byte) Register (address = 0x20 through 0x49) [reset = 0x00]

Figure 89. ADCn-Data (Low Byte) Register (R)

7	6	5	4	3	2	1	0
ADCn-DATA(7:0)							
			R-All	zeros			

Table 37. ADCn-Data (Low Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	ADCn-DATA(7:0)	R	All zeros	Stores the 12-bit ADC_n conversion results in straight binary format for both types of inputs channels (unipolar and bipolar)

7.6.7.2 ADCn-Data (High Byte) Register (address = 0x20 through 0x49) [reset = 0x00]

Figure 90. ADCn-Data (High Byte) Register (R)

7	6	5	4	3	2	1	0
	Rese	erved			ADCn-DA	ATA (11:8)	
	R-All	zeros			R-All	zeros	

Table 38. ADCn-Data (High Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R	All zeros	Reserved for factory use
3-0	ADCn-DATA (11:8)	R	All zeros	Stores the 12-bit ADC_n conversion results in straight binary format for both types of inputs channels (unipolar and bipolar).

Bit

7-0

Field

TEMP-DATA(7:0)

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7.6.7.3 Temperature Data (Low Byte) Register (address = 0x4A) [reset = 0x00]

7	6	5	4	3	2	1	0		
	TEMP-DATA(7:0)								
R-All zeros									
	Table 39. Temperature Data (Low Byte) Register Field Descriptions								

Description

Stores the temperature sensor reading in twos complement

Figure 91. Temperature Data (Low Byte) Register (R)

Reset

All zeros

		format.

7.6.7.4 Temperature Data (High Byte) Register (address = 0x4B) [reset = 0x00]

Туре

R

Figure 92. Temperature Data (High Byte) Register (R)

7	6	5	4	3	2	1	0
	Rese	erved			TEMP-D/	ATA(11:8)	
	R-All	zeros			R-All	zeros	

Table 40. Temperature Data (High Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R	All zeros	Reserved for factory use.
3-0	TEMP-DATA(11:8)	R	All zeros	Stores the temperature sensor reading in twos complement format.

7.6.8 DAC Data: Address 0x50 through 0x6F

7.6.8.1 DACn-Data (Low Byte) Register (address = 0x50 through 0x6F) [reset = 0x00]

Figure 93. DACn-Data (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0	
DACn-DATA (7:0)								
R/W-All zeros								

Table 41. DACn-Data (Low Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	DACn-DATA (7:0)	R/W	All zeros	Stores the 12-bit data to be loaded to the DAC_n latches in straight binary format. The straight binary format is used for all DAC ranges.



7.6.8.2 DACn Data (High Byte) Register (address = 0x50 through 0x6F) [reset = 0x00]

7	6	5	4	3	2	1	0
	Rese	erved			DACn-DA	TA (11:8)	
	R/W-A	II zeros			R/W-AI	zeros	

Figure 94. DACn Data (High Byte) Register (R/W)

Table 42. DACn Data (High Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use
3-0	DACn-DATA (11:8)	R/W	All zeros	Stores the 12-bit data to be loaded to the DAC_n latches in straight binary format. The straight binary format is used for all DAC ranges.

7.6.9 Status Registers: Address 0x70 through 0x72

The AMC7836 device continuously monitors all general purpose analog inputs and local temperature sensor during normal operation. When any input is out of the specified range N consecutive times, the corresponding alarm bit is set (1). If the input returns to the normal range before N consecutive times, the corresponding alarm bit remains clear (0). This configuration avoids any false alarms. When an alarm status occurs, the corresponding alarm bit is set (1). When the corresponding bit in the ALARMOUT Source Registers is cleared (0), the ALARMOUT pin is latched.

Whenever an alarm status bit is set, it remains set until the event that caused it is resolved and its status register is read. Reading the Alarm Status Registers clears the alarm status bits. The alarm bit can only be cleared by reading its Alarm Status register after the event is resolved, or by hardware reset, software reset, or power-on reset. All alarm status bits are cleared when reading the Alarm Status registers, and all these bits are reasserted if the out-of-limit condition still exists after the next conversion cycle, unless otherwise noted. ~

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7.6.9.1 Alarm Status 0 Register (address = 0x70) [reset = 0x00]

1	6 5		4	3	2	1	0	
	Reserved	ADC	20-ALR	ADC19-ALR	ADC18-ALR	ADC17-ALR	ADC16-ALR	
	R-All zeros		R-0	R-0	R-0	R-0	R-0	
	Table 43	3. Alarm St	tatus 0 Re	egister Field	Descriptions			
Bit	Field	Туре	Reset	Description				
7-5	Reserved	R	All zeros	Reserved for	r factory use			
4	ADC20-ALR	R	0	ADC20-ALR correspondir ADC20-ALR specified rar	ADC20-ALR = 1 when ADC20 is out of the range defined by the corresponding threshold registers. ADC20-ALR = 0 when the analog input is not out of the specified range.			
3	ADC19-ALR	R	0	ADC19-ALR correspondir ADC19-ALR specified rar	ADC19-ALR = 1 when ADC19 is out of the range defined by the corresponding threshold registers. ADC19-ALR = 0 when the analog input is not out of the specified range.			
2	ADC18-ALR	R	0	ADC18-ALR correspondir ADC18-ALR specified rar	ADC18-ALR = 1 when ADC18 is out of the range defined by the corresponding threshold registers. ADC18-ALR = 0 when the analog input is not out of the specified range			
1	ADC17-ALR	R	0	ADC17-ALR = 1 when ADC17 is out of the range defined by th corresponding threshold registers. ADC17-ALR = 0 when the analog input is not out of the specified range.			ge defined by the ut of the	
0	ADC16-ALR	R	0	ADC16-ALR = 1 when ADC16 is out of the range defined by the corresponding threshold registers. ADC16-ALR = 0 when the analog input is not out of the specified range.				

Figure 95. Alarm Status 0 Register (R)

7.6.9.2 Alarm Status 1 Register (address = 0x71) [reset = 0x00]

Figure 96. Alarm Status 1 Register (R)

7	6	5	4	3	2	1	0
	Rese	erved		ALARMIN-ALR	THERM-ALR	LT-HIGH-ALR	LT-LOW-ALR
	R-All	zeros		R-0	R-0	R-0	R-0

Table 44. Alarm Status 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R	All zeros	Reserved for factory use
3	ALARMIN-ALR	R	0	The ALARMIN-ALR is set to 1 if the ALARMIN pin is enabled and set high.
2	THERM-ALR	R	0	Thermal alarm flag. When the die temperature is equal to or greater than +150°C, the bit is set (1) and the THERM-ALR flag activates. The on-chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always 0. The hysteresis of this alarm is 8°C.
1	LT-HIGH-ALR	R	0	LT-HIGH-ALR = 1 when the temperature sensor is out of the range defined by the upper threshold.
0	LT-LOW-ALR	R	0	LT-LOW-ALR = 1 when the temperature sensor is out of the range defined by the lower threshold.



7.6.9.3 General Status Register (address = 0x72) [reset = 0x0C]

7	6	5	4	3	2	1	0
AVSSD	AVSSC	AVSSB	AVSSA	ADC_IDLE	Reserved	GALR	DAVF
_	_	_	_	R-1	R-1	R-0	R-0

Figure 97. General Status Register (R)

Table 45. General Status Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	AVSSD		—	This bit is the auto-range detection output for DAC group D. This bit is set to 1 when $AV_{SSD} < AV_{SSTH}$ (-10- to 0-V output range), and 0 when $A_{VSSD} > AV_{SSTH}$ (0- to 5-V output range).
6	AVSSC		-	This bit is the auto-range detection output for DAC group C. This bit is set to 1 when AV _{SSC} < AV _{SSTH} (–10- to 0-V output range), and 0 when AV _{SSC} > AV _{SSTH} (0- to 5-V output range).
5	AVSSB		_	This bit is the auto-range detection output for DAC group B. This bit is set to 1 when $AV_{SSB} < AV_{SSTH}$ (-10- to 0-V output range), and 0 when $AV_{SSB} > AV_{SSTH}$ (0- to 5-V output range).
4	AVSSA		_	This bit is the auto-range detection output for DAC group A. This bit is set to 1 when $AV_{EE} < AV_{SSTH}$ (-10- to 0-V output range), and 0 when $AV_{EE} > AV_{SSTH}$ (0- to 5-V output range).
3	ADC_IDLE	R	1	ADC Idle indicator.
				Auto mode: 1 by default; goes to 0 once the ADC is triggered and is running. Remains 0 until ADC is stopped, then ADC_IDLE returns to 1.
				Direct mode: 1 by default; goes to 0 once the ADC is triggered and direct conversions are running and returns to 1 when direct mode conversions are completed.
2	Reserved	R	1	Reserved for factory use
1	GALR	R	0	Global alarm bit. This bit is the OR function or all individual alarm bits of the status register. This bit is set to 1 when any alarm condition occurs and remains set until the status register is read. This bit is cleared after reading the Status Register.
0	DAVF	R	0	ADC Data available flag bit. Direct mode only. Always cleared in Auto mode.
				0: ADC conversion is in progress or ADC is in Auto mode
				1: ADC conversions are complete and new data is available

7.6.10 GPIO: Address 0x7A

7.6.10.1 GPIO Register (address = 0x7A) [reset = 0xFF]

Figure 98. GPIO Register (R/W)

7	6	5	4	3	2	1	0
GPIO-7	GPIO-6	GPIO-5	GPIO-4	GPIO-3	GPIO-2	GPIO-1	GPIO-0
R/W-1							

Table 46. GPIO Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	GPIO-7	R/W	1	For write operation the GPIO pin operates as an output. Writing
6	GPIO-6	R/W	1	a 1 to the GPIO-n bit sets the GPIO-N pin to high impedance.
5	GPIO-5	R/W	1	Writing a 0 sets the GPIO-n pin to logic low.
4	GPIO-4	R/W	1	the GPIO-n bit to receive the status of the GPIO-n pin.
3	GPIO-3	R/W	1	The GPIO-n pin has 48-k Ω input impedance to IOV _{DD} .
2	GPIO-2	R/W	1	
1	GPIO-1	R/W	1	
0	GPIO-0	R/W	1	

7.6.11 Out-Of-Range ADC Thresholds: Address 0x80 through 0x93

The unipolar analog inputs (LV_ADC16 to LV_ADC20) and the local temperature sensor implement an out-ofrange alarm function. The Upper-Thresh and Lower-Thresh registers define the upper bound and lower bounds for these inputs. This window determines whether the analog input or temperature is out-of-range. When the input is outside the window, the corresponding CH-ALR-n bit in the Status Register is set to 1. For normal operation, the value of the upper threshold must be greater than the value of lower threshold; otherwise, an alarm is always indicated. The analog input threshold values are specified in straight binary format while the local temperature ones are specified in two's complement format.

7.6.11.1 ADCn-Upper-Thresh (Low Byte) Register (address = 0x80 through 0x93) [reset = 0xFF]

Figure 99. ADCn-Upper-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
			THRU	n(7:0)			
	R/W-All ones						

Table 47. ADCn-Upper-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	THRUn(7:0)	R/W	All ones	Sets 12-bit upper threshold value for the ADC_n channel in straight binary format.



7-4

3-0

Reserved

THRUn(11:8)

Sets 12-bit upper threshold value for the ADC_n channel in

7.6.11.2 ADCn-Upper-Thresh (High Byte) Register (address = 0x80 through 0x93) [reset = 0x0F]

7	6	5	4	3	2	1	0	
	Re	served		THRUn(11:8)				
	R/W-	All zeros		R/W-0xF				
	Table 4	8. ADCn-Uppe	r-Thresh (Hi	gh Byte) Regis	ster Field Des	criptions		
Bit	Field	Т	vpe Reset	Description	1			

Reserved for factory use.

straight binary format.

Figure 100. ADCn-Upper-Thresh (High Byte) Register (R/W)

7.6.11.3 ADCn-Lower-Thresh (Low Byte) Register (address = 0x80 through 0x93) [reset = 0x00]

0xF

All zeros

R/W

R/W

Figure 101. ADCn-Lower-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0	
	THRLn(7:0)							
	R/W-All zeros							

Table 49. ADCn-Lower-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	THRLn(7:0)	R/W	All zeros	Sets 12-bit lower threshold value for the ADC_n channel in straight binary format.

7.6.11.4 ADCn-Lower-Thresh (High Byte) Register (address = 0x80 through 0x93) [reset = 0x00]

Figure 102. ADCn-Lower-Thresh (High Byte) Register (R/W)

7	6	5	4	3	2	1	0	
	Res	erved		THRLn(11:8)				
	R/W-A	II zeros			R/W-A	ll zeros		

Table 50. ADCn-Lower-Thresh (High Byte) Register Field Descriptions Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use.
3-0	THRLn(11:8)	R/W	All zeros	Sets 12-bit lower threshold value for ADC_n channel in straight binary format.

7.6.11.5 LT-Upper-Thresh (Low Byte) Register (address = 0x94) [reset = 0xFF]

Figure 103. LT-Upper-Thresh (Low Byte) Register (R/W)

7	6	5	4	3	2	1	0
			THRU-	LT(7:0)			
R/W-All ones							

Table 51. LT-Upper-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	THRU-LT(7:0)	R/W	All ones	Sets 12-bit upper threshold value for the local temperature sensor in two's complement format.

THRU-LT(11:8)

3-0

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Sets 12-bit upper threshold value for the local temperature

sensor in two's complement format.

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7.6.11.6 LT-Upper-Thresh (High Byte) Register (address = 0x95) [reset = 0x07]

7	6	5	4	3	2	1	0
	Rese	rved		THRU-LT(11:8)			
	R/W-AI	zeros			R/W	-0x7	
	Table 5	2. LT-Upper-1	Thresh (High	Byte) Registe	er Field Descr	iptions	
Bit	Field	T	ype Reset	Description			
7-4	Reserved	R	/W All zero	S Reserved for	factory use.		

0x7

Figure 104. LT-Upper-Thresh (High Byte) Register (R/W)

	7.6.11.7	LT-Lower-Thresh	(Low Byte) Regis	ter (address = 0x96)	[reset = 0x00]
--	----------	-----------------	------------------	----------------------	----------------

R/W

Figure 105. LT-Lower-Thresh (Low Byte) Register (R/W

7	6	5	4	3	2	1	0
			THRL-I	LT(7:0)			
R/W-All zeros							

Table 53. LT-Lower-Thresh (Low Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	THRL-LT(7:0)	R/W	All zeros	Sets 12-bit lower threshold value for the local temperature sensor in two's complement format.

7.6.11.8 LT-Lower-Thresh (High Byte) Register (address = 0x97) [reset = 0x08]

Figure 106. LT-Lower-Thresh (High Byte) Register (R/W)

7	6	5	4	3	2	1	0
	Rese	erved			THRL-L	T(11:8)	
	R/W-A	ll zeros			R/W	-0x8	

Table 54. LT-Lower-Thresh (High Byte) Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	Reserved	R/W	All zeros	Reserved for factory use.
3-0	THRL-LT(11:8)	R/W	0x8	Sets 12-bit lower threshold value for the local temperature sensor in two's complement format.



7.6.12 Alarm Hysteresis Configuration: Address 0xA0 and 0xA5

The hysteresis registers define the hysteresis in the out-of-range alarms.

7.6.12.1 ADCn-Hysteresis Register (address = 0xA0 through 0xA4) [reset = 0x08]

Figure 107. ADCn-Hysteresis Register (R/W)

7	6	5	4	3	2	1	0	
Reserved				HYSTn(6:0)				
R/W-0			R/W-0x08					

Table 55. ADCn-Hysteresis Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	Reserved	R/W	0	Reserved for factory use.
6-0	HYSTn(6:0)	R/W	0x08	Hysteresis of general purpose ADC n. 1 LSB per step

7.6.12.2 LT-Hysteresis Register (address = 0xA5) [reset = 0x08]

Figure 108. LT-Hysteresis Register (R/W)

7	6	5	4	3	2	1	0
	Reserved				HYST-LT(4:0)		
	R/W-All zeros				R/W-0x08		

Table 56. LT-Hysteresis Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	Reserved	R/W	All zeros	Reserved for factory use.
4-0	HYST-LT(4:0)	R/W	0x08	Hysteresis of local temperature sensor, 1°C per step. The range is 0°C to 31°C.

7.6.13 Clear and Power-Down Registers: Address 0xB0 through 0XB4

7.6.13.1 DAC Clear 0 Register (address = 0xB0) [reset = 0x00]

Figure 109. DAC Clear 0 Register (R/W)

7	6	5	4	3	2	1	0
CLR-B7	CLR-B6	CLR-B5	CLR-B4	CLR-A3	CLR-A2	CLR-A1	CLR-A0
R/W-0							

Table 57. DAC Clear 0 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	CLR-B7	R/W	0	This register uses software to force the DAC into a clear state.
6	CLR-B6	R/W	0	If CLRn = 1. DAC n is forced into a clear state.
5	CLR-B5	R/W	0	If CI Rn = 0, DAC, n is restored to normal operation.
4	CLR-B4	R/W	0	
3	CLR-A3	R/W	0	
2	CLR-A2	R/W	0	
1	CLR-A1	R/W	0	
0	CLR-A0	R/W	0	

7.6.13.2 DAC Clear 1 Register (address = 0xB1) [reset = 0x00]

7	6	5	4	1	3	2	1	0		
CLR-D1	5 CLR-D14	CLR-D13	CLR	-D12	CLR-C11	CLR-C10	CLR-C9	CLR-C8		
R/W-0	R/W-0	R/W-0	R/V	V-0	R/W-0	R/W-0	R/W-0	R/W-0		
Table 58. DAC Clear 1 Regist				jister Field D	Descriptions					
Bit	Field		Туре	Reset	Description					
7	CLR-D15		R/W	0	This register	uses software to	force the DAC int	o a clear state.		
6	CLR-D14		R/W	0	lf Cl Rn	If CI Rn = 1 DAC, n is forced into a clear state				
5	CLR-D13		R/W	0	If CI Rn	CI Rn = 0 DAC n is restored to normal operation		operation		
4	CLR-D12		R/W	0		- 0, 0, 10		sporadori.		
3	CLR-C11		R/W	0						
2	CLR-C10		R/W	0						
1	CLR-C9		R/W	0						
0	CLR-C8		R/W	0						

Figure 110. DAC Clear 1 Register (R/W)

7.6.13.3 Power-Down 0 Register (address = 0xB2) [reset = 0x00]

Figure 111. Power-Down 0 Register (R/W)

7	6	5	4	3	2	1	0
PDAC-B7	PDAC-B6	PDAC-B5	PDAC-B4	PDAC-A3	PDAC-A2	PDAC-A1	PDAC-A0
R/W-0							

Table 59. Power-Down 0 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	PDAC-B7	R/W	0	After power-on or reset, all bits in the power-down register are
6	PDAC-B6	R/W	0	cleared to 0, and all the components controlled by this register
5	PDAC-B5	R/W	0	the host to manage the AMC7836 power dissipation. When not
4	PDAC-B4	R/W	0	required, any of the DACs can be put into clamp mode and the
3	PDAC-A3	R/W	0	ADC and internal reference into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down
2	PDAC-A2	R/W	0	register control this power-down function. Set the respective bit
1	PDAC-A1	R/W	0	to 1 to activate the corresponding function.
0	PDAC-A0	R/W	0	



7.6.13.4 Power-Down 1 Register (address = 0xB3) [reset = 0x00]

7	6	5	4	3	2	1	0
PDAC-D15	PDAC-D14	PDAC-D13	PDAC-D12	PDAC-C11	PDAC-C10	PDAC-C9	PDAC-C8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Figure 112. Power-Down 1 Register (R/W)

Table 60. Power-Down 1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	PDAC-D15	R/W	0	After power-on or reset, all bits in the power-down register are
6	PDAC-D14	R/W	0	cleared to 0, and all the components controlled by this register
5	PDAC-D13	R/W	0	are either powered-down or off. The power-down register allows the host to manage the AMC7836 power dissipation. When not
4	PDAC-D12	R/W	0	required, any of the DACs can be put into clamp mode and the
3	PDAC-C11	R/W	0	ADC and internal reference into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down
2	PDAC-C10	R/W	0	register control this power-down function. Set the respective bit
1	PDAC-C9	R/W	0	to 1 to activate the corresponding function.
0	PDAC-C8	R/W	0	

7.6.13.5 Power-Down 2 Register (address = 0xB4) [reset = 0x00]

Figure 113. Power-Down 2 Register (R/W)

7	6	5	4	3	2	1	0
		Rese	erved			PREF	PADC
	R/W-All zeros					R/W-0	R/W-0

Table 61. Power-Down 2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	Reserved	R/W	All zeros	Reserved for factory use.
1	PREF	R/W	0	After power-on or reset, all bits in the power-down register are
0	PADC	R/W	0	cleared to 0, and all the components controlled by this register are either powered-down or off. The power-down register allows the host to manage the AMC7836 power dissipation. When not required, any of the DACs can be put into clamp mode and the ADC and internal reference into an inactive low-power mode to reduce current drain from the supply. The bits in the power-down register control this power-down function. Set the respective bit to 1 to activate the corresponding function.

7.6.14 ADC Trigger: Address 0xC0

7.6.14.1 ADC Trigger Register (address = 0xC0) [reset = 0x00]

Figure 114. ADC Trigger Register (R/W)

7	6	5	4	3	2	1	0
			Reserved				ICONV
			R/W-All zeros				R/W-0

Table 62. ADC Trigger Register Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	Reserved	R/W	All zeros	Reserved for factory use
0	ICONV	R/W	0	Internal ADC conversion bit. Set this bit to 1 to start the ADC conversion internally. The bit is automatically cleared to 0 after the ADC conversion starts.



8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The AMC7836 device is a highly integrated, low-power, analog monitoring and control solution that includes a 21-channel (12-bit) ADC, 16-channel (12-bit) DACs, eight GPIO, and a local temperature sensor. Although the device can be used in many different closed-loop systems, including industrial control and test and measurement, the device is largely used as a power amplifier controller in multi-channel RF communication applications.

Power amplifiers (PAs) include transistor technologies that are extremely temperature sensitive, and require DC biasing circuits to optimize RF performance, power efficiency, and stability. The AMC7836 device provides 16 DAC channels which can be used to adjust the power amplifier bias points in response to temperature changes. The device also includes an internal local temperature sensor, and 21 ADC channels for general-purpose monitoring.



图 115. AMC7836 Example Control and Monitor System



Application Information (接下页)

8.1.1 Temperature Sensing Applications

The AMC7836 device contains one local temperature and five unipolar analog inputs that are easily configurable to interface with remote temperature-sensor circuits. The integrated temperature sensor and analog input registers automatically update with every conversion.
^I■ 116 shows an example of a remote temperature sensor connection.

The selected temperature sensor is the LM50 device, a high precision integrated-circuit temperature sensor that operates in the -40° C to 125° C temperature range using a single positive supply. The full-scale output of the temperature sensor ranges from 100 mV to 1.75 V for the operational temperature range. In an extremely noisy environment, additional filtering is recommended. A typical value for the bypass capacitor is 0.1 μ F from the V+ pin to GND. A high-quality ceramic type NP0 or X7R is recommended because of optimal performance across temperature and very low dissipation factor.



图 116. Temperature Sensing Application With LM50


Application Information (接下页)

8.1.2 Current Sensing Applications

In applications that require current sensing of the power amplifier, an external high-side current sense amplifier can be added and configured to the unipolar ADC inputs. 🛽 117 shows this design.

The LMP8480 device is a precision current sense device that amplifies the small differential voltage developed across a current-sense resistor in the presence of high input common-mode voltages. The LMP8480 device accepts input signals with a common-mode voltage range from 4 V to 76 V with a bandwidth of 270 kHz. The LMP8480 device offers different fixed gain settings. The optimal gain setting is dependent on the accuracy requirement of the application. To maintain precision over temperature, the output of the LMP8480 device should be directly connected to the AMC7836 unipolar ADC inputs. If the output range of the LMP8480 device is scaled by a voltage divider, as shown in 🕅 117, an output amplifier may be required to drive the ADC unipolar input to ensure a low impedance source. If the series resistance, in this case R4, is low enough then the buffer may not be required because the LMP8480 device is capable of driving the input of the AMC7836 unipolar ADC channel.

注 The external resistors will cause some small error because of temperature drift and the input bias current of the operation amplifier.

In also shows a simple method to ensure proper power sequencing of the power amplifier by adding a series PMOS transistor to the PA drain terminal. The activation of the PMOS transistor connects the PAV_{DD} voltage supply to the drain pin of the power amplifier. The PMOS transistor is driven with a voltage divider that swings from the PAV_{DD} voltage to $PAV_{DD} \times (R2 / (R1 + R2))$. The NMOS shown in In 117 is connected to a microcontroller output that controls the state of the PMOS transistor.



图 117. Current-Sense Application With PMOS ON and OFF

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Texas

8.2 Typical Application

图 118 shows an example schematic incorporating the AMC7836 device.

DAC OUTPUTS connect to the gate (V_G) of the PA modules





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Typical Application (接下页)

8.2.1 Design Requirements

The AMC7836 example schematic uses the majority of the design parameters listed in 表 63.

	•
DESIGN PARAMETER	EXAMPLE VALUE
AV _{CC}	5 V
AV _{EE}	–12 V
IOV _{DD}	3.3 V
DV _{DD}	5 V
AV _{DD}	5 V
AV _{SS} banks	AV _{EE}
ADC bipolar inputs	ADC[0-15]: -12.5 to 12.5 V input range
ADC unipolar inputs	LV_ADC[16-20]: 0 to 5 V range
DAC outputs	Sixteen Monotonic 12-bit DACs Selectable ranges: 0 to 5 V, 0 to 10 V, -10 to 0 V or -5 to 0 V
Remote temperature sensing	IC temperature sensor (LM50) or thermistor

表	63.	Design	Param	eters
---	-----	--------	-------	-------

8.2.2 Detailed Design Procedure

Use the following parameters to facilitate the design process:

- AV_{CC} and AV_{EE} voltage values
- ADC input voltage range
- DAC Output voltage Ranges

8.2.2.1 ADC Input Conditioning

The AMC7836 device has an ADC with 21 analog inputs for external voltage sensing. Sixteen of these inputs are bipolar and the other five are unipolar. The bipolar inputs (ADC_0 through ADC_15) range is -12.5 to 12.5 V, and the unipolar analog inputs (LV_ADC16 through LV_ADC20) range is 0 to $2 \times V_{ref}$. The ADC operates from an internal 2.5 V reference (V_{ref}, measured at the REF_CMP pin). For additional noise filtering, a 4.7- μ F capacitor should be connected between the REF_CMP and AGND2 pins. A high-quality ceramic type NP0 or X7R is recommended because of the optimal performance of the capacitor across temperature and very-low dissipation factor.

The ADC timing signals are driven from an on-chip temperature compensated 4-MHz oscillator. The on-chip oscillator is primarily responsible for the sampling frequency of the ADC. The sampling frequency of the ADC is dynamic and dependent on the acquisition and conversion time of each channel. 表 64 lists the relationship between the total update time and the internal oscillator frequency.

		•				
ADC CONVERSION RATE ADC INPUT CHANNEL		ACQUISITION CLOCKS	CONVERSION CLOCKS	t _S (ACQUISITION + CONVERSION) NUMBER OF CLOCKS		
	Bipolar	124.5	13.5	138		
00	Unipolar	32.5	13.5	46		
	Internal Temperature Sensor	_	_	1025		
01	Bipolar	124.5	13.5	138		
	Unipolar	78.5	13.5	92		
	Internal Temperature Sensor	_	_	1025		
10	Bipolar	124.5	13.5	138		
	Unipolar	124.5	13.5	138		
	Internal Temperature Sensor	_	_	1025		
11	Bipolar	262.5	13.5	276		
	Unipolar	262.5	13.5	276		
	Internal Temperature Sensor	_	_	1025		

表 64. ADC Conversion Rate and Total Update Number of Clocks

The minimum and maximum oscillator frequency specifications in conjunction with the number of clocks required for the unipolar, bipolar and temperature sensor inputs should be applied to $\Delta \pm 5$ to calculate the total update time range.

$$T_{S} = \frac{(B_{CLK} \times \#B_{CH} + U_{CLK} \times \#U_{CH} + T_{CLK} \times \#T_{CH})}{f_{OSC}}$$

where

- T_s is the total update time
- B_{CLK} is the total bipolar clocks
- #B_{CH} is the number of active bipolar inputs
- U_{CLK} is the total unipolar clocks
- #U_{CH} is the number of active unipolar inputs
- T_{CKL} is the total internal temperature-sensor clocks
- #T_{CH} is the number of active internal temperature sensor channels; either 1 or 0
- f_{OSC} is the internal oscillator frequency

The following is an example of a complete calculation of the total update time range. In this example, the ADC conversion rate is set to 00 and the following ADC input channels are used:

- Bipolar channels: ADC_1 through ADC_5 (5 active bipolar channels)
- Unipolar channels: LV_ADC16 through LV_ADC18 (3 active unipolar channels)
- Internal temperature sensor (1 active temperature channel)

表 64 gives the total number of clocks required for each ADC input under the example conditions.

For the minimum specified oscillator frequency of 3.7 MHz, and with the ADC conversion rate set to 00, use $\Delta \vec{x}$ 6 to calculate the total maximum update time for this example.

$$T_{S} = \frac{(138 \times 5 + 46 \times 3 + 1025 \times 1)}{3.7 \text{ MHz}} = 500.811 \,\mu\text{s}$$

For the maximum specified oscillator frequency of 4.3 MHz, use 公式 7 to calculate the total minimum update time for this example.

$$T_{\rm S} = \frac{(138 \times 5 + 46 \times 3 + 1025 \times 1)}{4.3 \,\text{MHz}} = 430.93 \,\mu\text{s} \tag{7}$$

Therefore, the total update time range is 430.93 μs to 500.811 $\mu s.$

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(6) date

(5)



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During the conversion, the input current per channel varies with the total update time which is determined by the number and type of channels (NCH) and the conversion rate setting of the CONV-RATE bit in the ADC configuration register (address 0x10).

注 The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the acquisition time.

8.2.2.2 DAC Output Range Selection

The AMC7836 device includes 16 DACs split into four groups, each with four DACs. All of the DACs in a given group share the same output voltage range. The output range for each DAC group is independent and is programmable to either -10 to 0 V, -5 to 0 V, 0 to 10 V or 0 to 5 V. The DAC output ranges are configured by following the configuration settings listed in Table 1.

Each DAC includes an output buffer is capable of generating rail-to rail voltages. The *Electrical Characteristics: DAC* table lists the maximum source and sink capability of this internal amplifier. The graphs in the *Application Curves* section show the relationship of both stability and settling time with different capacitive loading structures.



8.2.3 Application Curves

9 Power Supply Recommendations

The preferred (not required) pin order for applying power is IOV_{DD} , DV_{DD} and AV_{DD} , AV_{CC} and lastly AV_{EE} , AV_{SSB} , AV_{SSC} , and AV_{SSD} . When power sequencing, ensure that all digital pins are not powered or in an active state while the IOV_{DD} pin ramps. Proper sequencing of the digital pins can be accomplished by attaching 10-k Ω pullup resistors to the IOV_{DD} pin, or pulldown resistors to the DGND pin. See the supply voltage ranges in the *Recommended Operating Conditions* table.

In applications where a negative voltage is applied to AV_{EE} , AV_{SSB} , AV_{SSC} , and AV_{SSD} first, the user may notice some small negative voltages at other supply pins, such as the AV_{DD} , DV_{DD} , and AV_{CC} pins. The negative voltages at the supply pins may exceed the values listed in the *Absolute Maximum Ratings* table, but because these voltages are created from intrinsic circuitry, the voltage levels are safe for operation.

In the case where all DAC outputs are in clamp state with AVEE = AVSSB = AVSSC = AVSSD = -12 V, the negative voltage observed on the other supply pins can be as low as -620 mV.

Although these negative voltages are observed on the pins, the user must still adhere to the guidelines specified in the *Absolute Maximum Ratings* table and verify that the inputs are driven within the range specified in the table. The user should also ensure that current is only applied when operating with voltages between the ranges listed in the *Absolute Maximum Ratings* table.

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In applications where the DAC channels are driving a large capacitive load and the output changes significantly (a full scale transition, for instance), the output current of the affected channels may drive to the short circuit current value as described in the specification table (see $\frac{1}{8}$ 64) while the capacitive load is being charged. This temporary increase in output current may inadvertently cause the AVCC or AVSS to collapse, potentially resulting in a POR event. It is recommended that the power supply solution for AVCC and AVSS be capable of supplying short circuit current for all DAC channels with capacitive loads simultaneously to ensure proper device performance.

9.1 Device Reset Options

9.1.1 Power-on-Reset (POR)

The AMC7836 device includes a power-on reset (POR) function. After all supplies have been established, a POR event is issued. The POR causes all registers to initialize to the default values, and communication with the device is valid only after a 250 µs power-on reset delay.

The default operation is power-down mode (register 0x02) in which the device is non-operational except for the communication interface as determined by the power-down registers. Before enabling normal operation, a hardware reset should be issued.

A power failure on DV_{DD} , AV_{DD} , AV_{CC} or IOV_{DD} has the potential to initiate a power-on-reset event. As long as DV_{DD} , AV_{DD} , AV_{CC} , and IOV_{DD} remain above the minimum recommended operating conditions a power failure event will not occur. When any of these supplies drops below the minimum recommended operating condition the device may or may not imitate a POR. In this case, issuing a hardware reset or proper POR is recommended to resume proper operation. To ensure a proper POR event, the DV_{DD} supply must fall below 750 mV. If the DV_{DD} supply falls below 2.7 V a hardware reset or proper POR must be issued.

9.1.2 Hardware Reset

A device hardware reset event is initiated by a minimum 20-ns logic low on the RESET pin. A hardware reset causes all registers to initialize to the default values and communication with the device is valid only after a 250µs reset delay.

9.1.2.1 Software Reset

A software reset event is initiated by setting the SOFT-RESET bit in the interface configuration 0 register (0x00). A software reset causes all registers, except 0x00 and 0x01, to initialize to the default values and communication with the device is valid only after a 100-ns delay.

10 Layout

10.1 Layout Guidelines

- All power supply pins should be bypassed to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitor has a value of 10-µF and is ceramic with a X7R or NP0 dielectric.
- To minimize interaction between the analog and digital return currents, the digital and analog sections should have separate ground planes that eventually connect at some point.
- To reduce noise on the internal reference, a 4.7-µF capacitor is recommended between the REF_CMP pin and ground.
- A high-quality ceramic type NP0 or X7R capacitor is recommended because of the optimal performance across temperature very-low dissipation factor of the capacitor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the AMC7836 device (see 图 122). The separation of analog and digital blocks allows for better design and practice as it ensures less coupling into neighboring blocks and minimizes the interaction between analog and digital return currents.



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10.2 Layout Example



图 121. AMC7836 Example Board Layout



图 122. AMC7836 Example Board Layout — Component Placement

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

如需相关文档,请参阅:

- 《LMP8480/LMP8481 具有电压输出的高精度 76V 高侧电流感测放大器》, SNVS829
- 《LM50/LM50-Q1 SOT-23 单电源摄氏温度传感器》, SNIS118

11.2 接收文档更新通知

要接收文档更新通知,请导航至 Ti.com 上的器件产品文件夹。单击右上角的通知我 进行注册,即可每周接收产品 信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点;请参阅 TI 的 《使用条款》。

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11.4 商标

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。存储或装卸时,应将导线一起截短或将装置放置于导电泡棉中,以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更,恕不另行通知和修 订此文档。如欲获取此数据表的浏览器版本,请参阅左侧的导航。



10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC7836IPAP	ACTIVE	HTQFP	PAP	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC7836	Samples
AMC7836IPAPR	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC7836	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal	*All	dimensions	are	nominal
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Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC7836IPAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

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PACKAGE MATERIALS INFORMATION

31-May-2019



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC7836IPAPR	HTQFP	PAP	64	1000	367.0	367.0	55.0

PAP 64

10 x 10, 0.5 mm pitch

GENERIC PACKAGE VIEW

HTQFP - 1.2 mm max height

QUAD FLATPACK

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.







PowerPAD[™] PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com.
- E. Falls within JEDEC MS-026

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PAP (S-PQFP-G64)

PowerPAD[™] PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD[™] package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.







NOTES:

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- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Ⅱ 均以"原样"提供技术性及可靠性数据(包括数据表)、设计资源(包括参考设计)、应用或其他设计建议、网络工具、安全信息和其他资源,不保证其中不含任何瑕疵,且不做任何明示或暗示的担保,包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

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