LMR23615 SIMPLE SWITCHER® 36V、1.5A 同步降压转换器

1 特性

- 4V 至 36V 输入范围
- 1.5A 持续输出电流
- 集成同步整流
- 具有内部补偿的电流模式控制
- 最短打开时间：60ns
- 可调开关频率
- 轻负载下的 PFM 模式
- 与外部时钟频率同步
- 75µA 静态电流
- 软启动至预偏置负载
- 支持高占空比运行模式
- 具有间断模式的输出短路保护
- 过热保护
- 12 引脚 WSON 可湿侧面封装，采用 PowerPAD™
- 使用 LMR23615 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 工厂和楼宇自动化系统：PLC CPU、HVAC 控制、电梯控制
- 用于机群管理、智能电网和安防的 GSM 和 GPRS 模块
- 通用宽输入电压稳压

3 说明

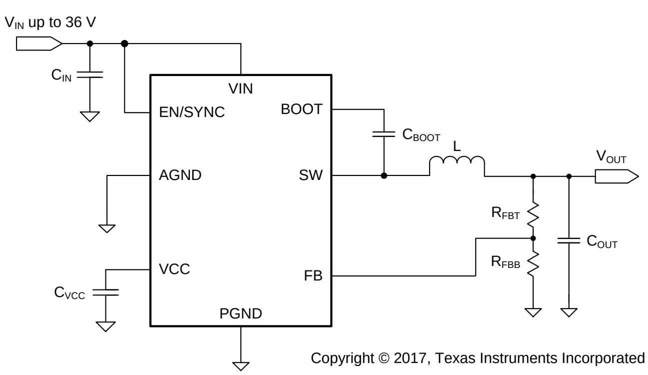
LMR23615 SIMPLE SWITCHER®是一款简便易用的 36V、1.5A 同步降压稳压器。该器件具有 4V 至 36V 的宽输入范围，适用于各种工业 应用， 可从非稳压源进行电源调节。该器件采用峰值电流模式控制来实现简单控制环路补偿和逐周期电流限制。该器件具有 75µA 的静态电流，因此适用于电池供电系统。2µA 的超低关断电流可进一步延长电池使用寿命。内部环路补偿意味着用户无需执行冗长乏味的环路补偿设计任务，并且能够最大程度地减少所需的外部组件。该器件的扩展系列产品能够以引脚到引脚兼容的封装提供 2.5A (LMR23625) 和 3A (LMR23630) 负载电流选项，从而可以实现简单且最佳的 PCB 布局。精密使能输入简化了稳压器控制和系统电源排序。保护功能 特性 包括逐周期电流限制、间断模式短路保护和过多功率耗散而引起的热关断。

器件信息(1)

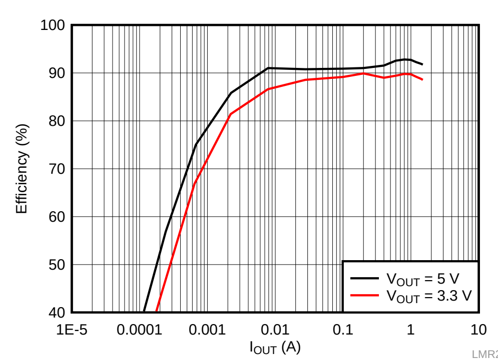
器件型号	封装	封装尺寸（标称值）
LMR23615	WSON (12)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



效率与负载间的关系，V_{IN} = 12V



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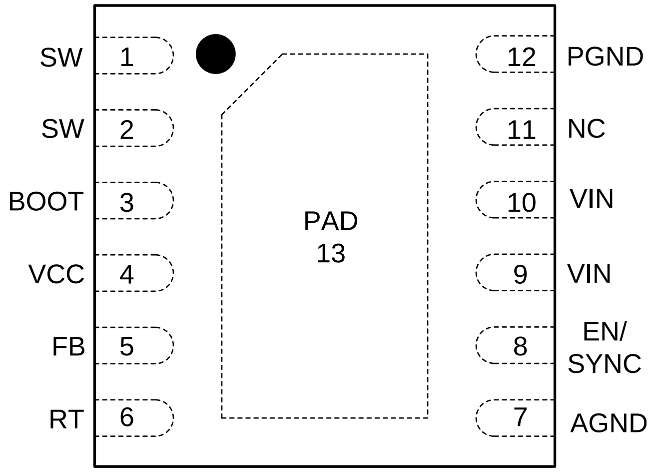
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2017) to Revision A	**Page**
• 首次发布生产数据数据表；添加了 WEBENCH 内容	1
• 已更改 将“应用”中的“可编程逻辑控制器电源”更改成了“工厂和楼宇自动化系统...” 应用	1
• 删除了“多功能打印机”和“工业电源”并修改了*应用*	1
• 已更改 将 “应用”中的“HVAC 系统” 更改成了“通用宽输入电压稳压”	1
• Changed the BOOT Capacitor value on Pin Functions to indicate value from 470nF to 100nF or higher	3
• Change the Abs Max Rating for EN/SYNC to AGND to V_{IN} + 0.3 from 42V	4
• Changed Typical Value for VIN_UVLO Rising threshold typical from 3.6-V to 3.7-V and minimum Falling threshold from 3-V to 2.9-V	5
• Change Figure 20 from V_{OUT} = 5 V, f_{SW} = 1600 kHz to V_{OUT} = 5 V, f_{SW} = 2100 kHz	14
• Changed from V_{OUT} = 7 V to 36 V to V_{IN} = 7 V to 36 V on Figure 28	22

5 Pin Configuration and Functions

DRR Package
12-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1, 2	SW	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to power inductor.
3	BOOT	P	Boot-strap capacitor connection for high-side driver. Connect a high-quality 100nF to 470nF capacitor from BOOT to SW.
4	VCC	P	Internal bias supply output for bypassing. Connect bypass capacitor from this pin to AGND. Do not connect external loading to this pin. Never short this pin to ground during operation.
5	FB	A	Feedback input to regulator, connect the feedback resistor divider tap to this pin.
6	RT	A	Connect a resistor R_T from this pin to AGND to program switching frequency. Leave floating for 400-kHz default switching frequency.
7	AGND	G	Analog ground pin. Ground reference for internal references and logic. Connect to system ground.
8	EN/SYNC	A	Enable input to regulator. High=On, Low=Off. Can be connected to VIN. Do not float. Adjust the input under voltage lockout with two resistors. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into this pin through a small coupling capacitor. See *Enable/Sync* for detail.
9, 10	VIN	P	Input supply voltage.
11	NC	N/A	Not for use. Leave this pin floating.
12	PGND	G	Power ground pin, connected internally to the low side power FET. Connect to system ground, PAD, AGND, ground pins of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
13	PAD	G	Low impedance connection to AGND. Connect to PGND on PCB. Major heat dissipation path of the die. Must be used for heat sinking to ground plane on PCB.

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input voltages	VIN to PGND	–0.3	42	V
	EN/SYNC to AGND	–5.5	V_{IN} + 0.3	
	FB to AGND	–0.3	4.5	
	RT to AGND	–0.3	4.5	
	AGND to PGND	–0.3	0.3	
Output voltages	SW to PGND	–1	V_{IN} + 0.3	V
	SW to PGND less than 10-ns transients	–5	42	
	BOOT to SW	–0.3	5.5	
	VCC to AGND	–0.3	4.5(2)	
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In shutdown mode, the VCC to AGND maximum value is 5.25 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±2500	V
		Charged-device model (CDM)(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	4	36	V
	EN/SYNC	–5	36	
	FB	–0.3	1.2	
Output voltage, V_{OUT}		1	28	V
Output current, I_{OUT}		0	1.5	A
Operating junction temperature, T_J		–40	125	°C

(1) Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)(2)		LMR23615 DRR (WSON) (12 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Determine power rating at a specific ambient temperature (T_A) with a maximum junction temperature (T_J) of 125°C (see *Recommended Operating Conditions*).

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4		36	V
VIN_UVLO	Undervoltage lockout thresholds	Rising threshold	3.3	3.7	3.9	V
		Falling threshold	2.9	3.3	3.5	
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, V_{IN} = 12 V, T_J = –40 °C to 125°C		2	4	µA
I_Q	Operating quiescent current (non- switching)	V_{IN} =12 V, V_{FB} = 1.2 V, T_J = –40 °C to 125°C, PFM mode		75		µA
ENABLE (EN/SYNC PIN)						
V_{EN_H}	Enable rising threshold voltage		1.4	1.55	1.7	V
V_{EN_HYS}	Enable hysteresis voltage			0.4		V
V_{WAKE}	Wake-up threshold		0.4			V
I_{EN}	Input leakage current at EN pin	V_{IN} = 4 V to 36 V, V_{EN}= 2 V		10	100	nA
		V_{IN} = 4 V to 36 V, V_{EN}= 36 V			1	µA
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	V_{IN} = 4 V to 36 V, T_J = 25 °C	0.985	1	1.015	V
		V_{IN} = 4 V to 36 V, T_J = –40 °C to 125°C	0.980	1	1.020	
I_{LKG_FB}	Input leakage current at FB pin	V_{FB}= 1 V		10		nA
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal LDO output voltage			4.1		V
VCC_UVLO	VCC undervoltage lockout thresholds	Rising threshold	2.8	3.2	3.6	V
		Falling threshold	2.4	2.8	3.2	
CURRENT LIMIT						
I_{HS_LIMIT}	Peak inductor current limit		2.9	3.9	4.9	A
I_{LS_LIMIT}	Valley inductor current limit		1.9	2.5	3.2	A
I_{L_ZC}	Zero cross current limit			–0.04		A
INTEGRATED MOSFETS						
$R_{DS\_ON\_HS}$	High-side MOSFET ON-resistance	V_{IN} = 12 V, I_{OUT} = 1 A		160		mΩ
$R_{DS\_ON\_LS}$	Low-side MOSFET ON-resistance	V_{IN} = 12 V, I_{OUT} = 1 A		95		mΩ

Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SHDN}	Thermal shutdown threshold		162	170	178	°C
T_{HYS}	Hysteresis			15		°C

6.6 Timing Characteristics

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
HICCUP MODE					
N_{OC} [(1)]	Number of cycles that LS current limit is tripped to enter hiccup mode		64		Cycles
T_{OC}	Hiccup retry delay time		10		ms
SOFT START					
T_{SS}	Internal soft-start time. The time of internal reference to increase from 0 V to 1 V		6		ms

(1) Specified by design.

6.7 Switching Characteristics

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW (SW PIN)						
T_{ON_MIN}	Minimum turnon time			60	90	ns
T_{OFF_MIN} [(1)]	Minimum turnoff time			100		ns
SYNC (EN/SYNC PIN)						
$f_{SW\_DEFAULT}$	Oscillator default frequency	RT pin open circuit	340	400	460	kHz
F_{ADJ}	Minimum adjustable frequency	R_T = 198 kΩ with 1% accuracy	150	200	250	kHz
	Maximum adjustable frequency	R_T = 17.8 kΩ with 1% accuracy	1750	2150	2425	kHz
f_{SYNC}	SYNC frequency range		200		2200	kHz
V_{SYNC}	Amplitude of SYNC clock AC signal (measured at SYNC pin)		2.8		5.5	V
T_{SYNC_MIN}	Minimum sync clock ON and OFF time			100		ns

(1) Ensured by design.

6.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 1600 kHz, L = 4.7 µH, C_{OUT} = 47 µF, T_A = 25 °C.

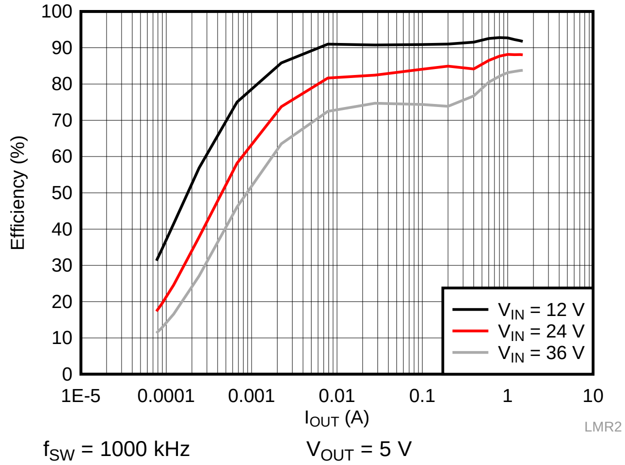


Figure 1. Efficiency vs Load Current

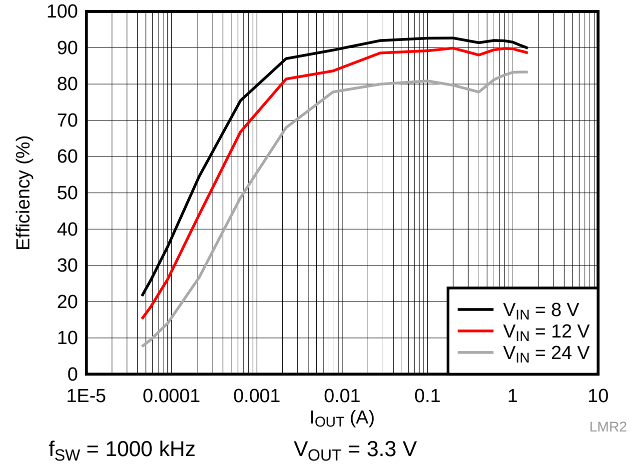


Figure 2. Efficiency vs Load Current

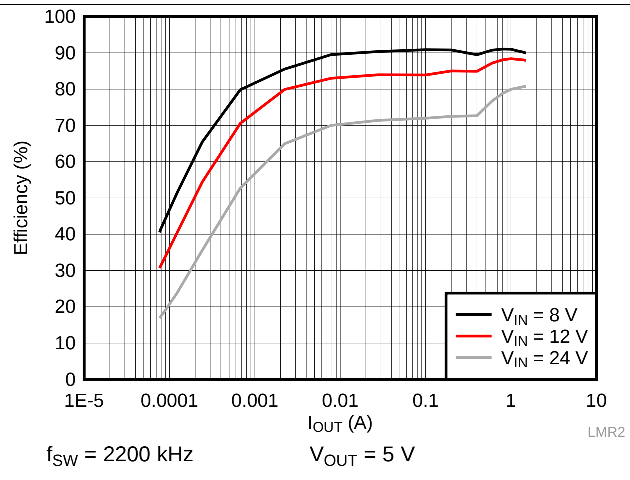


Figure 3. Efficiency vs Load Current

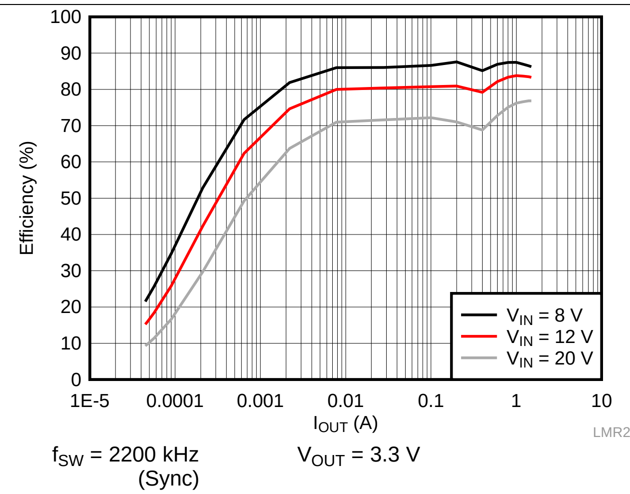


Figure 4. Efficiency vs Load Current

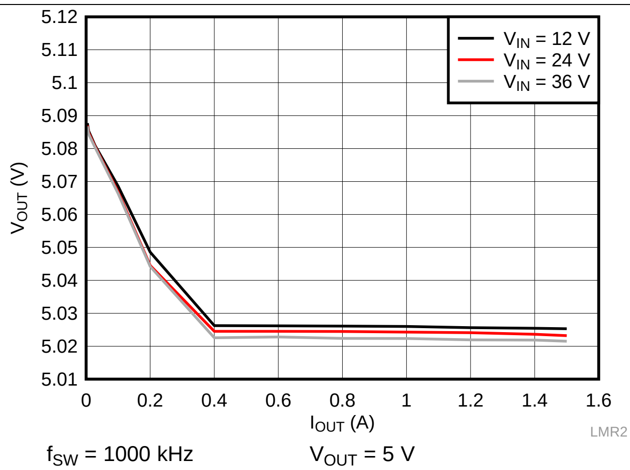


Figure 5. Load Regulation

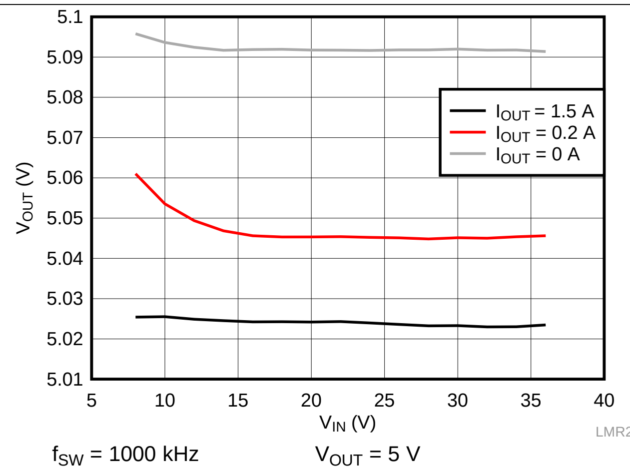
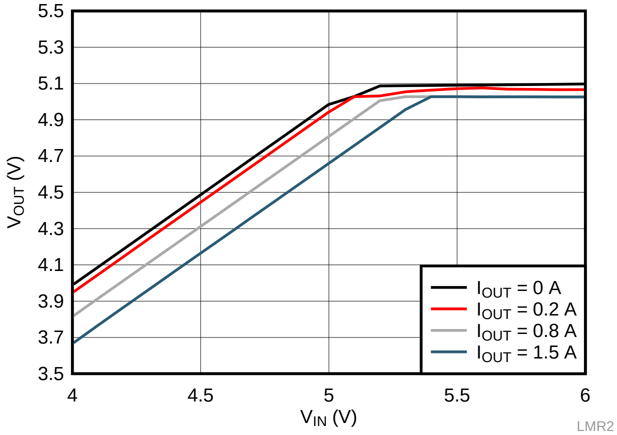


Figure 6. Line Regulation

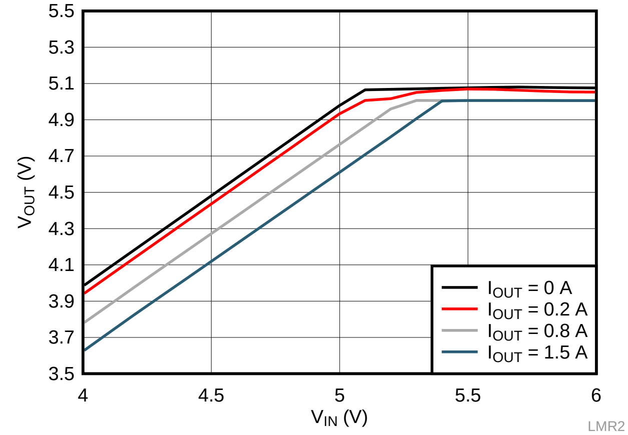
Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 1600 kHz, L = 4.7 µH, C_{OUT} = 47 µF, T_A = 25 °C.



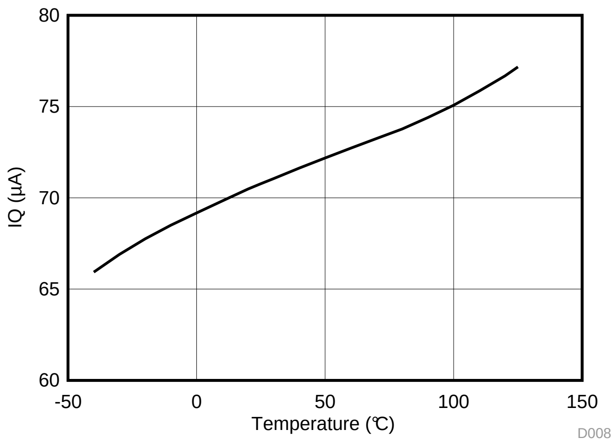
f_{SW} = 1000 kHz V_{OUT} = 5 V

Figure 7. Dropout Curve



f_{SW} = 2200 kHz V_{OUT} = 5 V

Figure 8. Dropout Curve



V_{IN} = 12 V V_{FB} = 1.1 V

Figure 9. I_Q vs Junction Temperature

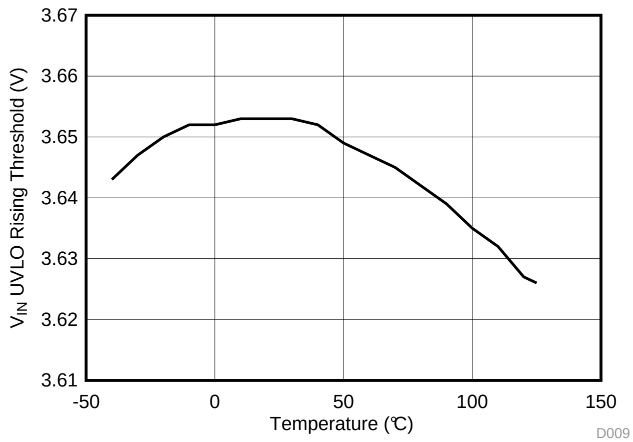


Figure 10. VIN UVLO Rising Threshold vs Junction Temperature

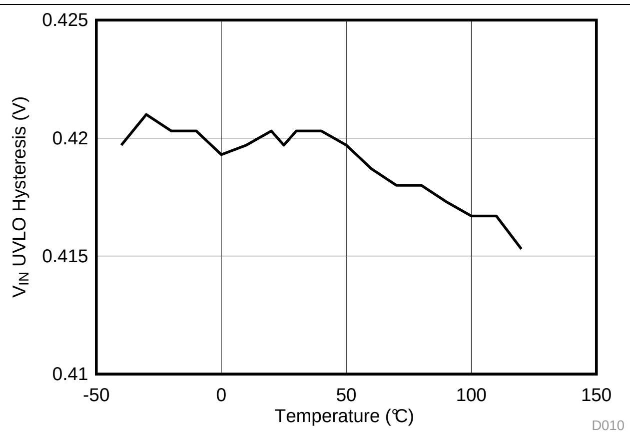
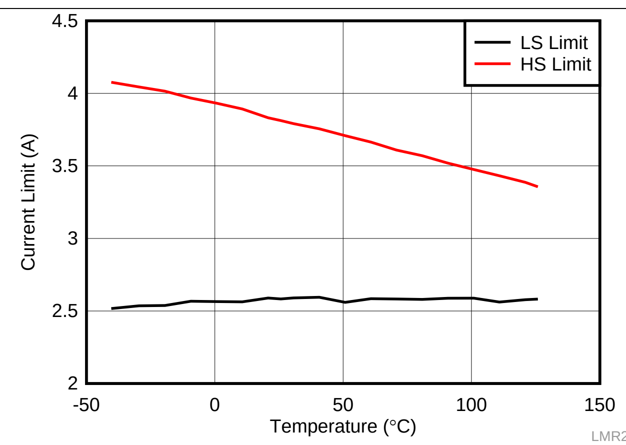


Figure 11. VIN UVLO Hysteresis vs Junction Temperature



V_{IN} = 12 V

Figure 12. HS and LS Current Limit vs Junction Temperature

7 Detailed Description

7.1 Overview

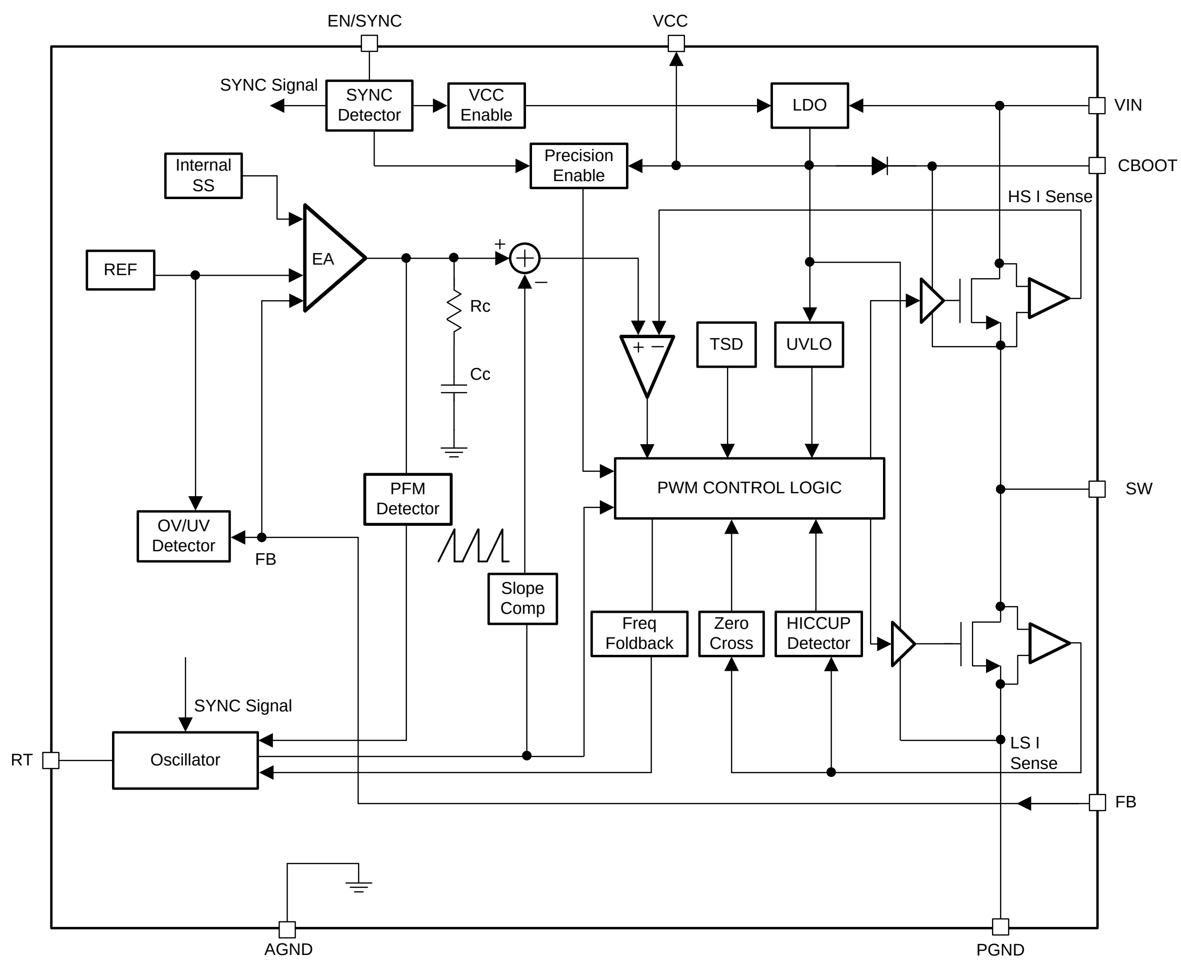
The LMR23615 SIMPLE SWITCHER® regulator is an easy-to-use synchronous step-down DC-DC converter operating from a 4-V to 36-V supply voltage. It is capable of delivering up to 1.5-A DC load current with good thermal performance in a small solution size. An extended family is available in multiple current options from 1.5 A to 3 A in pin-to-pin compatible packages.

The LMR23615 employs constant frequency peak-current-mode control. The device enters PFM mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time, and requires few external components. The switching frequency is adjustable from 200 kHz to 2.2 MHz, leaving the RT pin open for 400-kHz default switching frequency. The LMR23615 is also capable of synchronization to an external clock within the range of 200 kHz to 2.2 MHz.

Additional features such as precision enable and internal soft start provide a flexible and easy-to-use solution for a wide range of applications. Protection features include thermal shutdown, VIN and VCC undervoltage lockout, cycle-by-cycle current limit, and hiccup-mode short-circuit protection.

The LMR236xx family requires very few external components and has a pinout designed for simple, optimum PCB layout.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency, Peak-Current-Mode Control

The following operating description of the LMR23615 refers to the *Functional Block Diagram* and to the waveforms in Figure 13. The LMR23615 device is a step-down, synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR23615 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON-time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current I_L increase with linear slope $(V_{IN} – V_{OUT})$ / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of $–V_{OUT}$ / L. The control parameter of a buck converter is defined as duty cycle $D = t_{ON} / T_{SW}$, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

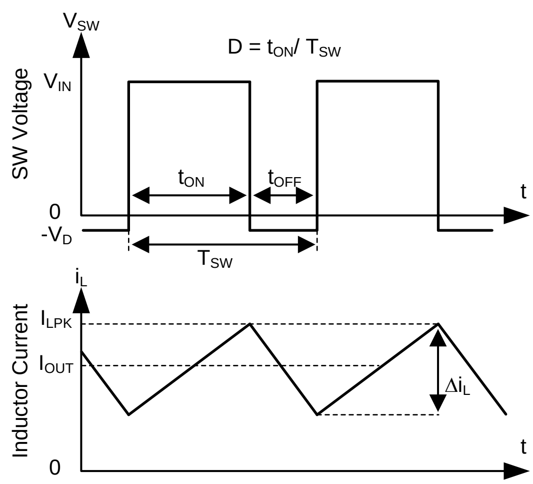


Figure 13. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR23615 employs fixed-frequency peak-current-mode control. A voltage-feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the on-time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At light load condition, the LMR23615 operates in PFM mode to maintain high efficiency.

7.3.2 Adjustable Frequency

The switching frequency can be programmed by the resistor from the RT pin to ground. The frequency is inversely proportional to the R_T resistance. The RT pin can be left floating, and the LMR23615 operates at 400-kHz default switching frequency. The RT pin is not designed to be shorted to ground. For a desired frequency, typical R_T resistance can be found by Equation 1. Table 1 gives typical R_T values for a given switching frequency (f_{SW}).

$$R_T(k\Omega) = 40200 / f_{SW}(kHz) – 0.6 \quad (1)$$

Feature Description (continued)

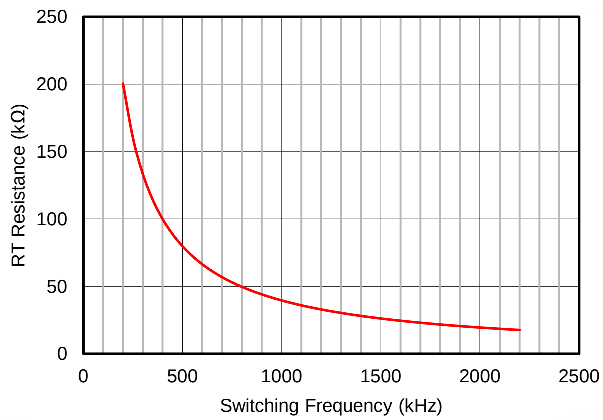


Figure 14. RT vs Frequency Curve

Table 1. Typical Frequency Setting RT Resistance

f_{SW} (kHz)	R_T (kΩ)
200	200
350	115
500	78.7
750	53.6
1000	39.2
1500	26.1
2000	19.6
2200	17.8

7.3.3 Adjustable Output Voltage

A precision 1-V reference voltage is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the low-side resistor R_{FBB} for the desired divider current and use Equation 2 to calculate high-side R_{FBT}. R_{FBT} in the range from 10 kΩ to 100 kΩ is recommended for most applications. A lower R_{FBT} value can be used if static loading is desired to reduce V_{OUT} offset in PFM operation. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and might be more desirable when light load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended because it makes the feedback path more susceptible to noise. Larger R_{FBT} value requires more carefully designed feedback path on the PCB. The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

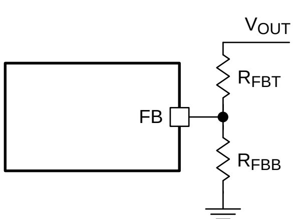


Figure 15. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (2)$$

7.3.4 Enable/Sync

The voltage on the EN pin controls the ON or OFF operation of LMR23615 device. A voltage less than 1 V (typical) shuts down the device while a voltage higher than 1.6 V (typical) is required to start the regulator. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR23615 is to connect the EN to V_{IN}. This allows self-start-up of the LMR23615 when V_{IN} is within the operation range.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} (Figure 16) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection.

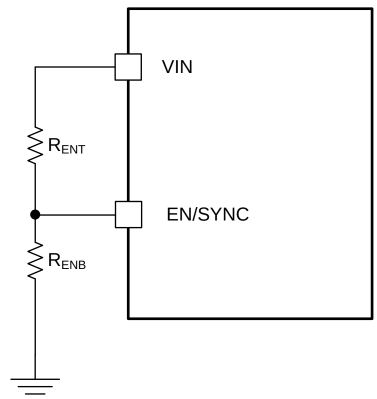


Figure 16. System UVLO by Enable Divider

The EN pin also can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the EN pin. The AC coupled peak-to-peak voltage at the EN pin must exceed the SYNC amplitude threshold of 2.8 V (typical) to trip the internal synchronization pulse detector, and the minimum SYNC clock ON and OFF time must be longer than 100 ns (typical). A 3.3-V or a higher amplitude pulse signal coupled through a 1-nF capacitor C_{SYNC} is a good starting point. Keeping R_{ENT} // R_{ENB} (R_{ENT} parallel with R_{ENB}) in the 100-kΩ range is a good choice. R_{ENT} is required for this synchronization circuit, but R_{ENB} can be left unmounted if system UVLO is not needed. Switching action of the LMR23615 device can be synchronized to an external clock from 200 kHz to 2.2 MHz. Figure 18 and Figure 19 show the device synchronized to an external system clock.

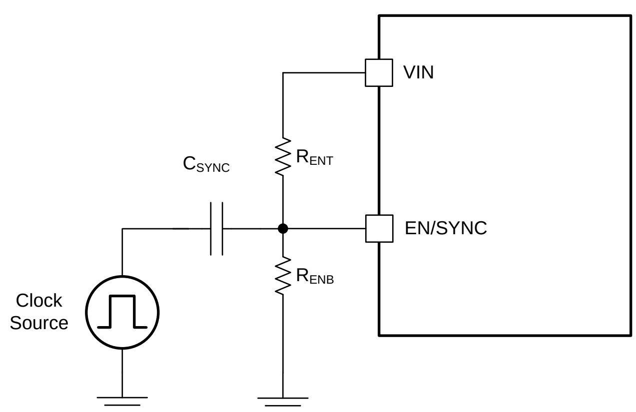


Figure 17. Synchronizing to External Clock

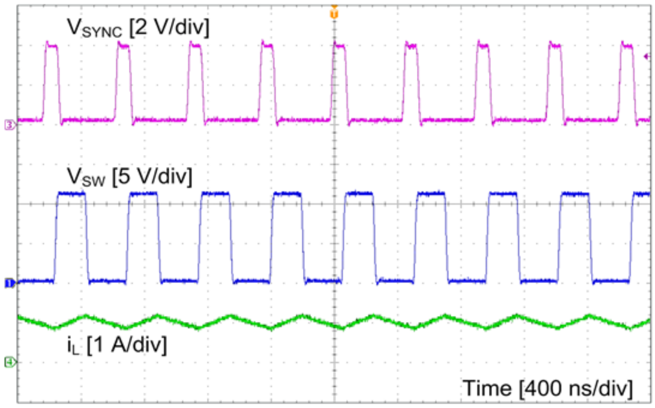


Figure 18. Synchronizing in PWM Mode

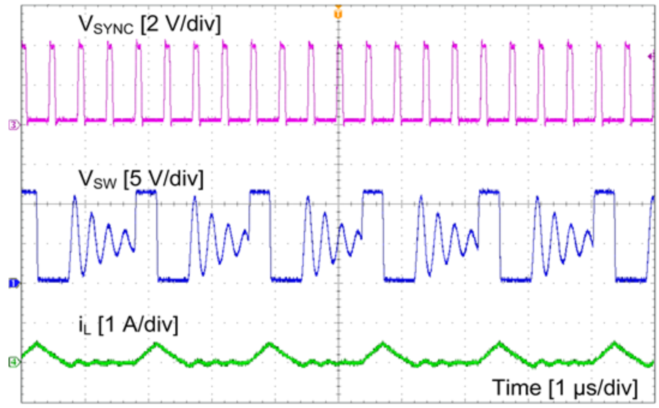


Figure 19. Synchronizing in PFM Mode

7.3.5 VCC, UVLO

The LMR23615 integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 4.1 V. The VCC pin is the output of an LDO and must be properly bypassed. Place a high-quality ceramic capacitor with a value of 2.2 µF to 10 µF, 16 V or higher rated voltage as close as possible to VCC, grounded to the exposed PAD and ground pins. The VCC output pin must not be loaded, or shorted to ground during operation. Shorting VCC to ground during operation may cause damage to the LMR23615 device.

VCC undervoltage lockout (UVLO) prevents the LMR23615 from operating until the V_{CC} voltage exceeds 3.2 V (typical). The VCC_UVLO threshold has 400 mV (typical) of hysteresis to prevent undesired shutdown due to temporary V_{IN} drops.

7.3.6 Minimum ON-Time, Minimum-OFF Time, and Frequency Foldback at Dropout Conditions

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 60 ns in the LMR23615. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 100 ns in the LMR23615. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \tag{3}$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \tag{4}$$

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency the narrower the range of the allowed duty cycle. In the LMR23615 device, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once longer duty cycle is needed under low V_{IN} conditions. Wide range of frequency foldback allows the LMR23615 output voltage stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective drop-out voltage.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size, and efficiency. The maximum operation supply voltage can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{\left(f_{SW} \times T_{ON\_MIN}\right)} \tag{5}$$

At lower supply voltage, the switching frequency decreases once T_{OFF_MIN} is tripped. The minimum V_{IN} without frequency foldback can be approximated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{\left(1 - f_{SW} \times T_{OFF\_MIN}\right)} \tag{6}$$

Taking considerations of power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in Equation 5. With frequency foldback, V_{IN_MIN} is lowered by decreased f_{SW}.

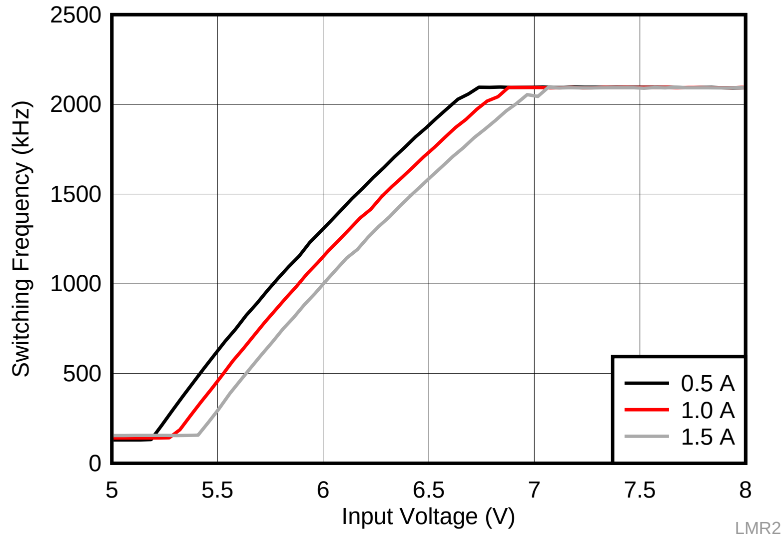


Figure 20. Frequency Foldback at Dropout (V_{OUT} = 5 V, f_{SW} = 2100 kHz)

7.3.7 Internal Compensation and C_{FF}

The LMR23615 is internally compensated as shown in *Functional Block Diagram*. The internal compensation is designed such that the loop response is stable over the entire operating frequency and output voltage range. Depending on the output voltage, the compensation loop phase margin can be low with all ceramic capacitors. An external feed-forward capacitor C_{FF} is recommended to be placed in parallel with the top resistor divider R_{FBT} for optimum transient performance.

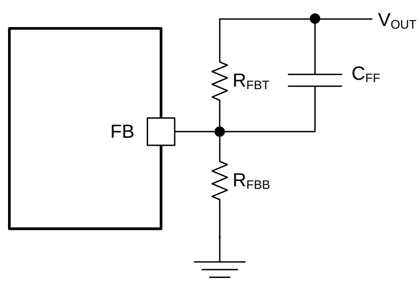


Figure 21. Feedforward Capacitor for Loop Compensation

The feed-forward capacitor C_{FF} in parallel with R_{FBT} places an additional zero before the crossover frequency of the control loop to boost phase margin. The zero frequency can be found by

$$f_{Z\_CFF} = \frac{1}{(2\pi \times C_{FF} \times R_{FBT})} \quad (7)$$

An additional pole is also introduced with C_{FF} at the frequency of

$$f_{P\_CFF} = \frac{1}{(2\pi \times C_{FF} \times R_{FBT} // R_{FBB})} \quad (8)$$

The zero f_{Z_CFF} adds phase boost at the crossover frequency and improves transient response. The pole $f_{P\text{-}CFF}$ helps maintaining proper gain margin at frequency beyond the crossover. Table 2 lists the combination of C_{OUT}, C_{FF} and R_{FBT} for typical applications, designs with similar C_{OUT} but R_{FBT} other than recommended value, adjust C_{FF} such that ($C_{FF} \times R_{FBT}$) is unchanged and adjust R_{FBB} such that (R_{FBT} / R_{FBB}) is unchanged.

Designs with different combinations of output capacitors need different C_{FF}. Different types of capacitors have different equivalent series resistance (ESR). Ceramic capacitors have the smallest ESR and need the most C_{FF}. Electrolytic capacitors have much larger ESR than ceramic, and the ESR zero frequency location would be low enough to boost the phase up around the crossover frequency. Designs that use mostly electrolytic capacitors at the output may not need any C_{FF}. The location of this ESR zero frequency can be calculated with Equation 9:

$$f_{Z\_ESR} = \frac{1}{\left(2\pi \times C_{OUT} \times ESR\right)} \tag{9}$$

The C_{FF} creates a time constant with R_{FBT} that couples in the attenuate output voltage ripple to the FB node. If the C_{FF} value is too large, it can couple too much ripple to the FB and affect V_{OUT} regulation. Therefore, calculate C_{FF} based on output capacitors used in the system. At cold temperatures, the value of C_{FF} might change based on the tolerance of the chosen component. This may reduce its impedance and ease noise coupling on the FB node. To avoid this, more capacitance can be added to the output or the value of C_{FF} can be reduced.

7.3.8 Bootstrap Voltage (BOOT)

The LMR23615 device provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate-drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 0.1 μF to 0.47 μF . TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher for stable performance over temperature and voltage.

7.3.9 Overcurrent and Short-Circuit Protection

The LMR23615 is protected from overcurrent conditions by cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode is activated if a fault condition persists to prevent overheating.

High-side MOSFET overcurrent protection is implemented by the nature of the peak-current-mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the error amplifier (EA) minus slope compensation every switching cycle. See *Functional Block Diagram* for more details. The peak current of HS switch is limited by a clamped maximum peak current threshold I_{HS_LIMIT}, which is constant. Thus the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty-cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch does not turn OFF at the end of a switching cycle if its current is above the LS current limit I_{LS_LIMIT}. The LS switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS switch turns OFF, and the HS switches on, after a dead time. This is somewhat different than the more typical peak-current limit and results in Equation 10 for the maximum load current.

$$I_{OUT\_MAX} = I_{LS\_LIMIT} + \frac{\left(V_{IN} - V_{OUT}\right)}{2 \times f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \tag{10}$$

If the current of the LS switch is higher than the LS current limit for 64 consecutive cycles, hiccup-current-protection mode is activated. In hiccup mode, the regulator is shut down and kept off for 5 ms, typically, before the LMR23615 tries to start again. If an overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents over-heating and potential damage to the device.

7.3.10 Thermal Shutdown

The LMR23615 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C (typical). The device is turned off when thermal shutdown activates. Once the die temperature falls below 155°C (typical), the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on- and off-control for the LMR23615. When V_{EN} is below 1 V (typical), the device is in shutdown mode. The LMR23615 also employs VIN and VCC UVLO protection. If V_{IN} or V_{CC} voltage is below their respective UVLO level, the regulator is turned off.

7.4.2 Active Mode

The LMR23615 is in active mode when V_{EN} is above the precision enable threshold, and V_{IN} and V_{CC} are above their respective UVLO level. The simplest way to enable the LMR23615 is to connect the EN pin to VIN pin. This allows self start-up when the input voltage is in the operating range: 4 V to 36 V. See *VCC, UVLO and Enable/Sync* for details on setting these operating levels.

In active mode, depending on the load current, the LMR23615 will be in one of three modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple.
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation.
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load.

7.4.3 CCM Mode

CCM operation is employed in the LMR23615 device when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode, and the maximum output current of 1.5 A can be supplied by the device.

7.4.4 Light Load Operation

When the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR23615 operate in DCM , also known as diode emulation mode (DEM). In DCM, the LS switch is turned off when the inductor current drops to I_{L_ZC} (–40 mA typical). Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

At even lighter current loads, PFM is activated to maintain high efficiency operation. When either the minimum HS switch ON time (t_{ON_MIN}) or the minimum peak inductor current I_{PEAK_MIN} (300 mA typical) is reached, the switching frequency decreasse to maintain regulation. In PFM, switching frequency is decreased by the control loop when load current reduces to maintain output voltage regulation. Switching loss is further reduced in PFM operation due to less frequent switching actions. The external clock synchronizing is not valid when the LMR23615 device enters into PFM mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMR23615 is a step-down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1.5 A. The following design procedure can be used to select components for the LMR23615. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes iterative design procedure and accesses comprehensive databases of components. See *Custom Design With WEBENCH® Tools* and ti.com for more details.

8.2 Typical Applications

The LMR23615 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. Figure 22 shows a basic schematic.

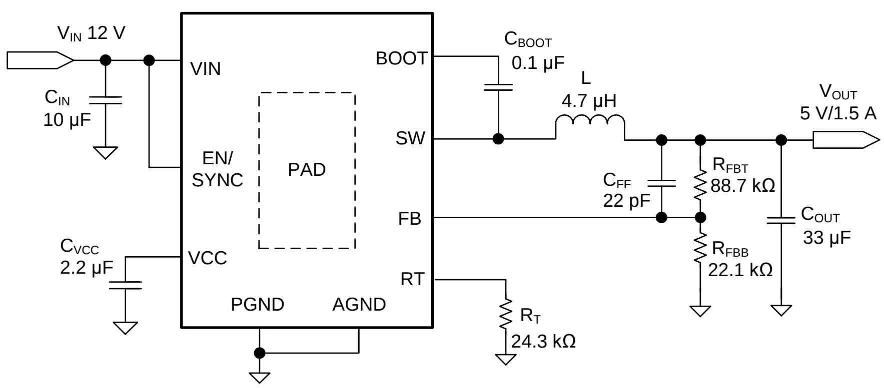


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Figure 22. Application Circuit

The external components must fulfill the needs of the application, but also the stability criteria of the device control loop. Table 2 can be used to simplify the output filter component selection.

Typical Applications (continued)

Table 2. L, C_{OUT}, and C_{FF} Typical Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH) (1)	C_{OUT} (µF) (2)	C_{FF} (pF) (3)	R_{FBT} (kΩ) (4)
200	3.3	22	200	220	51
	5	33	150	120	88.7
	12	56	68	See note (5)	243
	24	56	33	See note (5)	510
400	3.3	10	120	100	51
	5	15	90	68	88.7
	12	33	47	See note (5)	243
	24	33	22	See note (5)	510
1000	3.3	4.7	68	47	51
	5	5.6	47	22	88.7
	12	10	33	See note (5)	243
2200	3.3	2.2	33	22	51
	5	3.3	22	15	88.7

(1) Inductance value is calculated based on V_{IN} = 36 V.
(2) All the C_{OUT} values are after derating. Add more when using ceramic capacitors.
(3) For designs with R_{FBT} other than recommended value, adjust C_{FF} so that ($C_{FF} \times R_{FBT}$) is unchanged and adjust R_{FBB} such that (R_{FBT} / R_{FBB}) is unchanged.
(4) R_{FBT} = 0 Ω for V_{OUT} = 1 V. R_{FBB} = 22.1 kΩ for all other V_{OUT} settings.
(5) High ESR C_{OUT} gives enough phase boost and C_{FF} not needed.

8.2.1 Design Requirements

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Example Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, V_{IN}	12 V typical, range from 8 V to 28 V
Output voltage, V_{OUT}	5 V
Maximum output current I_{O_MAX}	1.5 A
Transient response 0.2 A to 1.5 A	5%
Output voltage ripple	50 mV
Input voltage ripple	400 mV
Switching frequency, f_{SW}	1600 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR23615 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats

- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of LMR23615 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 11 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (11)$$

For example, choosing the value of R_{FBB} as 22.1 kΩ, the desired output voltage set to 5 V, and the V_{REF} = 1 V, the R_{FBB} value is calculated using Equation 11. The formula yields to a value 88.7 kΩ.

8.2.2.3 Switching Frequency

The switching frequency can be adjusted by R_T resistance from RT pin to ground. Use Equation 1 to calculate the required value of R_T. The device can also be synchronized to an external clock for a desired frequency. See to *Enable/Sync* for more details.

For 1600 kHz frequency, the calculated R_T is 24.5 kΩ, and standard value 24.3 kΩ is selected to set the frequency approximate to 1600 kHz.

8.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the rated current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 13 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} would be 20% to 40%. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating must be higher than the current limit of the device.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times f_{SW}} \quad (12)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (13)$$

In general, it is preferable to choose lower inductance in switching power supplies, because lower inductance usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But inductance that is too low can generate an inductor current ripple that is too large such that overcurrent protection at the full load could be falsely triggered. It also generates more conduction loss and inductor core loss. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak-current-mode control, TI does not recommend having an inductor current ripple that is too small. A larger peak-current ripple improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 4.3 µH. Choose the nearest standard 4.7-µH ferrite inductor with a capability of 2-A RMS current and 4-A saturation current.

8.2.2.5 Output Capacitor Selection

Choose the output capacitor(s), C_{OUT} with care because it directly affects the steady-state output-voltage ripple, loop stability, and the voltage over/undershoot during load current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (14)$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{(8 \times f_{SW} \times C_{OUT})} = \frac{K_{IND} \times I_{OUT}}{(8 \times f_{SW} \times C_{OUT})}$$

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT}) (15)

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the regulator usually needs four or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for four clock cycles to maintain the output voltage within the specified range. Equation 16 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor, which causes an output voltage overshoot. Equation 17 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{4 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \quad (16)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L$$

where

- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot (17)

For this design example, the target output ripple is 50 mV. Presuppose $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 50 mV, and choose K_{IND} = 0.4. Equation 14 yields ESR no larger than 83.3 mΩ, and Equation 15 yields C_{OUT} no smaller than 0.9 µF. For the target over/undershoot range of this design, $V_{US} = V_{OS} = 5\% \times V_{OUT}$ = 250 mV. The C_{OUT} can be calculated to be no smaller than 14 µF and 4.1 µF by Equation 16 and Equation 17, respectively. Taking into account the derating factor of ceramic capacitor over temperature and voltage, one 33-µF, 16-V ceramic capacitor with 5-mΩ ESR is selected.

8.2.2.6 Feed-Forward Capacitor

The LMR23615 device is internally compensated. Depending on the V_{OUT} and frequency f_{SW}, if the output capacitor C_{OUT} is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feed-forward capacitor C_{FF} can be added in parallel with R_{FBT}. C_{FF} is chosen such that phase margin is boosted at the crossover frequency without C_{FF}. A simple estimation for the crossover frequency (f_X) without C_{FF} is shown in Equation 18, assuming C_{OUT} has very small ESR, and C_{OUT} value is after derating.

$$f_X = \frac{8.32}{V_{OUT} \times C_{OUT}} \quad (18)$$

Equation 19 for C_{FF} was tested:

$$C_{FF} = \frac{1}{4\pi \times f_X \times R_{FBT}} \quad (19)$$

For designs with higher ESR, C_{FF} is not needed when C_{OUT} has very high ESR, and C_{FF} calculated from Equation 19 should be reduced with medium ESR. Table 2 can be used as a quick starting point.

For the application in this design example, a 18-pF, 50-V, COG capacitor is selected.

8.2.2.7 Input Capacitor Selection

The LMR23615 device requires high-frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high-frequency decoupling capacitor is 4.7 μF to 10 μF. TI recommends a high-quality ceramic capacitor type X5R or X7R with sufficiency voltage rating. To compensate the derating of ceramic capacitors, a voltage rating twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LMR23615 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 4.7-μF, 50-V, X7R ceramic capacitors are used. A 0.1-μF for high-frequency filtering and place it as close as possible to the device pins.

8.2.2.8 Bootstrap Capacitor Selection

Every LMR23615 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 μF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

8.2.2.9 VCC Capacitor Selection

The VCC pin is the output of an internal LDO for the LMR23615 device. To insure stability of the device, place a minimum of 2.2-μF, 16-V, X7R capacitor from this pin to ground.

8.2.2.10 Undervoltage Lockout Setpoint

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. Equation 20 can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{20}$$

The EN rising threshold (V_{ENH}) for LMR23615 is set to be 1.55 V (typical). Choose the value of R_{ENB} to be 287 kΩ to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6 V, then the value of R_{ENT} can be calculated using Equation 21:

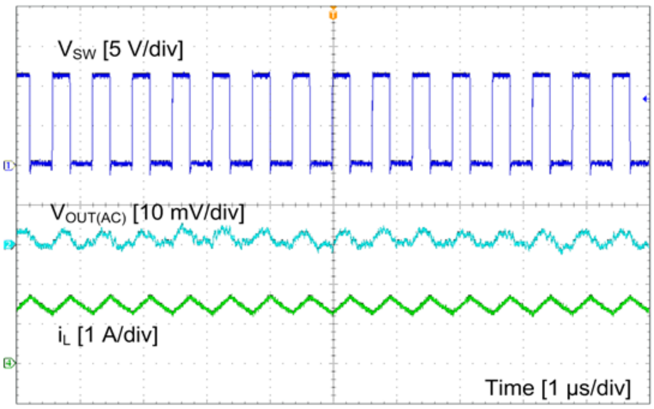
$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{21}$$

Equation 21 yields a value of 820 kΩ. The resulting falling UVLO threshold, equals 4.4 V, can be calculated by Equation 22, where EN hysteresis (V_{EN_HYS}) is 0.4 V (typica).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{22}$$

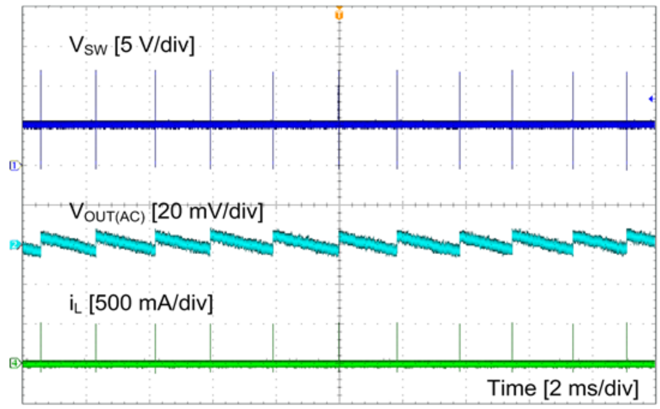
8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 1600 kHz, L = 4.7 µH, C_{OUT} = 47 µF, T_A = 25 °C.



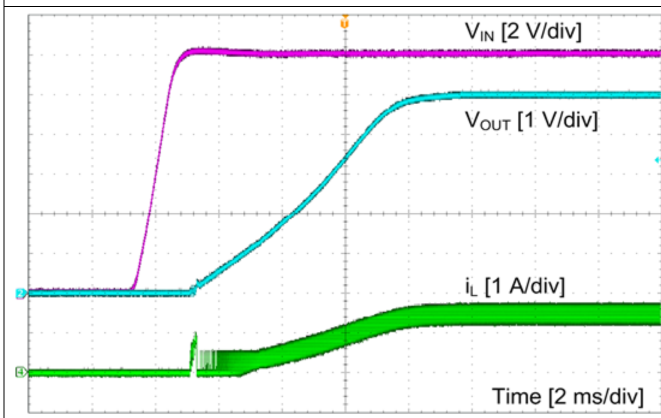
V_{OUT} = 5 V I_{OUT} = 1.5 A f_{SW} = 1600 kHz

Figure 23. CCM Mode



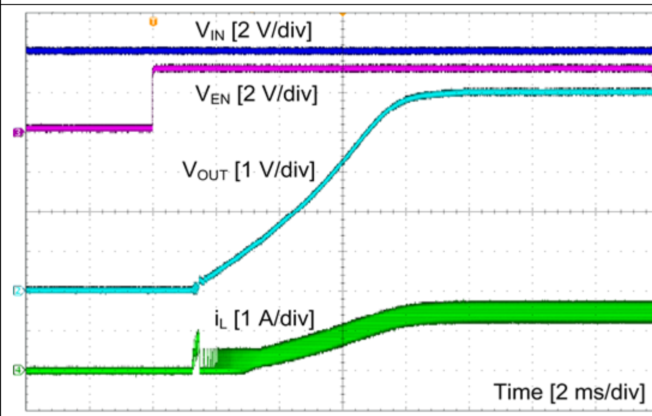
V_{OUT} = 5 V I_{OUT} = 0 mA f_{SW} = 1600 kHz

Figure 24. PFM Mode



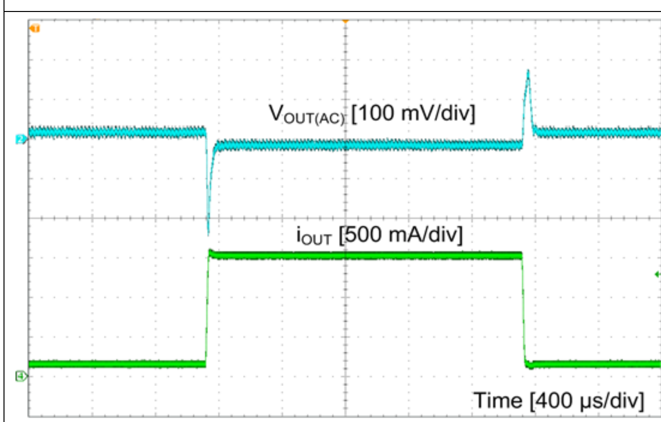
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 1.5 A

Figure 25. Start-Up by V_{IN}



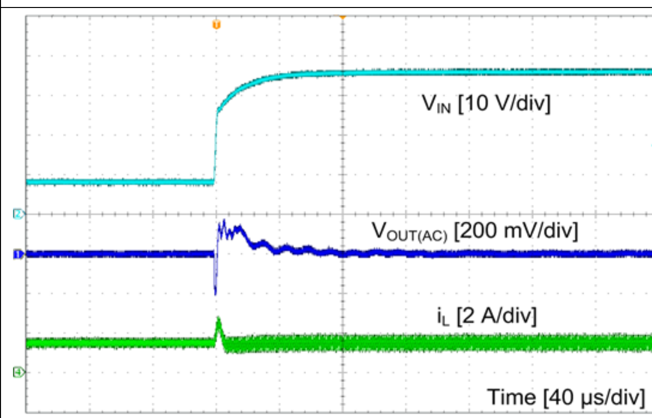
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 1.5 A

Figure 26. Start-Up by EN



V_{IN} = 12 V V_{OUT} = 5 V
I_{OUT} = 0.2 A to 1.5 A, 100 mA / µs

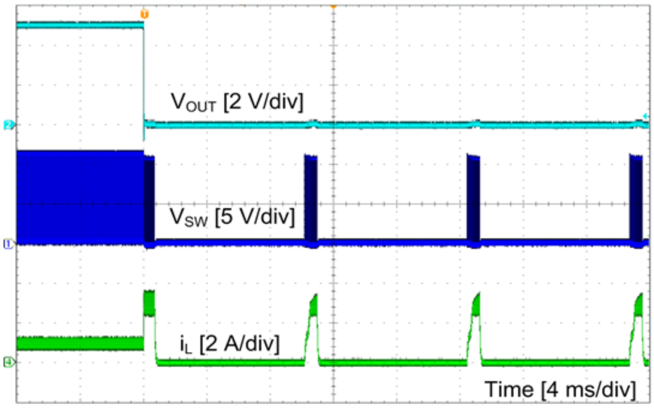
Figure 27. Load Transient



V_{IN} = 7 V to 36 V, 2 V / µs I_{OUT} = 1.5 A
V_{OUT} = 5 V

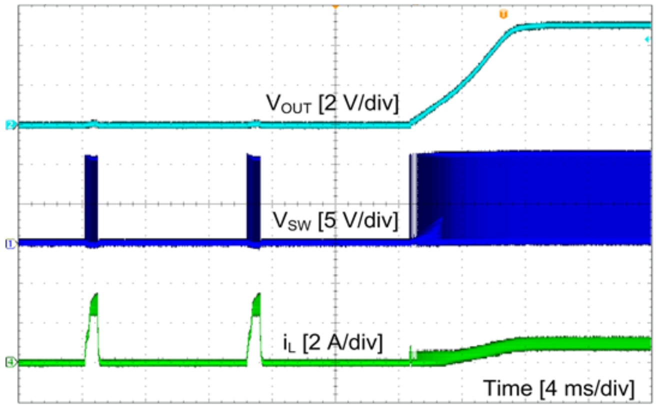
Figure 28. Line Transient

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 1600 kHz, L = 4.7 µH, C_{OUT} = 47 µF, T_A = 25 °C.



V_{OUT} = 5 V I_{OUT} = 1 A to short

Figure 29. Short Protection



V_{OUT} = 5 V I_{OUT} = short to 1 A

Figure 30. Short Recovery

9 Power Supply Recommendations

The LMR23615 is designed to operate from an input voltage supply range between 4 V and 36 V. This input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR23615 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR23615, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power-conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and PGND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the PGND pin and PAD.
2. Place bypass capacitors for V_{CC} close to the VCC pin and ground the bypass capacitor to device ground.
3. Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB} must be located close to the FB pin. Place C_{FF} directly in parallel with R_{FBT}. If V_{OUT} accuracy at the load is important, ensure that the V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
4. Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
5. Have a single point ground connection to the plane. Route the ground connections for the feedback and enable components to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
6. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. Provide adequate device heat sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat sinking to keep the junction temperature below 125°C.

10.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitor(s) as close as possible to the VIN and PGND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for high-current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD.

Place the bypass capacitors on VCC as close as possible to the pin and closely grounded to PGND and the exposed PAD.

10.1.2 Ground Plane and Thermal Considerations

TI recommends using one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground plane using vias right next to the bypass capacitors. PGND pin is connected to the source of the internal LS switch. They must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at switching frequency and may bounce due to load variations. PGND trace, as well as VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.

TI recommends providing adequate device heat sinking by utilizing the PAD of the device as the primary thermal path. Use a minimum 4 by 2 array of 12 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias should be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of, 2 oz / 1 oz / 1 oz / 2 oz. Four-layer boards with enough copper thickness provides low current conduction impedance, proper shielding, and lower thermal resistance.

Layout Guidelines (continued)

The thermal characteristics of the LMR23615 are specified using the parameter $R_{\theta JA}$, which characterize the junction temperature of silicon to the ambient temperature in a specific system. Although the value of $R_{\theta JA}$ is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \times R_{\theta JA} + T_A \tag{23}$$

$$P_D = V_{IN} \text{ x } I_{IN} \times (1 – \text{Efficiency}) – 1.1 \times I_{OUT}^2 \times \text{DCR in watt}$$

where

- T_J = junction temperature in °C
- P_D = device power dissipation in watt
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the device in °C/W
- T_A = ambient temperature in °C
- DCR = inductor DC parasitic resistance in ohm (24)

The recommended operating junction temperature of the LMR23615 is 125°C. $R_{\theta JA}$ is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

10.1.3 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider and C_{FF} close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider and C_{FF} closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provide the best output accuracy. Route the voltage sense trace from the load to the feedback resistor divider away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high-value resistors are used to set the output voltage. TI recommends routing the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This provides further shielding for the voltage feedback path from EMI noises.

10.2 Layout Example

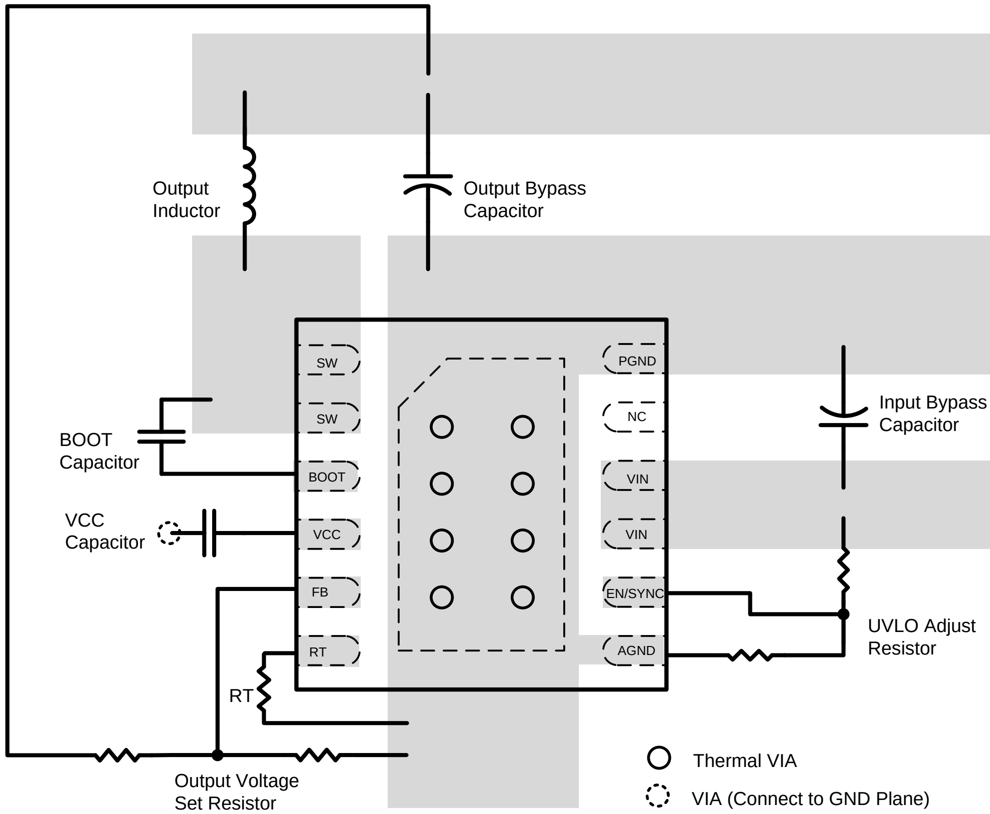


Figure 31. LMR23615 Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

*11.1.1.1 使用 **WEBENCH®** 工具创建定制设计*

单击此处，使用 LMR23615 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 首先键入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH, SIMPLE SWITCHER are registered trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR23615DRRR	ACTIVE	WSON	DRR	12	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	23615	Samples
LMR23615DRRT	ACTIVE	WSON	DRR	12	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	23615	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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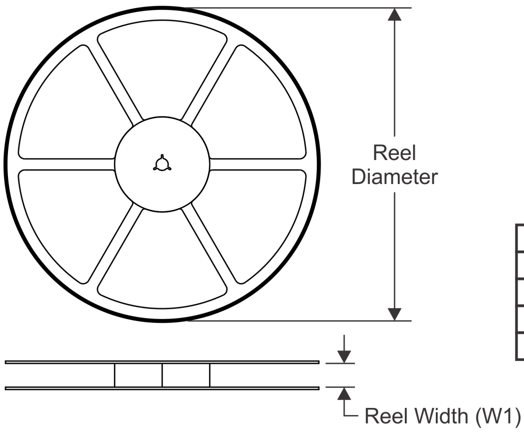
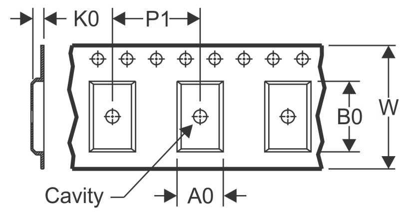
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

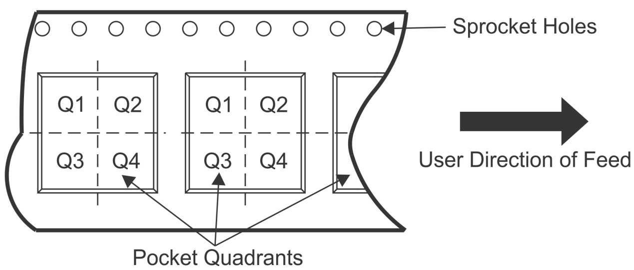


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

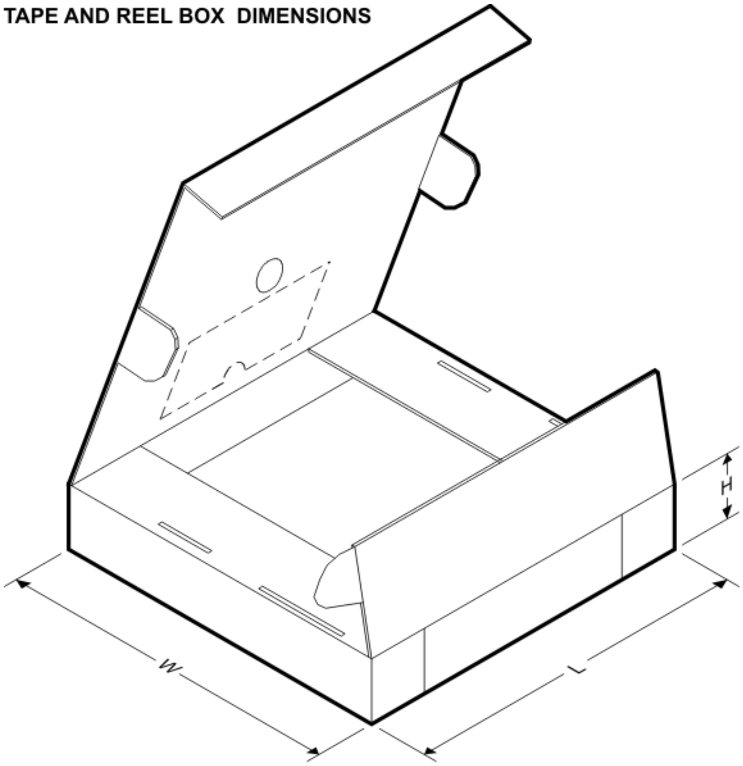
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

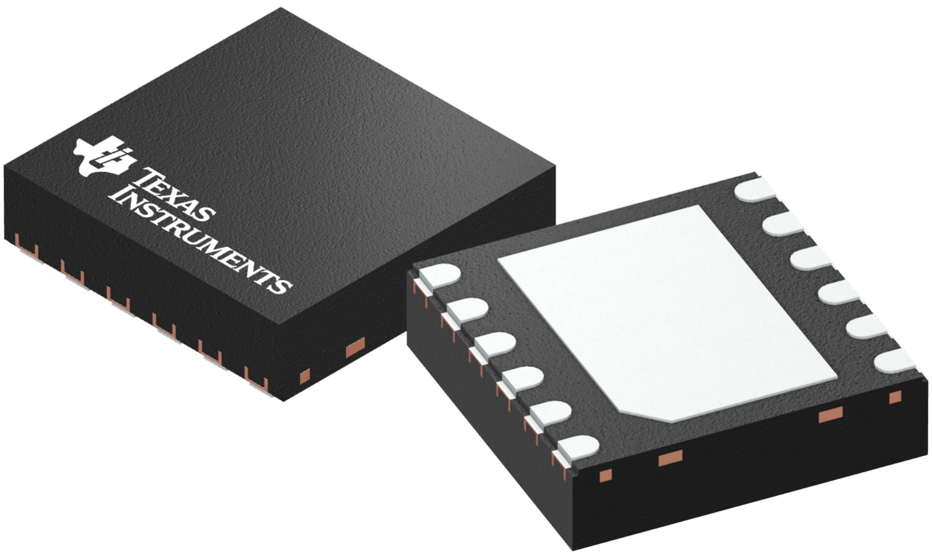
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR23615DRRR	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23615DRRT	WSON	DRR	12	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



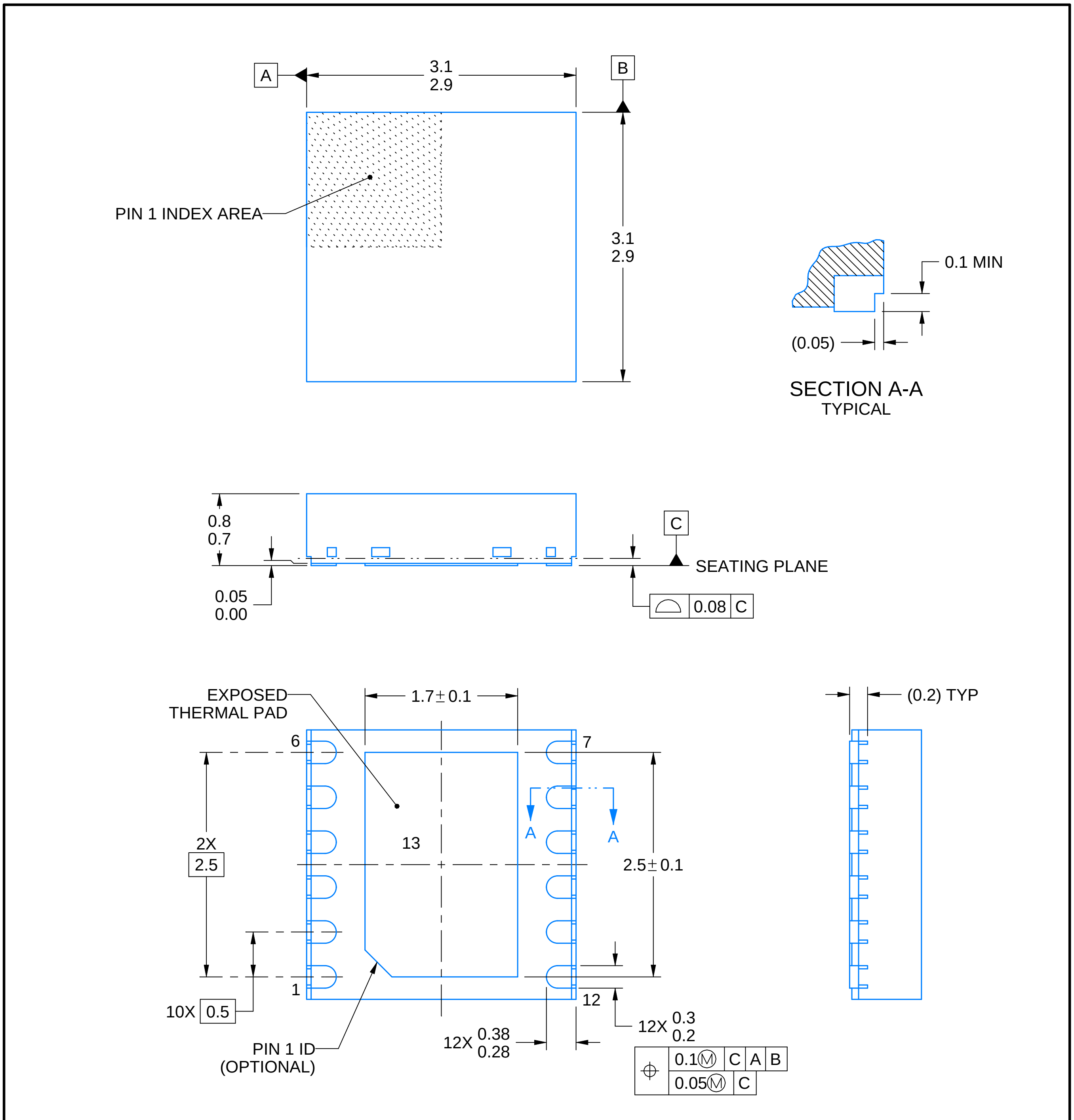
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR23615DRRR	WSON	DRR	12	3000	367.0	367.0	38.0
LMR23615DRRT	WSON	DRR	12	250	213.0	191.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4223490/A



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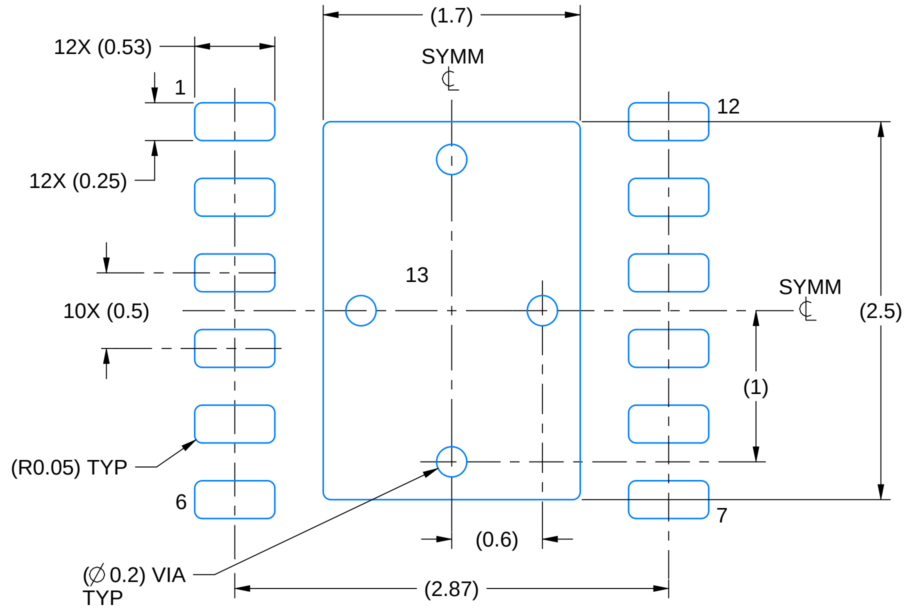
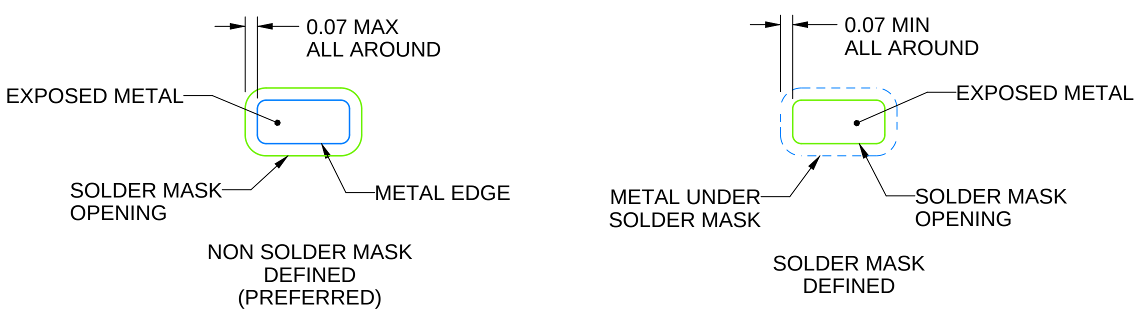
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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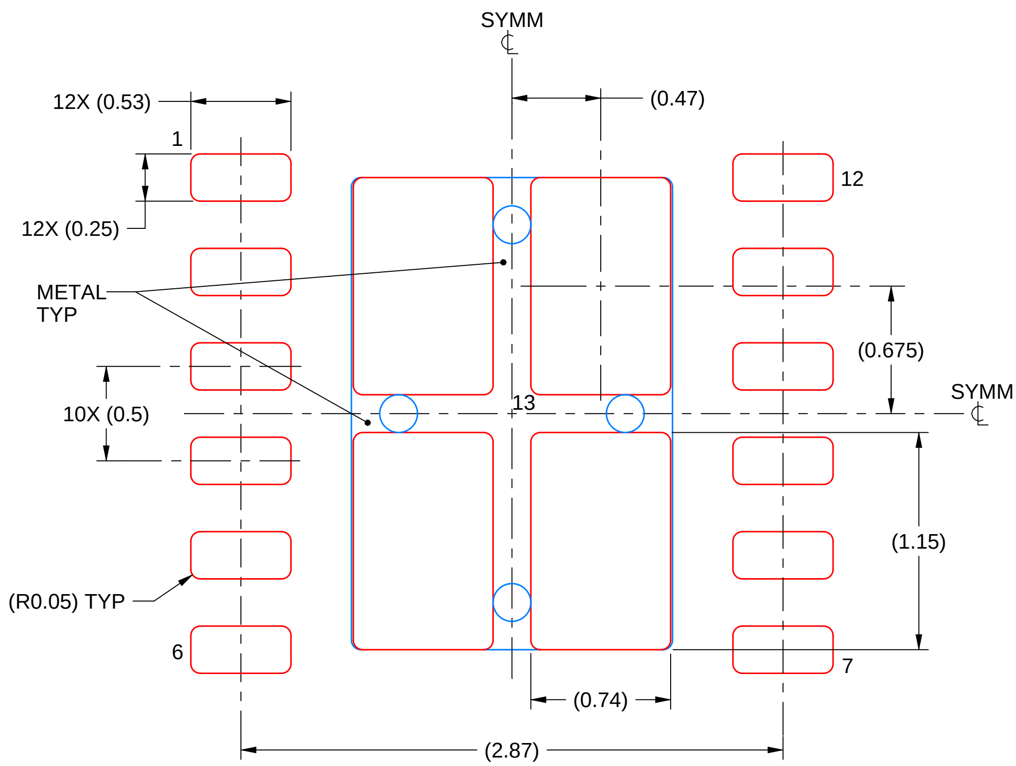
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80.1% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223146/D 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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