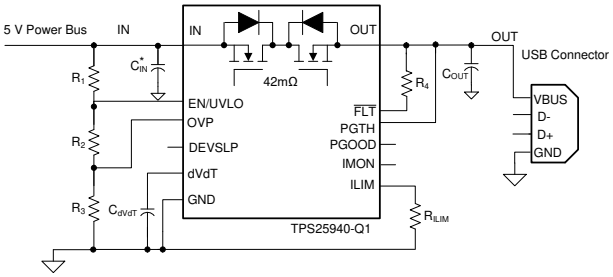
# 具有集成式电池短路保护功能的 TPS25940xx-Q1 2.7V 至 18V 电子保险丝

## 1 特性

- 适用于汽车电子应用
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C5
- 2.7V 至 18V 工作电压，20V（最大值）
- 总 $R_{ON}$：42mΩ（典型值）
- 可调节电流限值：0.6A 至 5.3A (±8%)
- IMON 电流指示器输出
  - 针对 TPS25940-Q1/TPS25940L-Q1 的 ±8% 精度
- 可调节欠压阈值和过压阈值 (±2%)
- 反向电流阻断
- 1 µs 反向电压关断
- 可编程 $dV_o/dt$ 控制
- 电源正常和故障输出
- 电池短路保护
- 接地短路保护
- TPS25940-Q1/TPS259401A-Q1：自动重试
- TPS25940L-Q1：闭锁

## 2 应用

- 汽车信息娱乐系统
- 高级驾驶员辅助系统 (ADAS) 摄像头和雷达传感器
- USB 集线器
- 电源多路复用
- 保持电源管理




简化版原理图

## 3 说明

TPS25940xx-Q1 电子保险丝电源开关是功能丰富的紧凑型电源管理器件，具有一整套保护功能。宽工作范围可实现对很多常用直流总线电压的控制。该器件集成的背靠背场效应晶体管 (FET) 可提供双向电流控制，很好地适用于防止系统中的负载侧储能流回故障电源总线。

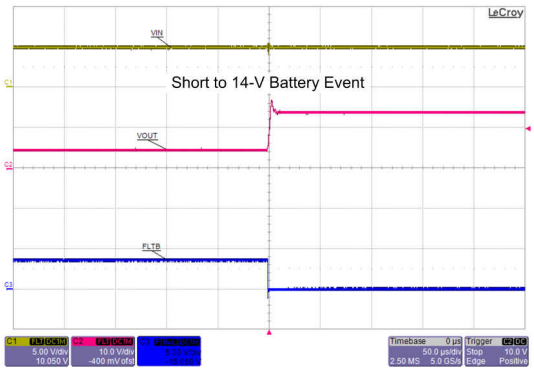
负载、电源和器件保护由很多可编程特性提供，其中包括过流，$dV_o/dt$ 斜率和过压、欠压阈值。为了实现系统状态监视和下游负载控制，此器件提供 PGOOD、$\overline{FLT}$ 和精密电流监视输出。精确的可编程欠压和过压阈值及模式简化了电源管理设计。

TPS25940xx-Q1 可监视 $V_{(IN)}$ 和 $V_{(OUT)}$，以便在 $V_{(IN)} < (V_{(OUT)} - 66mV)$ 时提供真正的反向电流阻断。该功能可在输出端发生电池短路故障期间为电源总线提供过压保护支持。

**器件信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS25940-Q1 | 超薄四方扁平无引线 (WQFN) (20) | 3.00mm x 4.00mm |
| TPS25940L-Q1 | | |
| TPS259401A-Q1 | | |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




输出端电池短路检测与保护

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision D (September 2018) to Revision E (January 2021) | Page |
|---|---|
| • 更新了整个文档的表、图和交叉参考的编号格式 | 1 |
| • 向数据表添加了 TPS259401A-Q1 型号 | 1 |
| • Added *Device Comparison* table | 3 |

| Changes from Revision C (July 2018) to Revision D (September 2018) | Page |
|---|---|
| • Changed internal ramp rate of 12 V/ms for output to 30 V/ms | 19 |

| Changes from Revision B (November 2017) to Revision C (July 2018) | Page |
|---|---|
| • 从“量产数据”更改为“混合量产” | 1 |
| • 添加了闭锁型号 (TPS25940L-Q1) | 1 |

| Changes from Revision A (June 2016) to Revision B (November 2017) | Page |
|---|---|
| • 向*应用信息* 部分添加了 9.2.4.3 小节“使用 TPS25940-Q1 进行过载检测” | 1 |

| Changes from Revision * (May 2016) to Revision A (June 2016) | Page |
|---|---|
| • 将器件状态从*产品预发布* 更改为*量产数据* | 1 |

## 5 Device Comparison Table

| Part Number | Fault Response | $R_{DSON}$ (max) | Minimum Current Limit | IMON Accuracy (max) |
|---|---|---|---|---|
| TPS25940-Q1 | Auto-Retry | 64 mΩ | 0.5 A | 8 % |
| TPS25940L-Q1 | Latch-off | 64 mΩ | 0.5 A | 8 % |
| TPS259401A-Q1 | Auto-Retry | 85 mΩ | 1 A | Not specified |

# 6 Pin Configuration and Functions

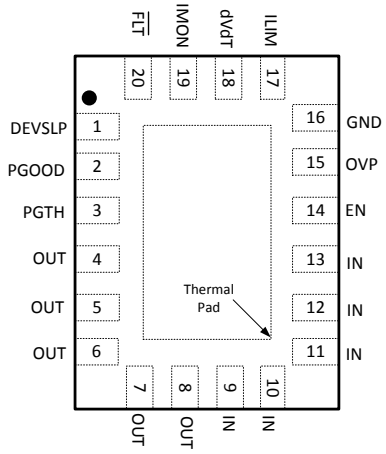



**图 6-1. RVC Package 20-Pin WQFN Top View**

**表 6-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DEVSLP | I | Active high. DevSleep mode control. A high at this pin activates the DevSleep mode (low power mode). If unused, leave floating or connect it to GND. |
| 2 | PGOOD | O | Active high. A high indicates PGTH has crossed the threshold value. It is an open drain output. If unused, leave floating. |
| 3 | PGTH | I | Positive input of PGOOD comparator. If unused connect to OUT or GND. |
| 4 | OUT | O | Power output of the device. |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| 8 | | | |
| 9 | IN | I | Power input and supply voltage of the device. |
| 10 | | | |
| 11 | | | |
| 12 | | | |
| 13 | | | |
| 14 | EN/UVLO | I | Input for setting programmable undervoltage lockout threshold. An undervoltage event opens internal FET and assert $\overline{FLT}$ to indicate power-failure. |
| 15 | OVP | I | Input for setting programmable overvoltage protection threshold. An overvoltage event opens the internal FET and assert $\overline{FLT}$ to indicate overvoltage. |
| 16 | GND | — | Ground. The GND terminal must be connected to the exposed PowerPAD. This PowerPAD must be connected to a PCB ground plane using multiple vias for good thermal performance. |
| 17 | ILIM | I/O | A resistor from this pin to GND sets the overload and short-circuit current limit. |
| 18 | dVdT | I/O | A capacitor from this pin to GND sets the ramp rate of output voltage. |
| 19 | IMON | O | This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage, used as analog current monitor. If unused, leave floating. |
| 20 | $\overline{FLT}$ | O | Fault event indicator, goes low to indicate fault condition because of undervoltage, overvoltage, reverse voltage and thermal shutdown event. It is an open drain output. If unused, leave floating. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | IN, OUT, PGTH, PGOOD, EN/UVLO, OVP, DEVSLP, $\overline{FLT}$ | –0.3 | 20 | V |
| | IN, OUT (10 ms transient) | | 22 | |
| | dVdT, ILIM | –0.3 | 3.6 | |
| | IMON | –0.3 | 7 | |
| Sink current | PGOOD, $\overline{FLT}$, dVdT | | 10 | mA |
| Maximum continuous switch current, $T_A$ = 85°C(2) | $I_{MAX}$ | | 4.78 | A |
| Source current | dVdT, ILIM, IMON | Internally Limited | | |
| Continuous power dissipation | | See the *Thermal Information* table | | |
| Maximum junction temperature | $T_J$ | –40 | 150 | °C |
| Storage temperature | $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Assumes 15 K power-on-hours at 100% duty cycle. This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI's semiconductor products.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±3000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| IN | Input voltage | 2.7 | | 18 | V |
| EN/UVLO, OVP, DEVSLP, OUT, PGTH, PGOOD, $\overline{FLT}$ | | 0 | | 18 | |
| dVdT, ILIM | | 0 | | 3 | |
| IMON | | 0 | | 6 | |
| ILIM | Resistance | 16.9 | | 150 | kΩ |
| IMON | | 1 | | | |
| OUT | External capacitance | 0.1 | | | µF |
| dVdT | | | | 470 | nF |
| $T_J$ | Operating junction temperature | –40 | 25 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | TPS25940xx-Q1 RVC (WQFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 38.1 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance | 40.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.7 | °C/W |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance | 3.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

–40°C ≤ $T_J$ = $T_A$ ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND INTERNAL UNDERVOLTAGE LOCKOUT** | | | | | | |
| $V_{(IN)}$ | Operating input voltage | | 2.7 | | 18 | V |
| $V_{(UVR)}$ | Internal UVLO threshold, rising | | 2.2 | 2.3 | 2.4 | V |
| $V_{(UVRhys)}$ | Internal UVLO hysteresis | | 105 | 116 | 125 | mV |
| $I_{Q\ (ON)}$ | Supply current, enabled | $V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 3 V | 140 | 210 | 300 | µA |
| | | $V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 12 V | 140 | 199 | 260 | |
| | | $V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 18 V | 140 | 202 | 270 | |
| $I_{Q\ (OFF)}$ | Supply current, disabled | $V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 3 V | 4 | 8.6 | 15 | µA |
| | | $V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 12 V | 6 | 15 | 20 | |
| | | $V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 18 V | 8 | 18.5 | 25 | |
| $I_{Q\ (DEVSLP)}$ | Supply current, devSleep mode | $V_{(DEVSLP)}$ = 0 V, $V_{(IN)}$ = 2.7 V to 18 V | 70 | 95 | 130 | µA |
| **ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT** | | | | | | |
| $V_{(ENR)}$ | EN/UVLO threshold voltage, rising | | 0.97 | 0.99 | 1.01 | V |
| $V_{(ENF)}$ | EN/UVLO threshold voltage, falling | | 0.9 | 0.92 | 0.94 | V |
| $V_{(SHUTF)}$ | EN threshold voltage for Low $I_Q$ shutdown, falling | | 0.3 | 0.47 | 0.63 | V |
| $V_{(SHUTF\ hys)}$ | EN hysteresis for low $I_Q$ shutdown, hysteresis[1] | | | 66 | | mV |
| $I_{EN}$ | EN Input leakage current | 0 V ≤ $V_{(EN/UVLO)}$ ≤ 18 V | –100 | 0 | 100 | nA |
| **OVER VOLTAGE PROTECTION (OVP) INPUT** | | | | | | |
| $V_{(OVPR)}$ | Overvoltage threshold voltage, rising | | 0.97 | 0.99 | 1.01 | V |
| $V_{(OVPF)}$ | Overvoltage threshold voltage, falling | | 0.9 | 0.92 | 0.94 | V |
| $I_{(OVP)}$ | OVP input leakage current | 0 V ≤ $V_{(OVP)}$ ≤ 5 V | –100 | 0 | 100 | nA |
| **DEVSLP MODE INPUT (DEVSLP): ACTIVE HIGH** | | | | | | |
| $V_{(DEVSLPR)}$ | DEVSLP threshold voltage, rising | | 1.6 | 1.85 | 2 | V |
| $V_{(DEVSLPF)}$ | DEVSLP threshold voltage, falling | | 0.8 | 0.96 | 1.1 | V |
| $I_{(DEVSLP)}$ | DEVSLP input leakage current | 0.2 V ≤ $V_{(DEVSLP)}$ ≤ 18 V | 0.6 | 1 | 1.25 | µA |
| **OUTPUT RAMP CONTROL (dVdT)** | | | | | | |
| $I_{(dVdT)}$ | dVdT charging current | $V_{(dVdT)}$ = 0 V | 0.85 | 1 | 1.15 | µA |
| $R_{(dVdT)}$ | dVdT discharging resistance | EN/UVLO = 0 V, $I_{(dVdT)}$ = 10 mA sinking | | 16 | 24 | Ω |
| $V_{(dVdTmax)}$ | dVdT maximum capacitor voltage | | 2.6 | 2.88 | 3.1 | V |
| $GAIN_{(dVdT)}$ | dVdT to OUT gain | $\Delta V_{(OUT)}/\Delta V_{(dVdT)}$ | 11.65 | 11.9 | 12.05 | V/V |

## 7.5 Electrical Characteristics (continued)

–40°C ≤ $T_J$ = $T_A$ ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT LIMIT PROGRAMMING (ILIM)** | | | | | | |
| $V_{(ILIM)}$ | ILIM bias voltage | | | 0.87 | | V |
| $I_{(LIM)}$ | Current limit[2] | $R_{(ILIM)}$ = 150 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V, Only for TPS25940-Q1/TPS25940L-Q1 | 0.53 | 0.58 | 0.63 | A |
| | | $R_{(ILIM)}$ = 88.7 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V | 0.9 | 0.99 | 1.07 | |
| | | $R_{(ILIM)}$ = 42.2 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V | 1.92 | 2.08 | 2.25 | |
| | | $R_{(ILIM)}$ = 20 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V | 4.09 | 4.45 | 4.81 | |
| | | $R_{(ILIM)}$ = 16.9 kΩ, ($V_{(IN)}$ – $V_{(OUT)}$) = 1 V | 4.78 | 5.2 | 5.62 | |
| | | $R_{(ILIM)}$ = OPEN, Open resistor current limit (single point failure test: UL60950) | 0.35 | 0.45 | 0.55 | |
| | | $R_{(ILIM)}$ = SHORT, Shorted resistor current limit (single point failure test: UL60950) | 0.55 | 0.67 | 0.8 | |
| $I_{(DEVSLP(LIM))}$ | DevSleep mode current limit | | 0.55 | 0.67 | 0.8 | A |
| $I_{OS}$ | Short-circuit current limit [2] | $R_{(ILIM)}$ = 42.2 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ – $V_{(OUT)}$) = 5 V | 1.91 | 2.07 | 2.24 | A |
| | | $R_{(ILIM)}$ = 20 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ – $V_{(OUT)}$) = 5 V | 4 | 4.4 | 4.7 | |
| | | $R_{(ILIM)}$ = 16.9 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ – $V_{(OUT)}$) = 5 V | 4.7 | 5.11 | 5.52 | |
| $I_{(FASTRIP)}$ | Fast-trip comparator threshold[1] [2] | | | 1.5 x $I_{(LIM)}$ + 0.375 | | A |
| **CURRENT MONITOR OUTPUT (IMON)** | | | | | | |
| $GAIN_{(IMON)}$ | Gain factor $I_{(IMON)}$:$I_{(OUT)}$ | 1 A ≤ $I_{(OUT)}$ ≤ 5 A | | 52.3 | | µA/A |
| | | 1 A ≤ $I_{(OUT)}$ ≤ 5 A, Only for TPS25940-Q1/TPS25940L-Q1 | 47.78 | 52.3 | 57.23 | µA/A |
| **MOSFET – POWER SWITCH** | | | | | | |
| $R_{ON}$ | IN to OUT - ON resistance | 1 A ≤ $I_{(OUT)}$ ≤ 5 A, $T_J$ = 25°C | 34 | 42 | 49 | mΩ |
| | | 1 A ≤ $I_{(OUT)}$ ≤ 5 A, –40°C ≤ $T_J$ ≤ +85°C | 26 | 42 | 58 | |
| | | 1 A ≤ $I_{(OUT)}$ ≤ 5 A, –40°C ≤ $T_J$ ≤ +125°C | 26 | 42 | 64 | |
| | | 1 A ≤ $I_{(OUT)}$ ≤ 5 A, –40°C ≤ $T_J$ ≤ +125°C, Only for TPS259401A-Q1 | | 55 | 85 | mΩ |
| **PASS FET OUTPUT (OUT)** | | | | | | |
| $I_{lkg(OUT)}$ | OUT leakage current in off state | $V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(OUT)}$ = 0 V (sourcing) | –2 | 0 | 2 | µA |
| | | $V_{(IN)}$ = 2.7 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(OUT)}$ = 18 V (sinking) | 6 | 13 | 20 | |
| $V_{(REVTH)}$ | $V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling | | –77 | –66 | –55 | mV |
| $V_{(FWDTH)}$ | $V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising | | 86 | 100 | 114 | mV |
| **FAULT FLAG ( $\overline{FLT}$): ACTIVE LOW** | | | | | | |
| $R_{(\overline{FLT})}$ | $\overline{FLT}$ internal pull-down resistance | $V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking | 10 | 18 | 30 | Ω |
| $I_{(\overline{FLT})}$ | $\overline{FLT}$ input leakage current | 0 V ≤ $V_{(\overline{FLT})}$ ≤ 18 V | –1 | 0 | 1 | µA |
| **POSITIVE INPUT for POWER-GOOD COMPARATOR (PGTH)** | | | | | | |
| $V_{(PGTHR)}$ | PGTH threshold voltage, rising | | 0.97 | 0.99 | 1.01 | V |
| $V_{(PGTHF)}$ | PGTH threshold voltage, falling | | 0.9 | 0.92 | 0.94 | V |
| $I_{(PGTH)}$ | PGTH input leakage current | 0 V ≤ $V_{(PGTH)}$ ≤ 18 V | –100 | 0 | 100 | nA |
| **POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH** | | | | | | |
| $R_{(PGOOD)}$ | PGOOD internal pull-down resistance | $V_{(PGTH)}$ = 0V, $I_{(PGOOD)}$ = 5 mA sinking | 10 | 20 | 35 | Ω |
| $I_{(PGOOD)}$ | PGOOD input leakage current | 0 V ≤ $V_{(PGOOD)}$ ≤ 18 V | –1 | 0 | 1 | µA |
| **THERMAL SHUT DOWN (TSD)** | | | | | | |
| $T_{(TSD)}$ | TSD threshold[1] | | | 160 | | °C |

## 7.5 Electrical Characteristics (continued)

–40°C ≤ $T_J$ = $T_A$ ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN\ /UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{(TSDhys)}$ | TSD hysteresis(1) | | | 12 | | °C |
| | Thermal fault response | TPS25940-Q1, TPS259401A-Q1 | | Auto-retry | | |
| | | TPS25940L-Q1 | | Latch-off | | |

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.

## 7.6 Timing Requirements

–40°C ≤ $T_J$ = $T_A$ ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN\ /UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). See 图 8-1 for the timing diagrams.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ENABLE and UVLO INPUT** | | | | | | |
| $t_{ON(dly)}$ | EN turnon delay | EN/UVLO ↑ (100 mV above $V_{(ENR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ < 0.8 nF | | 220 | | µs |
| | | EN/UVLO ↑ (100 mV above $V_{(ENR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ ≥ 0.8 nF, [$C_{(dVdT)}$ in nF] | | 100 + 150 × $C_{(dVdT)}$ | | µs |
| $t_{OFF(dly)}$ | EN turnoff delay | EN/UVLO ↓ (100 mV below $V_{(ENF)}$) to $\overline{FLT}$ ↓ | | 2 | | µs |
| **OVERVOLTAGE PROTECTION INPUT (OVP)** | | | | | | |
| $t_{OVP(dly)}$ | OVP disable delay | OVP ↑ (100 mV above $V_{(OVPR)}$) to $\overline{FLT}$ ↓ | | 2 | | µs |
| **OUTPUT RAMP CONTROL (dV/dT )** | | | | | | |
| $t_{dVdT}$ | Output ramp time | EN/UVLO ↑ to $V_{(OUT)}$ = 4.5 V, with $C_{(dVdT)}$ = open | | 0.12 | | ms |
| | | EN/UVLO ↑ to $V_{(OUT)}$ = 11 V, with $C_{(dVdT)}$ = open | 0.25 | 0.37 | 0.5 | ms |
| | | EN/UVLO ↑ to $V_{(OUT)}$ = 11 V, with $C_{(dVdT)}$ = 1 nF | | 0.97 | | ms |
| **CURRENT LIMIT** | | | | | | |
| $t_{FASTRIP(dly)}$ | Fast-trip comparator delay | $I_{(OUT)}$ > $I_{(FASTRIP)}$ | | 200 | | ns |
| **REVERSE PROTECTION COMPARATOR** | | | | | | |
| $t_{REV(dly)}$ | Reverse protection comparator delay | ($V_{(IN)}$ – $V_{(OUT)}$) ↓ (1 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$ ↓ | | 10 | | µs |
| | | ($V_{(IN)}$ – $V_{(OUT)}$) ↓ (10 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$ ↓ | | 1 | | µs |
| $t_{FWD(dly)}$ | | ($V_{(IN)}$ – $V_{(OUT)}$) ↑ (10 mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$ ↑ | | 3.1 | | µs |
| **POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH** | | | | | | |
| $t_{PGOODR}$ | PGOOD delay (de-glitch) time | Rising edge | 0.42 | 0.54 | 0.66 | ms |
| $t_{PGOODF}$ | | Falling edge | 0.42 | 0.54 | 0.66 | ms |
| **THERMAL SHUT DOWN (TSD)** | | | | | | |
| | Retry delay in TSD | TPS25940-Q1/TPS259401A-Q1 Only | | 128 | | ms |

## 7.7 Typical Characteristics

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

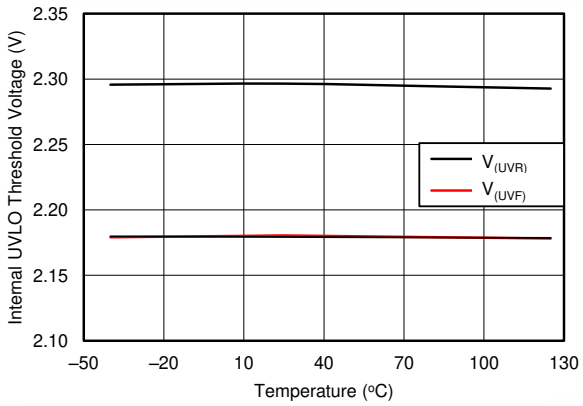



**图 7-1. UVLO Threshold Voltage vs Temperature**

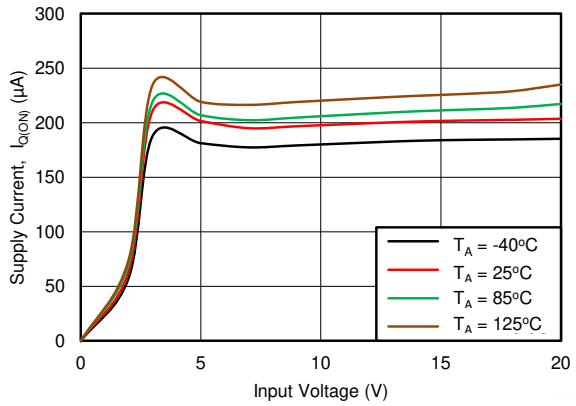



**图 7-2. Input Supply Current vs Supply Voltage During Normal Operation**

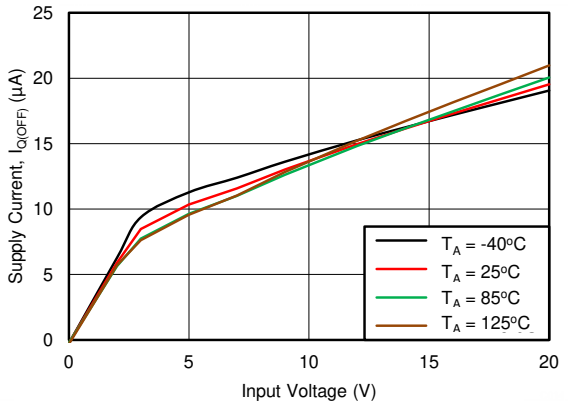



**图 7-3. Input Supply Current vs Supply Voltage at Shutdown**

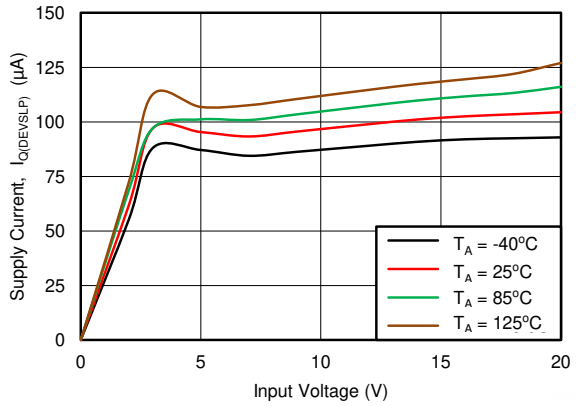



**图 7-4. Input Supply Current vs Supply Voltage in DevSleep Mode**

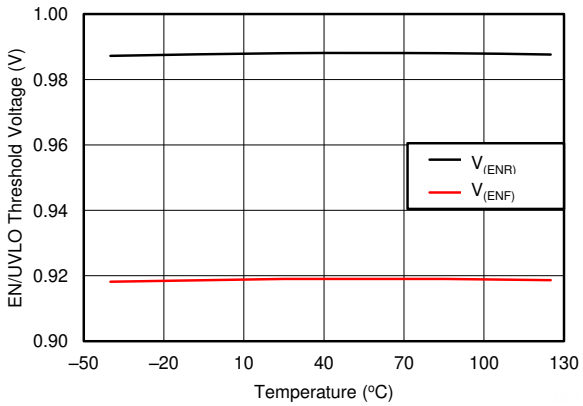



**图 7-5. EN Threshold Voltage vs Temperature**

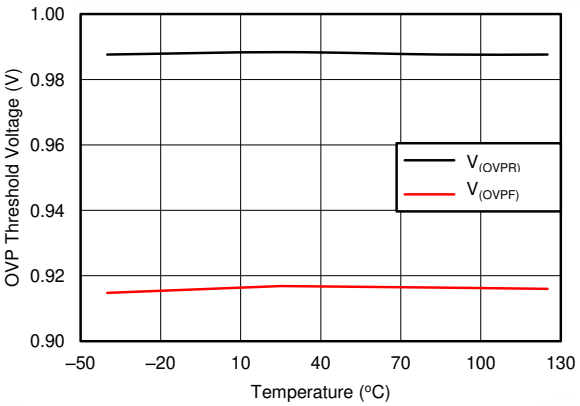



**图 7-6. OVP Threshold Voltage vs Temperature**

## 7.7 Typical Characteristics (continued)

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

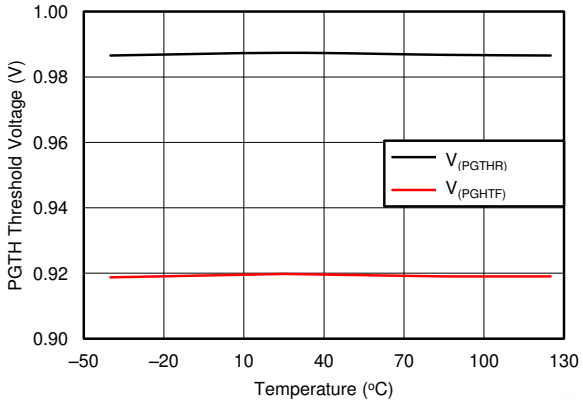



图 7-7. PGTH Threshold Voltage vs Temperature

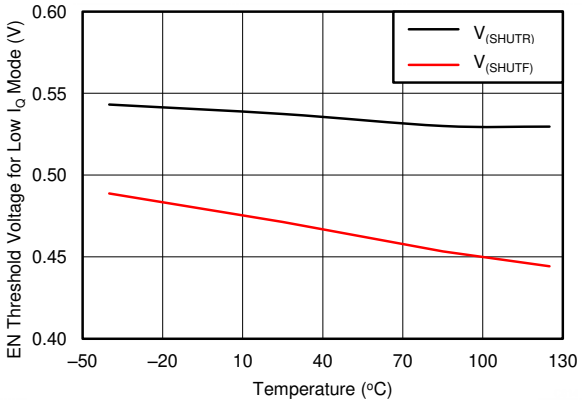



图 7-8. EN Threshold Voltage for Low IQ Mode vs Temperature

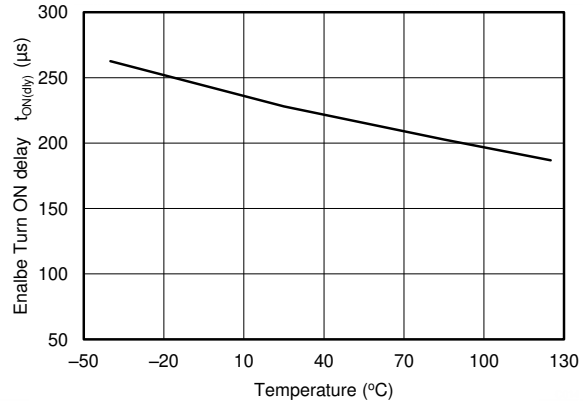



图 7-9. Enable Turn ON Delay vs Temperature

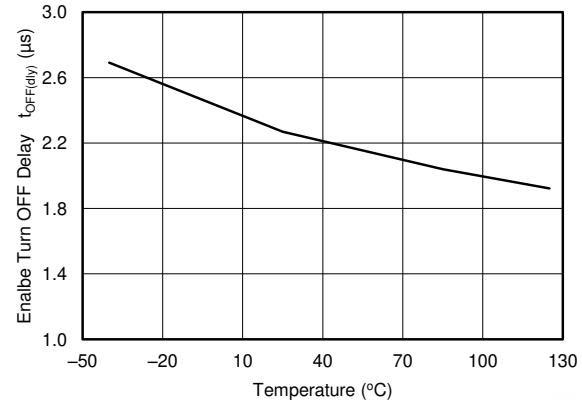



图 7-10. Enable Turn OFF Delay vs Temperature

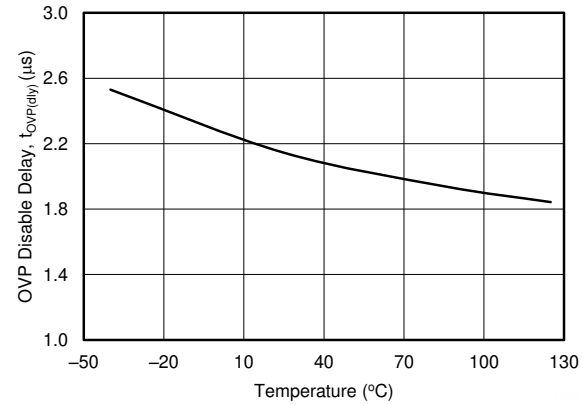



图 7-11. OVP Disable Delay vs Temperature

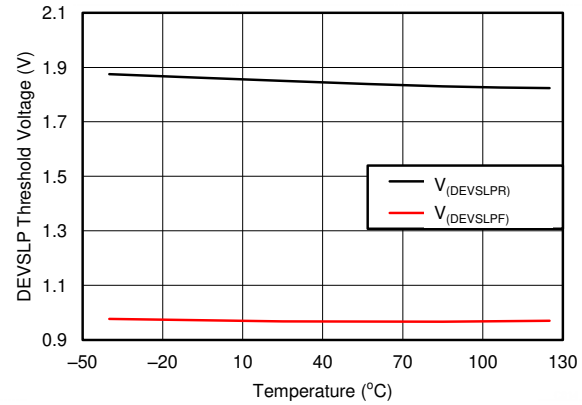



图 7-12. DEVSLP Threshold Voltage vs Temperature

## 7.7 Typical Characteristics (continued)

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

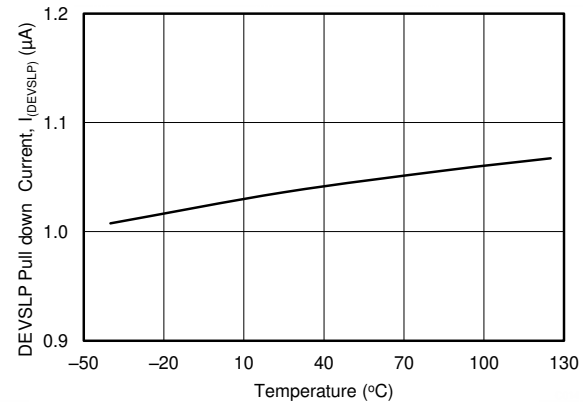



图 7-13. DEVSLP Pull Down Current vs Temperature

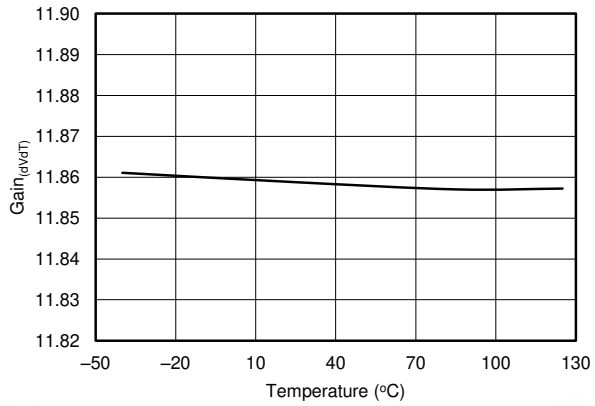



图 7-14. $GAIN_{(dVdT)}$ vs Temperature

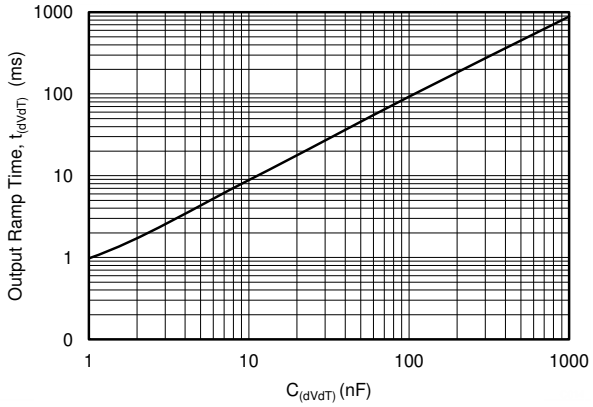



图 7-15. Output Ramp Time vs $C_{(dVdT)}$

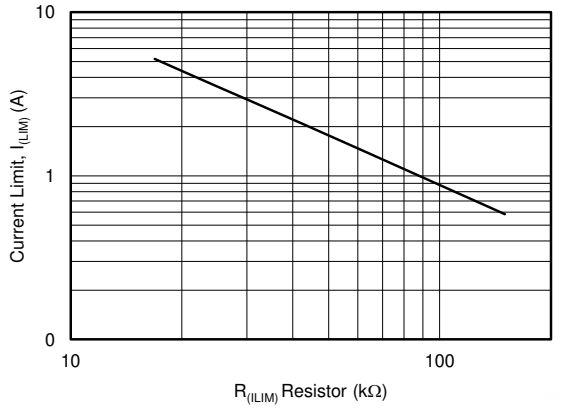



图 7-16. Current Limit vs Current Limit Resistor

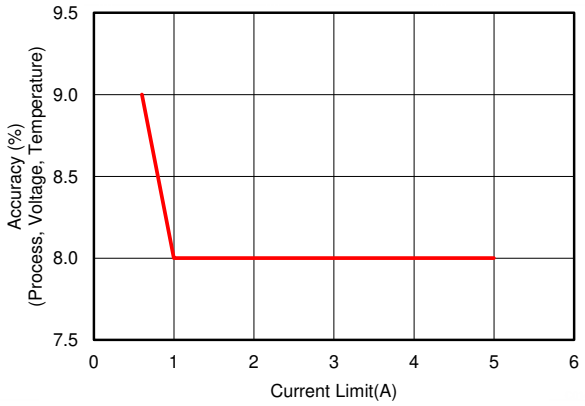



图 7-17. Current Limit Accuracy vs Current Limit

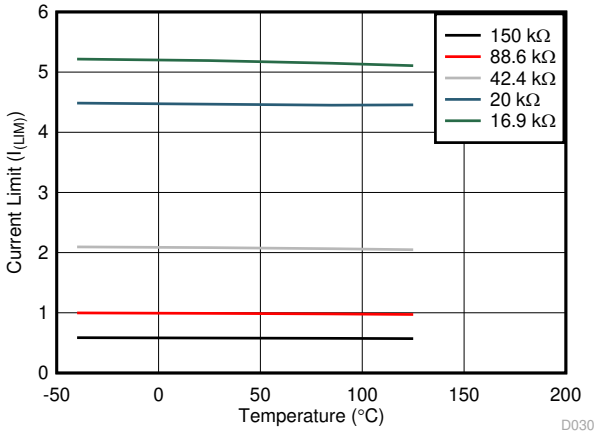



图 7-18. Current Limit vs Temperature Across $R_{(ILIM)}$

## 7.7 Typical Characteristics (continued)

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

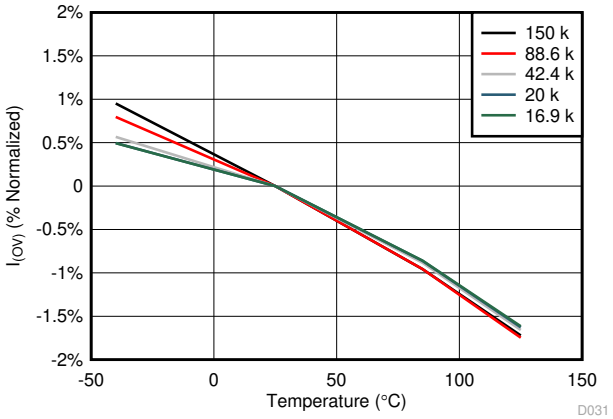
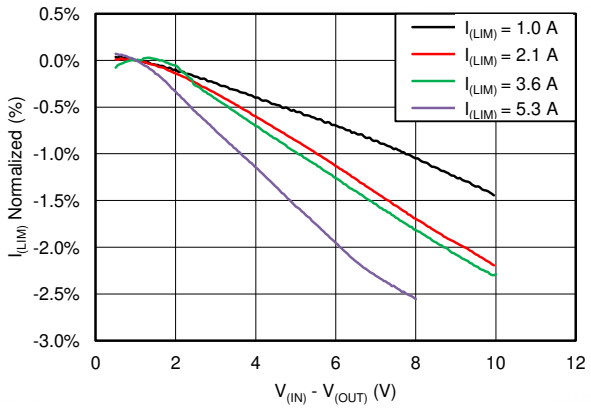



**图 7-19. Current Limit (% Normalized) vs $R_{(LIMIT)}$ Resistor**




Thermal shutdown occurs when $I_{(LIM)}$ = [$V_{(IN)}$ - $V_{(OUT)}$] > 8 V
5.3 A

**图 7-20. Current Limit Normalized (%) vs $V_{(IN)}$ – $V_{(OUT)}$**

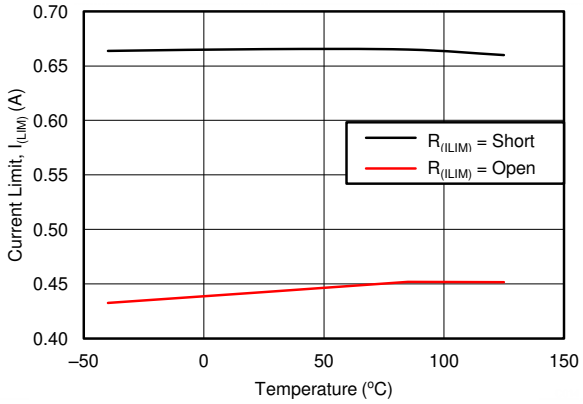



**图 7-21. Current Limit for $R_{(ILIM)}$ = Open and Short vs Temperature**

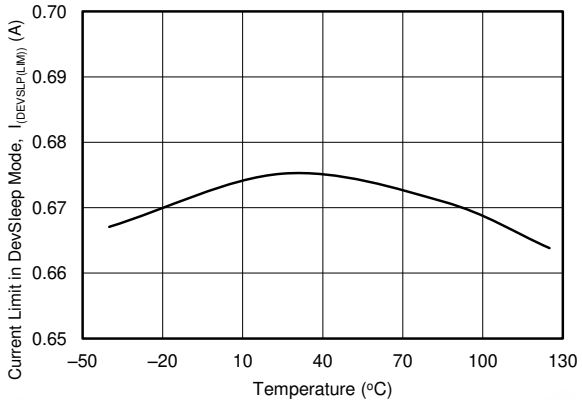



**图 7-22. Current Limit in DevSleep Mode vs Temperature**

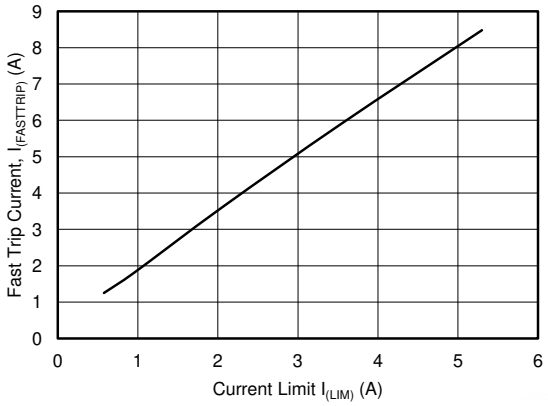



**图 7-23. Fast Trip Threshold vs Current Limit**

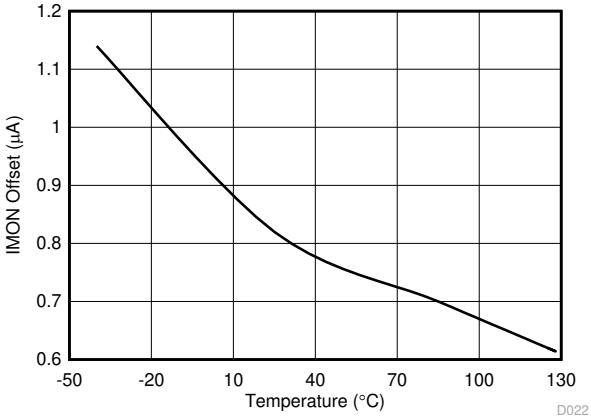



**图 7-24. IMON Offset vs Temperature**

## 7.7 Typical Characteristics (continued)

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

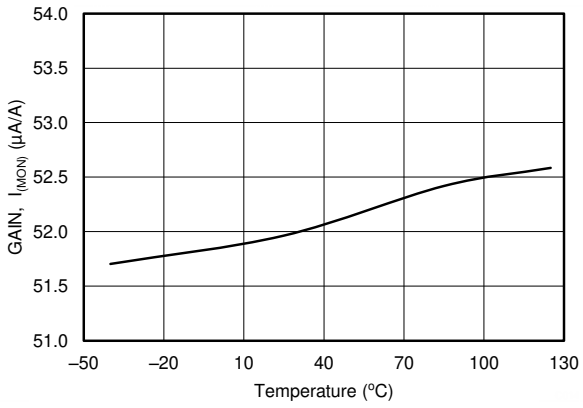



图 7-25. $GAIN_{(IMON)}$ vs Temperature

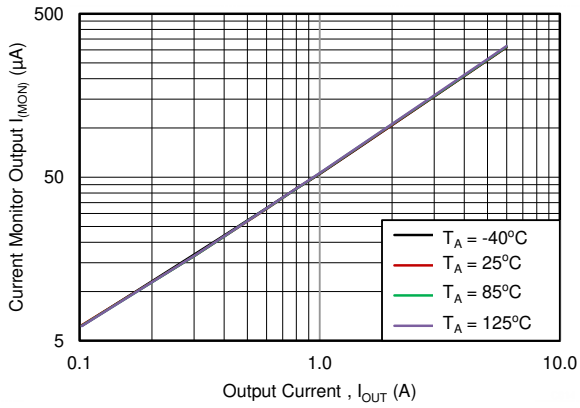



图 7-26. Current Monitor Output vs Output Current

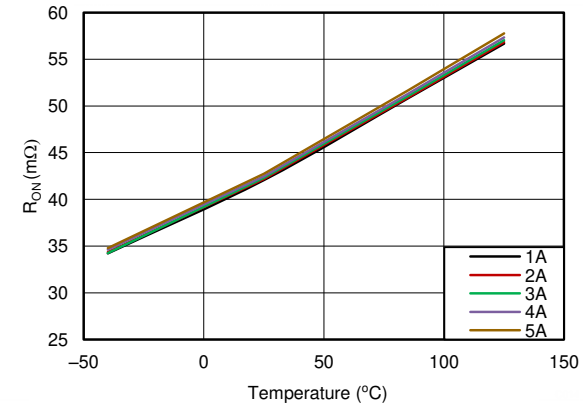



图 7-27. $R_{ON}$ vs Temperature Across Load Current

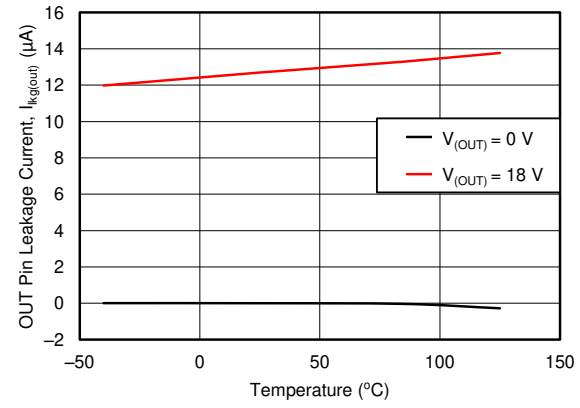



图 7-28. OUT Leakage Current in Off State vs Temperature

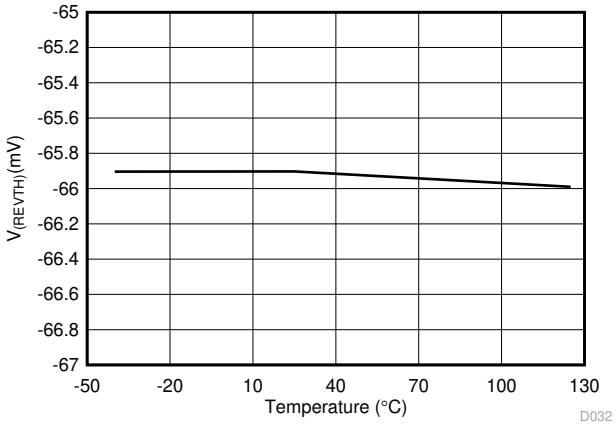



图 7-29. $V_{(REVTH)}$ vs Temperature

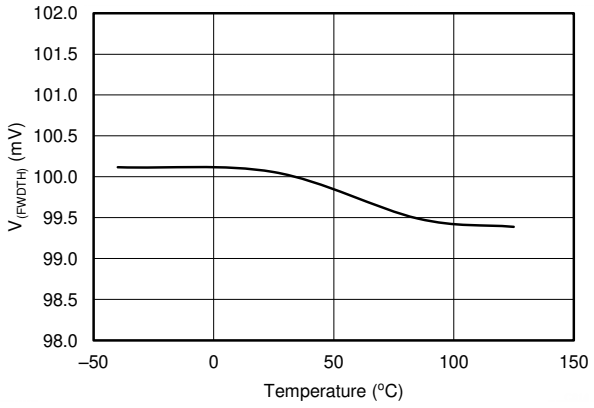
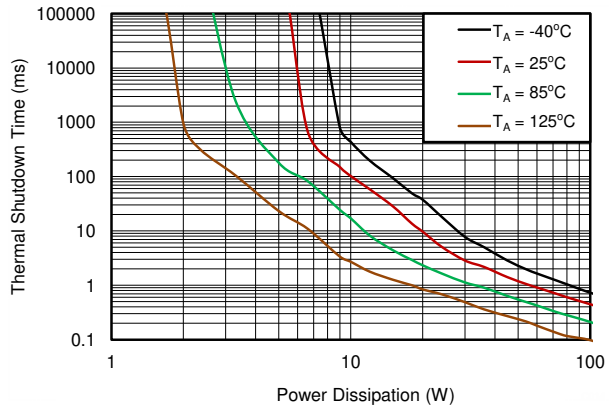



图 7-30. $V_{(FWDTH)}$ vs Temperature

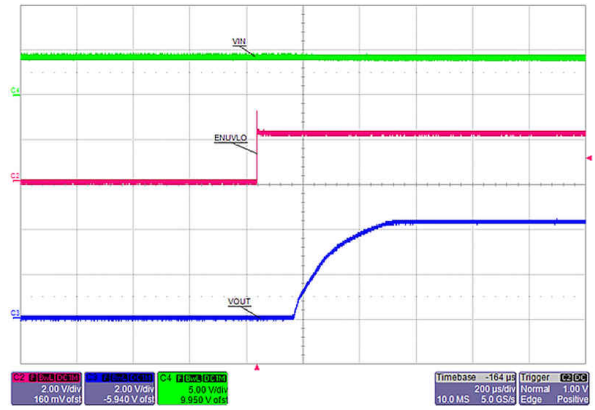
## 7.7 Typical Characteristics (continued)

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



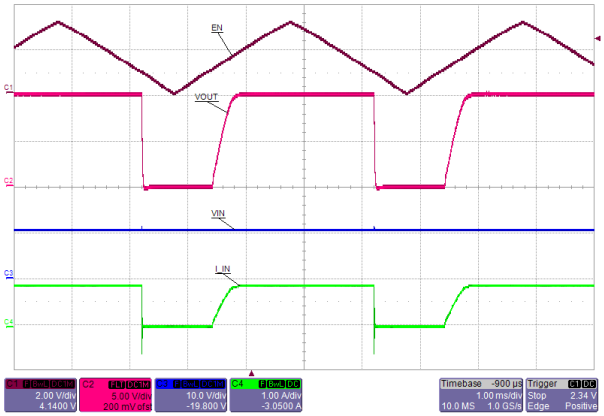

Taken on 2-Layer board, 2 oz.(0.08-mm thick) with GND plane area: 14 $cm^2$ (Top) and 20 $cm^2$ (bottom)

**图 7-31. Thermal Shutdown Time vs Power Dissipation**



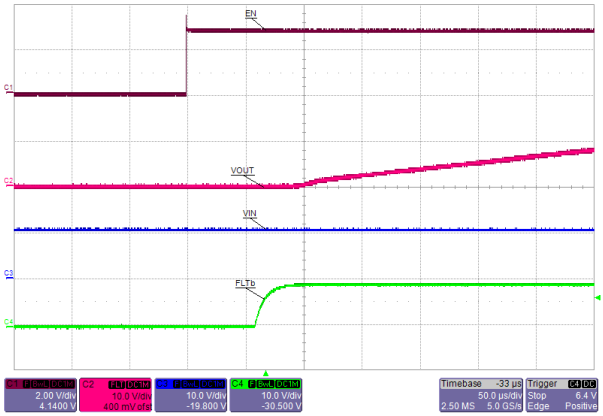

$V_{(IN)}$ = 4.5 V

**图 7-32. Turn ON with Enable**



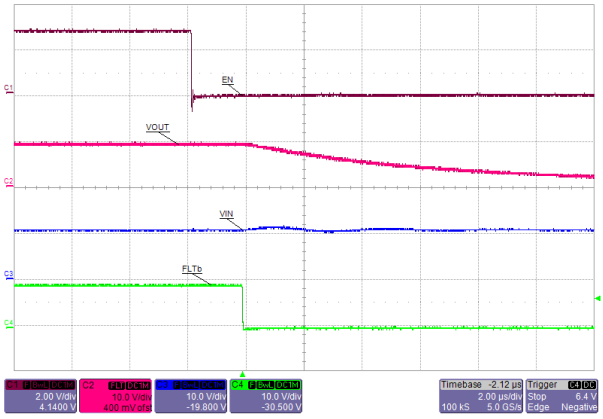

$V_{(IN)}$ = 11 V

**图 7-33. Turn ON and OFF with Enable**



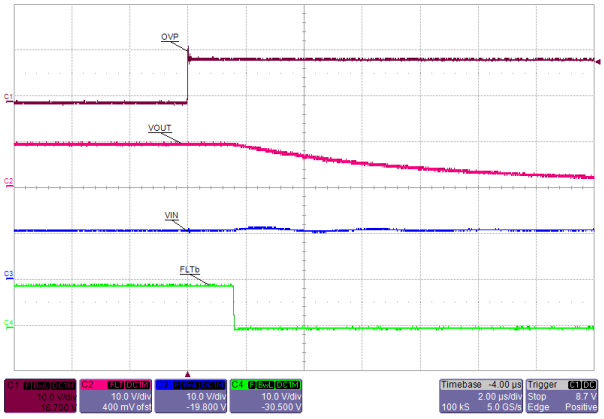

$R_{(\overline{FLT})}$=100 kΩ

**图 7-34. EN Turn ON Delay : EN ↑ to Output Ramp ↑**




$R_{(\overline{FLT})}$=100 kΩ

**图 7-35. EN Turn OFF Delay : EN ↓ to Fault ↓**

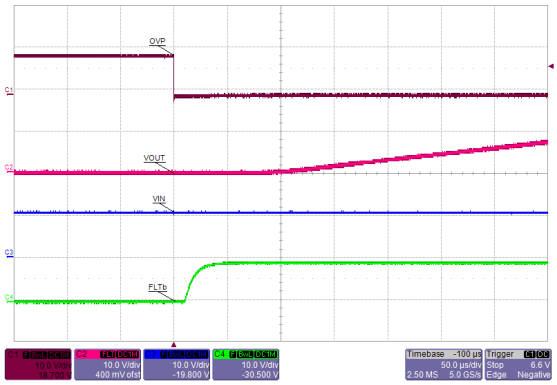



$V_{(IN)}$ = 12 V $R_L$ = 12 Ω $R_{(\overline{FLT})}$=100 kΩ

**图 7-36. OVP Turn OFF Delay: OVP ↑ to Fault ↓**

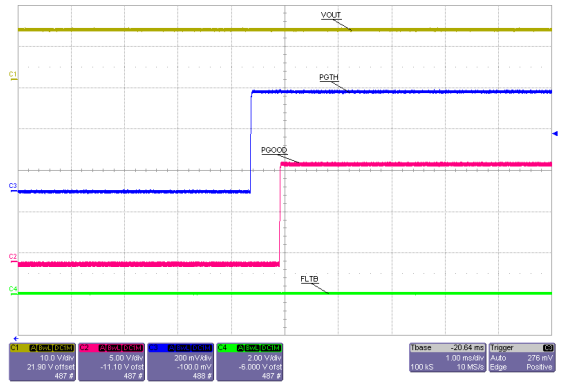
## 7.7 Typical Characteristics (continued)

Conditions are –40°C ≤ $T_A$ = $T_J$ ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



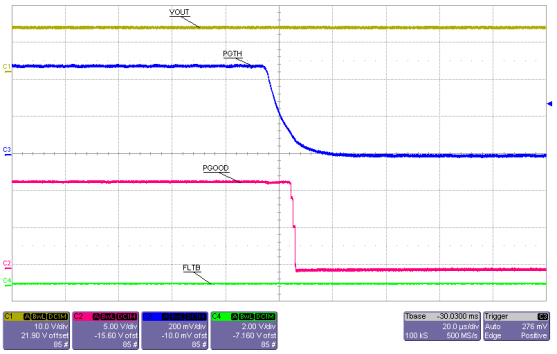

$V_{(IN)}$ = 12 V  $R_L$ = 12 Ω  $R_{(\overline{FLT})}$=100 kΩ

**图 7-37. OVP Turn ON Delay: OVP ↓ to Output Ramp ↑**



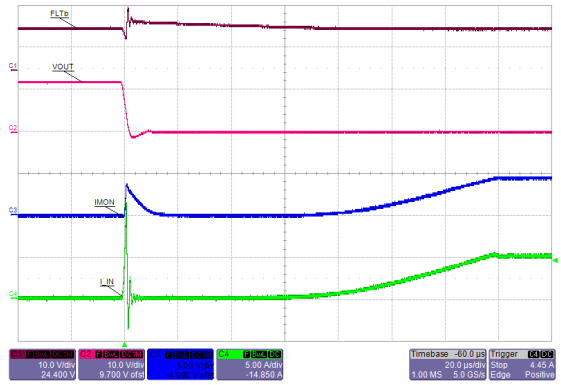

$V_{(IN)}$ = 12 V  $R_L$ = 12 Ω  $R_{(\overline{FLT})}$= 100 kΩ

**图 7-38. Power Good Delay (Rising)**



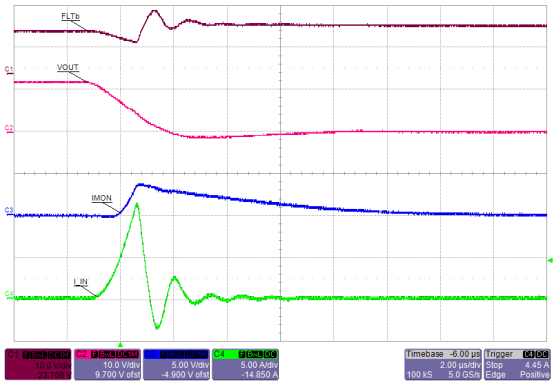

$V_{(IN)}$ = 12 V  $R_L$ = 12 Ω  $R_{(\overline{FLT})}$= 100 kΩ

**图 7-39. Power Good Delay (Falling)**




$R_{(\overline{FLT})}$ = 100 kΩ  $R_{(IMON)}$ = 16.9 kΩ  $R_{(ILIM)}$ = 17.8 kΩ

**图 7-40. Hot-Short: Fast Trip Response and Current Regulation**




$R_{(\overline{FLT})}$= 100 kΩ  $R_{(IMON)}$ = 16.9 kΩ  $R_{(ILIM)}$ = 17.8 kΩ

**图 7-41. Hot-Short: Fast Trip Response (Zoomed)**

## 8 Parametric Measurement Information

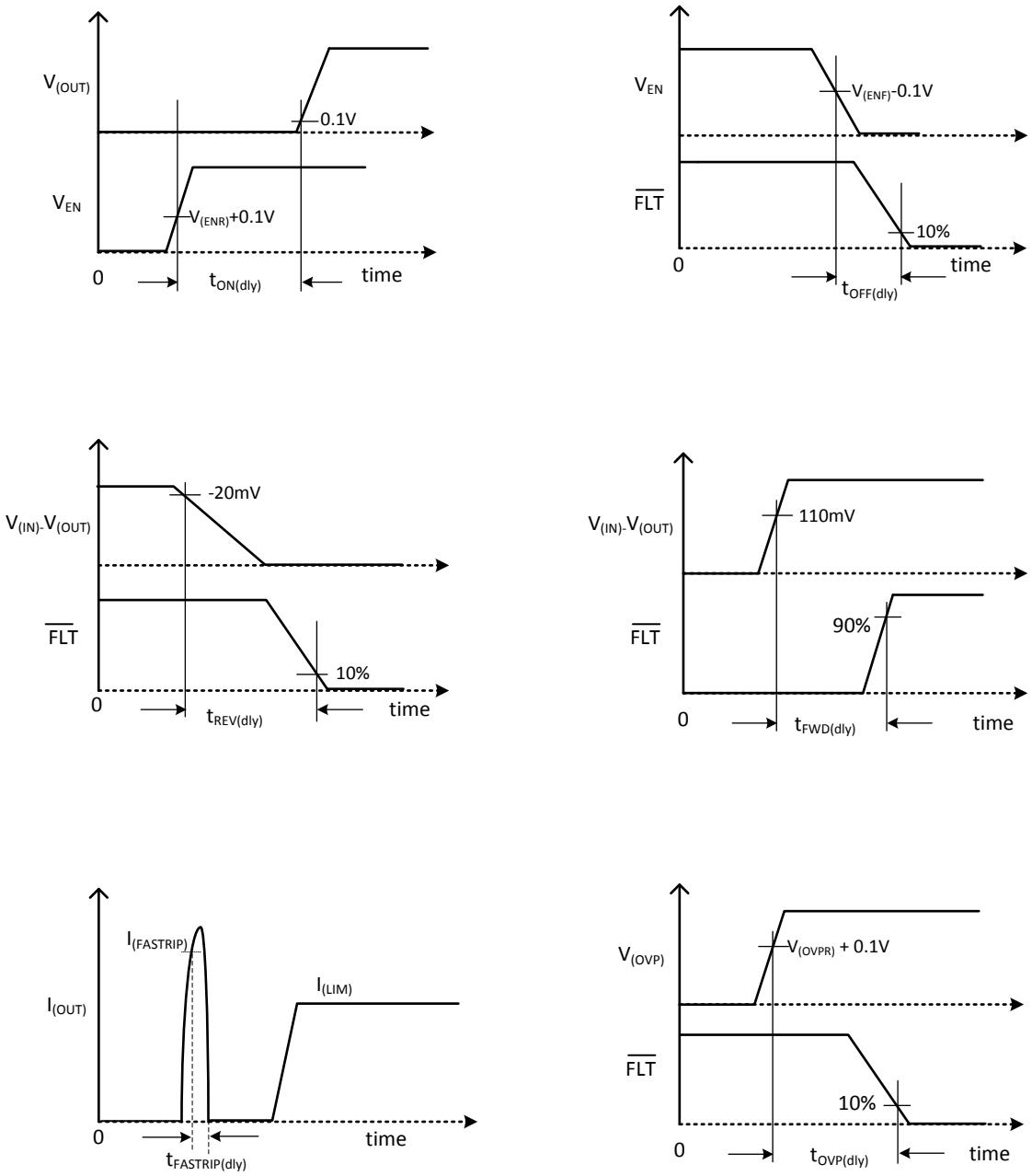



**图 8-1. Timing Diagrams**

# 9 Detailed Description

## 9.1 Overview

The TPS25940xx-Q1 device is a smart eFuse with integrated back-to-back FETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 2.7 V to 18 V.

For hot-plug-in boards, the device provides hot-swap power management with in-rush current control and programmable output ramp-rate. The device integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.6 A and 5.3 A via an external resistor.

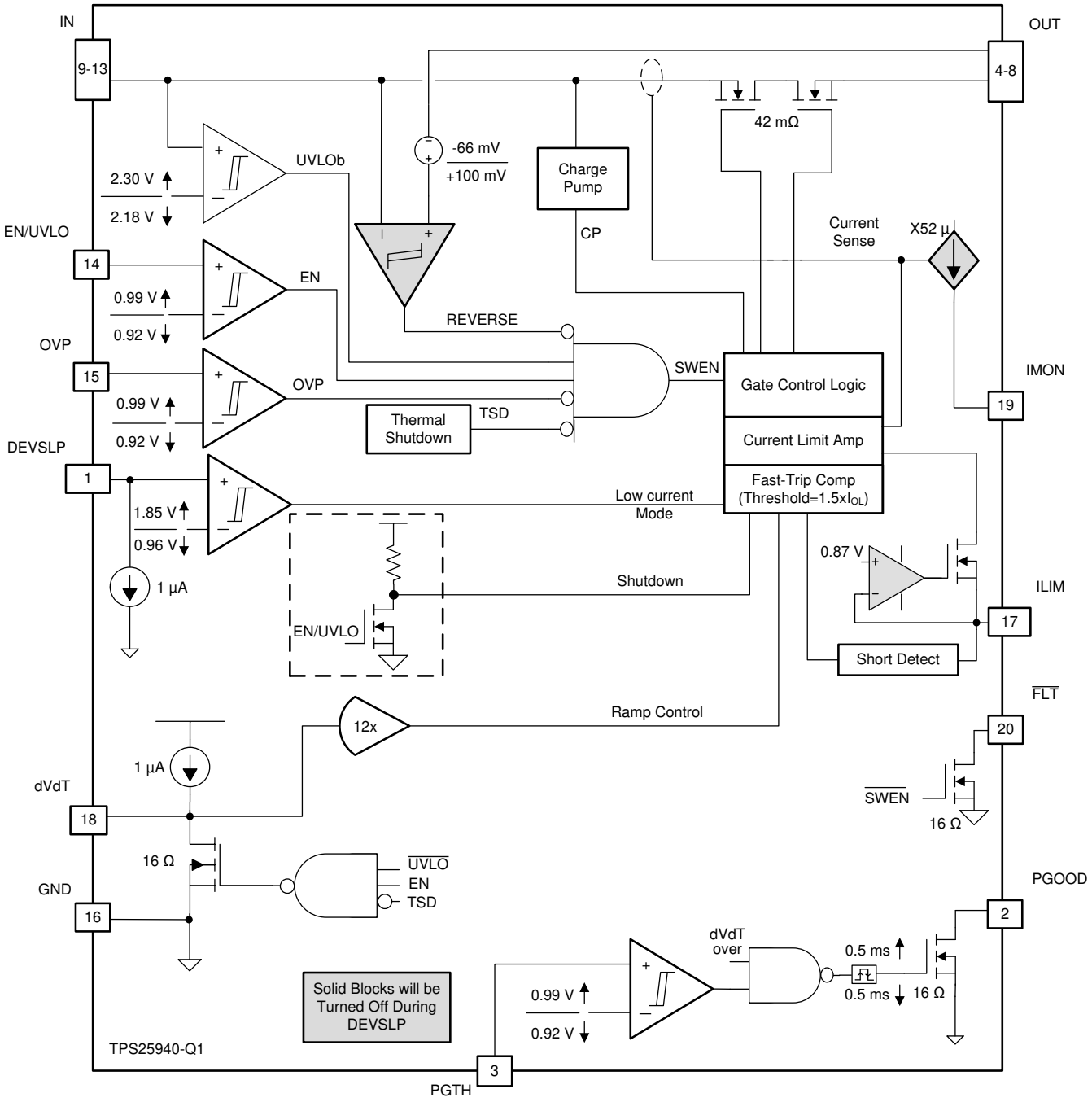
The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault for downstream system. Its overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip.

The device is designed to protect systems such as USB hubs against sudden output short to battery events. The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse blocking from output when output short to battery fault condition or input power fail condition is detected.

The additional features include:

- Precise current monitor output for health monitoring of the system
- Additional power good comparator with precision internal reference for output or any other rail voltage monitoring
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for brown-out and overvoltage faults
- A choice of latched or automatic restart mode

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Enable and Adjusting Undervoltage Lockout

The EN/UVLO pin controls the ON and OFF state of the internal FET. A voltage $V_{(EN/UVLO)} < V_{(ENF)}$ on this pin turns off the internal FET, thus disconnecting IN from OUT, while voltage below $V_{(SHUTF)}$ takes the device into shutdown mode, with $I_Q$ less than 15 µA to ensure minimal power loss. Cycling EN/UVLO low and then back high resets the TPS25940L-Q1 that has latched off due to a fault condition.

The internal de-glitch delay on EN/UVLO falling edge is kept low for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO terminal to GND.

The undervoltage lock out can be programmed by using an external resistor divider from supply IN terminal to EN/UVLO terminal to GND as shown in 图 9-1. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off, and $\overline{FLT}$ is asserted. If the Under-Voltage Lock-Out function is not needed, the EN/UVLO terminal must be connected to the IN terminal. EN/UVLO terminal must not be left floating.

The device also implements internal undervoltage-lockout (UVLO) circuitry on the IN terminal. The device disables when the IN terminal voltage falls below internal UVLO Threshold $V_{(UVF)}$. The internal UVLO threshold has a hysteresis of 115 mV.

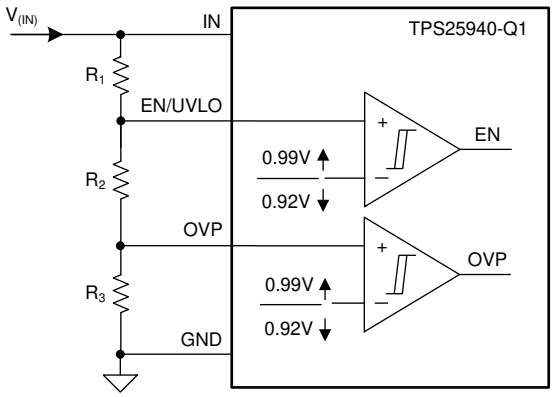



**图 9-1. UVLO and OVP Thresholds Set By $R_1$, $R_2$ and $R_3$**

### 9.3.2 Overvoltage Protection (OVP)

The device incorporates circuit to protect system during overvoltage conditions. A resistor divider connected from the supply to OVP terminal to GND (as shown in 图 9-1) programs the overvoltage threshold. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. This pin must be tied to GND when not used.

### 9.3.3 Hot Plug-In and In-Rush Current Control

The device is designed to control the in-rush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane’s supply voltage and prevents unintended resets of the system power. A slew rate controlled startup (dVdT) also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on (as shown in 图 9-2). Equation governing slew rate at start-up is shown in 方程式 1.

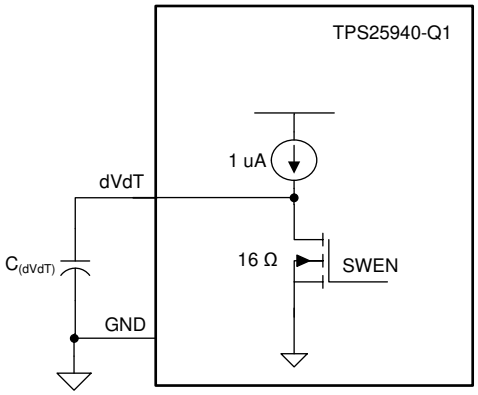



**图 9-2. Output Ramp Up Time $t_{dVdT}$ is Set by $C_{(dVdT)}$**

$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{GAIN_{(dVdT)}}\right) x \left(\frac{dV_{(OUT)}}{dt}\right) \quad (1)$$

where

- $I_{(dVdT)}$ = 1 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$ = Desired output slew rate
- $GAIN_{(dVdT)}$ = dVdT to OUT gain = 12

The total ramp time ($t_{dVdT}$) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using 方程式 2.

$$t_{dVdT} = 8.3 \times 10^4 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

The inrush current, $I_{(INRUSH)}$ can be calculated as shown in 方程式 3.

$$I_{(INRUSH)} = C_{(OUT)} \times V_{(IN)} / t_{dVdT}. \quad (3)$$

The dVdT pin can be left floating to obtain a predetermined slew rate ($t_{dVdT}$) on the output. When terminal is left floating, the device sets an internal ramp rate of 30 V/ms for output ($V_{(OUT)}$) ramp.

图 10-7 and 图 10-8 illustrate the inrush current control behavior of the device. For systems where load is present during start-up, the current never exceeds the overcurrent limit set by $R_{(ILIM)}$ resistor for the application. For defining appropriate charging time-rate under different load conditions, see the *Setting Output Voltage Ramp Time ($T_{dVdT}$)* section.

### 9.3.4 Overload and Short Circuit Protection

At all times load current is monitored by sensing voltage across an internal sense resistor. During overload events, current is limited to the current limit ($I_{(LIM)}$) programmed by $R_{(ILIM)}$ resistor as shown in 方程式 4.

$$I_{(LIM)} = \frac{89}{R_{(ILIM)}} \quad (4)$$

where

- $I_{(LIM)}$ is overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

The device incorporates two distinct levels: a current limit ($I_{(LIM)}$) and a fast-trip threshold ($I_{(FASTRIP)}$). Fast trip and current limit operation are shown in 图 9-3.

Bias current on ILIM pin directly controls current-limiting behavior of the device, and PCB routing of this node must be kept away from any noisy (switching) signals.

#### 9.3.4.1 Overload Protection

For overload conditions, the internal current-limit amplifier regulates the output current to $I_{(LIM)}$. The output voltage droops during the current regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold ($T_{(TSD)}$), the internal FET is turned off. When in thermal shutdown, the TPS25940L-Q1 version stays latched off, whereas the TPS25940-Q1/TPS259401A-Q1 versions commence an auto-retry cycle 128 ms after $T_J < [T_{(TSD)} - 12°C]$. During thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition. 图 10-11 and 图 10-12 illustrate overload behavior.

#### 9.3.4.2 Short Circuit Protection

During a transient short circuit event, the current through the device increases very rapidly. As current-limit amplifier cannot respond quickly to this event because of its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. This comparator shuts down the pass device within 1µs, when the current through internal FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), and terminates the rapid short-circuit peak current. The trip threshold is set to more than 50% of the programmed overload current limit ( $I_{(FASTRIP)} = 1.5 \times I_{(LIM)} + 0.375$ ). The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(LIM)}$. Then, device behaves similar to overload condition. 图 10-13 through 图 10-14 illustrate the behavior of the system when the current exceeds the fast-trip threshold.

#### 9.3.4.3 Start-Up with Short on Output

During start-up into a short circuit current is limited to $I_{(LIM)}$. 图 9-3 and 图 10-15 illustrate start-up with a short on the output. This feature helps in quick fault isolation and hence ensures stability of the DC bus.

#### 9.3.4.4 Constant Current Limit Behavior During Overcurrent Faults

When power dissipation in the internal FET [$P_D = (V_{(IN)} - V_{(OUT)}) \times I_{(OUT)}$] > 10 W, there is approximately 0% to 5% thermal fold back in the current limit value so that $I_{(LIM)}$ drops to $I_{OS}$. Eventually, the device shuts down because of over temperature.

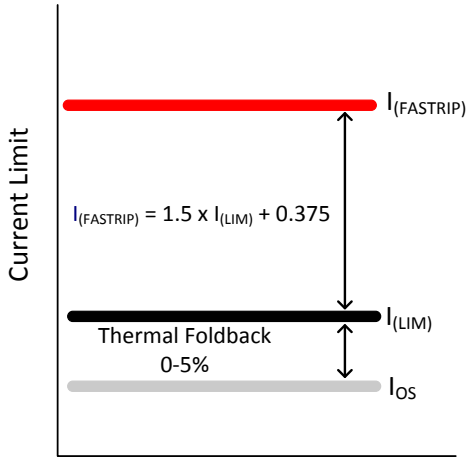



**图 9-3. Fast-Trip Current**

### 9.3.5 FAULT Response

The $\overline{FLT}$ open-drain output is asserted (active low) during undervoltage, overvoltage, reverse voltage-current and thermal shutdown conditions. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. The device is designed to eliminate false fault reporting by using an internal "de-glitch" circuit for undervoltage and overvoltage (2.2-µs typical) conditions without the need for external circuitry. This ensures that fault is not accidentally asserted during transients on input bus.

Connect $\overline{FLT}$ with a pull up resistor to Input or Output voltage rail. $\overline{FLT}$ may be left open or tied to ground when not used. $V_{(IN)}$ falling below $V_{(UVF)}$ = 2.1 V resets $\overline{FLT}$.

### 9.3.6 Current Monitoring

The current source at IMON terminal is configured to be proportional to the current flowing from IN to OUT. This current can be converted to a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. This voltage, computed using 方程式 6, can be used as a means of monitoring current flow through the system.

The maximum voltage range for monitoring the current ($V_{(IMONmax)}$) is limited to minimum([$V_{(IN)}$ – 2.2 V], 6 V) to ensure linear output. This puts limitation on maximum value of $R_{(IMON)}$ resistor and is determined by 方程式 5.

$$R_{(IMONmax)} = \frac{\text{minimum } (V_{(IN)} - 2.2,\ 6)}{1.6 \times I_{(LIM)} \times GAIN_{(IMON)}} \tag{5}$$

The output voltage at IMON terminal is calculated from 方程式 6.

$$V_{(IMON)} = \left[ I_{(OUT)} \times GAIN_{(IMON)} + I_{(IMON\_OS)} \right] \times R_{(IMON)} \tag{6}$$

where

- $GAIN_{(IMON)}$ = Gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 52 µA/A
- $I_{(OUT)}$ = Load current
- $I_{(IMON\_OS)}$ = 0.8 µA (typical)

This pin must not have a bypass capacitor to avoid delay in the current monitoring information.

The voltage at IMON pin can be digitized using an ADC (such as ADS1100, SBAS239) to read the current monitor information over an $I^2C$ bus.

### 9.3.7 Power Good Comparator

The device incorporates a Power Good comparator for co-ordination of status to downstream DC-DC converters or system monitoring circuits. The comparator has an internal reference of $V_{(PGTHR)}$ = 0.99 V at negative terminal and positive terminal PGTH can be utilized for monitoring of either input or output of the device. The comparator output PGOOD is an open-drain active high signal, which can be used to indicate the status to downstream units. PGOOD is asserted high when internal FET is fully enhanced and PGTH pin voltage is higher than internal reference $V_{(PGTHR)}$.

The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by downstream converters. Rising de-glitch delay is determined by 方程式 7.

$$t_{PGOOD(degl)} = \text{Maximum}\{(3.5 \times 10^6 \times C_{(dVdT)}),\ t_{PGOODR}\} \tag{7}$$

Connect the PGOOD pin with a pull up resistor to Input or Output voltage rail. PGOOD may be left open or tied to ground when not used.

### 9.3.8 IN, OUT and GND Pins

The device has multiple pins for input (IN) and output (OUT).

All IN pins must be connected together and to the power source. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 2.7 V – 18 V.

Similarly all OUT pins must be connected together and to the load. $V_{(OUT)}$ in the ON condition, is calculated using 方程式 8.

$$V_{(OUT)} = V_{(IN)} - (R_{ON} \times I_{(OUT)}) \tag{8}$$

where, $R_{ON}$ is the total ON resistance of the internal FET.

GND terminal is the most negative voltage in the circuit and is used as a reference for all voltage reference unless otherwise specified.

### 9.3.9 Thermal Shutdown

Internal over temperature shutdown disables turns off the FET when $T_J$ > 160°C (typical). The TPS25940L-Q1 version stays latched off, whereas TPS25940-Q1/TPS259401A-Q1 versions commence an auto-retry cycle 128 ms after $T_J$ drops below [$T_{(TSD)}$ – 12°C]. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition.

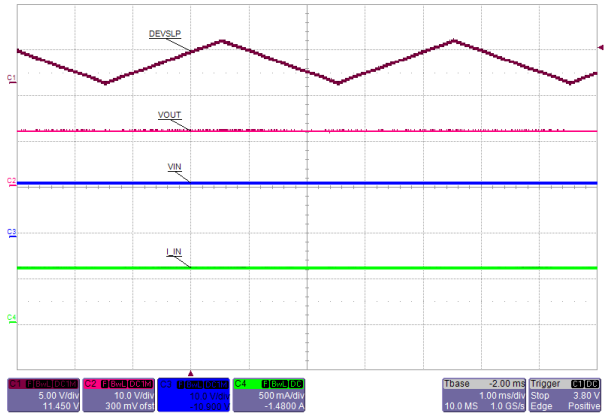
## 9.4 Device Functional Modes

### 9.4.1 DevSleep Mode

The TPS25940xx-Q1 device provides a dedicated DevSleep interface terminal (DEVSLP) to drive the device in low power mode. When pulled high, it puts the device in low power DevSleep mode. In this mode, the quiescent current consumption of the device is limited to less than 130 µA (95-µA typical). During this mode, the output voltage remains active, the overload current limit is set to $I_{(DEVSLP(LIM))}$ and functionality of reverse comparator and current monitoring is disabled. All other protections are kept active ensuring the safety of the system even in DevSleep mode.

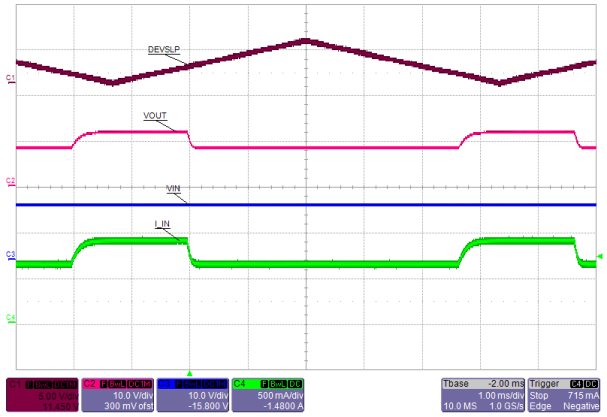
User must ensure that load currents on the bus are limited to less than $I_{(DEVSLP(LIM))}$, when the device is driven to DevSleep mode. Also, while coming out of DevSleep, it is important to sequence the TPS25940xx-Q1 earlier than the load. Otherwise, the load can exceed $I_{(DEVSLP(LIM))}$ and cause the TPS25940xx-Q1 to enter the overload mode.

IN and OUT of DevSleep Mode with 550-mA Load through TPS25940-Q1/TPS259401A-Q1 Hot Short and Retry in DevSleep Mode illustrate the behavior of the system in DevSleep mode.



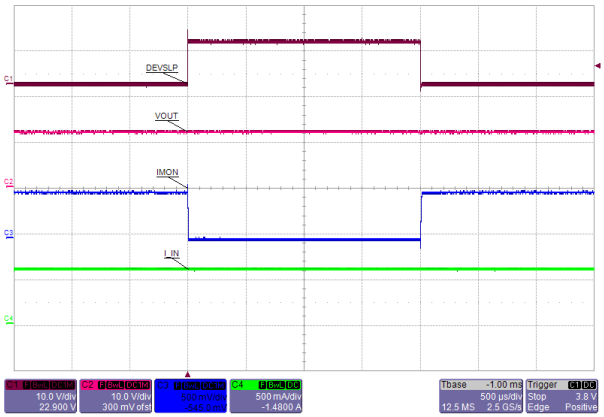

$V_{(IN)}$ = 12 V  $I_{(LIM)}$ = 5.3 A  $R_L$ = 22 Ω
$C_{(OUT)}$ = 1 µF

**图 9-4. IN and OUT of DevSleep Mode with 550-mA Load**



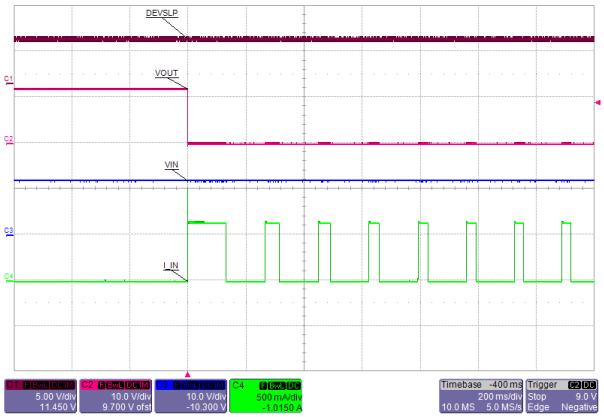

$V_{(IN)}$ = 12 V  $I_{(LIM)}$ = 5.3 A  $R_L$ = 15 Ω
$C_{(OUT)}$ = 1 µF

**图 9-5. IN and OUT of DevSleep Mode with 800-mA Load. In DevSleep, Load Current Gets Limited to $I_{(DEVSLP(LIM))}$**




$R_L$ = 22 Ω $I_{(LIM)}$ = 5.3 A $C_{(OUT)}$ = 1 µF

**图 9-6. IMON Disabled in DevSleep Mode**




$I_{(LIM\ -\ )}$ = 5.3 A $C_{(OUT)}$ = 1 µF

**图 9-7. TPS25940-Q1/TPS259401A-Q1 Hot Short and Retry in DevSleep Mode**

### 9.4.2 Shutdown Control

The internal FET and hence the load current can be remotely switched off by taking the UVLO pin below its 0.6-V threshold with an open collector or open drain device as shown in 图 9-8. The device quiescent current is reduced to less than 20 µA in this state. Upon releasing the UVLO pin the device turns on with soft-start cycle.

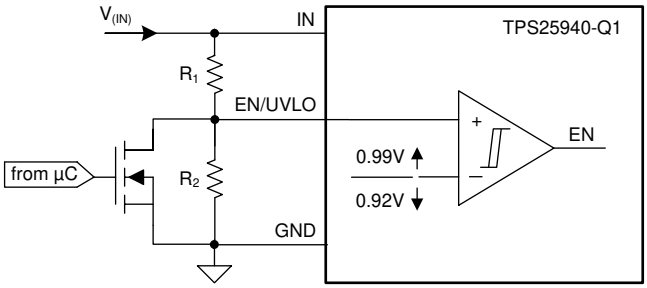



**图 9-8. Shutdown Control**

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

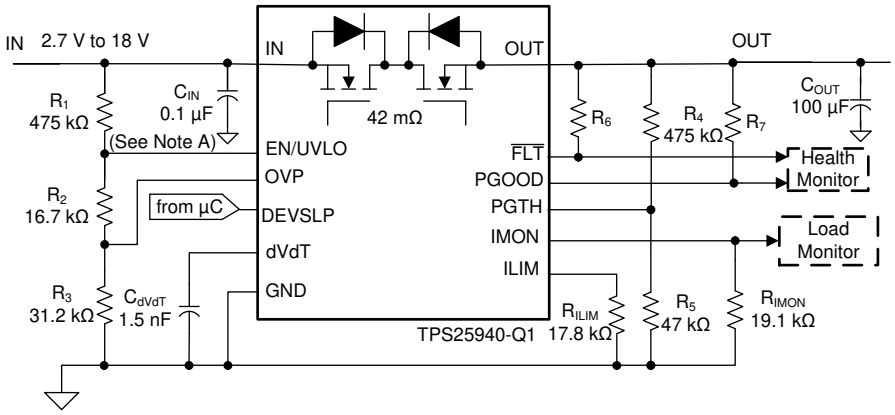
## 10.1 Application Information

The TPS25940xx-Q1 device is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 2.7 V to 18 V with programmable current limit, overvoltage and undervoltage protection. The device aids in controlling the in-rush current and provides fast turn-off during reverse voltage conditions for systems such as USB ports prone to Short-to-Battery faults, Servers, Power Back-up Storage units and RAID cards. The device also provides robust protection for multiple faults on the sub-system rail.

The *Detailed Design Procedure* section can be used to select component values for the device.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS25940 Design Calculator* is available on web folder.

## 10.2 Typical Application




A. $C_{IN}$: Optional and only for noise suppression.

**图 10-1. Typical Application Schematic**

### 10.2.1 Design Requirements

表 10-1 lists the Design Parameters.

**表 10-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage, $V_{(IN)}$ | 12 V |
| Undervoltage lockout set point, $V_{(UV)}$ | 10.8 V |
| Overvoltage protection set point, $V_{(LIM)}$ | 16.5 V |
| Load at Start-Up, $R_{L(SU)}$ | 4.8 Ω |
| Current limit, $I_{(LIM)}$ | 5 A |
| Load capacitance, $C_{(OUT)}$ | 100 µF |
| Maximum ambient temperatures, $T_A$ | 85°C |

### 10.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25940xx-Q1.

#### *10.2.2.1 Step by Step Design Procedure*

To begin the design process a few parameters must be decided upon. The designer must know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

#### *10.2.2.2 Programming the Current-Limit Threshold: $R_{(ILIM)}$ Selection*

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using 方程式 9.

$$R_{(ILIM)} = \frac{89}{5} = 17.8k\Omega \tag{9}$$

Choose closest standard value: 17.8-k, 1% standard value resistor.

#### *10.2.2.3 Undervoltage Lockout and Overvoltage Set Point*

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using the external voltage divider network of $R_1$, $R_2$ and $R_3$ as connected between IN, EN, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated solving 方程式 10 and 方程式 11.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \tag{10}$$

$$V_{(ENR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \tag{11}$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)}/(R_1 + R_2 + R_3)$}, it is recommended to use higher values of resistance for $R_1$, $R_2$ and $R_3$.

However, leakage currents because of the external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R123)}$ must be chosen to be 20 times greater than the leakage current expected.

From the device electrical specifications, $V_{(OVPR)}$ = 0.99 V and $V_{(ENR)}$ = 0.99 V. For design requirements, $V_{(OV)}$ is 16.5 V and $V_{(UV)}$ is 10.8 V. To solve the equation, first choose the value of $R_3$ = 31.2 kΩ and use 方程式 10 to solve for ($R_1$ + $R_2$) = 488.8 kΩ. Use 方程式 11 and value of ($R_1$ + $R_2$) to solve for $R_2$ = 16.47 kΩ and finally $R_1$= 472.33 kΩ.

Using the closest standard 1% resistor values gives $R_1$ = 475 kΩ, $R_2$ = 16.7 kΩ, and $R_3$ = 31.2 kΩ.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 7% lower than the rising threshold, $V_{(UV)}$. This is calculated using 方程式 12.

$$V_{(PFAIL)} = 0.93 \times V_{(UV)} \quad (12)$$

#### 10.2.2.4 Programming Current Monitoring Resistor—$R_{IMON}$

Voltage at IMON pin $V_{(IMON)}$ represents the voltage proportional to load current. This can be connected to an ADC of the downstream system for health monitoring of the system. The $R_{(IMON)}$ need to be configured based on the maximum input voltage range of the ADC used. $R_{(IMON)}$ is set using 方程式 13.

$$R_{(IMON)} = \frac{V_{(IMONmax)}}{I_{(LIM)} \times 52 \times 10^{-6}} \ k\Omega \quad (13)$$

For $I_{(LIM)}$ = 5 A, and considering the operating range of ADC from 0 V to 5 V, $V_{(IMONmax)}$ is 5 V and $R_{(IMON)}$ is determined by:

$$R_{(IMON)} = \frac{5}{5 \times 52 \times 10^{-6}} = 19.23 \ k\Omega \quad (14)$$

Selecting $R_{(IMON)}$ value less than determined by 方程式 14 ensures that ADC limits are not exceeded for maximum value of load current.

If the IMON pin voltage is not being digitized with an ADC, $R_{(IMON)}$ can be selected to produce a 1V/1A voltage at the IMON pin, using 方程式 13.

Choose closest 1 % standard value: 19.1 kΩ.

If current monitoring up to $I_{(FASTRIP)}$ is desired, $R_{(IMON)}$ can be reduced by a factor of 1.6, as in 方程式 5.

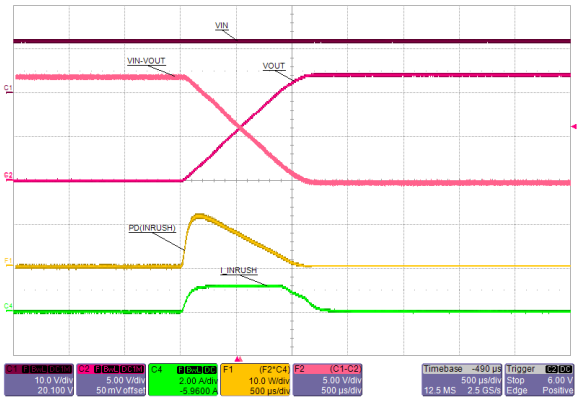
#### 10.2.2.5 Setting Output Voltage Ramp Time ($t_{dVdT}$)

For a successful design, the junction temperature of device must be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor $C_{(dVdT)}$ needed is calculated considering the two possible cases *Case 1: Start-up Without Load: Only Output Capacitance C(OUT) Draws Current During Start-up* and *Case 2: Start-Up With Load: Output Capacitance C(OUT) and Load Draws Current During Start-Up*.

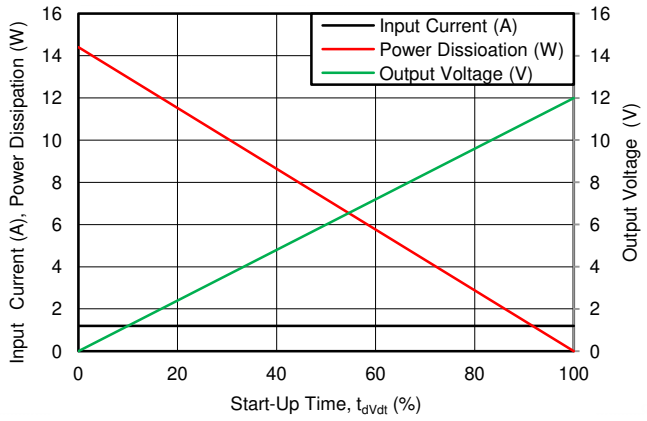
##### 10.2.2.5.1 Case1: Start-Up Without Load: Only Output Capacitance $C_{(OUT)}$ Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipated decreases as well. Typical ramp-up of output voltage $V_{(OUT)}$ with inrush current limit of 1.2 A and power dissipated in the device during start-up is shown in Start-Up Without Load. The average power dissipated in the device during start-up is equal to area of triangular plot (red curve in Start-Up Without Load) averaged over $t_{dVdT}$.




$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $C_{(OUT)}$=100 µF

**图 10-2. Start-Up Without Load**




$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $C_{(OUT)}$=100 µF

**图 10-3. $P_{D(INRUSH)}$ Due to Inrush Current**

For the TPS25940-Q1 device, the inrush current is determined as shown in 方程式 15.

$$I = C \times \frac{dV}{dT} \Rightarrow I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (15)$$

Power dissipation during start-up is given by 方程式 16.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (16)$$

方程式 16 assumes that load does not draw any current until the output voltage has reached its final value.

#### 10.2.2.5.2 Case 2: Start-Up With Load: Output Capacitance $C_{(OUT)}$ and Load Draws Current During Start-Up

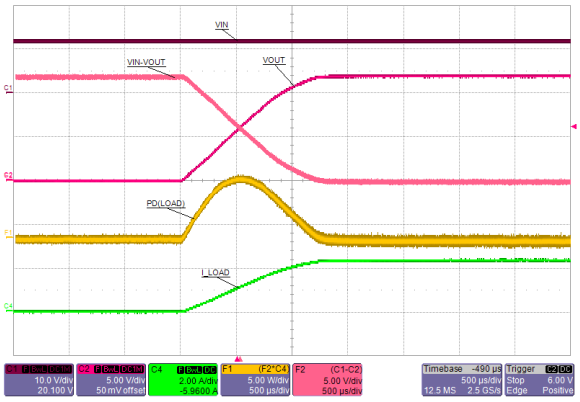
When load draws current during the turn-on sequence, there is additional power dissipated. Considering a resistive load $R_{L(SU)}$ during start-up, load current ramps up proportionally with increase in output voltage during $t_{dVdT}$ time. Typical ramp-up of output voltage, Load current and power dissipation in the device is shown in Start-Up With Load and power dissipation with respect to time is plotted in $P_{D(LOAD)}$ in Load During Start-Up. The additional power dissipation during start-up phase is calculated as shown in 方程式 17 and 方程式 18.

$$(V_I - V_O)(t) = V_{(IN)} \times \left(1 - \frac{t}{t_{dVdT}}\right) \quad (17)$$

$$I_L(t) = \left(\frac{V_{(IN)}}{R_{L(SU)}}\right) \times \frac{t}{t_{dVdT}} \quad (18)$$

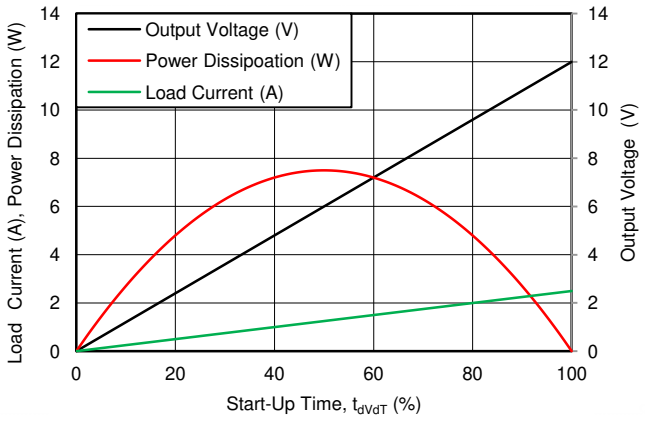
Where $R_{L(SU)}$ is the load resistance present during start-up. Average energy loss in the internal FET during charging time due to resistive load is given by 方程式 19.

$$W_t = \int_0^{tdVdT} V_{(IN)} \times \left(1 - \frac{t}{t_{dVdT}}\right) \times \left(\frac{V_{(IN)}}{R_{L(SU)}} \times \frac{t}{t_{dVdT}}\right) dt \quad (19)$$




$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $R_{L(SU)}$ = 4.8 Ω

**图 10-4. Start-Up With Load**




$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $R_{L(SU)}$ = 4.8 Ω

**图 10-5. $P_{D(LOAD)}$ in Load During Start-Up**

On solving 方程式 19 the average power loss in the internal FET due to load is shown in 方程式 20.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (20)$$

Total power dissipated in the device during startup is shown is 方程式 21.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (21)$$

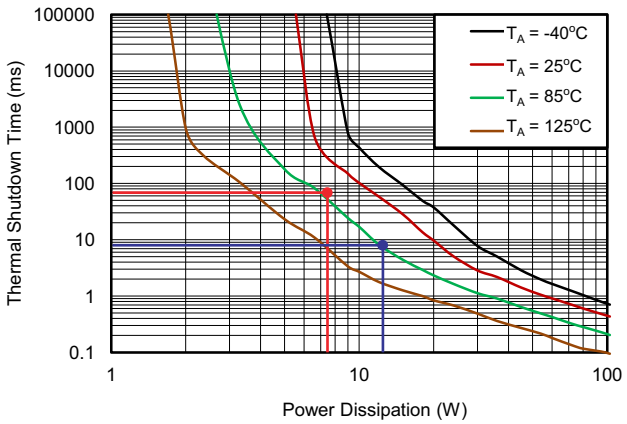
Total current during startup is given by 方程式 22.

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (22)$$

If $I_{(STARTUP)} > I_{(LIM)}$, the device limits the current to $I_{(LIM)}$ and the current limited charging time is determined by 方程式 23.

$$t_{dVdT(current\ limited)} = C_{(OUT)} \times \frac{V_{(IN)}}{I_{(LIM)}} \quad (23)$$

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in Thermal Shutdown Limit Plot.




Taken on 2-Layer board, 2oz.(0.08-mm thick) with GND plane area: 14 $cm^2$ (Top) and 20 $cm^2$ (bottom)

**图 10-6. Thermal Shutdown Limit Plot**

For the design example under discussion,

Select ramp-up capacitor $C_{(dVdT)}$ = 1nF, using 方程式 24.

$$t_{dvdt} = 8.3 \times 10^{4} \times 12 \times 1 \times 10^{-9} = 0.996\text{ms} = \sim 1\text{ms} \quad (24)$$

The inrush current drawn by the load capacitance ($C_{(OUT)}$) during ramp-up using 方程式 25.

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{1 \times 10^{-3}}\right) = 1.2\text{ A} \quad (25)$$

The inrush Power dissipation is calculated, using 方程式 26.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 1.2 = 7.2\text{ W} \quad (26)$$

For 7.2 W of power loss, the thermal shut down time of the device must not be less than the ramp-up time $t_{dVdT}$ to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Thermal Shutdown Limit Plot at $T_A$ = 85°C, for 7.2 W of power the shutdown time is approximately 60 ms. So it is safe to use 1 ms as start-up time without any load on output.

Considering the start-up with load 4.8 Ω, the additional power dissipation, when load is present during start up is calculated, using 方程式 27.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{12 \times 12}{4.8} = 5\text{ W} \quad (27)$$

The total device power dissipation during start up is given by 方程式 28.

$$P_{D(STARTUP)} = (7.2 + 5) = 12.2\text{ W} \quad (28)$$

From thermal shutdown limit graph at $T_A$ = 85°C, the thermal shutdown time for 12.2 W is close to 7.5 ms. It is safe to have 30% margin to allow for variation of system parameters such as load, component tolerance, and input voltage. So it is well within acceptable limits to use the 1 nF capacitor with start-up load of 4.8 Ω.

If there is a need to decrease the power loss during start-up, it can be done with increase of $C_{(dVdT)}$ capacitor.

To illustrate, choose $C_{(dVdT)}$ = 1.5 nF as an option and recalculate:

$$t_{dvdt} = 1.5\text{ms} \quad (29)$$

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{1.5 \times 10^{-3}}\right) = 0.8\ A \quad (30)$$

$$P_{D(INRUSH)} = 0.5 \times 12x\ 0.8 = 4.8\ W \quad (31)$$

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \left(\frac{12 \times 12}{4.8}\right) = 5\ W \quad (32)$$

$$P_{D(STARTUP)} = 4.8 + 5 = 9.8\ W \quad (33)$$

From thermal shutdown limit graph at $T_A$ = 85°C, the shutdown time for 10-W power dissipation is approximately 17 ms, which increases the margins further for shutdown time and ensures successful operation during start up and steady state conditions.

The spreadsheet tool available on the web can be used for iterative calculations.

#### *10.2.2.6 Programing the Power Good Set Point*

As shown in 图 10-1, $R_4$ and $R_5$ sets the required limit for PGOOD signal as needed for the downstream converters. Considering a power good threshold of 11 V for this design, the values of $R_4$ and $R_5$ are calculated using 方程式 34.

$$V_{(PGTH)} = 0.99 \times \left(1 + \frac{R_4}{R_5}\right) \quad (34)$$

It is recommended to have high values for these resistors to limit the current drawn from the output node. Choosing a value of $R_4$ = 475 kΩ, $R_5$ = 47 kΩ provides $V_{(PGTH)}$ = 11 V.

#### *10.2.2.7 Support Component Selections—$R_6$, $R_7$ and $C_{IN}$*

Reference to application schematics, $R_6$ and $R_7$ are required only if PGOOD and $\overline{FLT}$ are used; these resistors serve as pull-ups for the open-drain output drivers. The current sunk by each of these pins must not exceed 10 mA (refer to the *Absolute Maximum Ratings* table). $C_{IN}$ is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for $C_{(IN)}$.

### 10.2.3 Application Curves

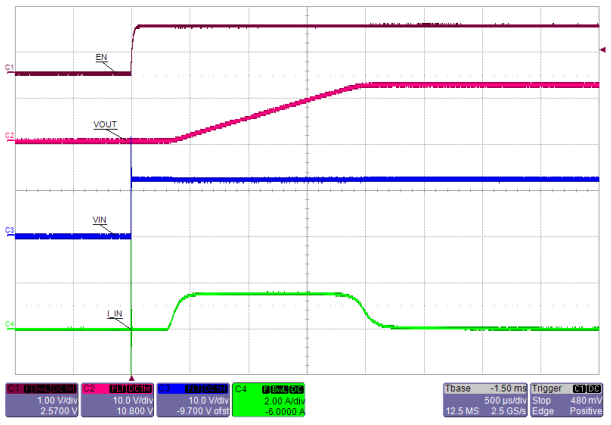



图 10-7. Hot-Plug Start-Up: Output Ramp Without Load on Output

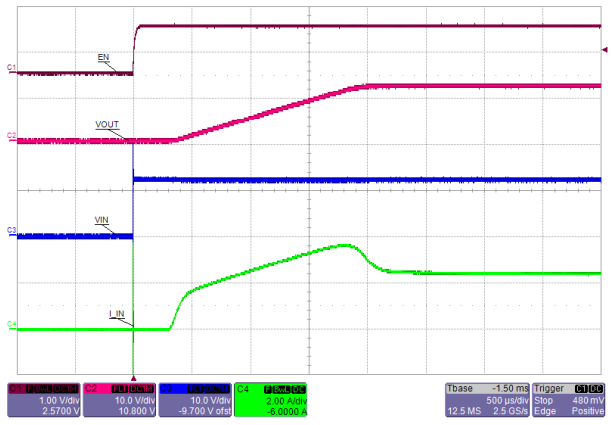



图 10-8. Hot-Plug Start-Up: Output Ramp With Start-Up Load of 4.8 Ω

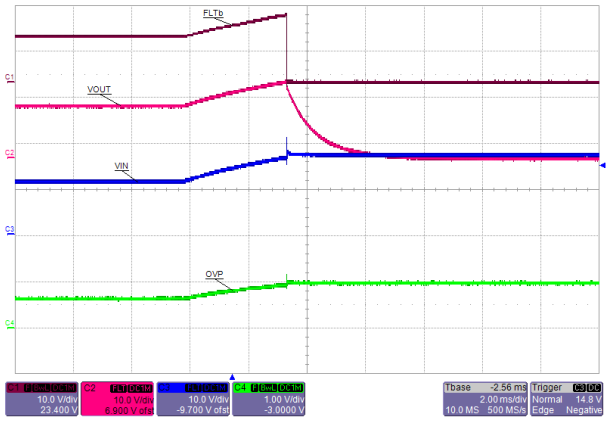



图 10-9. Overvoltage Shutdown

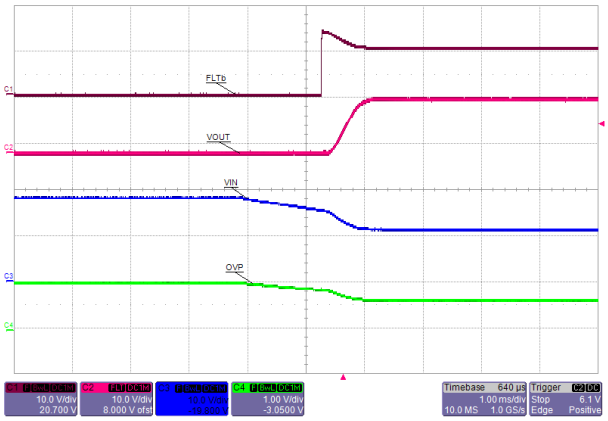



图 10-10. Overvoltage Recovery

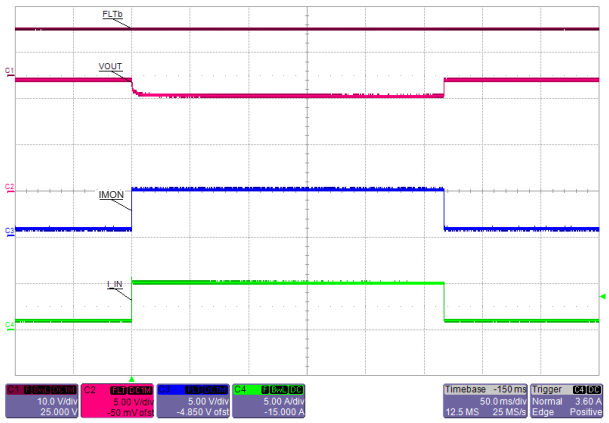



图 10-11. Over Load: Step Change in Load from 12 Ω to 2 Ω and Back

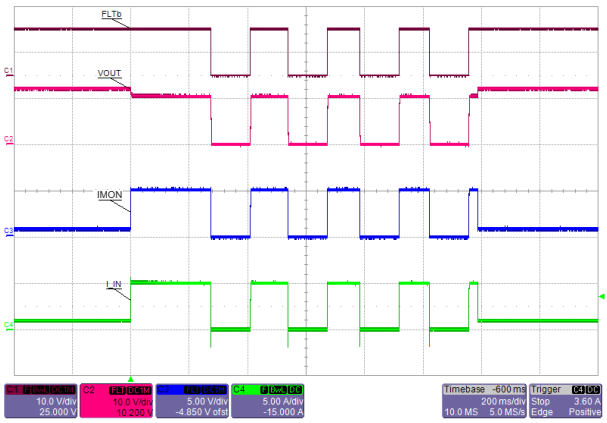



图 10-12. Overload Condition: Auto Retry and Recovery - TPS25940-Q1

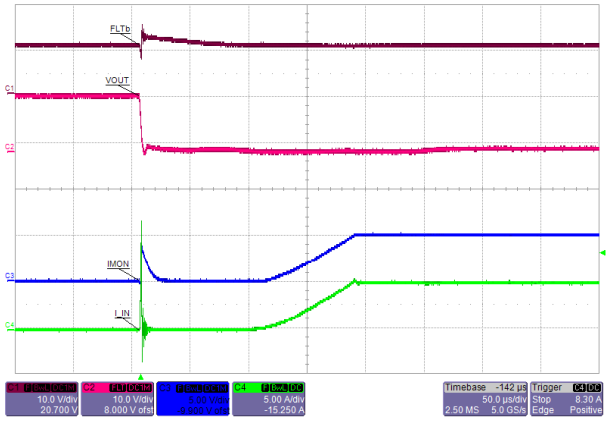



图 10-13. Hot Short: Fast Trip and Current Regulation

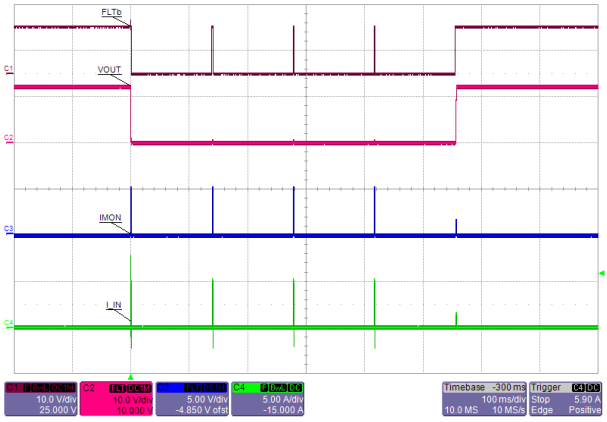



图 10-14. Hot Short: Auto-Retry and Recovery from Short Circuit - TPS25940-Q1

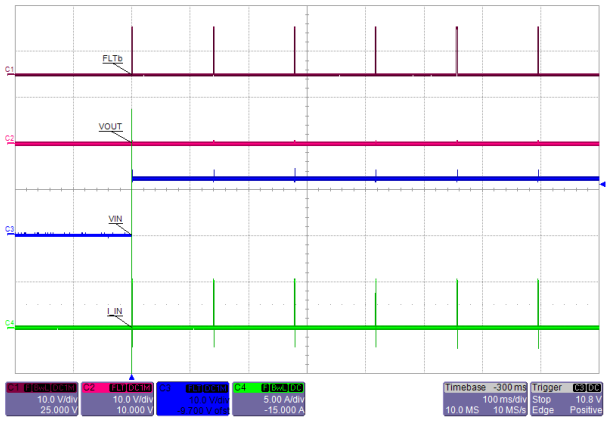



图 10-15. Hot Plug-In with Short on Output: Auto-Retry - TPS25940-Q1

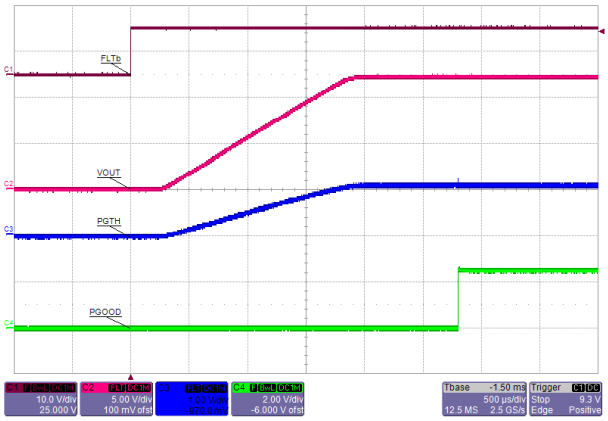



图 10-16. Power Good Response During Turn-ON

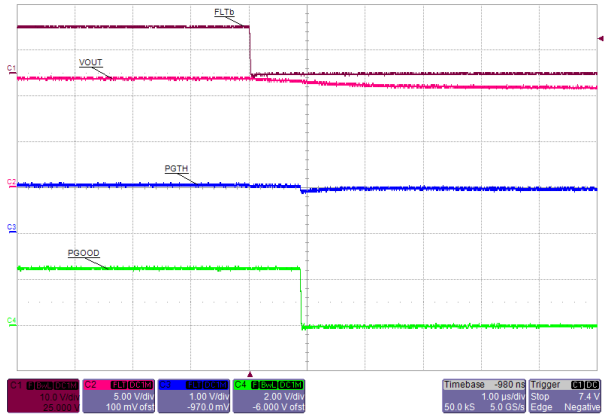



图 10-17. Power Good Response During Turn-OFF

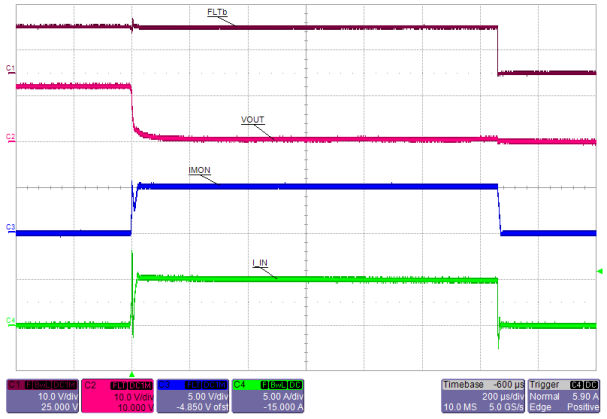



图 10-18. Hot Short: Latched - TPS25940L-Q1

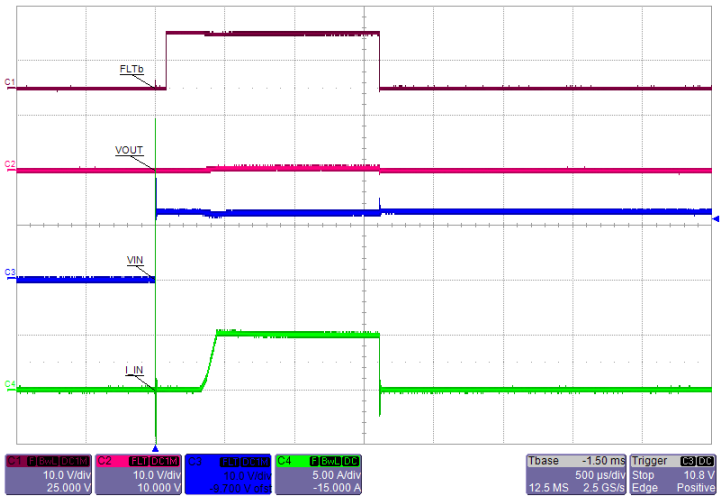



图 10-19. Hot Plug-in with Short on Output: Latched - TPS25940L-Q1

### 10.2.4 System Examples

#### *10.2.4.1 $V_{BUS}$ Short-to-Battery, Short-to-Ground Protection of USB Port in Automotive Systems*

The TPS25940xx-Q1 eFuse offers robust protection for the 5-V Power rail of USB ports under faults conditions like Short-to-Ground, Short-to-Battery and Overload.

5-V Power rail gets disconnected from the output within approximately 200 nsec during short circuit to Ground fault.

The eFuse monitors the reverse voltage from IN to OUT and when it exceeds – 66 mV, it stops the flow of reverse current. This operation protects the 5-V power rail from Short-to-Battery faults.

Typical application schematic of TPS25940xx-Q1 usage in USB port protection for automotive application is shown in 图 10-20.

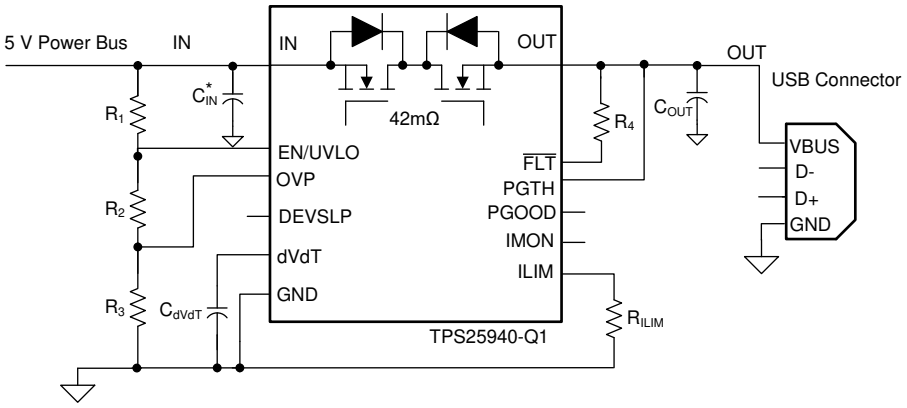



**图 10-20. Automotive USB Hub-Port – $V_{BUS}$ Short to Battery, $V_{BUS}$ Short to GND Protection**

图 10-21 and 图 10-22 show the performance of TPS25940-Q1 under Short-to-Battery and Short-to-Ground faults.

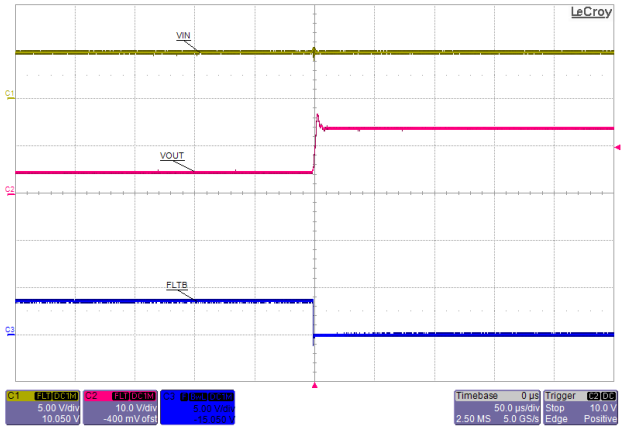



**图 10-21. $V_{BUS}$ Short-to-Battery Protection**

$V_{(IN)}$ = 5 V $C_{(OUT)}$ = 4.7 µF

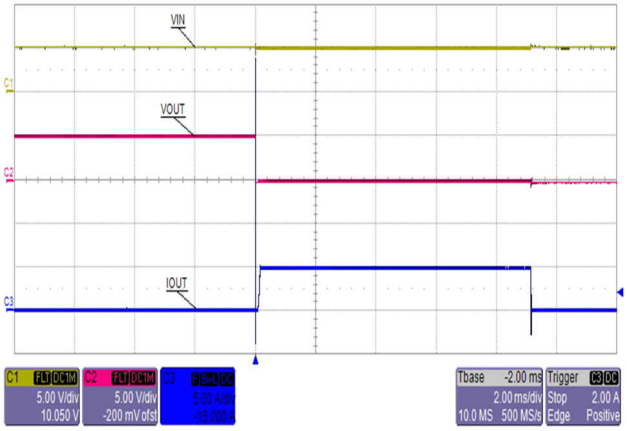


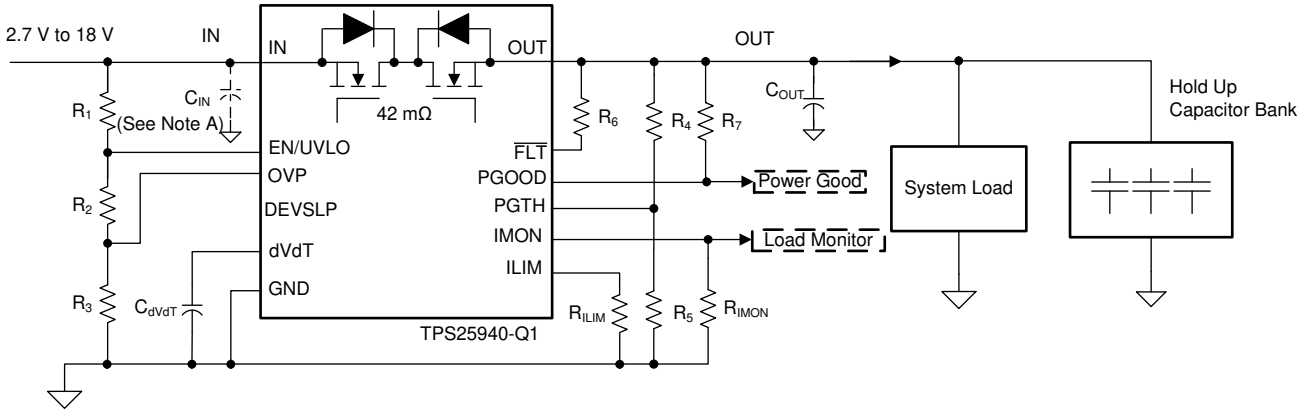

**图 10-22. $V_{BUS}$ Short-to-Ground Protection**

### *10.2.4.2 Power Failure Protection for Holdup Power*

For certain applications, it is necessary to have hold-up circuit and capacitor bank to ensure that critical user data is never lost during power-failure to the drive. The power-failure event could be because of the momentary loss of power regulation (transient brown-out condition) or because of the loss of power when system is hot-plugged out.

The TPS25940xx-Q1 device continuously monitors the supply voltage at EN/UVLO pin and swiftly disconnects the input bus from output when the voltage drops below a predefined threshold (power fail detection). Reverse current flow from output side to input supply gets blocked when reverse voltage from IN to OUT exceeds –66 mV. In addition, it provides an instant warning signal ( $\overline{FLT}$) to the controller. Its swift true reverse blocking feature reacts in 1 µs (typical) ensuring that the capacitor bank charge is retained. This helps the drive to have power for longer time to harden data and reduces the capacitance required in the hold-up bank, saving system cost.

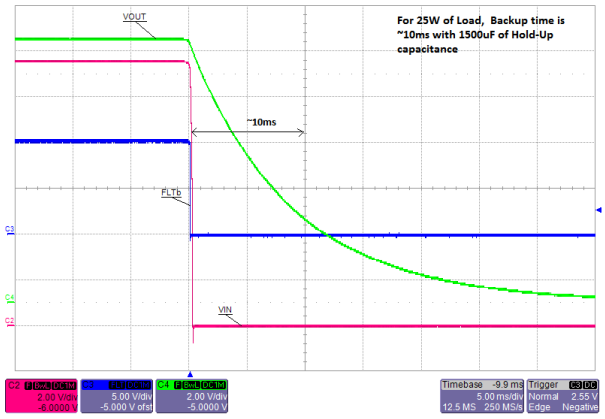
The typical application diagram of TPS25940xx-Q1 usage for holdup power is shown in 图 10-23.




A. $C_{IN}$: Optional and only for noise suppression.

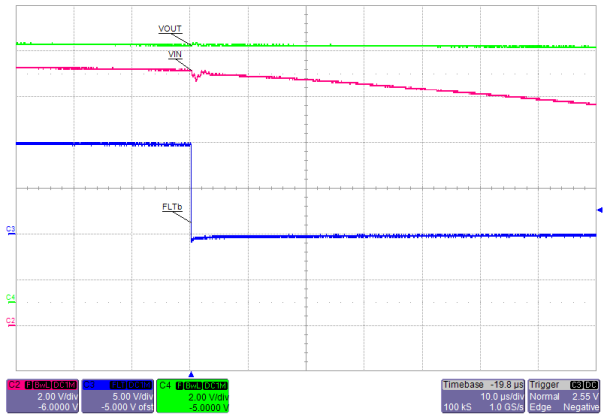
**图 10-23. Holdup Capacitor Implementation Using TPS25940xx-Q1**

The oscilloscope plots demonstrating the true reverse blocking, fast turn-off and $\overline{FLT}$ signal delay are shown in Hot-Plug Out Condition through Standard Power Shutdown or Brownout Conditions.



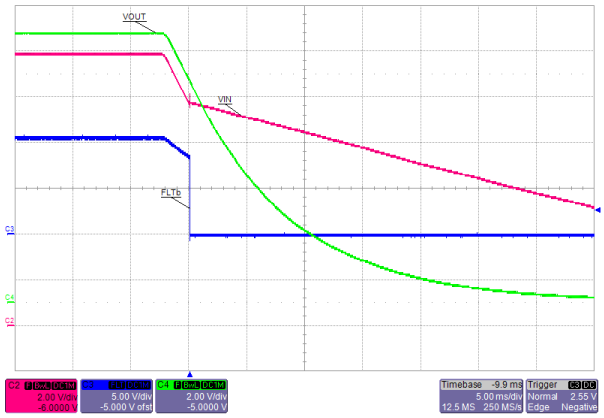

$V_{(IN)}$ = 12 V $C_{(OUT)}$ = 1500 µF $R_L$ = 5.6 Ω

**图 10-24. Hot-Plug Out Condition**




$V_{(IN)}$ = 12 V $C_{(OUT)}$ = 1500 µF $R_L$ = 5.6 Ω

**图 10-25. Hot-Plug Out Condition: $\overline{FLT}$ Delay**




$V_{(IN)}$ = 12 V $C_{(OUT)}$ = 1500 µF $R_L$ = 5.6 Ω

**图 10-26. Standard Power Shutdown or Brownout Conditions**

### *10.2.4.3 Overload Detection Using TPS25940xx-Q1*

The TPS25940xx-Q1 device has enhanced features such as load current monitoring output IMON and an integrated power good comparator for voltage monitoring. These two functional blocks can be utilized as per circuit configuration shown in 图 10-27, to FLAG the overload event.

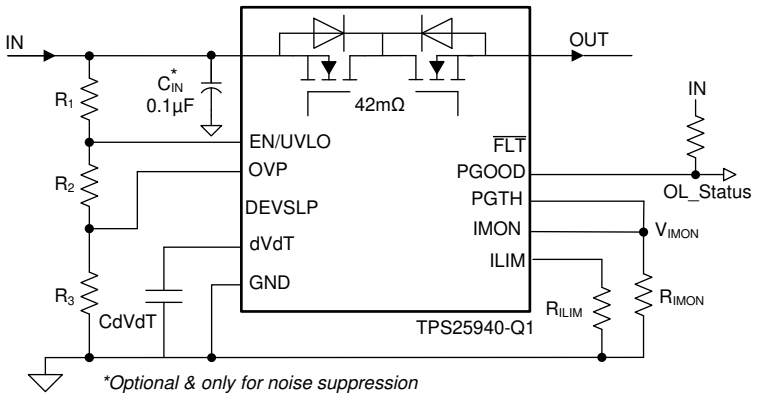



**图 10-27. Circuit Configuration for Overload Detection Using TPS25940xx-Q1**

The output voltage at IMON terminal $V_{IMON}$ can be used as a means of monitoring current flow through the system and its value can be calculated from 方程式 6.

The power good comparator of TPS25940xx-Q1 has an internal reference of $V_{PGTHR}$ = 0.99 V at the negative terminal and the positive terminal PGTH can be utilized for monitoring voltage of any specific rail. As shown in the 图 10-27, the output voltage at IMON terminal ($V_{IMON}$) is fed to the positive terminal PGTH ($V_{PGTH}$) of the comparator. When the PGTH pin voltage ($V_{PGTH}$ = $V_{IMON}$) is higher than the internal reference $V_{PGTHR}$, the open-drain comparator output PGOOD asserts HIGH to indicate overload event.

For example, to detect overcurrent event at load current $I_{OUT}$ of 300 mA, the value of $R_{IMON}$ can be calculated using 方程式 35.

$$V_{IMON} = V_{PGTHR} = \left(I_{OUT} \times GAIN_{IMON} + I_{IMON\_OS}\right) \times R_{IMON} \tag{35}$$

$$R_{IMON} = \frac{V_{PGTHR}}{\left(I_{OUT} \times GAIN_{IMON} + I_{IMON\_OS}\right)} = \frac{0.99\ V}{\left(300\ mA \times 52\ \frac{\mu A}{A} + 0.8\ \mu A\right)} = 60.36\ k\Omega \tag{36}$$

A close value of 61.9 kΩ is chosen for $R_{IMON}$.

图 10-28 shows the overload flag status when the load is changed from 150 mA to 600 mA and back. As seen in the 图 10-28, the overload status (OL_Status) becomes active HIGH when the load current crosses 300 mA.

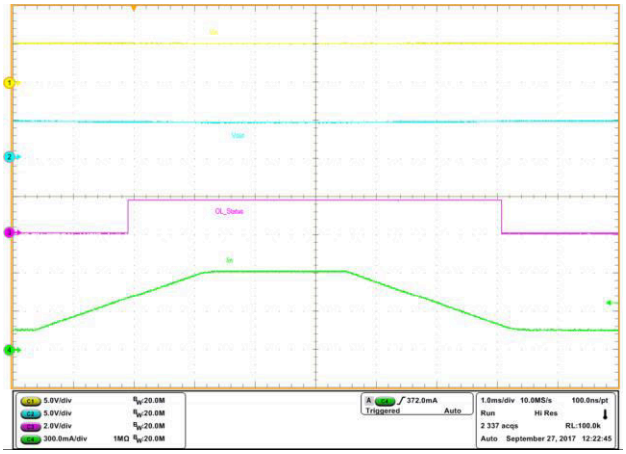


**图 10-28. Overload Flag Status for Change in Load from 150 mA to 600 mA and Back**

# 11 Power Supply Recommendations

The TPS25940xx-Q1 device is designed for supply voltage range of 2.7 V ⩽ $V_{IN}$ ⩽ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

## 11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. In case of sudden Output short-to-Battery faults with a long external cable, the cable inductance and output capacitance generates over voltage spike at the output. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- A 18-V TVS across output to GND to absorb positive spikes. Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with 方程式 37.

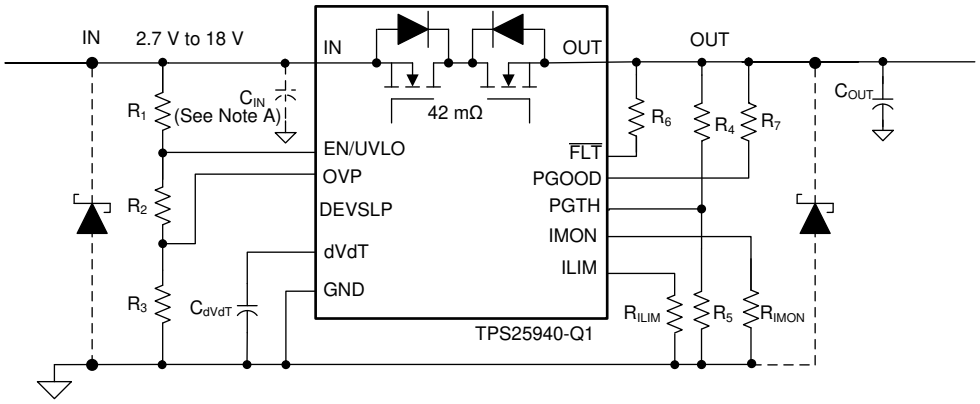
$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (37)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current,
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in 图 11-1.




A. Optional components needed for suppression of transients

**图 11-1. Circuit Implementation with Optional Protection Components**

## 11.2 Output Short-Circuit Measurements

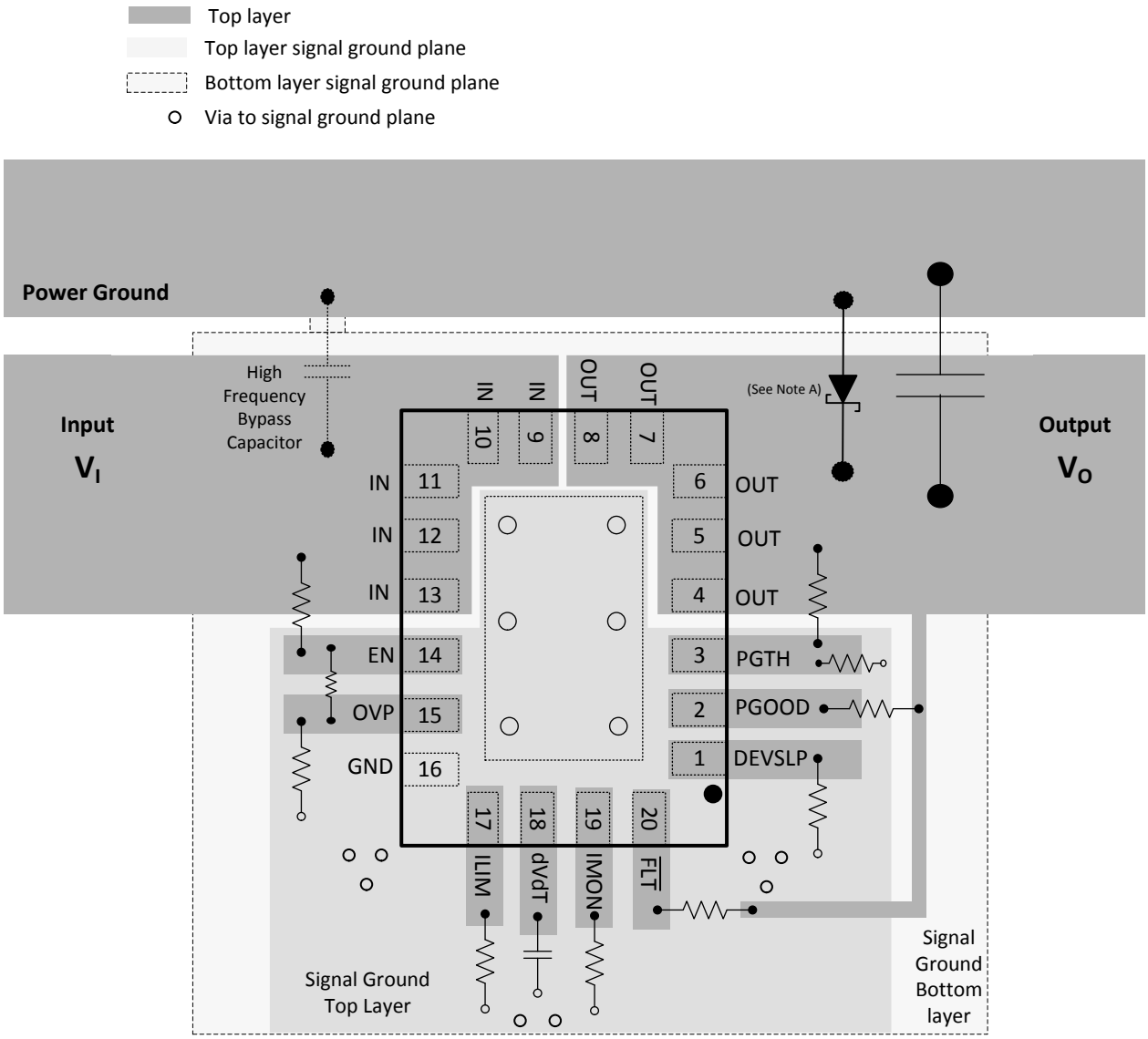
It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

# 12 Layout

## 12.1 Layout Guidelines

- For all applications, a 0.1-uF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See 图 12-1 for a PCB layout example.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- Low current signal ground (SGND), which is the reference ground for the device must be a copper plane or island.
- Locate all TPS25940xx-Q1 support components: $R_{(ILIM)}$, $C_{dVdT}$, $R_{(IMON)}$, and resistors for UVLO and OVP, close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
- The trace routing for the $R_{ILIM}$ and $R_{(IMON)}$ components to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- The SGND plane must be connected to high current ground (main power ground) at a single point, that is at the negative terminal of input capacitor.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Thermal Considerations: When properly mounted the PowerPAD™ package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. The PowerPAD is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. See the Technical Briefs, PowerPad™ Thermally Enhanced Package, SLMA002) and PowerPAD™ Made Easy, SLMA004) for more information on using this PowerPAD™ package.
- The thermal via land pattern specific to TPS25940xx-Q1 can be downloaded from the TPS25940 device webpage.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

## 12.2 Layout Example




A. Optional: Needed only to suppress the transients caused by inductive load switching

**图 12-1. Board Layout**

# 13 Device and Documentation Support

## 13.1 Documentation Support

### 13.1.1 Related Documentation

For related documetation see the following:

- *High-Efficiency Backup Power Supply*, SLVA676
- *TPS25940 Evaluation Module User's Guide*, SLVUA44

## 13.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 13.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 13.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS259401AQRVCRQ1 | ACTIVE | WQFN | RVC | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 9401AQ | Samples |
| TPS25940AQRVCRQ1 | ACTIVE | WQFN | RVC | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2594AQ | Samples |
| TPS25940AQRVCTQ1 | ACTIVE | WQFN | RVC | 20 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2594AQ | Samples |
| TPS25940LQRVCRQ1 | ACTIVE | WQFN | RVC | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T594LQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

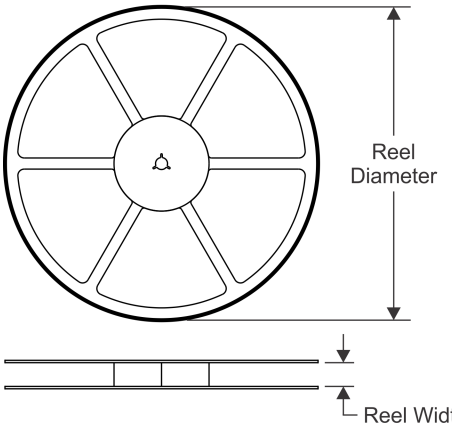
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

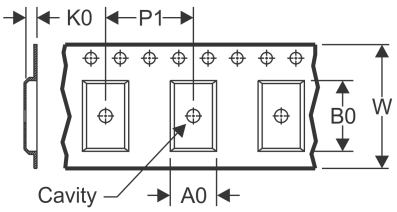
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

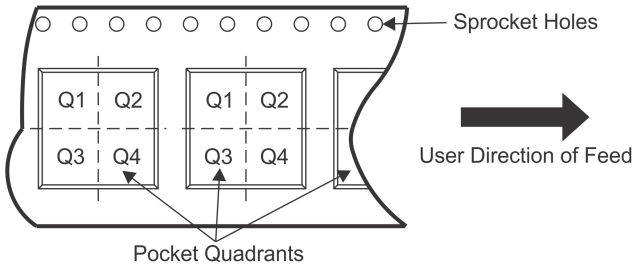



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

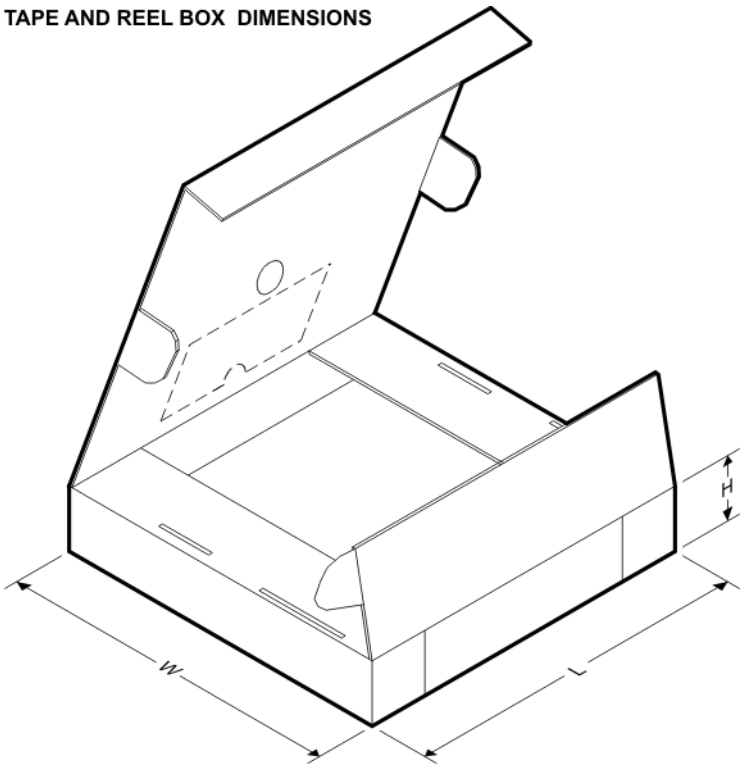
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS259401AQRVCRQ1 | WQFN | RVC | 20 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS25940AQRVCRQ1 | WQFN | RVC | 20 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS25940AQRVCTQ1 | WQFN | RVC | 20 | 250 | 180.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| TPS25940LQRVCRQ1 | WQFN | RVC | 20 | 3000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



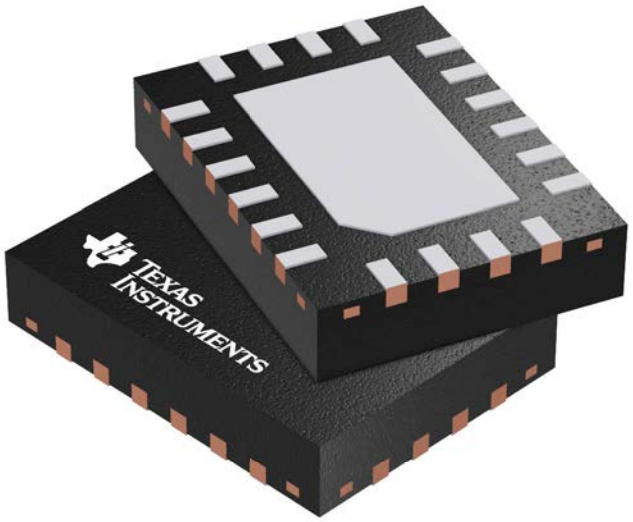

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS259401AQRVCRQ1 | WQFN | RVC | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS25940AQRVCRQ1 | WQFN | RVC | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS25940AQRVCTQ1 | WQFN | RVC | 20 | 250 | 210.0 | 185.0 | 35.0 |
| TPS25940LQRVCRQ1 | WQFN | RVC | 20 | 3000 | 367.0 | 367.0 | 35.0 |

# GENERIC PACKAGE VIEW

## RVC 20 WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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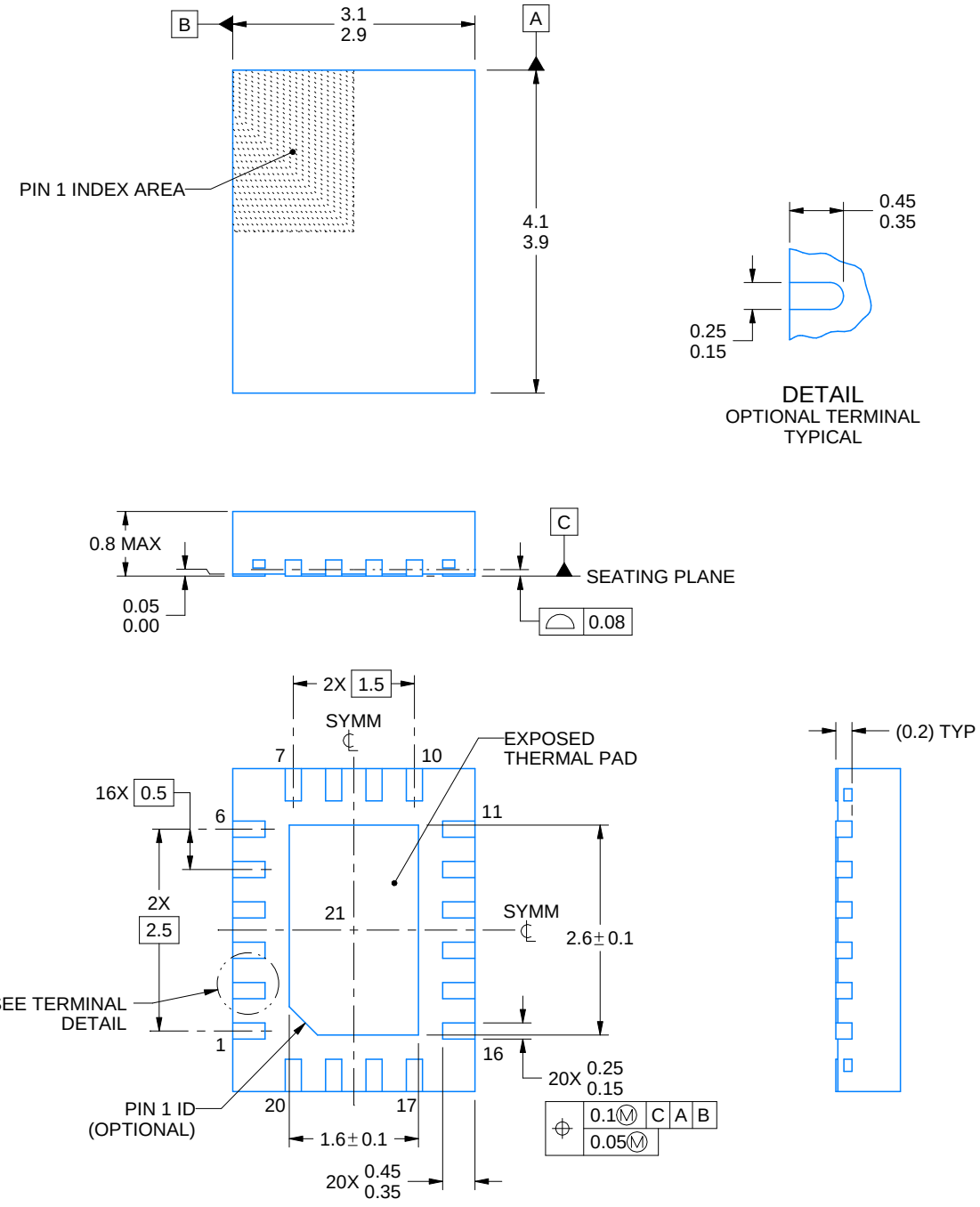
# PACKAGE OUTLINE

## RVC0020A

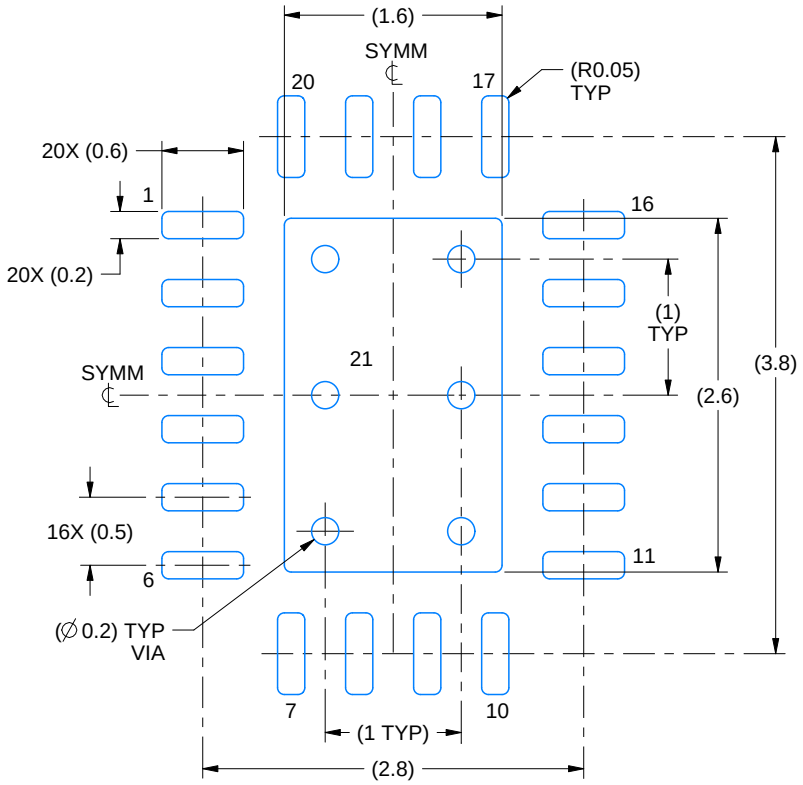
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

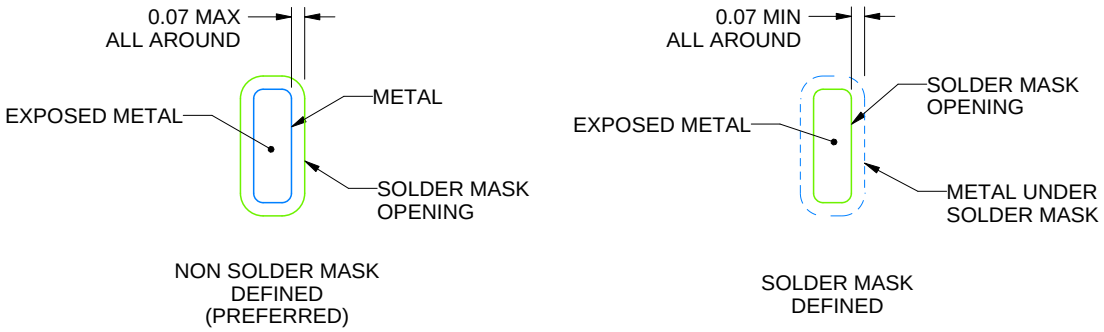



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X




SOLDER MASK DETAILS

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NOTES: (continued)

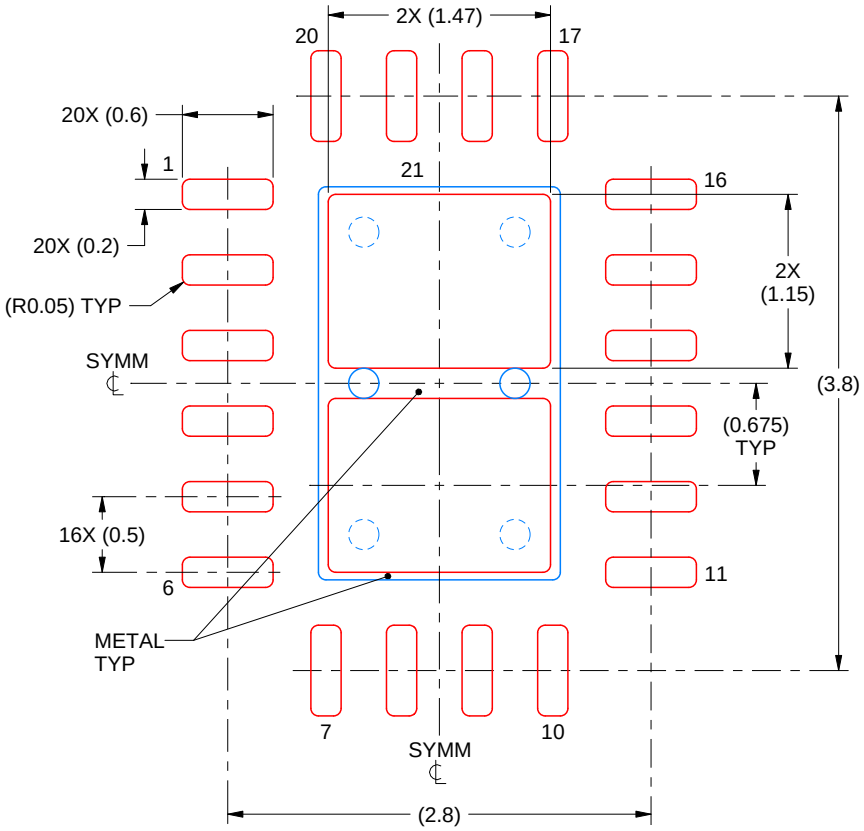
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## RVC0020A

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD X
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

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