SNx4AHCT16373 16-Bit Transparent D-Type Latches With 3-State Outputs

1 Features

- Members of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Inputs are TTL-Voltage Compatible
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include:
  - Plastic Shrink Small-Outline (DL) Package
  - Thin Shrink Small-Outline (DGG) Package
  - Thin Very Small-Outline (DGV) Package
  - 80-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

2 Applications

- Wearable Health and Fitness Devices
- Toys
- PCs and Notebooks
- Power Infrastructures
- Servers

3 Description

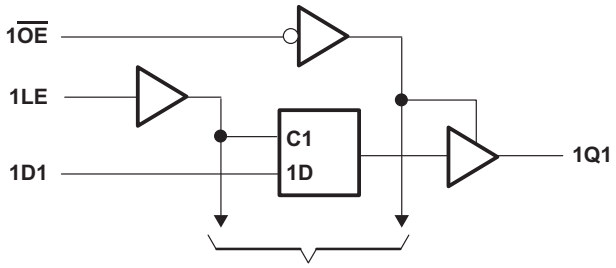
The SNxAHCT16373 devices are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

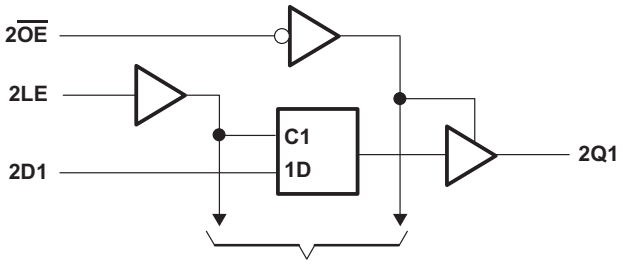
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC16373	TSSOP (48)	12.50 mm × 6.10 mm
	TVSOP (48)	9.70 mm × 4.40 mm
	SSOP (48)	15.88 mm × 7.49 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic





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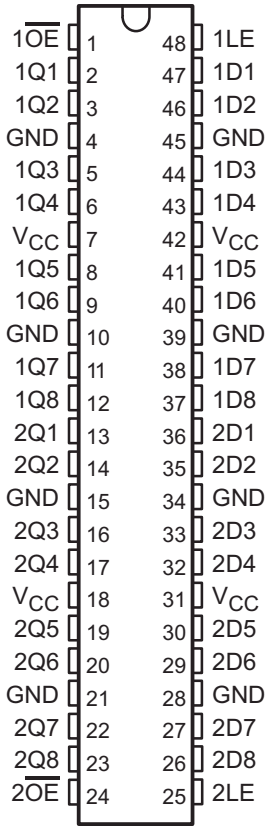
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2000) to Revision I	Page
• Updated document to new TI data sheet format.	1
• Deleted Ordering Information table.	1
• Added Applications.	1
• Added Pin Functions table.	3
• Added Handling Ratings table.	5
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	5
• Added Thermal Information table.	6
• Added –40°C to 125°C for SN74AHCT16373 in Electrical Characteristics table.	6
• Added T_A = –40°C to 125°C for SN74AHCT16373 in the Timing Requirements table.	6
• Added T_A = –40°C to 125°C for SN74AHCT16373 in the Switching Characteristics table.	7
• Added Typical Characteristics.	8
• Added Detailed Description section.	10
• Added Application and Implementation section.	12
• Added Power Supply Recommendations and Layout sections.	13

6 Pin Configuration and Functions

SN54AHCT16373 . . . WD PACKAGE
SN74AHCT16373 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$1\overline{OE}$	I	Output Enable 1
2	1Q1	O	1Q1 Output
3	1Q2	O	1Q2 Output
4	GND	—	Ground Pin
5	1Q3	O	1Q3 Output
6	1Q4	O	1Q4 Output
7	V_{CC}	—	Power Pin
8	1Q5	O	1Q5 Output
9	1Q6	O	1Q6 Output
10	GND	—	Ground Pin
11	1Q7	O	1Q7 Output
12	1Q8	O	1Q8 Output
13	2Q1	O	2Q1 Output
14	2Q2	O	2Q2 Output
15	GND	—	Ground Pin
16	2Q3	O	2Q3 Output
17	2Q4	O	2Q4 Output
18	V_{CC}	—	Power Pin

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
19	2Q5	O	2Q5 Output
20	2Q6	O	2Q6 Output
21	GND	—	Ground Pin
22	2Q7	O	2Q7 Output
23	2Q8	O	2Q8 Output
24	$2\overline{OE}$	I	Output Enable 2
25	2LE	I	Latch Enable 2
26	2D8	I	2D8 Input
27	2D7	I	2D7 Input
28	GND	—	Ground Pin
29	2D6	I	2D6 Input
30	2D5	I	2D5 Input
31	V_{CC}	—	Power Pin
32	2D4	I	2D4 Input
33	2D3	I	2D3 Input
34	GND	—	Ground Pin
35	2D2	I	2D2 Input
36	2D1	I	2D1 Input
37	1D8	I	1D8 Input
38	1D7	I	1D7 Input
39	GND	—	Ground Pin
40	1D6	I	1D6 Input
41	1D5	I	1D5 Input
42	V_{CC}	—	Power Pin
43	1D4	I	1D4 Input
44	1D3	I	1D3 Input
45	GND	—	Ground Pin
46	1D2	I	1D2 Input
47	1D1	I	1D1 Input
48	1LE	I	Latch Enable 1

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHCT16373(2)		SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) Product Preview

7.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT16373			UNIT
		DGG	DGV	DL	
		48 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.9	80.9	61.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.2	32.8	31.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	26.9	44.0	33.2	
ψ_{JT}	Junction-to-top characterization parameter	1.9	3.3	9.0	
ψ_{JB}	Junction-to-board characterization parameter	36.6	43.4	32.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16373[1]		–40°C to 85°C SN74AHCT16373		–40°C to 125°C SN74AHCT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44		0.44	
I_I	V_I = V_{CC} or GND	0 V to 5.5 V			±0.1		±1[2]		±1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40		40	µA
ΔI_{CC}[3]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2.5	10				10			pF
C_o	V_O = V_{CC} or GND	5 V		4.5								pF

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(3) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

7.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		SN54AHCT16373[1]		SN74AHCT16373		T_A = –40°C to 125°C SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	6.5		6.5		6.5		6.5		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		1.5		1.5		ns
t_h	Hold time, data after LE↓	3.5		3.5		3.5		3.5		ns

(1) Product Preview

7.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (OUTPUT)	TO (INPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16373(1)		SN74AHCT16373		SN74AHCT16373 T_A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	C_L = 15 pF		5.1(2)	8.5(2)	1(2)	9.5(2)	1	9.5	1	10.5	ns
t_{PHL}					5.1(2)	8.5(2)	1(2)	9.5(2)	1	9.5	1	10.5	
t_{PLH}	LE	Q	C_L = 15 pF		5(2)	8.5(2)	1(2)	9.5(2)	1	9.5	1	10.5	ns
t_{PHL}					5(2)	8.5(2)	1(2)	9.5(2)	1	9.5	1	10.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5(2)	9.5(2)	1(2)	10.5(2)	1	10.5	1	11.1	ns
t_{PZL}					5(2)	9.5(2)	1(2)	10.5(2)	1	10.5	1	11.1	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		6(2)	10.2(2)	1(2)	11(2)	1	11	1	11.6	ns
t_{PLZ}					6.8(2)	10.2(2)	1(2)	11(2)	1	11	1	11.6	
t_{PLH}	D	Q	C_L = 50 pF		5.9	9.5	1	10.5	1	10.5	1	11.5	ns
t_{PHL}					5.9	9.5	1	10.5	1	10.5	1	11.5	
t_{PLH}	LE	Q	C_L = 50 pF		6.4	9.5	1	10.5	1	10.5	1	11.5	ns
t_{PHL}					5.9	9.5	1	10.5	1	10.5	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6	10.5	1	11.5	1	11.5	1	12.1	ns
t_{PZL}					6	10.5	1	11.5	1	11.5	1	12.1	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.8	11.2	1	12	1	12	1	12.6	ns
t_{PLZ}					7.8	11.2	1	12	1	12	1	12.6	
$t_{sk(o)}$			C_L = 50 pF			1(3)				1		1	ns

(1) Product Preview
(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(3) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		SN74AHCT16373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.32	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

7.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	22	pF

7.10 Typical Characteristics

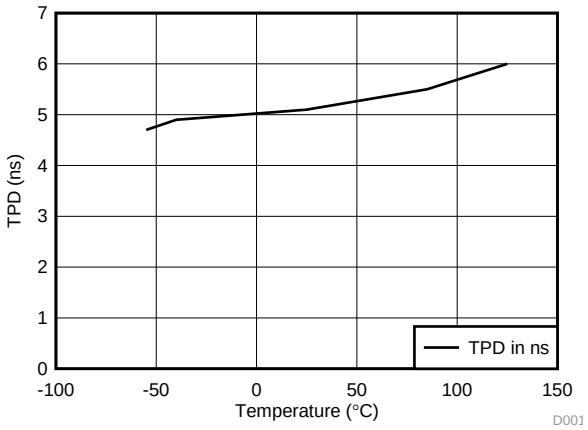
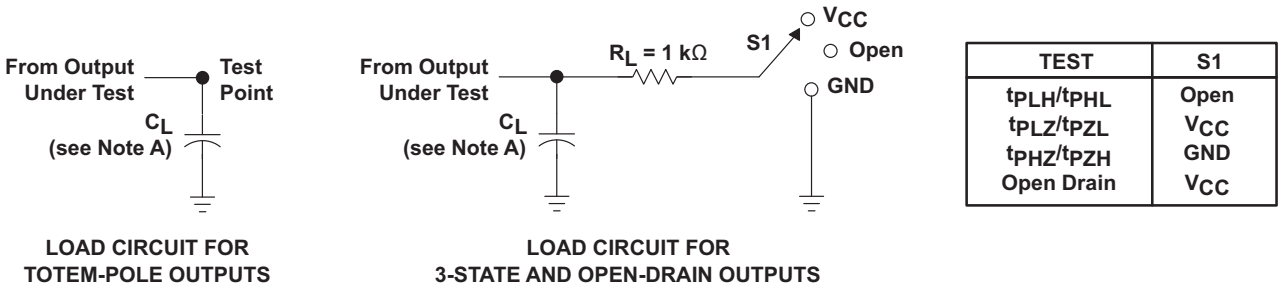


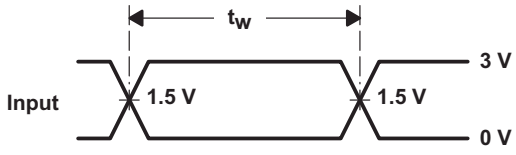
Figure 1. TPD vs Temperature

8 Parameter Measurement Information

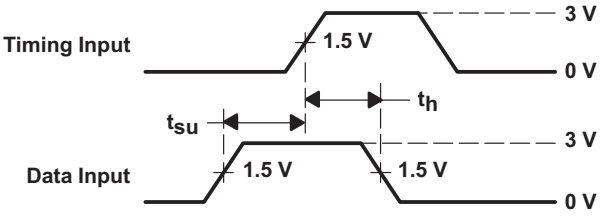


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

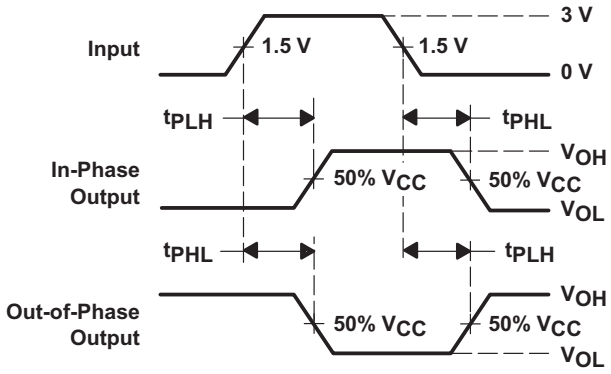
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



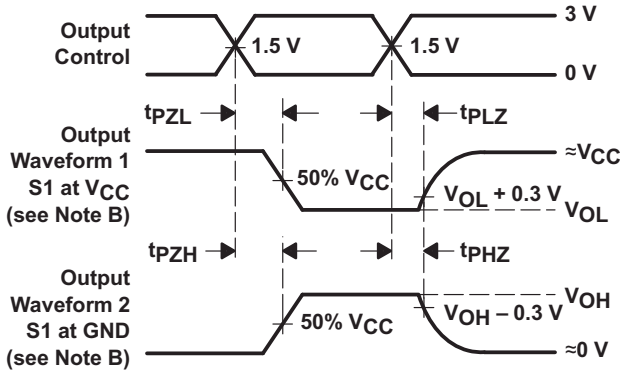
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNxAHCT16373 devices are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, IO ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagrams

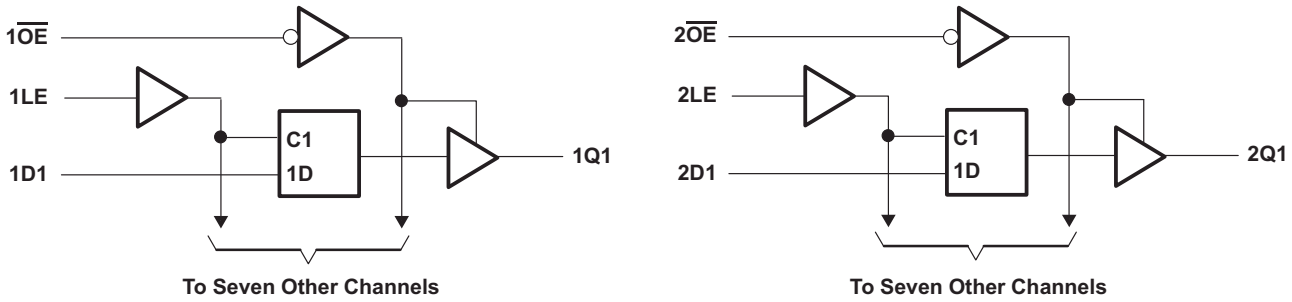
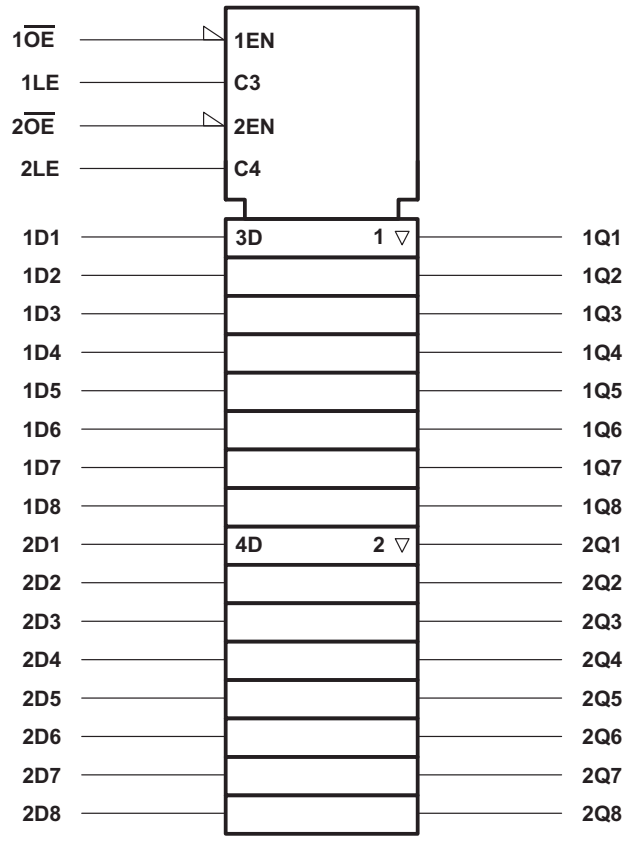


Figure 3. Logic Diagram (Positive Logic)

Functional Block Diagrams (continued)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 4. Logic Symbol

9.3 Feature Description

- TTL inputs
  - Lowered switching threshold allows up translation from 3.3 V to 5 V
- Slow edges reduce output ringing

9.4 Device Functional Modes

Table 1. Function Table (Each 8-bit Latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

10 Application and Implementation

10.1 Application Information

The SN74AHCT16373 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH}. This feature makes it ideal for translating up from 3.3 V to 5 V. Figure 6 shows this type of translation.

10.2 Typical Application

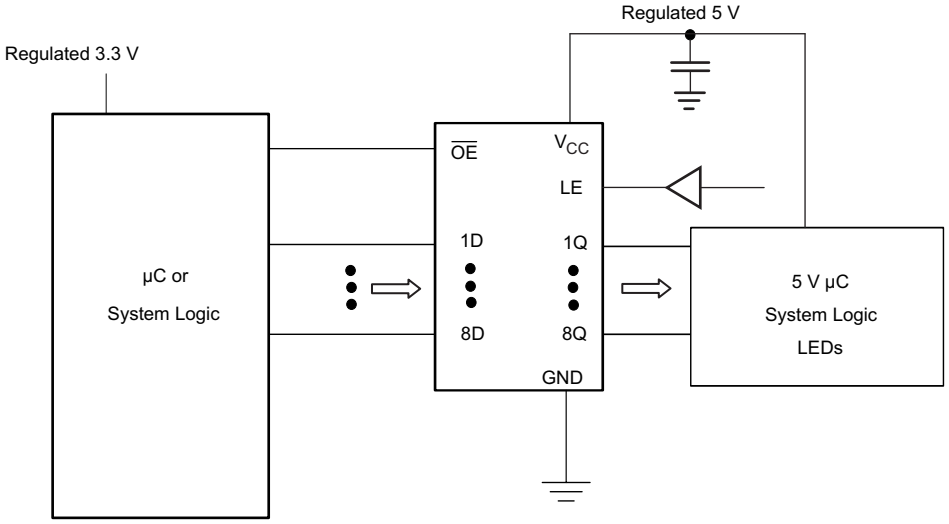


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified High and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 25 mA per output and 75 mA total for the part
   - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curves

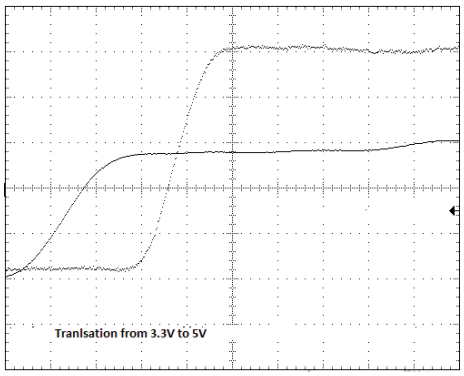


Figure 6. Up Translation

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input-AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 7 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

12.2 Layout Example

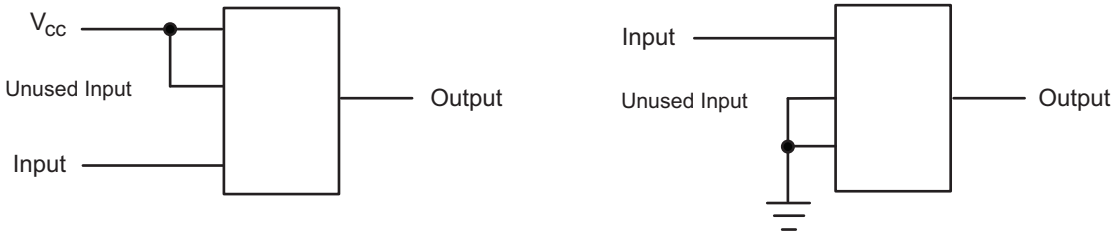


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT16373	Click here	Click here	Click here	Click here	Click here
SN74AHCT16373	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHCT16373DGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT16373	Samples
SN74AHCT16373DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT16373	Samples
SN74AHCT16373DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HF373	Samples
SN74AHCT16373DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT16373	Samples
SN74AHCT16373DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT16373	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

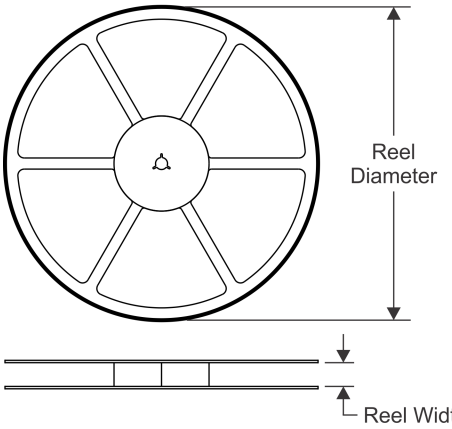
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

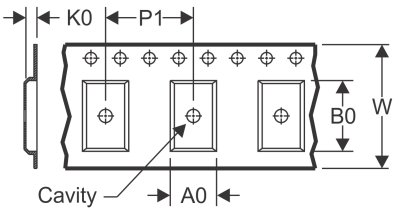
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

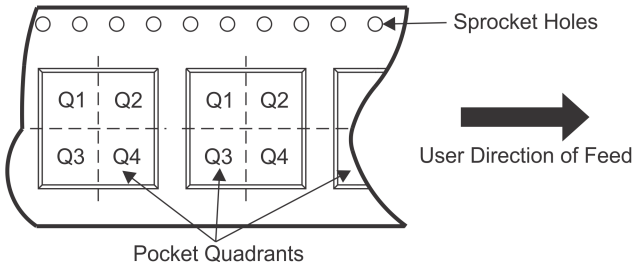


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

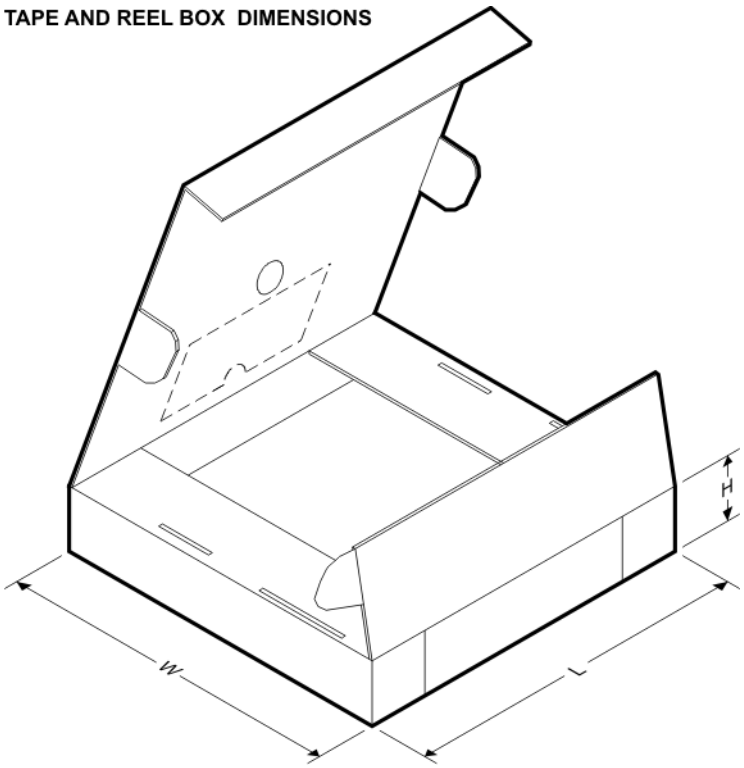
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT16373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AHCT16373DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AHCT16373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

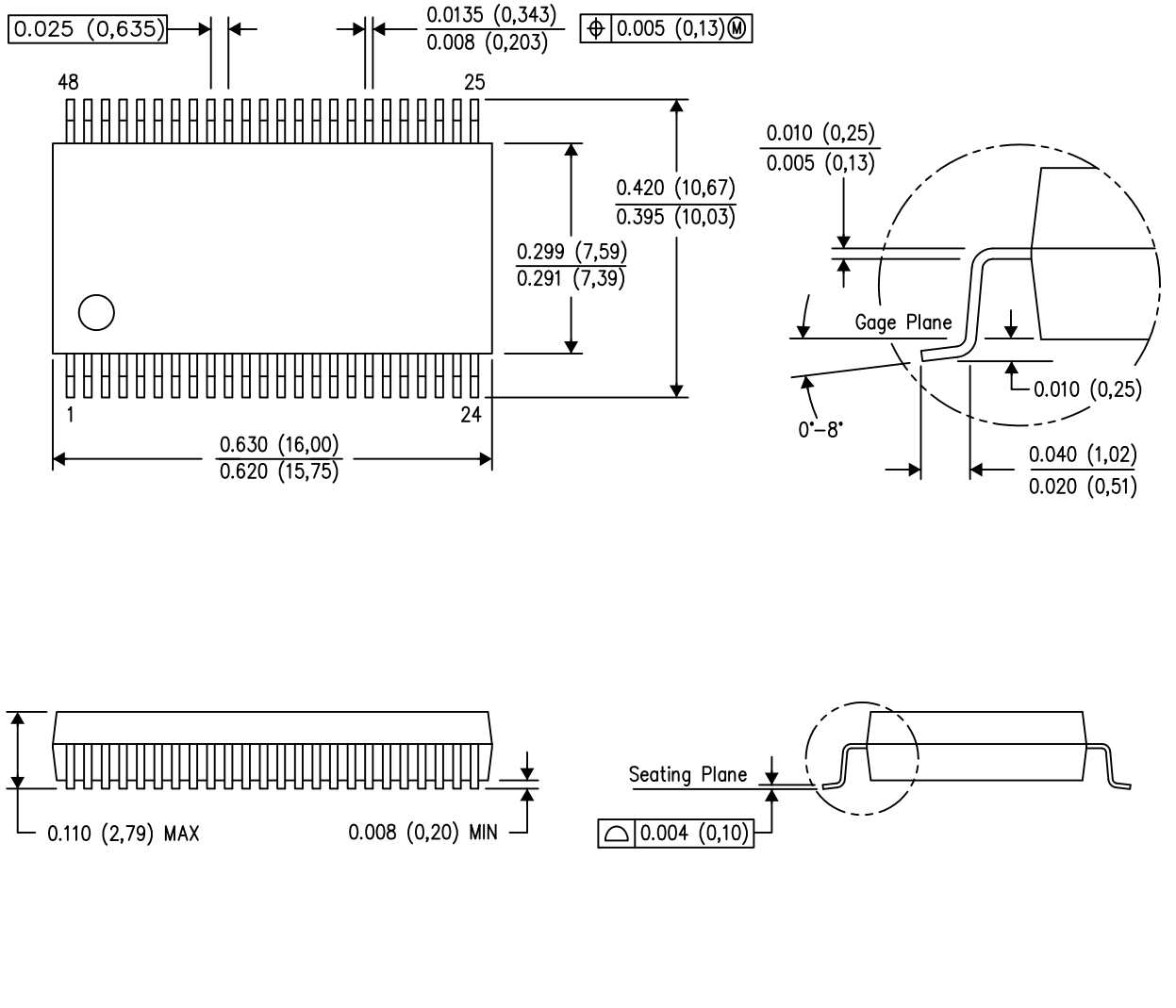
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT16373DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AHCT16373DGVR	TVSOP	DGV	48	2000	853.0	449.0	35.0
SN74AHCT16373DLR	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE

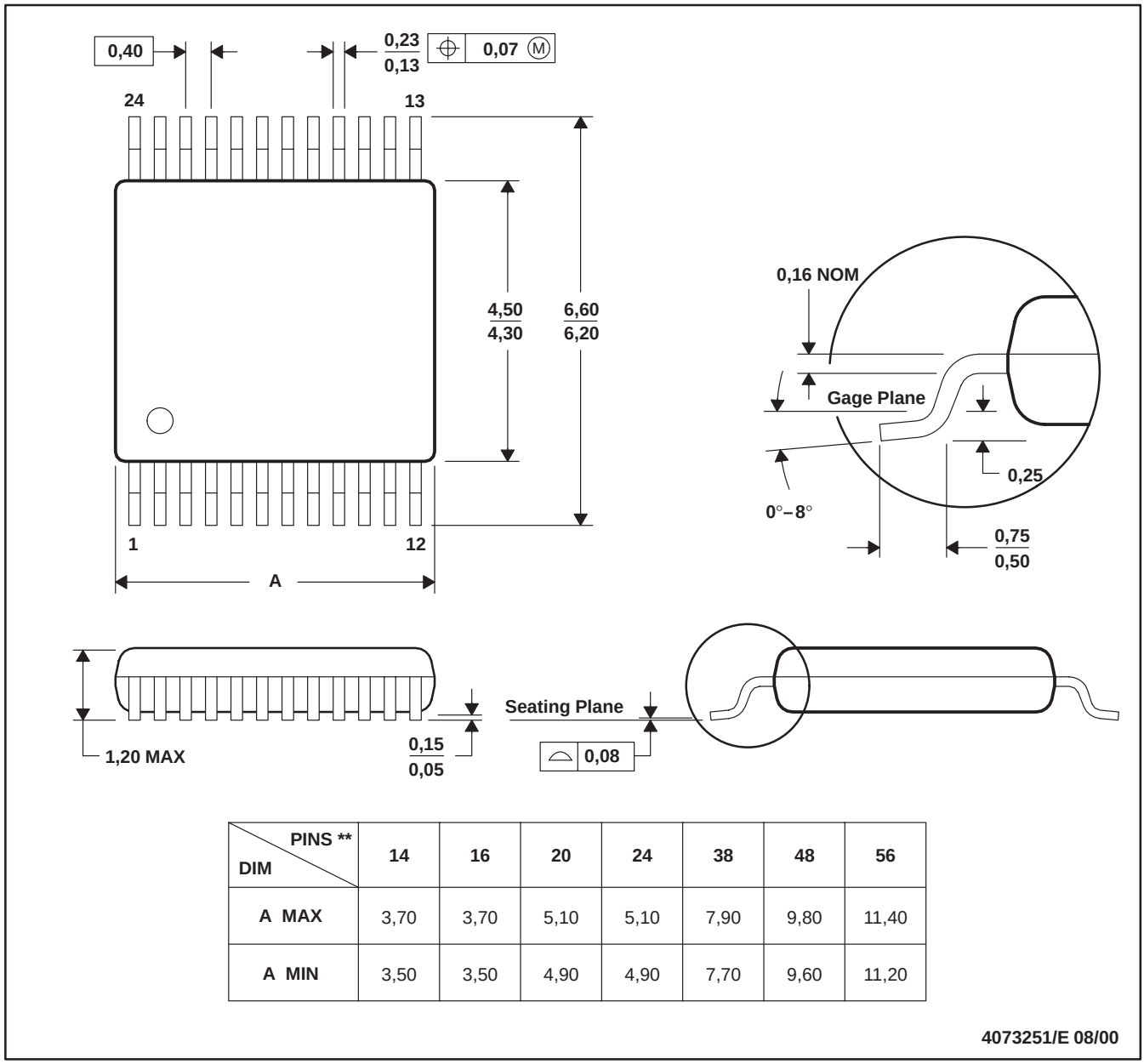


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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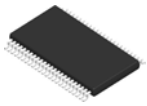
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

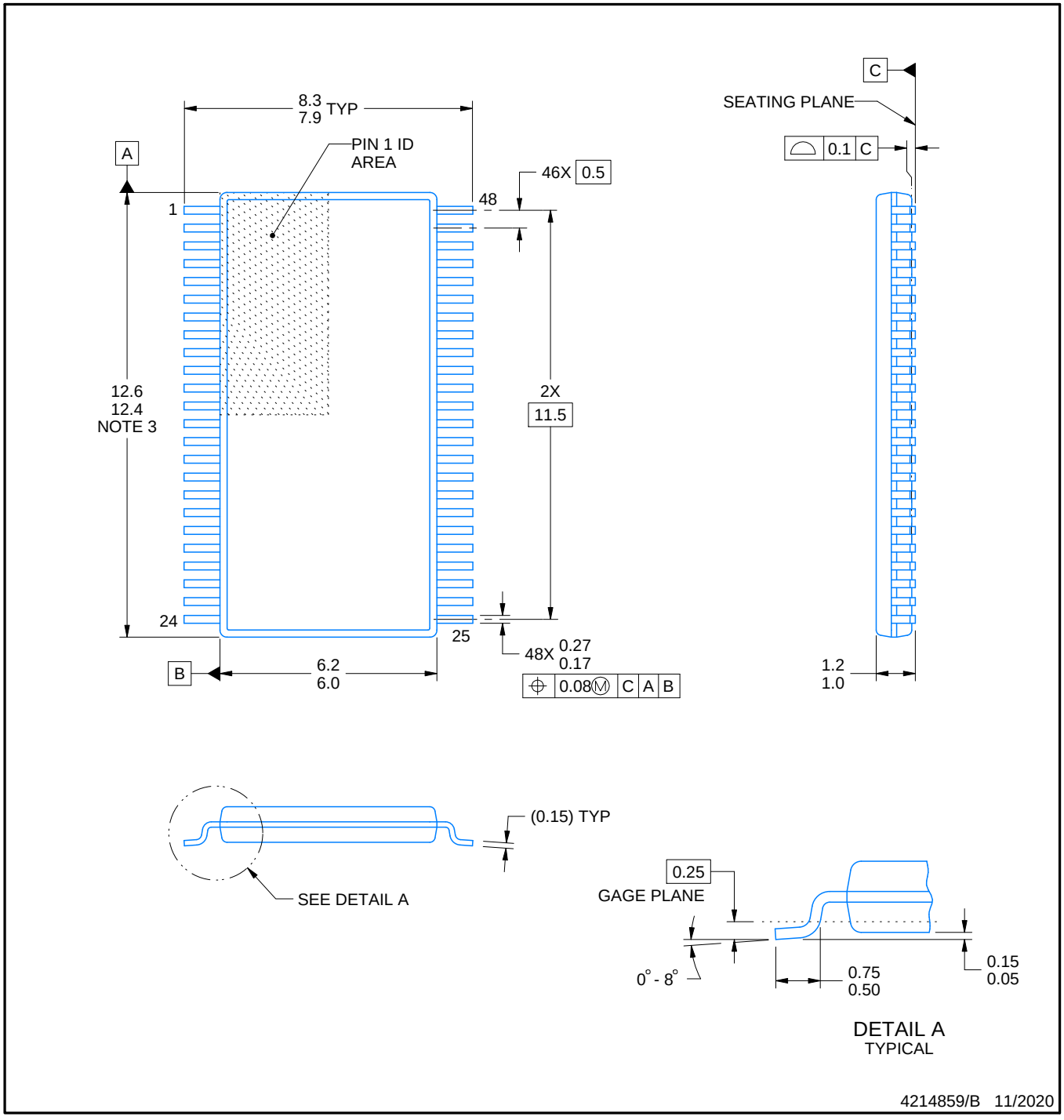


PACKAGE OUTLINE

DGG0048A

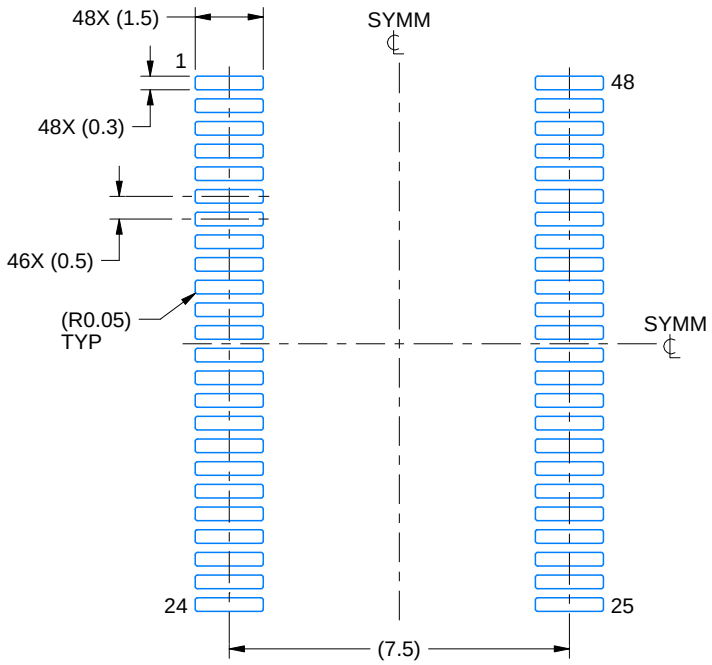
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

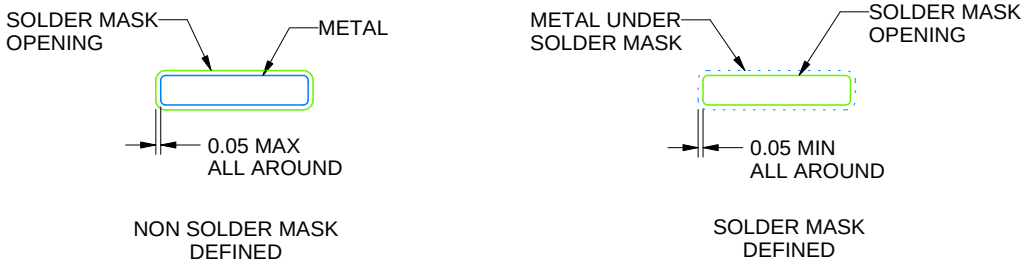


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

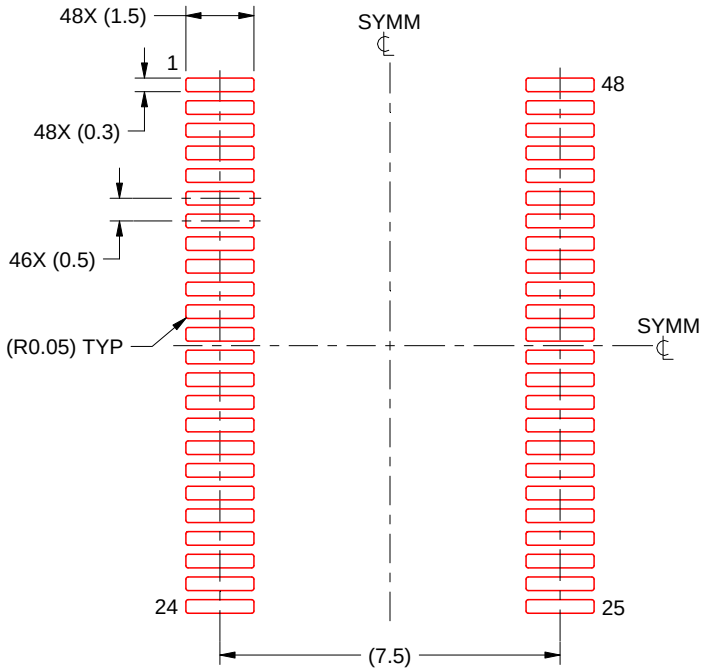


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

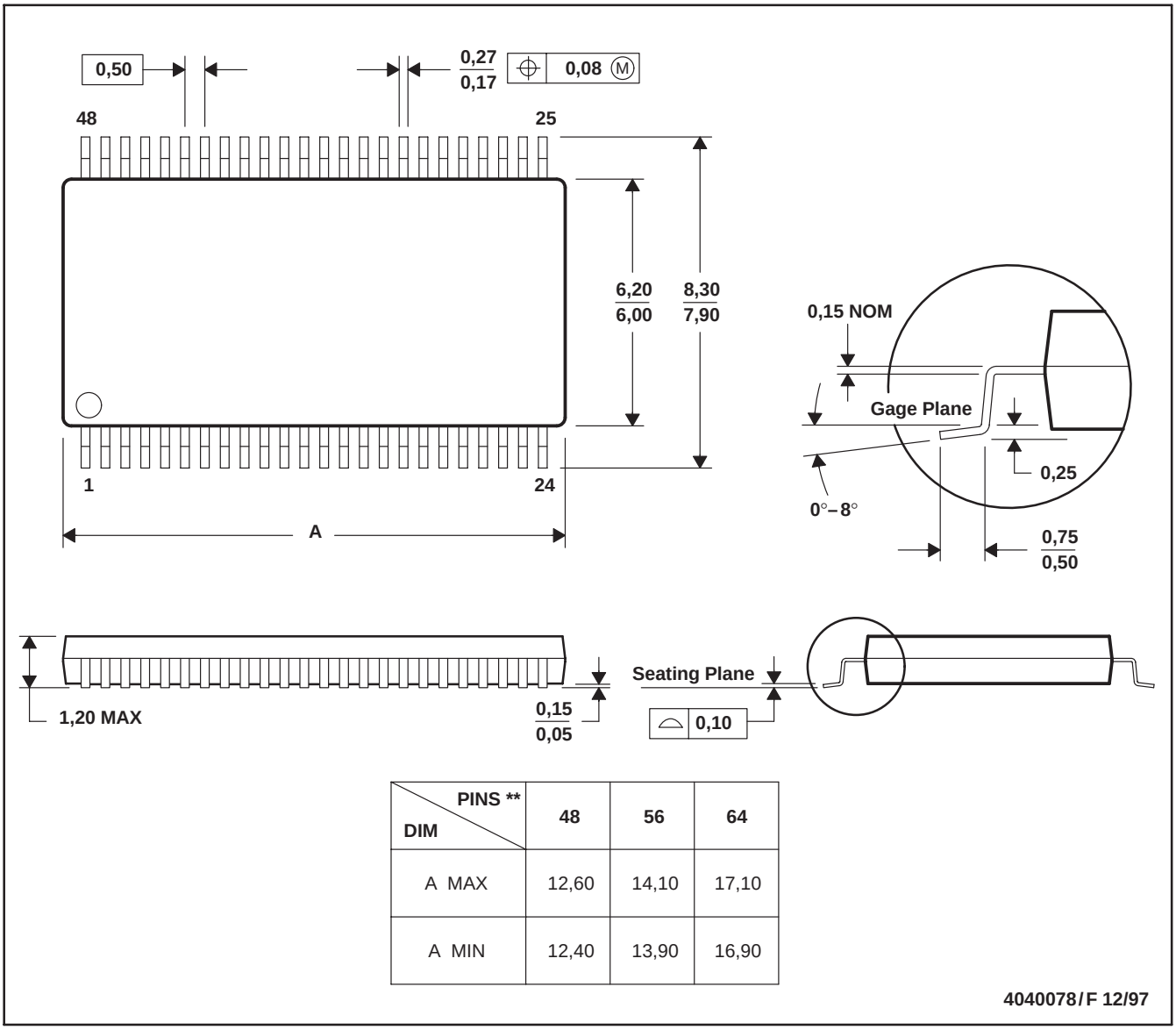
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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