适用于 SiC/IGBT 并具有主动保护、隔离式模拟感应和高 CMTI 的 UCC21750-Q1 10A 拉电流/灌电流增强型隔离式单通道栅极驱动器

1 特性

- 5.7kV $_{RMS}$ 单通道隔离式栅极驱动器
- 符合面向汽车应用的 AEC-Q100 标准
- 高达 2121V$_{pk}$ 的 SiC MOSFET 和 IGBT
- 33V 最大输出驱动电压 (VDD-VEE)
- ±10A 驱动强度和分离输出
- 150V/ns 最小 CMTI
- 具有 200ns 快速响应时间的 DESAT 保护
- 4A 内部有源米勒钳位
- 发生故障时的 400mA 软关断
- 具有 PWM 输出的隔离式模拟传感器
  - 采用 NTC、PTC 或热敏二极管的温度感应
  - 高电压直流链路或相电压
- 过流警报 $\overline{\text{FLT}}$ 和通过 $\overline{\text{RST}}$/EN 重置
- 针对 $\overline{\text{RST}}$/EN 的快速启用/禁用响应
- 抑制输入引脚上的 <40ns 噪声瞬态和脉冲
- RDY 上的 12V VDD UVLO（具有电源正常指示功能）
- 具有高达 5V 的过冲/欠冲瞬态电压抗扰度的输入/输出
- 130ns（最大）传播延迟和 30ns（最大）脉冲/器件间偏移
- SOIC-16 DW 封装，爬电距离和间隙 > 8mm
- 工作结温范围：-40°C 至 +150°C

2 应用

- 适用于 EV 的牵引逆变器
- 车载充电器和充电桩
- 用于 HEV/EV 的直流/直流转换器

3 说明

UCC21750-Q1 是一款电隔离单通道栅极驱动器，用于具有高达 2121V 直流工作电压的 SiC MOSFET 和 IGBT，具有高级保护功能 功能、出色的动态性能和稳健性。UCC21750-Q1 具有高达 ±10A 的峰值拉电流和灌电流。

输入侧通过 SiO_2 电容隔离技术与输出侧相隔离，支持高达 1.5kV$_{RMS}$ 的工作电压、12.8kV$_{PK}$ 的浪涌抗扰度，隔离层寿命超过 40 年，并提供较低的器件间偏移、大于 150V/ns 的共模噪声抗扰度 (CMTI)。

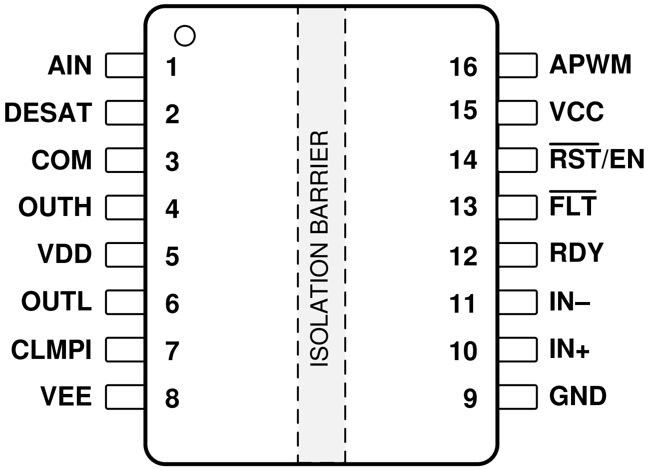
UCC21750-Q1 具有高级保护功能 功能，如快速过流和短路检测、分流电流检测支持、故障报告、有源米勒钳位、输入和输出侧电源 UVLO（用于优化 SiC 和 IGBT 开关行为）和稳健性。可以利用隔离式模拟至 PWM 传感器更轻松地进行温度或电压检测，从而进一步提高驱动器的多功能性并简化系统设计工作量、尺寸和成本。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC21750-Q1	DW SOIC-16	10.3mm × 7.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件引脚配置



Not to scale

ADVANCE INFORMATION

English Data Sheet: SLUSDH9

目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 Pin Configuration and Functions 3
6 Specifications 5
  6.1 Absolute Maximum Ratings 5
  6.2 ESD Ratings 5
  6.3 Recommended Operating Conditions 5
  6.4 Thermal Information 5
  6.5 Power Ratings 6
  6.6 Insulation Specifications 7
  6.7 Safety-Related Certifications 8
  6.8 Safety Limiting Values 8
  6.9 Electrical Characteristics 9
  6.10 Switching Characteristics 11
  6.11 Insulation Characteristics Curves 12
  6.12 Typical Characteristics 13
7 Parameter Measurement Information 16
  7.1 Propagation Delay 16
  7.2 Input Deglitch Filter 17
  7.3 Active Miller Clamp 18
  7.4 Under Voltage Lockout (UVLO) 19
  7.5 Desaturation (DESAT) Protection 21
8 Detailed Description 23
  8.1 Overview 23
  8.2 Functional Block Diagram 24
  8.3 Feature Description 24
  8.4 Device Functional Modes 31
9 Applications and Implementation 32
  9.1 Application Information 32
  9.2 Typical Application 32
10 Power Supply Recommendations 43
11 Layout 44
  11.1 Layout Guidelines 44
  11.2 Layout Example 45
12 器件和文档支持 46
  12.1 文档支持 46
  12.2 接收文档更新通知 46
  12.3 社区资源 46
  12.4 商标 46
  12.5 静电放电警告 46
  12.6 Glossary 46
13 机械、封装和可订购信息 47

4 修订历史记录

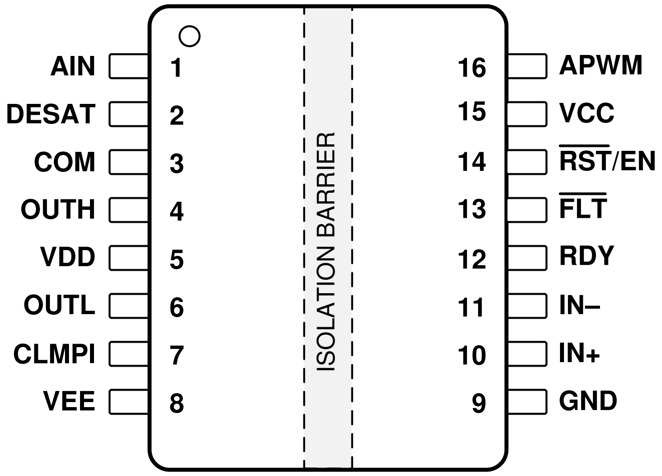
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年9 月	*	预告信息发布

ADVANCE INFORMATION

5 Pin Configuration and Functions

UCC21750-Q1
DW SOIC (16)
Top View



Not to scale

Pin Functions

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
AIN	1	I	Isolated analog sensing input, parallel a small capacitor to COM for better noise immunity
DESAT	2	I	Denaturation current protection input
COM	3	P	Common ground reference, connecting to emitter pin for IGBT and source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pull up
VDD	5	P	Positive supply rail for gate drive voltage, Bypassing a >220nF capacitor to COM to support specified gate driver source peak current capability
OUTL	6	O	Gate driver output pull down
CLMPI	7	I	Internal Active miller clamp, connecting this pin directly to the gate of the power transistor
VEE	8	P	Negative supply rail for gate drive voltage. Bypassing a >220nF capacitor to COM to support specified gate driver sink peak current capability
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Non-inverting gate driver control input
IN–	11	I	Inverting gate driver control input
RDY	12	O	Power good for VCC-GND and VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals
$\overline{\text{FLT}}$	13	O	Active low fault alarm output upon over current or short circuit. $\overline{\text{FLT}}$ is in open drain configuration and can be paralleled with other faults
$\overline{\text{RST}}$/EN	14	I	The $\overline{\text{RST}}$/EN serves two purposes: 1) Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low; 2) Resets the DESAT condition signaled on $\overline{\text{FLT}}$ pin. if terminal $\overline{\text{RST}}$/EN is set to low for more than 1000ns. A reset of signal $\overline{\text{FLT}}$ is asserted at the rising edge of terminal $\overline{\text{RST}}$/EN. For automatic RESET function, this pin only serves as an EN pin. Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low.
VCC	15	P	Input power supply from 3V to 5.5V, bypassing a >100nF capacitor to GND
APWM	16	O	Isolated Analog Sensing PWM output

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			MIN	MAX	UNIT
VCC	VCC – GND		–0.3	6	V
VDD	VDD – COM		–0.3	36	V
VEE	VEE – COM		–17.5	0.3	V
V_{MAX}	VDD – VEE		–0.3	36	V
IN+, IN–, $\overline{\text{RST}}$/EN		DC	GND–0.3	VCC	V
		Transient, less than 100 ns(2)	GND–5.0	VCC+5.0	V
DESAT	Reference to COM		COM–0.3	VDD+0.3	V
AIN	Reference to COM		–0.3	5	V
OUTH, OUTL , CLMPI		DC	VEE–0.3	VDD	V
		Transient, less than 100 ns(2)	VEE–5.0	VDD+5.0	V
CLMPE	Reference to VEE		–0.3	5	V
RDY, $\overline{\text{FLT}}$, APWM			GND–0.3	VCC	V
$I_{\overline{FLT}}$, I_{RDY}	$\overline{\text{FLT}}$, and RDY pin input current			20	mA
I_{APWM}	APWM pin output current			20	mA
T_J	Junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization on bench.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

PARAMETER			MIN	MAX	UNIT
VCC	VCC–GND		3.0	5.5	V
VDD	VDD–COM		13	33	V
V_{MAX}	VDD–VEE		–	33	V
IN+, IN–, $\overline{\text{RST}}$/EN	Reference to GND	High level input voltage	0.7×VCC	VCC	V
		Low level input voltage	0	0.3×VCC	
AIN	Reference to COM		0.6	4.5	V
$t_{RST/EN}$	Minimum pulse width that reset the fault		1000		ns
T_A	Ambient Temperature		–40	125	°C
T_J	Junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC21750-Q1	UNIT
		DW (SOIC)	
		16	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		UCC21750-Q1	UNIT
		DW (SOIC)	
		16	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.3	°C/W

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	Value	UNIT
P_D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T_a=25^{o}C	985	mW
P_{D1}	Maximum power dissipation by transmitter side		20	mW
P_{D2}	Maximum power dissipation by receiver side		965	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (Internal clearance) of the double insulation (2 × 0.0085 mm)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11):2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST}=V_{IOTM}, t = 60 s (qualification test)	8000	V_{PK}
		V_{TEST}=1.2 x V_{IOTM}, t = 1 s (100% production test)	9600	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 12800 V_{PK} (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 2545 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 3394 V_{PK}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = 3977 V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 sin (2πft), f = 1 MHz	~ 1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$\geq 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$\geq 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$\geq 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 6840 V_{RMS}, t = 1 s (100% production)	5700	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	UL	CSA	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01; DIN EN 61010-1 (VDE 0411-1):2011-07	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Single protection, 5700 V_{RMS}	Isolation Rating of 5700 V_{RMS}; Reinforced insulation per CSA 60950-1- 07+A1+A2 and IEC 60950-1 (2nd Ed.), 1450 V_{RMS} max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage	Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 1000 V_{RMS} 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 1450 V_{RMS}
Certification Planned	Certification Planned	Certification Planned	Certification Planned	Certification Planned

6.8 Safety Limiting Values

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance. These limits vary with the ambient temperature, the junction-to-air thermal resistance, and the power supply voltages in different applications.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =68.3°C/W, V_{DD} = 15V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			91	mA
		$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			73	
P_S	Safety input, output, or total power	$R_{\theta JA}$ =68.3°C/W, V_{DD} = 20V, V_{EE}=-5V, T_J = 150°C, T_A = 25°C			1830	mW
T_S	Safety temperature				150	°C

6.9 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD – COM = 20 V, 18 V or 15 V, COM – VEE = 0 V, 5 V, 8 V or 15 V, C_L = 100 pF, –40°C < T_J < 150°C (unless otherwise noted)(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC UVLO THRESHOLD AND DELAY						
$V_{\text{VCC\_ON}}$	VCC–GND		2.55	2.7	2.85	V
$V_{\text{VCC\_OFF}}$			2.35	2.5	2.65	
$V_{\text{VCC\_HYS}}$				0.2		
t_{VCCFIL}	VCC UVLO Deglitch time			10		µs
$t_{\text{VCC+ to OUT}}$	VCC UVLO on delay to output high	IN+ = VCC, IN– = GND		37.8		
$t_{\text{VCC– to OUT}}$	VCC UVLO off delay to output low			10		
$t_{\text{VCC+ to RDY}}$	VCC UVLO on delay to RDY high	$\overline{\text{RST}}$/EN = VCC		37.8		
$t_{\text{VCC– to RDY}}$	VCC UVLO off delay to RDY low			10		
VDD UVLO THRESHOLD AND DELAY						
$V_{\text{VDD\_ON}}$	VDD–COM		11.2	12.0	12.8	V
$V_{\text{VDD\_OFF}}$			9.9	10.7	11.5	
$V_{\text{VDD\_HYS}}$				0.8		
t_{VDDFIL}	VDD UVLO Deglitch time			5		µs
$t_{\text{VDD+ to OUT}}$	VDD UVLO on delay to output high	IN+ = VCC, IN– = GND		5		
$t_{\text{VDD– to OUT}}$	VDD UVLO off delay to output low			5		
$t_{\text{VDD+ to RDY}}$	VDD UVLO on delay to RDY high	$\overline{\text{RST}}$/EN = $\overline{\text{FLT}}$=High		10		
$t_{\text{VDD– to RDY}}$	VDD UVLO off delay to RDY low			10		
VCC, VDD QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	OUT(H) = High, f_S = 0Hz, AIN=2V		3		mA
		OUT(L) = Low, f_S = 0Hz, AIN=2V		2		
I_{VDDQ}	VDD quiescent current	OUT(H) = High, f_S = 0Hz, AIN=2V		4		mA
		OUT(L) = Low, f_S = 0Hz, AIN=2V		3.7		
LOGIC INPUTS — IN+, IN– and $\overline{\text{RST}}$/EN						
V_{INH}	Input high threshold	V_{CC}=3.3V		1.85	2.31	V
V_{INL}	Input low threshold	V_{CC}=3.3V	0.99	1.52		V
V_{INHYS}	Input threshold hysteresis	V_{CC}=3.3V		0.33		V
I_{IH}	Input high level input leakage current	V_{IN} = VCC		90		µA
I_{IL}	Input low level input leakage	V_{IN} = GND		–90		µA
R_{IND}	Input pins pull down resistance	see Detailed Description for more information		55		kΩ
R_{INU}	Input pins pull up resistance	see Detailed Description for more information		55		
T_{INFIL}	IN+, IN– and $\overline{\text{RST}}$/EN deglitch (ON and OFF) filter time	f_S = 50kHz	28	40		ns
T_{RSTFIL}	Deglitch filter time to reset /FLT		500	650	800	ns
GATE DRIVER STAGE						
I_{OUT}, I_{OUTH}	Peak source current	C_L=0.18µF, f_S=1kHz		–10		A
I_{OUT}, I_{OUTL}	Peak sink current			10		A
R_{OUTH}	Output pull-up resistance	I_{OUT} = –0.1A		2.5		Ω
R_{OUTL}	Output pull-down resistance	I_{OUT} = 0.1A		0.3		Ω
V_{OUTH}	High level output voltage	I_{OUT} = –0.2A, V_{DD}=15V		14.5		V
V_{OUTL}	Low level output voltage	I_{OUT} = 0.2A		60		mV
ACTIVE PULLDOWN						
V_{OUTPD}	Output active pull down on OUT, OUTL	I_{OUTL} or I_{OUT} = 0.1×$I_{OUT(L)(tpy)}$, VDD=OPEN, VEE=COM			2.5	V
INTERNAL ACTIVE MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.7	2.0	2.3	V
V_{CLMPI}	Output low clamp voltage	I_{CLMPI} = 1A		VEE + 0.5		V

---

(1) Current are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise notified.

Electrical Characteristics (continued)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD – COM = 20 V, 18 V or 15 V, COM – VEE = 0 V, 5 V, 8 V or 15 V, C_L = 100 pF, –40°C < T_J < 150°C (unless otherwise noted)(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CLMPI}	Output low clamp current	V_{CLMPI} = 0V, VEE = –2.5V		4		A
R_{CLMPI}	Miller clamp pull down resistance	I_{CLMPI} = 0.2A		0.6		Ω
t_{DCLMPI}	Miller clamp ON delay time	C_L = 1.8nF		25	50	ns
SHORT CIRCUIT CLAMPING						
$V_{CLP\text{-}OUT(H)}$	V_{OUT}–VDD, V_{OUTH}–VDD	OUT = Low, $I_{OUT(H)}$ = 500mA, t_{CLP}=10us		0.9		V
$V_{CLP\text{-}OUT(L)}$	V_{OUT}–VDD, V_{OUTL}–VDD	OUT = High, $I_{OUT(L)}$ = 500mA, t_{CLP}=10us		1.8		V
$V_{CLP\text{-}CLMPI}$	V_{CLMPI}–VDD	OUT = High, I_{CLMPI} = -20mA, t_{CLP}=10us		1.0		V
DESAT PROTECTION						
I_{CHG}	Blanking capacitor charge current	V_{DESAT} = 2.0V	450	500	550	µA
I_{DCHG}	Blanking capacitor discharge current	V_{DESAT} = 6.0V	10	15		mA
V_{DESAT}	Detection Threshold		8.5	9.0	9.5	V
V_{DESATL}	Voltage when OUT(L) = LOW, Reference to COM	I_{DESAT} = 15mA			1	V
$t_{DESATLEB}$	Leading edge blank time			200		ns
$t_{DESATFIL}$	DESAT deglitch filter			150		ns
$t_{DESATOFF}$	DESAT propagation delay to OUT(L) 90%			200		ns
$t_{DESATFLT}$	DESAT to $\overline{FLT}$ low delay			600		ns
INTERNAL SOFT TURN-OFF						
I_{STO}	Soft turn-off current on fault conditions			400		mA
ISOLATED TEMPERATURE SENSE AND MONITOR (AIN–APWM)						
V_{AIN}	Analog sensing voltage range		0.5		4.5	V
I_{AIN}	Internal current source	V_{AIN}=2.5V, -40°C< T_J< 150°C	196	200	206	µA
f_{APWM}	APWM output frequency	V_{AIN}=2.5V	360	400	440	kHz
BW_{AIN}	AIN–APWM bandwidth			10		kHz
D_{APWM}	APWM Dutycycle	V_{AIN} = 0.5V	85	90	95	%
		V_{AIN} = 2.5V	45	50	55	
		V_{AIN} = 4.5V	5	10	15	
$\overline{FLT}$ AND RDY REPORTING						
t_{RDYHLD}	VDD UVLO RDY low minimum holding time		0.55		1	ms
$t_{FLTMUTE}$	Output mute time on fault	Reset fault through $\overline{RST}$/EN	0.55		1	ms
R_{ODON}	Open drain output on resistance	I_{ODON} = 5mA		30		Ω
V_{ODL}	Open drain low output voltage	IODON = 5mA			0.3	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity		150			V/ns

6.10 Switching Characteristics

VCC=5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE = 3V, 5V or 8V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDHL}	Propagation delay time – High to Low			90		ns
t_{PDLH}	Propagation delay time – Low to High			90		
PWD	Pulse width distortion $\lvert t_{PDHL} – t_{PDLH} \rvert$				25	
$t_{sk\text{-}pp}$	Part to Part skew	Rising or Falling Propagation Delay			30	
t_r	Driver output rise time	C_L=10nF			28	
t_f	Driver output fall time	C_L=10nF			24	
f_{MAX}	Maximum switching frequency				1	MHz

6.11 Insulation Characteristics Curves

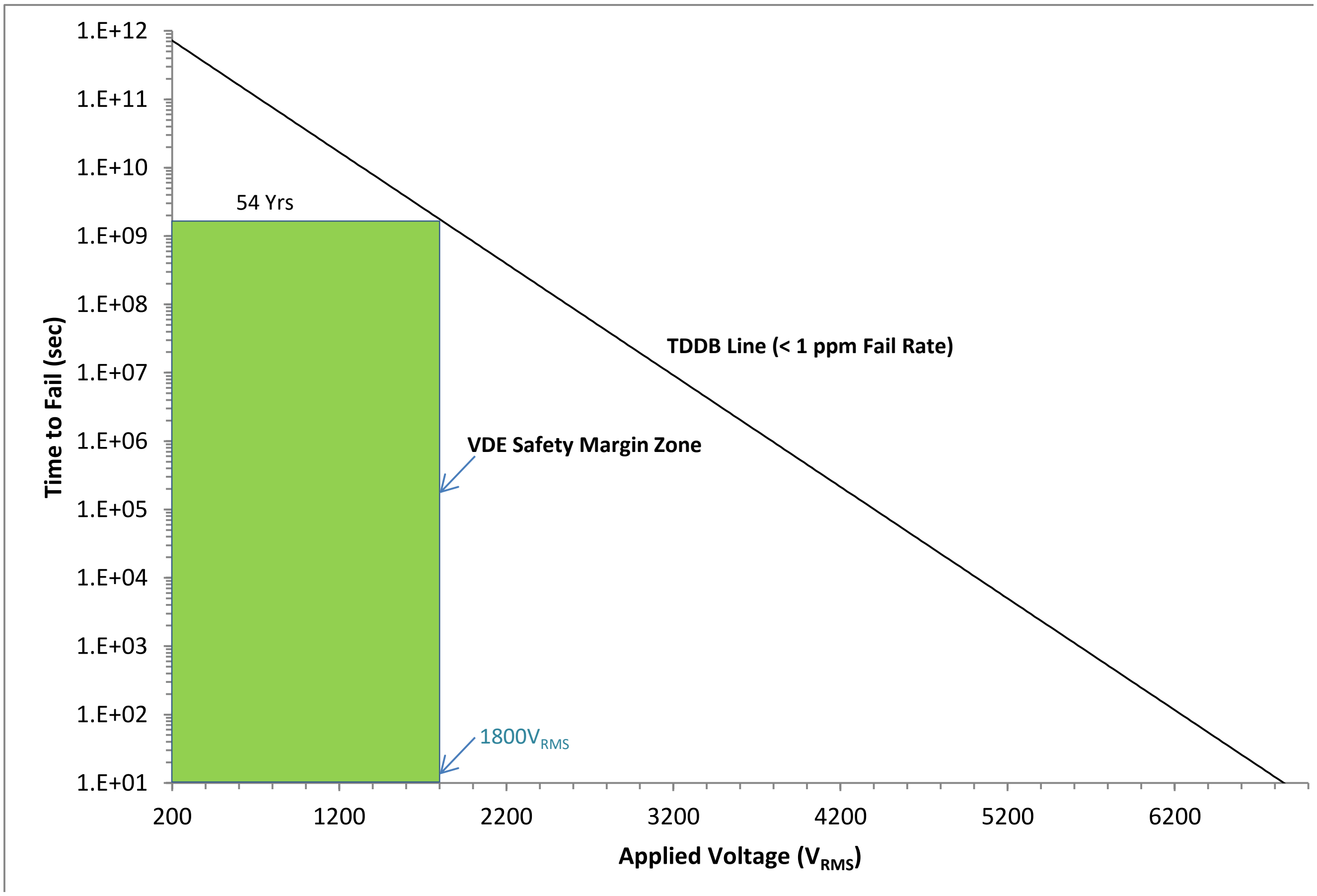


图 1. Reinforced Isolation Capacitor Life Time Projection

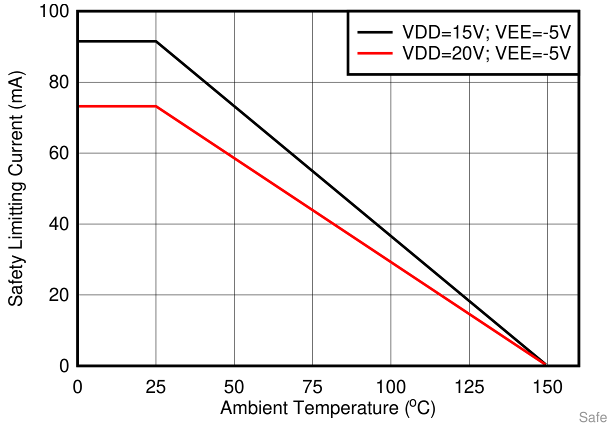


图 2. Thermal Derating Curve for Limiting Current per VDE

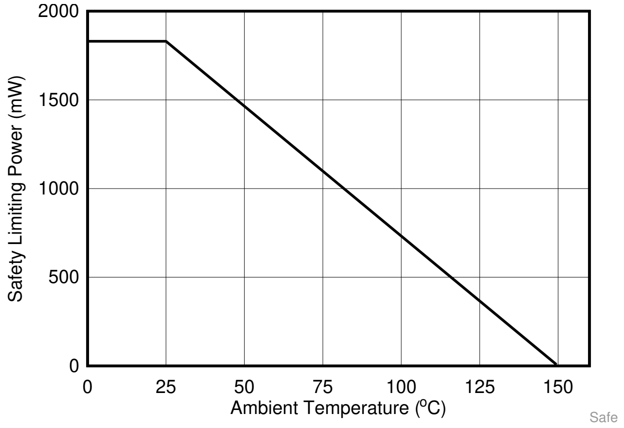


图 3. Thermal Derating Curve for Limiting Power per VDE

6.12 Typical Characteristics

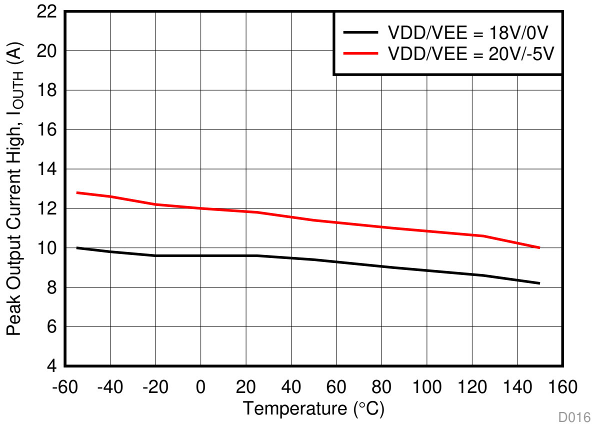


图 4. Output High Drive Current vs. Temperature

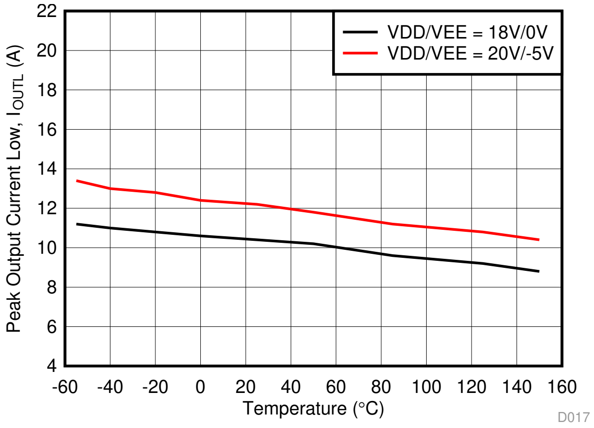
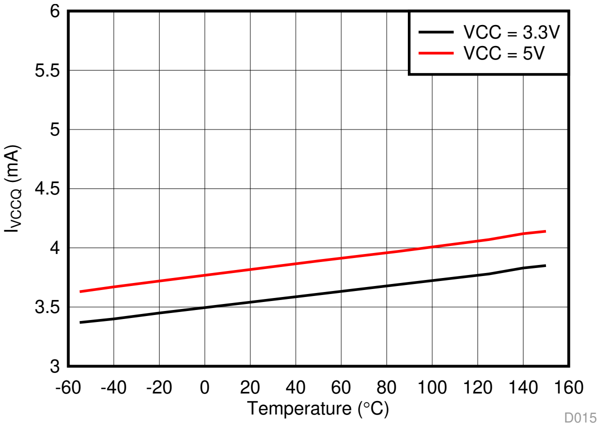
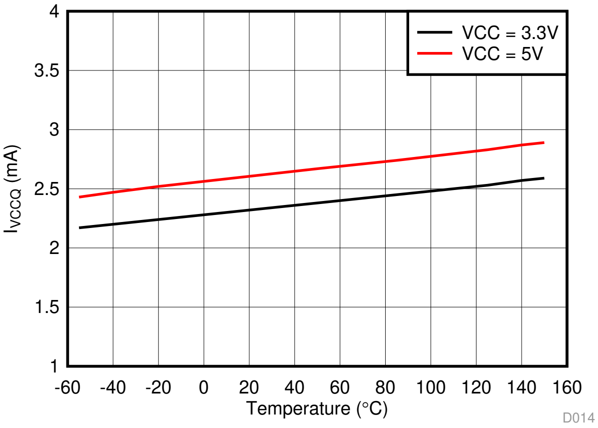


图 5. Output Low Driver Current vs. Temperature



IN+ = High IN- = Low

图 6. I_{VCCQ} Supply Current vs. Temperature



IN+ = Low IN- = Low

图 7. I_{VCCQ} Supply Current vs. Temperature

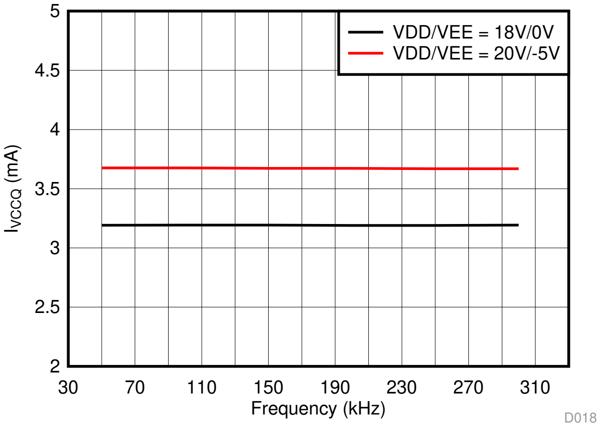
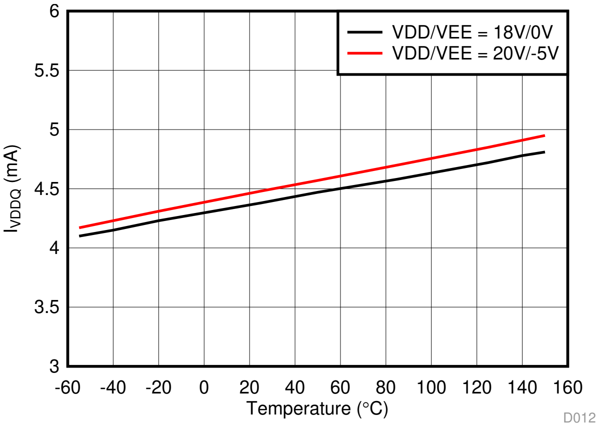


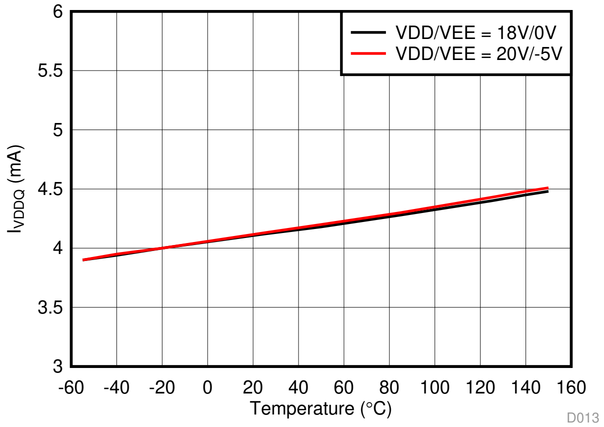
图 8. I_{VCCQ} Supply Current vs. Input Frequency



IN+ = High IN- = Low

图 9. I_{VDDQ} Supply Current vs. Temperature

Typical Characteristics (接下页)



IN+ = Low IN- = Low

图 10. I_{VDDQ} Supply Current vs. Temperature

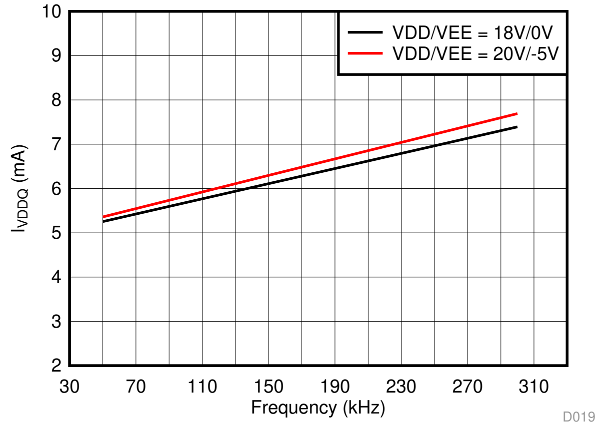


图 11. I_{VDDQ} Supply Current vs. Input Frequency

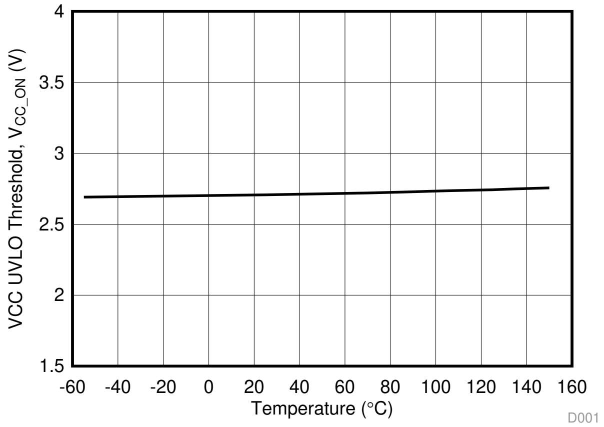


图 12. VCC UVLO vs. Temperature

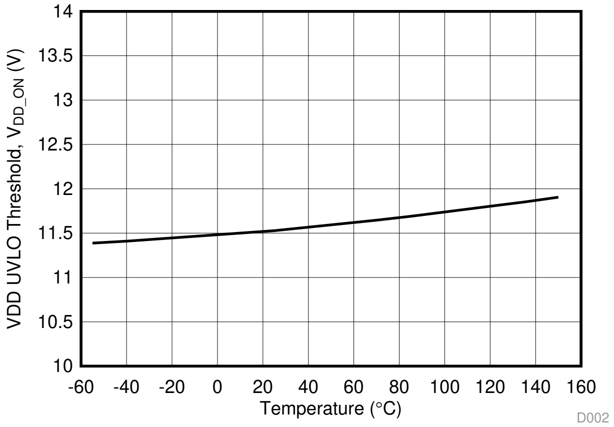
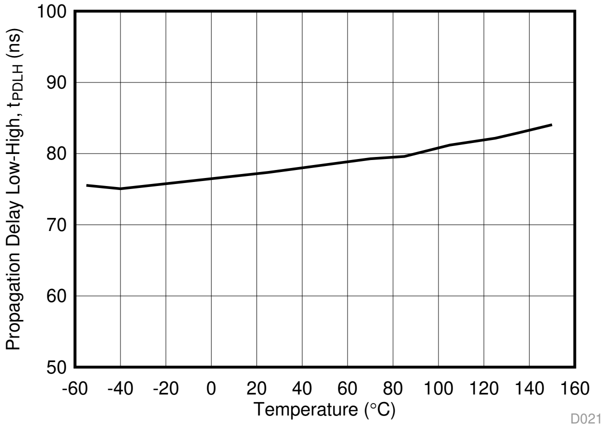


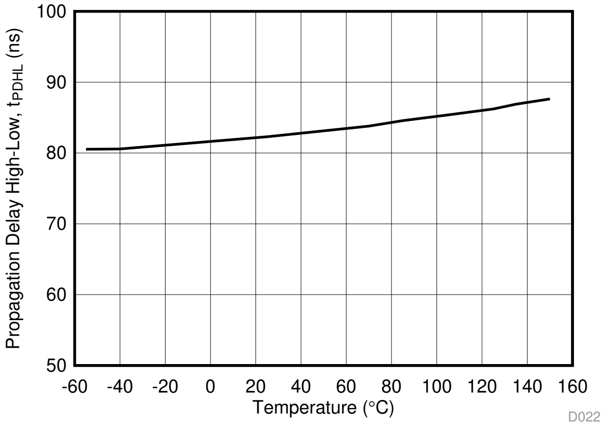
图 13. VDD UVLO vs. Temperature



V_{CC} = 3.3V V_{DD}=18V C_L = 100pF

R_{ON} = 0Ω R_{OFF} = 0Ω

图 14. Propagation Delay t_{PDLH} vs. Temperature

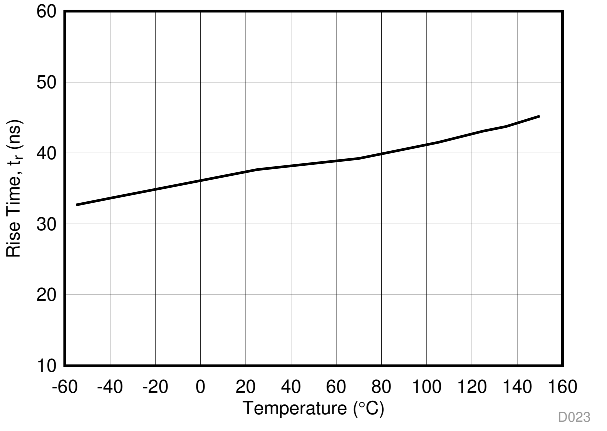


V_{CC} = 3.3V V_{DD}=18V C_L = 100pF

R_{ON} = 0Ω R_{OFF} = 0Ω

图 15. Propagation Delay t_{PDHL} vs. Temperature

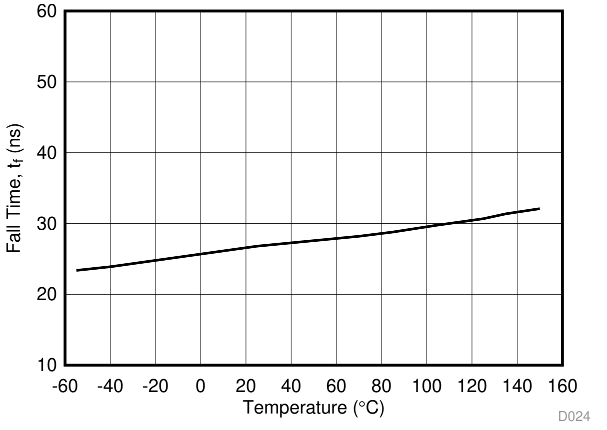
Typical Characteristics (接下页)



V_{CC} = 3.3V V_{DD}=18V C_L = 10nF

R_{ON} = 0Ω R_{OFF} = 0Ω

图 16. t_r Rise Time vs. Temperature



V_{CC} = 3.3V V_{DD}=18V C_L = 10nF

R_{ON} = 0Ω R_{OFF} = 0Ω

图 17. t_f Fall Time vs. Temperature

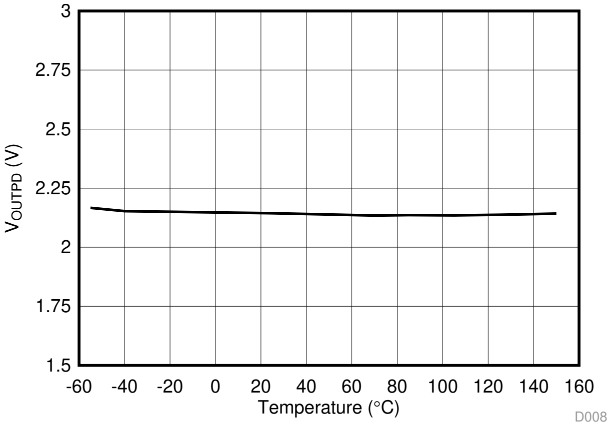


图 18. V_{OUTPD} Output Active Pulldown Voltage vs. Temperature

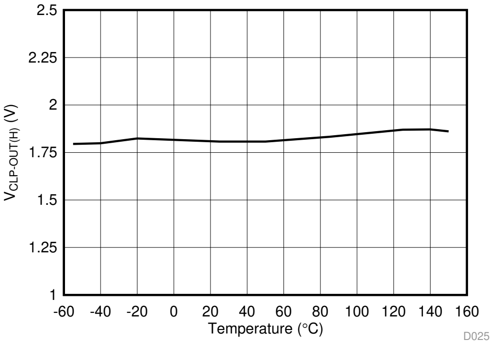


图 19. $V_{CLP-OUT(H)}$ Short Circuit Clamping Voltage vs. Temperature

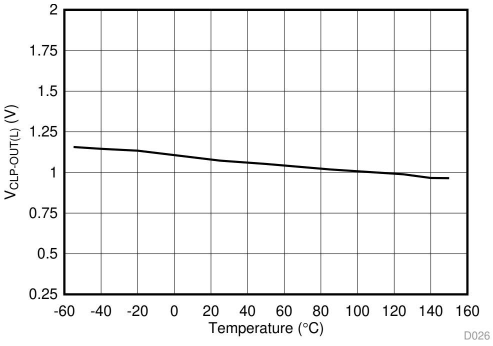


图 20. $V_{CLP-OUT(L)}$ Short Circuit Clamping Voltage vs. Temperature

ADVANCE INFORMATION

7 Parameter Measurement Information

7.1 Propagation Delay

7.1.1 Regular Turn-OFF

图 21 shows the propagation delay measurement for non-inverting configurations. 图 22 shows the propagation delay measurement with the inverting configurations.

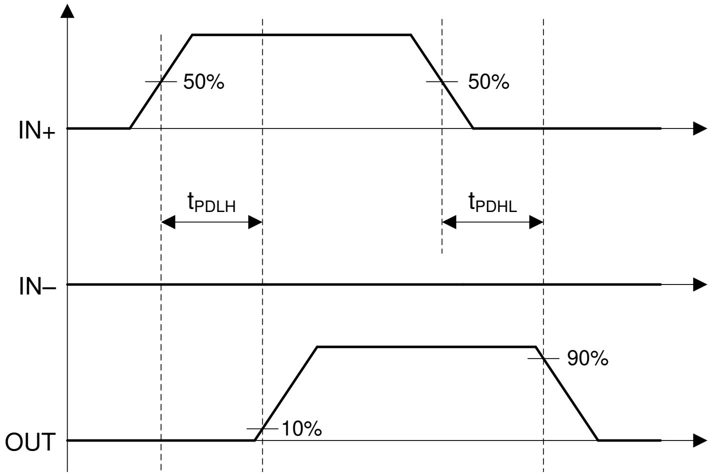


图 21. Non-inverting Logic Propagation Delay Measurement

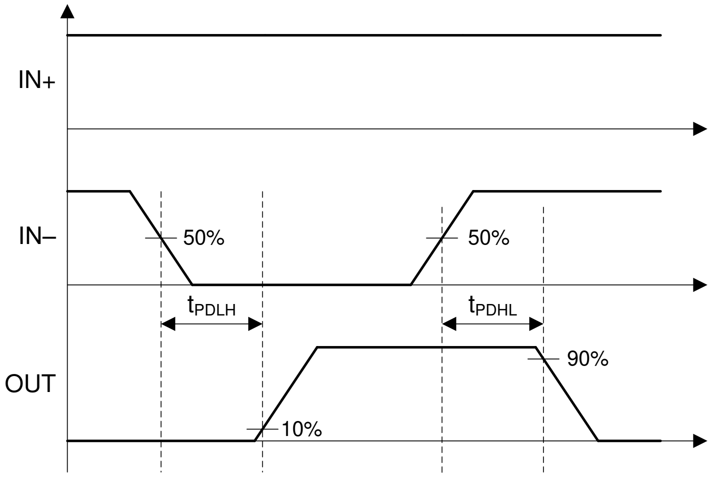


图 22. Inverting Logic Propagation Delay Measurement

7.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, i.e. IN+, IN–, $\overline{RST}$/EN, a 40ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN– PWM pulse is smaller than the input deglitch filter width, T_{INFIL}, there will be no responses on OUT drive signal. 图 23 and 图 24 shows the IN+ pin ON and OFF pulse deglitch filter effect. 图 25 and 图 26 shows the IN– pin ON and OFF pulse deglitch filter effect.

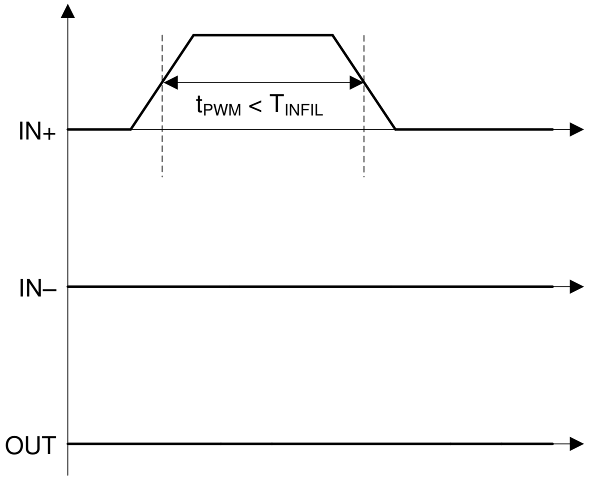


图 23. IN+ ON Deglitch Filter

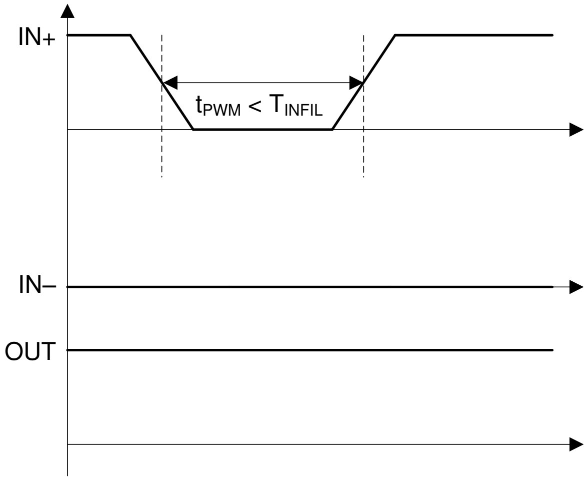


图 24. IN+ OFF Deglitch Filter

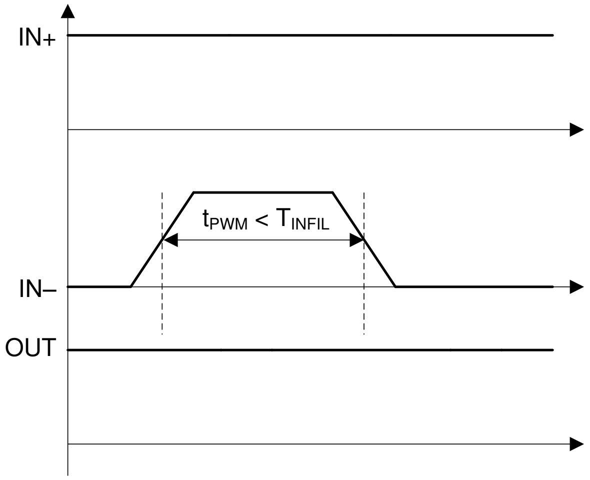


图 25. IN– ON Deglitch Filter

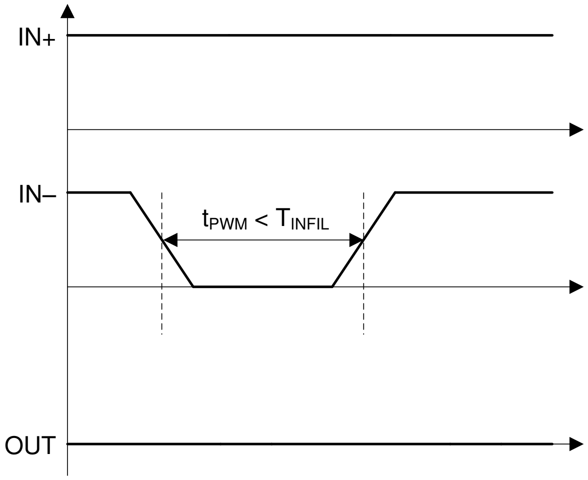


图 26. IN– OFF Deglitch Filter

7.3 Active Miller Clamp

7.3.1 Internal On-chip Active Miller Clamp

For gate driver application with unipolar bias supply or bipolar supply with small negative turn-off voltage, active miller clamp can help add a additional low impedance path to bypass the miller current and prevent the high dV/dt introduced unintentional turn-on through the miller capacitance. 图 27 shows the timing diagram for on-chip internal miller clamp function.

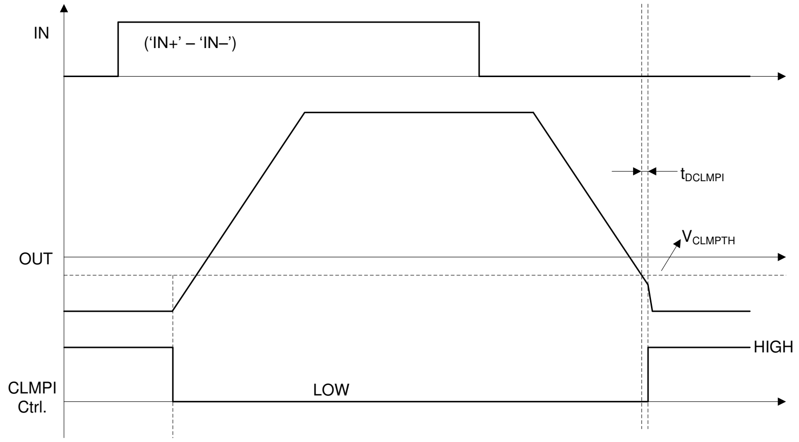


图 27. Timing Diagram for Internal Active Miller Clamp Function

7.4 Under Voltage Lockout (UVLO)

UVLO is one of the key protection features designed to protect the system in case of bias supply failures on VCC — primary side power supply, and VDD — secondary side power supply.

7.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. 图 28 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

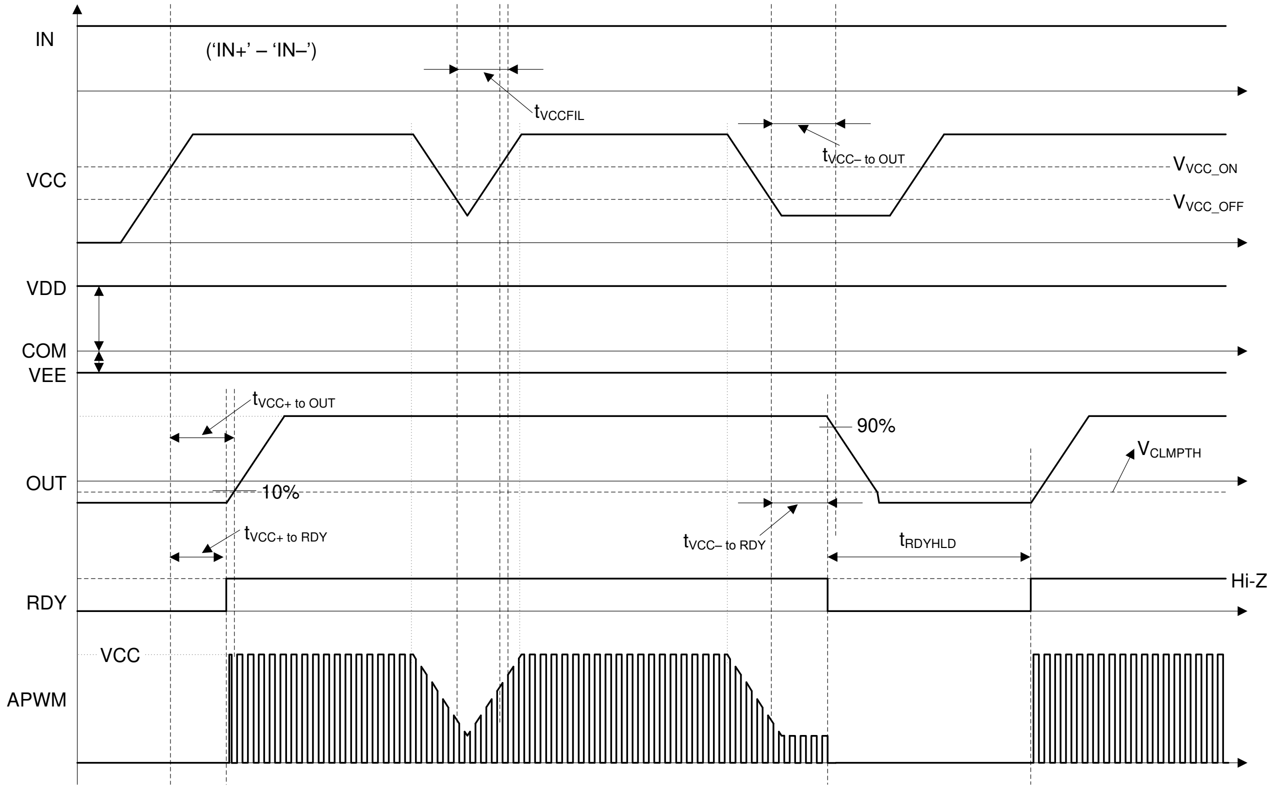


图 28. VCC UVLO Protection Timing Diagram

Under Voltage Lockout (UVLO) (接下页)

7.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. 图 29 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

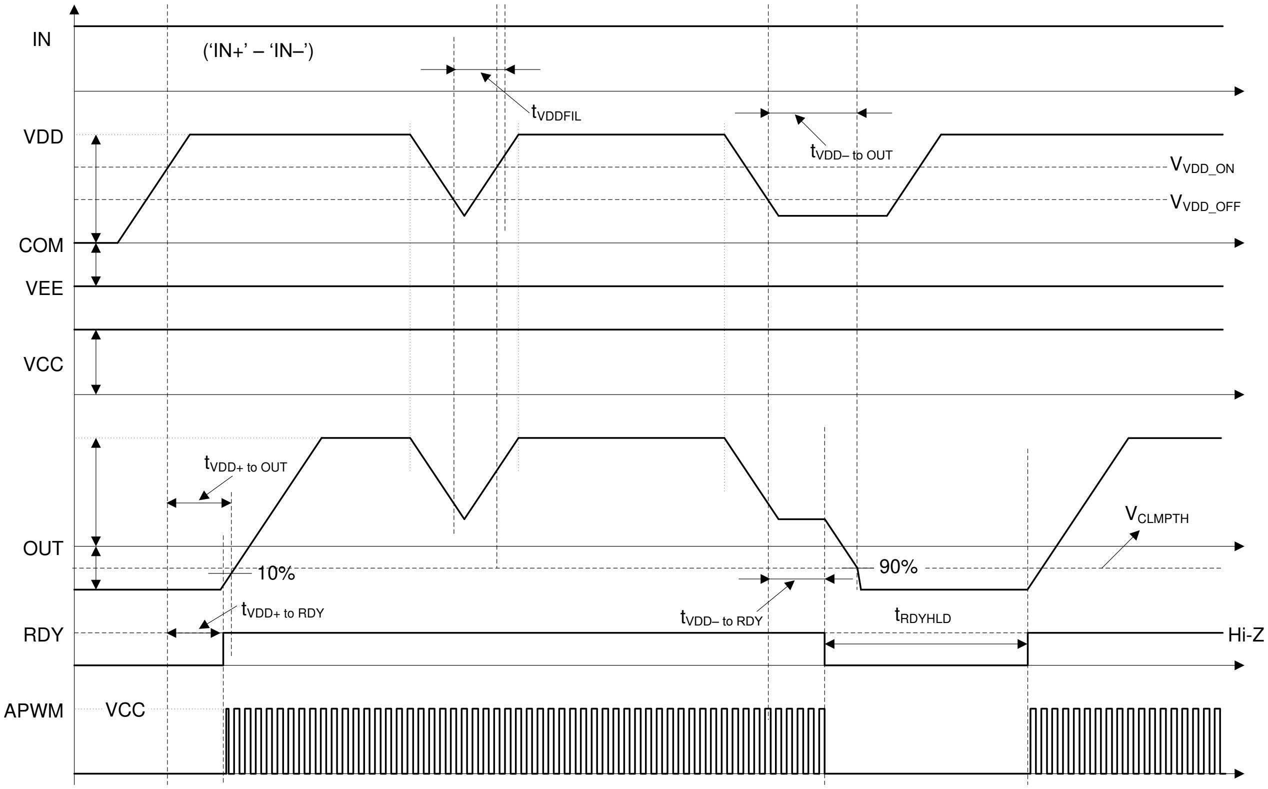


图 29. VDD UVLO Protection Timing Diagram

7.5 Desaturation (DESAT) Protection

7.5.1 DESAT Protection with Soft Turn-OFF

DESAT function is used to detect V_{DS} for SiC-MOSFETs or V_{CE} for IGBTs under over current conditions. 图 30 shows the timing diagram of DESAT operation with soft turn-off during the turning on transition.

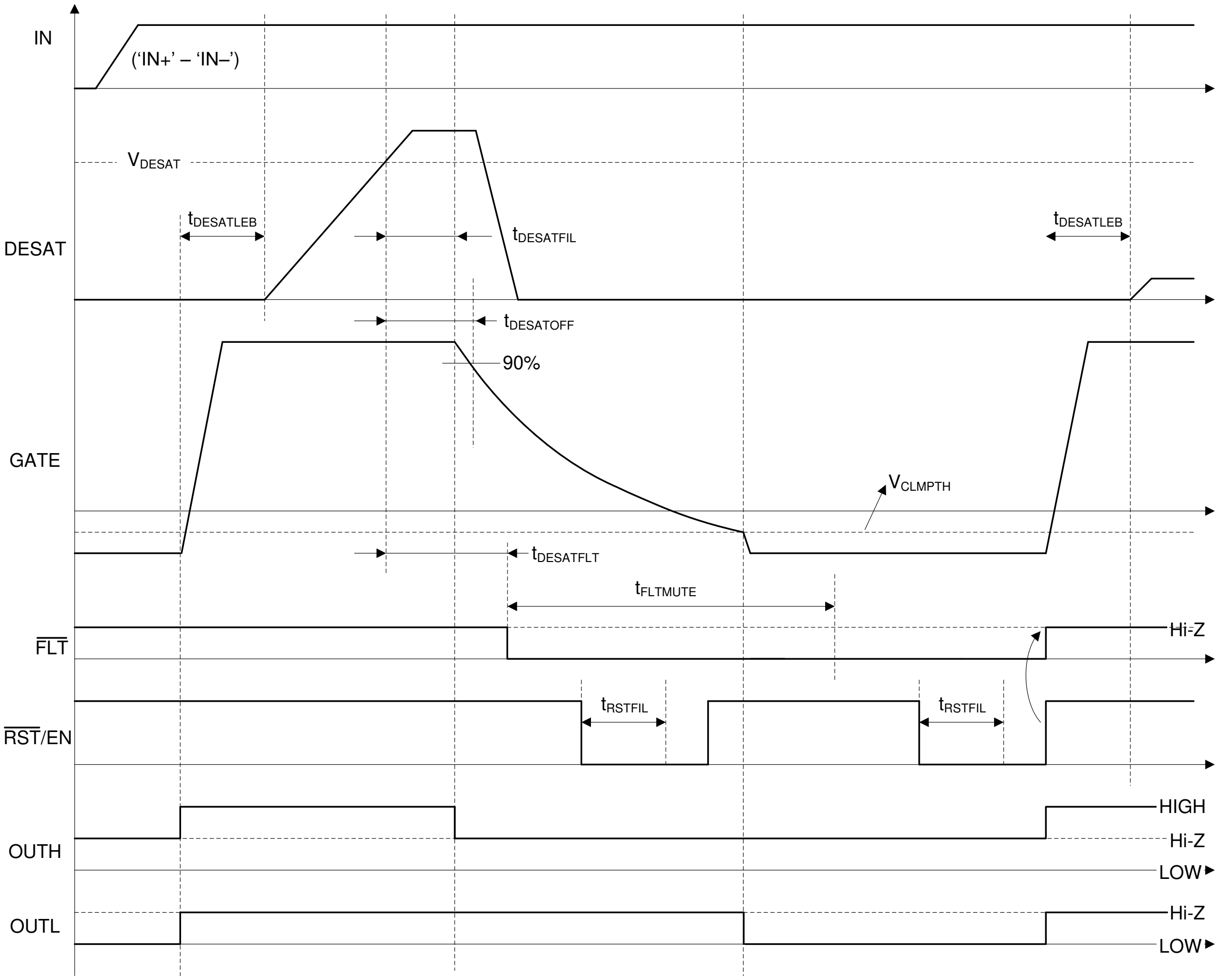


图 30. DESAT Protection with Soft Turn-OFF During Turn-on Transition

Desaturation (DESAT) Protection (接下页)

图 31 shows the timing diagram of DESAT protection while the power device is already turned on.

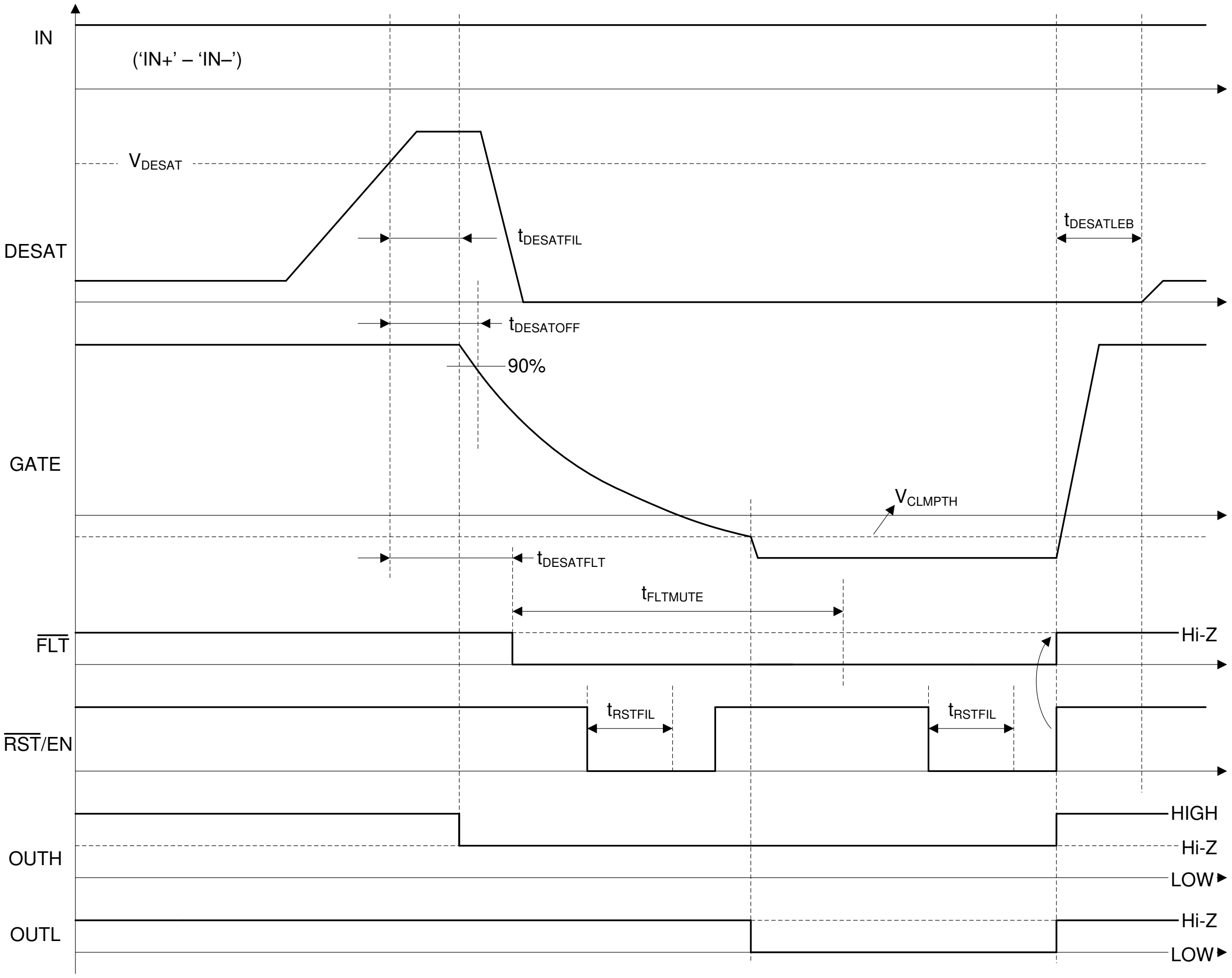


图 31. DESAT Protection with Soft Turn-OFF While Power Device is ON

8 Detailed Description

8.1 Overview

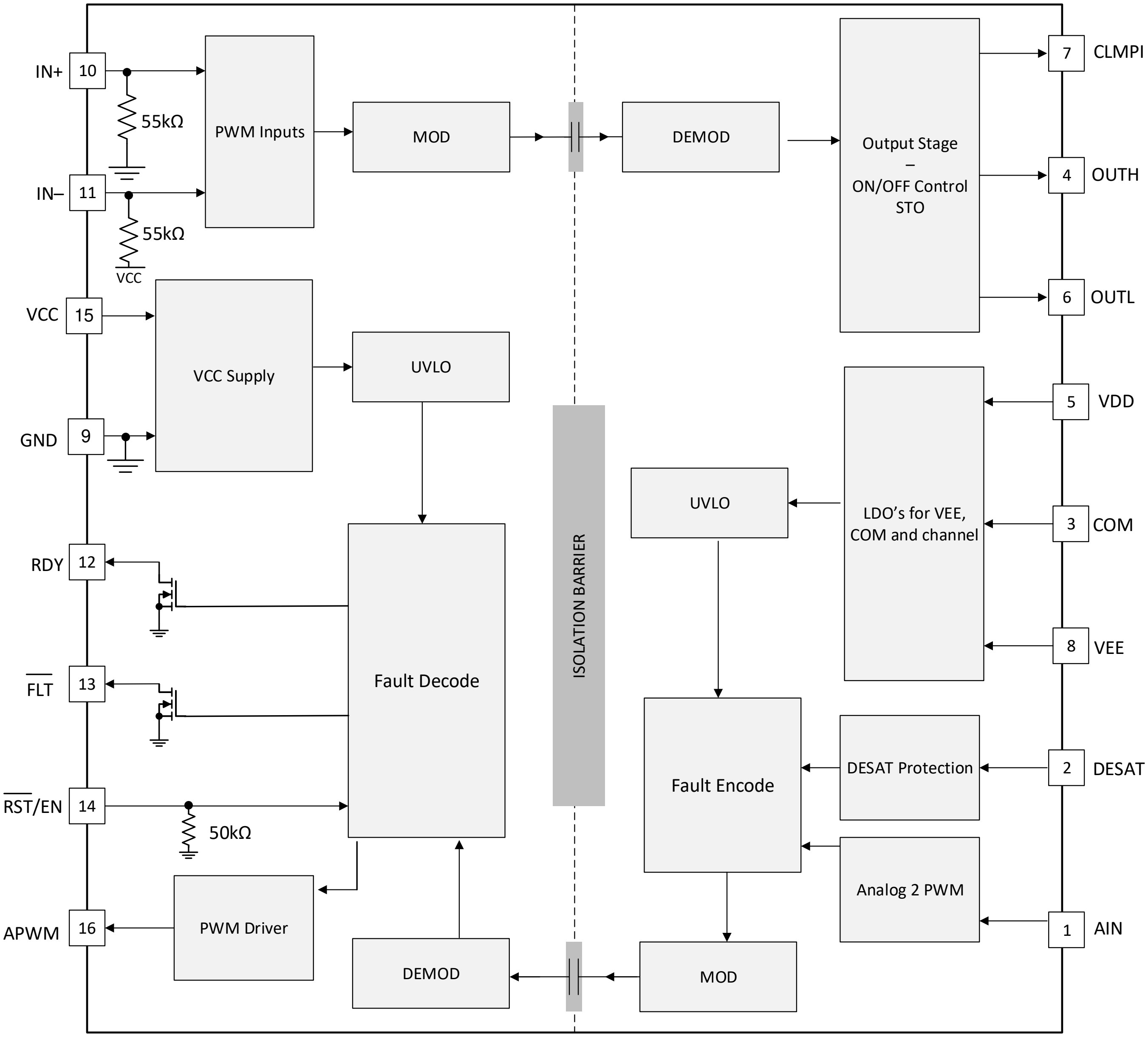
The UCC21750-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, etc. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

The ±10A peak sink and source current of UCC21750-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The input side is isolated with the output side with a reinforced isolation barrier based on capacitive isolation technology. The device can support up to 1.5-kV_{RMS} working voltage, 12.8-kV_{PK} surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss. While the 150V/ns minimum CMTI guarantees the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12V output side power supply UVLO is suitable for switches with gate voltage ≥ 15V. The active miller clamp feature prevents the false turn on causing by miller capacitance during fast switching. The device has the state-of-art DESAT detection time, and fault reporting function to the low voltage side DSP/MCU. The soft turn off is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The isolated analog to PWM sensor can be used as switch temperature sensing, DC bus voltage sensing, auxiliary power supply sensing, etc. The PWM signal can be fed directly to DSP/MCU or through a low-pass-filter as an analog signal.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3V to 5.5V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13V to 33V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

Feature Description (接下页)

8.3.2 Driver Stage

UCC21750-Q1 has ±10A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. UCC21750-Q1 can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10A. The driver features an important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in LOW state. The split output of the driver stage is depicted in . The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance R_{NMOS} is the same as R_{OL}. The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the miller plateau region of the power semiconductor turn-on transient. The R_{OH} in represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than R_{OH}. Since the pull-up N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pull-up N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3V below VDD voltage. The effective resistance of the hybrid pull-up structure during this period is about 2 x R_{OL} . Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pull-up impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pull-down structure of the driver stage is implemented solely by a pull-down N-Channel MOSFET. The on-resistance of the N-Channel MOSFET R_{OL} can be found in the . This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pull-down impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the miller effect.

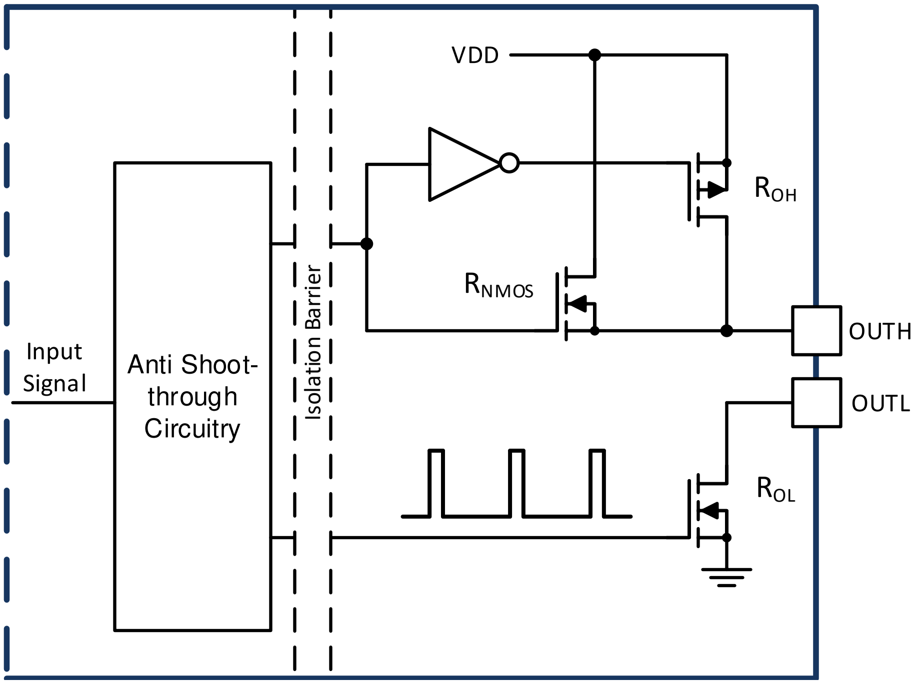


图 32. Gate Driver Output Stage

Feature Description (接下页)

8.3.3 VCC and VDD Undervoltage Lockout (UVLO)

UCC21750-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. UCC21750-Q1 implements 12V threshold voltage of VDD UVLO, with 800mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in 图 28, and 图 29. The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good. The AIN-APWM function stops working during the UVLO status. The APWM pin on the input side will be held LOW.

8.3.4 Active Pulldown

UCC21750-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.

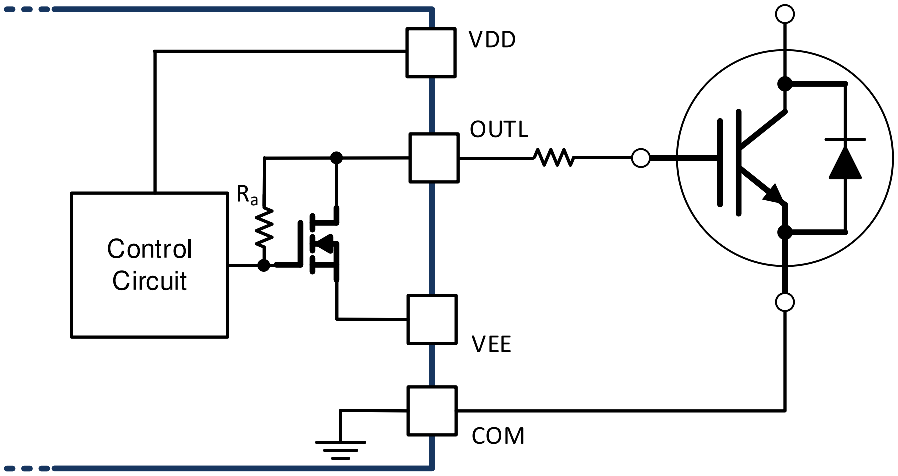


图 33. Active Pulldown

8.3.5 Short Circuit Clamping

During short circuit condition, the miller capacitance can cause a current sinking to the OUTH/OUTL/CLMPI pin due to the high dV/dt and boost the OUTH/OUTL/CLMPI voltage. The short circuit clamping feature of UCC21750-Q1 can clamp the OUTH/OUTL/CLMPI pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL/CLMPI to VDD.

Feature Description (接下页)

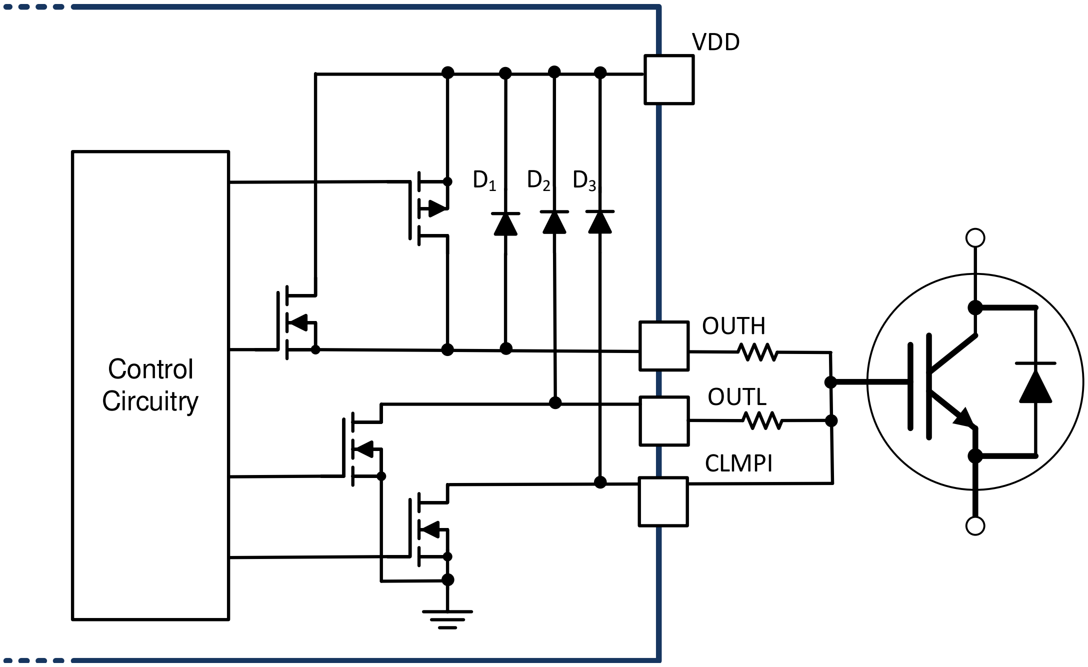


图 34. Short Circuit Clamping

8.3.6 Internal Active Miller Clamp

Active miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. In applications which the device can be in synchronous rectifier mode, the body diode conducts the current during the deadtime while the device is in OFF state, the drain-source or collector-emitter voltage remains the same and the dV/dt happens when the other power semiconductor of the phase leg turns on. The low internal pull-down impedance of UCC21750-Q1 can provide a strong pulldown to hold the OUTL to VEE. However, external gate resistance is usually adopted to limit the dV/dt. The miller effect during the turn on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boost the gate-source or gate-emitter voltage. If the voltage on V_{GS} or V_{GE} is higher than the threshold voltage of the power semiconductor, a shoot through can happen and cause catastrophic damage. The active miller clamp feature of UCC21750-Q1 drives an internal MOSFET, which connects to the device gate. The MOSFET is triggered when the gate voltage is lower than V_{CLMPTH}, which is 2V above VEE, and creates a low impedance path to avoid the false turn on issue.

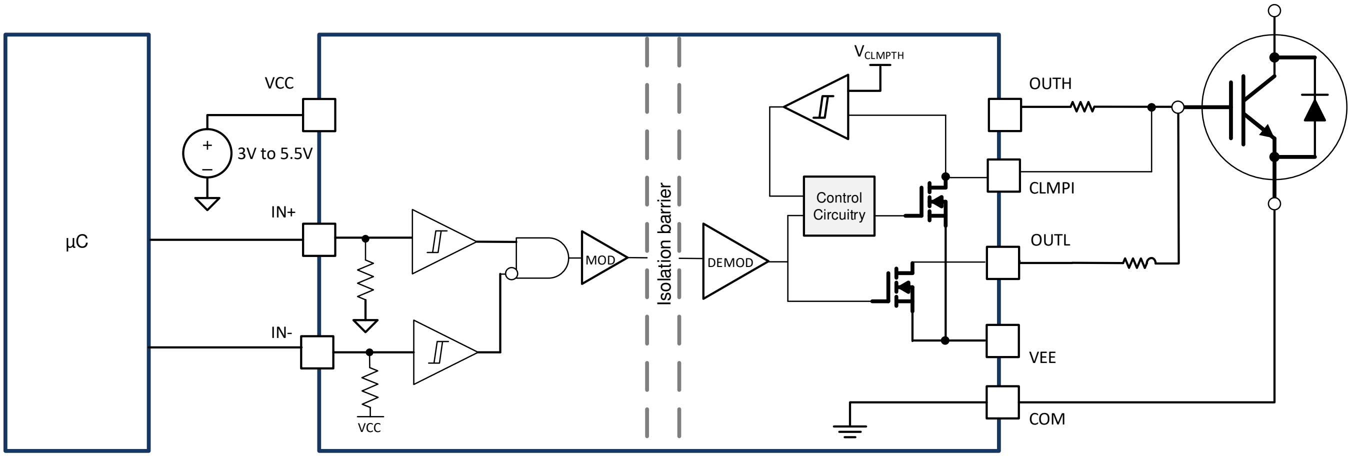


图 35. Active Miller Clamp

Feature Description (接下页)

8.3.7 Overcurrent and Short Circuit Protection

The UCC21750-Q1 implements a fast overcurrent and short circuit protection feature to protect the IGBT module from catastrophic breakdown during fault. The DESAT pin of the device has a typical 9V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the DESAT pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of DESAT pin when the power semiconductor is turned off. UCC21750-Q1 features a 200ns internal leading edge blanking time after the OUTH switches to high state. The internal current source is activated to charge the external blanking capacitor after the internal leading edge blanking time. The typical value of the internal current source is 500μA.

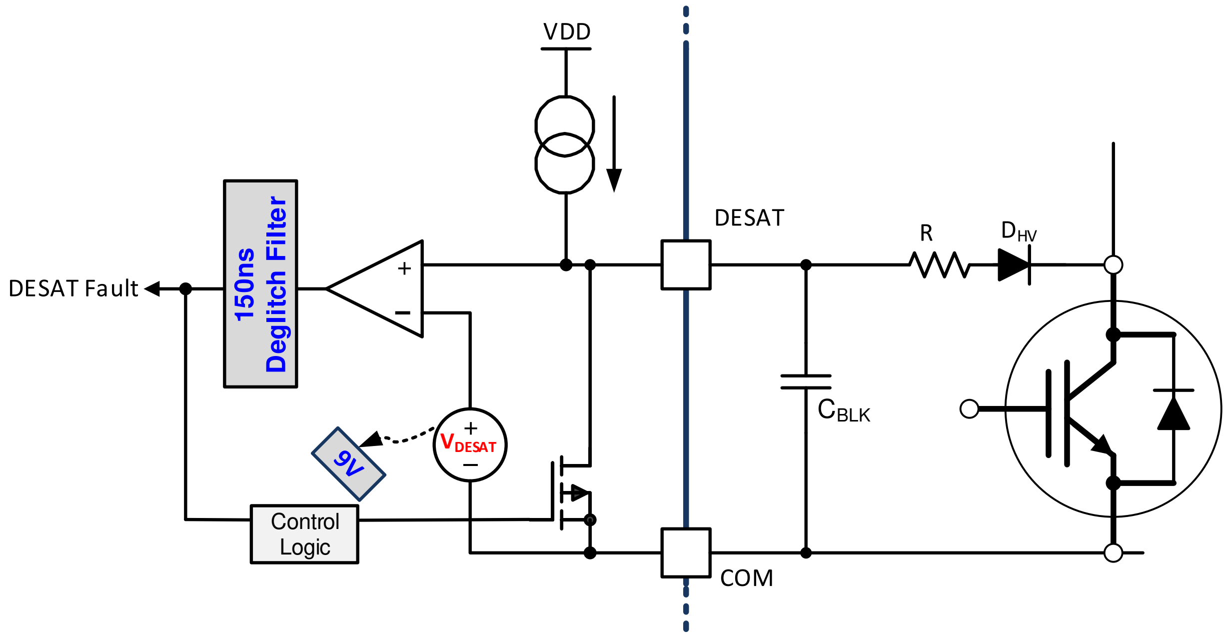


图 36. **Overcurrent and Short Circuit Protection**

8.3.8 Soft Turn-off

UCC21750-Q1 initiates a soft turn-off when the overcurrent and short circuit protection is triggered. When the overcurrent and short circuit fault happens, the IGBT transits from the active region to the desaturation region very fast. The channel current is controlled by the gate voltage and decreasing in a soft manner, thus the overshoot of the IGBT is limited and prevents the overvoltage breakdown. There is a tradeoff between the overshoot voltage and short circuit energy. The turn off speed needs to be slow to limit the overshoot voltage, but the shutdown time should not be too long that the large energy dissipation can breakdown the device. The 400mA soft turn off current of UCC21750-Q1 makes sure the power switches is safely turned off during short circuit events. The timing diagram of soft turn-off shows in 图 30.

Feature Description (接下页)

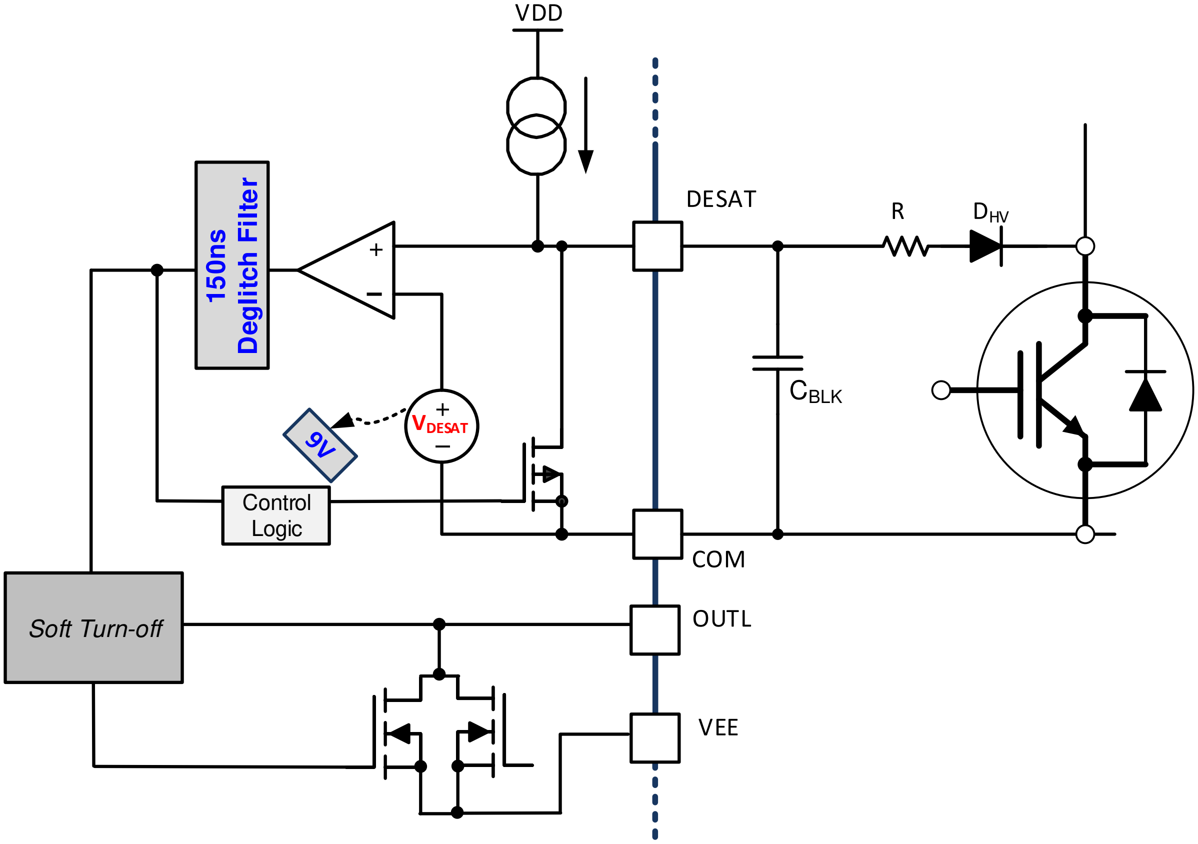


图 37. 2-Level Turn-off

8.3.9 Fault ($\overline{\text{FLT}}$, Reset and Enable ($\overline{\text{RST}}$/EN)

The $\overline{\text{FLT}}$ pin of UCC21750-Q1 is open drain and can report a fault signal to the DSP/MCU when the overcurrent and short circuit fault is detected through DESAT pin. The $\overline{\text{FLT}}$ pin is pulled down to GND, and is held in low state unless a reset signal is received from $\overline{\text{RST}}$/EN. The device has a fault mute time $t_{FLTMUTE}$, within which the device ignores any reset signal.

The $\overline{\text{RST}}$/EN is pulled down internally. The device is disabled by default if the $\overline{\text{RST}}$/EN pin is floating. The pin has two purposes:

- Resets the overcurrent and short circuit fault signaled on $\overline{\text{FLT}}$ pin. The $\overline{\text{RST}}$/EN pin is active low, if the pin is set and held in low state for more than t_{RSTFIL}, the fault signal is reset and$\overline{\text{FLT}}$ is reset back to the high impedance status at the rising edge of $\overline{\text{RST}}$/EN pin.
- Enable and shutdown the device. If the $\overline{\text{RST}}$/EN pin is pulled low, the driver is disabled and shut down by the regular turn off. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

8.3.10 Isolated Analog to PWM Signal Function

The UCC21750-Q1 features an isolated analog to PWM signal function from AIN to APWM pin, which allows the isolated temperature sensing, high voltage dc bus voltage sensing, etc. An internal current source I_{AIN} in AIN pin is implemented in the device to bias an external thermal diode or temperature sensing resistor. The UCC21750-Q1 encodes the voltage signal V_{AIN} to a PWM signal, passing through the reinforced isolation barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.6V to 4.5V, and the corresponding duty cycle of the APWM output ranges from 88% to 10%. The duty cycle increases

Feature Description (接下页)

linearly from 10% to 88% while the AIN voltage decreases from 4.5V to 0.6V. This corresponds to the temperature coefficient of the negative temperature coefficient (NTC) resistor and thermal diode. When AIN is floating, the AIN voltage is 5V and the APWM operates at 400kHz with approximately 10% duty cycle. The accuracy of the duty cycle is ±5% across temperature without one time calibration. The accuracy can be improved to ±2% with calibration. The accuracy of the internal current source I_{AIN} is 3% across temperature.

The isolated analog to PWM signal feature can also support other analog signal sensing, such as the high voltage dc bus voltage, etc. The internal current source I_{AIN} should be taken into account when designing the potential divider if sensing a high voltage.

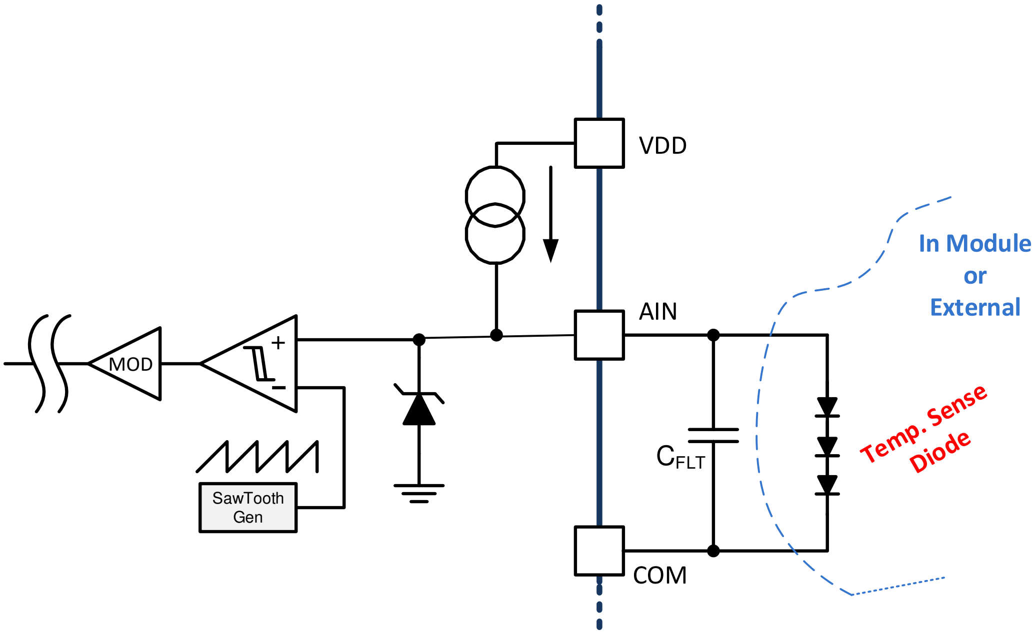


图 38. Isolated Analog to PWM Signal

8.4 Device Functional Modes

lists the device function.

表 1. Function Table

Input							Output				
VCC	VDD	VEE	IN+	IN-	$\overline{\text{RST}}$/EN	AIN	RDY	$\overline{\text{FLT}}$	OUTH/ OUTL	CLMPI	APWM
PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PD	PU	PU	X	X	X	X	HiZ	HiZ	Low	Low	Low
PU	PU	PU	X	X	Low	X	HiZ	HiZ	Low	Low	Low
PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ	HiZ
PU	PU	Open	X	X	X	X	Low	HiZ	Low	Low	Low
PU	PU	PU	Low	X	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	X	High	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	High	High	High	X	HiZ	HiZ	Low	Low	P*

PU: Power Up (VCC ≥ 2.85V, VDD ≥ 13.1V, VEE ≤ 0V); PD: Power Down (VCC ≤ 2.35V, VDD ≤ 9.9V); X: Irrelevant; P*: PWM Pulse; HiZ: High Impedance

9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC21750-Q1 device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kVPK surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 2121V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and etc. The device can drive the high power SiC MOSFET module, IGBT module or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. UCC21750-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3V to 5V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13V to 33V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

UCC21750-Q1 device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The semiconductor is shutdown when the fault is detected and FLTb pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the $\overline{\text{RST}}$/EN pin.
- Soft turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Analog signal seensing with isolated analog to PWM signal feature. This feature allows the device to sense the temperature of the semiconductor from the thermal diode or temperature sensing resistor, or dc bus voltage with resistor divider. A PWM signal is generated on the low voltage side with reinforced isolated from the high voltage side. The signal can be fed back to the microcontroller for the temperature monitoring, voltage monitoring and etc.
- The active miller clamp feature protects the power semiconductor from false turn on.
- Enable and disable function through the RSTb/EN pin.
- Short circuit clamping.
- Active pulldown.

9.2 Typical Application

shows the typical application of a half bridge using two UCC21750-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle's battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

Typical Application (接下页)

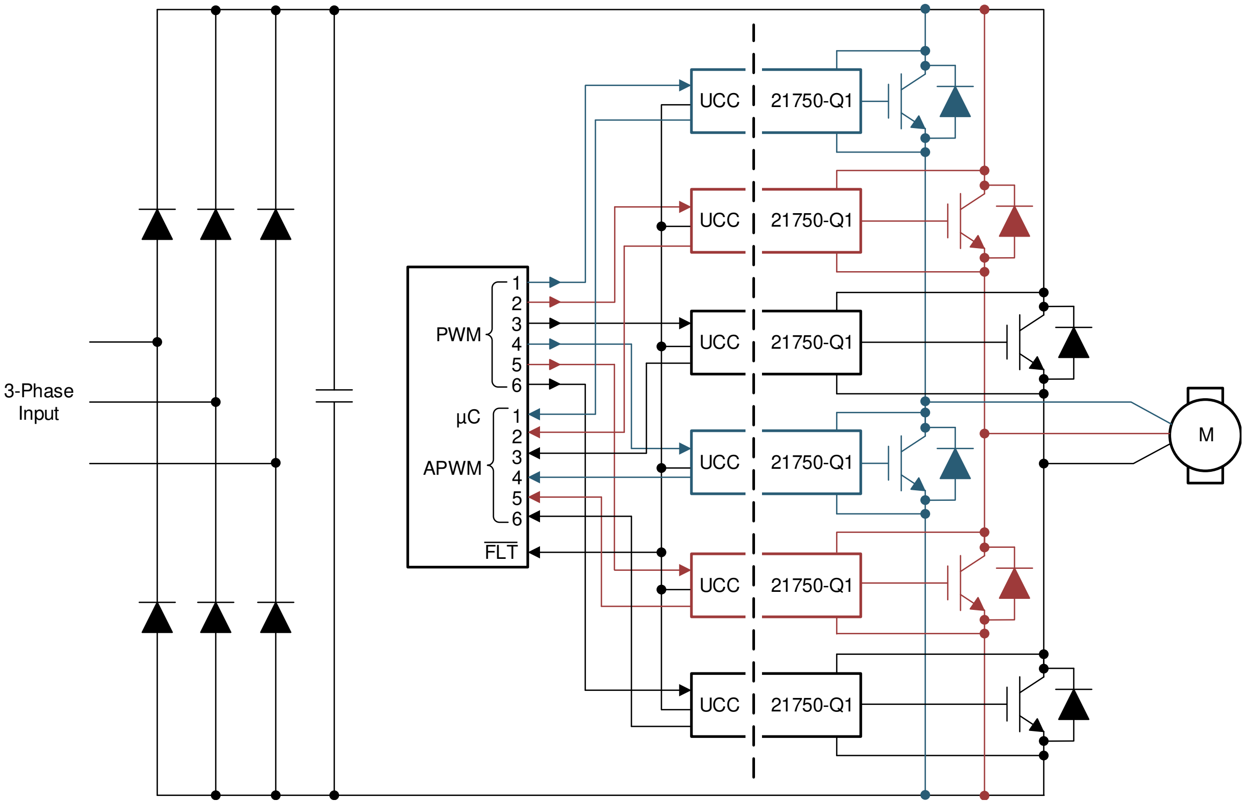


图 39. Typical Application Schematic

9.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of UCC1750-Q1 through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing and etc.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are show in .

表 2. Design Parameters

Parameter	Value
Input Supply Voltage	5V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15V
Negative Output Voltage VEE	-5V
DC Bus Voltage	800V
Peak Drain Current	300A
Switching Frequency	50kHz
Switch Type	IGBT Module

9.2.2 Detailed Design Procedure

9.2.2.1 *Input filters for IN+, IN- and $\overline{\text{RST}}$/EN*

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of UCC21750-Q1, the dV/dt can be high, especially for SiC MOSFET. Noise can not only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the non-ideal PCB layout and coupled capacitance.

UCC21750-Q1 features a 40ns internal deglitch filter to IN+, IN- and $\overline{\text{RST}}$/EN pin. Any signal less than 40ns can be filtered out from the input pins. For noisy systems, external low pass filter can be added externally to the input pins. Adding low pass filters to IN+, IN- and $\overline{\text{RST}}$/EN pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN- and $\overline{\text{RST}}$/EN pins should not be floating. IN- should be tied to GND if only IN+ is used for non-inverting input to output configuration. The purpose of the low pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

9.2.2.2 *PWM Interlock of IN+ and IN-*

UCC21750-Q1 features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in , the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in , the PWM_T is the PWM signal to top side switch, the PWM_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom side gate driver, the PWM_B signal is given to the IN+ pin, while PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

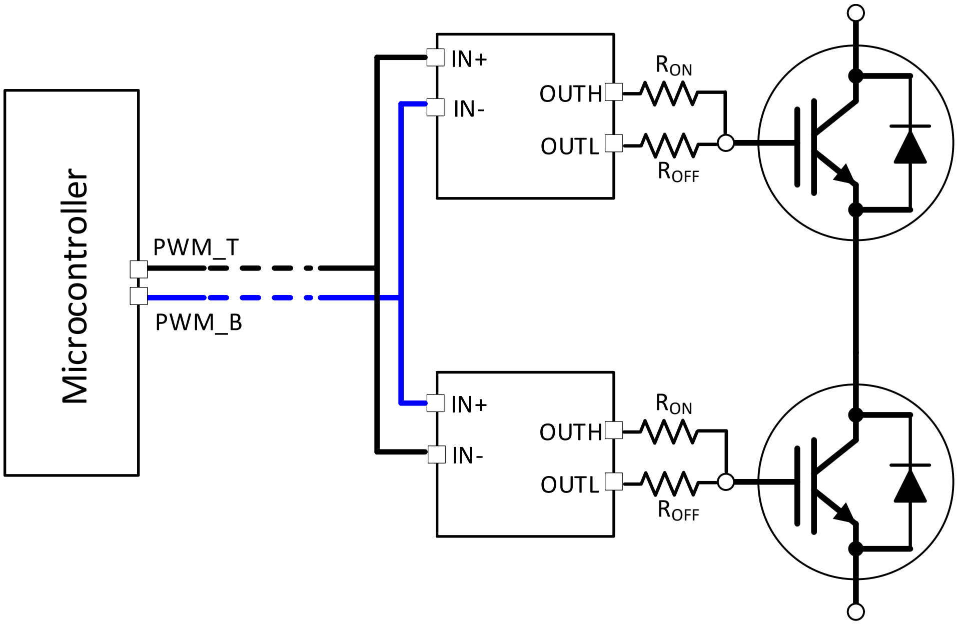


图 40. PWM Interlock for a Half Bridge

9.2.2.3 *$\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN Pin Circuitry*

Both $\overline{\text{FLT}}$ and RDY pin are open-drain output. The $\overline{\text{RST}}$/EN pin has 50kΩ internal pulldown resistor, so the driver is in OFF status if the $\overline{\text{RST}}$/EN pin is not pulled up externally. A 5kΩ resistor can be used as pullup resistor for the $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, low pass filters can be added between the $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN pins and the microcontroller. A filter capacitor between 100pF to 300pF can be added.

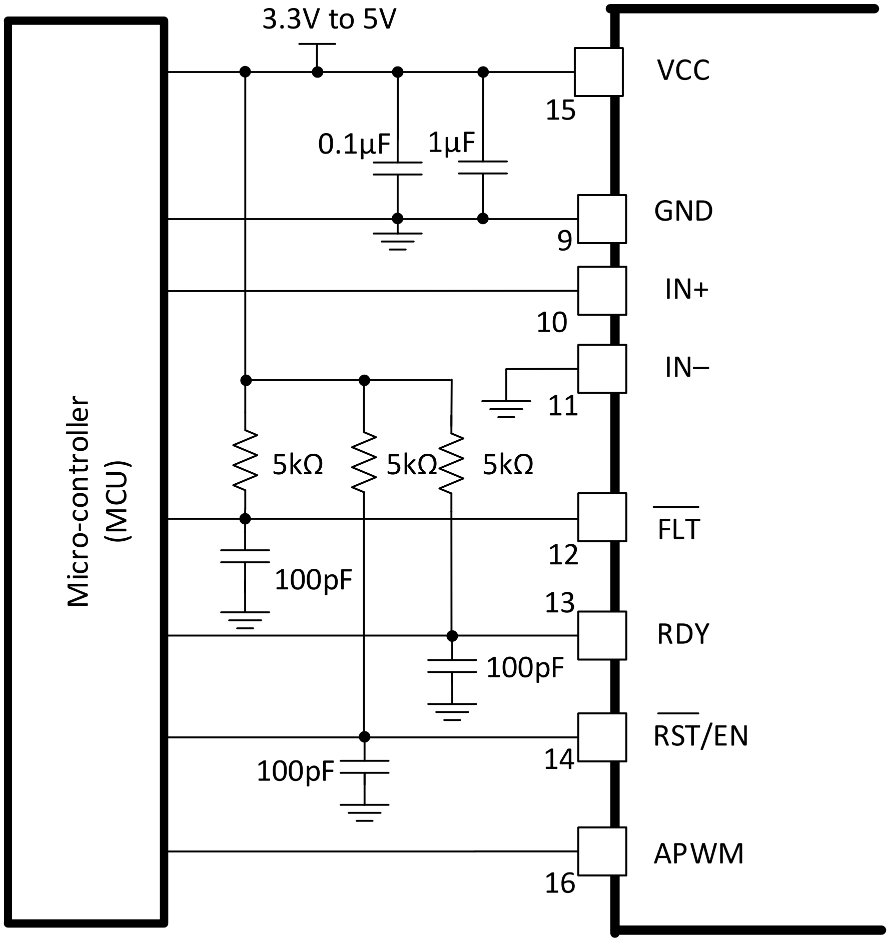


图 41. $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN Pins Circuitry

9.2.2.4 $\overline{\text{RST}}$/EN Pin Control

$\overline{\text{RST}}$/EN pin has two functions. It can be used to enable and shutdown the outputs of the driver, and reset the fault signaled on the $\overline{\text{FLT}}$ pin. $\overline{\text{RST}}$/EN pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. With a 50kΩ pulldown resistor existing, the driver is disabled by default.

When the driver is latched after overcurrent or short circuit fault is detected, the $\overline{\text{FLT}}$ pin and output are latched low and need to be reset by$\overline{\text{RST}}$/EN pin. $\overline{\text{RST}}$/EN pin is active low. The microcntroller needs to send a signal to $\overline{\text{RST}}$/EN pin after the fault mute time $t_{FLTMUTE}$ to reset the driver. This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to $\overline{\text{RST}}$/EN pin, so the microcontroller does not need to generate another control signal to reset the driver. If non-inverting input IN+ is used, then IN+ can be tied to $\overline{\text{RST}}$/EN pin. If inverting input IN- is used, then a NOT logic is needed between the inverting PWM signal from the microcontroller and the $\overline{\text{RST}}$/EN pin. In this case, the driver can be reset in every switching cycle without an extra control signal from microcontroller to $\overline{\text{RST}}$/EN pin.

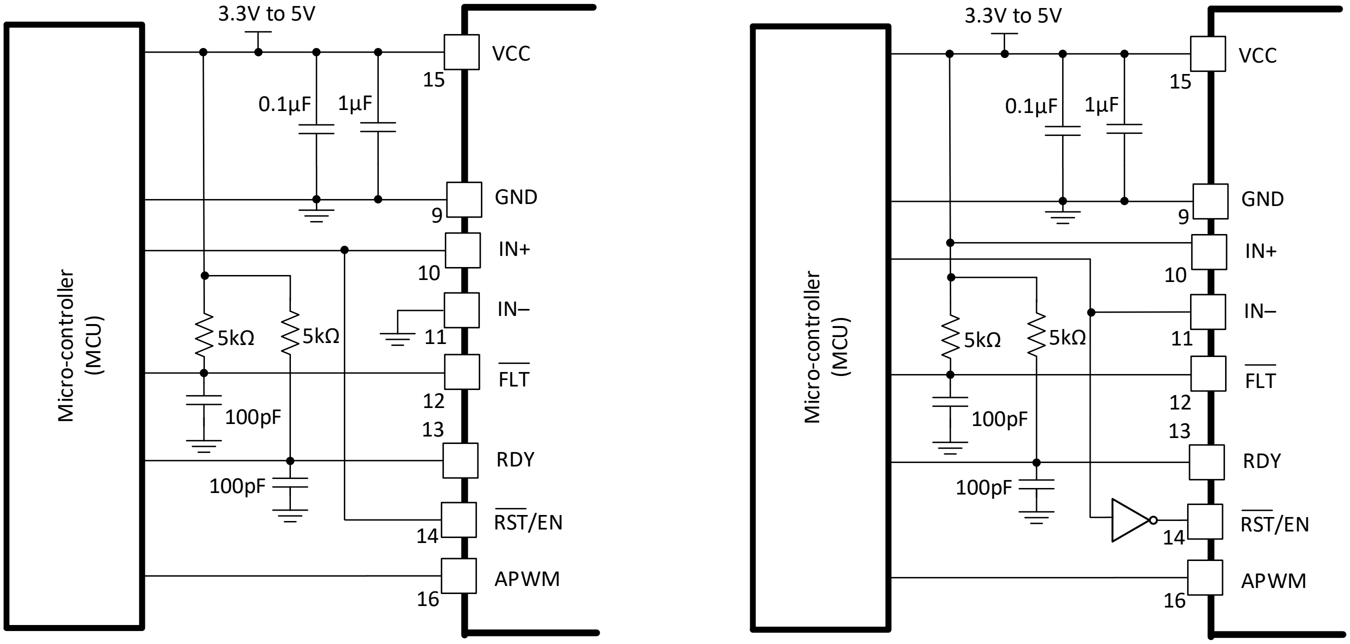


图 42. **Automatic Reset Control**

9.2.2.5 *Turn on and turn off gate resistors*

UCC21750-Q1 features split outputs OUTH and OUTL, which enables the independent control of the turn on and turn off switching speed. The turn on and turn off resistance determine the peak source and sink current, which controls the switching speed in turn. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink current are calculated as:

$$I_{source\_pk} = \min(10A, \frac{VDD - VEE}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}})$$

$$I_{sink\_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G\_Int}}) \quad (1)$$

Where

- R_{OH_EFF} is the effective internal pull up resistance of the hybrid pull-up structure, which is approximately 2 x R_{OL}, about 0.7 Ω
- R_{OL} is the internal pulldown resistance, about 0.3 Ω
- R_{ON} is the external turn on gate resistance
- R_{OFF} is the external turn off gate resistance
- R_{G_Int} is the internal resistance of the SiC MOSFET or IGBT module

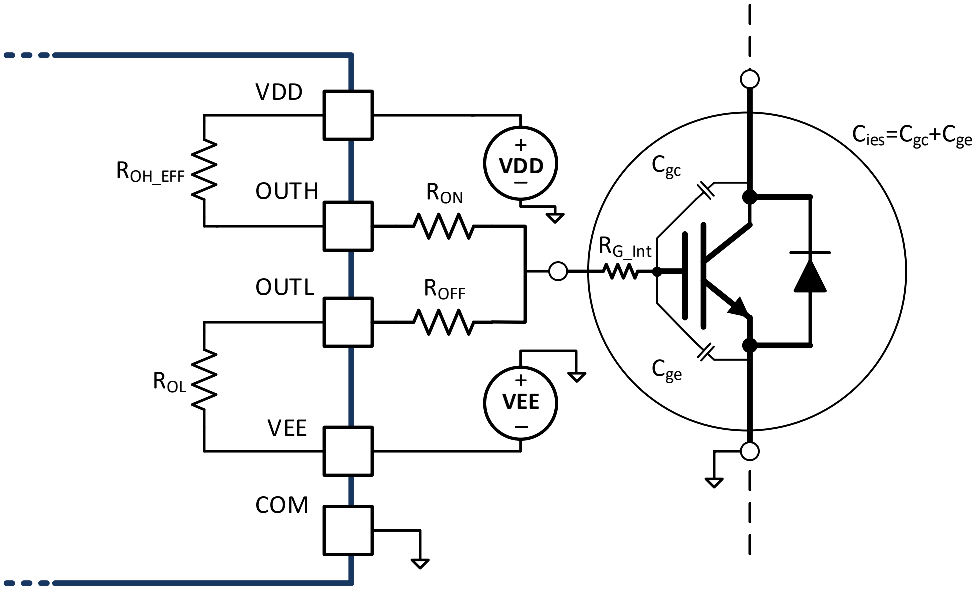


图 43. Output Model for Calculating Peak Gate Current

For example, for an IGBT module based system with the following parameters:

- Q_g = 3300 nC
- R_{G_Int} = 1.7 Ω
- $R_{ON}=R_{OFF}$= 1 Ω

The peak source and sink current in this case are:

$$I_{source\_pk} = \min(10A, \frac{VDD - VEE}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}}) \approx 5.9A$$

$$I_{sink\_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G\_Int}}) \approx 6.7A \tag{2}$$

Thus by using 1Ω external gate resistance, the peak source current is 5.9A, the peak sink current is 6.7A. The collector-to-emitter dV/dt during the turn on switching transient is dominated by the gate current at the miller plateau voltage. The hybrid pullup structure ensures the peak source current at the miller plateau voltage, unless the turn on gate resistor is too high. The faster the collector-to-emitter, V_{ce}, voltage rises to V_{DC}, the smaller the turn on switching loss is. The dV/dt can be estimated as Q_{gc}/I_{source_pk}. For the turn off switching transient, the drain-to-source dV/dt is dominated by the load current, unless the turn off gate resistor is too high. After V_{ce} reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by V_{ge}. The peak sink current determines the dI/dt, which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn off gate resistance, the V_{ce} overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{stray} \cdot I_{load} / ((R_{OFF} + R_{OL} + R_{G\_Int}) \cdot C_{ies} \cdot \ln(V_{plat} / V_{th})) \tag{3}$$

Where

- L_{stray} is the stray inductance in power switching loop, as shown in 图 44
- I_{load} is the load current, which is the turn off current of the power semiconductor
- C_{ies} is the input capacitance of the power semiconductor
- V_{plat} is the plateau voltage of the power semiconductor
- V_{th} is the threshold voltage of the power semiconductor

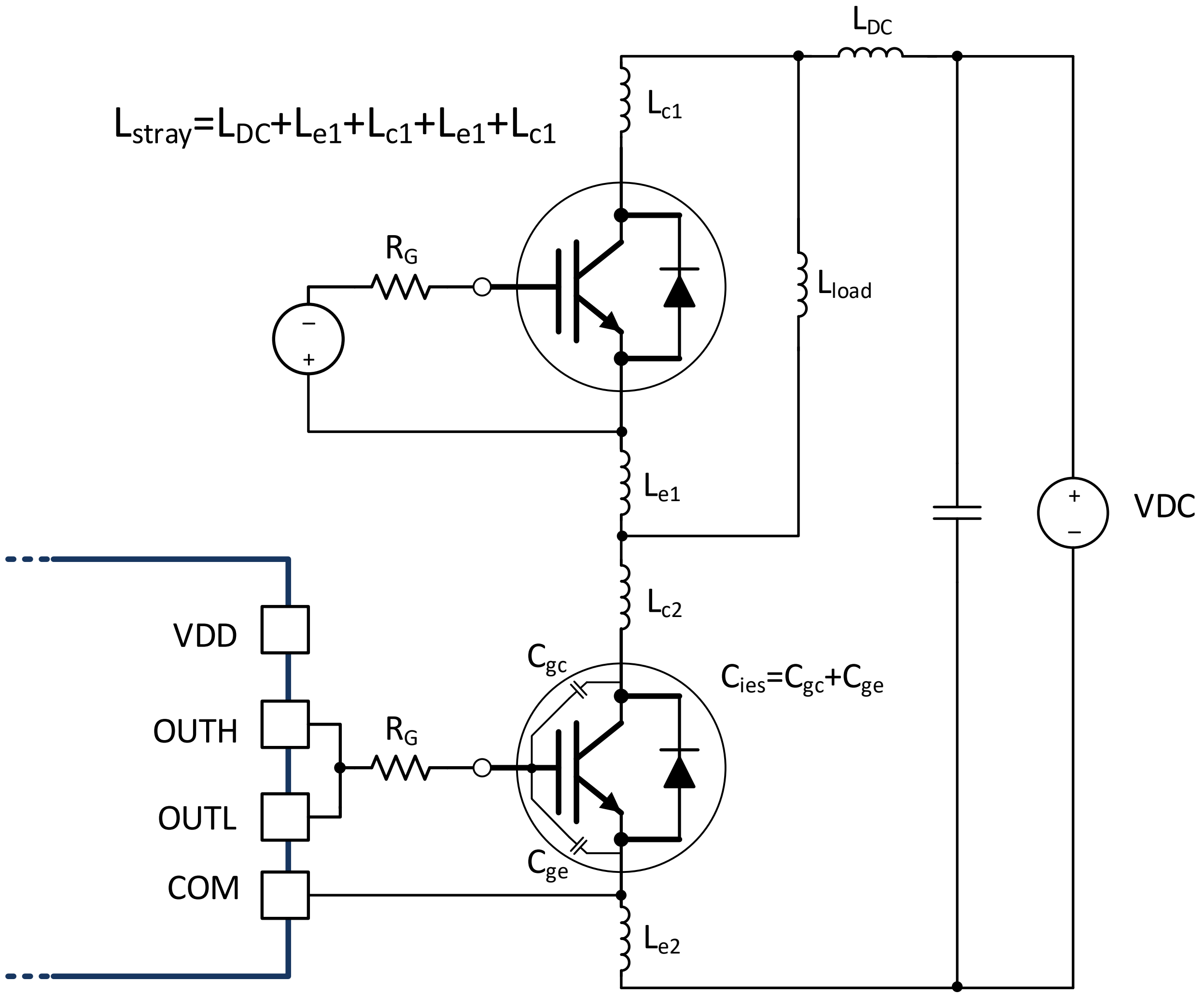


图 44. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration

The power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \tag{4}$$

P_Q is the quiescent power loss for the driver, which is I_q x (VDD-VEE) = 5mA x 20V = 0.100W. The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is swithing when the driver is biased with VDD and VEE, and also the charging and discharing current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}}\right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g \tag{5}$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD
- f_{sw} is the switching frequency

In this example, the P_{SW} can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}}\right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505W \tag{6}$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150^{\circ}C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

9.2.2.6 Overcurrent and Short Circuit Protection

A standard desaturation circuit can be applied to the DESAT pin. If the voltage of the DESAT pin is higher than the threshold V_{DESAT}, the soft turn-off is initiated. A fault will be reported to the input side to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{RST}$/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

If DESAT pin is not in use, it must be tied to COM to avoid overcurrent fault false triggering.

- Fast reverser recovery high voltage diode is recommended in the desaturation circuit. A resistor is recommended in series with the high voltage diode to limit the inrush current.
- A diode is recommended from COM to DESAT to prevent driver damage caused by negative voltage

9.2.2.7 Isolated Analog Signal Sensing

The isolated analog signal sensing feature provides a simple isolated channel for the isolated temperature detection, voltage sensing and etc. One typical application of this function is the temperature monitor of the power semiconductor. Thermal diodes or temperature sensing resistors are integrated in the SiC MOSFET or IGBT module close to the dies to monitor the junction temperature. UCC21750-Q1 has an internal 200uA current source with 3% accuracy across temperature, which can forward bias the thermal diodes or create a voltage drop on the temperature sensing resistors. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a PWM signal. The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5V to 0.6V and can be represented using 公式 9.

$$D_{APWM}(\%) = -20 * V_{AIN} + 100 \quad (9)$$

9.2.2.7.1 Isolated Temperature Sensing

A typical application circuit is shown in 图 45. To sense temperature, the AIN pin is connected to the thermal diode or thermistor which can be discrete or integrated within the power module. A low pass filter is recommended for the AIN input. Since the temperature signal does not have a high bandwidth, the low pass filter is mainly used for filtering the noise introduced by the switching of the power device, which does not require stringent control for propagation delay. The filter capacitance for C_{filt} can be chosen between 1nF to 100nF and the filter resistance R_{filt} between 1Ω to 10Ω according to the noise level.

The output of APWM is directly connected to the microcontroller to measure the duty cycle dependent on the voltage input at AIN, using 公式 9.

ADVANCE INFORMATION

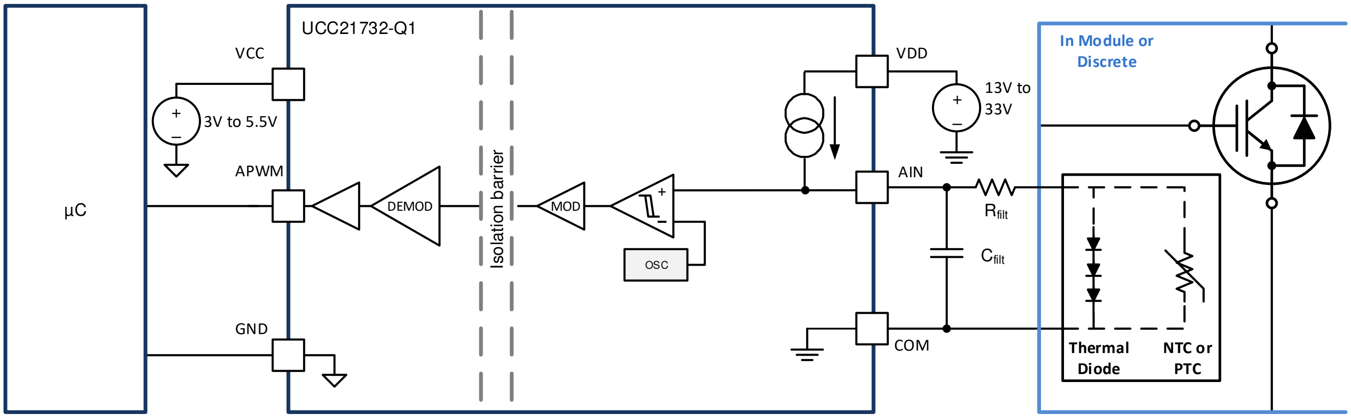


图 45. Thermal Diode or Thermistor Temperature Sensing Configuration

When a high-precision voltage supply for VCC is used on the primary side of UCC21750-Q1 the duty cycle output of APWM may also be filtered and the voltage measured using the microcontroller's ADC input pin, as shown in 图 46. The frequency of APWM is 400kHz, so the value for R_{filt_2} and C_{filt_2} should be such that the cutoff frequency is below 400kHz. Temperature does not change rapidly, thus the rise time due to the RC constant of the filter is not under a strict requirement.

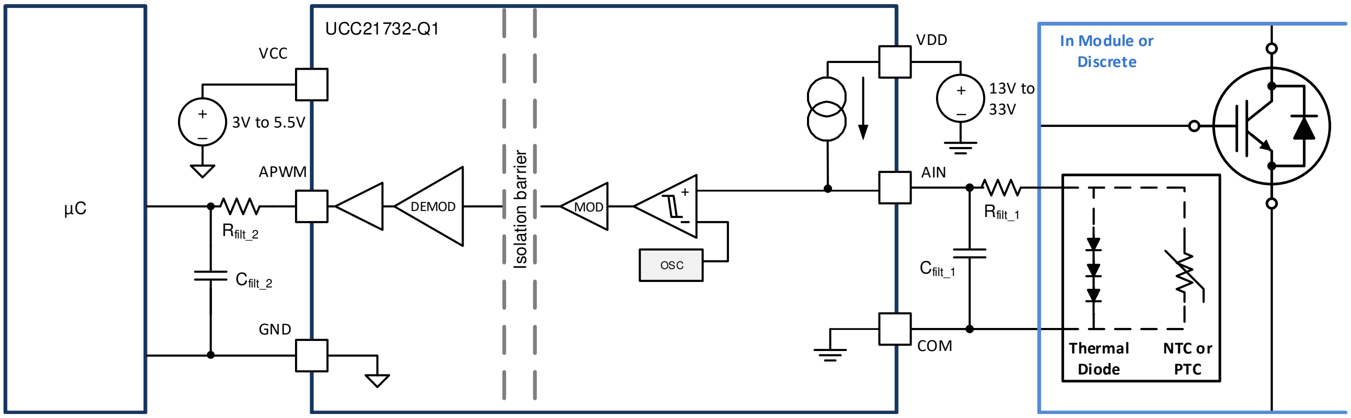


图 46. APWM Channel with Filtered Output

The example below shows the results using a 4.7kΩ NTC, NTCS0805E3472FMT, in series with a 3kΩ resistor and also the thermal diode using four diode-connected MMBT3904 NPN transistors. The sensed voltage of the 4 MMBT3904 thermal diodes connected in series ranges from about 2.5V to 1.6V from 25°C to 135°C, corresponding to 50% to 68% duty cycle. The sensed voltage of the NTC thermistor connected in series with the 3kΩ resistor ranges from about 1.5V to 0.6V from 25°C to 135°C, corresponding to 70% to 88% duty cycle. The voltage at VAIN of both sensors and the corresponding measured duty cycle at APWM is shown in 图 47.

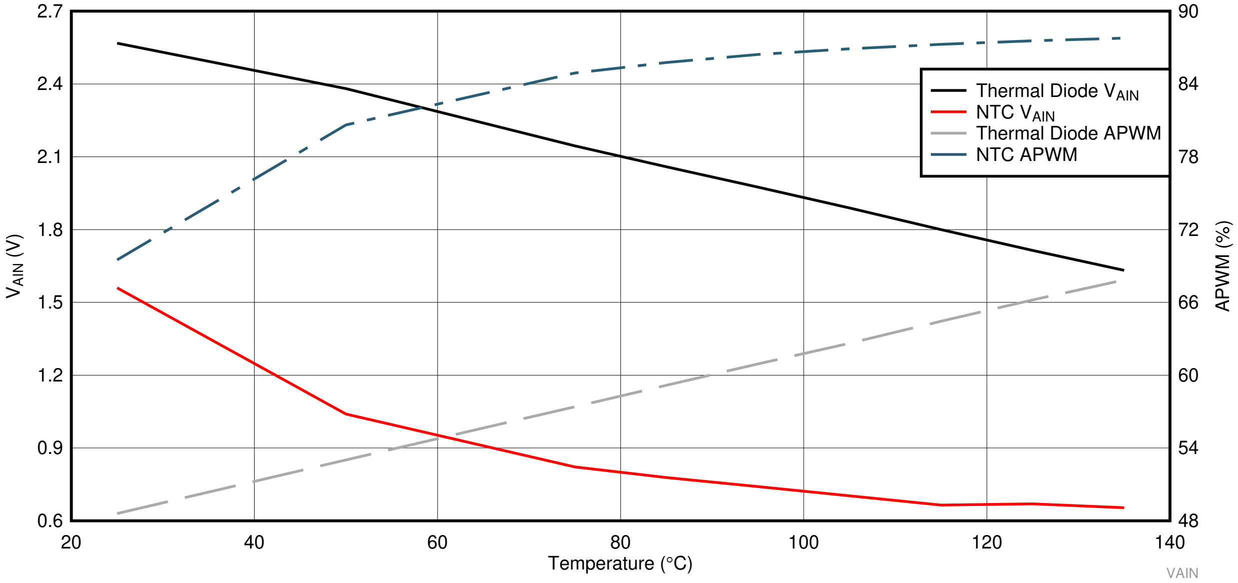


图 47. Thermal diode and NTC V_{AIN} and Corresponding Duty Cycle at APWM

The duty cycle output has an accuracy of ±3% throughout temperature without any calibration, as shown in 图 48 but with single-point calibration at 25°C, the duty accuracy can be improved to ±1%, as shown in 图 49.

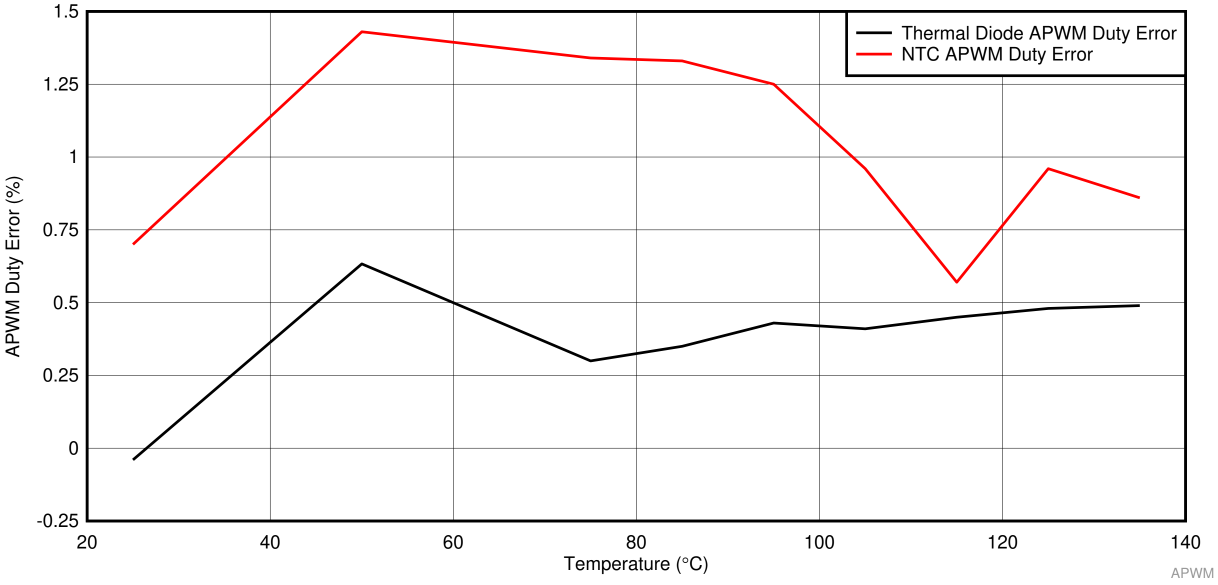


图 48. APWM Duty Error Without Calibration

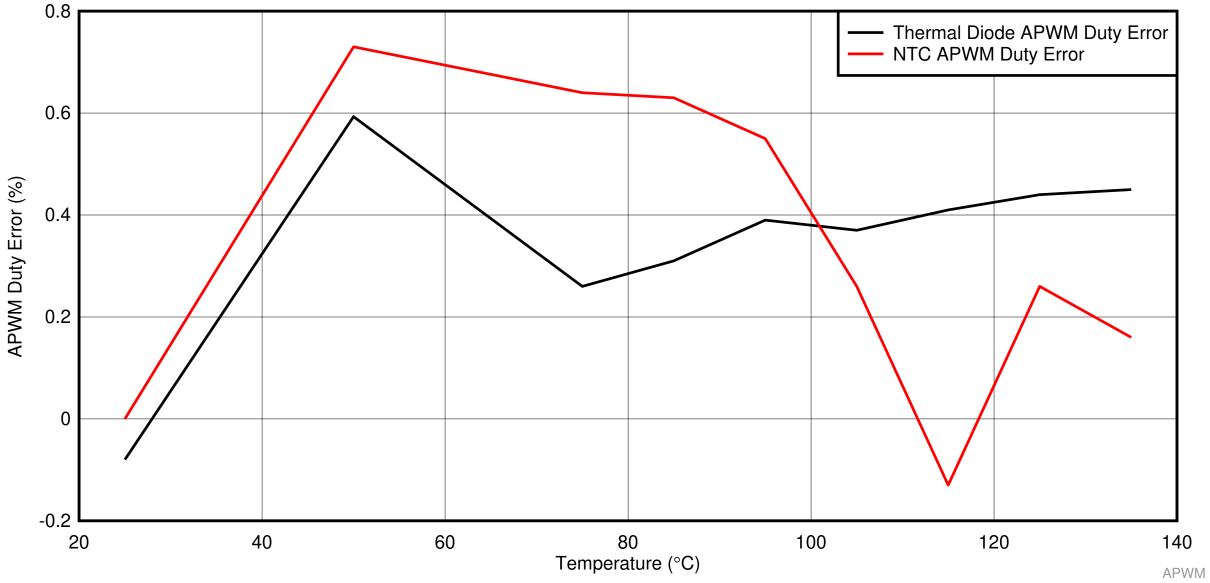


图 49. APWM Duty Error with Single-Point Calibration

9.2.2.7.2 Isolated DC Bus Voltage Sensing

The AIN to APWM channel may be used for other applications such as the DC-link voltage sensing, as shown in 图 50. The same filtering requirements as given above may be used in this case, as well. The number of attenuation resistors, R_{atten_1} through R_{atten_n}, is dependent on the voltage level and power rating of the resistor. The voltage is finally measured across R_{LV_DC} to monitor the stepped-down voltage of the HV DC-link which must fall within the voltage range of AIN from 0.6V to 4.5V. The driver should be referenced to the same point as the measurement reference, thus in the case shown below the UCC21750-Q1 is driving the lower IGBT in the half-bridge and the DC-link voltage measurement is referenced to COM. The internal current source I_{AIN} should be taken into account when designing the resistor divider. The AIN pin voltage is:

$$V_{AIN} = \frac{R_{LV\_DC}}{R_{LV\_DC} + \sum_{i=1}^{n} R_{atten\_i}} \cdot V_{DC} + R_{LV\_DC} \cdot I_{AIN} \tag{10}$$

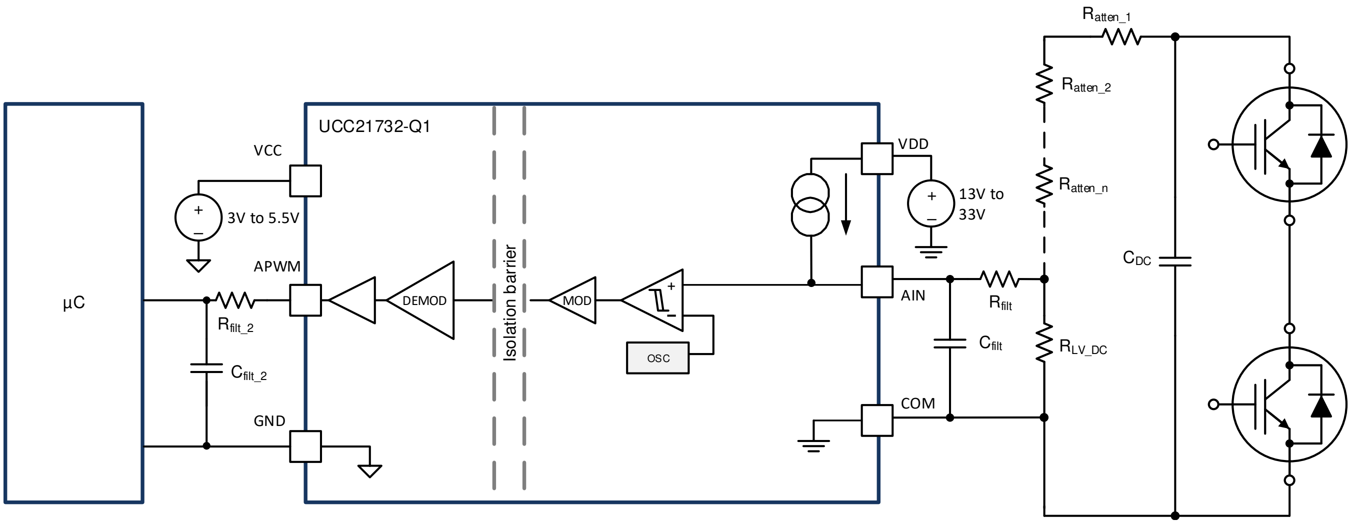


图 50. DC-link Voltage Sensing Configuration

9.2.2.8 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the NPN/PNP buffer shown in 图 51) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/ D45VH10 pair is up to 20 A peak.

In the case of a over-current detection, the soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn off speed when an external buffer is used. C_{STO} sets the timing for soft turn off and R_{STO} limits the inrush current to below the current rating of the internal FET (10A). R_{STO} should be at least (VDD-VEE)/10. The soft turn off timing is determined by the internal current source of 400mA and the capacitor C_{STO}. C_{STO} is calculated using .

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \tag{11}$$

- I_{STO} is the the internal STO current source, 400mA
- t_{STO} is the desired STO timing

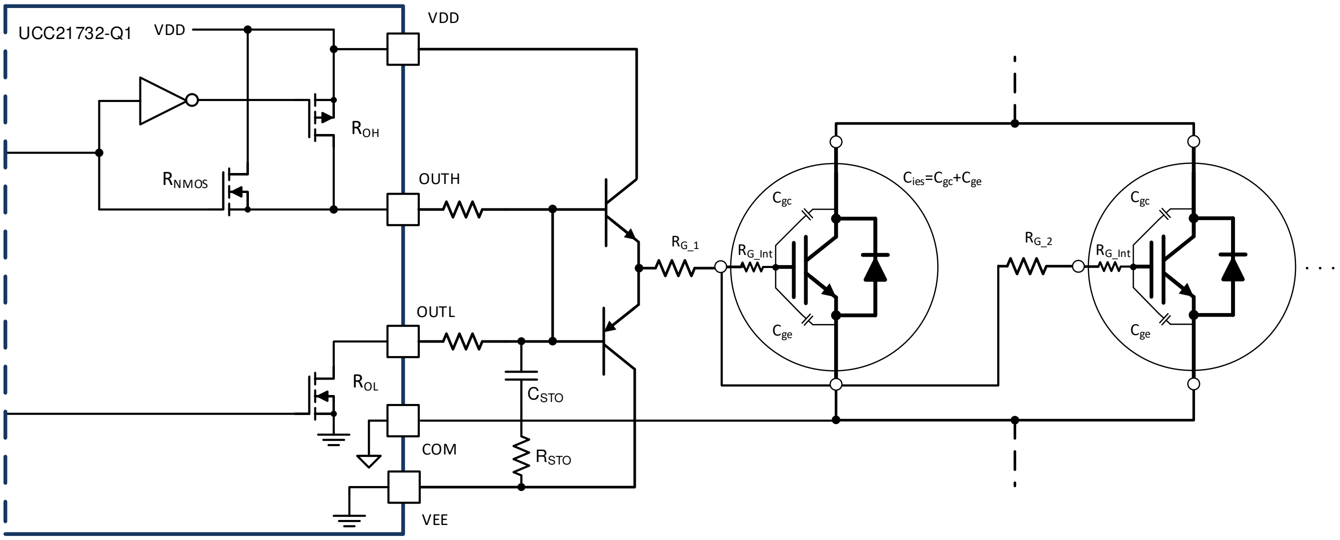


图 51. **Current Buffer for Increased Drive Strength**

10 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering UCC21750-Q1 has ±10A peak drive strength and can generate high dV/dt, a 10µF bypass cap is recommended between VDD and COM, VEE and COM. A 1µF bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1µF decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

11 Layout

11.1 Layout Guidelines

Due to the strong drive strength of UCC21750-Q1, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high dI/dt and voltage spike on the parasitic inductance of PCB traces
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended
- If ground plane is not used on the output side, separate the return path of the DESAT and AIN ground loop from the gate loop ground which has large peak source and sink current
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier

11.2 Layout Example

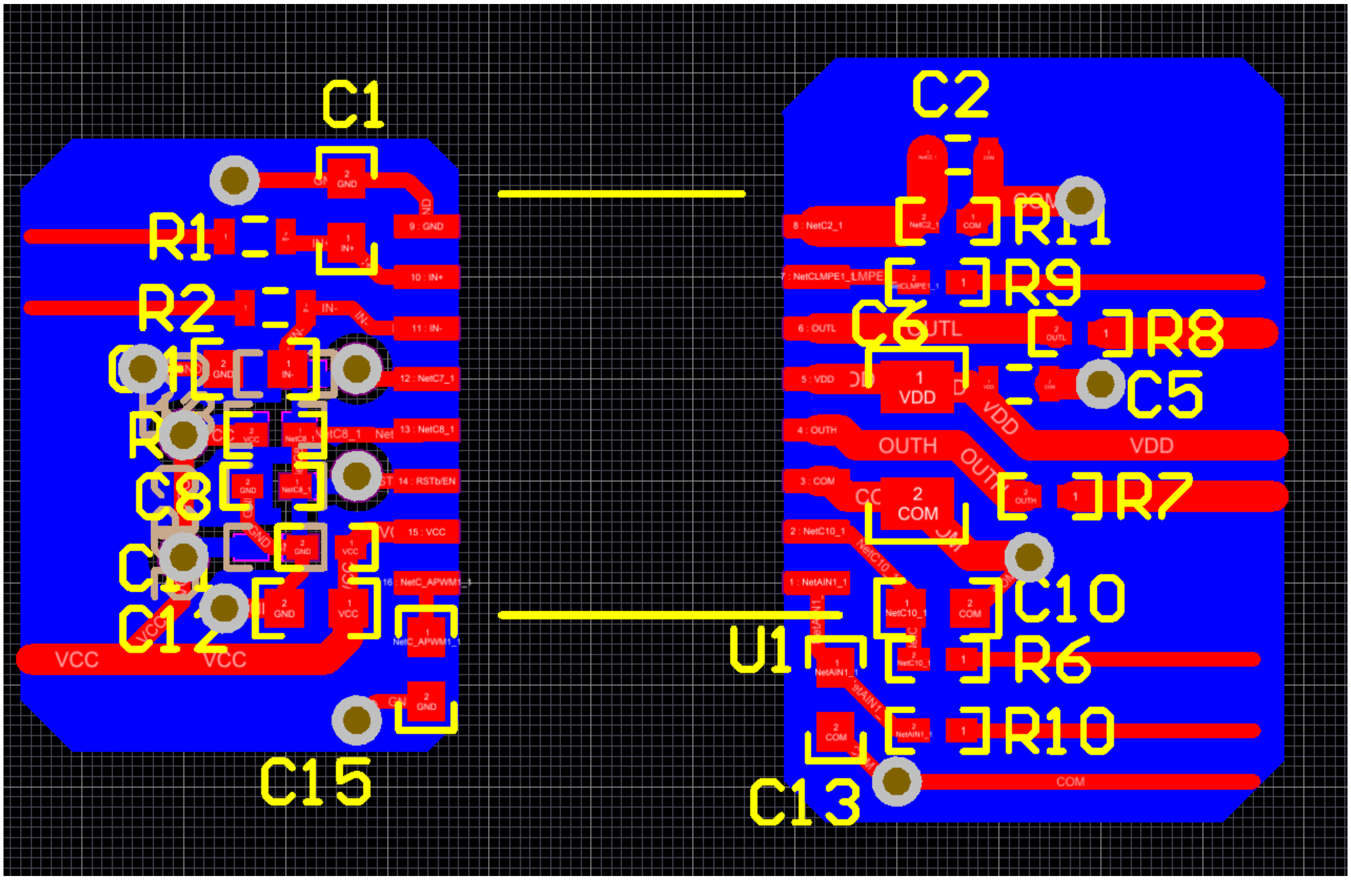


图 52. Layout Example

ADVANCE INFORMATION

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《隔离相关术语》*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

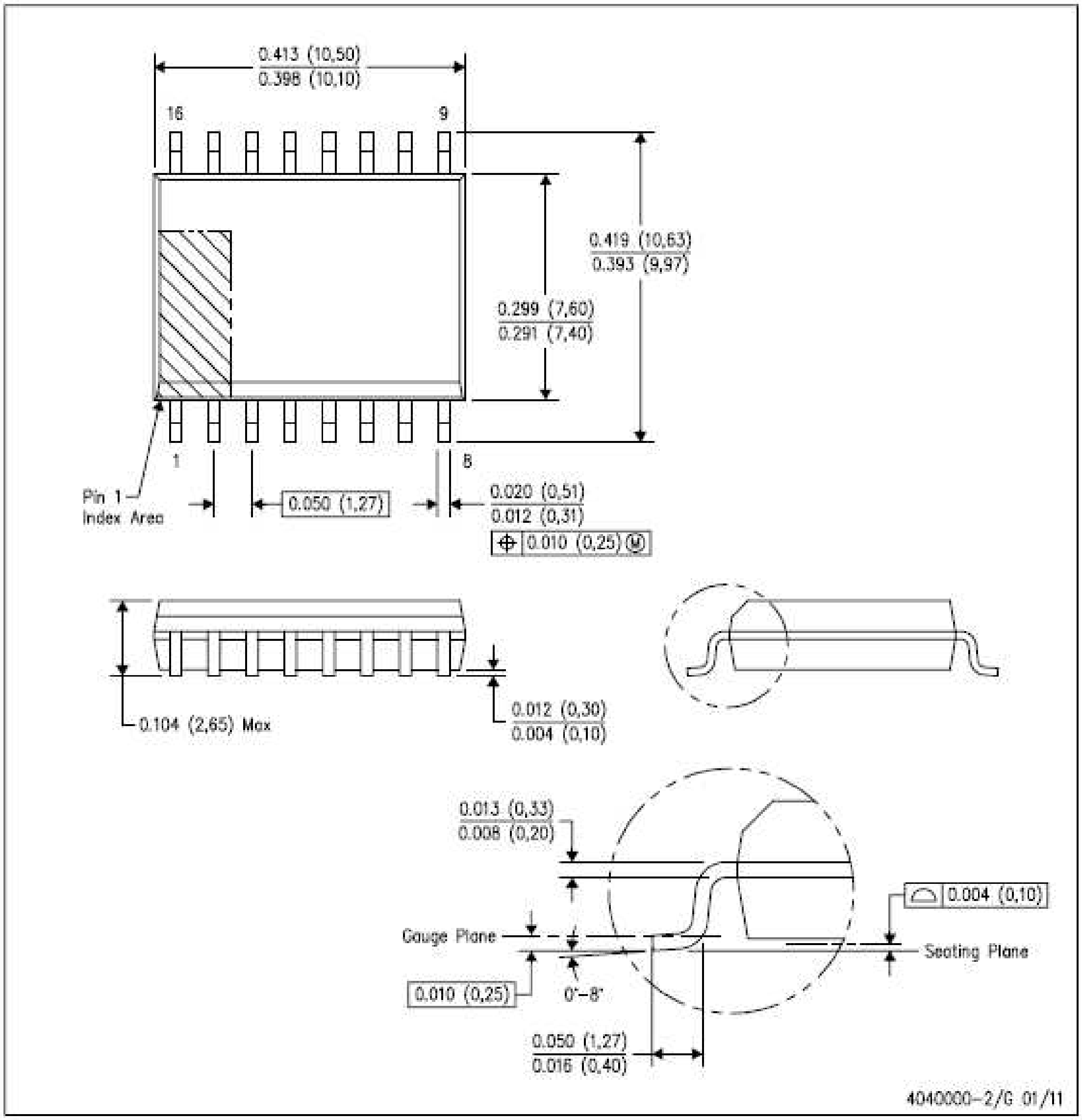
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

MECHANICAL DATA

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21750QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21750Q	Samples
UCC21750QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21750Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

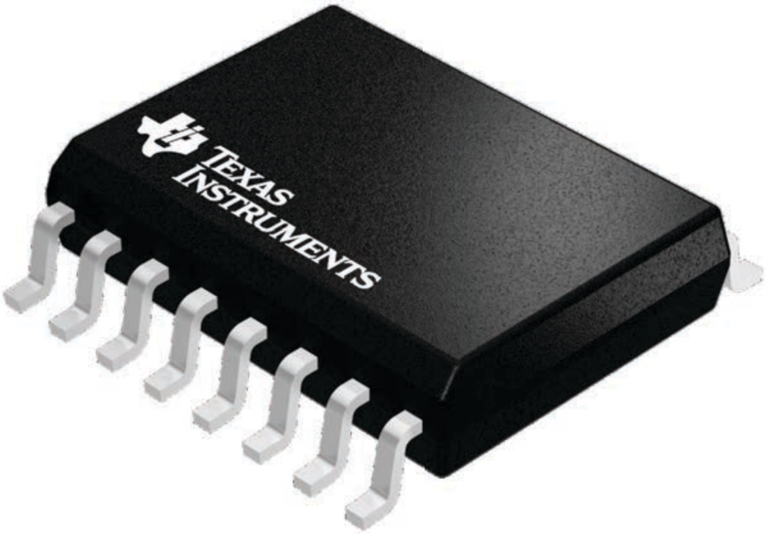
DW 16

SOIC - 2.65 mm max height

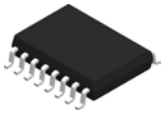
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

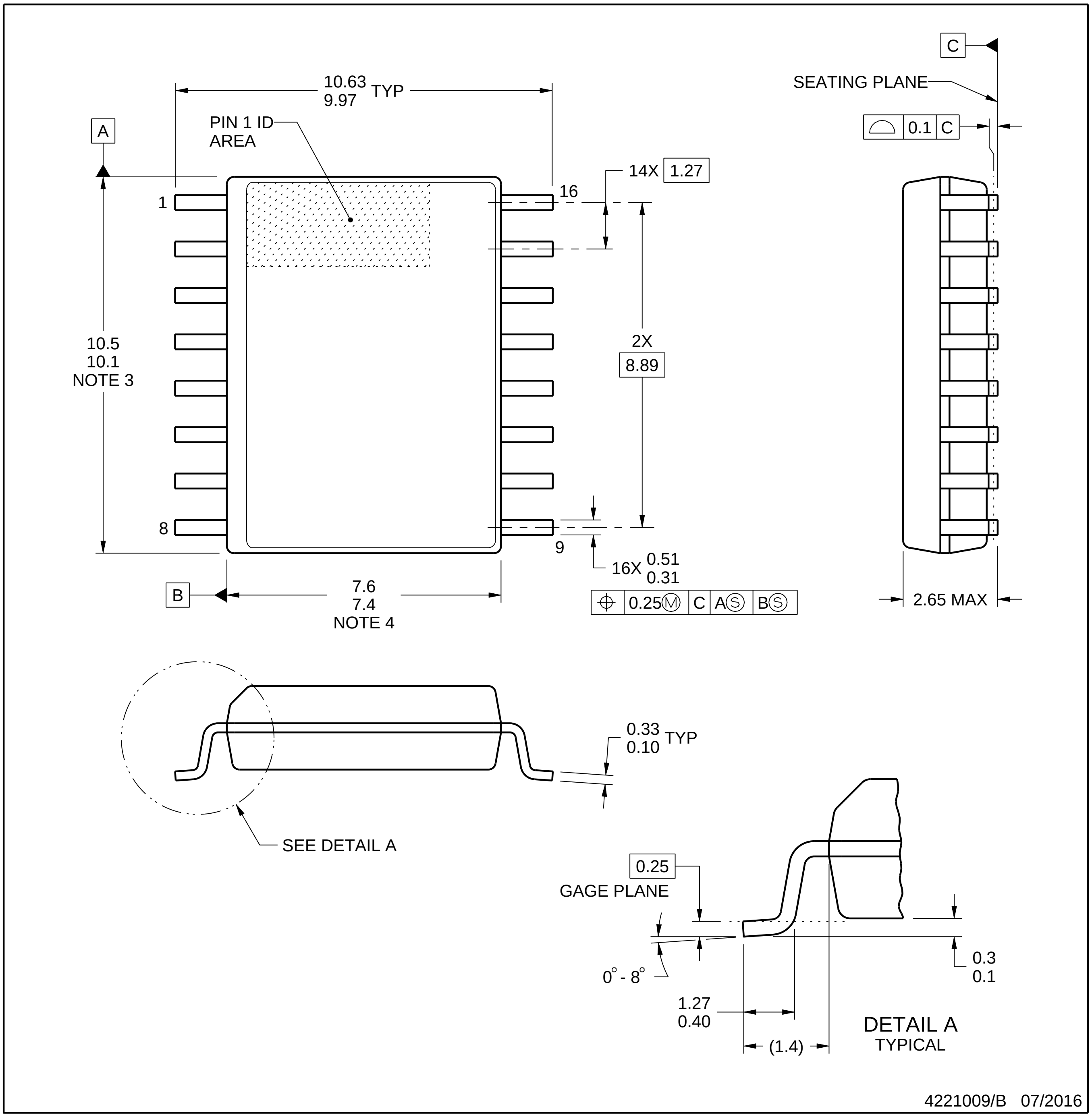


PACKAGE OUTLINE

DW0016B

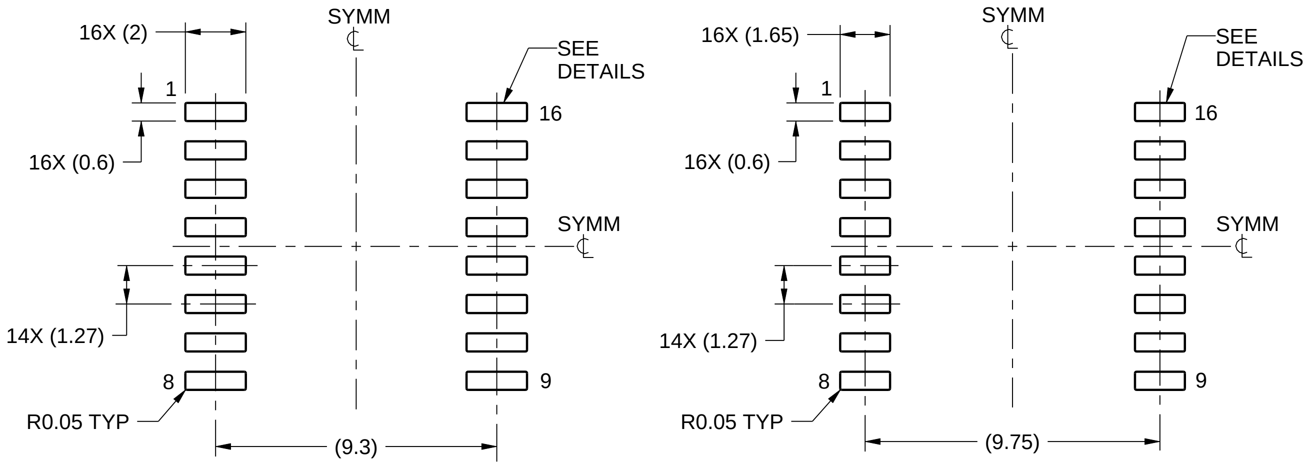
SOIC - 2.65 mm max height

SOIC



NOTES:

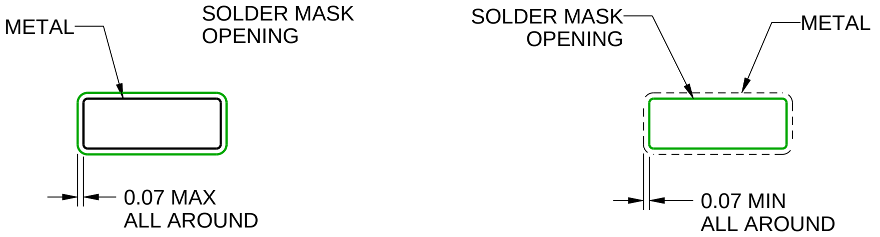
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

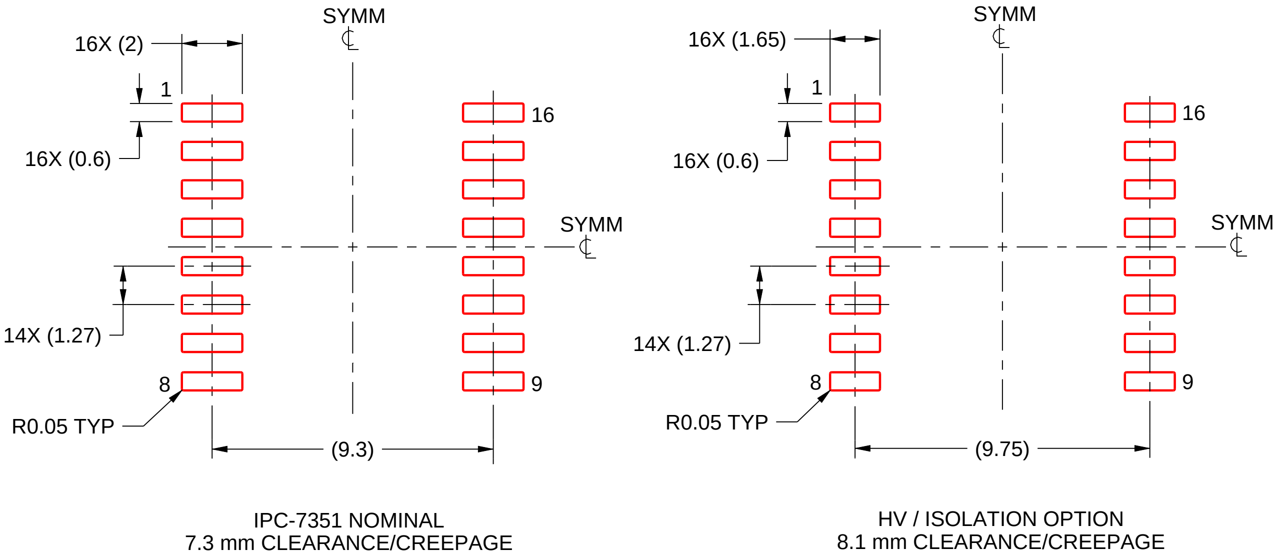
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122