TDP142 DisplayPort™ 8.1Gbps 线性转接驱动器

1 特性

- DisplayPort™1.4 高达 8.1Gbps (HBR3)
- 超低功耗架构
- 具有高达 14dB 均衡功能的线性转接驱动器
- 透明呈现 DisplayPort 链路训练
- 可通过 GPIO 或 I^2C 进行配置
- 支持热插拔
- 支持 DisplayPort 双模标准版本 1.1（交流耦合 HDMI）
- 工业级温度范围：-40ºC 至 85ºC (TDP142I)
- 商业级温度范围：0ºC 至 70ºC (TDP142)
- 4mm x 6mm、0.4mm 间距 WQFN 封装

2 应用

- 平板电脑、笔记本电脑、台式电脑、PC
- 有源电缆
- 监视器
- 扩展坞

3 说明

TDP142 是一款能够嗅探 AUX 和 HPD 信号的 DisplayPort™(DP) 线性转接驱动器。该器件符合 VESA DisplayPort 标准版本 1.4，支持 1-4 通道主链路接口，以符合 HBR3 标准的速率（每个通道 8.1Gbps）发送信号。此外，该器件与位置无关。它可置于源设备、电缆或接收设备内，从而为总体链路预算有效提供“负损耗”分量。

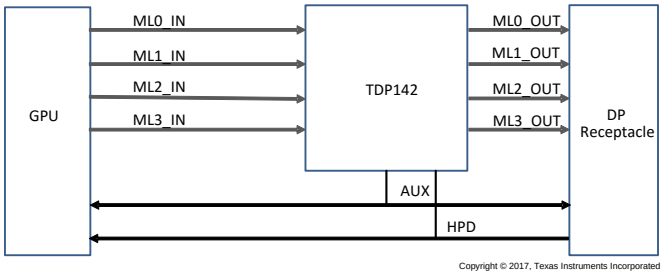
TDP142 提供多个接收线性均衡级别，用于补偿线缆或电路板走线中因码间串扰 (ISI) 而产生的损耗。该器件由 3.3V 单电源供电，支持商业级温度范围 (TDP142) 和工业级温度范围 (TDP142I)。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TDP142	WQFN (40)	4.00mm x 6.00mm
TDP142I	WQFN (40)	4.00mm x 6.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

Changes from Revision B (August 2018) to Revision C **Page**

- Added following to pin 11 description: If I2C_EN = “F”, then this pin must be set to “F” or “0”. ... 3

Changes from Revision A (October 2017) to Revision B **Page**

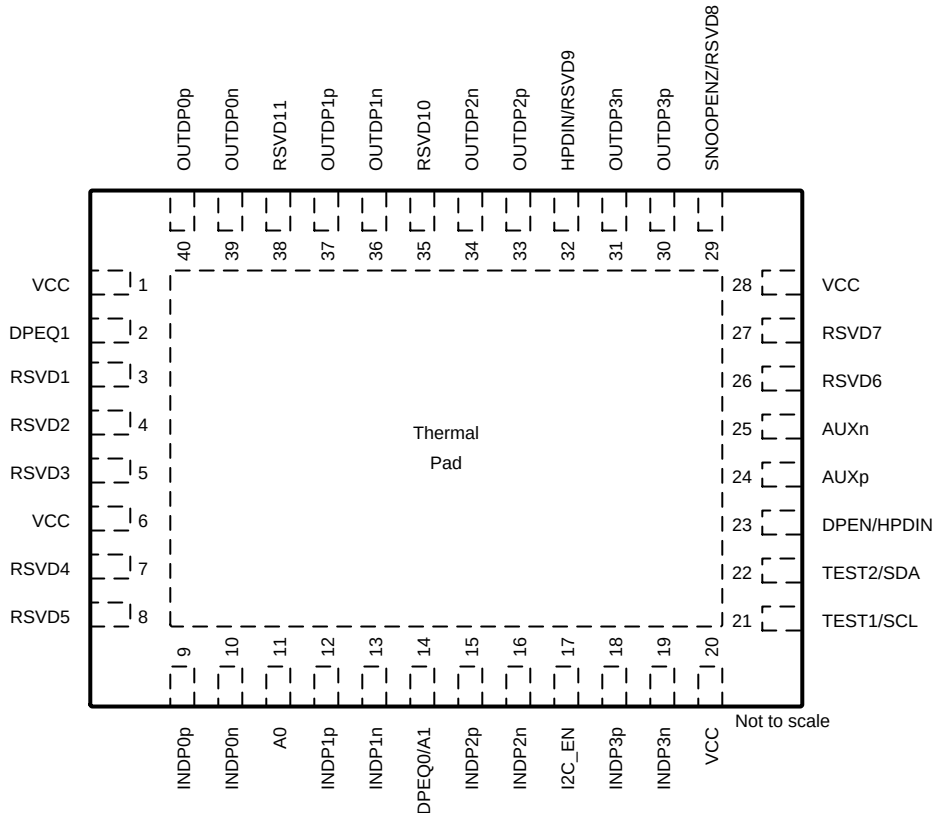
- Changed the appearance of the pinout image in the Pin Configuration and Function section ... 3
- Added Note 2 To pins 29 and 32 in the *Pin Functions* table ... 4

Changes from Original (September 2017) to Revision A **Page**

- Changed the Human-body model (HBM) value From: ±6000 To: ±5000 in the *ESD Ratings* ... 5

5 Pin Configuration and Functions

RNQ Package
40-Pin (WQFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC	1, 6, 20, 28	P	3.3-V Power Supply.
DPEQ1	2	4 Level I	DisplayPort Receiver EQ control. This along with DPEQ0 will select the DisplayPort receiver equalization gain. Refer to 表 2 for equalization settings.
RSVD1	3	I	Reserved.(1)
RSVD2	4	O	Reserved.(1)
RSVD3	5	O	Reserved.(1)
RSVD4	7	I	Reserved.(1)
RSVD5	8	I	Reserved.(1)
INDP0p	9	I	DP Differential positive input for DisplayPort Lane 0.
INDP0n	10	I	DP Differential negative input for DisplayPort Lane 0.
A0	11	4 Level I	When I2C_EN = 0, leave the pin unconnected. When I2C_EN is not '0', this pin will also set the TDP142 I^2C address. See 表 4. If I2C_EN = "F", then this pin must be set to "F" or "0".
INDP1p	12	Diff I	DP Differential positive input for DisplayPort Lane 1.
INDP1n	13	Diff I	DP Differential negative input for DisplayPort Lane 1.
DPEQ0/A1	14	4 Level I	DisplayPort Receiver EQ control. This along with DPEQ1 will select the DisplayPort receiver equalization gain. Refer to 表 2 for equalization settings. When I2C_EN is not '0', this pin will also set the TDP142 I^2C address. See 表 4.
INDP2p	15	Diff I	DP Differential positive input for DisplayPort Lane 2.
INDP2n	16	Diff I	DP Differential negative input for DisplayPort Lane 2.

(1) Leave unconnected on PCB.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
I2C_EN	17	4 Level I	I^2C Programming Mode or GPIO Programming Select. I2C is only disabled when this pin is '0". 0 = GPIO mode (I^2C disabled). R = TI Test Mode (I^2C enabled at 3.3 V). F = I^2C enabled at 1.8 V. 1 = I^2C enabled at 3.3 V.
INDP3p	18	Diff I	DP Differential positive input for DisplayPort Lane 3.
INDP3n	19	Diff I	DP Differential negative input for DisplayPort Lane 3.
TEST1/SCL	21	2 Level I	When I2C_EN='0', pull down with 10k or directly connect to ground. Otherwise this pin is I^2C clock. . When used for I^2C clock pullup to I^2C master's VCC I^2C supply.
TEST2/SDA	22	2 Level I	When I2C_EN='0' , pull down with 10k or directly connect to ground. Otherwise this pin is I^2C data. When used for I^2C data pullup to I^2C master's VCC I^2C supply.
DPEN/HPDIN	23	2 Level I (Failsafe) (PD)	DP Enable Pin. When I2C_EN = '0', this pin will enable or disable DisplayPort functionality. Otherwise, when I2C_EN is not "0", DisplayPort functionality is enabled and disabled through I^2C registers. L = DisplayPort Disabled. (Pull-down with 10k resistor) H = DisplayPort Enabled. (Pull-up with10k resistor) When I2C_EN is not "0" this pin is an input for Hot Plug Detect (HPD) received from DisplayPort sink. When this HPDIN is low for greater than 2 ms, all DisplayPort lanes are disabled.
AUXp	24	I/O, CMOS	This pin along with AUXN is used by the TDP142 for AUX snooping. See the *Application and Implementation* section for more detail.
AUXn	25	I/O, CMOS	This pin along with AUXP is used by the TDP142 for AUX snooping. See the *Application and Implementation* section for more detail.
RSVD6	26	I/O, CMOS	Reserved.(1)
RSVD7	27	I/O, CMOS	Reserved.(1)
SNOOPENZ/RSVD8	29(2)	I/O (PD)	When I2C_EN ! = 0, this pin is reserved. When I2C_EN = 0 , this pin is SNOOPENZ (L = AUX snoop enabled and H = AUX snoop disabled with all lanes active).
OUTDP3p	30	Diff O	DP Differential positive output for DisplayPort Lane 3.
OUTDP3n	31	Diff O	DP Differential negative output for DisplayPort Lane 3.
HPDIN/RSVD9	32(2)	I/O (PD)	When I2C_EN ! = 0, this pin is reserved. When I2C_EN = 0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is low for greater than 2ms, all DisplayPort lanes are disabled.
OUTDP2p	33	Diff O	DP Differential positive output for DisplayPort Lane 2.
OUTDP2n	34	Diff O	DP Differential negative output for DisplayPort Lane 2.
RSVD10	35	I	Reserved.(1)
OUTDP1n	36	Diff O	DP Differential negative output for DisplayPort Lane 1.
OUTDP1p	37	Diff O	DP Differential positive output for DisplayPort Lane 1.
RSVD11	38	I	Reserved.(1)
OUTDP0n	39	Diff O	DP Differential negative output for DisplayPort Lane 0.
OUTDP0p	40	Diff O	DP Differential positive output for DisplayPort Lane 0.
GND	Thermal Pad	G	Ground.

(2) Not a fail-safe I/O. Actively driving pin high while VCC is removed results in leakage voltage on VCC pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range(2), V_{CC}		–0.3	4	V
Voltage Range at any input or output pin	Differential voltage between positive and negative inputs	–2.5	2.5	V
	Voltage at differential inputs	–0.5	V_{CC} + 0.5	V
	CMOS Inputs	–0.5	V_{CC} + 0.5	V
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Main power supply		3	3.3	3.6	V
	Supply Ramp Requirement				100	ms
$V_{(12C)}$	Supply that external resistors are pulled up to on SDA and SCL		1.7		3.6	V
$V_{(PSN)}$	Supply Noise on V_{CC} pins				100	mV
T_A	Operating free-air temperature	TDP142	0		70	°C
		TDP142I	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TDP142 RNQ (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE--DP)}$	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1 Gbps; DPEN = H; TEST2 = L;		660		mW
$P_{CC(NC)}$	Average power with no connection	No device is connected		2.4		mW
$P_{CC(SHUTDOWN)}$	Device Shutdown	DPEN = L; TEST2 = L; I2C_EN = 0;		0.85		mW

6.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-State CMOS Inputs(DPEQ[1:0], I2C_EN)						
I_{IH}	High level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	20		80	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	–160		-40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3 V		0.55		V
	Threshold R/ Float	V_{CC} = 3.3 V		1.65		V
	Threshold Float / 1	V_{CC} = 3.3 V		2.7		V
R_{PU}	Internal pull-up resistance			35		kΩ
R_{PD}	Internal pull-down resistance			95		kΩ
2-State CMOS Input (DPEN, Test1, Test2, SNOOPENZ, HPDIN) DPEN, TEST1 and TEST2 are Failsafe.						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
R_{PD}	Internal pull-down resistance for DPEN			500		kΩ
$R_{(ENPD)}$	Internal pull-down resistance for SNOOPENZ (pin 29), and HPDIN (pin 32)			150		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V	–25		25	µA
I_{IL}	Low-level input current	V_{IN} = GND, V_{CC} = 3.6 V	–25		25	µA
I^2C Control Pins SCL, SDA						
V_{IH}	High-level input voltage	I2C_EN = 0	0.7 x $V_{(I2C)}$		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = 0	0		0.3 x $V_{(I2C)}$	V
V_{OL}	Low-level output voltage	I2C_EN = 0; I_{OL} = 3 mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN = 0; V_{OL} = 0.4 V	20			mA
$I_{I(I2C)}$	Input current on SDA pin	0.1 x $V_{(I2C)}$ < Input voltage < 3.3 V	–10		10	µA
$C_{I(I2C)}$	Input capacitance				10	pF
$C_{(I2C\_FM+\_BUS)}$	I2C bus capacitance for FM+ (1MHz)				150	pF
$C_{(I2C\_FM\_BUS)}$	I2C bus capacitance for FM (400kHz)				150	pF
$R_{(EXT\_I2C\_FM+)}$	External resistors on both SDA and SCL when operating at FM+ (1MHz)	$C_{(I2C\_FM+\_BUS)}$ = 150 pF	620	820	910	Ω
$R_{(EXT\_I2C\_FM)}$	External resistors on both SDA and SCL when operating at FM (400kHz)	$C_{(I2C\_FM\_BUS)}$ = 150 pF	620	1500	2200	Ω

6.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DisplayPort Transmitter (OUTDP[3:0]p or OUTDP[3:0]n)						
$V_{TX(DIFF-PP)}$	Transmitter dynamic differential voltage swing range.			1500		mV_{PP}
$V_{TX(RCV-DETECT)}$	Amount of voltage change allowed during receiver detection				600	mV
$V_{TX(CM-AC-PP-ACTIVE)}$	Tx AC common-mode voltage active	Max mismatch from Txp + Txn for both time and amplitude			100	mV_{PP}
$V_{TX(IDLE-DIFF-AC-PP)}$	AC electrical idle differential peak-to-peak output voltage	At package pins	0		10	mV
$V_{TX(IDLE-DIFF-DC)}$	DC electrical idle differential output voltage	At package pins after low pass filter to remove AC component	0		14	mV
$R_{TX(DIFF)}$	Differential impedance of the driver		75		120	Ω
$C_{AC(COUPLING)}$	AC coupling capacitor		75		265	nF
$R_{TX(CM)}$	Common-mode impedance of the driver	Measured with respect to AC ground over 0–500 mV	18		30	Ω
$C_{TX(PARASITIC)}$	TX input capacitance for return loss	At package pins, at 2.5GHz			1.25	pF
$R_{LTX(DIFF)}$	Differential return loss	50 MHz – 1.25 GHz at 90 Ω		-15		dB
		2.5 GHz at 90 Ω		-12		dB
$R_{LTX(CM)}$	Common-mode return loss	50 MHz – 2.5 GHz at 90 Ω		-13		dB
$I_{TX(SHORT)}$	TX short circuit current	TX± shorted to GND			67	mA
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)		0		0	V
AC Characteristics						
Crosstalk	Differential crosstalk between TX and RX signal pairs	at 2.5 GHz		–30		dB
$C_{(P1dB-LF)}$	Low frequency 1-dB compression point	at 100 MHz, 200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$		1300		mV_{PP}
$C_{(P1dB-HF)}$	High frequency 1-dB compression point	at 2.5 GHz, 200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$		1300		mV_{PP}
f_{LF}	Low frequency cutoff	200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$		20	50	kHz
	TX output deterministic jitter	200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$, PRBS7, 5 Gbps		0.05		UIpp
		200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$, PRBS7, 8.1 Gbps		0.08		UIpp
	TX output total jitter	200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$, PRBS7, 5 Gbps		0.08		UIpp
		200 $mV_{PP} < V_{ID} < 2000\ mV_{PP}$, PRBS7, 8.1 Gbps		0.135		UIpp
DisplayPort Receiver (INDP[3:0]p or INDP[3:0]n)						
$V_{ID(PP)}$	Peak-to-peak input differential dynamic voltage range			2000		V
V_{IC}	Input common mode voltage		0		2	V
$C_{(AC)}$	AC coupling capacitance		75		200	nF
$E_{Q(DP)}$	Receiver equalization	DPEQ[1:0] at 4.05 GHz			14	dB
d_R	Data rate	HBR3			8.1	Gbps
$R_{(ti)}$	Input termination resistance		80	100	120	Ω
AUXp or AUXn						
$V_{(AUXP\_DC\_CM)}$	AUX Channel DC common mode voltage for AUXp	V_{CC} = 3.3 V	0		0.4	V
$V_{(AUXN\_DC\_CM)}$	AUX Channel DC common mode voltage for AUXn	V_{CC} = 3.3 V	2.7		3.6	V

6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{DIFF_DLY}	Differential Propagation Delay	See 图 7			300	ps
t_R, t_F	Output Rise/Fall time (see 图 9)	20%-80% of differential voltage measured 1 inch from the output pin	40			ps
t_{RF_MM}	Output Rise/Fall time mismatch	20%-80% of differential voltage measured 1 inch from the output pin			2.6	ps

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DPEN and HPDIN						
$t_{DPEN\_DEBOUNCE}$	DPEN and HPDIN debounce time when transitioning from H to L.		2		10	ms
I^2C (Refer to 图 6)						
f_{SCL}	I^2C clock frequency				1	MHz
t_{BUF}	Bus free time between START and STOP conditions		0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.26			µs
t_{LOW}	Low period of the I^2C clock		0.5			µs
t_{HIGH}	High period of the I^2C clock		0.26			µs
t_{SUSTA}	Setup time for a repeated START condition		0.26			µs
t_{HDDAT}	Data hold time		0			µs
t_{SUDAT}	Data setup time		50			ns
t_R	Rise time of both SDA and SCL signals				120	ns
t_F	Fall time of both SDA and SCL signals		20 × ($V_{(I2C)}$/5.5 V)		120	ns
t_{SUSTO}	Setup time for STOP condition		0.26			µs
C_b	Capacitive load for each bus line				150	pF

6.10 Typical Characteristics

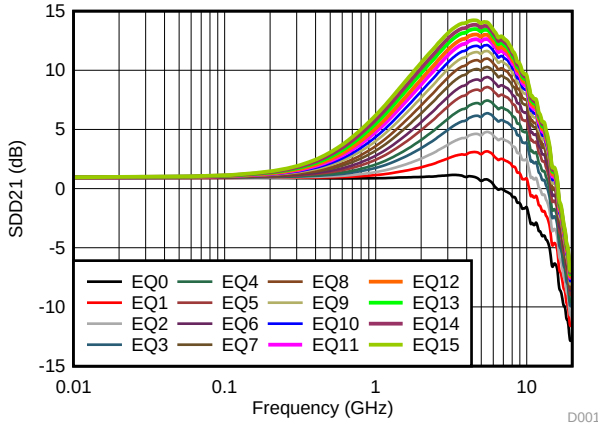


图 1. DisplayPort EQ Settings Curves

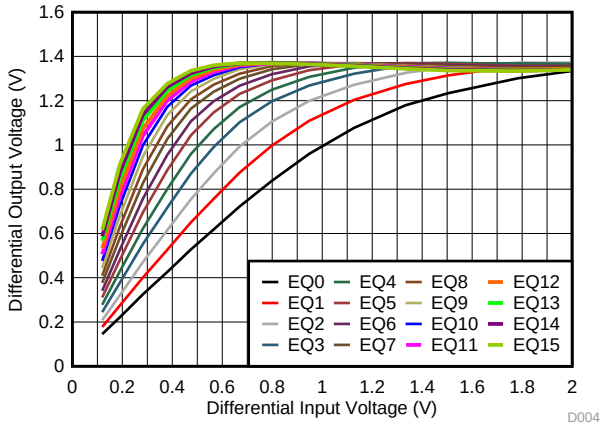


图 2. DisplayPort Linearity Curves at 4.05 GHz

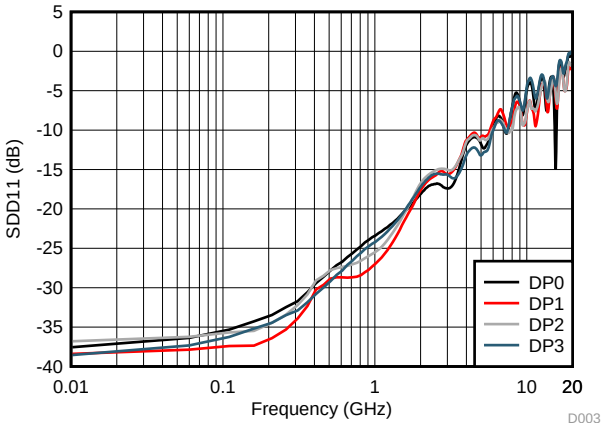


图 3. Input Return Loss Performance

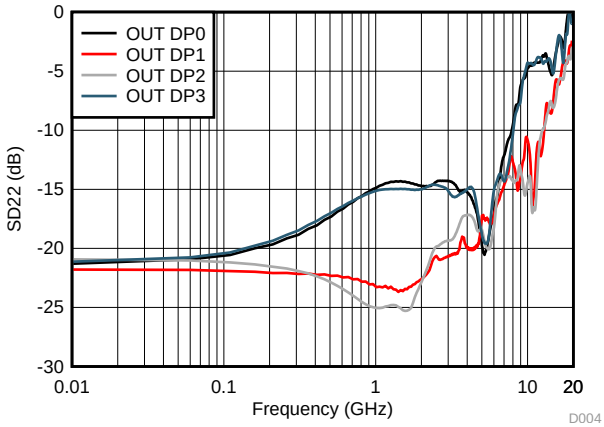


图 4. Output Return Loss Performance

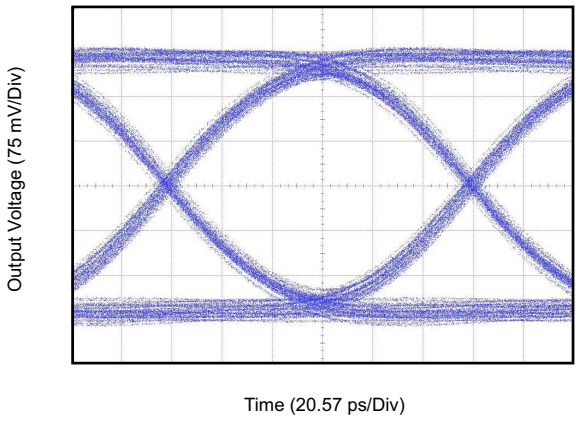


图 5. DisplayPort HBR3 Eye-Pattern Performance with 12-inch Input PCB Trace at 8.1 Gbps

7 Parameter Measurement Information

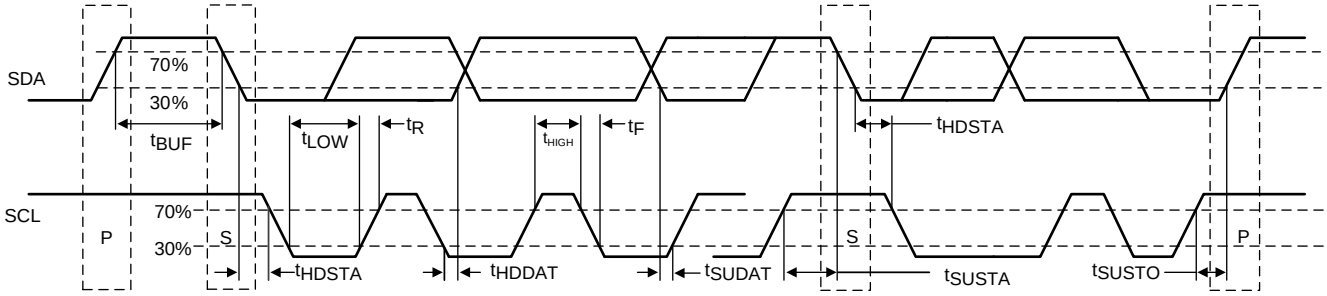


图 6. I²C Timing Diagram Definitions

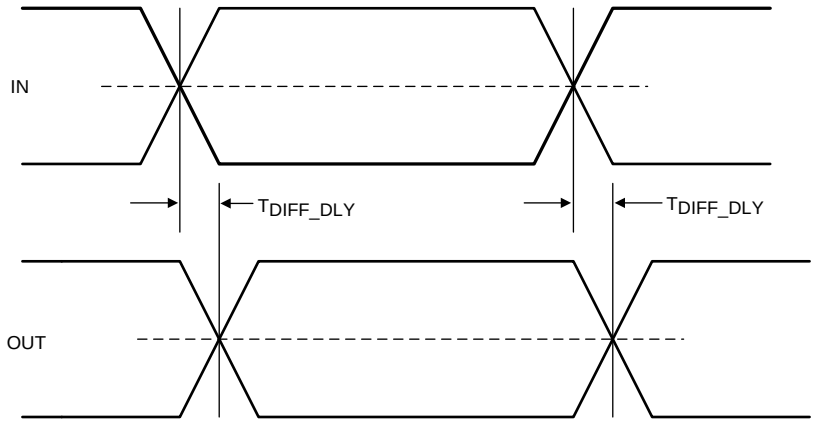


图 7. Propagation Delay

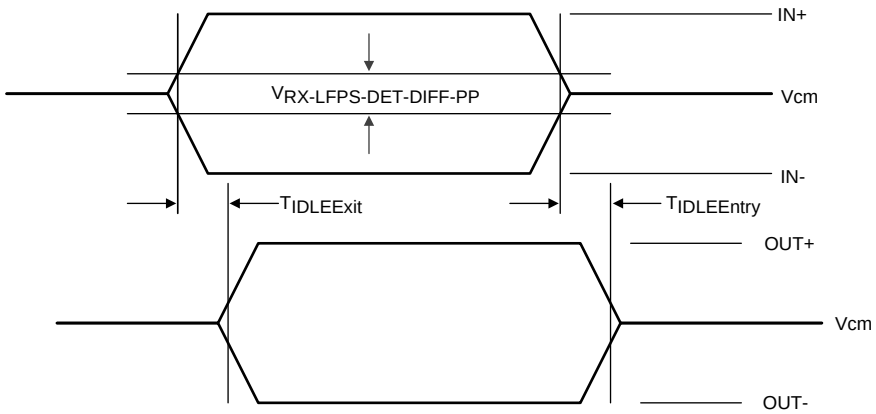


图 8. Electrical Idle Mode Exit and Entry Delay

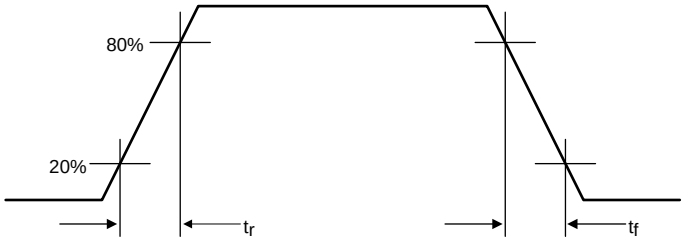


图 9. Output Rise and Fall Times

8 Detailed Description

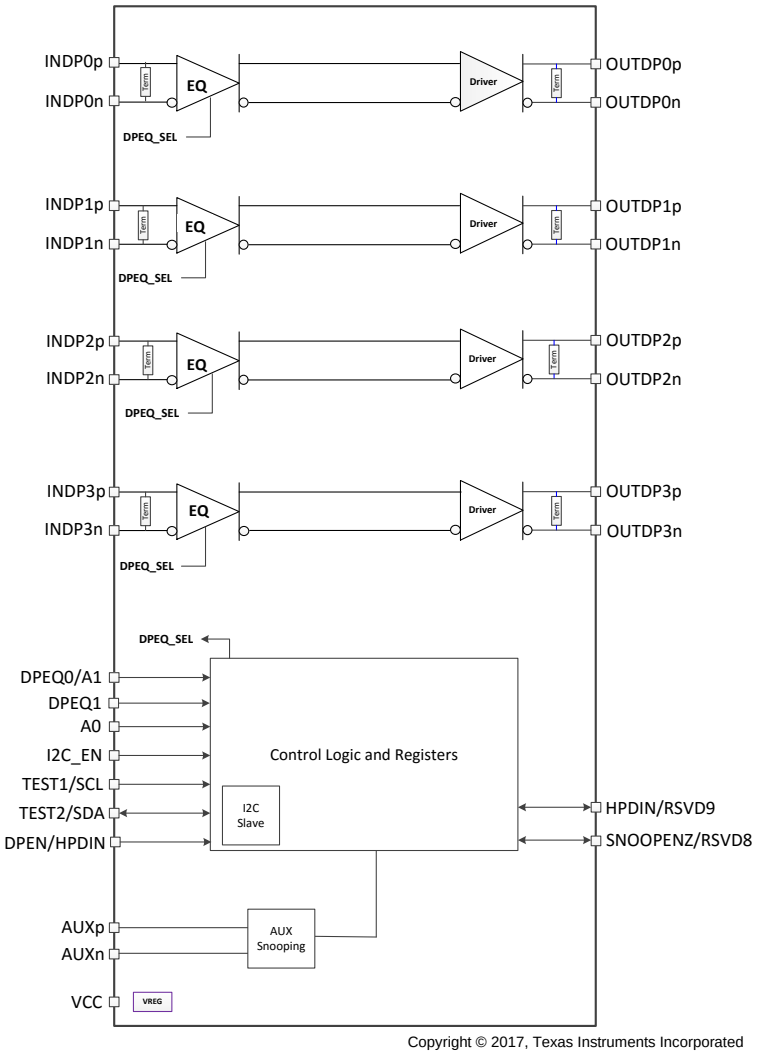
8.1 Overview

The TDP142 is a DisplayPort™ linear re-driver that supports up to 8.1 Gbps for each lane. Additionally, its transparency to the DP link training makes TDP142 a position independent device, suitable for source/sink or cable application.

The TDP142 helps the system to pass compliance of both transmitter and receiver for DisplayPort version 1.4 HBR3. The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. The equalization should be set based on the amount of insertion loss before the TDP142 receivers. The equalization control can be controlled by DPEQ[1:0] pins or I^2C registers.

The device ultra-low-power architecture operates at a 3.3-V power supply and achieves enhanced performance. Also, it comes in a commercial temperature range and industrial temperature range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DisplayPort

The TDP142 supports up to 4 DisplayPort lanes at data rates up to 8.1Gbps (HBR3). The TDP142 monitors the native AUX traffic as it traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TDP142 manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TDP142 snoops native AUX writes to DisplayPort sink's DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE). TDP142 disables/enables lanes based on value written to LANE_COUNT_SET. The TDP142 disables all lanes when SET_POWER_STATE is in the D3. Otherwise active lanes will be based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. Once AUX snoop is disabled, management of TDP142 DisplayPort lanes are controlled through various configuration registers. When TDP142 is enabled for GPIO mode (I2C_EN = "0"), the SNOOPENZ pin can be used to disable AUX snooping. When SNOOPENZ pin is high, the AUX snooping functionality is disabled and all four DisplayPort lanes will be active.

8.3.2 4-level Inputs

The TDP142 has (I2C_EN, A0, and DPEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TDP142 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and pull-down and combine with the external resistor connection to achieve the desired voltage level.

表 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

注

All four-level inputs are latched on rising edge of internal reset. After t_{cfg_hd}, the internal pull-up and pull-down resistors will be isolated in order to save power.

8.3.3 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TDP142. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TDP142 receivers. Two 4-level inputs pins enable up to 16 possible equalization settings. The TDP142 also provides the flexibility of adjusting settings through I^2C registers.

8.4 Device Functional Modes

8.4.1 Device Configuration in GPIO Mode

The TDP142 is in GPIO configuration when I2C_EN = “0”. The DPEN pin controls whether DisplayPort is enabled and SNOOPENZ pin controls whether AUX snoop mode is enabled.

8.4.2 Device Configuration In I²C Mode

The TDP142 is in I²C mode when I2C_EN is not equal to “0”. The same configurations defined in GPIO mode are also available in I²C mode. The TDP142 DisplayPort configuration is programmed based on the *Programming* section .

8.4.3 Linear EQ Configuration

The receiver equalization gain value can be controlled either through I²C registers or through GPIOs. 表 2 details the gain value for each available combination when TDP142 is in GPIO mode. The I²C mode can do the same option or even individual lane EQ setting by updating registers DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, and DP3EQ_SEL.

表 2. TDP142 Receiver Equalization GPIO Control

Equalization Setting #	ALL DISPLAYPORT LANES		
	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	1.0
1	0	R	3.3
2	0	F	4.9
3	0	1	6.5
4	R	0	7.5
5	R	R	8.6
6	R	F	9.5
7	R	1	10.4
8	F	0	11.1
9	F	R	11.7
10	F	F	12.3
11	F	1	12.8
12	1	0	13.2
13	1	R	13.6
14	1	F	14.0
15	1	1	14.4

8.4.4 Operation Timing – Power Up

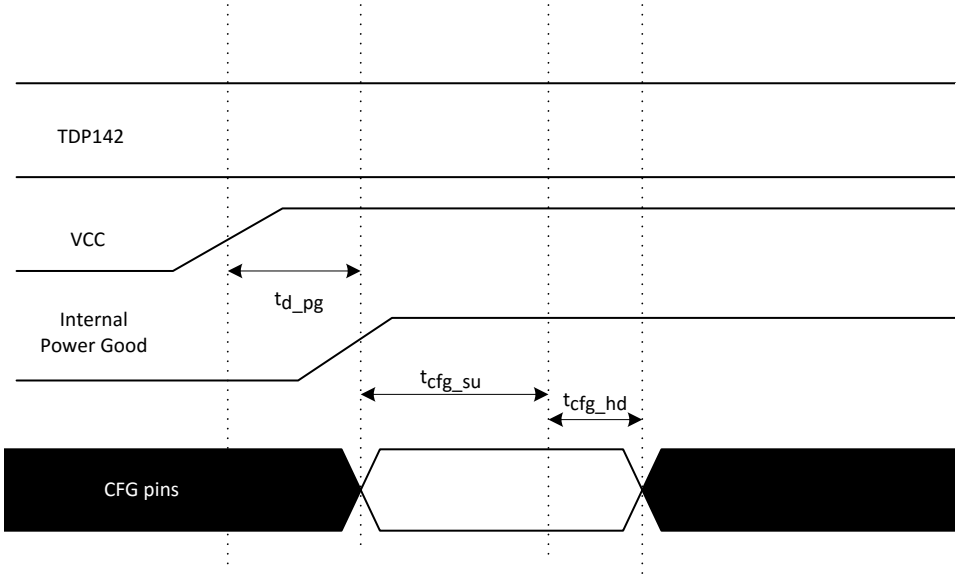


图 10. Power-Up Timing

表 3. Power-Up Timing(1)(2)

PARAMETER		MIN	MAX	UNIT
t_{d_pg}	V_{CC} (minimum) to Internal Power Good asserted high		500	µs
t_{cfg_su}	CFG(1) pins setup(2)	50		µs
t_{cfg_hd}	CFG(1) pins hold	10		µs
t_{VCC_RAMP}	VCC supply ramp requirement		100	ms

(1) Following pins comprise CFG pins: I2C_EN, DPEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at min.

8.5 Programming

For further programmability, the TDP142 can be controlled using I^{2}C. When I2C_EN !=0, the SCL and SDA pins are used for I^{2}C clock and I^{2}C data respectively.

表 4. TDP142 I^{2}C Target Address

DPEQ0/A1 PIN LEVEL	A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

The following procedure should be followed to write to TDP142 I^{2}C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TDP142 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP142 acknowledges the address cycle.
3. The master presents the sub-address (I^{2}C register within TDP142) to be written, consisting of one byte of data, MSB-first.
4. The TDP142 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^{2}C register.
6. The TDP142 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TDP142.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TDP142 I^{2}C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TDP142 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TDP142 acknowledges the address cycle.
3. The TDP142 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I^{2}C register occurred prior to the read, then the TDP142 shall start at the sub-address specified in the write.
4. The TDP142 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^{2}C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TDP142 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I^{2}C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TDP142 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP142 acknowledges the address cycle.
3. The master presents the sub-address (I^{2}C register within TDP142) to be written, consisting of one byte of data, MSB-first.
4. The TDP142 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

注

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I^{2}C master terminates the read operation. If a I^{2}C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

表 5. Register Legend

ACCESS TAG	NAME	MEANING
R	Read	The field may be read by software
W	Write	The field may be written by software
S	Set	The field may be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable

8.6 Register Maps

8.6.1 General Register (address = 0x0A) [reset = 00000001]

图 11. General Registers

7	6	5	4	3	2	1	0
Reserved		SWAP_HPDIN	EQ_OVERRIDE	HPDIN_OVRRIDE	Reserved.	CTLSEL[1:0].	
R		R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 6. General Registers

Bit	Field	Type	Reset	Description
7:6	Reserved	R	00	Reserved.
5	SWAP_HPDIN	R/W	0	0 – HPDIN is in default location (Default) 1 – HPDIN location is swapped (PIN 23 to PIN 32, or PIN 32 to PIN 23).
4	EQ_OVERRIDE	R/W	0	Setting of this field will allow software to use EQ settings from registers instead of value sample from pins. 0 – EQ settings based on sampled state of the EQ pins (DPEQ[1:0]). 1 – EQ settings based on programmed value of each of the EQ registers
3	HPDIN_OVRRIDE	R/W	0	0 – HPD based on state of HPDIN pin (Default) 1 – HPD high.
2	Reserved	R/W	0	Reserved.
1:0	CTLSEL[1:0]	R/W	01	Upon power-on, software must write 2'b10 to enable DisplayPort functionality. If DisplayPort functionality is not required, then software must write 2'b00 to disable DisplayPort. 00 - Shutdown. DP disabled and lowest power state. 01 - DP disabled but not in lowest power state. 10 - DP enabled 11 - Reserved.

8.6.2 DisplayPort Control/Status Registers (address = 0x10) [reset = 00000000]

图 12. DisplayPort Control/Status Registers (0x10)

7	6	5	4	3	2	1	0
DP1EQ_SEL				DP0EQ_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7. DisplayPort Control/Status Registers (0x10)

Bit	Field	Type	Reset	Description
7:4	DP1EQ_SEL	R/W/U	0000	Field selects between 0 to 14dB of EQ for DP lane 1. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 1 based on value written to this field.
3:0	DP0EQ_SEL	R/W/U	0000	Field selects between 0 to 14dB of EQ for DP lane 0. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 0 based on value written to this field.

8.6.3 DisplayPort Control/Status Registers (address = 0x11) [reset = 00000000]

图 13. DisplayPort Control/Status Registers (0x11)

7	6	5	4	3	2	1	0
DP3EQ_SEL				DP2EQ_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8. DisplayPort Control/Status Registers (0x11)

Bit	Field	Type	Reset	Description
7:4	DP3EQ_SEL	R/W/U	0000	Field selects between 0 to 14dB of EQ for DP lane 3. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 3 based on value written to this field.
3:0	DP2EQ_SEL	R/W/U	0000	Field selects between 0 to 14dB of EQ for DP lane 2. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DP lane 2 based on value written to this field.

8.6.4 DisplayPort Control/Status Registers (address = 0x12) [reset = 00000000]

图 14. DisplayPort Control/Status Registers (0x12)

7	6	5	4	3	2	1	0
Reserved	SET_POWER_STATE		LANE_COUNT_SET				
R	RU		RU				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9. DisplayPort Control/Status Registers (0x12)

Bit	Field	Type	Reset	Description
7	Reserved	R	0	Reserved.
6:5	SET_POWER_STATE	R/U	00	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 1'b0, the TDP142 will enable/disable DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1'b1, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 2'b00 by hardware when CTLSEL1 registers changes from a 1'b1 to a 1'b0.
4:0	LANE_COUNT_SET	R/U	00000	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 1'b0, TDP142 will enable DP lanes specified by the snoop value. Unused DP lanes will be disabled to save power. When AUX_SNOOP_DISABLE = 1'b1, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0x0 by hardware when CTLSEL1 register changes from a 1'b1 to a 1'b0.

8.6.5 DisplayPort Control/Status Registers (address = 0x13) [reset = 00000000]

图 15. DisplayPort Control/Status Registers (0x13)

7	6	5	4	3	2	1	0
AUX_SNOOP_DISABLE	Reserved	AUX_SBU_OVR		DP3_DISABLE	DP2_DISABLE	DP1_DISABLE	DP0_DISABLE
R/W	R	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 10. DisplayPort Control/Status Registers (0x13)

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0	0 – AUX snoop enabled. (Default) 1 – AUX snoop disabled.
6	Reserved	R	0	Reserved.
5:4	Reserved	R/W	00	Reserved.
3	DP3_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 3 functionality. 0 – DP Lane 3 Enabled (default) 1 – DP Lane 3 Disabled.
2	DP2_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 2 functionality. 0 – DP Lane 2 Enabled (default) 1 – DP Lane 2 Disabled.
1	DP1_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 1 functionality. 0 – DP Lane 1 Enabled (default) 1 – DP Lane 1 Disabled.
0	DP0_DISABLE	R/W	0	DISABLE. When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 0 functionality. 0 – DP Lane 0 Enabled (default) 1 – DP Lane 0 Disabled.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TDP142 is a linear redriver designed specifically to compensate the inter-symbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cable. It can be used in Source, Sink, and cable applications, where the device is transparent to the link training. For illustrating purposes, this section shows the implementations of Source application and Sink application. 图 16 and 图 17 are the high level block diagram for DisplayPort Source side application and DisplayPort Sink side application respectively, where the TDP142 is snooping both channels of AUX signal and HPD signal.

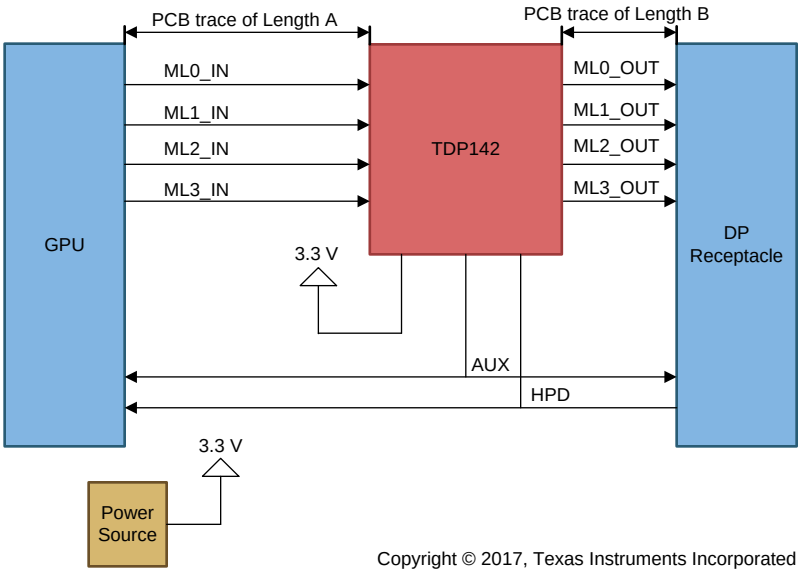


图 16. Source Application for TDP142

Application Information (接下页)

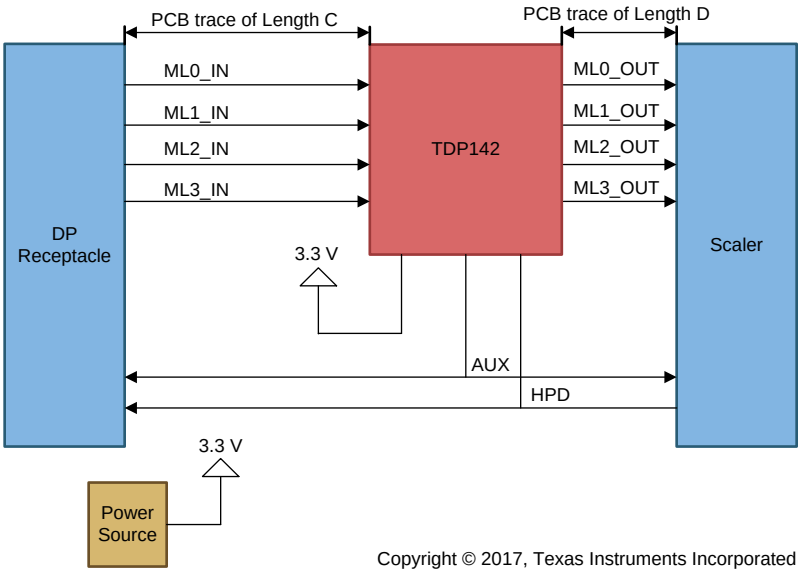


图 17. The Implementation of Sink Application

9.2 Typical Application

9.2.1 Source Application Implementation

图 18 shows the schematic for the Source side application. The TDP142 is placed between the DisplayPort Graphics Processor Unit (GPU) and the DisplayPort receptacle. The TDP142 monitors AUX traffic for power management purposes when SNOOPENZ is low.

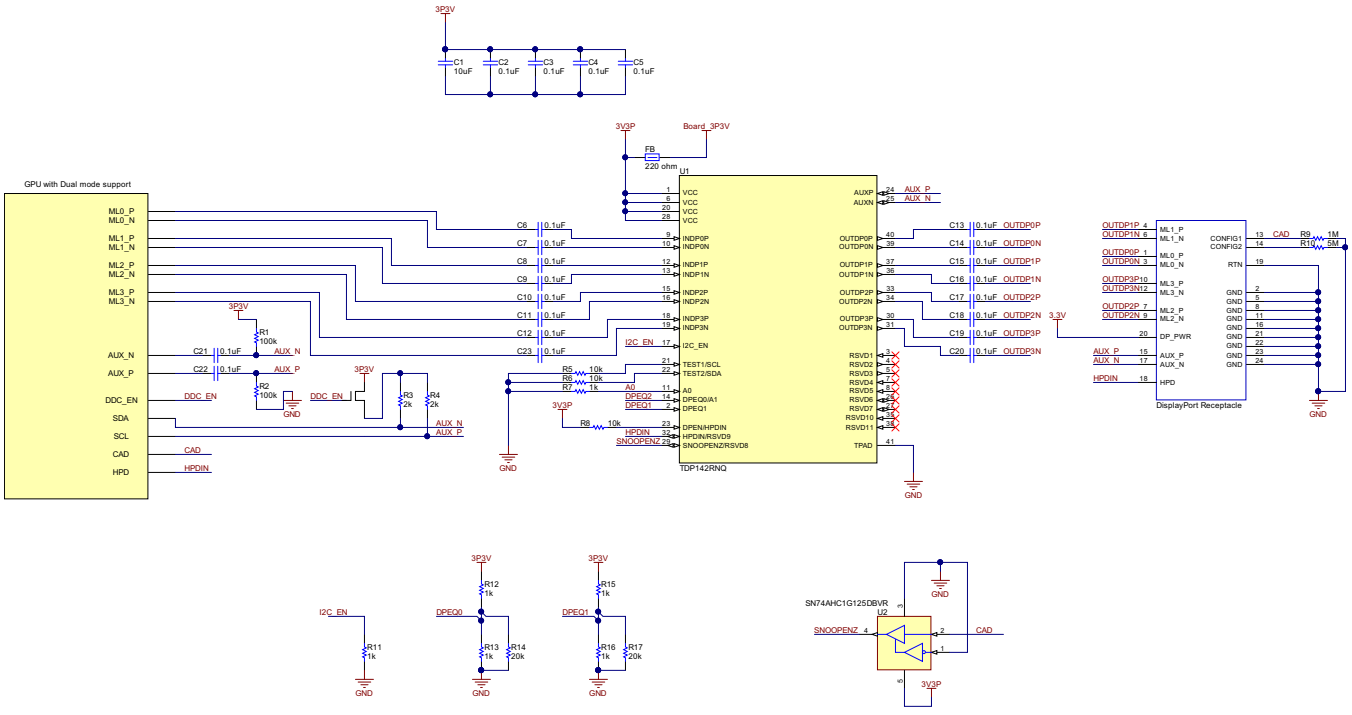


图 18. The Block Diagram of DisplayPort Source Application

9.2.1.1 Design Requirement

The TDP142 can be designed into many types of applications. All applications have certain requirements for the system to work properly. For example, source application uses different hardware configuration on the HPD channel and AUX channel from a sink application. The device can be configured by using I2C. However, the GPIO configuration is provided as I2C is not available in all cases. Additionally, because sources may have different naming conventions, please confirm the link between source and receptacle is correctly mapped through the TDP142.

表 11. Design Parameters

PARAMETER	VALUE
Maximum Operating data rate (RBR, HBR, HBR2, or HBR3)	HBR3 (8.1 Gbps)
Supply voltage	3.3V
Trace length/width of A	12 inch /6 mil width
Trace length/width of B	2 inch/ 6 mil width
Main link AC decoupling capacitor (75 nF to 265 nF)	Recommend 100nF
Control mode (I2C or GPIO)	GPIO (I2C_EN = 0)
Dual Mode DisplayPort Support (Yes/No)	Yes. SNOOPENZ must be connected to CONFIG1 thru a buffer.

9.2.1.2 Detail Design Procedure

Designing in the TDP142 requires the following:

- Determine the loss profile on the DisplayPort input (A) and output (B) channels. See 图 20 for 6 mil trace insertion loss.
- Based upon the loss profile, determine the optimal configuration for the TDP142, to pass electrical compliance. DPEQ[1:0] must be set to appropriate value. For this case, 12-in of FR4 trace approximately equates to 8 dB loss at 4.05 GHz. Therefore, DPEQ1 should be tied 20k ohms to ground and DPEQ0 should be tied 1 kΩ to ground.
- See 图 18 for information of Source application on using the AC coupling capacitors, control pin resistors, and for recommended decouple capacitors from VCC pins to ground.
  - AUX: AUXP should have a 100 kΩ pull-down resistor and AUXN should have a 100 kΩ pull-up resistor. These 100 kΩ resistors must be on the TDP142 side of the 100 nF capacitors.
  - HPDIN is used to enable or disable DisplayPort functionality for power saving. The HPD signal should be routed to either pin 23 or pin 32 based on the GPIO/I2C mode.

表 12. HPD GPIO/I2C Selection

MODE	HPD
GPIO (I2C_EN = 0)	Pin 32
I2C (I2C_EN != 0)	Pin 23

  - For the application supporting Dual mode DisplayPort: SNOOPENZ pin must be connected to the CONFIG1 on DisplayPort Receptacle through a buffer like the SN74AHC125. The buffer is needed because the internal pulldown on SNOOPENZ pin is too strong to register a valid VIH when a Dual mode adapter is plugged into the DisplayPort receptacle.
- Configure the TDP142 using the GPIO terminals or the I2C interface:
  - GPIO – Using the terminals DPEQ0 and DPEQ1.
  - I2C - Refer to the *I2C Register Maps* and the *Programming* section for a detail configuration procedures.
- The thermal pad must be connected to ground.

9.2.2 Sink Application Implementation

图 19 is the schematic for the Sink application, and the left side of TDP142 is connected to DisplayPort receptacle and the right side of TDP142 is connected to Scaler or DisplayPort sink.

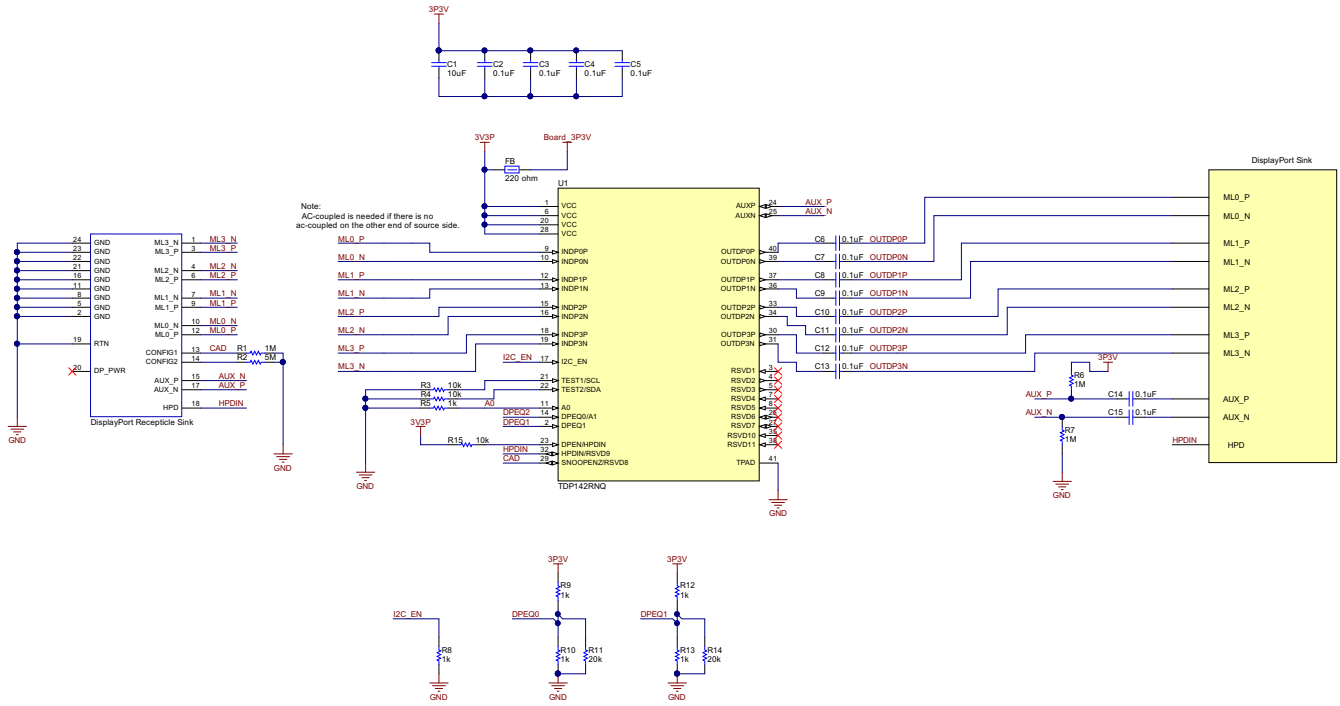


图 19. The Block diagram of DisplayPort Sink Application

9.2.2.1 Design Requirements

For this design example, the parameters listed in 表 13 are used.

表 13. Design Parameters

PARAMETER	VALUE
Maximum Operating data rate (RBR, HBR, HBR2, or HBR3)	HBR3 (8.1Gbps)
Supply voltage	3.3V
Trace length/width of C	12 inch/ 6 mil
Trace length/width of D	2 inch/ 6 mil
Main link AC decoupling capacitor (75 nF to 265 nF)	Recommend 100 nF
Control mode (I2C or GPIO)	GPIO (I2C_EN = 0)

9.2.2.2 Detailed Design Procedure

The design procedure for Sink application is listed as follows:

- Determine the loss profile on the DP input (C) and output (D) channels and cables. See 图 20 for 6 mil trace insertion loss.
- Based upon the loss profile, determine the optimal configuration for the TDP142, to pass electrical compliance.
- See 图 19 for information of Sink application on using the AC coupling capacitors, control pin resistors, and for recommended decouple capacitors from VCC pins to ground.
  - AUX: AUXP has a 1 MΩ pull-up resistor and AUXN should have a 1 MΩ pull-down resistor. Theses 1 MΩ resistors must be on the TDP142 side of the 100 nF capacitors.
  - HPDIN: The HPD signal should be routed to either pin 23 or pin 32 based on the GPIO/I2C mode. In that way, the TDP142 will always be able to conserve power when a source is not connected.

表 14. HPD GPIO/I2C Selection

MODE	HPD
GPIO (I2C_EN = 0)	Pin 32
I2C (I2C_EN != 0)	Pin 23

- Configure the TDP142 using the GPIO terminals or the I2C interface:
  - GPIO – Using the terminals DPEQ0 and DPEQ1.
  - It is recommended to start a higher equalization value like 13 dB and 15 dB first and adjust the value if necessary.
  - I2C - Refer to the *I2C Register Maps* and the *Programming* section for a detail configuration procedures.
- The thermal pad must be connected to ground.

9.2.3 Application Curve

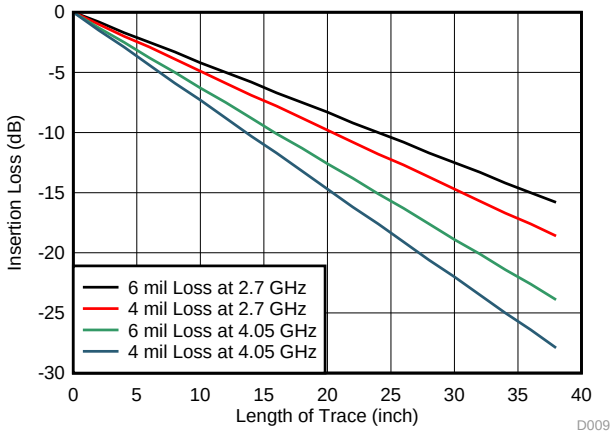


图 20. Insertion Loss of FR4 PCB Traces

10 Power Supply Recommendations

The TDP142 is designed to operate with a 3.3-V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-µF capacitor should be used on each power pin.

11 Layout

11.1 Layout Guidelines

1. INDP[3:0]P/N and OUTDP[3:0]P/N pairs should be routed with controlled 100-Ω differential impedance (±10%).
2. Keep away from other high speed signals.
3. Intra-pair routing should be kept to within 5 mils.
4. Inter-pair skew should be kept within 2 UI according to the *DisaplyPort Design Guide*
5. Length matching should be near the location of mismatch.
6. Each pair should be separated at least by 3 times the signal trace width.
7. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
8. Route all differential pairs on the same of layer.
9. The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
10. Refer to figure 28, the layout might face signal crossing on OUTDP2 and OUTDP3 due to mismatched order between the output pins of the device and the connector. One of the solutions is to do polarity swap on the input of the device when GPU is BGA package. It can minimize the number of VIAS being used.
11. Keep traces on layers adjacent to ground plane.
12. Do NOT route differential pairs over any plane split.
13. Adding Test points will cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

11.2 Layout Example

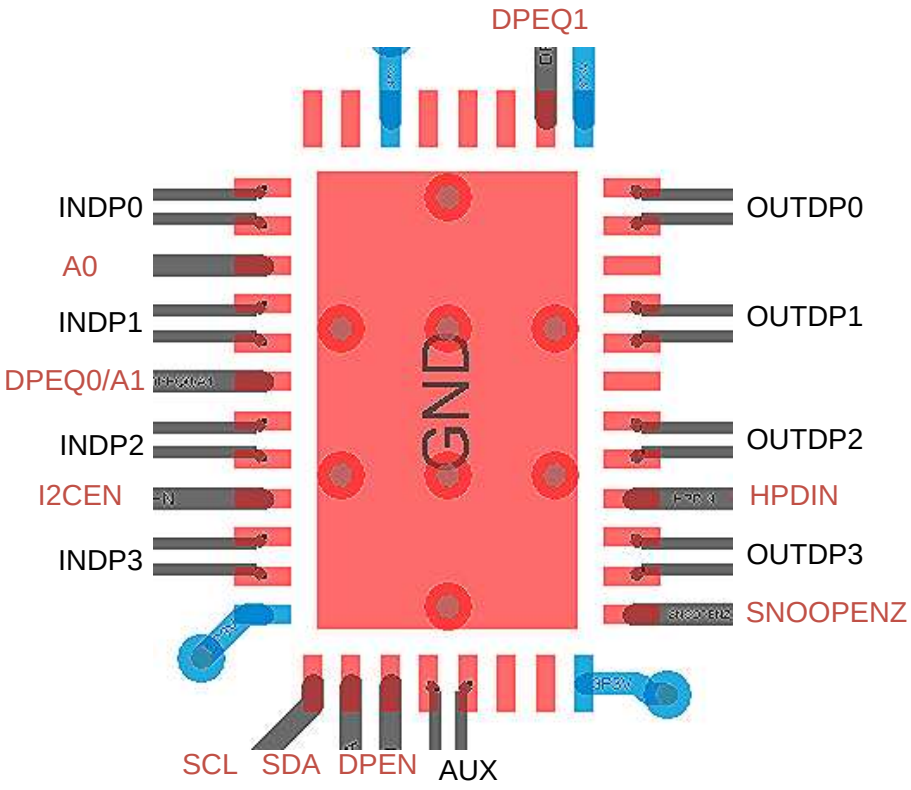


图 21. Layout Example

Layout Example (接下页)

Figure 22 demonstrates the solution of mismatched order between the output of the device and the DisplayPort connector for the source using BGA package. Top image of Figure 22 shows the crossing section between TDP142 and connector. Usually, Vias would be applied to avoid the cross, but using Via can attenuate the signal integrity. Therefore, the polarity swap would be implemented at the input of TDP142. The bottom image shows there is no more crossing section between the TDP142 and connector, which can minimize the number of Vias being used. Note that, the solution is only useful for the source using BGA package.

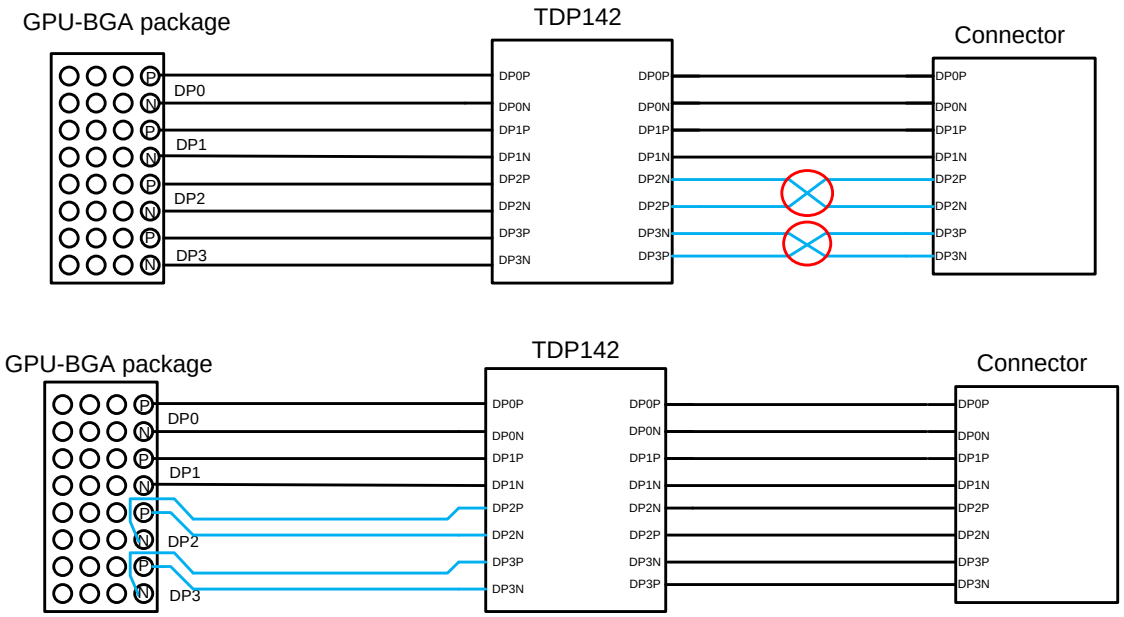


图 22. Layout Example, Top: signal crossing on the output. Bottom: INDP2 and INDP3 Polarity Swap

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **15.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TDP142	单击此处	单击此处	单击此处	单击此处	单击此处
TDP142I	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
DisplayPort is a trademark of VESA.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDP142IRNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TDP142	Samples
TDP142IRNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TDP142	Samples
TDP142RNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TDP142	Samples
TDP142RNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TDP142	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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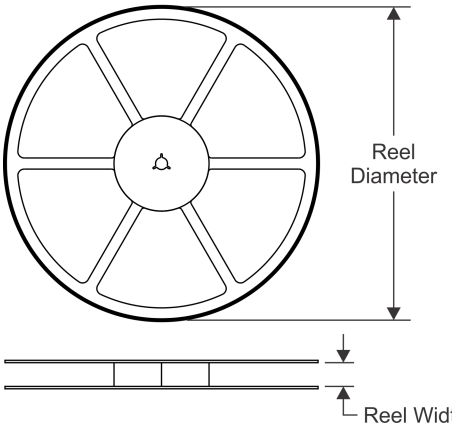
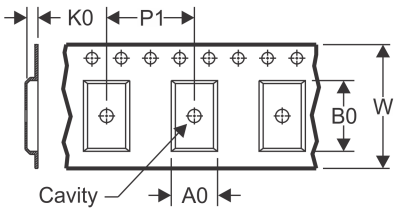
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

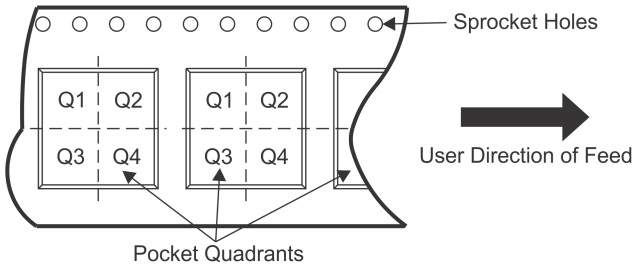


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

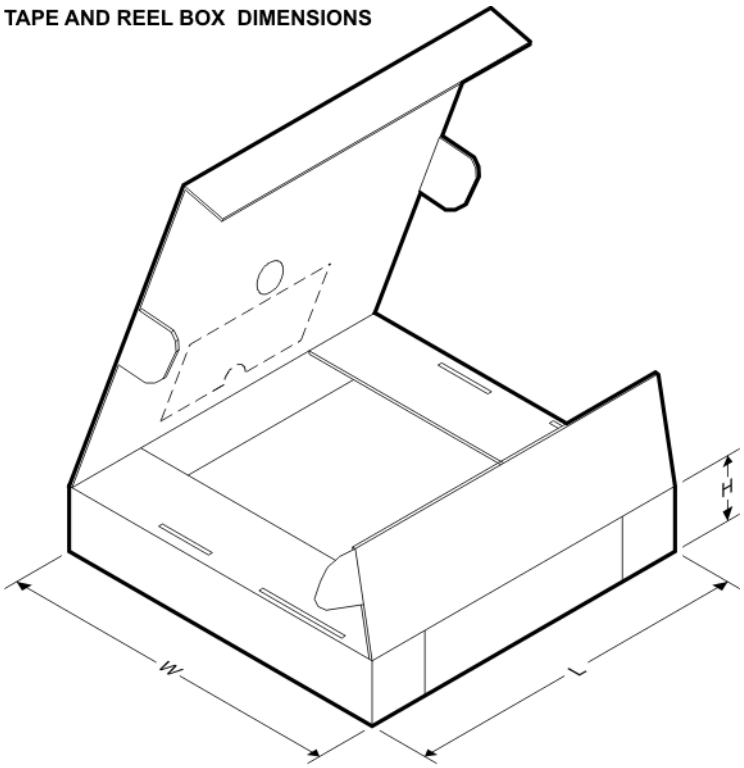
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDP142IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TDP142IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TDP142RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TDP142RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

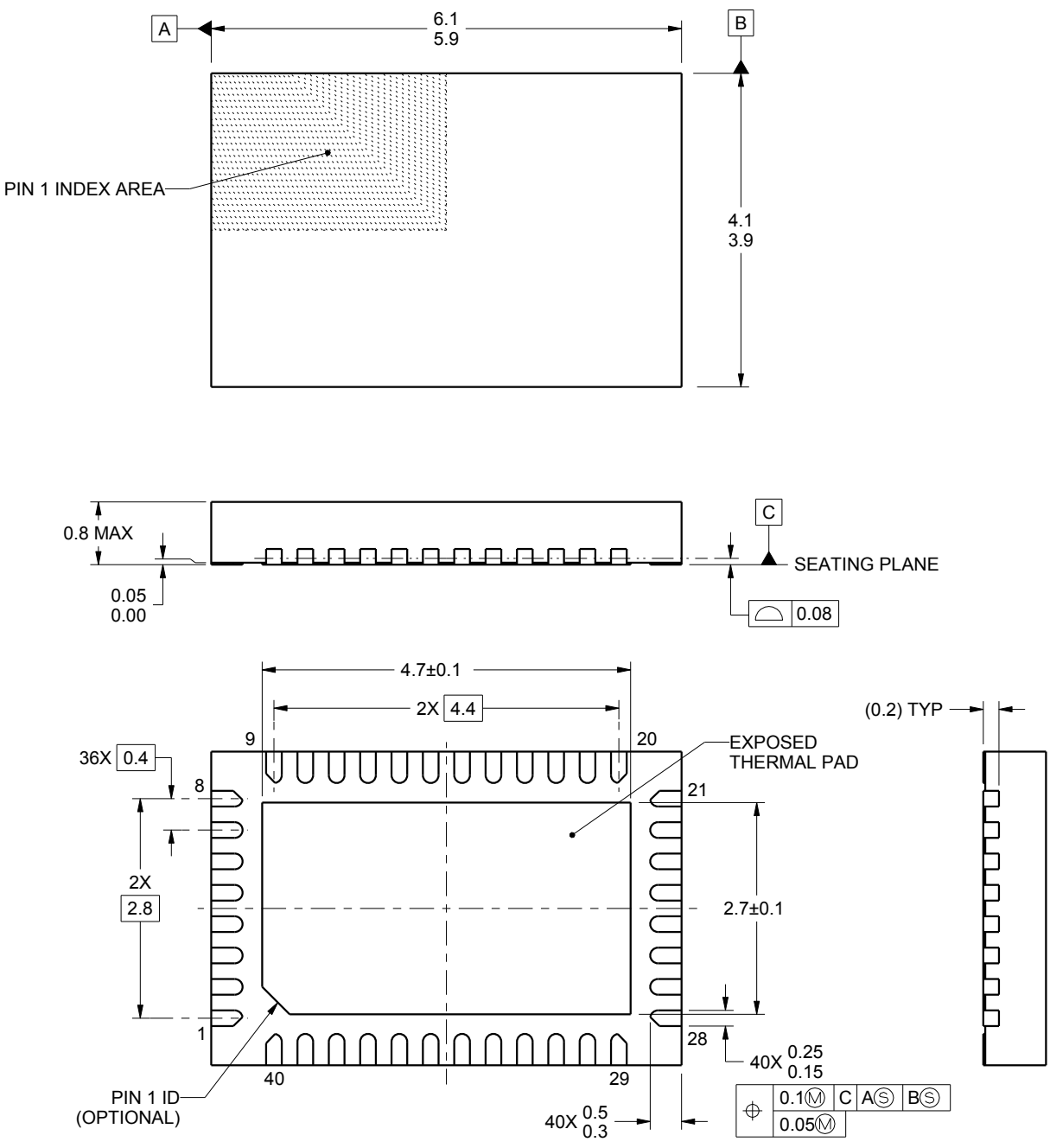
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDP142IRNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TDP142IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0
TDP142RNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TDP142RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNQ0040A

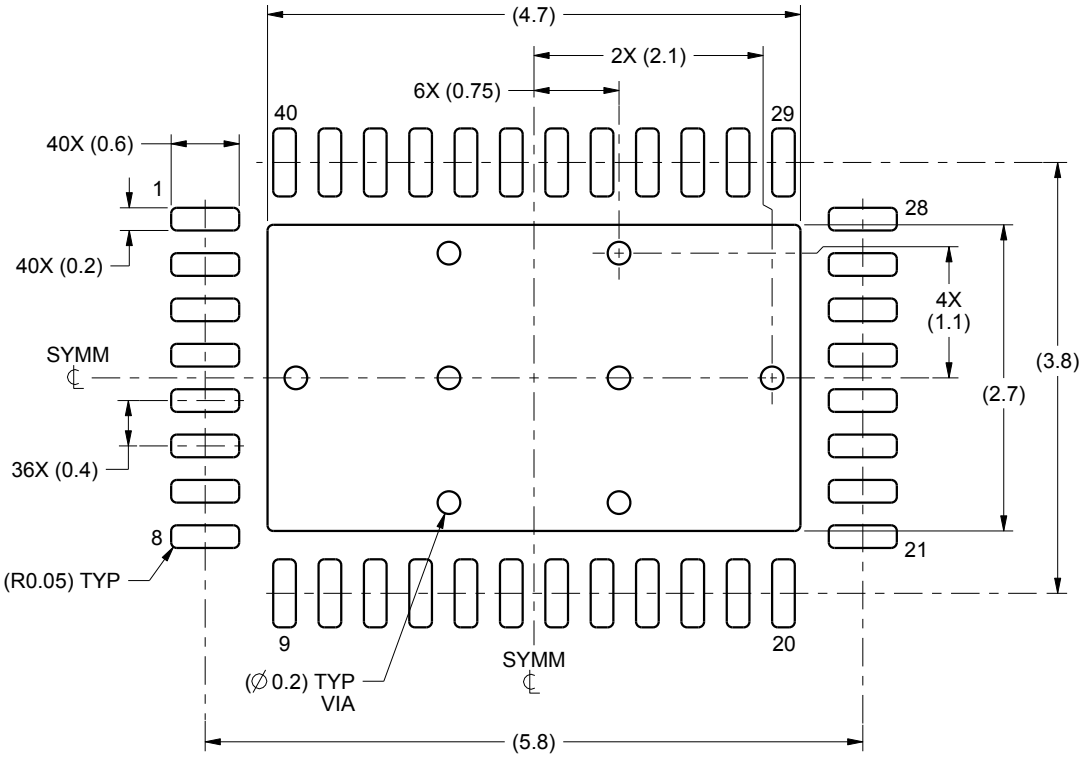
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

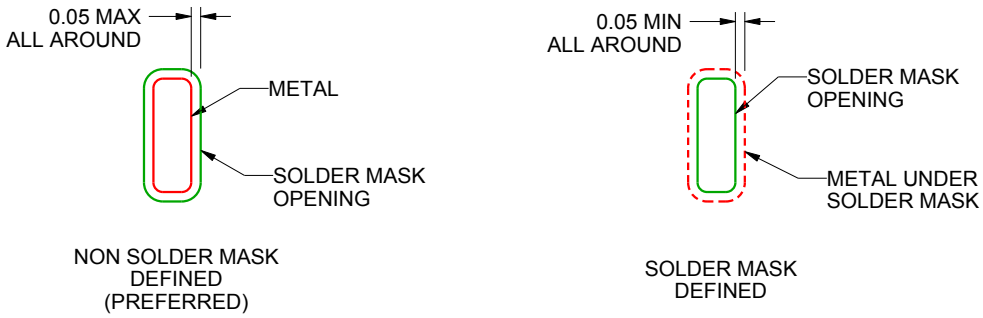


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

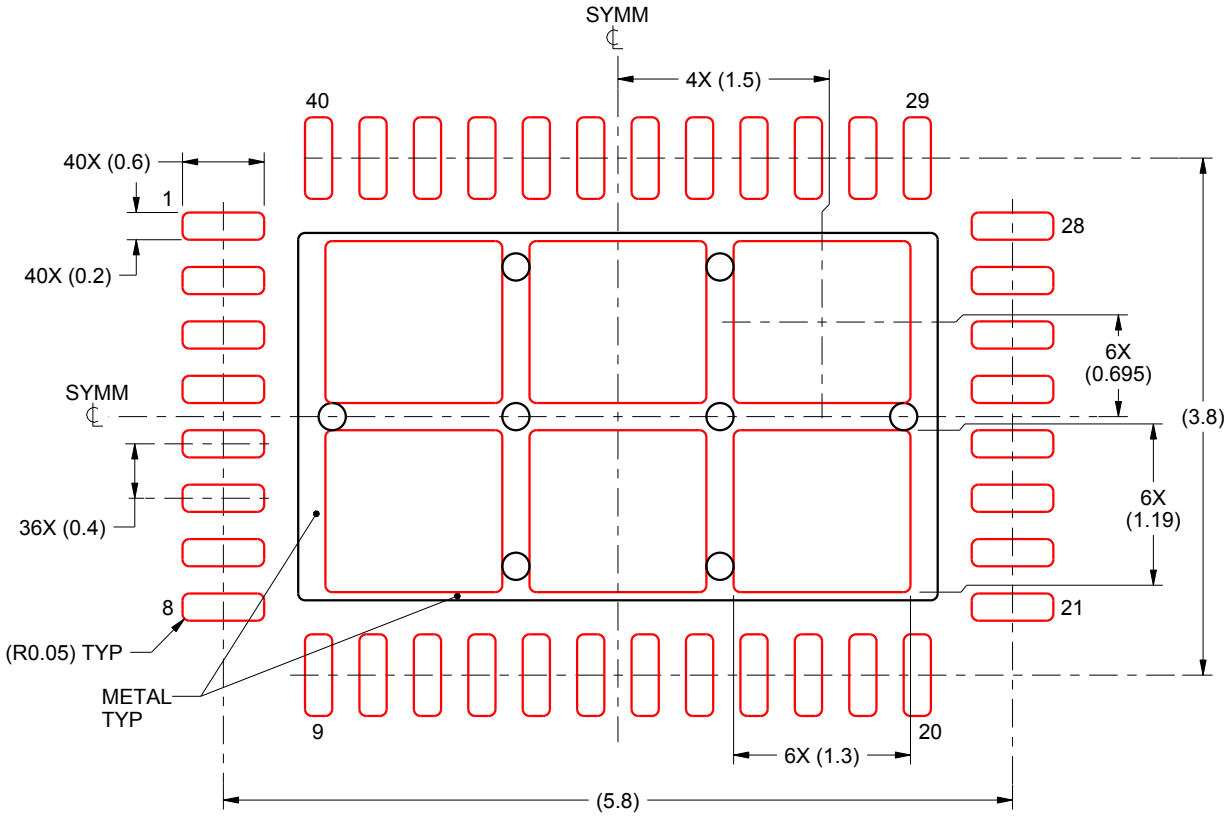


SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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