TMDS181x 6Gbps TMDS 重定时器

1 特性

- HDMI™ 输入端口与输出端口间具有时钟和数据恢复 (CDR) 电路，支持高达 6Gbps 的数据速率
- 在重定时器模式下可兼容高达 6Gbps 的 HDMI™ 电气参数
- 支持 4k2k60p 和高达 WUXGA 16 位色深或 1080p，具有更高的刷新率
- 对输入流重新定时以补偿随机抖动
- 自适应接收器均衡器或可编程固定均衡器
- I^2C 和引脚设置可编程
- 5+ 位对内偏移补偿
- 支持单端模式 ARC
- 链路调试工具包括位于RX 均衡器之后眼图
- 48 引脚 7mm × 7mm 0.5mm 间距超薄型四方扁平无引线 (VQFN) 封装
- 扩展商业温度范围为 0°C 至 85°C (TMDS181)
- 工业温度范围为 -40°C 至 85°C (TMDS181I)

2 应用

- 数字电视
- 数字投影仪
- 音频/视频设备
- Blu-Ray™DVD
- 监视器
- 台式机/一体化计算机
- 有源线缆

3 说明

TMDS181x 是一款数字视频接口 (DVI) 或高清多媒体接口 (HDMI™) 重定时器。TMDS181x 支持四条 TMDS 通道，音频返回通道 (SPDIF_IN/ARC_OUT) 和数字显示控制 (DDC) 接口。TMDS181x 支持高达 6Gbps 的信号传输速率，可实现最高分辨率达 4k2k60p 24 位/像素和高达 WUXGA 16 位色深或 1080p，并且具有较高的刷新率。TMDS181x 经配置可支持 HDMI2.0a 标准。TMDS181x 在低于 1.0Gbps 的数据速率下会自动配置为重驱动器，而在高于该速率时会自动配置为重定时器。重驱动器模式支持 HDMI1.4b，数据速率高达 3.4Gbps

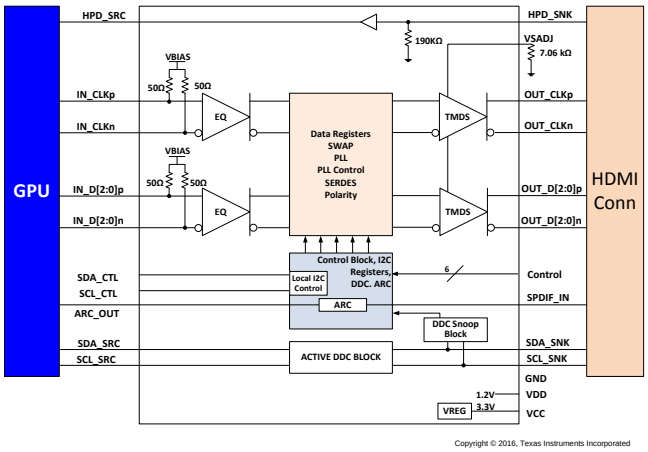
TMDS181x 支持双电源轨（V_{DD} 为 1.2V，V_{CC} 为 3.3V），有助于降低功耗。该器件采用多种电源管理方法来降低整体功耗。TMDS181x 通过 I^2C 或引脚设置支持固定的接收 EQ 增益或自适应接收 EQ 控制，以补偿不同长度的输入电缆或电路板走线。

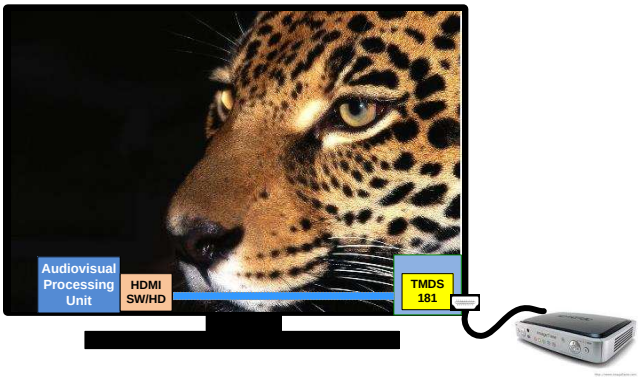
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMDS181	VQFN (48)	7.00mm × 7.00mm
TMDS181I		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图





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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (July 2016) to Revision D — **Page**

- Added Note 5 to the *Power Supply Electrical Characteristic* table ... 8
- Deleted text "which is needed for certain HDMI CTS test." from the third paragraph in the *Overview* section ... 24
- Changed section: *Input Signal Detect Block* ... 28
- Changed H to X in the first row of the HPD_SNK column in Table 12 ... 47
- Changed the IN_Dx column in Table 12 ... 47

Changes from Revision B (April 2016) to Revision C — **Page**

- *Recommended Operating Conditions*, Changed the CONTROL PINS section ... 7
- *DDC, I²C, HPD, and ARC Electrical Characteristics*, Changed the DDC AND I²C section ... 11

Changes from Revision A (October 2015) to Revision B — **Page**

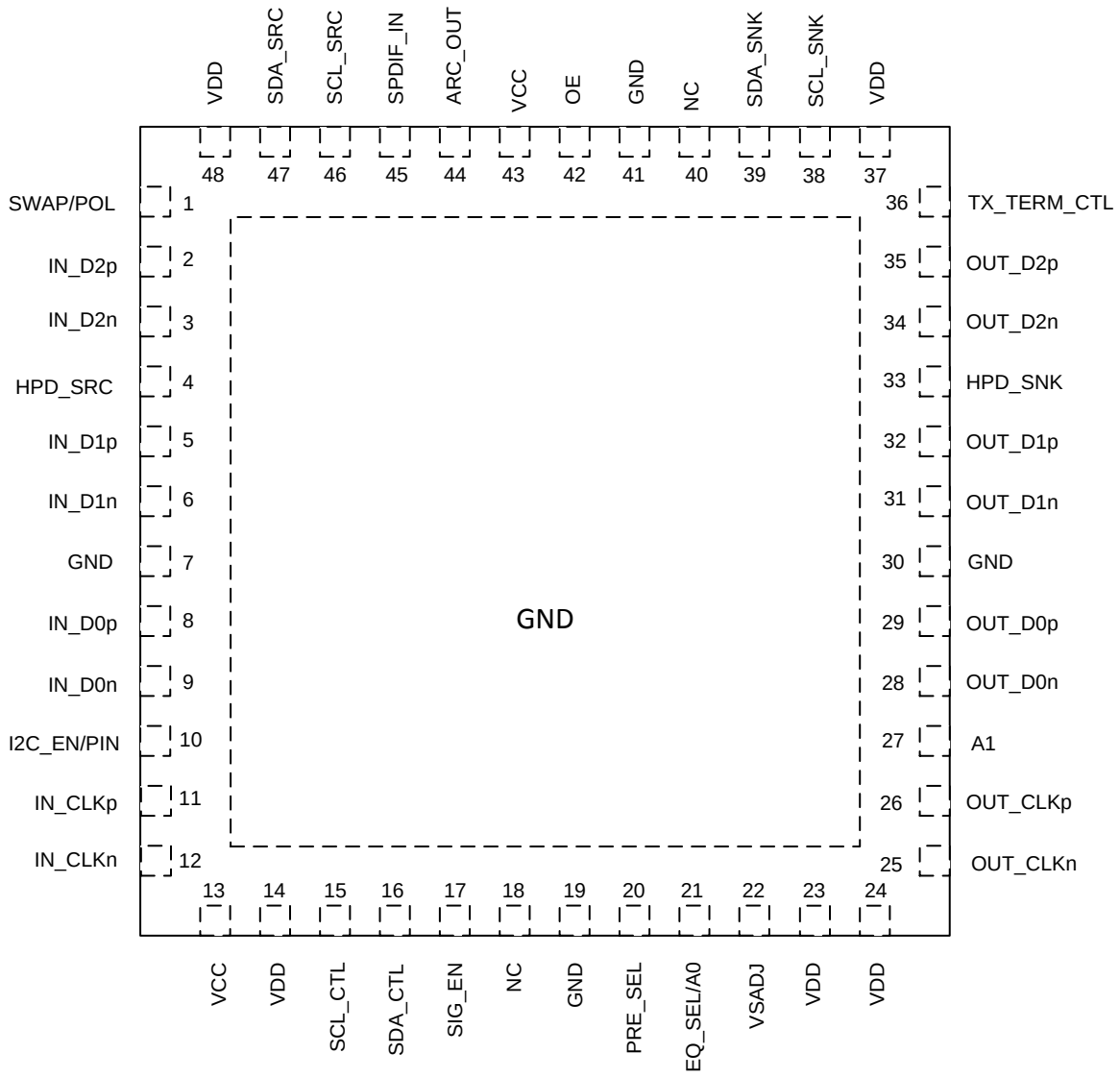
- *Recommended Operating Conditions*, Added V_{IL} "Low-level input voltage at HPD, OE" ... 7
- *Recommended Operating Conditions*, Moved pin OE From: V_{IH} MIN value of 2 V To: V_{IH} MIN value of 2.6 V ... 7
- *Power-Up and Operation Timing Requirements*, Deleted the VDD_ramp and VCC_ramp MIN values ... 12
- Changed Figure 1 ... 12
- *DDC Functional Description* , Changed text "address 22h (see Figure 31) through the I2C interface." To: "address 0Bh through the I2C interface." ... 32
- Added Note to 11–400-kbps in Table 6 ... 35
- Added Note to 11–400-kbps in Table 6 ... 36

Changes from Original (August 2015) to Revision A **Page**

- 已将器件状态从“产品预览”更新为“量产数据” 1
- *Absolute Maximum Ratings*, Changed max value from 1.56 V to VCC + 0.3V; added input current and Min value 6
- *Absolute Maximum Ratings*, Added Max Input Current on Main Link Differential Input pins 6
- *Recommended Operating Conditions*, Updated the note showing the values shown are only for Microcontroller driven and not values based upon pull up or pull down resistors. 7
- *Power Supply Electrical Characteristics*, Increased Max Value of ISD2 from 10 to 15mA 8
- *TMDS Differential Input Electrical Characteristics*, Changed Max Receiver impedance value to 115 9
- *DDC, I^2C, HPD, and ARC Electrical Characteristics*, Inserted values for SCL/SDA_SNK 11
- *TMDS Switching Characteristics*, Changed from 6000 to 3400 13
- Table 4, Deleted Clear and NA Access Tags 34
- Table 8, Removed reg20h[5:4] ARC_SWING 39
- Figure 35, Removed 1k pullup from switch as not needed 43
- *Pin Strapping Configuration for HDMI2.0a and HDMI1.4b* , Added Note for VSADJ resistor value in Compliance Pin Strapping section 46
- *Pin Strapping Configuration for HDMI2.0a and HDMI1.4b* , Changed De-emphasis value from 0 dB to -2 dB for recommended configuration for compliance testing. 46
- *I^2C Control for HDMI2.0a and HDMI1.4b*, Added Note for VSADJ resistor value in Compliance I2C control section and included register that can increase or decrease the VOD swing 46

5 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions(1)

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
VCC	13, 43	P	3.3 V power supply
VDD	14, 23, 24, 37, 48	P	1.2 V power supply
GND	7, 19, 41, 30, Thermal pad	G	Ground
MAIN LINK INPUT PINS			
IN_D2p/n	2, 3	I	Channel 2 differential input
IN_D1p/n	5, 6	I	Channel 1 differential input
IN_D0p/n	8, 9	I	Channel 0 differential input
IN_CLKp/n	11, 12	I	Clock differential input
MAIN LINK OUTPUT PINS (FAIL SAFE)			
OUT_D2n/p	34, 35	O	TMDS data 2 differential output
OUT_D1n/p	31, 32	O	TMDS data 1 differential output
OUT_D0n/p	28, 29	O	TMDS data 0 differential output
OUT_CLKn/p	25, 26	O	TMDS data clock differential output
HOT PLUG DETECT PINS			
HPD_SRC	4	O	Hot plug detect output to source side
HPD_SNK	33	I	Hot plug detect input from sink side
AUDIO RETURN CHANNEL AND DDC PINS			
SPDIF_IN ARC_OUT	45 44	I/O	SPDIF signal input Audio return channel output
SDA_SRC SCL_SRC	47 46	I/O	Source side TMDS port bidirectional DDC data line Source side TMDS port bidirectional DDC clock line
SDA_SNK SCL_SNK	39 38	I/O	Sink side TMDS port bidirectional DDC data line Sink side TMDS port bidirectional DDC clock line
CONTROL PINS			
OE	42	I	Operation enable/reset pin OE = L: Power-down mode OE = H: Normal operation Internal weak pull up: Resets device when transitions from H to L
SIG_EN	17	I	Signal detector circuit enable SIG_EN = L: Signal detect circuit disabled: SIG_EN = H: Signal detect circuit enabled: When no valid clock device enters standby mode. Internal weak pull down
PRE_SEL	20	I 3 level	De-emphasis control when I2C_EN/PIN = Low. PRE_SEL = L: –2 dB PRE_SEL = No Connect: 0 dB PRE_SEL = H: Reserved When I2C_EN/PIN = High de-emphasis is controlled through I^2C
EQ_SEL/A0	21	I 3 level	Input receive equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5 dB at 3 GHz EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14 dB at 3 GHz When I2C_EN/PIN = High address bit 1 Note: 3 level for pin strap programming but 2 level when I^2C address
I2C_EN/PIN	10	I	I2C_EN/PIN = High; puts device into I^2C Control Mode I2C_EN/PIN = Low; puts device into pin strap mode Note: I^2C CSR is addressable at all times, but features that can be controlled by pin strapping can only be changed by I^2C when this pin is pulled high
SCL_CTL	15	I	I^2C clock signal Note: When I2C_EN = Low Pin strapping takes priority and those functions cannot be changed by I^2C

(1) (H) Logic high (pin strapped to VCC through 65 kΩ resistor); (L) Logic Low (pin strapped to GND through 65 kΩ resistor); (for mid-level = No connect)
(2) G = Ground, I = Input, O = Output, P = Power

Pin Functions(1) (continued)

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
SDA_CTL	16	I/0	I^2C data signal Note: When I2C_EN = Low Pin strapping takes priority and those functions cannot be changed by I^2C
VSadj	22	I	TMDS-compliant voltage swing control nominal resistor to GND
A1	27	I	High address bit 2 for I^2C programming Weak internal pull down Note: When in Pin Strapping Mode leave pin as No connect
TX_TERM_CTL	36	I 3 level	Transmit termination control TX_TERM_CTL = H, no transmit termination TX_TERM_CTL = L, transmit termination impedance in approximately 75 to 150 Ω TX_TERM_CTL = No Connect, automatically selects the termination impedance Data rate (DR) > 3.4 Gbps – 75 to 150 Ω differential near end termination 2 Gbps > DR < 3.4 Gbps – 150 to 300 Ω differential near end termination DR < 2 Gbps – no termination Note: If left floating will be in automatic select mode.
SWAP/POL	1	I 3 level	Input lane SWAP and polarity control pin SWAP/POL = H: receive lanes polarity swap (retimer mode only) SWAP/POL = L: receive lanes swap (redriver and retimer mode) SWAP/POL = No Connect: normal operation
NC	18, 40	NA	No connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Supply voltage(3)	V_{CC}	–0.3	4	V
	V_{DD}	–0.3	1.4	
Voltage	Main link input differential voltage (IN_Dx, IN_CLKx) I_{IN} = 15mA	V_{CC} - 0.75V	VCC + 0.3V	V
	TMDS outputs (OUT_Dx)	–0.3	4	
	HPD_SRC, Vsadj, SDA_CTL, SCL_CTL, OE, A1, PRE_SEL, EQ_SEL/A0, I2C_EN/PIN, SIG_EN, TX_TERM_CTL,	–0.3	4	
	HDP_SNK, SDA_SNK, SCL_SNK, SDA_SRC, SCL_SRC	–0.3	6	
Input Current I_{IN}	Main link input current (IN_Dx, IN_CLKx)		15	mA
	Continuous power dissipation	See *Thermal Information*		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage nominal value 3.3 V		3.135	3.3	3.465	V
V_{DD}	Supply voltage nominal value 1.2 V		1.1	1.2	1.27	V
T_{CASE}	Case temperature				92.7	°C
T_A	Operating free-air temperature	TMDS181	0		85	°C
		TMDS181I	–40		85	°C
MAIN LINK DIFFERENTIAL PINS						
V_{ID_PP}	Peak-to-peak input differential voltage		75		1560	mVpp
V_{IC}	Input common mode voltage		V_{CC} – 0.4		V_{CC} + 0.1	V
d_R	Data rate		0.25		6	Gbps
R_{VSADJ}	TMDS compliant swing voltage bias resistor nominal		4.5	7.06		kΩ
CONTROL PINS						
V_{I-DC}	DC input voltage	Control pins	–0.3		3.6	V
V_{IL} (1)	Low-level input voltage at PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL pins only				0.3	V
	Low-level input voltage at OE				0.8	
V_{IM} (1)	Mid-level input voltage at PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL pins only		1	1.2	1.4	V
V_{IH} (1)	High-level input voltage at PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL, OE (2) pins only		2.6			V
V_{OL}	Low-level output voltage				0.4	V
V_{OH}	High-level output voltage		2.4			V
I_{IH}	High-level input current		–30		30	µA
I_{IL}	Low-level input current		–25		25	µA
I_{OS}	Short-circuit output current		–50		50	mA
I_{OZ}	High impedance output current				10	µA
R_{OEPU}	Pullup resistance on OE pin		150		250	kΩ

(1) These values are based upon a microcontroller driving the control pins. The pullup/pulldown/floating resistor configuration will set the internal bias to the proper voltage level which will not match the values shown here.
(2) This value is based upon a microcontroller driving the OE pin. A passive reset circuit using an external capacitor and the internal pullup resistor will set OE pin properly, but may have a different value than shown due to internal biasing.

6.4 Thermal Information

THERMAL METRIC[1][2]		TMDS181x RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Test conditions for Ψ_{JB} and Ψ_{JT} are clarified in the *Semiconductor and IC Package Thermal Metrics*.

6.5 Power Supply Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX[2]	UNIT
P_{D1}[3][4]	Device power dissipation (retimer operation)	OE = H, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V IN_Dx: V_{ID_PP} = 1200 mV, 6 Gbps TMDS pattern, V_I = 3.3 V, I2C_EN/PIN = L, PRE_SEL= NC, EQ_SEL= NC, SDA_CTL/CLK_CTL = 0 V			800	900	mW
P_{D2}[3][4]	Device power dissipation (redriver operation)	OE = H, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V IN_Dx: V_{ID_PP} = 1200 mV, 2.97 Gbps TMDS pattern, V_I = 3.3 V, I2C_EN/PIN = L, PRE_SEL= NC, EQ_SEL= H, SDA_CTL/CLK_CTL = 0 V			500	600	mW
P_{SD1}[3][4][5]	Device power in standby	OE = H, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V, HPD = H, No valid input signal			50	100	mW
P_{SD2}[3][4][5]	Device power in power down	OE = L, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V			10	30	mW
I_{CC1}[3][4]	VCC supply current (TMDS 6Gpbs retimer mode)	OE = H, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V IN_Dx: V_{ID_PP} = 1200 mV, 6 Gbps TMDS pattern I2C_EN/PIN = L, PRE_SEL = NC, EQ_CTL = NC, SDA_CTL/CLK_CTL = 0 V			131	150	mA
I_{DD1}[3][4]	VDD supply current (TMDS 6Gpbs retimer mode)	OE = H, V_{CC} = 3.3 V/3.465 V, VDD = 1.2 V/1.27 V IN_Dx: V_{ID_PP} = 1200 mV, 6 Gbps TMDS pattern I2C_EN/PIN = L, PRE_SEL = NC, EQ_CTL = NC, SDA_CTL/CLK_CTL = 0 V			332	350	mA
I_{CC2}[3][4]	VCC supply current (TMDS 6Gpbs redriver mode)	OE = H, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V IN_Dx: V_{ID_PP} = 1200 mV, 2.97 Gbps TMDS pattern I2C_EN/PIN = L, PRE_SEL = NC, EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V			92		mA
I_{DD2}[3][4]	VDD supply current (TMDS 6Gpbs redriver mode)	OE = H, V_{CC}= 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V IN_Dx: V_{ID_PP} = 1200 mV, 3.4 Gbps TMDS pattern I2C_EN/PIN = L, PRE_SEL = NC, EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V			187		mA
I_{SD1}[5]	Standby current	OE = H, V_{CC} = 3.3 V/3.465 V, VDD = 1.2 V/1.27 V, HPD = H: No valid signal on IN_CLK	3.3 V rail[3]		6	15	mA
			1.2 V rail		40	50	
I_{SD2}[5]	Power-down current	OE = L, V_{CC} = 3.3 V/3.465 V, V_{DD} = 1.2 V/1.27 V	3.3 V rail[3]		2	5	mA
			1.2 V rail		3.5	15	

(1) The typical rating is simulated at 3.3 V V_{CC} and 1.2 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The maximum rating is simulated at 3.465 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted
(3) I_{CC} is a direct result of the source design as the TMDS181x integrated receive termination resistor accounts for 85 to 110 mA.
(4) I_{DD} is impacted by ARC usage. Connecting a 500 kΩ resistor to GND at SPDIF reduces the value by more than 20 mA
(5) The measurements were made with no active source connected.

6.6 TMDS Differential Input Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$D_{R\_RX\_DATA\_RT}$	TMDS data lanes data rate (Retimer Mode)		0.25		6	Gbps
$D_{R\_RX\_DATA\_RD}$	TMDS data lanes data rate (Redriver Mode)		0.25		3.4	Gbps
$D_{R\_RX\_CLK}$	TMDS clock lanes clock rate		25		340	MHz
t_{RX_DUTY}	Input clock duty circle		40%	50%	60%	
t_{CLK_JIT}	Input clock jitter tolerance				0.3	Tbit
t_{DATA_JIT}	Input data jitter tolerance	Test the TTP2, see Figure 12			150	ps
t_{RX_INTRA}	Input intrapair skew tolerance	Test at TTP2 when DR = 1.6 Gbps, see Figure 12	112			ps
t_{RX_INTER}	Input interpair skew tolerance				1.8	ns
$E_{QH(D)}$	Fixed EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0 = H; fixed EQ gain, test at 6 Gbps		15		dB
$E_{QL(D)}$	Fixed EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0 = L; fixed EQ gain, test at 6 Gbps		7.5		dB
$E_{QZ(D)}$	Adaptive EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0 = NC; adaptive EQ (Retimer Mode Only)	2		15	dB
$E_{Q(c)}$	EQ gain for clock lane IN_CLKn/p	EQ_SEL/A0 = H,L,NC		3		dB
R_{INT}	Input differential termination impedance		85	100	115	Ω
V_{ITERM}	Input termination voltage	OE = H		3.3	3.465	V

(1) The typical rating is simulated at 3.3 V V_{CC} and 1.2 V V_{DD} and at 27°C unless otherwise noted
(2) The maximum rating is simulated at 3.465 V V_{CC} and 1.27 V V_{DD} and at 85°C unless otherwise noted

6.7 TMDS Differential Output Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
V_{OH}	Single-ended high level output voltage Data rate ≤1.65 Gbps	PRE_SEL = NC; TX_TERM_CTL = H; OE = H; DR = 750 Mbps; VSadj = 7.06 kΩ;	V_{CC} – 10		V_{CC} + 10	V
	Single-ended high level output voltage Data rate >1.65 Gbps and <3.4 Gbps	PRE_SEL = NC; TX_TERM_CTL = NC; OE = H; DR = 2.97 Gbps; VSadj = 7.06 kΩ;	V_{CC}-200		V_{CC} + 10	
	Single-ended high level output voltage Data rate >3.4 Gbps and < 6 Gbps(2)	PRE_SEL = NC; TX_TERM_CTL = L; OE = H; DR = 6 Gbps; VSadj = 7.06 kΩ;	V_{CC} – 400		V_{CC} + 10	
V_{OL}	Single-ended low level output voltage Data rate ≤1.65 Gbps	PRE_SEL = NC; TX_TERM_CTL = H; OE = H; DR = 750 Mbps; VSadj = 7.06 kΩ;	V_{CC} – 600		V_{CC} – 400	V
	Single-ended low level output voltage Data rate >1.65 Gbps and <3.4 Gbps	PRE_SEL = NC; TX_TERM_CTL = NC; OE = H; DR = 2.97 Gbps; VSadj = 7.06 kΩ;	V_{CC} – 700		V_{CC} – 400	
	Single-ended low level output voltage Data rate >3.4 Gbps and < 6 Gbps(2)	PRE_SEL = NC; TX_TERM_CTL = L; OE = H; DR = 6 Gbps; VSadj = 7.06 kΩ;	V_{CC} – 1000		V_{CC} – 400	
V_{SWING_DA}	Single-ended output voltage swing on data lane	PRE_SEL = NC; TX_TERM_CTL = H/NC/L; OE = H; DR = 270 Mbps/2.97/6 Gbps VSadj = 7.06 kΩ;	400	500	600	mV
V_{SWING_CLK}	Single-ended output voltage swing on clock lane	PRE_SEL = NC; TX_TERM_CTL = H; OE = H; Data rate ≤ 3.4 Gbps; VSadj = 7.06 kΩ;	400	500	600	mV
		PRE_SEL = NC; TX_TERM_CTL = NC; OE = H; Data rate > 3.4 Gbps; VSadj = 7.06 kΩ;	200	300	400	
ΔV_{SWING}	Change in single-end output voltage swing per 100 Ω ΔVSadj			20		mV
$\Delta V_{OCM(SS)}$	Change in steady state output common mode voltage between logic levels		–5		5	mV
$V_{OD(PP)}$	Output differential voltage before pre-emphasis	V_{SADJ} = 7.06 kΩ; PRE_SEL = NC see Figure 10	800		1200	mV
$V_{OD(SS)}$	Steady state output differential voltage	V_{SADJ} = 7.06 kΩ; PRE_SEL = L, see Figure 11	600		1075	mV
V_{OD_range}	Total TMDS data lanes output differential voltage for HDMI2.0. Retimer Mode Only See Figure 14	3.4 Gbps < R_{bit} ≤ 3.712 Gps TX_TERM_CTL = NC; PRE_SEL = NC; OE = H; VSadj = 7.06 kΩ;	335			mV
		3.712 Gbps < R_{bit} < 5.94 Gbps TX_TERM_CTL = NC; PRE_SEL = NC; OE = H; VSadj = 7.06 kΩ;	–19.66 × (R_{bit}^2) + (106.74 × R_{bit}) + 209.58			
		5.94 Gbps ≤ R_{bit} ≤ 6.0 Gbps TX_TERM_CTL = NC; PRE_SEL = NC; OE = H; VSadj = 7.06 kΩ;	150			
I_{OS}	Short-circuit current limit	Main link output shorted to GND			50	mA
I_{LEAK}	Failsafe condition leakage current	V_{CC} = 0 V; V_{DD} = 0 V; TMDS Outputs pulled to 3.3 V through 50 Ω resistor;			45	μA
R_{TERM}	Source termination resistance for HDMI2.0		75		150	Ω

(1) The typical rating is simulated at 3.3 V V_{CC} and 1.2 V V_{DD} and at 27°C unless otherwise noted
(2) The maximum rating is simulated at 3.465 V V_{CC} and 1.27 V V_{DD} and at 85°C unless otherwise noted

6.8 DDC, I²C, HPD, and ARC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
DDC AND I²C						
$V_{I\text{-}DC}$	SCL/SDA_SNK, SCL/SDA_SRC DC input voltage		–0.3		5.5	V
	SCL/SDA_CTL, DC input voltage		–0.3		3.6	V
V_{IL}	SCL/SDA_SNK, SCL/SDA_SRC Low level input voltage				0.3 x V_{CC}	V
	SCL/SDA_CTL Low level input voltage				0.3 x V_{CC}	V
V_{IH}	SCL/SDA_SNK, SCL/SDA_SRC high level input voltage		3			V
	SCL/SDA_CTL high level input voltage		0.7 x V_{CC}			V
V_{OL}	SCL/SDA_CTL, SCL/SDA_SRC low level output voltage	I_0 = 3 mA and V_{CC} > 2 V			0.4	V
		I_0 = 3 mA and V_{CC} < 2 V			0.2 x V_{CC}	
f_{SCL}	SCL clock frequency fast I2C mode for local I2C control				400	kHz
C_{bus}	Total capacitive load for each bus line (DDC and local I2C pins)				400	pF
HPD						
V_{IH}	High-level input voltage	HPD_SNK	2.1			V
V_{IL}	Low-level input voltage	HPD_SNK			0.8	V
V_{OH}	High-level output voltage	I_{OH} = –500 µA; HPD_SRC,	2.4		3.6	V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA; HPD_SRC,	0		0.1	V
I_{LEAK}	Failsafe condition leakage current	V_{CC} = 0 V; V_{DD} = 0 V; HPD_SNK = 5 V;			40	µA
I_{H_HPD}	High-level input current	Device powered; V_{IH} = 5 V; I_{H_HPD} includes R_{pdHPD} resistor current			40	µA
		Device powered; V_{IL} = 0.8 V; I_{L_HPD} includes R_{pdHPD} resistor current			30	
R_{pdHPD}	HPD input termination to GND	V_{CC} = 0 V	150	190	220	kΩ
SPDIF AND ARC						
V_{EL}	Operating DC voltage for single mode ARC output	Test at ARC_OUT, see Figure 22	0		5	V
V_{IN_DC}	Operating DC voltage for SPDIF input				0.05	V
V_{SP_SW}	Signal amplitude of SPDIF input		0.2	0.5	0.6	V
$V_{EISWING}$	Signal amplitude on the ARC output	Test at ARC_OUT, 55 Ω external termination resistor, see Figure 22	0.4	0.5	0.6	V
CLK_ARC	Signal frequency on ARC	Test at ARC_OUT, see Figure 22	3.687	5.645 ±0.1%	13.517	MHz
Duty cycle	Output clock duty cycle		45%	50%	55%	
Data rate	SPDIF input DR		7.373	11.29	27.034	Mbps
t_{EDGE}	Rise/fall time for ARC output	From 10% to 90% voltage level			0.4	UI
$R_{\_IN\_SPDIF}$	Input termination resistance for SPDIF			75		Ω
R_{est}	Single mode output termination resistance	0.1 MHz to 128× the maximum frame rate	36	55	75	Ω

(1) The typical rating is simulated at 3.3 V V_{CC} and 1.2 V V_{DD} and at 27°C unless otherwise noted
(2) The maximum rating is simulated at 3.465 V V_{CC} and 1.27 V V_{DD} and at 85°C unless otherwise noted

6.9 Power-Up and Operation Timing Requirements

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
t_{d1}	V_{DD} stable before V_{CC}	0		200	µs
t_{d2}	V_{DD} and V_{CC} stable before OE assertion	100			µs
t_{d3}	CDR active operation after retimer mode initial			15	ms
t_{d4}	CDR turn off time after retimer mode de-assert			120	ns
VDD_ramp	V_{DD} supply ramp up requirements			100	ms
VCC_ramp	V_{CC} supply ramp up requirements			100	ms

(1) See *Operation Timing* for more information

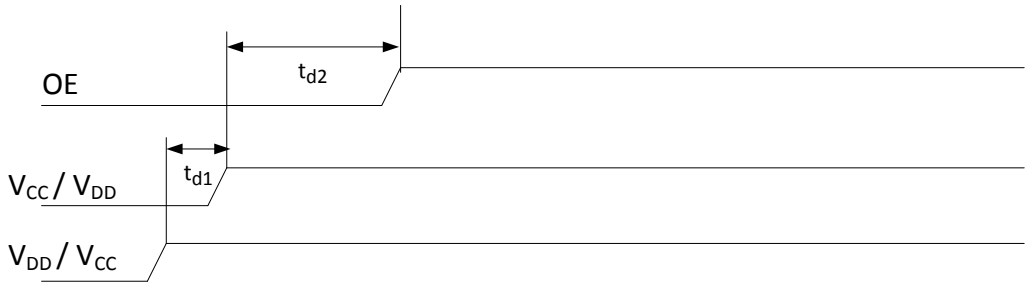


Figure 1. Power-Up Timing for TMDS181

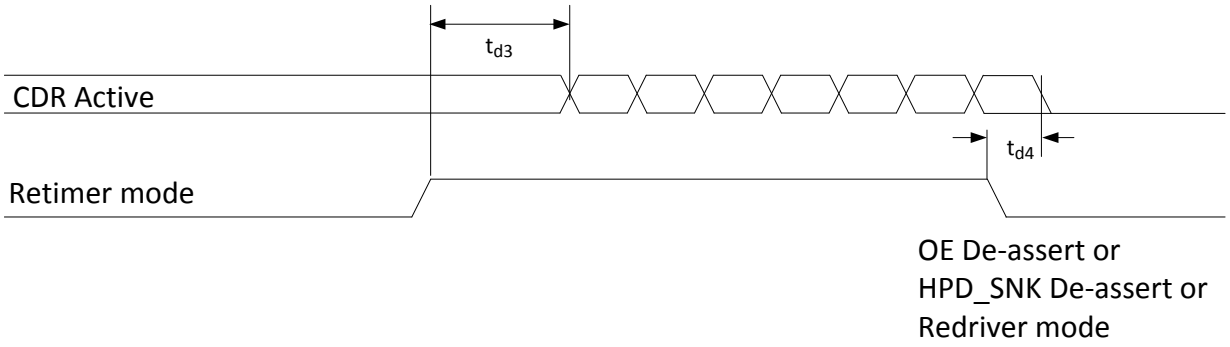


Figure 2. CDR Timing for TMDS181

6.10 TMDS Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
REDRIVER MODE						
d_R	Data rate (redriver mode)		250		3400	Mbps
t_{PLH}	Propagation delay time (low to high)		250		600	ps
t_{PHL}	Propagation delay time (high to low)		250		800	ps
$t_{T1(1.4b)}$	Transition time (rise and fall time); measured at 20% and 80% levels for data lanes. TMDS clock meets t_{T3} for all three times.	TX_TERM_CTL = NC; PRE_SEL = NC; OE = H; 1.48 Gbps and 2.97 Gbps data lines, 148 MHz and 297 MHz clock	75			ps
t_{T3}		TX_TERM_CTL = NC; PRE_SEL = NC; OE = H; 1.48 Gbps, 2.97 Gbps	100			ps
t_{SK_INTRA}	Intra-pair output skew	Default setting for internal intra-pair skew adjust, TX_TERM_CTL = NC; PRE_SEL = NC; 1.48 Gbps, 2.97 Gbps; See Figure 8			40	ps
t_{SK_INTER}	Inter-pair output skew	Default setting for internal inter-pair skew adjust, TX_TERM_CTL = NC; PRE_SEL = NC; 1.48 Gbps, 2.97 Gbps; See Figure 8			100	ps
$t_{JITD1(1.4b)}$	Total output data jitter HDMI1.4b	DR = 2.97 Gbps, PRE_SEL = NC, EQ_SEL/A0 = NC ; . See Figure 12 at TTP3			0.2	Tbit
$t_{JITC1(1.4b)}$	Total output clock jitter	CLK = 25 MHz, 74.25 MHz, 75 MHz, 150 MHz, 297 MHz			0.25	Tbit
RETIMER MODE						
d_R	Data rate (retimer mode)		0.25		6	Gbps
d_{XVR}	Automatic redriver to retimer crossover (when selected)	Measured with input signal applied = 200 mVpp	0.75	1	1.25	Gbps
$f_{CROSSOVER}$	Crossover frequency hysteresis			250		MHz
$PLLB_W$	Data retimer PLL bandwidth	Default loop bandwidth setting		0.4	1	MHz
t_{ACQ}	Input clock frequency detection and retimer acquisition time			180		µs
I_{JT1}	Input clock jitter tolerance	Tested when data rate >1.0Gbps			0.3	Tbit
$t_{T1(2.0)}$	Transition time (rise and fall time); measured at 20% and 80% levels for data lanes. TMDS clock meets t_{T3} for all three times.	TX_TERM_CTL = L; PRE_SEL = NC; 6 Gbps data lines,	45			ps
$t_{T1\ (1.4b)}$		TX_TERM_CTL = NC; PRE_SEL = NC; 1.48 Gbps and 2.97 Gbps data lines, 148 MHz and 297 MHz clock	75			ps
t_{T3}		TX_TERM_CTL = NC; PRE_SEL = NC; 1.48 Gbps, 2.97 Gbps, 6 Gbps data lines, 148 MHz, 297 MHz clock	100			ps
t_{DCD}	OUT_CLK ± duty cycle		40%	50%	60%	
t_{SK_INTER}	Inter-pair output skew	Default setting for internal inter-pair skew adjust, TX_TERM_CTL = NC; PRE_SEL = NC; 1.48 Gbps, 2.97 Gbps, 6 Gbps data lines, 148 MHz, 297 MHz clock; See Figure 8			0.2	Tch
t_{SK_INTRA}	Intra-pair output skew	Default setting for internal intra-pair skew adjust, TX_TERM_CTL = NC; PRE_SEL = NC; 1.48 Gbps, 2.97 Gbps, 6 Gbps data lines, 148 MHz, 297 MHz clock; See Figure 8			0.15	Tbit
$t_{JITC1(1.4b)}$	Total output clock jitter	CLK = 25 MHz, 74.25 MHz, 75 MHz, 150 MHz, 297 MHz			0.25	Tbit

(1) The typical rating is simulated at 3.3 V V_{CC} and 1.2 V V_{DD} and at 27°C unless otherwise noted
(2) The maximum rating is simulated at 3.465 V V_{CC} and 1.27 V V_{DD} and at 85°C unless otherwise noted

TMDS Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$t_{JITC1(2.0)}$		DR = 6 Gbps: CLK = 150 MHz			0.3	Tbit
t_{JITD2}	Total output data jitter See Figure 14	3.4 Gbps < R_{bit} ≤ 3.712 Gps TX_TERM_CTL = NC; PRE_SEL = NC; OE = H			0.4	Tbit
		3.712 Gbps < R_{bit} < 5.94 Gbps TX_TERM_CTL = NC; PRE_SEL = NC; OE = H			$-0.0332R_{bit}^2 + 0.2312R_{bit} + 0.1998$	
		5.94 Gbps ≤ R_{bit} ≤ 6.0 Gbps TX_TERM_CTL = NC; PRE_SEL = NC; OE = H			0.6	

6.11 HPD Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$t_{PD(HPD)}$	Propagation delay from HPD_SNK to HPD_SRC; rising edge and falling edge(2)	See Figure 16; not valid during switching time		40	120	ns
$t_{T(HPD)}$	HPD logical disconnected timeout	See Figure 17		2		ms

(1) The typical rating is simulated at 3.3 V V_{CC} and 1.2 V V_{DD} and at 27°C unless otherwise noted
(2) The maximum rating is simulated at 3.465 V V_{CC} and 1.27 V V_{DD} and at 85°C unless otherwise noted

6.12 DDC and I²C Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of both SDA and SCL signals	V_{CC} = 3.3 V			300	ns
t_f	Fall time of both SDA and SCL signals				300	ns
t_{HIGH}	Pulse duration, SCL high		0.6			µs
t_{LOW}	Pulse duration, SCL low		1.3			µs
t_{SU1}	Setup time, SDA to SCL		100			ns
$t_{ST,\ STA}$	Setup time, SCL to start condition		0.6			µs
$t_{HD,STA}$	Hold time, start condition to SCL		0.6			µs
$t_{ST,STO}$	Setup time, SCL to stop condition		0.6			µs
$t_{(BUF)}$	Bus free time between stop and start condition		1.3			µs
t_{PLH1}	Propagation delay time, low-to-high-level output	Source to sink: 100kbps pattern; Cb(Sink) = 400 pF(1); see Figure 20		360		ns
t_{PHL1}	Propagation delay time, high-to-low-level output			230		ns
t_{PLH2}	Propagation delay time, low-to-high-level output	Sink to source: 100kbps pattern; Cb(Source) = 100 pF(1); see Figure 21		250		ns
t_{PHL2}	Propagation delay time, high-to-low-level output			200		ns

(1) Cb = total capacitance of one bus line in pF.

6.13 Typical Characteristics

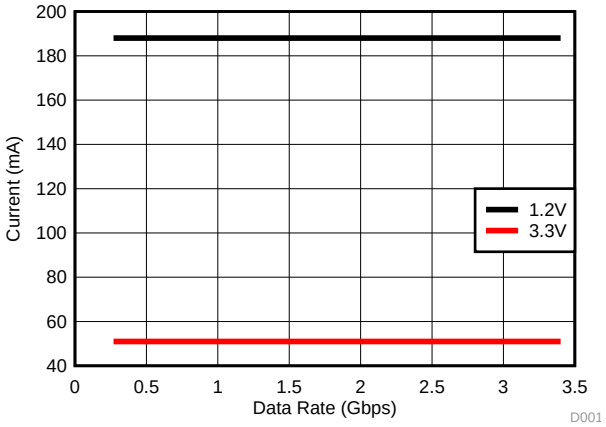


Figure 3. Current vs Data Rate Redriver Mode

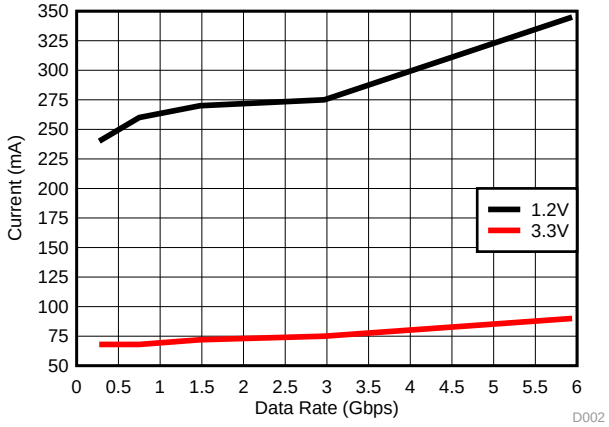


Figure 4. Current vs Data Rate Retimer Mode

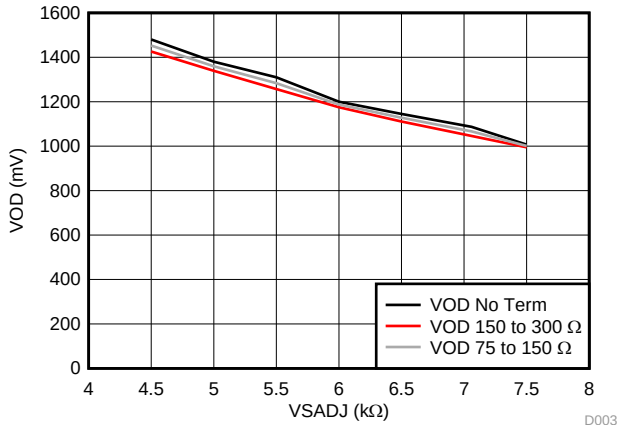


Figure 5. VSADJ vs VOD

7 Parameter Measurement Information

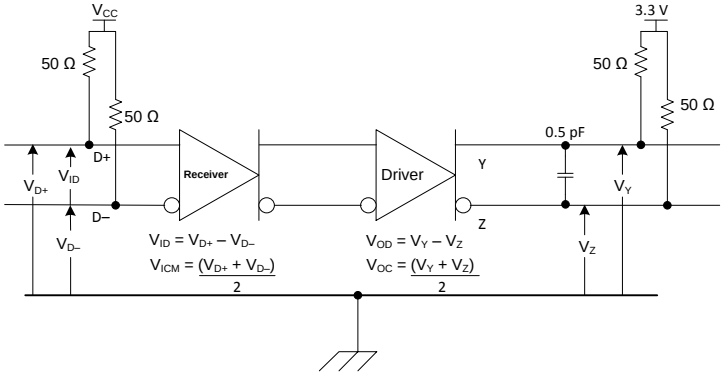


Figure 6. TMDS Main Link Test Circuit

Parameter Measurement Information (continued)

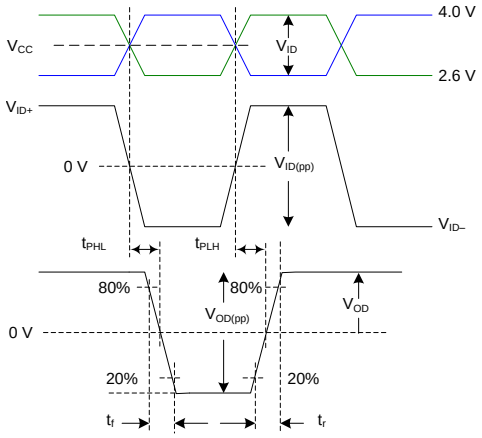


Figure 7. Input/Output Timing Measurements

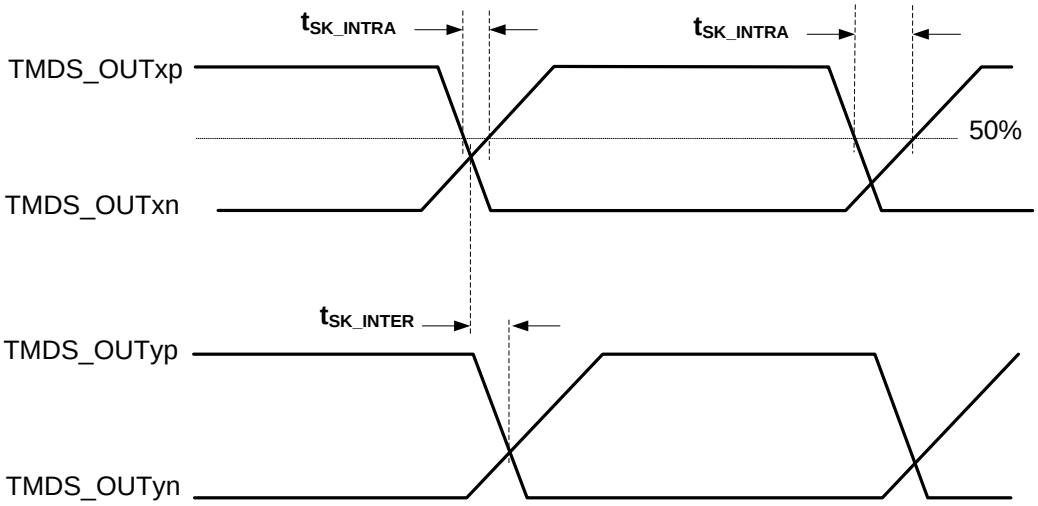


Figure 8. TMDS Output Skew Measurements

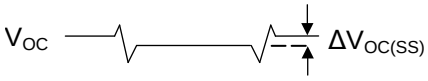
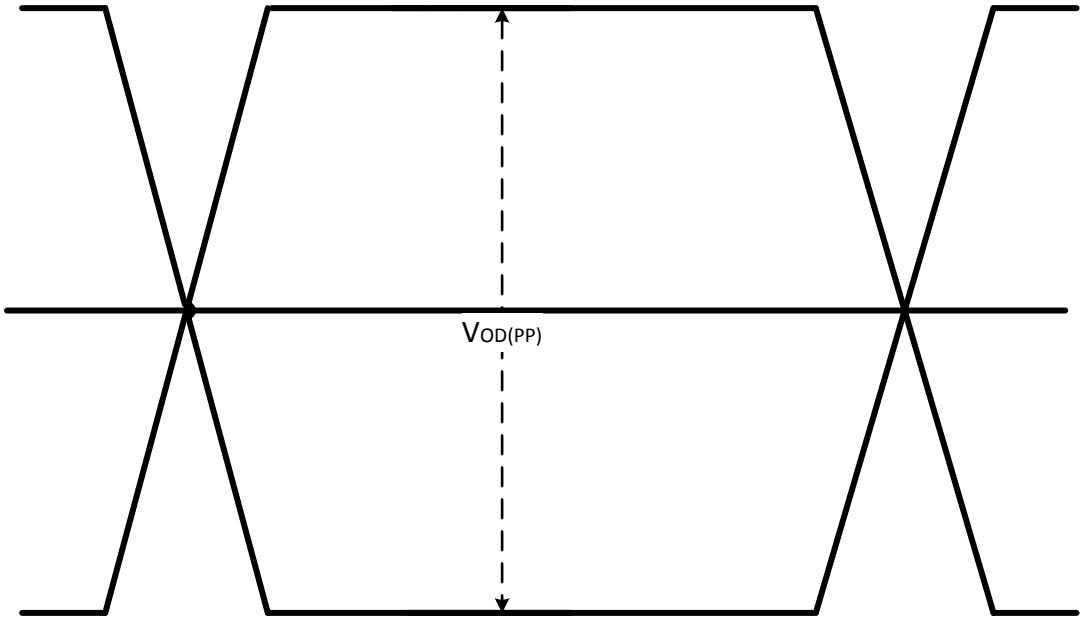


Figure 9. HDMI/DVI TMDS Output Common Mode Measurement

Parameter Measurement Information (continued)



PRE_SEL=Z
Vsadj = 7.06KΩ

Figure 10. Output Differential Waveform

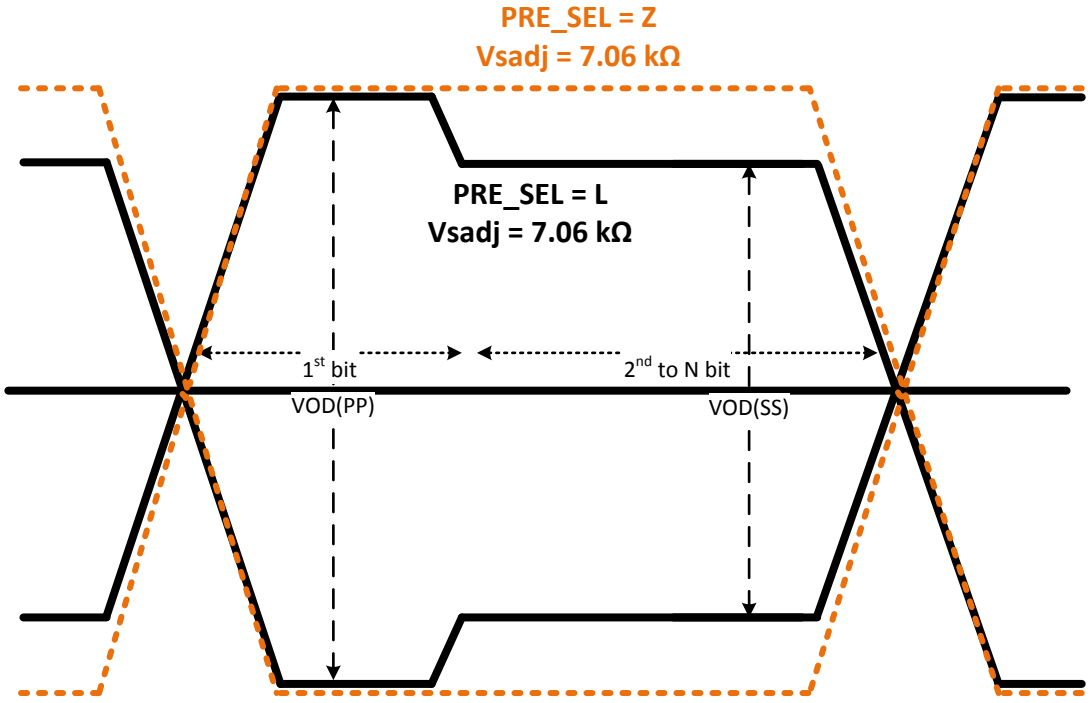
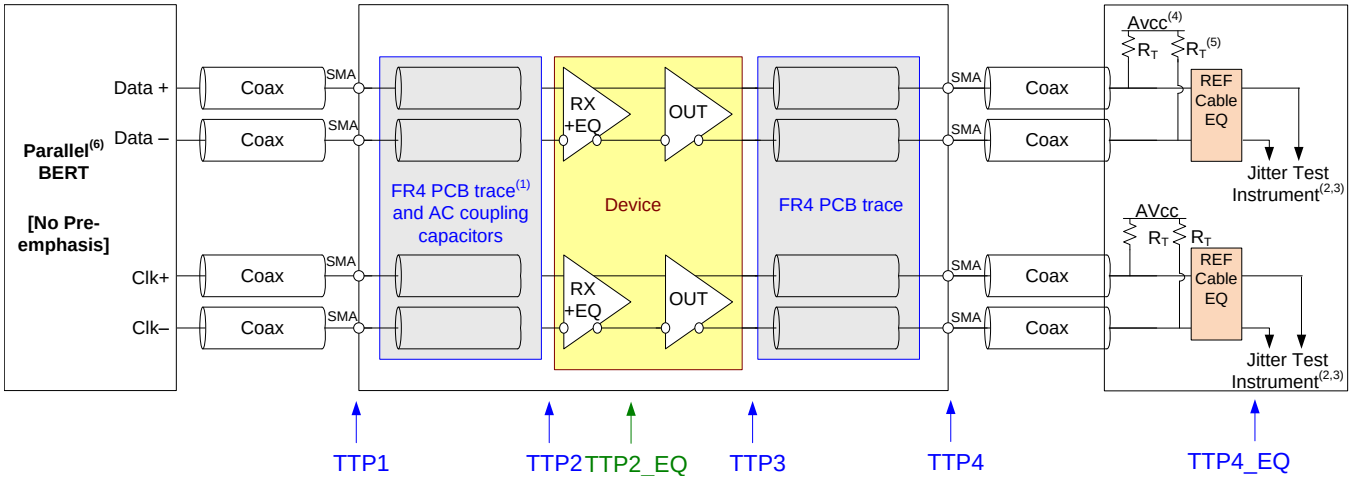


Figure 11. Output De-Emphasis Waveform

Parameter Measurement Information (continued)



A. The FR4 trace between TTP1 and TTP2 is designed to emulate 1 to 8 inches of FR4, AC coupling capacitor, connector, and another 1 to 8 inches of FR4. Trace width = 4 mils. 100-Ω differential impedance.

B. All jitter is measured at a BER of 10-9

C. Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1

D. AVCC = 3.3 V

E. R_T = 50 Ω,

F. The input signal from parallel Bert does not have any pre-emphasis. Refer to *Recommended Operating Conditions*.

Figure 12. HDMI Output Jitter Measurement

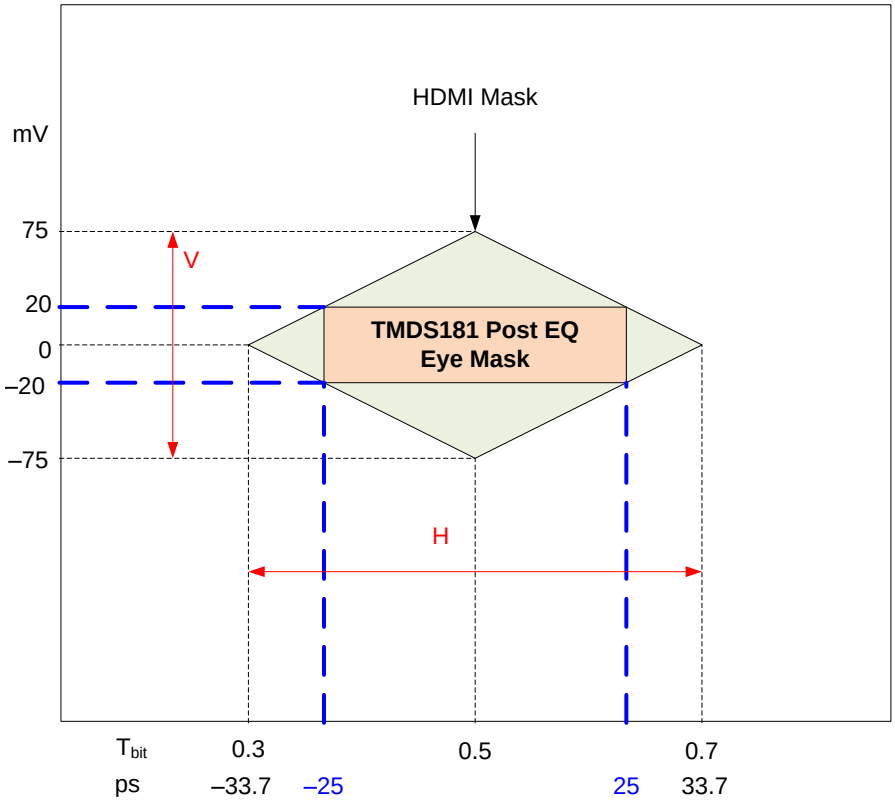
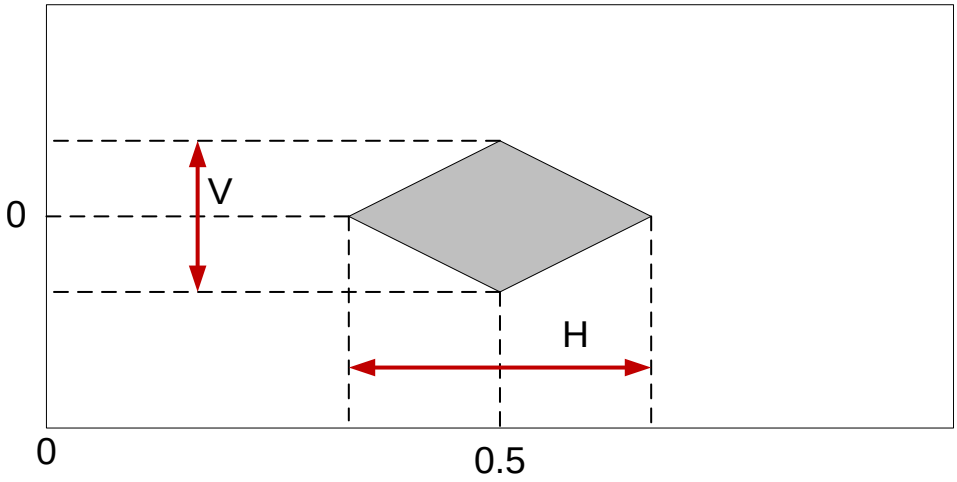


Figure 13. Input Eye Mask Post EQ – TTP2_EQ

Parameter Measurement Information (continued)



A. See Table 1.

Figure 14. Output Eye Mask at TTP4_EQ

Table 1. Output Eye Mask V and H Values

TMDS Data Rate (Gbps)	H (T_{bit})	V (mV)
3.4 < DR < 3.712	0.6	335
3.712 < DR < 5.94	$-0.0332R_{bit}^2 + 0.2312\ R_{bit} + 0.1998$	$-19.66R_{bit}^2 + 106.74R_{bit} + 209.58$
5.94 ≤ DR ≤ 6.0	0.4	150

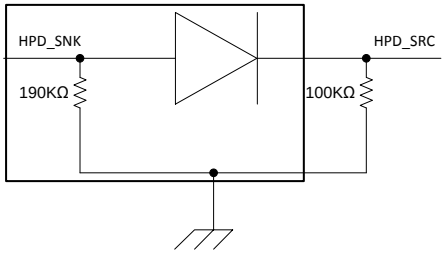


Figure 15. HPD Test Circuit

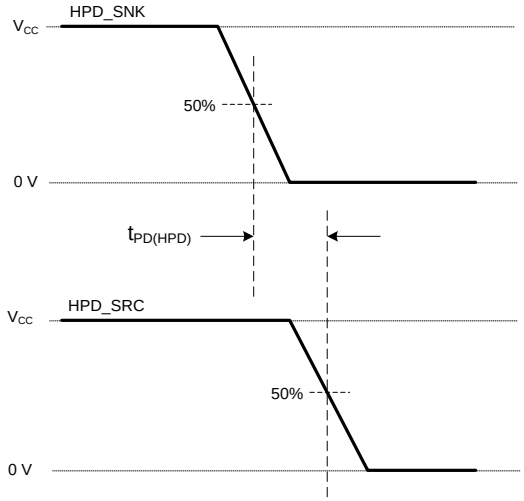


Figure 16. HPD Timing Diagram 1

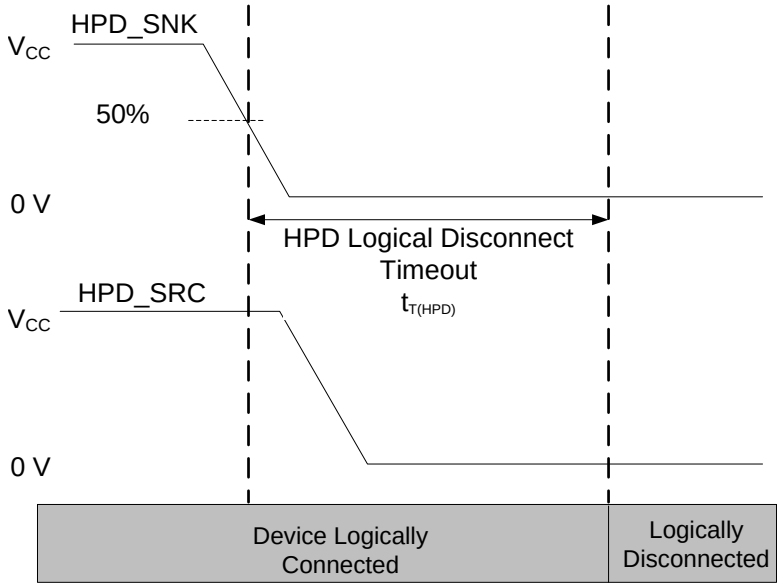


Figure 17. HPD Logic Disconnect Timeout

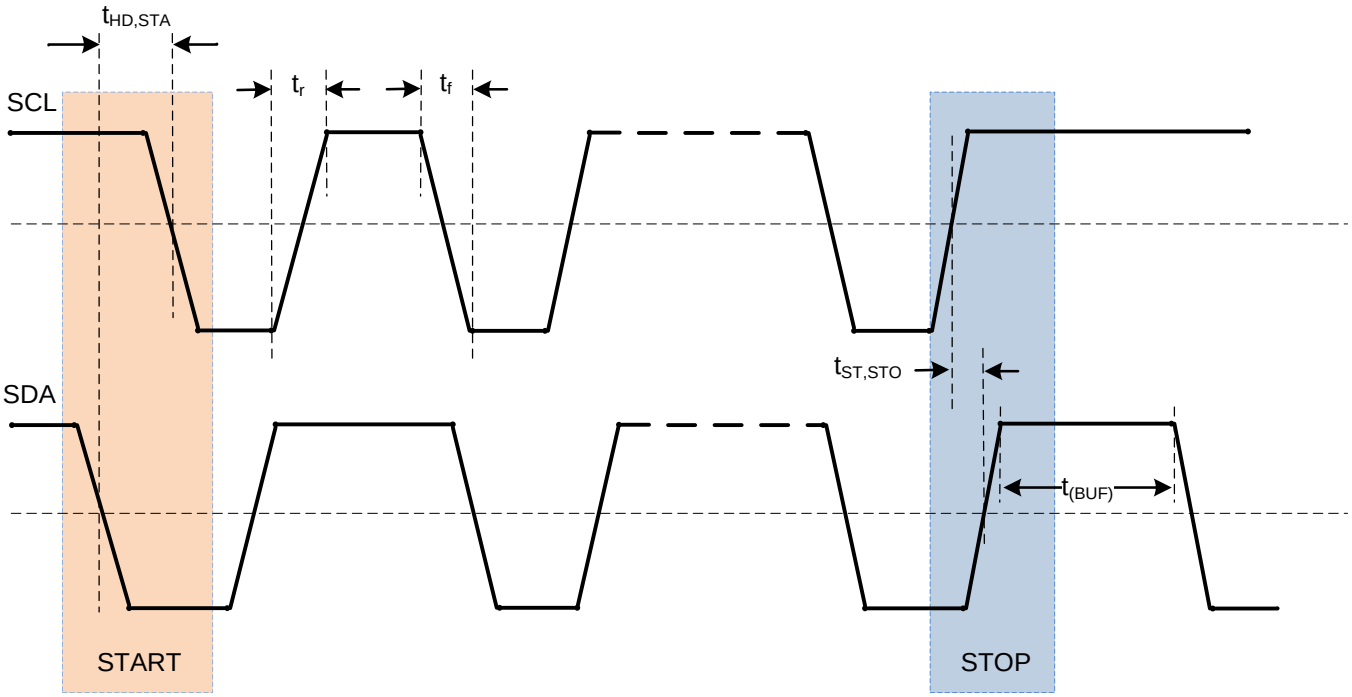


Figure 18. START and STOP Condition Timing

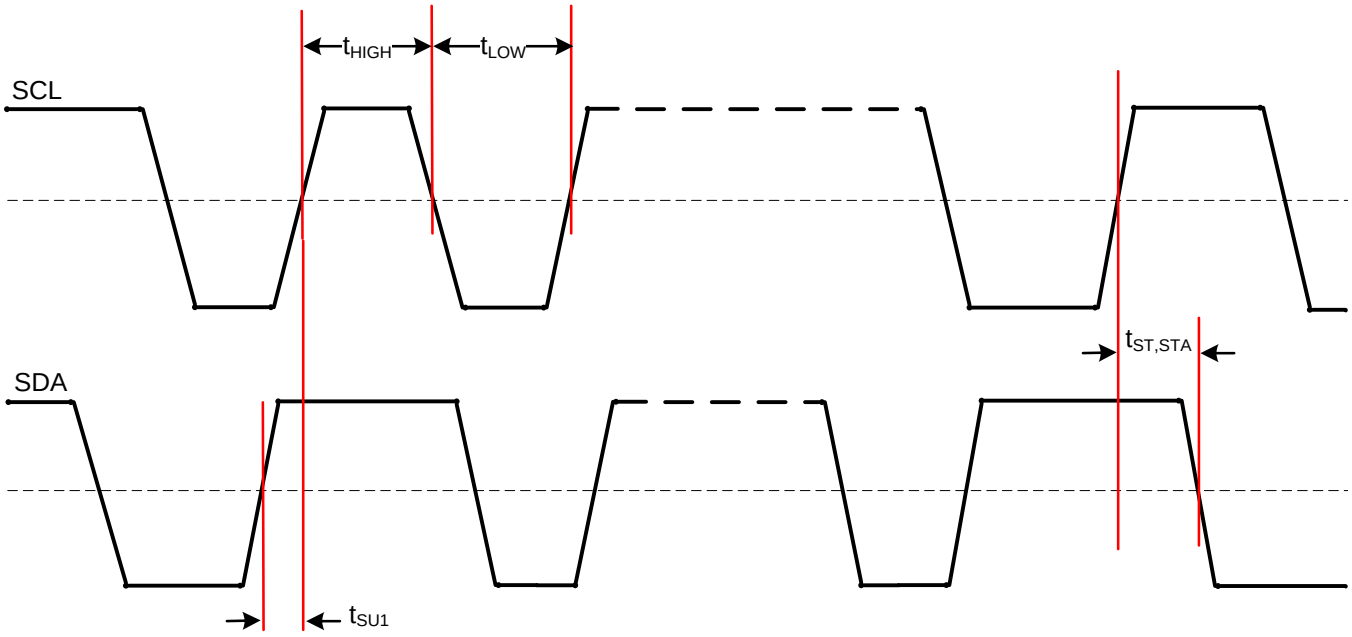


Figure 19. SCL and SDA Timing

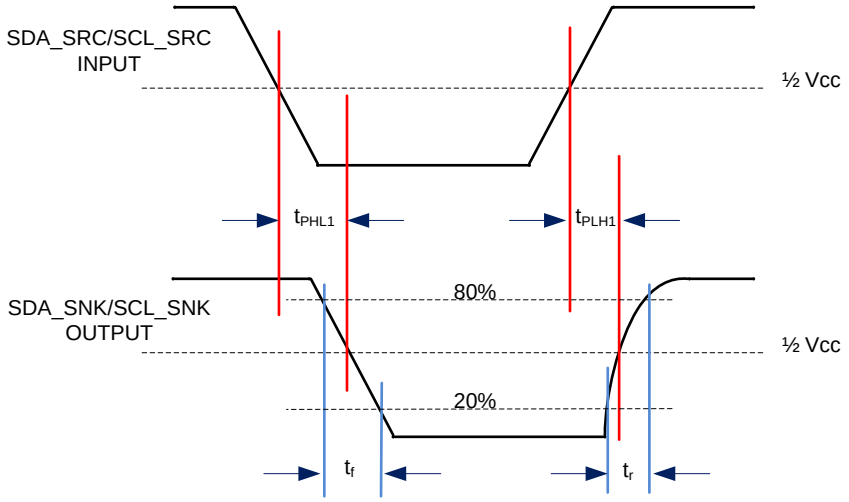


Figure 20. DDC Propagation Delay – Source to Sink

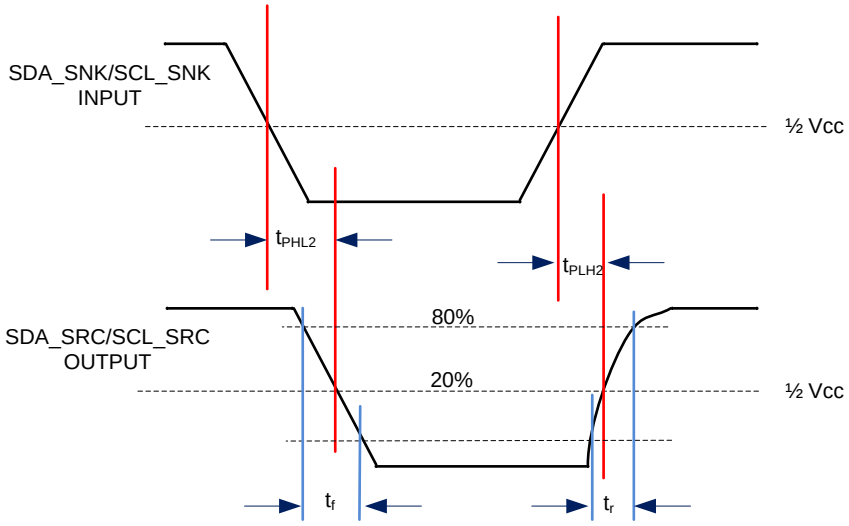


Figure 21. DDC Propagation Delay – Sink to Source

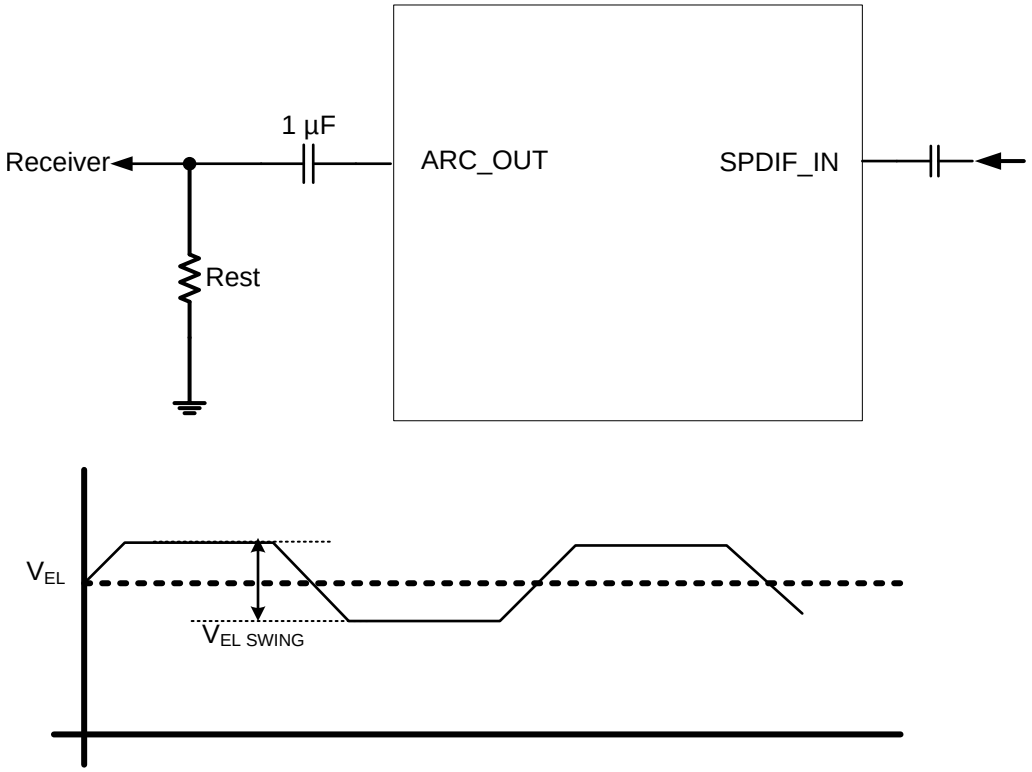


Figure 22. ARC Output

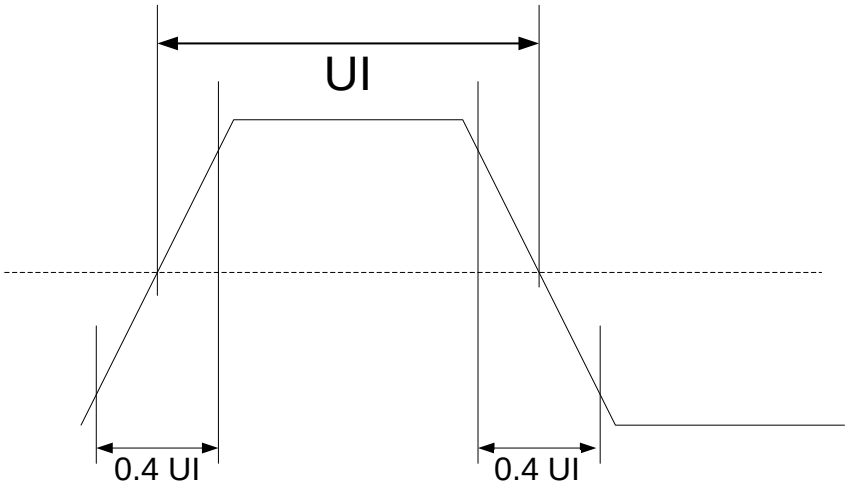


Figure 23. Rise and Fall Time of ARC

8 Detailed Description

8.1 Overview

The TMDS181 is a DVI or HDMI™ retimer. The TMDS181 supports four TMDS channels, audio return channel (SPDIF_IN/ARC_OUT), hot plug detect, and DDC interfaces. The TMDS181 supports signaling rates up to 6 Gbps in retimer mode to allow for the highest resolutions of 4k2k60p 24 bits per pixel and up to WUXGA 16-bit color depth or 1080p with higher refresh rates. In redriver mode it supports HDMI1.4b with data rates up to 3.4 Gbps. The TMDS181 can be configured to support the HDMI2.0a standard which includes higher data rate, lower clock swing, and clock frequency. The TMDS181 can automatically configure itself as a redriver at low data rate (<1.0 Gbps) or as a retimer above this data rate. For passing compliance and reducing system-level design issues, several features are included such as TMDS output amplitude adjust using an external resistor on the VSADJ pin and source termination selection control. Device operation and configuration can be programmed by pin strapping or I^2C. Four TMDS181s can be used on one I^2C bus when I2C_EN enable and device address set by A0/A1.

To reduce active power, the TMDS181 supports dual power supply rails of 1.2 V on VDD and 3.3 V on VCC. There are several methods of power management, such as going into power-down mode using three methods:

- HPD is low
- Writing a 1 to register 09h[3]
- De-asserting OE

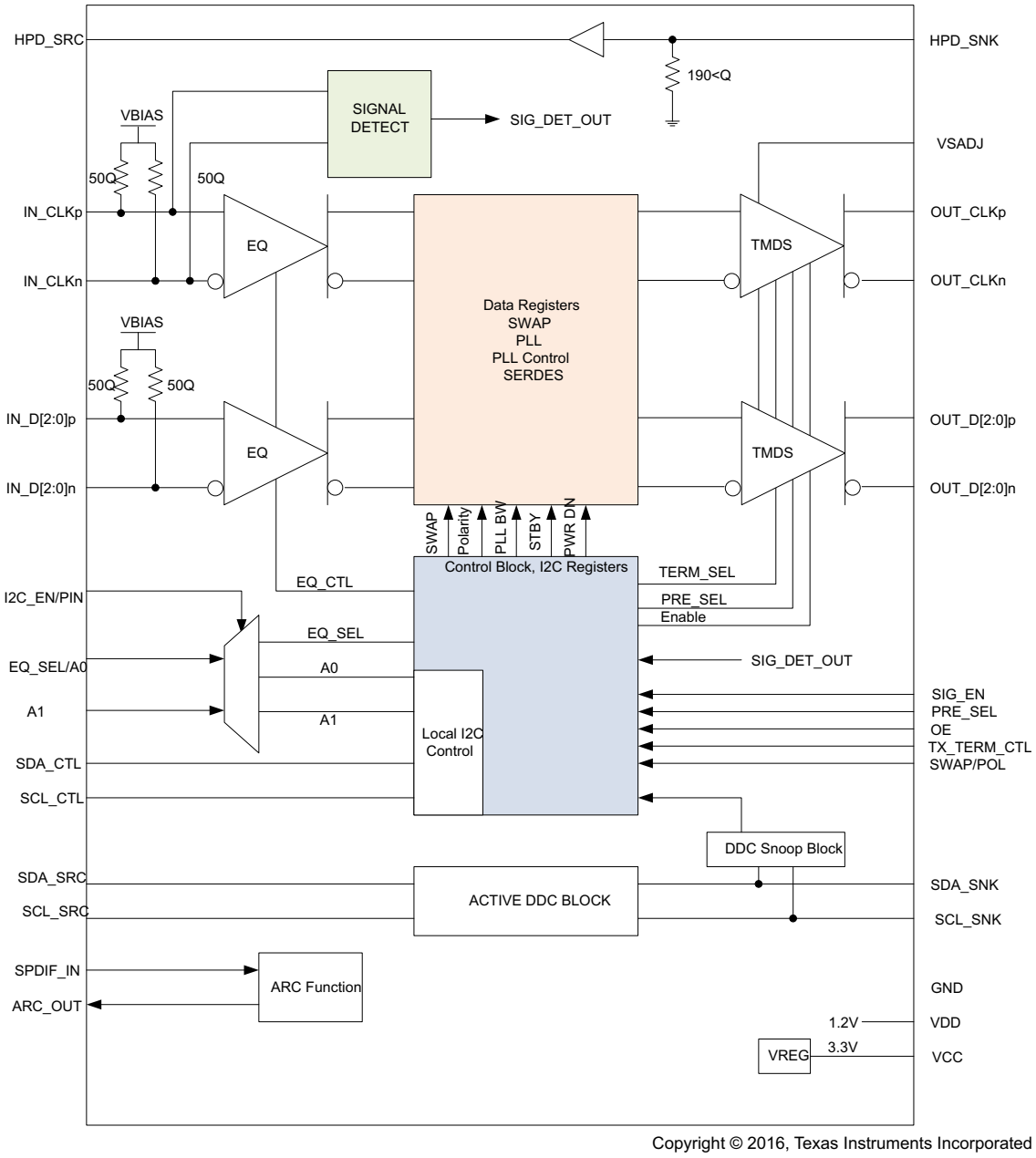
De-asserting OE clears the I^2C registers, thus once reasserted the device must be reprogrammed if I^2C was used for device setup. Upon return to normal active operation from reasserted OE or reasserted HPD, the TMDS181 requires the source to write a 1 to the TMDS_CLOCK_RATIO_STATUS bit for the TMDS181 to resume $1/40^{th}$ clock mode. The TMDS181 does not reset this bit based upon a DDC read transaction. The SIG_EN pin enables the signal detect circuit that provides an automatic power-management feature during normal operation. When no valid signal is present on the inputs, the device will enter standby mode. By disabling the detect circuit, the receiver block is always on. DDC bridge supports the HDMI2.0 SCDC communication, 100 Kbps data rate default and 400 kbps adjustable by software.

TMDS181 supports both fixed EQ gain control or adaptive equalization to compensate for different lengths of input cables or board traces. The EQ gain can be software adjusted by I^2C control or selection between two fixed values or adaptive (Retimer Mode Only) equalization by pin strapping EQ_SEL pin. The customer can pull up or down TX_TERM_CTL through a 65 kΩ resistor to change the termination impedance for improved output performance when working in HDMI1.4b or leave it not connected. When not connected, the TMDS181 in conjunction with the rate detect automatically changes its output termination to meet HDMI1.4b or HDMI2.0a needs. For HDMI1.4b a transmitter termination of 150 Ω to 300 Ω is allowed for data rates above 2 Gbps to compensate for reflections. The automatic termination selection will configure the TMDS181 for this. It is important to note that there are times that this is not the best solution and no termination may be needed to pass compliance. For HDMI2.0a the 75 Ω to 150 Ω transmitter termination is required and the link will not work if this is not set.

The TMDS181 supports the audio return channel to support HDMI1.4b. To make implementation easier, the TMDS181 supports input pin swapping and input polarity swap. When swapping the input pins, IN_CLK and IN_D2 swap and IN_D1 and IN_D0 swap with each other. Swap works in both retimer and redriver mode. Polarity swap exchanges the N and P channel polarity in each input lane and is only available during retimer mode. Lane swap and polarity swap can be implemented at the same time in retimer mode.

Two temperature gradient versions of the device are available: extended commercial temperature range 0ºC to 85ºC (TMDS181) and industrial temperature range from –40ºC to 85ºC (TMDS181I).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reset Implementation

When OE is de-asserted, control signal inputs are ignored; the HDMI inputs and outputs are high impedance. It is critical to transition the OE from a low level to a high level after the V_{CC} supply has reached the minimum recommended operating voltage. Achieve this transition by a control signal to the OE input, or by an external capacitor connected between OE and GND. To ensure the TMDS181 is properly reset, the OE pin must be de-asserted for at least 100 μs before being asserted. When OE is reasserted, the TMDS181 must be

Feature Description (continued)

reprogrammed if it was programmed by I^2C and not pin strapping. When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger-value external capacitor. Refer to the latest reference schematic for TMDS181; consider approximately 200 nF capacitor as a reasonable first estimate for the size of the external capacitor. Figure 24 and Figure 25 show both OE implementations.

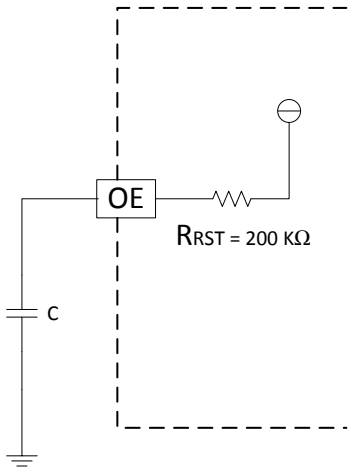


Figure 24. External Capacitor Controlled OE

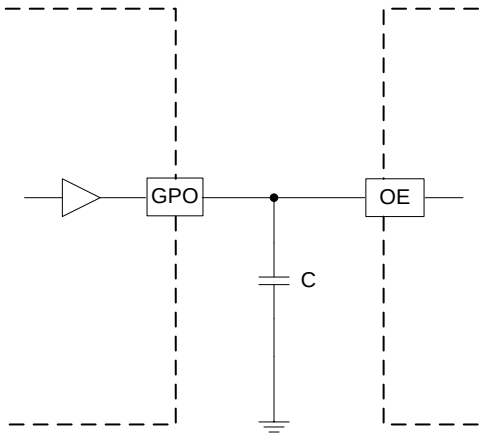


Figure 25. OE Input from Active Controller

8.3.2 Operation Timing

TMDS181 starts to operate after the OE signal is properly set after power-up timing completes. See Figure 1, Figure 2, and *Power-Up and Operation Timing Requirements*. If OE is held low until V_{DD} and V_{CC} become stable, there is no rail sequence requirement.

8.3.3 Swap and Polarity Working

TMDS181 incorporates swap function, which can set the input lanes in swap mode. The IN_D2 routes to the OUT_CLK position. The IN_D1 swaps with IN_D0. The swap function only changes the input pins. The EQ setup follows the new mapping (see Figure 26). This function can be used with the SWAP/POL pin 1 and control the register 0x09h bit 7 for SWAP enable. Lane swap function works in both redriver and retimer mode.

The TMDS181 can also swap the input polarity signals. When SWAP/POL is high the n and p pins on each lane will swap. Polarity swap only works when in retimer mode. Take care when this function is enabled and the device is in automatic crossover mode between redriver and retimer modes. When the data rate drops to the redriver level, the polarity swap is lost.

Table 2. SWAP Function(1)

Normal Operation	SWAP = L or CSR 0x09h bit 7 is 1'b1
IN_D2 → OUT_D2	IN_D2 → OUT_CLK
IN_D1 → OUT_D1	IN_D1 → OUT_D0
IN_D0 → OUT_D0	IN_D0 → OUT_D1
IN_CLK → OUT_CLK	IN_CLK → OUT_D2

(1) The output lanes never change, only the input lanes change. See Figure 26.

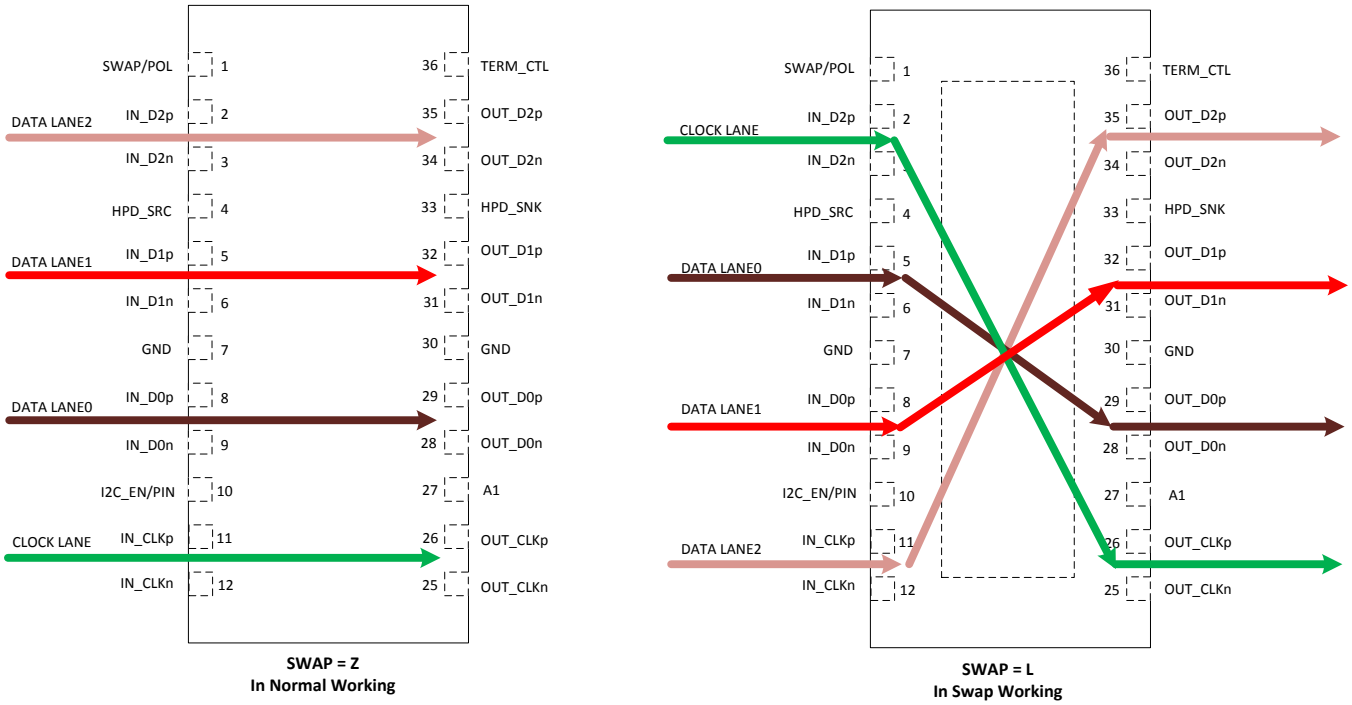


Figure 26. TMDS181 Swap Function

8.3.4 TMDS Inputs

Standard TMDS terminations are integrated on all TMDS inputs. External terminations are not required. Each input data channel contains an adaptive or fixed equalizer to compensate for cable or board losses. The voltage at the TMDS input pins must be limited below the absolute maximum ratings. An unused input should not be connected to ground because this would result in excessive current flow damaging the device. An unused input channel can be externally biased to prevent output oscillation. The complementary input pin is recommended to be grounded through a 1 kΩ resistor and the other pin left open. The input pins can be polarity changed through the local I^2C register when in retimer mode.

8.3.5 TMDS Inputs Debug Tools

There are two methods for debugging a system to make sure the inputs to the TMDS181 are valid. A TMDS error checker is implemented to provide a rough bit error rate per data lane. This allows the system implementer to determine how the link between the source and TMDS181 is performing on all three data lanes. See *RX PATTERN VERIFIER CONTROL/STATUS Register*.

If a high error count is evident, the TMDS181 has a way to view the general eye quality. A tool is available that uses the I^2C link to download the data that can be plotted for an eye diagram. This is available per data lane. This tool also provides a method to turn on an internal PRBS generator that will transmit a data signal on the data pins. A clock at the proper frequency is required on the IN_CLK pins to generate the expected output data rate.

8.3.6 Receiver Equalizer

Equalizers are used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces and cables. TMDS181 supports fixed receiver equalizer (Retimer and Redriver Mode) and adaptive receiver equalizer (Retimer Mode) by setting the EQ_SEL/A0 pin or through I^2C reg0Ah[5]. When EQ_SEL/A0 is high, the EQ gain is fixed to 14 dB and when set low ,the EQ gain is set to 7.5 dB. TMDS181 operates in adaptive equalizer mode when the EQ_SEL/A0 pin is left floating. The EQ gain is automatically adjusted based on the data rate to compensate for trace or cable loss. Various fixed EQ values can be set through local I^2C control, reg0Dh[5:1]. The fixed EQ value can be programmed for both the data and clock. Adaptive equalization is the default setting.

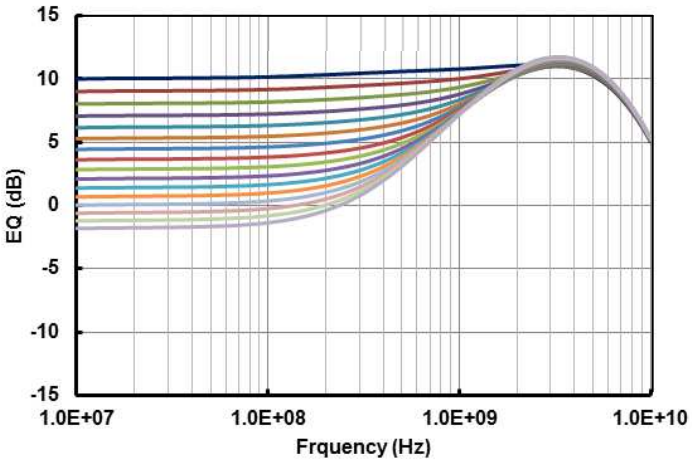


Figure 27. Adaptive EQ Gain Curve for >3.4 Gbps

8.3.7 Input Signal Detect Block

When SIG_EN is enabled, the TMDS looks for a valid TMDS clock signal input. The device is fully functional when a valid signal is detected. If no valid TMDS clock signal is detected, the device enters standby mode waiting for a valid signal at the clock input. The internal CDR is shut down and all of the TMDS outputs are in high-Z status. TMDS signal detect circuit can be set as enable by SIG_EN pin or through local I^2C control but is default disabled. Implementer should activate this function in normal operation for power saving.

8.3.8 Audio Return Channel

The audio return channel in TMDS181 enables a TV, through a single HDMI cable, to send audio data upstream to an A/V receiver or surround audio controller, increasing user flexibility and eliminating the need for any separate S/PDIF audio connection. The TMDS181 supports single mode audio return channel. Customer can import the S/PDIF signal to SPDIF_IN and send out the signal from ARC_OUT and pass through the general HDMI cable to audio receiver. By I^2C control, customer can disable ARC_OUT by register. Default enable after initialize.

8.3.9 Transmitter Impedance Control

HDMI2.0a standard requires a termination impedance in the 75 Ω to 150 Ω range for data rates >3.4 Gbps. Source termination is disabled at data rates <2 Gbps. When the data rate is between 2 Gbps and 3.4 Gbps, the output signal may be better if the termination value is between 150 Ω to 300 Ω, depending upon system implementation. It is important to note that there are times that this is not the best solution and no termination may be needed to pass compliance. TMDS181 supports three different source termination impedances for HDMI1.4b and HDMI2.0a. Pin 36, TX_TERM_CTL, offers a selection option to choose the output termination impedance value. This function can be programmed using I^2C, reg0Bh[4:3] TX_TERM_CTL. For HDMI2.0a the 75 Ω to 150 Ω transmitter termination is required and the link will not work if this is not set.

Table 3. TX Termination Control

PIN 36 CONFIGURATION	DESCRIPTION
TX_TERM_CTL = H	The transmitter has no termination
TX_TERM_CTL = L	The transmit termination impedance is approximately 75 Ω to 150 Ω to support HDMI2.0a
TX_TERM_CTL = NC	Automatically selects the impedance • DR > 3.4 Gbps – 75 Ω to 150 Ω differential near end termination • 2 Gbps > DR < 3.4 Gbps – 150 Ω to 300 Ω differential near-end termination • DR < 2 Gbps – No termination

8.3.10 TMDS Outputs

A 1% precision resistor, 7.06 kΩ, is recommended to be connected from VSADJ pin to ground to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10 mA current sink capability, which provides a typical 500 mV voltage drop across a 50 Ω termination resistor.

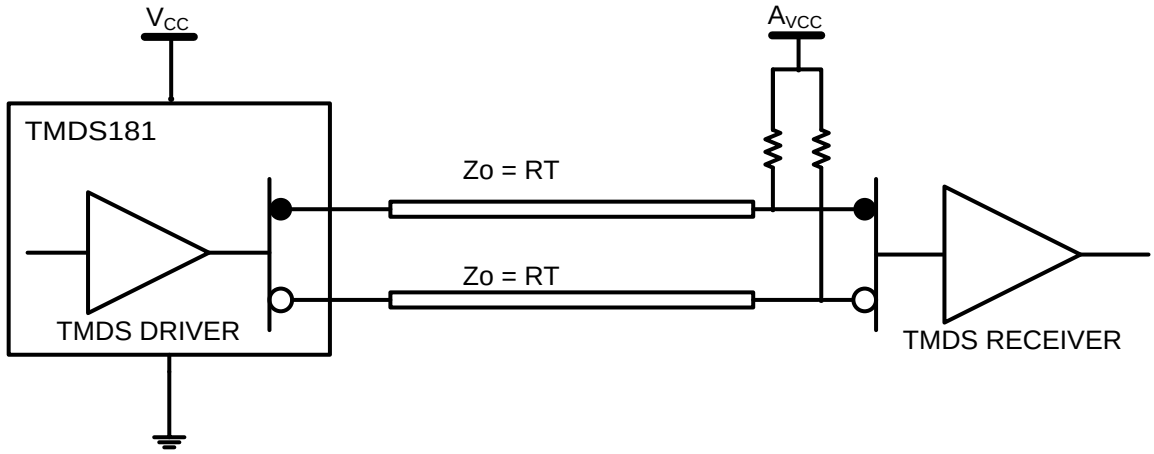


Figure 28. TMDS Driver and Termination Circuit

Referring to Figure 28, if V_{CC} (TMDS181 supply) and AVCC (sink termination supply) are both powered, the TMDS output signals are high impedance when OE = high. The normal operating condition is that both supplies are active. Refer to Figure 28, if V_{CC} is on and AVCC is off, the TMDS outputs source a typical 5-mA current through each termination resistor to ground. A total of 33 mW of power is consumed by the terminations independent of the OEB logical selection. When AVCC is powered on, normal operation (OE controls output impedance) is resumed. When the power source of the device is off and the power source to termination is on, the $I_{O(off)}$ output leakage current specification ensures the leakage current is limited to 45 μA or less. The V_{OD} of the clock and data lanes can be reduced through I^2C. See Table 12 for details. Figure 3 shows the different output voltages based on the different VSADJ settings.

8.3.11 Pre-Emphasis/De-Emphasis

The TMDS181 provides de-emphasis as a way to compensate for ISI loss between the TMDS181 outputs to a TMDS receiver. There are two methods to implement this function. When in pin strapping mode the PRE_SEL pin controls this function. The PRE_SEL pin provides - 2 dB or 0 dB de-emphasis, which allows the output signal pre-conditioning to offset interconnect losses from the TMDS181 device to the TMDS receiver. De-emphasis is recommended to be set at 0 dB while connecting to a receiver through short PCB route. When pulled to ground though a 65 kΩ resistor - 2 dB can be realized, see Figure 11. When using I^2C, reg0Ch[1:0] is used to make these adjustments.

As there are times that true pre-emphasis may be the best solution there are two ways to accomplish this. If pin strapping is being used the best method is to reduce the VSADJ resistor value thus increasing the VOD swing and then pulling the PRE_SEL pin to ground using the 65 kΩ resistor, see Figure 29. If using I^2C there are two methods to accomplish this. The first is similar to pin strapping by reducing the VSADJ resistor value and then implementing - 2 dB de-emphasis. The second method is to set reg0Ch[7:5] = 011 and set reg0Ch[1:0] = 01 which will accomplish the same pre-emphasis setting, see Figure 30.

NOTE

De-emphasis is only implement able during retimer mode. In redriver mode this function is not available.

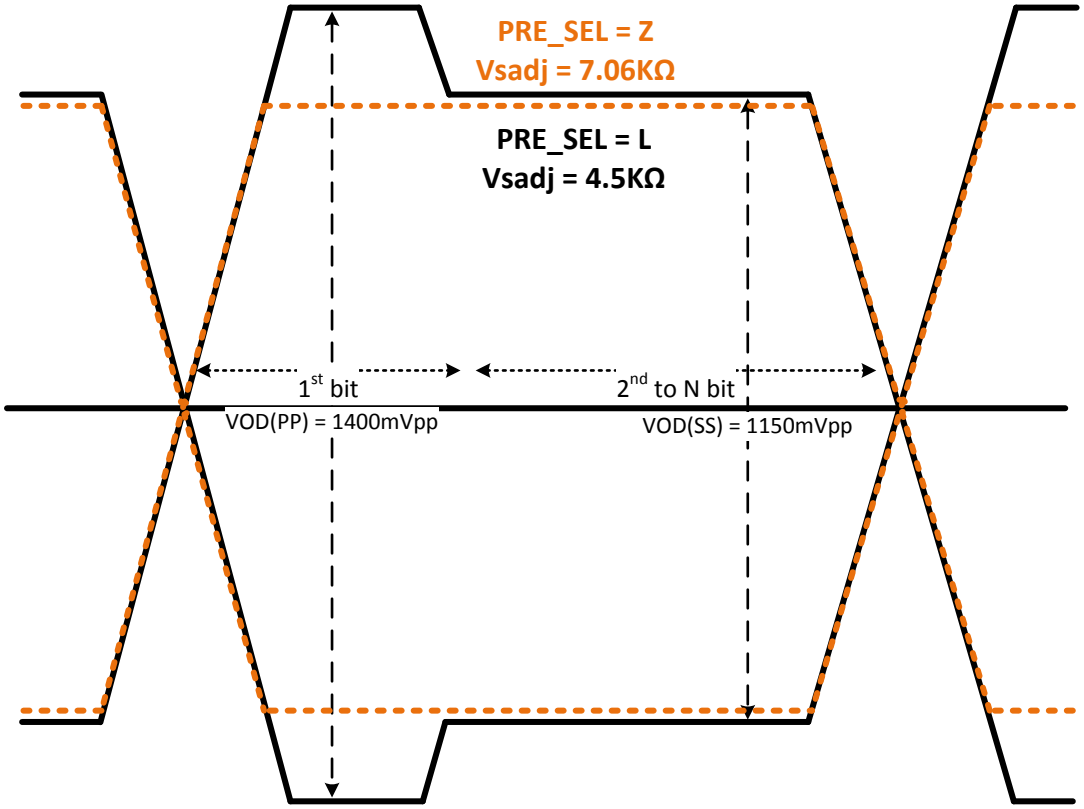


Figure 29. Output Pre-Emphasis Using Pin Strapping

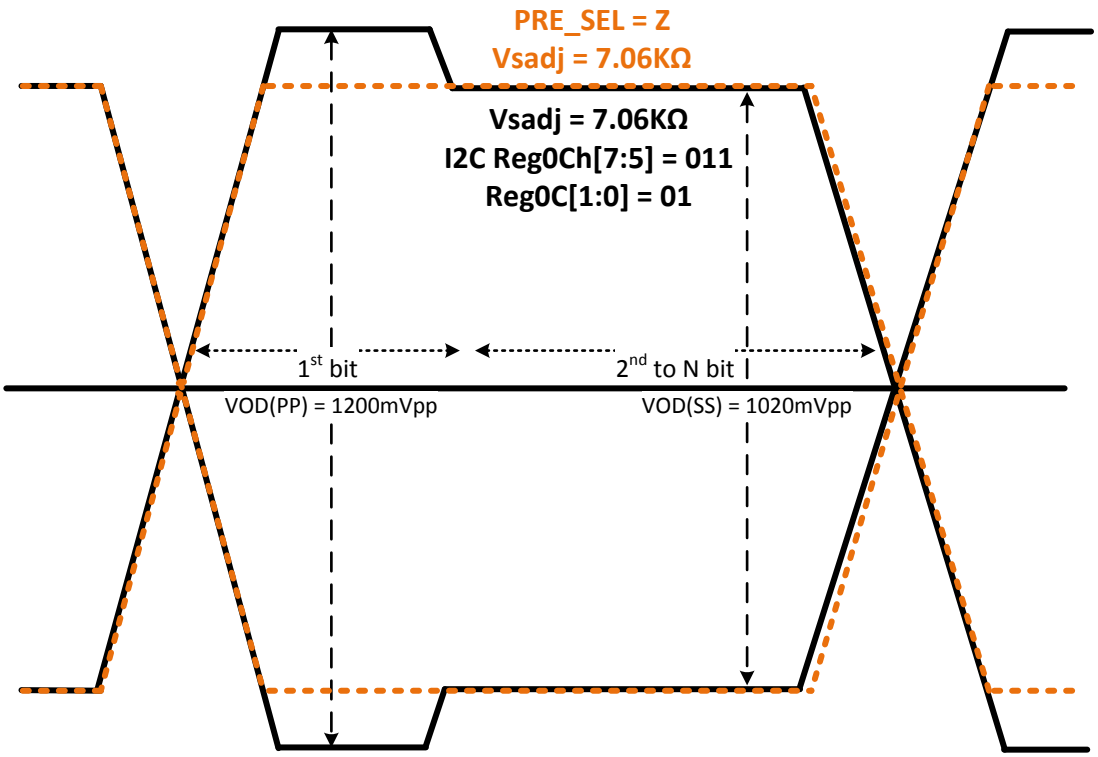


Figure 30. Output Pre-Emphasis Using I^2C

8.4 Device Functional Modes

8.4.1 Retimer Mode

Clock and data recovery circuits (CDR) are used to track, sample, and retime the equalized data bit streams. The CDRs are designed with a loop bandwidth to minimize the amount of jitter transfer from the video source to the TMDS outputs. Input jitter within the CDR's PLL bandwidth, < 1 MHz will be transferred to the TMDS outputs. Higher frequency jitter above the CDR loop bandwidth is attenuated, providing a jitter cleaning function to reduce the amount of high frequency jitter from the video source. The retimer is automatically activated at pixel clock approximately above 100 MHz when jitter cleaning is needed for robust operation when this option is enabled (default). The retimer operates at about 1 Gbps to 6 Gbps DR.

When systems switch to higher data rates above 3.4 Gbps, the CDR operates at between 85 MHz to 150 MHz pixel clock (3.4+ to 6.0 Gbps), supporting up to 4K2K high resolution with a 60 Hz refresh rate, or 3D 1080p HDTV. At pixel clock below 100 MHz, the TMDS181 automatically bypasses the internal retimer and operates as a redriver. When the video source changes resolution, the internal retimer starts the acquisition process to determine the input clock frequency and acquire lock to new data bit streams. During the clock frequency detection period and the retimer acquisition period that last approximately 7 ms, the TMDS drivers can be kept active (default) or programmed to be disabled to avoid sending invalid clock or data to the downstream receiver. The TMDS181 can be configured to work as a redriver (full range), crossover (redriver-retimer), and retimer (full range).

Device Functional Modes (continued)

8.4.2 Redriver Mode

The TMDS181 also has a redriver mode that can be enabled through I^2C, at reg0Ah[1:0] DEV_FUNC_MODE, which compensates for ISI channel loss. In this mode, power is reduced as the CDR and PLL are turned off. When in automatic mode, the TMDS181 is in redriver mode for data rates <1.0 Gbps. By using I^2C, the device can be put in redriver mode for the complete data range of 250 Mbps to 3.4 Gbps. This is done by writing a 00 to register 0Ah[1:0]. If the link has excessive random jitter, then retimer mode is the best operating mode. When in redriver mode, the device only compensates for ISI loss. When in redriver mode compliance is not guaranteed as skew compensation and retiming functions are disabled. If a significant amount of random jitter is present, the system may not pass compliance at the connector.

8.4.3 DDC Training for HDMI2.0a Data Rate Monitor

As part of discovery, the source reads the sink's E-EDID information to understand the capabilities of the sink. Part of this read is HDMI Forum Vendor Specific Data Block (HF-VSDB) MAX_TMDS_Character_Rate byte to determine the data rate supported. Depending upon the value, the source writes to slave address 0xA8 offset 0x20 bit1, TMDS_CLOCK_RATIO_STATUS. The TMDS181 snoops this write to determine the TMDS clock ratio and thus sets its own TMDS_CLOCK_RATIO_STATUS bit accordingly. If a 1 is written, then the TMDS clock is set to $1/40^{th}$ of TMDS bit period. If a 0 is written, then the TMDS clock is set to $1/10^{th}$ of TMDS bit period. The TMDS181 defaults to $1/10^{th}$ of TMDS bit period unless a 1 is written to address 0xA8 offset 0x20 bit 1. When HPD is deasserted, this bit is reset to default values. If the source does not write this bit, the TMDS181 will not be configured for TMDS clock $1/40^{th}$ mode in support of HDMI2.0a. As the TMDS181 is in the system link, but not recognized as part of the link, it is possible that the source could read the sink EDID where this bit is set and does not rewrite this bit. If the TMDS181 has entered a power-down state, this bit is cleared and does not re-set on a read. To work properly, the bit has to be set again with a write by the source.

8.4.4 DDC Functional Description

The TMDS181 solves sink/source level issues by implementing a master/slave control mode for the DDC bus. When the TMDS181 detects the start condition on the DDC bus from the SDA_SRC/SCL_SRC, it will transfer the data or clock signal to the SDA_SNK/SCL_SNK with little propagation delay. When SDA_SNK detects the feedback from the downstream device, the TMDS181 will pull up or pull down the SDA_SRC bus and deliver the signal to the source.

The DDC link defaults to 100 kbps but can be set to various values including 400 kbps by setting the correct value to address 0Bh through the I^2C interface. The DDC lines are 5 V tolerant when the device is powered off.

NOTE

The TMDS181 utilizes clock stretching for DDC transactions. As there are sources and sinks that do not perform this function correctly a system may not work correctly as DDC transactions are incorrectly transmitted/received. To overcome this a snoop configuration can be implemented where the SDA/SCL from the source is connected directly to the SDA/SCL sink. The TMDS181 will need its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Care must be taken when this configuration is being implemented as the voltage levels for DDC between the source and sink may be different, 3.3 V vs 5 V; See Figure 35 and See Figure 36

8.4.5 Mode Selection Functional Description

Mode selection definition: This bit lets the receiver know where the device is located in a system for the purpose of centering the AEQ point. The TMDS181 is targeting sink applications, so the default value is 1, which will center the EQ at 12 to 13 dB depending upon TMDS_CLOCK_RATIO_STATUS value (see *Equalization Control Register)*. If the TMDS181 is in a source application, the value should be changed to a value of 0, which centers the EQ at 6.5 to 7.5 dB depending upon the TMDS_CLOCK_RATIO_STATUS value.

8.5 Register Maps

8.5.1 Local I²C Overview

The TMDS181 local I²C interface is always enabled, but will only be able to overwrite pin strapped features when I2C_EN/PIN is high. The SCL_CTL and SDA_CTL terminals are used for I²C clock and data respectively. The TMDS181 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports the fast mode transfer up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7-bit device address for TMDS181 decides by the combination of EQ_SEL/A0 and A1. Figure 31 clarifies the TMDS181 target address.

Figure 31. TMDS181 I²C Device Address Description

A1/A0	7 (MSB)	6	5	4	3	2	1	0 (W/R)	HEX
00	1	0	1	1	1	1	0	0/1	BC/BD
01	1	0	1	1	1	0	1	0/1	BA/BB
10	1	0	1	1	1	0	0	0/1	B8/B9
11	1	0	1	1	0	1	1	0/1	B6/B7

The typical source application of the TMDS181 is as a retimer in a TV connecting the HDMI output connector and an internal HDMI transmit through flat cables. The register setup can adjust by source side. When TMDS181 is used in a sink side application, it receives data from input connector and transmits to receiver. Local I²C buses run at 400 kHz supporting fast-mode I²C operation.

The following procedure is used to write to the TMDS181 I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TMDS181 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The TMDS181 acknowledges the address cycle.
3. The master presents the sub-address (I²C register within TMDS181) to be written, consisting of one byte of data, MSB-first.
4. The TMDS181 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The TMDS181 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TMDS181.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is used to read the TMDS181 I²C registers.

1. The master initiates a read operation by generating a start condition (S), followed by the TMDS181 7-bit address and a one-value W/R bit to indicate a read cycle.
2. The TMDS181 acknowledges the address cycle.
3. The TMDS181 transmits the contents of the memory registers MSB-first starting at register 00h.
4. The TMDS181 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TMDS181 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

NOTE

Upon reset, the TMDS181 sub-address is always set to 0x00. When no sub-address is included in a read operation, the TMDS181 sub-address increments from the previous acknowledged read or write data byte. If it is required to read from a sub-address that is different from the TMDS181 internal sub-address, a write operation with only a sub-address specified is needed before performing the read operation.

Refer to *Local I²C Control Bit Access TAG Convention* for TMDS181 local I²C register descriptions. Reads from reserved fields not described return zeros, and writes are ignored.

8.5.2 Local I²C Control Bit Access TAG Convention

Reads from reserved fields return zero, and writes to read-only reserved registers are ignored. All addresses not defined by this specification are considered reserved. Reads from these addresses return zero and writes are ignored.

BIT ACCESS TAG CONVENTIONS

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. Table 4 describes the field access tags.

Table 4. Field Access Tags

ACCESS TAG	NAME	DESCRIPTION
R	Read	The field will be read by software
W	Write	The field will be written by software
S	Set	The field will be set by a write of 1. Writes of 0 to the field have no effect
U	Update	Hardware may autonomously update this field

8.5.3 CSR Bit Field Definitions

8.5.3.1 ID Registers

Table 5. ID Registers Field Descriptions

ADDRESS	BITS	DESCRIPTION	ACCESS
00h~07h	7:0	DEVICE_ID These fields return a string of ASCII characters “TMDS181” followed by one space character. TMDS181: Address 0x00 – 0x07 = {- 0x54”T”, 0x4D”M”, 0x44”D”, 0x53”S”, 0x31”1”, 0x38”8”, 0x31”1”, 0x20},	R
08h	7:0	REV _ID. This field identifies the device revision. 0000001 – TMDS181 revision 1	R

8.5.3.2 MISC CONTROL Register

Table 6. MISC CONTROL Register Field Descriptions

ADDRESS	BITS	DEFAULT	DESCRIPTION	ACCESS
09h	7	1'b0	LANE_SWAP. This field swaps the input lanes as per Figure 26. **0 – Disable (default) no lane swap** 1 – Enable: Swaps input lanes (redriver and retimer mode) Note: Field is loaded from SWAP/POL pin; Writes are ignored when I2C_EN/PIN = 0	RWU
	6	1'b0	LANE_POLARITY swaps the input data and clock lanes polarity. **0 – Disabled (default) no polarity swap** 1 – Swaps the input data and clock lane polarity (retimer mode only) Note: Field is loaded from SWAP/POL pin; Writes are ignored when I2C_EN/PIN = 0	RWU
	5	1'b0	Reserved	R
	4	1'b0	SIG_EN. This field enables the clock lane activity detect circuitry. (Redriver mode only because the retimer requires a clock input to work, so without a clock input, the device enters standby regardless) **0 – Disable (default) Clock detector circuit closed and receiver always works in normal operation.** 1 – Enable, clock detector circuit makes the receiver automatically enter the standby state when no valid data detect. Note: Field is loaded from SIG_EN pin; Writes are ignored when I2C_EN/PIN = 0	RWU
	3	1'b0	PD_EN **0 – Normal working (default)** 1 – Forced power down by I^2C, lowest power state	RW
	2	1'b0	HPD_AUTO_PWRDWN_DISABLE **0 – Automatically enters power-down mode based on HPD_SNK (default)** 1 – Does not automatically enter power down mode	RW
	1:0	2'b10	I2C_DR_CTL. I^2C data rate supported for configuring device. 00 – 5 Kbps 01 – 10 Kbps **10 – 100 Kbps (default)** 11 – 400 Kbps (Note: HPD_AUTO_PWRDWN_DISABLE must be set before enabling 400 Kbps mode)	RW
0Ah	7	1'b1	Application mode selection (see *Device Functional Modes*) TMDS181 0 – Source **1 – Sink (default)**	RW
	6	1'b0	HPDSNK_GATE_EN. The field sets the functional relationship between HPD_SNK and HPD_SRC. **0 – HPD_SNK passed through to the HPD_SRC (default)** 1 – HPD_SNK does not pass through to the HPD_SRC.	RW
	5	1'b1	EQ_ADA_EN. This field enables the equalizer functioning state. 0 – Fixed EQ **1 – Adaptive EQ (default)** Writes are ignored when I2C_EN/PIN = 0	RWU
	4	1'b1	EQ_EN. This field enables the equalizer. 0 -- EQ disable **1 – EQ enable (default)** Writes are ignored when I2C_EN/PIN = 0	RW
	3	1'b0	Reserved	R
	2	1'b0	APPLY_RXTX_CHANGES, Self-clearing write-only bit. Writing a 1 to this bit will apply new TX_TERM, HDMI_TWPST1, EQ_EN, EQ_ADA_EN, VSWING, Fixed EQ Value settings to the clock and data lanes. Writes to the respective registers do not take immediate effect. This bit does not need to be written if I^2C configuration occurs while HPD_SNK are low, I^2CPD_EN = 1 or there is no HDMI clock applied and SIGN_EN is high.	W
	1:0	2'b01	DEV_FUNC_MODE. This field selects the device working function mode. 00 – Redriver mode: 250 Mbps – 3.4 Gbps **01 – Automatic redriver to retimer crossover at 1.0 Gbps (default)** 10 – Automatic retimer when HDMI2.0a based upon TMDS_CLOCK_RATIO_STATUS 11 – Retimer mode across full range 250 Mbps to 6 Gbps When changing crossover point, need to toggle PD_EN or toggle external HPD_SNK.	RW

Table 6. MISC CONTROL Register Field Descriptions (continued)

ADDRESS	BITS	DEFAULT	DESCRIPTION	ACCESS
0Bh	7:5	3'b000	Reserved	R
	4:3	2'b00	TX_TERM_CTL. Controls termination for HDMI TX. **00 – No termination (default)** 01 – 150 Ω to 300 Ω 10 – Reserved 11 – 75 Ω to 150 Ω Note: Writes are ignored when I2C_EN/PIN = 0; reflects the value of TX_TERM_CTL pin.	RWU
	2	1'b0	DDC_DR_SEL Defines the DDC output speed for DDC bridge **0 = 100 kbps (default)** 1 = 400 kbps (Note: HPD_AUTO_PWRDWN_DISABLE must be set before enabling 400 Kbps mode)	RW
	1	1'b0	TMDS_CLOCK_RATIO_STATUS. This field is updated from snoop of DDC write to slave address 0xA8 offset 0x20 bit 1 that occurred on the SDA_SRC/SCL_SRC interface. When bit 1 of address 0xA8 offset 0x20 in the SCDC register set is written to a 1'b1, then this field will be set to a 1'b1. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b0, then this field will be set to a 1'b0. This field is reset to default value whenever HPD_SNK is de-asserted for greater than 2 ms. **0 – TMDS Clock is 1/10 of TMDS bit period (default)** 1 – TMDS Clock is 1/40 of TMDS bit period	RWU
	0	1'b0	DDC_TRAIN_SETDISABLE; This field indicate the DDC training block function status. If disabled the device will only work in HDMI1.x or DVI modes. **0 – DDC training enable (default)** 1 – DDC training disable Note: To force TMDS_CLOCK_RATIO_STATUS to 1 this register bit must be set to 1 which will force the 1/40 mode for HDMI2.0	RW
0Ch	7:5	3'b000	VSWING_DATA: Data output swing control **000 – Vsadj set (default)** 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%	RW
	4:2	3'b000	VSWING_CLK: Clock output swing control: Default is set by Vsadj resistor value and the value of reg_0Dh[0]. **000 – Vsadj (default)** 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%	RW
	1:0	2'b00	HDMI_TWPST1[1:0]. HDMI de-emphasis FIR post-cursor-1 signed tap weight. (Retimer Mode Only) **00 – No de-emphasis (default)** 01 – 2 dB de-emphasis 10 – Reserved 11 – Reserved Note: Reflects value of PRE_SEL pin; Writes are ignored when I2C_EN/PIN = 0	RWU

8.5.3.3 Equalization Control Register

Table 7. Equalization Control Register Field Descriptions

ADDRESS	BITS	DEFAULT	DESCRIPTION		ACCESS
0Dh	7:6	2'b00	Reserved		R
	5:3	1'b000	Data lane EQ – Sets fixed EQ values		RW
			HDMI1.x	HDMI2.0a	
			000 – 0 dB (default)	**000 – 0 dB (default)**	
			001 – 4.5 dB	001 – 3 dB	
			010 – 6.5 dB	010 – 5 dB	
			011 – 8.5 dB	011 – 7.5 dB	
			100 – 10.5 dB	100 – 9.5 dB	
			101 – 12 dB	101 – 11 dB	
			110 – 14 dB	110 – 13 dB	
			111 – 16.5 dB	111 – 14.5 dB	
	2:1	1'b00	Clock lane EQ - Sets fixed EQ values		RW
			HDMI1.x	HDMI2.0a	
			00 – 0 dB (default)	**00 – 0 dB (default)**	
			01 – 1.5 dB	01 – 1.5 dB	
			10 – 3 dB	10 – 3 dB	
			11 – RSVD	11 – 4.5 dB	
	0	1'b0	DIS_HDMI2_SWG: **0 – Clock V_{OD} is half of set values when TMDS_CLOCK_RATIO_STATUS states in HDMI2.0a mode (default)** 1 – Disables TMDS_CLOCK_RATIO_STATUS control of the clock VOD so output swing is at full swing.		RW

8.5.3.4 RX PATTERN VERIFIER CONTROL/STATUS Register

Table 8. RX PATTERN VERIFIER CONTROL/STATUS Register Field Description(1)

ADDRESS	BITS	DEFAULT	DESCRIPTION	ACCESS
0Eh	7:4	4'b0000	PV_SYNC[3:0]. Pattern timing pulse. This field is updated for 8UI once every cycle of the PRBS generator. 1 bit per lane.	R
	3:0	4'b0000	PV_LD[3:0]. Load pattern-verifier controls into RX lanes. When asserted high, the PV_TO, PV_SEL, PV_LEN, PV_CP20, and PV_CP values are enabled into the corresponding RX lane. These values are then latched and held when PV_LD[n] is subsequently deasserted low. 1 bit per lane.	RWU
0Fh	7:4	4'b0000	PV_FAIL[3:0]. Pattern verification mismatch detected. 1 bit per lane.	RU
	3:0	4'b0000	PV_TIP[3:0]. Pattern search/training in progress. 1 bit per lane.	RU
10h	7	1'b0	PV_CP20. Customer pattern length 20/16 bits. **0 – 16 bits (default)** 1 – 20 bits	RW
	6	1'b0	Reserved	R
	5:3	3'b000	PV_LEN[2:0]. PRBS pattern length **000 – PRBS7 (default)** 001 – PRBS11 010 – PRBS23 011 – PRBS31 100 – PRBS15 101 – PRBS15 110 – PRBS20 111 – PRBS20	RW
	2:0	3'b000	PV_SEL[24:0]. Pattern select control **000 – Disabled (default)** 001 – PRBS 010 - Clock 011 - Custom 1xx – Timing only mode with sync pulse spacing defined by PV_LEN	RW
11h	7:0	'h00	PV_CP[7:0]. Custom pattern data.	RW
12h	7:0	'h00	PV_CP[15:8]. Custom pattern data.	RW
13h	7:4	4'b0000	Reserved	R
	3:0	4'b0000	PV_CP[19:16]. Custom pattern data. Used when PV_CP20 = 1'b1.	RW
14h	7:3	5'b00000	Reserved	R
	2:0	3'b000	PV_THR[2:0]. Pattern-verifier retain threshold.	RW
15h	7	1'b0	DESKEW_CMPLT. Indicates that TMDS lane deskew has completed when high.	R
	6:5	2'b00	Reserved	R
	4	1'b0	BERT_CLR. Clear BERT counter (on rising edge).	RSU
	3	1'b0	TST_INTQ_CLR. Clear latched interrupt flag.	RSU
	2:0	3'b000	TST_SEL[2:0]. Test interrupt source select.	RW
16h	7:4	4'b0000	PV_DP_EN[3:0]. Enable datapath verified based on DP_TST_SEL, 1 bit per lane.	RW
	3	1'b0	Reserved	R
	2:0	3'b000	DP_TST_SEL[2:0] Selects pattern reported by BERT_CNT[11:0], TST_INT[0] and TST_INTQ[0] and PV_DP_EN is non-zero. **000 – TMDS disparity or data errors (default)** 001 – FIFO errors 010 – FIFO overflow errors 011 – FIFO underflow errors 100 – TMDS deskew status 101,110,111 – Reserved	RW
17h	7:4	4'b0000	TST_INTQ[3:0]. Latched interrupt flag. 1 bit per lane.	RU
	3:0	4'b0000	TST_INT[3:0]. Test interrupt flag. 1 bit per lane.	RU
18h	7:0	'h00	BERT_CNT[7:0]. BERT error count. Lane 0	RU
19h	7:4	4'b0000	Reserved	R
	3:0	4'b0000	BERT_CNT[11:8]. BERT error count. Lane 0	RU

(1) If PV_DP_EN is used to monitor TMDS data path errors the counters for lanes 0, 1, 2, and 3 are ignored.

Table 8. RX PATTERN VERIFIER CONTROL/STATUS Register Field Description(1) (continued)

ADDRESS	BITS	DEFAULT	DESCRIPTION	ACCESS
1Ah	7:0	‘h00	BERT_CNT[19:12]. BERT error count. Lane 1	RU
1Bh	7:4	4’b0000	Reserved	R
	3:0	4’b0000	BERT_CNT[23:20]. BERT error count. Lane 1	RU
1Ch	7:0	‘h00	BERT_CNT[31:24]. BERT error count. Lane 2	RU
1Dh	7:4	4’b0000	Reserved	R
	3:0	4’b0000	BERT_CNT[35:32]. BERT error count. Lane 2	RU
1Eh	7:0	‘h00	BERT_CNT[19:12]. BERT error count. Lane 3	RU
	7:4	4’b0000	Reserved	R
1Fh	3:0	‘h00	BERT_CNT[23:20]. BERT error count. Lane 3	RU
20h	7	1’b0	Power Down Status Bit. **0 – Normal Operation (default)** 1 – Device in Power Down Mode	R
	6	1’b0	Standy Status Bit. **0 – Normal Operation (default)** 1 – Device in Standby Mode	R
	5:0	6’b000000	Reserved	R

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMDS181 was defined to work in many applications. This includes source applications like a Blu-ray™ DVD player or AVR. The adaptive receive equalizer makes it ideal for sink applications like UHDTV, monitors, and projectors where cable length can be widely varied. When in a sink application, the designer must consider several system-level architectures. The TMDS181 is also capable of working in an active cable to extend the cable length even further.

9.2 Typical Applications

9.2.1 Source Side Application

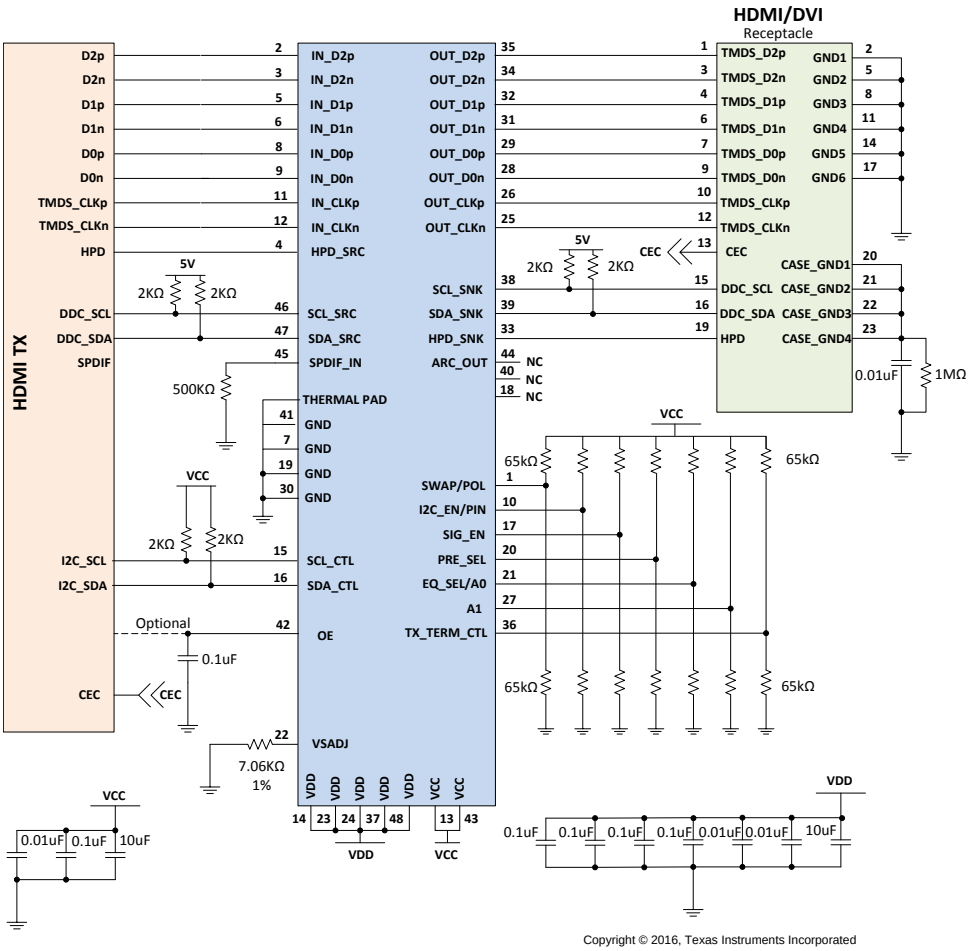


Figure 32. TMDS181 in Source Side Application

Typical Applications (continued)

9.2.1.1 Design Requirements

The TMDS181 can be designed into many different applications. All applications have certain requirements for the system to work properly. Two voltage rails are required to support the lowest power consumption possible. The OE pin must have a 0.1 µF capacitor to ground. This pin can be driven by a processor, but the pin needs to change states after voltage rails have stabilized. The best way to configure the device is by using I^2C. However, pin strapping is provided because I^2C is not available in all cases. As sources may have different naming conventions, it is necessary to confirm that the link between the source and the TMDS181 are correctly mapped. A swap function is provide for the input pins in case signaling is reversed between source and device. The control pin values in Table 9 are based upon driving pins with a microcontroller; otherwise, the shown pullup/pulldown configuration meet device levels. Table 9 provides information on expected values in order to perform properly.

Table 9. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
V_{DD}	1.2 V
Main link input voltage	V_{ID} = 75 mVpp to 1.2 Vpp
Control pin max voltage for low	65 kΩ resistor connected to GND
Control pin voltage range mid	Not connected
Control pin min voltage for high	65 kΩ resistor connected to Vcc
VSADJ resistor	7.06 kΩ 1%

9.2.1.2 Detailed Design Procedure

The TMDS181 is a signal conditioning device that provides several forms of signal conditioning to support compliance for HDMI or DVI at a source connector. These forms of signal conditioning are accomplished using receive equalization, retiming, and output driver configure ability. The transmitter drives 2 to 3 inches of board trace and connector when compliance is required at the connector.

To design in the TMDS181 for a source side application, the designer must understand the following.

- Determine the loss profile between the GPU/chipset and the HDMI/DVI connector.
- Based upon this loss profile and signal swing, determine the optimal location for the TMDS181 in order to pass source electrical compliance, usually within 2 to 3 inches of the connector.
- Use the typical application Figure 32 for information on control pin resistors.
- The TMDS181 has a receiver adaptive equalizer, but can also be configured using EQ_SEL control pin.
- Set the V_{OD}, pre-emphasis and termination levels appropriately to support compliance by using the appropriate VSADJ resistor value and setting PRE_SEL and TX_TERM_CTL control pins.
- The thermal pad must be connected to ground.
- See schematics in Figure 32 on recommended decoupling capacitors from V_{CC} pins to ground.

9.2.1.3 Application Curves

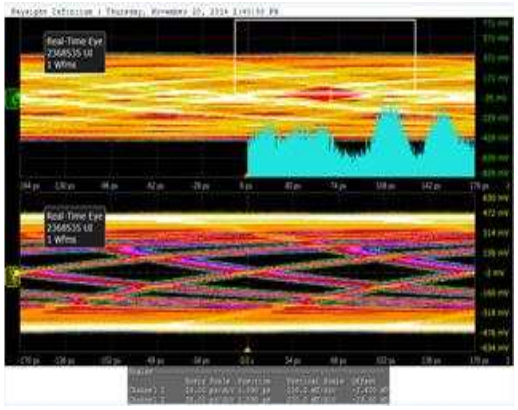


Figure 33. Input Eye After 3M Cable at 5.94Gbps

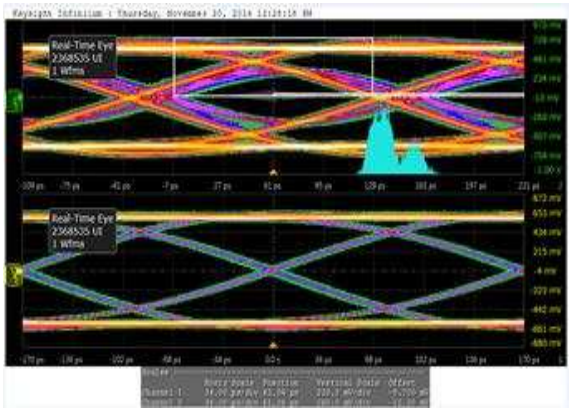


Figure 34. Output Eye from TMDS181 after 3M Input Cable at 5.94Gbps

9.2.2 Sink Side Application

For a sink side application, HPD needs consideration. The TMDS181 drives the HPD signal to 3.3 V, which meets requirements, but if 5 V HPD signaling is required, the two circuits shown in Figure 35 are required. As sources are not consistent in implementing all aspects of the DDC link, TI recommends to configure the TMDS181 as per Figure 35. Another consideration for how HPD is implemented is the architecture and behavior of the HDMI RX/scalar. The standard requires sinks to clear the TMDS_CLOCK_RATIO_STATUS in the SCDC when either +5 V power signal from source is not present or when hot plug detect pin goes low for 100 ms or more. When HPD goes low, the TMDS181 automatically clears this bit. The TMDS181 expects the TMDS_CLOCK_RATIO_STATUS bit to be set with a write from source to receiver/sink. If this does not happen, the TMDS181 may come up in the wrong configuration. Until the HDMI ecosystem matures, TI recommends to implement sink application as per Figure 36 to address this.

Designing the TMDS181 into a sink side application requires similar care as for a source side application. However, because compliance is at the receiver, there is more flexibility for the transmitter to the HDMI RX/chipset link. Because many different reflection points are possible, the TMDS181 allows for swing, pre-emphasis, and transmitter termination control that can help minimize these reflections. The TMDS181 has a 3.3 V HPD drive capability which meets requirements. In cases where the designer needs to support 5 V HPD drive capability, the circuit shown in Figure 35 is required.

To design in the TMDS181 for a source side application, the designer must understand the following.

- Determine the loss profile between the RX/chipset and the HDMI/DVI connector
- Based upon this loss profile and signal swing, determine the optimal location for the TMDS181 to pass sink electrical compliance.
- Use the typical application Figure 35 for information on control pin resistors.
- The TMDS181 has a receiver adaptive equalizer, but can also be configured using EQ_SEL control pin.
- Set the V_{OD}, pre-emphasis and termination levels appropriately to support a link between TMDS181 and HDMI RX/chipset by using the appropriate VSADJ resistor value and setting PRE_SEL and TX_TERM_CTL control pins.
- The thermal pad must be connected to ground.
- See schematics in Figure 35 on recommended decoupling capacitors from VCC pins to ground.
- Because the HDMI ecosystem supporting 4k2kp60 is not mature, TI recommends to design the TMDS181 into the sink application as shown in Figure 36.

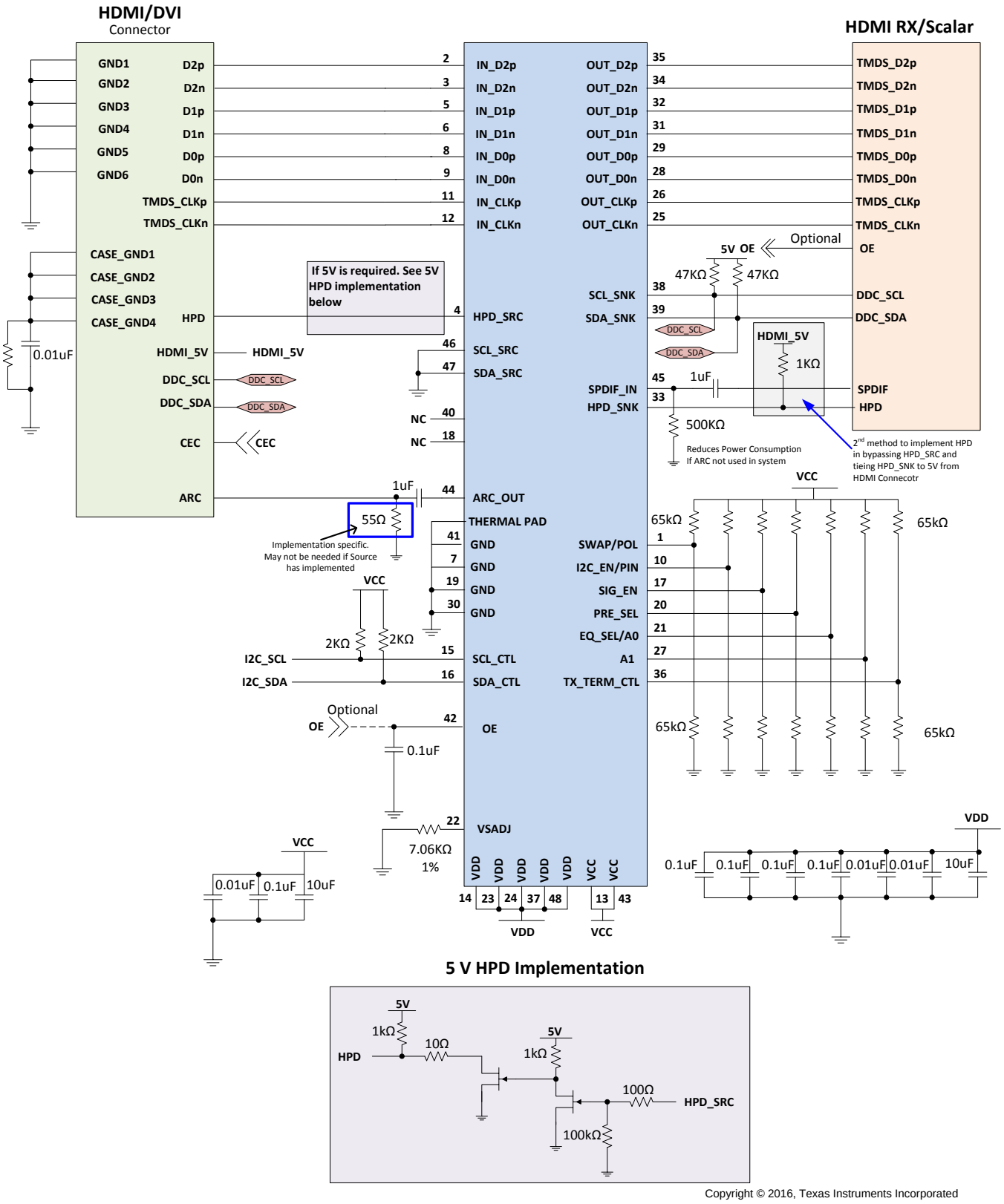


Figure 35. TMDS181 in Sink Side Application (Including 5 V HPD Implementation)

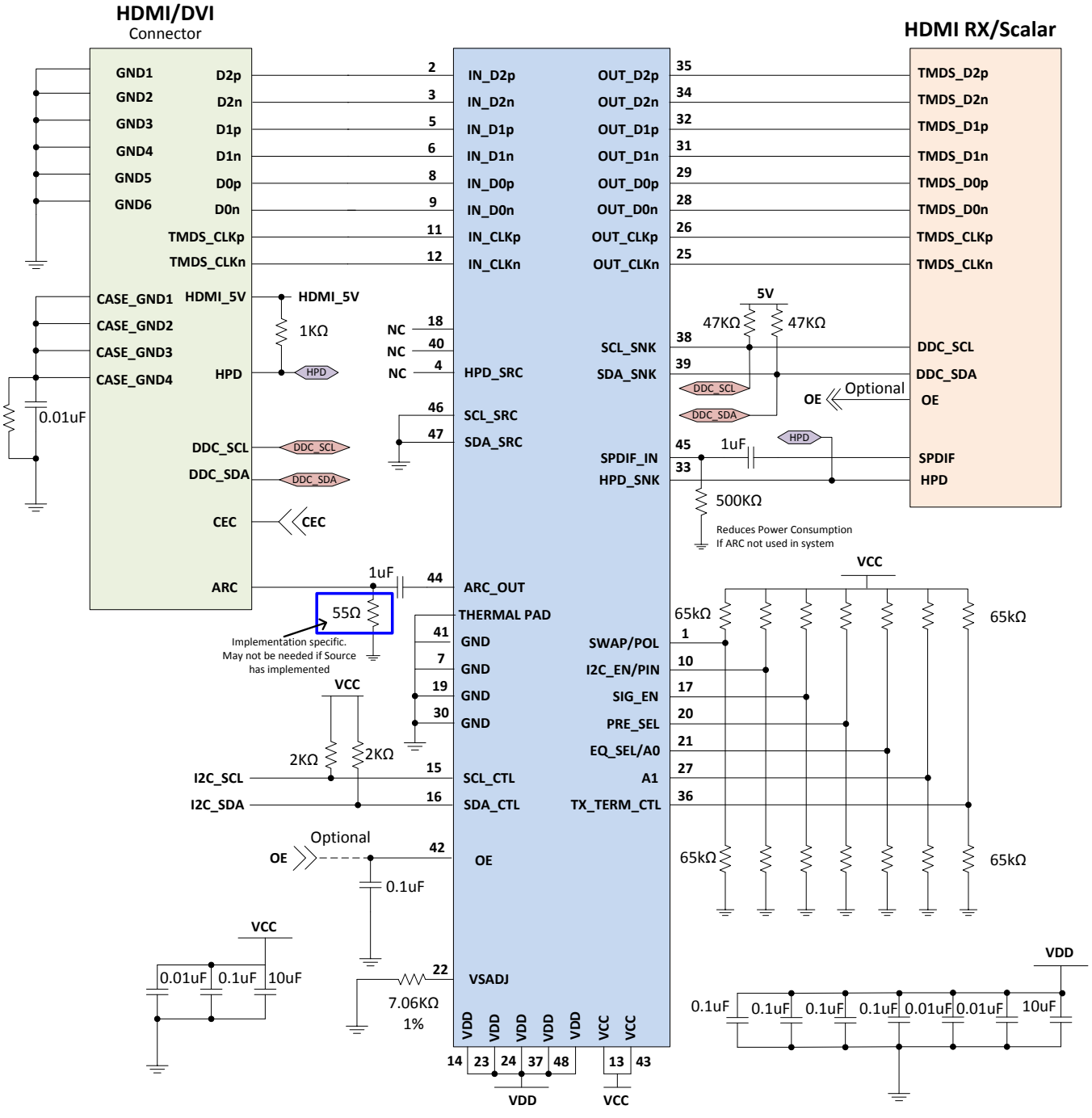


Figure 36. TMDS181 in Sink Side Application

9.2.3 Application Chain Showing DDC Connections

The DDC circuitry inside the TMDS181 allows multiple stage operation (see Figure 36). The retimer devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time of flight considerations for the maximum bus speed requirements.

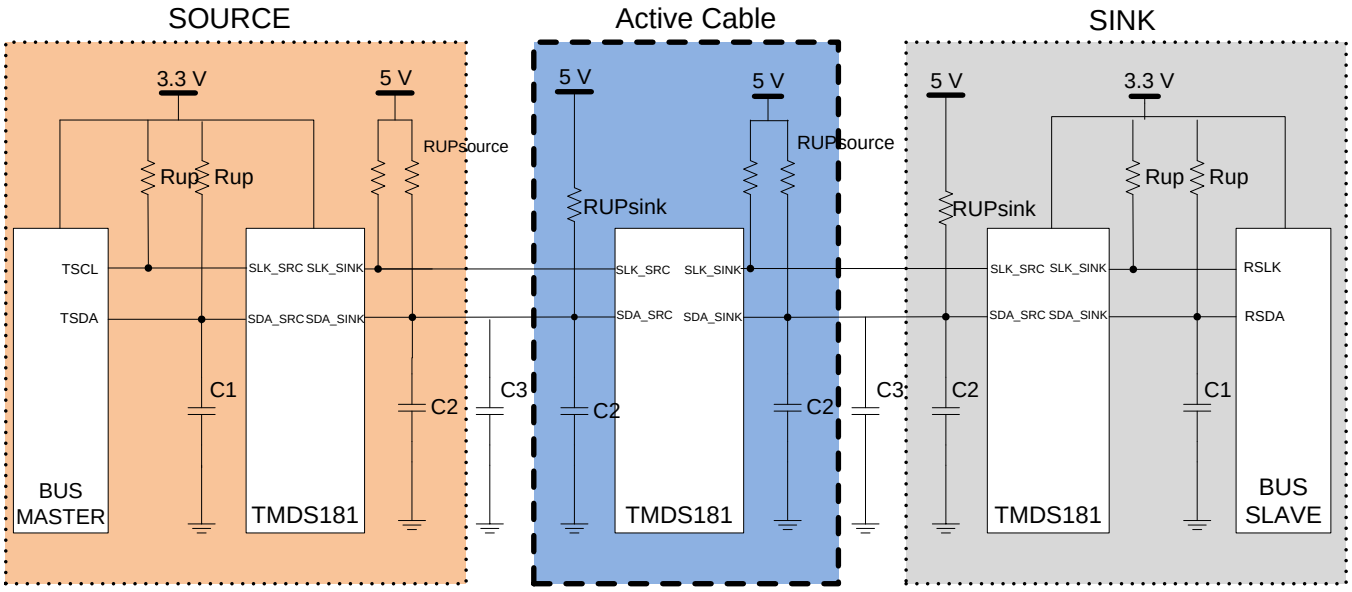


Figure 37. Typical Series Application

9.2.3.1 Detailed Design Procedure

9.2.3.1.1 DDC Pullup Resistors

NOTE

This section is informational only and subject to change depending upon the specific system implementation.

The pullup resistor value is determined by two requirements.

1. The maximum sink current of the I^2C buffer: The maximum sink current is 3 mA or slightly higher for an I^2C driver supporting standard-mode I^2C operation.

$$R_{up(min)} = \frac{V_{CC}}{I_{sink}} \quad (1)$$

2. The maximum transition time on the bus: The maximum transition time, T, of an I^2C bus is set by an RC time constant. The parameter, k, can be calculated from Equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 10 summarizes the possible values of k under different threshold combinations.

$$T = k \times RC \quad (2)$$

where

- R is the pullup resistor value.
- C is the total load capacitance.

$$V(t) = V_{DD} \times (1 - e^{\frac{-t}{RC}}) \quad (3)$$

Table 10. Value k upon Different Input Threshold Voltages

Vth–\Vth+	0.7VCC	0.65VCC	0.6VCC	0.55VCC	0.5VCC	0.45VCC	0.4VCC	0.35VCC	0.3VCC
0.1VCC	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15VCC	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2VCC	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25VCC	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3VCC	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	

From Equation 1, $R_{up(min)}$ = 5.5 V / 3 mA = 1.83 kΩ to operate the bus under a 5 V pullup voltage and provide <3 mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, $R_{up(min)}$ can be as low as 1.375 kΩ. If DDC working at standard mode of 100 Kbps, the maximum transition time T is fixed, 1 μs, and using the k values from Table 10, the recommended maximum total resistance of the pullup resistors on an I^2C bus can be calculated for different system setups. If DDC working in fast mode of 400 Kbps, the transition time should be set at 300 ns according to I^2C specification. To support the maximum load capacitance specified in the HDMI specification, calculate Ccable(max) = 700 pF / Csource = 50 pF / Ci = 50 pF, R(max) as shown in Table 11.

Table 11. Pullup Resistor Upon Different Threshold Voltages and 800 pF Loads

Vth-\Vth+	0.7VCC	0.65VCC	0.6VCC	0.55VCC	0.5VCC	0.45VCC	0.4VCC	0.35VCC	0.3VCC	UNIT
0.1VCC	1.14	1.32	1.54	1.8	2.13	2.54	3.08	3.84	4.97	kΩ
0.15VCC	1.2	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
0.2VCC	1.27	1.51	1.8	2.17	2.66	3.34	4.35	6.02	9.36	kΩ
0.25VCC	1.36	1.64	1.99	2.45	3.08	4.03	5.6	8.74	18.12	kΩ
0.3VCC	1.48	1.8	2.23	2.83	3.72	5.18	8.11	16.87	—	kΩ

To accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

9.2.3.1.2 Compliance Testing

Compliance testing is very system design specific. Properly designing the system and configuring the TMDS181 can help pass compliance for a system. The following information is a starting point to help prepare for compliance testing. As each system is different there are many features in the TMDS181 to help tune the circuit. These include fixed RX equalization, adaptive RX equalization, V_{OD} adjust by several methods, pre-emphasis/de-emphasis, and source termination. Passing both HDMI2.0a and HDMI1.4b compliance is easier to accomplish when using I^2C as this provides more fine tuning capability.

9.2.3.1.2.1 Pin Strapping Configuration for HDMI2.0a and HDMI1.4b

- VSADJ Resistor = 7.06 kΩ: Note: This value may be changed in order to improve Intra-pair skew margin but will increase output V_{OD} so care must be taken to avoid V_{OD} and V_L compliance issues.
- PRE_SEL = L for -2 dB (For Intra-pair Skew)
- TX_TERM_CTL = NC for Auto Select.

9.2.3.1.2.2 I^2C Control for HDMI2.0a and HDMI1.4b

- VSADJ Resistor = 7.06 kΩ: This value may be changed in order to improve Intra-pair skew but will increase V_{OD} so care must be taken to avoid V_{OD} and V_L compliance issues. The V_{OD} can be increased or decreased by using I^2C Reg0Ch[7:2]
- PRE_SEL = Reg0Ch[1:0] = 01 for -2 dB (Labeled HDMI_TWPST)
- TX_TERM_CTL = NC for Auto Select.
  - Reg0Bh[4:3] = 00 → No TX Term; HDMI1.4b < 2 Gbps (This may be best value for all HDMI1.4b)
  - Reg0Bh[4:3] = 01 → 150 Ω to 300 Ω; HDMI1.4b > 2 Gbps
  - Reg0Bh[4:3] = 11 → 75 Ω to 150 Ω; HDMI2.0a

10 Power Supply Recommendations

To minimize the power consumption of customer application, TMSD181 used the dual power supply. V_{CC} is 3.3 V with 5% range to support the I/O voltage. V_{DD} is 1.2 V to supply the internal digital control circuit. TMDS181 operates in three different working states.

- Power-down mode:
  - OE = Low puts the device into its lowest power state by shutting down all function blocks.
    - When OE is reasserted, the transitions from L → H create a reset, and if the device is programmed through I^2C, it must be reprogrammed.
  - Writing a 1 to register 09h[3].
  - OE = High, HPD_SNK = Low
- Standby mode: HPD_SNK = High, but no valid clock signal detect on clock lane.
- Normal operation: Working in redriver or retimer
- When HPD asserts, the device CDR and output enables based on the signal detector circuit result.
- HPD_SRC = HPD_SNK in all conditions. The HPD channel is operational when V_{CC} is over 3 V.

NOTE

1. When the TMDS181 is put into a power-down state, the I^2C registers are cleared. This is important as the TMDS_CLOCK_RATIO_STATUS bit will be cleared. If cleared and HDMI2.0 resolutions are to be supported, the TMDS181 expects the source to write a 1 to this bit location. If this does not happen, the PLL will not be set properly and no video may be evident.
2. Power performance of the TMDS181 is highly dependent upon the HDMI transmitter architecture driving the TMDS181 receiver. The TMDS181 has integrated the termination resistors, which increases the power consumption on the 3.3 V rail by as much as 400 mW. This is the power required by the HDMI transmitter to switch and not needed by the TMDS181 to operate properly.

Table 12. Power-Up and Operation Timing Requirements

INPUTS					STATUS						
HPD_SNK	OE	SIG_EN	IN_CLK	DATA RATE	HPD_SRC	IN_Dx	SDA/SCL_CTL	OUT_Dx OUT_CLK	DDC	ARC	MODE
X	L	H or L	X	X	H	RX Termination On	Disable	High-Z	Disabled	Disable	Power-down mode
L	H	H or L	X	X	L	RX Termination On	Active	High-Z	Disabled	Disable	Power-down mode
H	H	H or L	X	X	H	RX Termination On	Active	High-Z	Disabled	Disable	Power-down mode by W 1 to 09h[3]
H	H	H (no valid signal)	No valid TMDS clock	X	H	D0-D2 disabled with RX termination On, IN_CLK active	Active	High-Z	Active	Active	Standby mode (squelch waiting)
H	H	H or L (no valid signal)	No valid TMDS clock	Retimer mode	H	D0-D2 disabled with RX termination On, IN_CLK activee	Active	High-Z	Active	Active	Standby mode (Squelch waiting)
H	H	H (Valid signal)	Valid TMDS clock	Retimer mode	H	RX active	Active	TX active	Active	Active	Normal operation
H	H	L (no valid signal)	No valid TMDS clock	Redriver mode	H	RX active	Active	TX active	Active	Active	Normal operation
H	H	H (Valid signal)	Valid TMDS clock	Redriver mode	H	RX active	Active	TX active	Active	Active	Normal operation

11 Layout

11.1 Layout Guidelines

For the TMDS181 on a high-K board: It is required to solder the PowerPAD™ onto the thermal land to ground. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the TMDS181 can operate over the full temperature range by soldering the PowerPAD onto the thermal land.

On a low-K board: For the device to operate across the temperature range on a low-K board, the designer must use a 1-oz Cu trace connecting the GND pins to the thermal land. A simulation shows $R_{\theta JA}$ = 100.84°C/W allowing 545 mW power dissipation at 70°C ambient temperature. A general PCB design guide for PowerPAD packages is provided in *PowerPAD Thermally Enhanced Package*, SLMA002. TI recommends using at a minimum a four-layer stack to accomplish a low-EMI PCB design. TI recommends six layers as the TMDS181 is a two-voltage-rail device.

- Routing the high-speed TMDS traces on the top layer avoids the use of vias (and their discontinuities) and allows for clean interconnects from the HDMI connectors to the retimer inputs and outputs. It is important to match the electrical length of these high-speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed single layer establishes controlled impedance for transmission link interconnects and provides an excellent low-inductance path for the return current flow.
- Placing a power plane next to the ground plane creates an additional high-frequency bypass capacitance.
- Routing slower-speed control signals on the bottom layer allows for greater flexibility because these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep symmetry. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

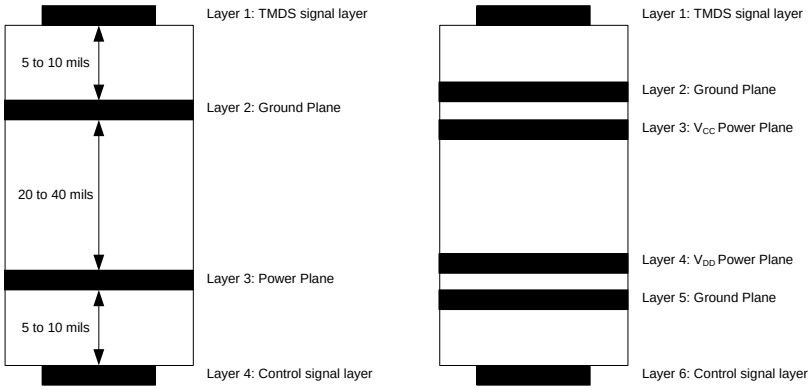
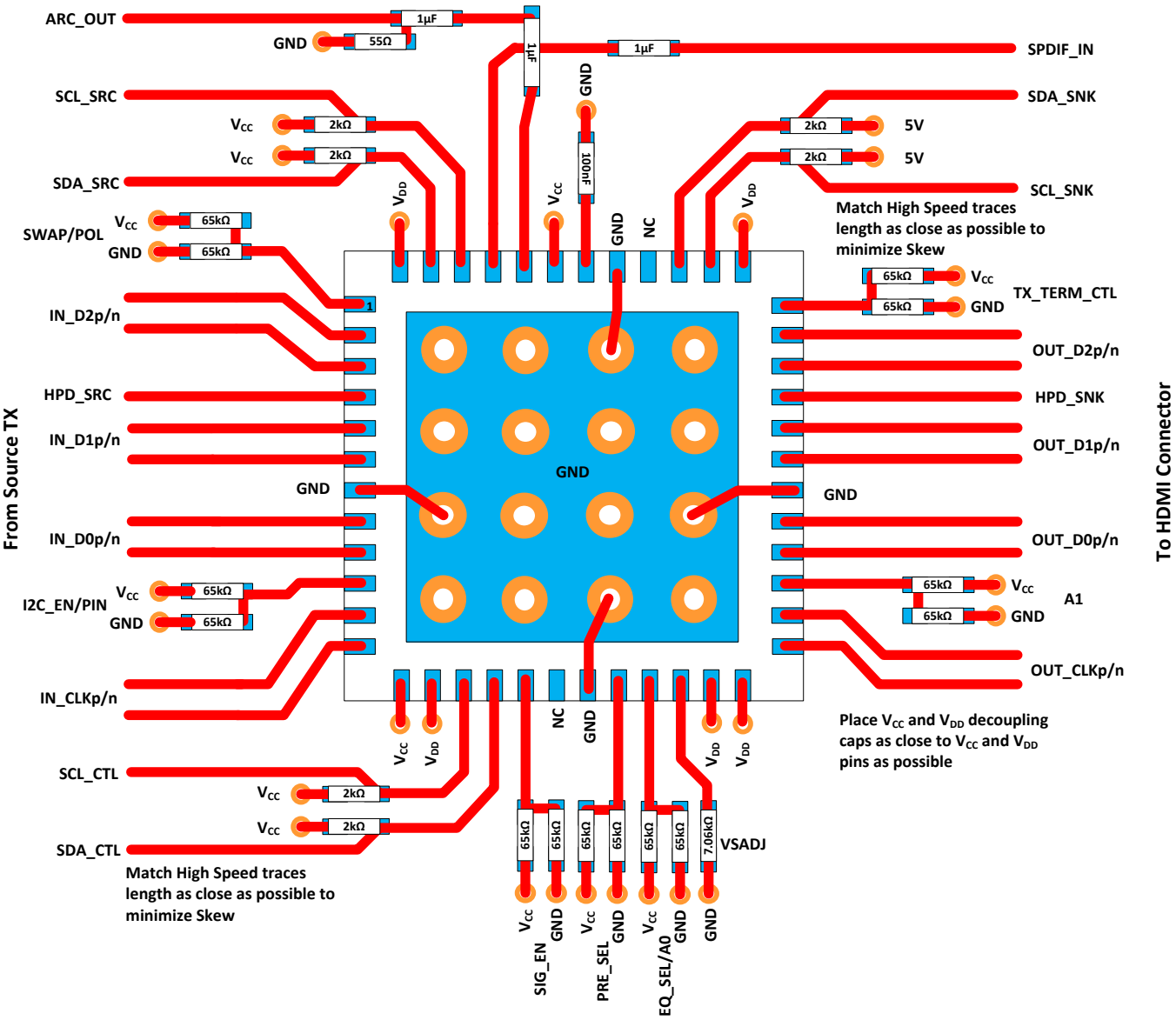


Figure 38. Recommended 4- or 6-Layer PCB Stack

11.2 Layout Example



A. If ARC is not used, tie a 500 kΩ resistor to GND at the SPDIF_IN pin.

B. The 55 Ω resistor to GND on the ARC_OUT pin is implementation specific and may not be needed if it is already implemented elsewhere.

Figure 39. Layout Example – Source Side

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

本节标识的文档均在本规范中引用。为简化文本，文中的大多数参考文献均用文档标签 [文档标签] 标识，而不使用完整的文档标题。

1. [HDMI] 高清多媒体接口规范版本 1.4b，2011 年 10 月
2. [HDMI] 高清多媒体接口规范版本 2.0a，2015 年 3 月
3. [HDMI] 高清多媒体接口 CTS 版本 1.4b，2011 年 10 月
4. [HDMI] 高清多媒体接口 CTS 版本 2.0k，2015 年 6 月
5. [I²C] I²C 总线规范版本 2.1，2000 年 1 月

12.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **13.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TMDS181	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TMDS181I	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

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Blu-Ray, Blu-ray are trademarks of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMDS181IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TMDS181I	Samples
TMDS181IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TMDS181I	Samples
TMDS181RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TMDS181	Samples
TMDS181RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TMDS181	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

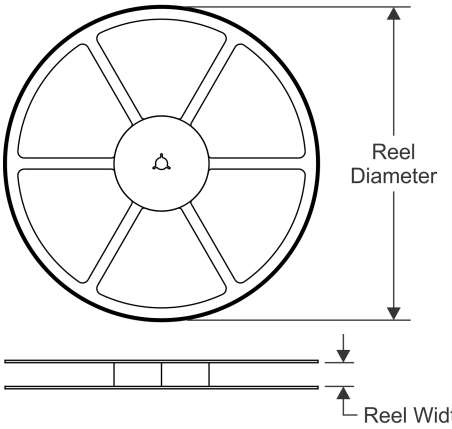
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

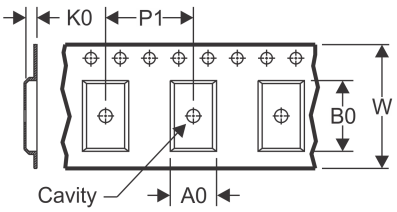
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

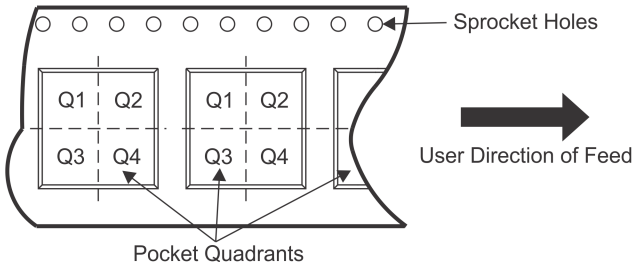


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

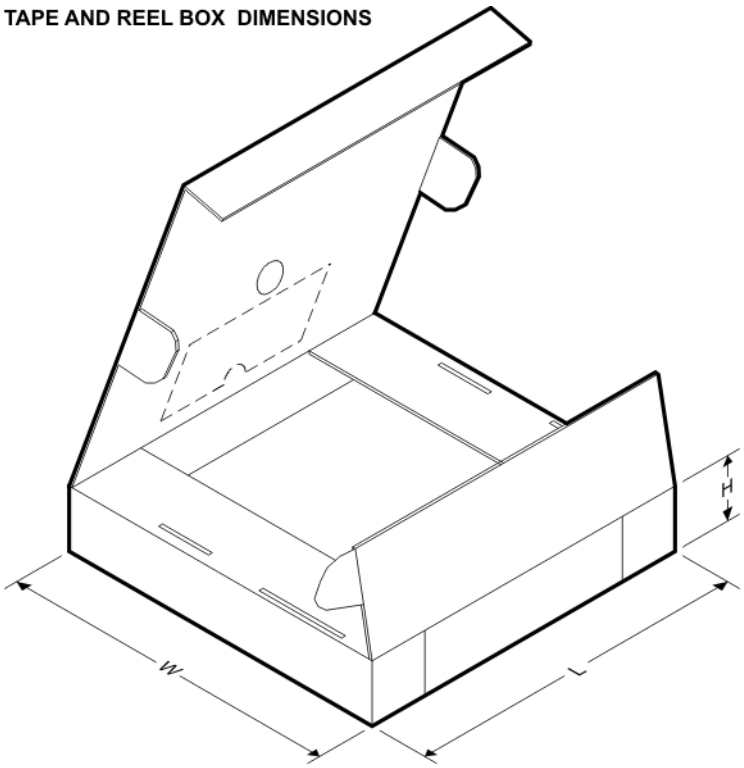
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS181IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TMDS181IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TMDS181RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TMDS181RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMDS181IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TMDS181IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
TMDS181RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TMDS181RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

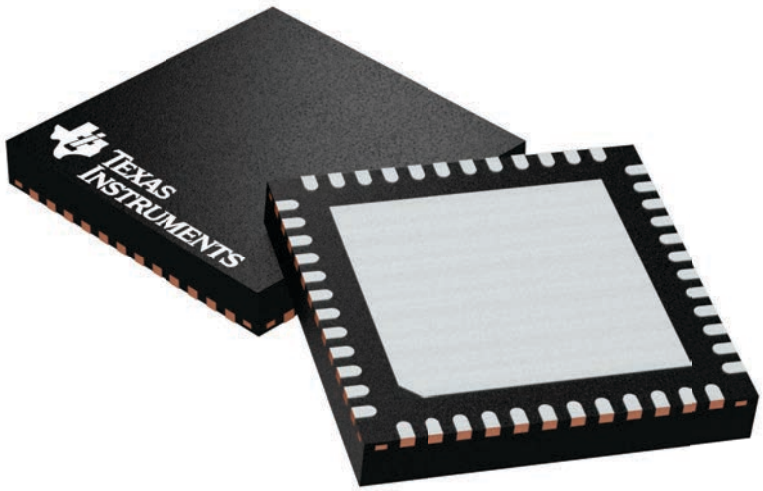
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

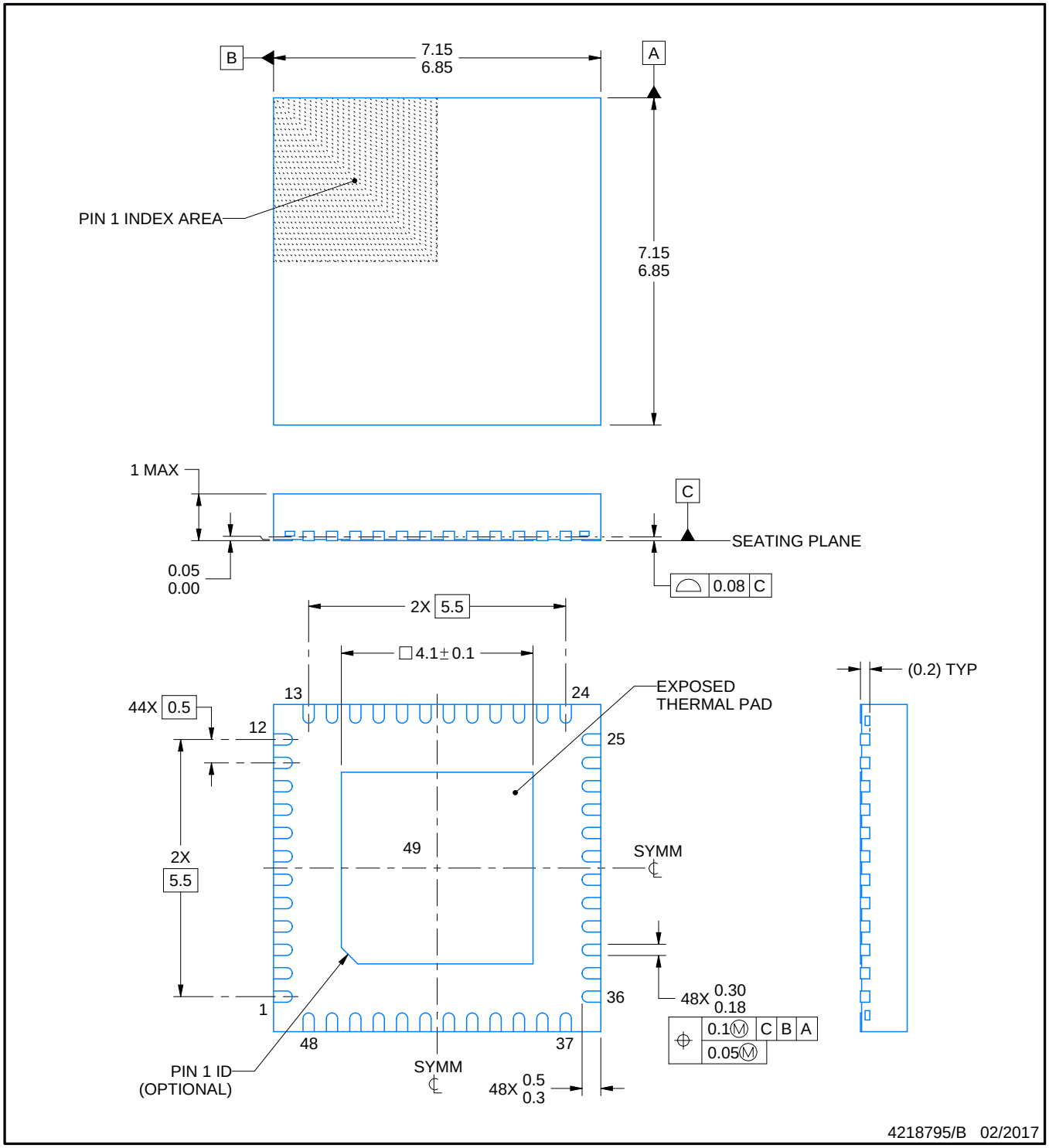
4224671/A

RGZ0048B

PACKAGE OUTLINE

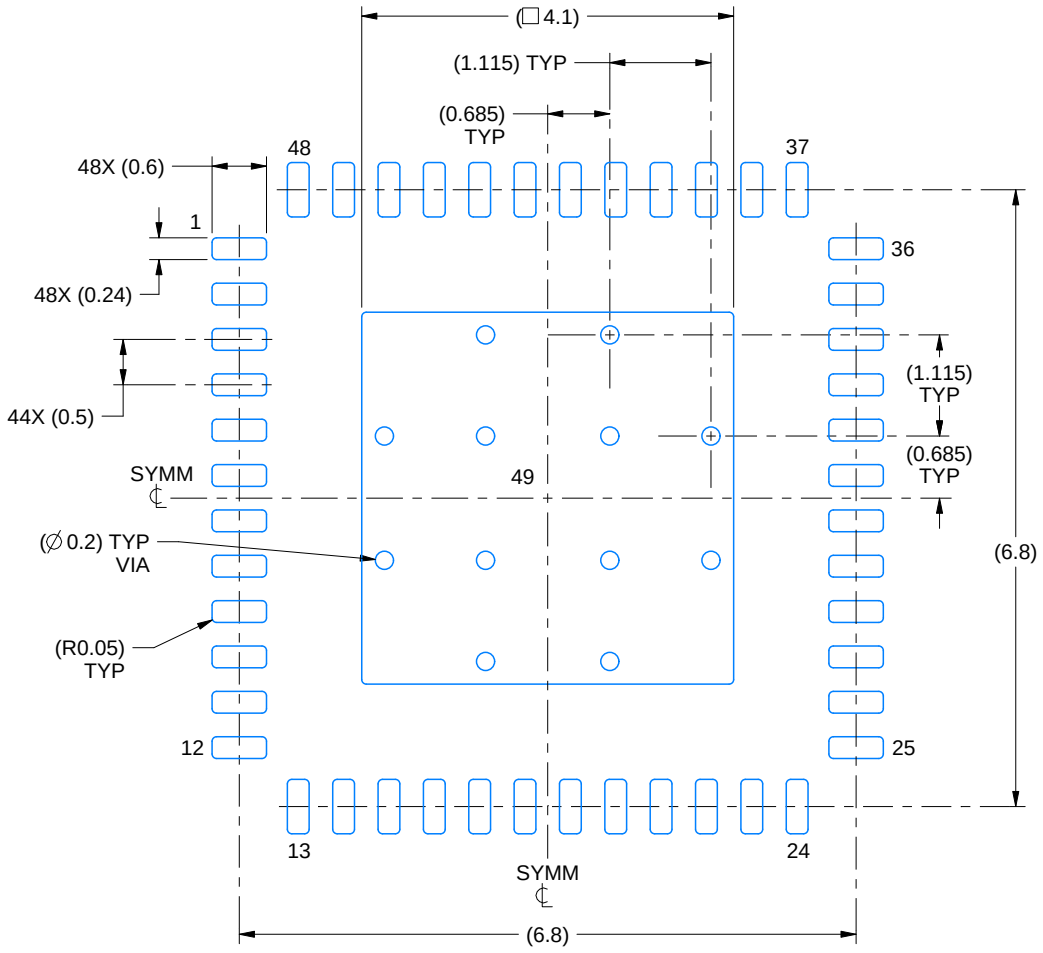
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

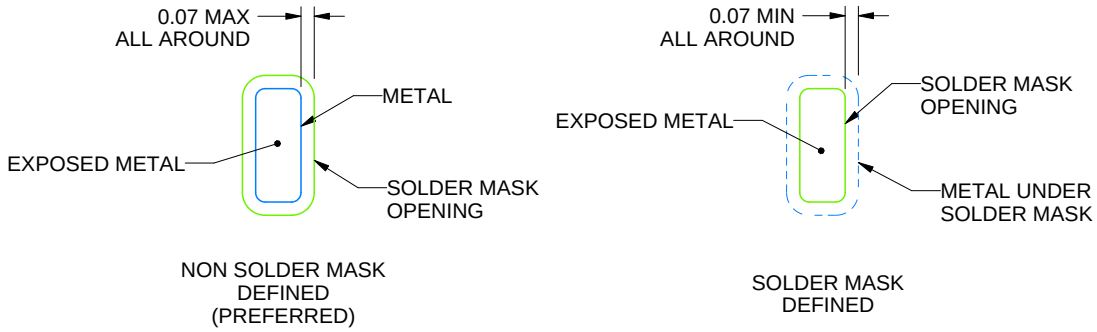


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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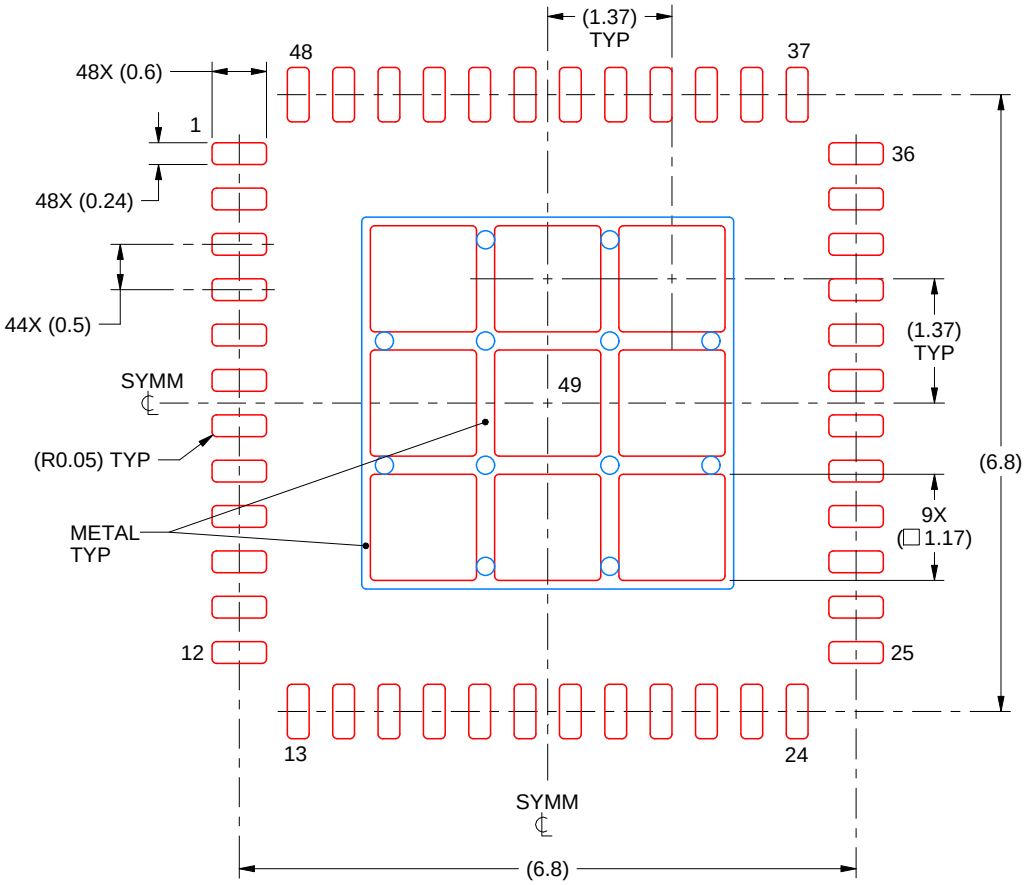
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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