14.2Gbps 四通道、双模式线性均衡器

查询样片: **SN65LVCP1414**

特性

- 背板和线缆连接串行运行数据速率高达 **14.2Gbps** 的四通道、单向、多速率、双模式线性均衡器
- 线性均衡增加了系统执行判决反馈均衡器 **(DFE)** 时的链路裕量
- 针对背板模式或者线缆模式，在具有 **1dB** 阶跃控制的 **7.1GHz** 上可实现 **17dB** 模拟均衡
- 输出线性动态范围：**1200mV**
- 带宽：**> 20GHz -** 典型值
- **7.1GHz** 上，好于 **15dB** 的回波损耗
- 支持带外 **(OOB)** 信令
- 低功耗，**2.5V VCC** 时，每通道为 **80mW**（典型值）
- **38** 端子 **QFN**（四方扁平、无引线）**5mm x 7mm x 0.75mm**，**0.5mm** 端子间距
- 到 **100Ω** 差分印刷电路板 **(PCB)** 传输线路的出色阻抗匹配
- 通用输入输出接口 **(GPIO)** 或者 **I^{2}C** 控制
- **2.5V** 和 **3.3V±5%** 单电源
- **2kV** 静电放电 **(ESD)** 人体模型 **(HBM)**
- 流经阳引脚的数据流简化了路由访问
- 小型封装尺寸节省了电路板空间
- 低功率

应用范围

- 电信和数据通信中的高速连接
- 针对 **10GbE**，**16GFC**，**10G** 同步光网络 **(SONET)**，**SAS**，**SATA**，通用公共无线接口 **(CPRI)**，开放基站架构协议 **(OBSAI)**，**Infiniband**，**10GBase-KR**，和 **XFI/SFI** 的背板和线缆连接

说明

SN65LVCP1414 是一款异步、协议无关、低延迟、四通道线性均衡器，此均衡器针对高达 14.2Gbps 的数据速率，以及针对背板或有源线缆应用中的损耗补偿进行了优化。 SN65LVCP1414 的架构设计用于与一个特定用途集成电路 (ASIC) 或者一个现场可编程栅极阵列 (FPGA)（采用判决反馈均衡器 (DFE) 来实现数字均衡）一起运行。 SN65LVCP1414 线性均衡器保持已发送信号的波形，以确保最优 DFE 性能。
SN65LVCP1414 在充分发挥 DFE 效率的同时提供了一个低功耗解决方案。

SN65LVCP1414 可经由 I^{2}C 或者 GPIO 接口进行配置。 SN65LVCP1414 的 I^{2}C 接口使得用户能够独立地控制均衡、路径增益、和针对每个独立通道的输出动态范围。 在 GPIO 模式下，通过使用 GPIO 输入引脚，可为所有通道设置均衡、路径增益、和输出动态范围。

SN65LVCP1414 输出可由 I^{2}C 单独禁用。

SN65LVCP1414 在一个 2.5V 或者 3.3V 单电源下运行。

SN65LVCP1414 采用 38 引脚 5mm x 7mm x 0.75mm QFN（四方扁平无引线）无铅 0.5mm 焊球间距封装，额定运行温度范围 -40°C 至 85°C。

English Data Sheet: SLLSEC5

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

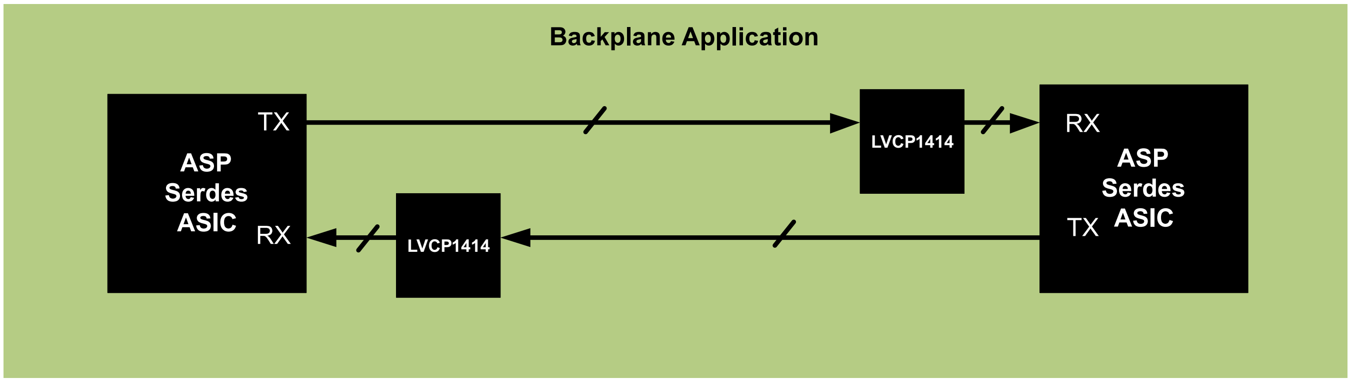


Figure 1. Typical Backplane Application – Trace Mode

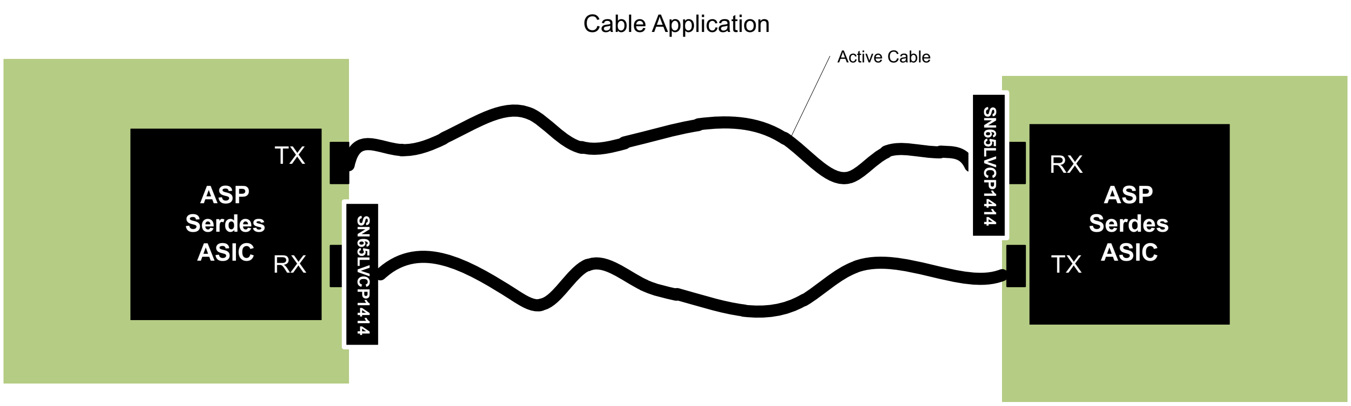


Figure 2. Typical Cable Application – Cable Mode

Block Diagram (GPIO or I²C Mode)

A simplified block diagram of the SN65LVCP1414 is shown in Figure 3 for GPIO or I²C input control mode. This compact, low power, 14.2Gbps quad-channel dual-mode linear analog equalizer consists of four high-speed data paths and an input GPIO pin logic-control block and a two-wire interface with a control-logic block.

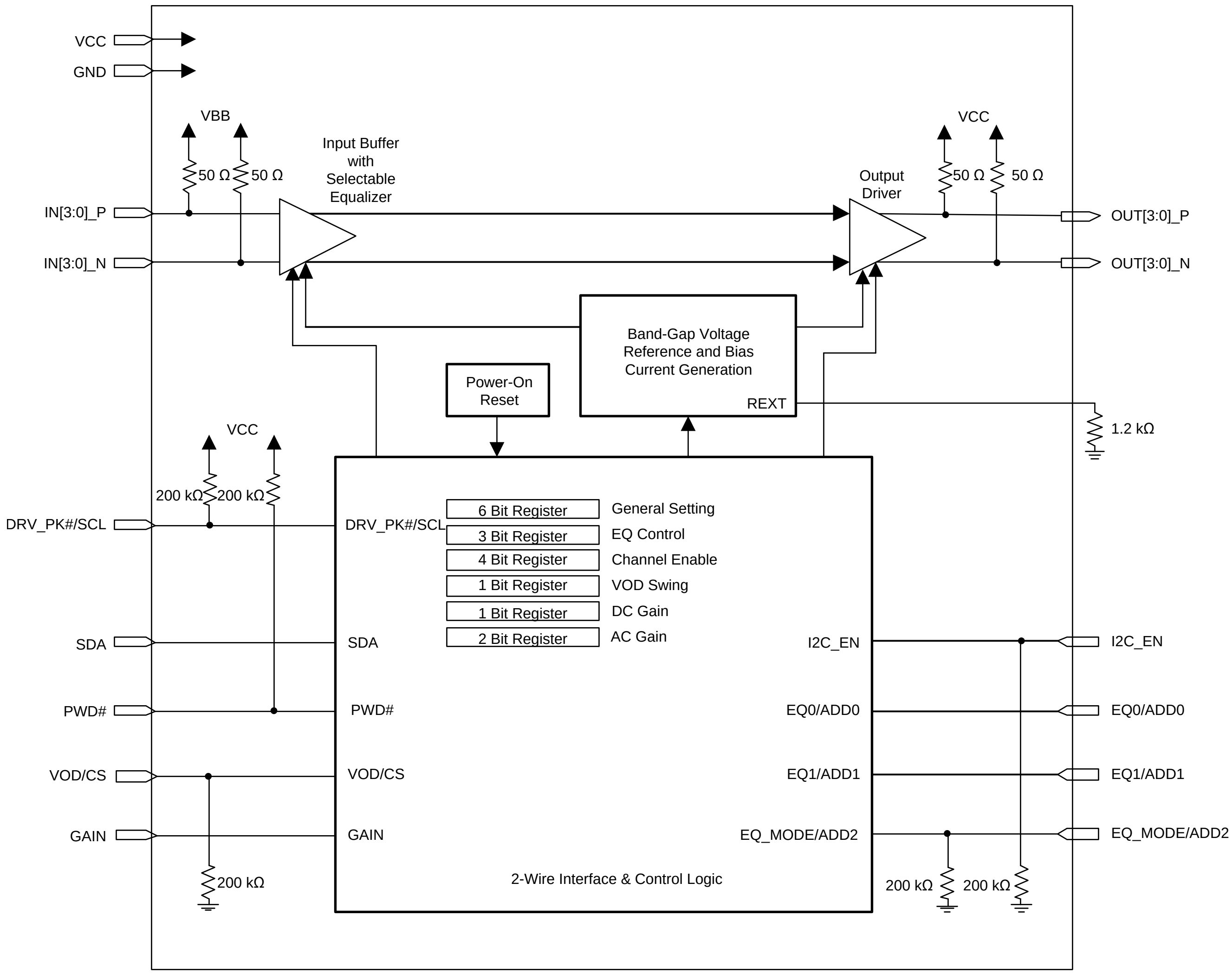


Figure 3. Simplified Block Diagram of the SN65LVCP1414

Package

The package pin locations and assignments are shown in Figure 4. The SN65LVCP1414 is packaged in a 5mm x 7mm x 0.75mm, 38 pin, 0.5mm pitch lead-free QFN.

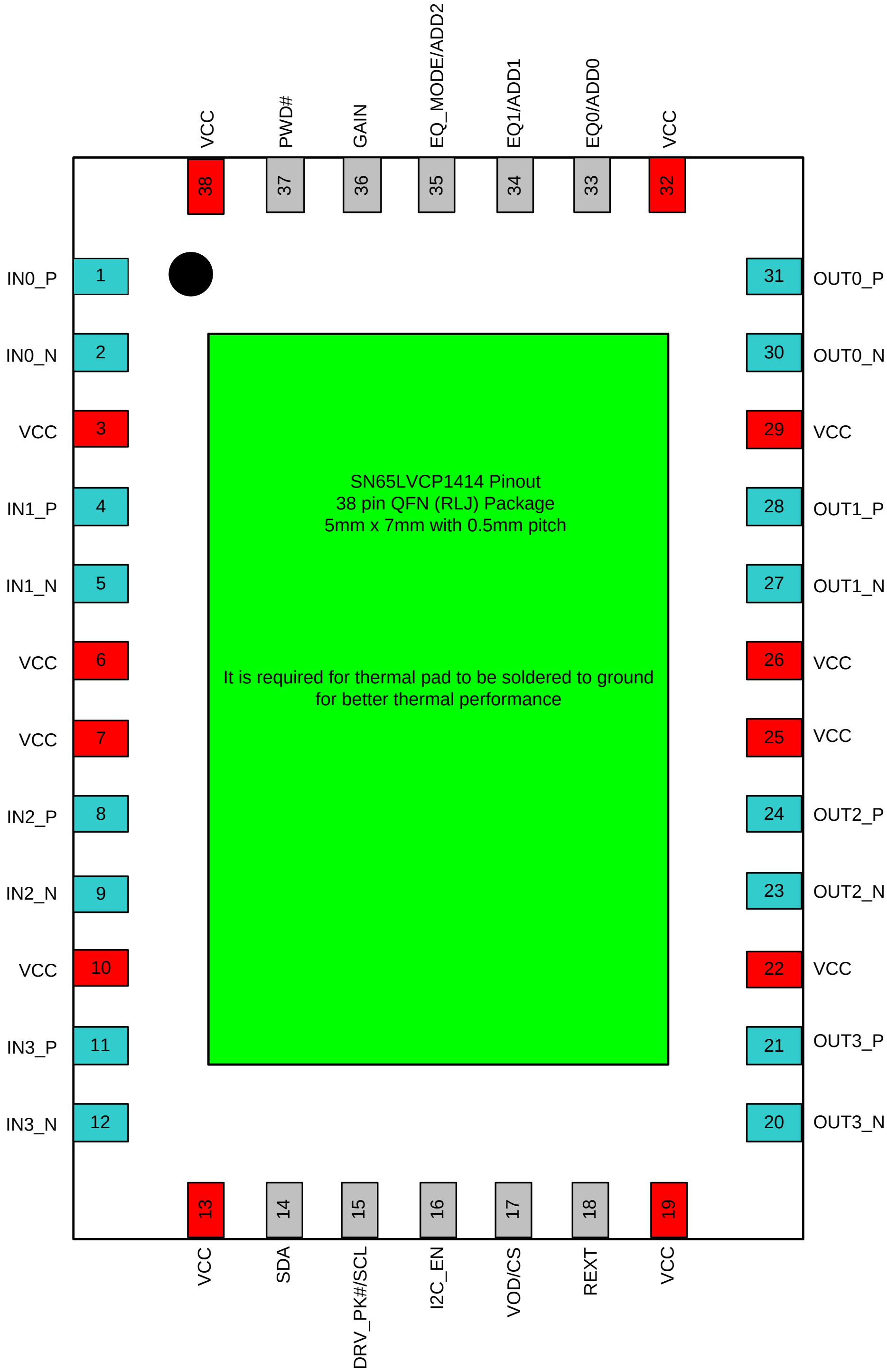


Figure 4. Package Drawing (Top View)

Pin Descriptions

PINS		DIRECTION TYPE SUPPLY	DESCRIPTION	
NAME	NO.			
DIFFERENTIAL HIGH-SPEED I/O				
IN0_P IN0_N	1 2	Input, (with 50 Ω termination to input common mode)	Differential input, lane 0	
IN1_P IN1_N	4 5	Input, (with 50 Ω termination to input common mode)	Differential input, lane 1	
IN2_P IN2_N	8 9	Input, (with 50 Ω termination to input common mode)	Differential input, lane 2	
IN3_P IN3_N	11 12	Input, (with 50 Ω termination to input common mode)	Differential input, lane 3	
OUT0_P OUT0_N	31 30	Output	Differential output, lane 0	
OUT1_P OUT1_N	28 27	Output	Differential output, lane 1	
OUT2_P OUT2_N	24 23	Output	Differential output, lane 2	
OUT3_P OUT3_N	21 20	Output	Differential output, lane 3	
CONTROL SIGNALS				
SDA	14	Input Output, Open drain	**GPIO mode** No action needed	**I^2C mode** I^2C data. Connect a 10kΩ pull-up resistor externally
DRV_PK#/SCL	15	Input. (with 200kΩ pull-up)	**GPIO mode** HIGH: disable Driver peaking LOW: enables Driver 6dB AC peaking	**I^2C mode** I^2C clock. Connect a 10kΩ pull-up resistor externally
I2C_EN	16	Input, (wtih 200kΩ pull-down) 2.5V/3.3V CMOS	Configures the device operation for I^2C or GPIO mode: HIGH: enables I^2C mode LOW: enables GPIO mode	
VOD/CS	17	Input, (with 200kΩ pull-down) 2.5V/3.3V CMOS	**GPIO mode** HIGH: set high VOD range LOW: set low VOD range	**I^2C mode** HIGH: acts as Chip Select LOW: disables I^2C interface
REXT	18	Input, Analog	External Bias Resistor: 1,200 Ω to GND	
EQ0/ADD0	33	Input, 2.5V/3.3V CMOS - 3-state	**GPIO mode** Working with EQ1 to determine input EQ gain.	**I^2C mode** ADD0 along with pins ADD1 and ADD2 comprise the three bits of I^2C slave address. ADD2:ADD1:ADD0:XXX

Pin Descriptions (continued)

<table>
<tr><th colspan="2">PINS</th><th rowspan="2">DIRECTION TYPE SUPPLY</th><th colspan="2" rowspan="2">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td rowspan="2">EQ1/ADD1</td><td rowspan="2">34</td><td rowspan="2">Input, 2.5V/3.3V CMOS - 3-state</td><td>GPIO mode
Working with EQ0 to determine input EQ gain steps of approximately 2dB
<table>
<tr><th>EQ1</th><th>EQ0</th><th>EQ GAIN</th></tr>
<tr><td>GND</td><td>GND</td><td>000</td></tr>
<tr><td>GND</td><td>HiZ</td><td>000</td></tr>
<tr><td>GND</td><td>VCC</td><td>001</td></tr>
<tr><td>HiZ</td><td>GND</td><td>010</td></tr>
<tr><td>HiZ</td><td>HiZ</td><td>011</td></tr>
<tr><td>HiZ</td><td>VCC</td><td>100</td></tr>
<tr><td>VCC</td><td>GND</td><td>101</td></tr>
<tr><td>VCC</td><td>HiZ</td><td>110</td></tr>
<tr><td>VCC</td><td>VCC</td><td>111</td></tr>
</table></td><td>I²C mode
ADD1 along with pins ADD0 and ADD2 comprise the three bits of I²C slave address
ADD2:ADD1:ADD0:XXX</td></tr>
<tr><td colspan="2">EQ1 and EQ0 works with AC_GAIN and DC_GAIN to determine final EQ gain as this:
<table>
<tr><th>EQ1/ EQ0</th><th>GAIN</th><th>DC GAIN (dB)</th><th>EQ GAIN (dB)</th></tr>
<tr><td>000 ~ 111</td><td>LOW</td><td>-6</td><td>1 ~ 9</td></tr>
<tr><td>000 ~ 111</td><td>HiZ</td><td>-6</td><td>7 ~ 17</td></tr>
<tr><td>000 ~ 111</td><td>HiGH</td><td>0</td><td>1 ~ 9</td></tr>
</table></td></tr>
<tr><td>EQ_MODE/ ADD2</td><td>35</td><td>Input, (with 200kΩ pull-down),
2.5V/3.3V CMOS</td><td>GPIO mode
HIGH: Trace mode
LOW: Cable mode</td><td>I²C mode
ADD2 along with pins ADD1 and ADD0 comprise the three bits of I²C slave address.
ADD2:ADD1:ADD0:XXX</td></tr>
<tr><td>GAIN</td><td>36</td><td>Input, 2.5V/3.3V CMOS - 3-state</td><td>GPIO mode
Work with EQ1/EQ0 to set total EQ Gain. See table above.</td><td>I²C mode
No action needed</td></tr>
<tr><td>PWD#</td><td>37</td><td>Input, (with 200kΩ pull-up),
2.5V/3.3V CMOS</td><td colspan="2">HIGH: Normal Operation
LOW: Power downs the device, inputs off and outputs disabled, resets I²C</td></tr>
<tr><td colspan="5">POWER SUPPLY</td></tr>
<tr><td>VCC</td><td>3, 6, 7, 10, 13, 19, 22, 25, 26, 29, 32, 38</td><td>Power</td><td colspan="2">Power supply 2.5V±5%, 3.3V±5%</td></tr>
<tr><td>GND Center Pad</td><td></td><td>Ground</td><td colspan="2">The ground center pad is the metal contact at the bottom of the package. This pad must be connected to the GND plane. At least 15 PCB vias are recommended to minimize inductance and provide a solid ground. Refer to the package drawing (RLJ-package) for the via placement.</td></tr>
</table>

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		VALUES	UNIT
V_{CC}	Supply voltage range[2]	–0.3 to 4	V
$V_{IN,DIFF}$	Differential voltage between INx_P and INx_N	±2.5	V
$V_{IN+, IN–}$	Voltage at Inx_P and fINx_N	–0.5 V to VCC+0.5	V
V_{IO}	Voltage on control IO pins	–0.5 V to VCC+0.5	V
I_{IN+} $I_{IN–}$	Continuous current at high speed differential data inputs (differential)	–25 to 25	mA
I_{OUT+} $I_{OUT–}$	Continuous current at high speed differential data outputs	–25 to 25	mA
ESD	Human Body Model[3] (All Pins)	2.0	kV
	Charged-Device Model[4] (All Pins)	500	V
Moisture sensitivity level		3	
Reflow temperature package soldering, 4 sec		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

Thermal Information

THERMAL METRIC[1]		SN65LVCP1414	UNITS
		RLJ (38 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance[2]	36.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	22.3	
θ_{JB}	Junction-to-board thermal resistance[4]	10.7	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.3	
ψ_{JB}	Junction-to-board characterization parameter[6]	10.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	1.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
dR	Operating data rate			14.2	Gbps
V_{CC}	Supply voltage	2.375	2.5	2.625	V
V_{CC}	Supply voltage	3.135	3.3	3.465	V
TC	Junction temperature	–10		125	°C
TB	Maximum board temperature			85	°C
CMOS DC SPECIFICATIONS					
V_{IH}	High-level input voltage	0.8×V_{CC}			V
V_{MID}	Mid-level input voltage	V_{CC}×0.4		V_{CC}×0.6	V
V_{IL}	Low-level input voltage	–0.5		0.2×V_{CC}	V
PSNR BG	Bandgap circuit PSNR	20			dB

Electrical Characteristics (VCC 2.5V ±5%)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation	VOD = LOW at 2.5V VCC with all 4 channels active		317	475	mW
PD_H	Device power dissipation	VOD = HIGH, at 2.5V VCC with all 4 channels active		485	675	mW
PD_{OFF}	Device power with all 4 channels switched off	Refer to I^2C section for device configuration. 2.5V VCC		10		mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

Electrical Characteristics (VCC 3.3V ±5%)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation	VOD = LOW at 3.3V VCC with all 4 channels active		450	625	mW
PD_H	Device power dissipation	VOD = HIGH, at 3.3V VCC with all 4 channels active		697	925	mW
PD_{OFF}	Device power with all 4 channels switched off	Refer to I^2C section for device configuration, 3.3V VCC		10		mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

Electrical Characteristics (VCC 2.5V ±5%, 3.3V ±5%)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CMOS DC SPECIFICATIONS						
I_{IH}	High level input current	VIN = 0.9 × V_{CC}	-40	17	40	µA
I_{IL}	Low level input current	VIN = 0.1 × V_{CC}	-40	17	40	µA
CML INPUTS (IN[3:0]_P, IN[3:0]_N)						
r_{IN}	Differential input resistance	INx_P to INx_N		100		Ω
V_{IN}	Input linear dynamic range	Gain = 0.5		1200		mV_{pp}
V_{ICM}	Input common mode voltage	Internally biased		V_{CC}–0.8		V
SCD11	Input differential to common mode conversion	100MHz to 7.1GHz		–20		dB
SDD11	Differential input return loss	100MHz to 7.1GHz		–15		dB

(1) All typical values are at 25°C and with 2.5V and 3.3V supply unless otherwise noted.

Electrical Characteristics (VCC 2.5V ±5%, 3.3V ±5%) (continued)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CML OUTPUTS (OUT[3:0]_P, OUT[3:0]_N)						
V_{OD}	Output linear dynamic range	R_L = 100 Ω, V_{OD} = HIGH		1200		mV_{pp}
		R_L = 100 Ω, V_{OD} = LOW		600		mV_{pp}
V_{OS}	Output offset voltage	R_L = 100 Ω, 0 V applied at inputs		10		mV_{pp}
V_{OCM}	Output common mode voltage	See Figure 5		V_{CC}-0.4		V
$V_{CM,RIP}$	Common mode output ripple	K28.5 pattern at 14.2Gbps on all 4 channels, No interconnect loss, VOD = HIGH		10	20	mV_{RMS}
$V_{OD,RIP}$	Differential path output ripple	K28.5 pattern at 14.2Gbps on all channels, No interconnect loss, VIN = 1200mVpp.			20	mV_{pp}
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			±10		mV
t_R	Rise time(2)	Input signal with 30ps rise time, 20% to 80%, See Figure 7		31		ps
t_F	Fall time(2)	Input signal with 30ps fall time, 20% to 80%, See Figure 7		32		ps
SDD22	Differential output return loss	100MHz to 7.1GHz		–15		dB
SCC22	Common-mode output return loss	100MHz to 7.1GHz		–5		dB
t_{PLH}	Low-to-high propagation delay	See Figure 6		65		ps
t_{PHL}	High-to-low propagation delay			65		ps
$t_{SK(O)}$	Inter-Pair (lane to lane) output skew(3)	All outputs terminated with 100 Ω, See Figure 8		8		ps
$t_{SK(PP)}$	Part-to-part skew(4)	All outputs terminated with 100 Ω			50	ps
r_{OT}	Single ended output resistance	Single ended on-chip termination to VCC, Outputs will be AC coupled		50		Ω
r_{OM}	Output termination mismatch at 1MHz	$\Delta rom = 2 \times \frac{rp - rn}{rp + rn} \times 100$		5		%
Ch_{iso}	Channel-to-channel isolation	Frequency at 7.1GHz	35	45		dB
OUT_{NOISE}	Output referred noise(5)	10MHz to 7.1GHz, No other noise source present, VOD = LOW		400		µVRMS
		10MHz to 7.1GHz, No other noise source present, VOD = HIGH		500		µVRMS
EQUALIZATION						
EQ_{Gain}	At 7.1GHz input signal	Equalization Gain, EQ = MAX	15	17		dB
Vpre	Output pre-cursor pre-emphasis	Input signal with 3.75 pre-cursor and measure it on the output signal, Refer Figure 9. Vpre = 20log(V3/V2)		3.75		dB
Vpst	Output post-cursor pre-emphasis	Input signal with 12dB post-cursor and measure it on the output signal, Refer Figure 9, Vpst = 20log(V1/V2)		12		dB
DJ1	Residual deterministic jitter at 10.3125 Gbps	Transmit Side application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel -> 0”, See Figure 11		0.016		UIp-p
DJ2	Residual deterministic jitter at 10.3125 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel -> 12” (9dB loss at 5GHz), See Figure 10		0.11		UIp-p
DJ3	Residual deterministic jitter at 14.2 Gbps	Transmit Side Application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel -> 0”, See Figure 11		0.041		UIp-p
DJ4	Residual deterministic jitter at 14.2 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel -> 8” (9dB loss at 7GHz), See Figure 10		0.13		UIp-p

(2) Rise and Fall measurements include board and channel effects of the test environment, refer to Figure 10 and Figure 11.
(3) $t_{SK(O)}$ is the magnitude of the time difference between the channels.
(4) $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(5) All noise sources added.

Parameter Measurement Information

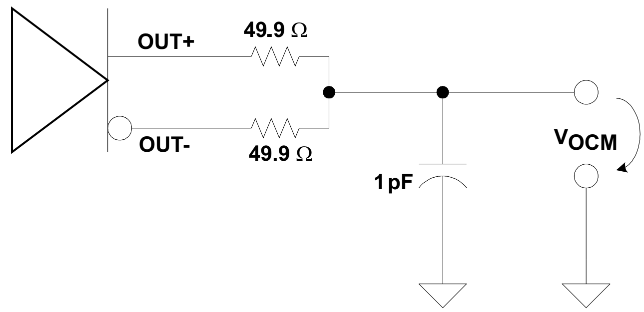


Figure 5. Common Mode Output Voltage Test Circuit

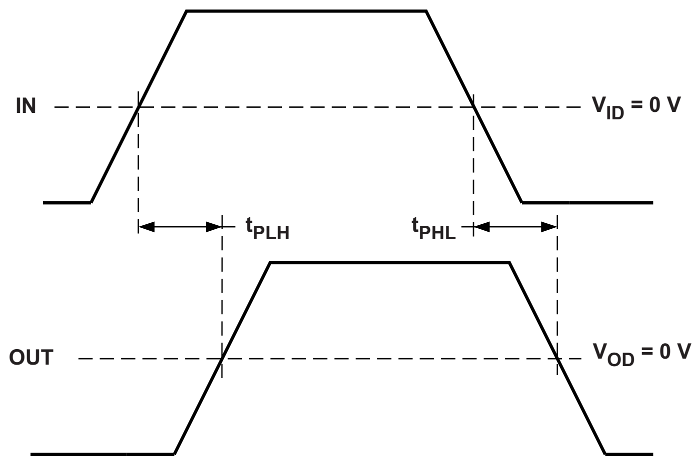


Figure 6. Propagation Delay Input to Output

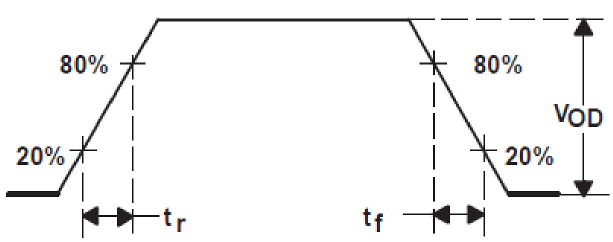


Figure 7. Output Rise and Fall Times

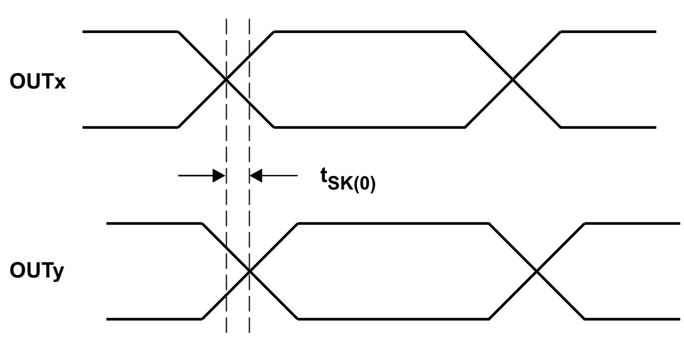


Figure 8. Output Inter-Pair Skew

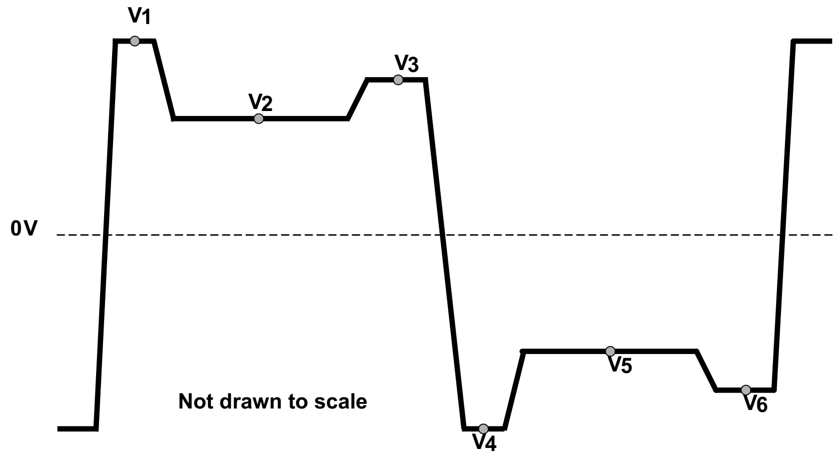


Figure 9. Vpre and Vpost (test pattern is 1111111100000000 (8-1s, 8-0s))

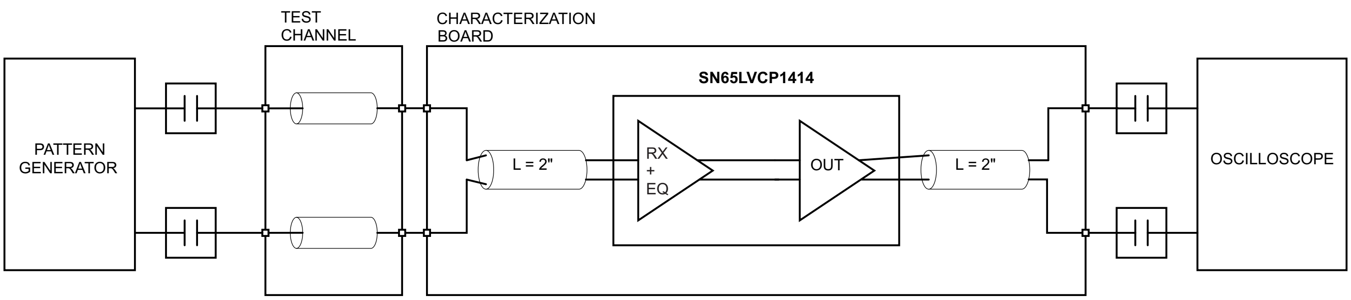


Figure 10. Receive Side Performance Test Circuit

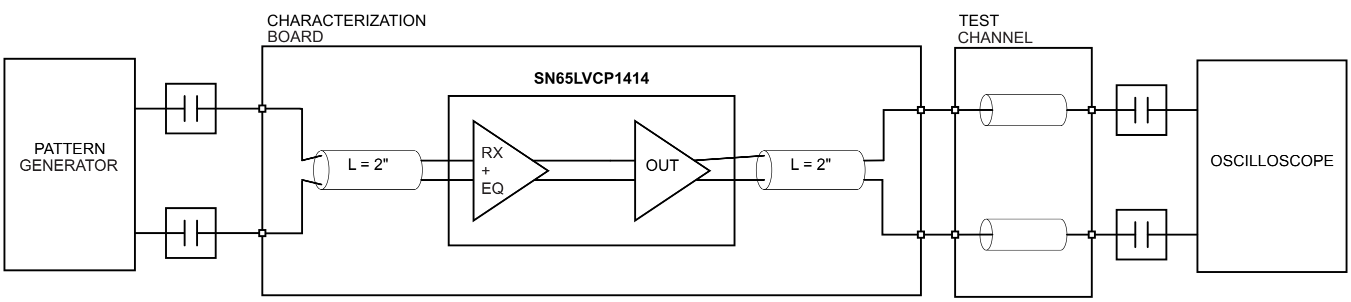


Figure 11. Transmit Side Performance Test Circuit

Equivalent Input and Output Schematic Diagrams

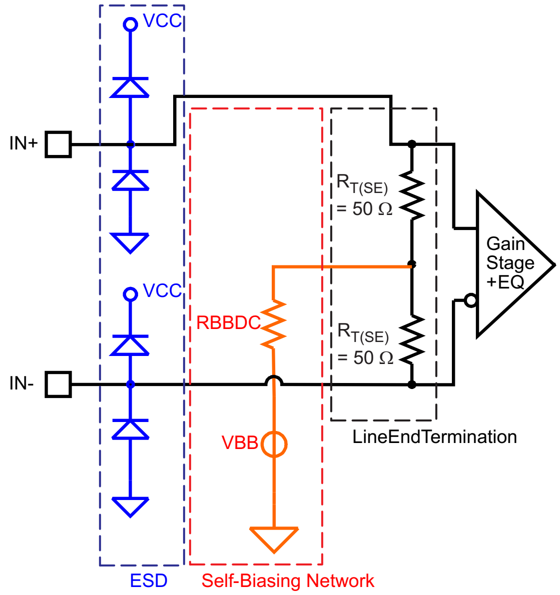


Figure 12. Equivalent Input Circuit Design

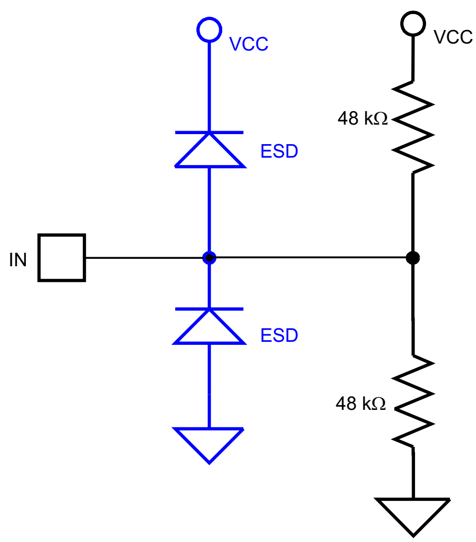


Figure 13. 3-Level Input Biasing Network

Typical Characteristics

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

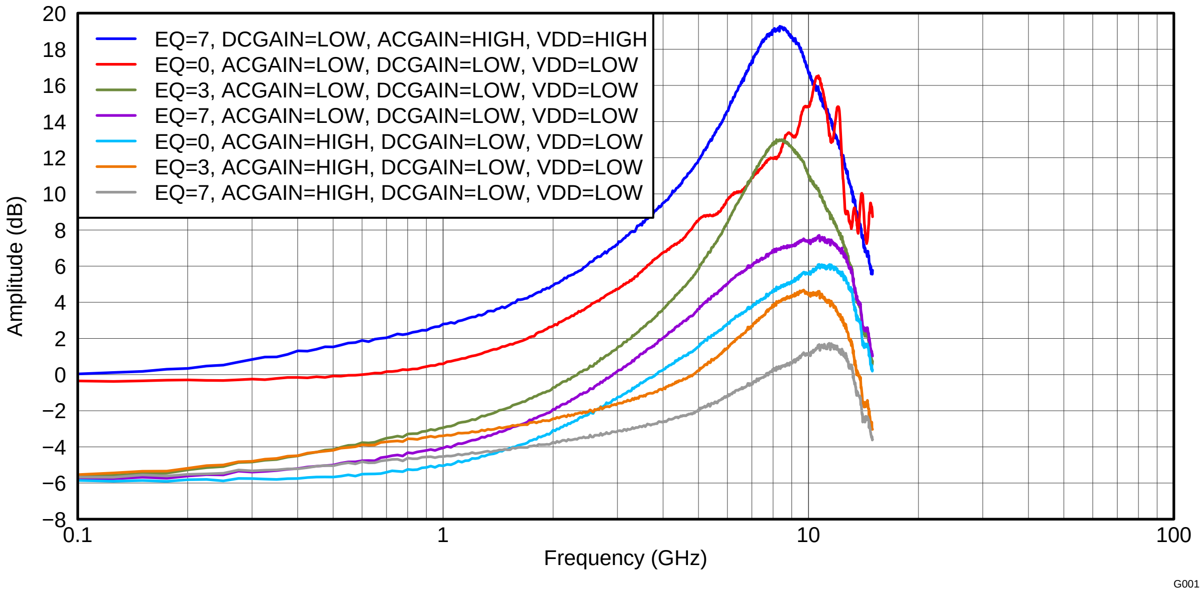


Figure 14. Typical EQ Gain Profile Curve

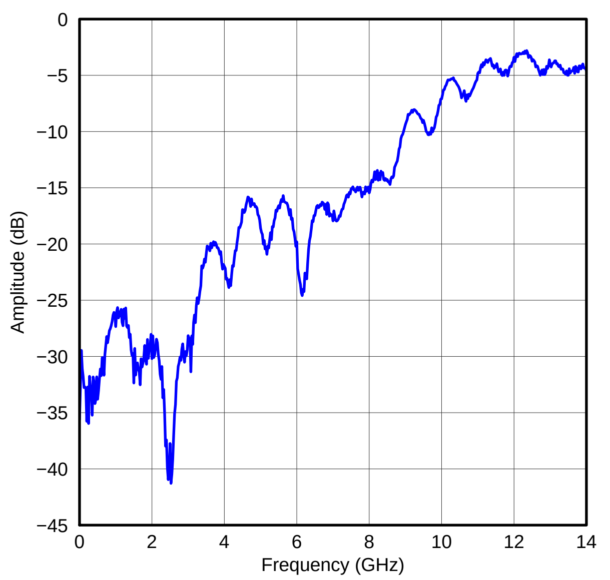


Figure 15. Differential Input Return Loss

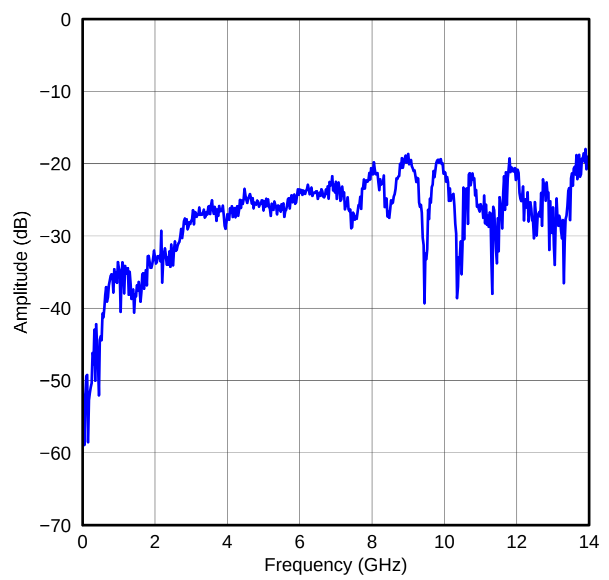


Figure 16. Differential to Common Mode Conversion

Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

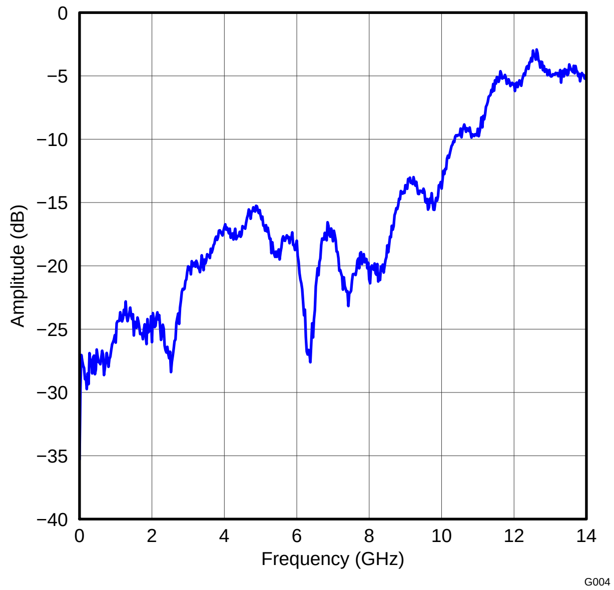


Figure 17. Differential Output Return Loss

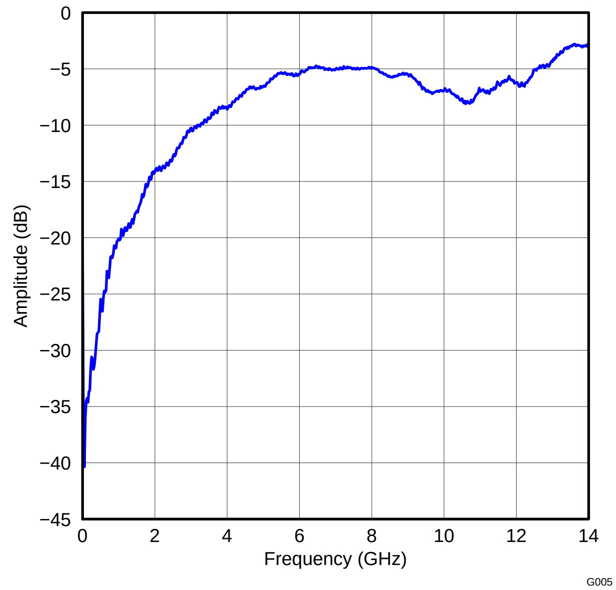
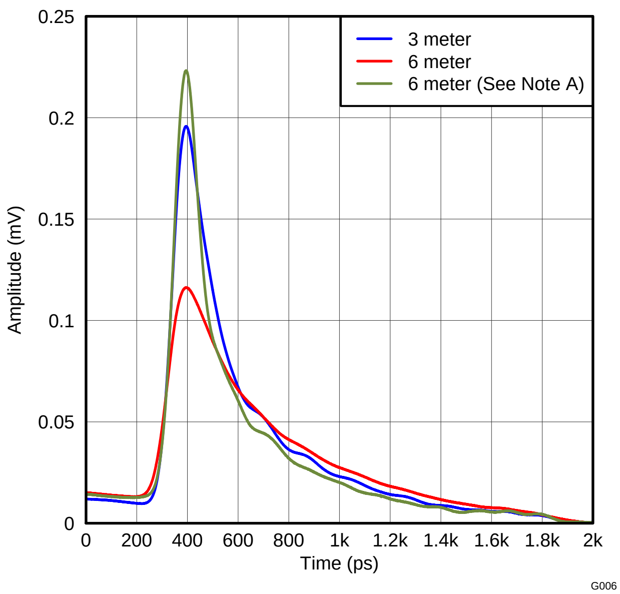
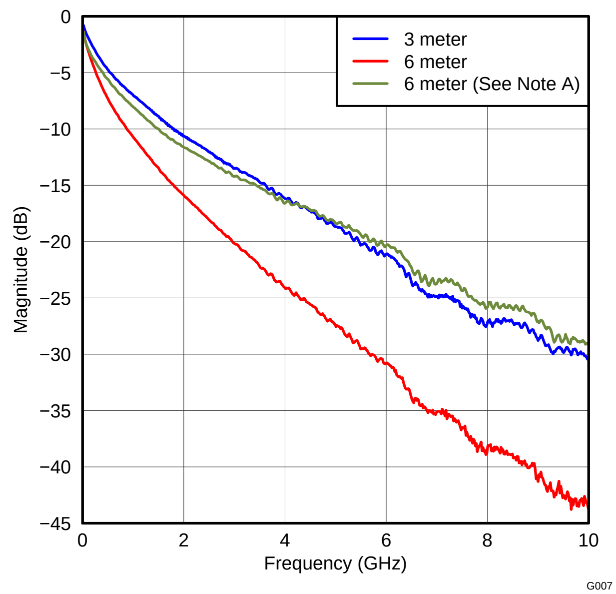


Figure 18. Common Mode Output Return Loss



A. With SN65LVCP1414 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 19. Cable Mode – Symbol Response

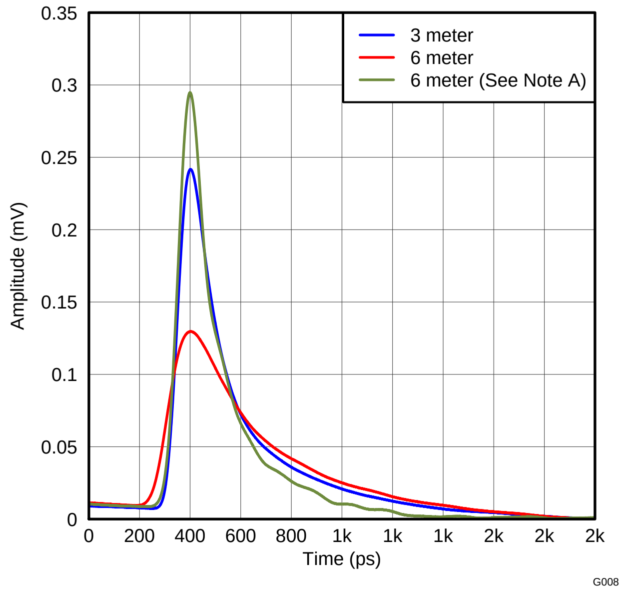


A. With SN65LVCP1414 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 20. Cable Mode – Frequency Domain

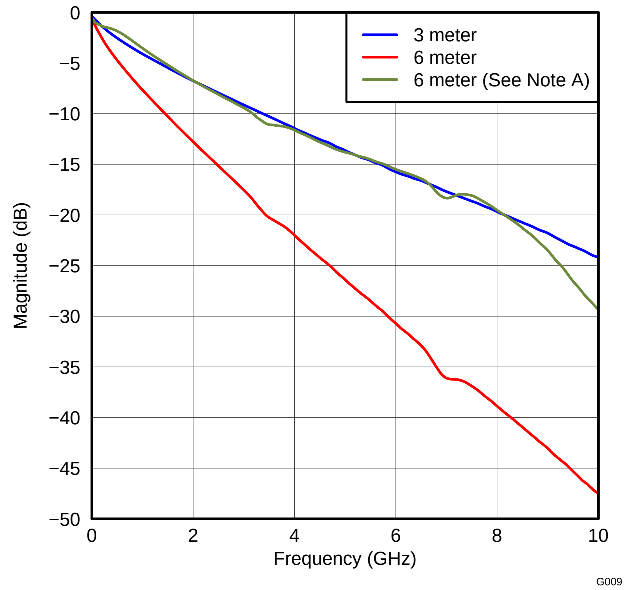
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).



A. With SN65LVCP1414 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 21. Trace Mode – Symbol Response



A. With SN65LVCP1414 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 22. Trace Mode - Frequency Domain

Table 1. Control Settings Descriptions

MODE	DCGAIN	ACGAIN<1:0>	EQ<2:0>	DC GAIN (dB)	EQ GAIN (dB)	APPLICATION
0	0	0	000 to 111	–6	1 to 9	Short Input Trace; Large Input Swing
0	0	11	000 to 111	–6	7 to 17	Long Input Trace; Large Input Swing
0	1	1	000 to 111	0	1 to 9	Short Input Trace; Small Input Swing
0	1	11	000 to 111	0	2 to 10	Short Input Trace; Small Input Swing
1	0	0	000 to 111	–6	1 to 9	Short Input Cable; Large Input Swing
1	0	11	000 to 111	–6	7 to 17	Long Input Cable; Large Input Swing
1	1	1	000 to 111	0	1 to 9	Short Input Cable; Small Input Swing
1	1	11	000 to 111	0	2 to 10	Short Input Cable; Small Input Swing

Table 2. Control Settings Descriptions

GAIN	DC GAIN	ACGAIN<1:0>
Low	0	00
HighZ	0	11
High	1	01

Two-Wire Serial Interface and Control Logic

The SN65LVCP1414 uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. The SDA and SCK pins require external 10kΩ pull-ups to VCC.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The SN65LVCP1414 is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0000ADD[2:0]) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD[2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7 bit slave address is 0000000.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the SN65LVCP1414 is I^2C compatible. The typical timing is shown in Figure 9 and a complete data transfer is shown in Figure 10. Parameters for Figure 9 are defined in Table 3.

Bus Idle: Both SDA and SCL lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

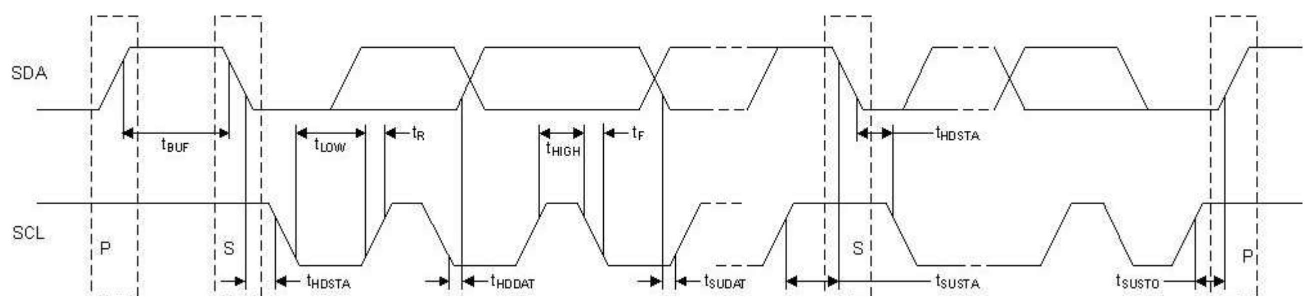


Figure 23. Two-Wire Serial Interface Timing Diagram

Table 3. Two-Wire Serial Interface Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		μs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		μs
t_{LOW}	Low period of the SCL clock	1.3		μs
t_{HIGH}	High period of the SCL clock	0.6		μs
t_{SUSTA}	Setup time for a repeated START condition	0.6		μs
t_{HDDAT}	Data HOLD time	0		μs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		μs

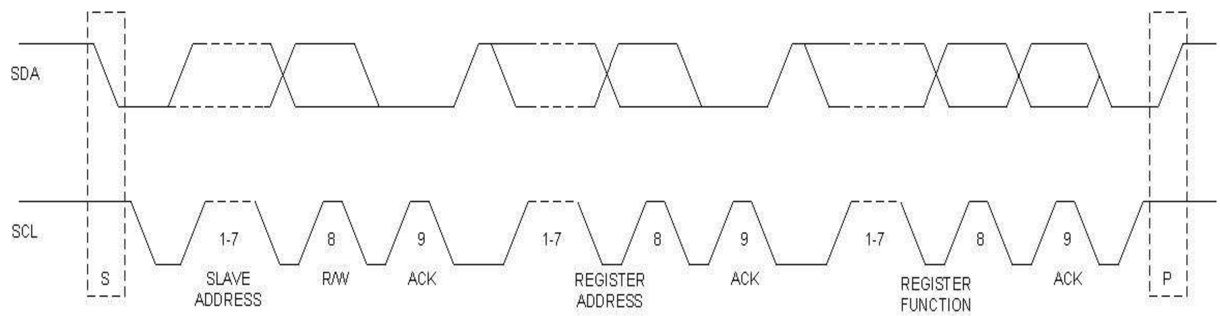


Figure 24. Two-Wire Serial Interface Data Transfer

Register Mapping

The register mapping for read/write register addresses 0 (0x00) through 22 (0x18) are shown in Table 4. Table 5 describes the circuit functionality based on the register settings.

Table 4. SN65LVCP1414 Register Mapping Information

Register 0x00 (General Device Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SW_GPIO	PWRDOWN	SYNC_01	SYNC_ 23	SYNC_ALL	EQ_MODE		RSVD
Register 0x01 (Channel Enable) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
				LN_EN_CH3	LN_EN_CH2	LN_EN_CH1	LN_EN_CH0
Register 0x02 (Channel 0 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x03 (Channel 0 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x05 (Channel 1 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x06 (Channel 1 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x08 (Channel 2 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x09 (Channel 2 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x0B (Channel 3 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x0C (Channel 3 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x0F Read Only							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Register 0x11 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	RSVD						
Register 0x12 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD							

Table 5. SN65LVCP1414 Register Description

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x00	7	SW_GPIO	Switching logic is controlled by GPIO or I^2C: 0 = I^2C control 1 = GPIO control	00000000
	6	PWRDOWN	Power down the device: 0 = Normal operation 1 = Powerdown	
	5	SYNC_01	All settings from channel 1 will be used for channel 0 and 1: 0 = Channel 0 tracking channel 1 settings 1 = No tracking tracking	
	4	SYNC_23	All settings from channel 2 will be used for channel 2 and 3: 0 = Channel 3 tracking channel 2 settings 1 = No channel tracking	
	3	SYNC_ALL	All settings from channel 1 will be used on all channels: 0 = All channels tracking channel 1 1 = No channel tracking Overwrites SYNC_01 and SYNC_23	
	2	EQ_MD	Set EQ mode: 0 = Cable mode 1 = Trace mode	
	1			
	0	RSVD	For TI use only	
0x01	7			00000000
	6			
	5			
	4			
	3	LN_EN_CH3	Channel 3 enable: 0 = Enable 1 = Disable	
	2	LN_EN_CH2	Channel 2 enable: 0 = Enable 1 = Disable	
	1	LN_EN_CH1	Channel 1 enable: 0 = Enable 1 = Disable	
	0	LN_EN_CH0	Channel 0 enable: 0 = Enable 1 = Disable	
0x02 0x05 0x08 0x0B	7	RSVD		00000000
	6	EQ2	Equalizer adjustment setting: 000 = Minimum equalization setting 111 = Maximum equalization setting	
	5	EQ1		
	4	EQ0		
	3	VOD_CTRL	Channel [x] VOD control: 0 = Low VOD range 1 = High VOD range	
	2	DC_GAIN_CTRL	Channel [x] EQ DC gain: 0 = Set EQ DC gain to 0.5x 1 = Set EQ DC gain to 1x	
	1	AC_GAIN_CTRL1	AC Gain Control: 00 = Low 01 = HiZ 11 = High	
	0	AC_GAIN_CTRL0		

Table 5. SN65LVCP1414 Register Description (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x03 0x06 0x09 0x0C	7			00000000
	6			
	5			
	4			
	3			
	2	DRV_PEAK	Channel [x] driver peaking: 0 = Disables driver Peaking 1 = Enables driver 6db AC Peaking	
	1	EQ_EN	Channel [x] EQ stage enable: 0 = Enable 1 = Disable	
	0	DRV_EN	Channel [x] driver stage enable: 0 = Enable 1 = Disable	
0x0F	7	RSVD	For TI use only	00110000
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	
0x11	7			00000000
	6	RSVD	For TI use only	
	5			
	4			
	3			
	2			
	1			
	0			
0x12	7	RSVD	For TI use only	00000000
	6			
	5			
	4			
	3			
	2			
	1			
	0			

REVISION HISTORY

Changes from Original (August 2012) to Revision A **Page**

- Changed OUT2_P pin number from 23 to 24 5
- Changed OUT2_N pin number from 24 to 23 5
- Changed OUT3_P pin number from 20 to 21 5
- Changed OUT3_N pin number from 21 to 20 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVCP1414RLJR	ACTIVE	WQFN	RLJ	38	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP 1414	Samples
SN65LVCP1414RLJT	ACTIVE	WQFN	RLJ	38	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP 1414	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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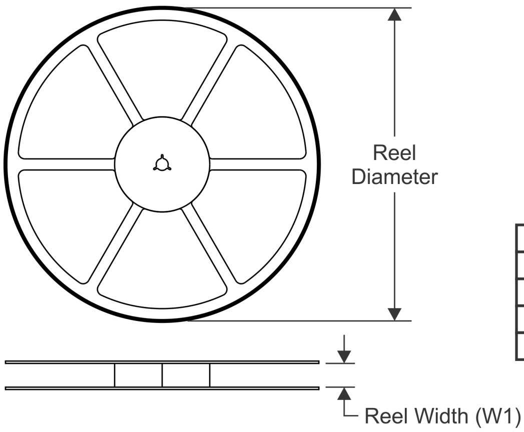
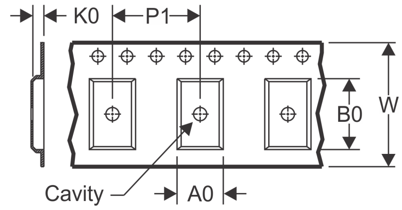
TAPE AND REEL INFORMATION

REEL DIMENSIONS

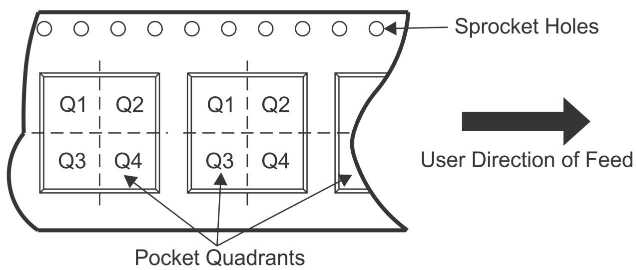


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

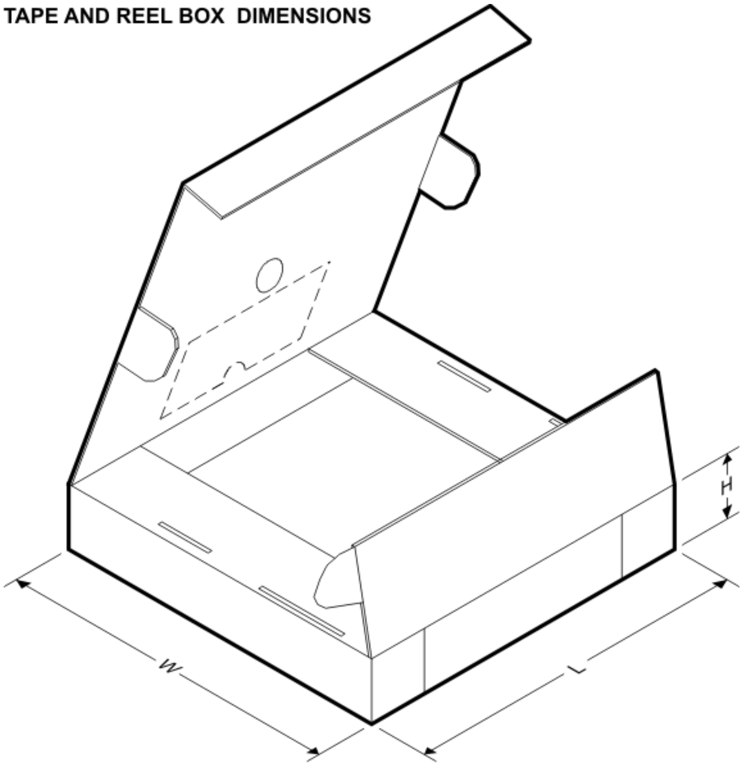
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP1414RLJR	WQFN	RLJ	38	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
SN65LVCP1414RLJT	WQFN	RLJ	38	250	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

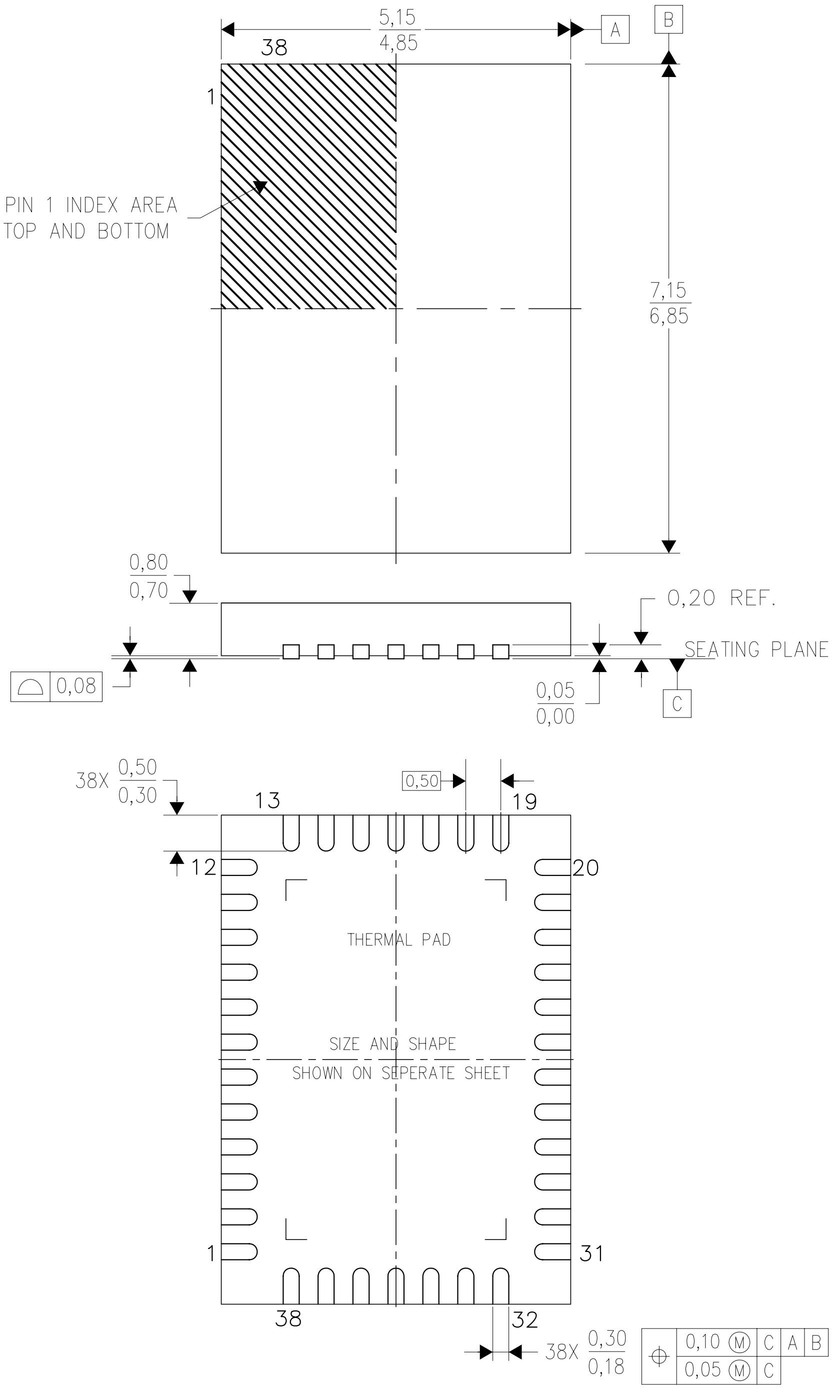
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP1414RLJR	WQFN	RLJ	38	3000	367.0	367.0	38.0
SN65LVCP1414RLJT	WQFN	RLJ	38	250	367.0	367.0	38.0

RLJ (R–PWQFN–N38) PLASTIC QUAD FLATPACK NO–LEAD



4212454/A 01/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

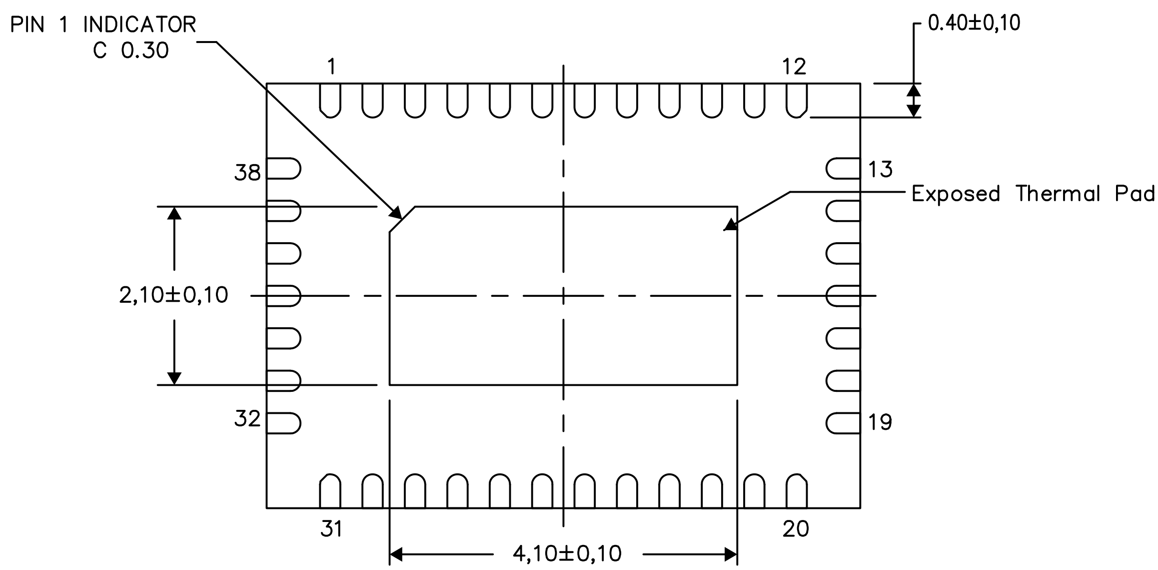
RLJ (R-PVQFN-N38) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



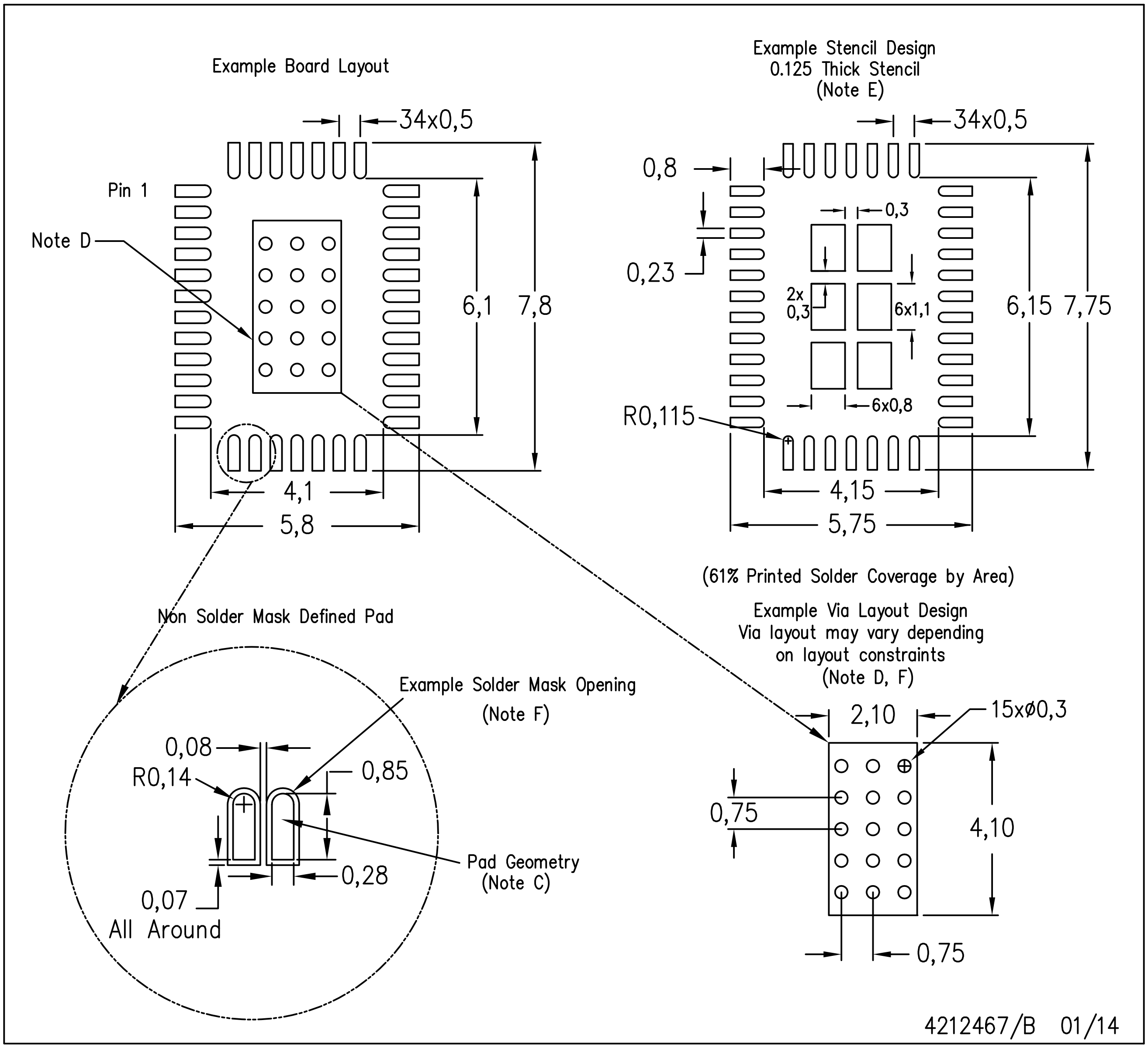
Bottom View

Exposed Thermal Pad Dimensions

4212466/B 01/14

NOTE: All linear dimensions are in millimeters

RLJ (R–PVQFN–N38) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122