TCA9539-Q1 具有中断输出、复位引脚和配置寄存器的低压 16 位 I²C 和系统管理总线 (SMBus) 低功耗输入输出 (I/O) 扩展器

1 特性

- 符合汽车类应用的 应用
- I²C 至并行端口扩展器
- 开漏电路低电平有效中断输出
- 低电平有效复位输入
- 5V 耐压输入和输出端口
- 兼容多数微控制器
- 400kHz 快速 I²C 总线
- 极性反转寄存器
- 内部上电复位
- 加电时无毛刺脉冲
- 通过两个硬件地址引脚寻址，以便使用多达 4 个器件
- 锁存输出，用于直接驱动 LED
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 2000V 人体模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 汽车信息娱乐系统、高级驾驶员辅助系统 (ADAS)、汽车车身电子装置、混合动力汽车 (HEV)、电动车 (EV) 和动力传动
- 工业自动化、工厂自动化、楼宇自动化、测试与测量、电子销售点终端 (EPOS)
- I²C GPIO 扩展

3 说明

TCA9539-Q1 是一款 24 引脚器件，可为双线制双向 I²C 总线（或 SMBus 协议）提供 16 位通用并行输入和输出 (I/O) 扩展。该器件的工作电源电压 (V_{CC}) 范围为 1.65V 至 3.6V，并且支持 100kHz（I²C 标准模式）和 400kHz（I²C 快速模式）两种时钟频率。当开关、传感器、按钮、LED、风扇以及其他相似器件需要额外的 I/O 时，I/O 扩展器（如 TCA9539-Q1）可提供简单解决方案。

当 端口 状态发生变化时，TCA9539-Q1 可在 $\overline{INT}$ 引脚上生成中断。硬件可选地址引脚 A0 和 A1 最多允许四个 TCA9539-Q1 器件位于同一 I²C 总线上。该器件可通过电源循环供电以生成上电复位，从而复位到默认状态。此外，TCA9539-Q1 还具有一个硬件 $\overline{RESET}$ 引脚，可用于将器件复位为默认状态。

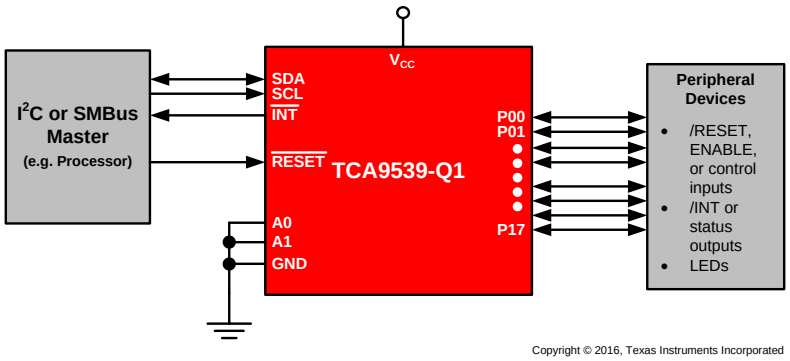
TCA9539-Q1 I²C I/O 扩展器符合汽车应用的 要求。

器件信息(1)

器件型号	封装类型	封装尺寸（标称值）
TCA9539-Q1	TSSOP (24)	7.80mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化方框图



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4 修订历史记录

Changes from Revision B (April 2016) to Revision C **Page**

- Changed the appearance of the PW pinout image 3
- Removed (5 V) from the V_{CC} label in Figure 31 26

Changes from Revision A (September 2015) to Revision B **Page**

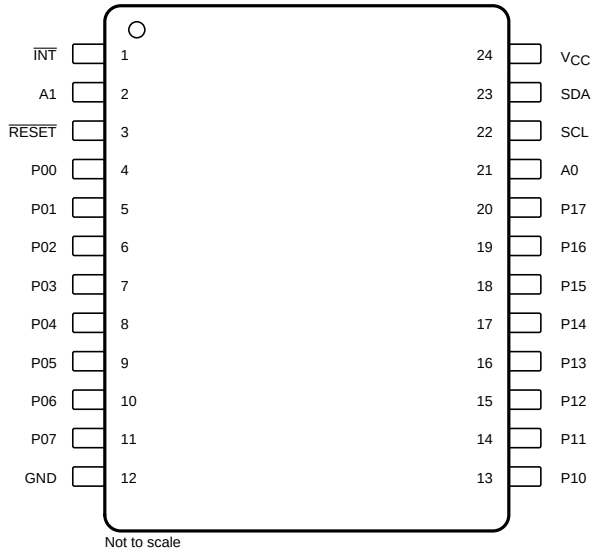
- 已将器件状态由*"产品预览"*改为*"量产数据"* 1

Changes from Original (January 2014) to Revision A **Page**

- 已添加 ESD 额定值表，特性 说明 "部分、器件功能模式、"应用和实施"部分、"电源相关建议"部分、"布局"部分、"器件和文档支持"部分以及"机械、封装和可订购信息"部分。 1

5 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{INT}$	O	Interrupt open-drain output. Connect to V_{CC} through a pull-up resistor
2	A1	I	Address input. Connect directly to V_{CC} or ground
3	$\overline{RESET}$	I	Active-low reset input. Connect to V_{CC} through a pull-up resistor if no active connection is used
4	P00	I/O	P-port input-output. Push-pull design structure. At power-on, P00 is configured as an input
5	P01	I/O	P-port input-output. Push-pull design structure. At power-on, P01 is configured as an input
6	P02	I/O	P-port input-output. Push-pull design structure. At power-on, P02 is configured as an input
7	P03	I/O	P-port input-output. Push-pull design structure. At power-on, P03 is configured as an input
8	P04	I/O	P-port input-output. Push-pull design structure. At power-on, P04 is configured as an input
9	P05	I/O	P-port input-output. Push-pull design structure. At power-on, P05 is configured as an input
10	P06	I/O	P-port input-output. Push-pull design structure. At power-on, P06 is configured as an input
11	P07	I/O	P-port input-output. Push-pull design structure. At power-on, P07 is configured as an input
12	GND	—	Ground
13	P10	I/O	P-port input-output. Push-pull design structure. At power-on, P10 is configured as an input
14	P11	I/O	P-port input-output. Push-pull design structure. At power-on, P11 is configured as an input
15	P12	I/O	P-port input-output. Push-pull design structure. At power-on, P12 is configured as an input
16	P13	I/O	P-port input-output. Push-pull design structure. At power-on, P13 is configured as an input
17	P14	I/O	P-port input-output. Push-pull design structure. At power-on, P14 is configured as an input
18	P15	I/O	P-port input-output. Push-pull design structure. At power-on, P15 is configured as an input
19	P16	I/O	P-port input-output. Push-pull design structure. At power-on, P16 is configured as an input
20	P17	I/O	P-port input-output. Push-pull design structure. At power-on, P17 is configured as an input
21	A0	I	Address input. Connect directly to V_{CC} or ground
22	SCL	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
23	SDA	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor
24	V_{CC}	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	3.6	V
V_I	Input voltage (2)		–0.5	6	V
V_O	Output voltage (2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
$T_{j(MAX)}$	Maximum junction temperature			135	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	3.6	V
$V_{I/O}$	I/O ports voltage	SCL, SDA, A0, A1, $\overline{RESET}$, $\overline{INT}$ (1)		–0.5	5.5	V
		For P00–P07, P10–P17 configured as outputs		–0.5	3.6	V
		For P00–P07, P10–P17 configured as inputs (1)		–0.5	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, A0, A1, $\overline{RESET}$, P07–P00, P10–P17		0.7 × V_{CC}		V
V_{IL}	Low-level input voltage	SCL, SDA, A0, A1, $\overline{RESET}$, P07–P00, P10–P17			0.3 × V_{CC}	V
I_{OH}	High-level output current	P00–P07, P10–P17			–10	mA
I_{OL} (2)	Low-level output current	P00–P07, P10–P17	$T_j \le 65°C$		25	mA
			$T_j = 85°C$		18	
			$T_j = 105°C$		9	
			$T_j = 125°C$		4.5	
			$T_j = 135°C$		3.5	
I_{OL} (2)	Low-level output current	$\overline{INT}$, SDA	$T_j \le 85°C$		6	mA
			$T_j = 105°C$		3	
			$T_j = 125°C$		1.8	
			$T_j = 135°C$		1.5	
T_A	Operating free-air temperature			–40	125	°C

(1) For voltages applied above V_{CC}, an increase in I_{CC} results.
(2) The values shown apply to specific junction temperatures. See the *Calculating Junction Temperature and Power Dissipation* section on how to calculate the junction temperature.

6.4 Thermal Information

THERMAL METRIC (1)		TCA9539-Q1 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP (1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA		1.65 V to 3.6 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	$V_I = V_{CC}$ or GND		1.65 V to 3.6 V		1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	$V_I = V_{CC}$ or GND		1.65 V to 3.6 V	0.75	1		V
V_{OH}	P-port high-level output voltage (2)	I_{OH} = –8 mA		1.65 V	1.2			V
				2.3 V	1.8			
				3 V	2.6			
				3.6 V	3.3			
		I_{OH} = –10 mA		1.65 V	1			
				2.3 V	1.7			
				3 V	2.5			
				3.6 V	3.2			
I_{OL}	SDA	V_{OL} = 0.4 V		1.65 V to 3.6 V	3			mA
	P port (3)	V_{OL} = 0.5 V			8			
		V_{OL} = 0.7 V			10			
	$\overline{INT}$	V_{OL} = 0.4 V			3			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND		1.65 V to 3.6 V			±1	µA
	A0, A1, $\overline{RESET}$						±1	
I_{IH}	P port	$V_I = V_{CC}$		1.65 V to 3.6 V			1	µA
I_{IL}	P port	V_I = GND		1.65 V to 3.6 V			–1	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 400-kHz, no load		3.6 V		10	30	µA
				2.7 V		5	19	
				1.95 V		4	11	
	Standby mode	I_O = 0, I/O = inputs, f_{SCL} = 0-kHz, no load	$V_I = V_{CC}$	3.6 V		1.1	5	
				2.7 V		1	4.5	
				1.95 V		0.4	3.5	
			V_I = GND	3.6 V		1.1	13	
				2.7 V		1	9.5	
				1.95 V		0.4	6.5	
C_i	SCL	$V_I = V_{CC}$ or GND		1.65 V to 3.6 V		3	8	pF

(1) All typical values are at nominal supply voltage (1.8 V, 2.5 V, or 3.3 V, V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to the maximum allowed I_{OL}, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA at $T_j \le 85°C$. See the *Recommended Operating Conditions* table for more information.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10) for $T_j \le 85°C$. See the *Recommended Operating Conditions* table for more information.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP (1)	MAX	UNIT
C_{io}	SDA	V_{IO} = V_{CC} or GND	1.65 V to 3.6 V		3	9.5	pF
	P port				3.7	9.5	

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 15)

			MIN	MAX	UNIT
I²C BUS—STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF

			MIN	MAX	UNIT
I²C BUS—FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{CC} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	pF

6.7 $\overline{\text{RESET}}$ Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 18)

		MIN	MAX	UNIT
t_W	Reset pulse duration	6		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset; For V_{CC} = 2.3 V – 3.6 V	400		ns
	Time to reset; For V_{CC} = 1.65 V – 2.3 V	550		ns

6.8 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted) (see Figure 16 and Figure 17)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid; For V_{CC} = 2.3 V – 3.6 V	SCL	P port		200	ns
	Output data valid; For V_{CC} = 1.65 V – 2.3 V				300	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

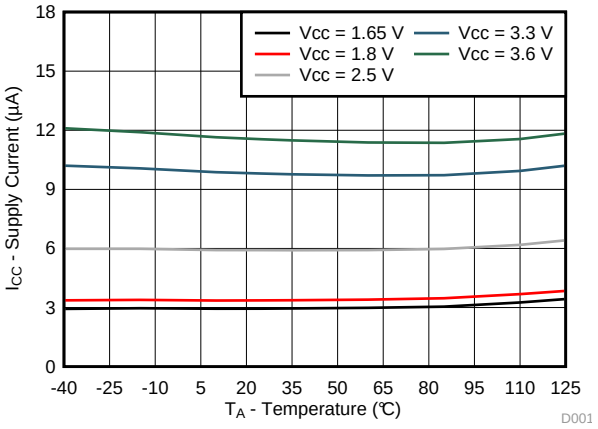


Figure 1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

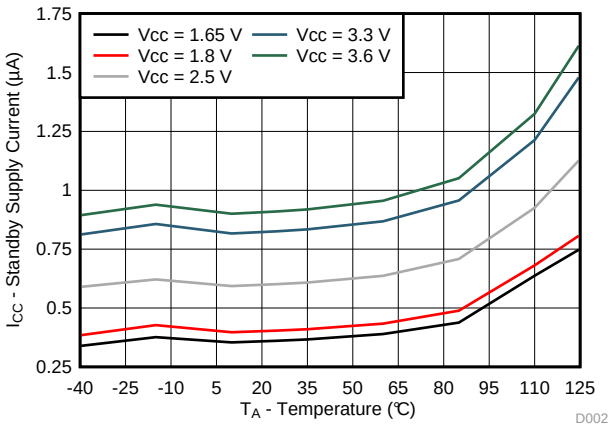


Figure 2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

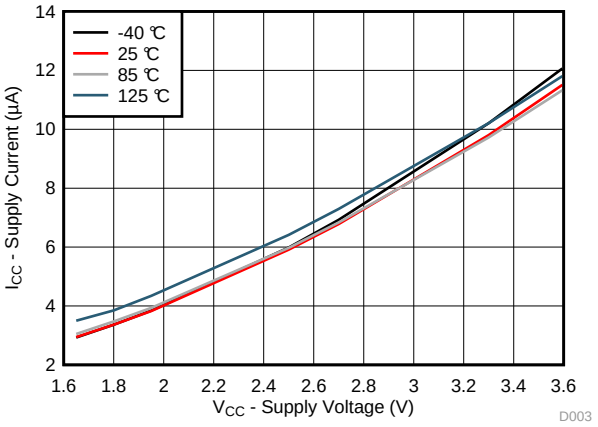


Figure 3. Supply Current vs Supply Voltage for Different Temperature (T_A)

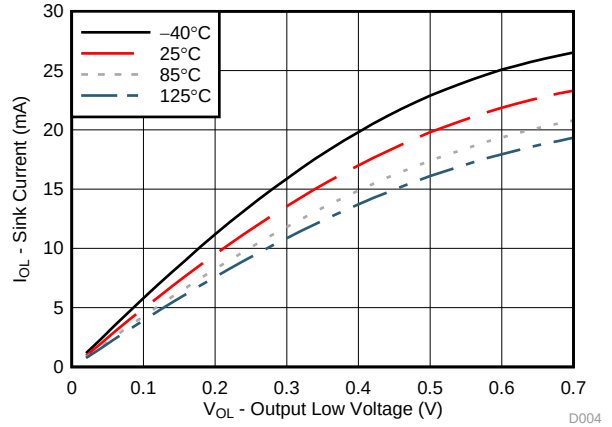


Figure 4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

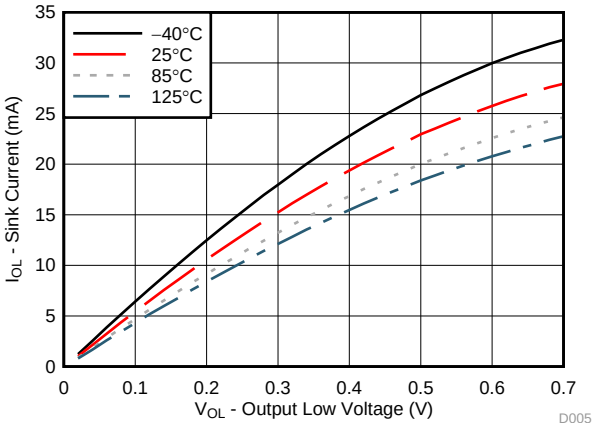


Figure 5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

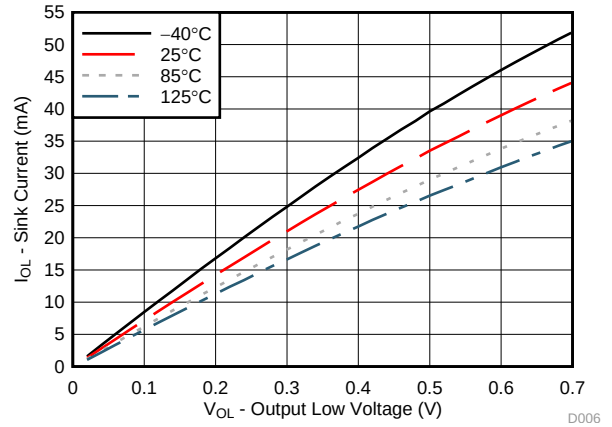


Figure 6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

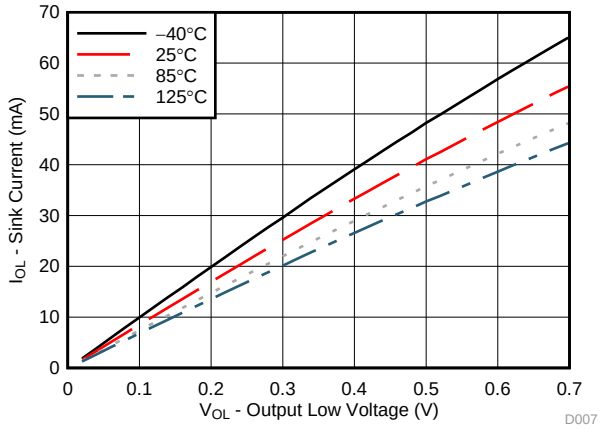


Figure 7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

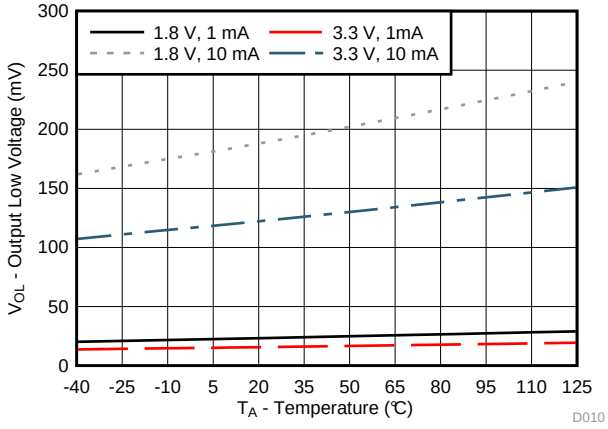


Figure 8. I/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

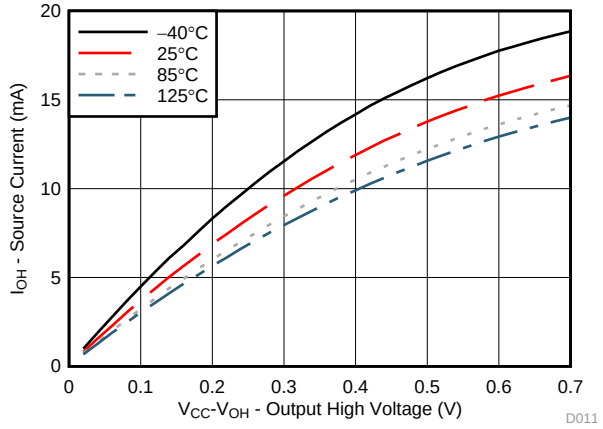


Figure 9. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

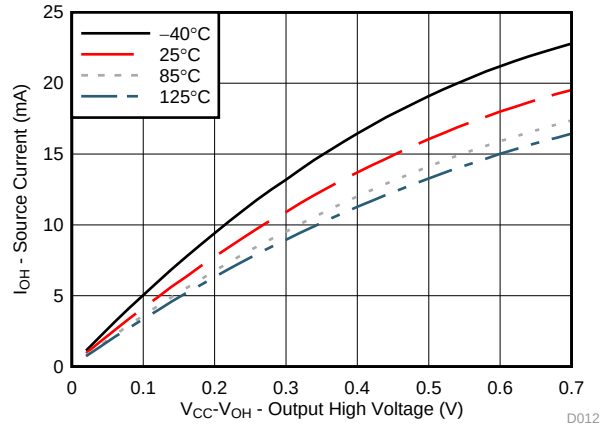


Figure 10. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

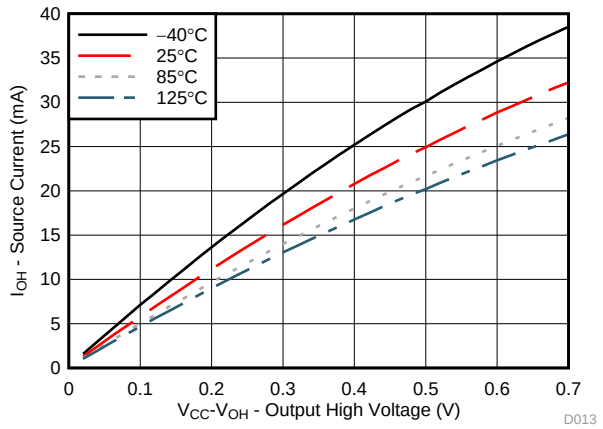


Figure 11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

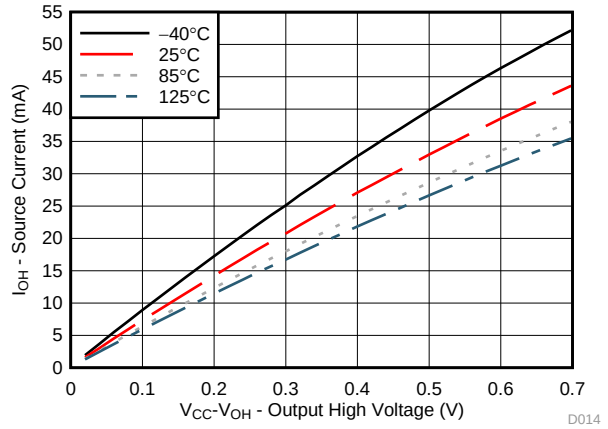


Figure 12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

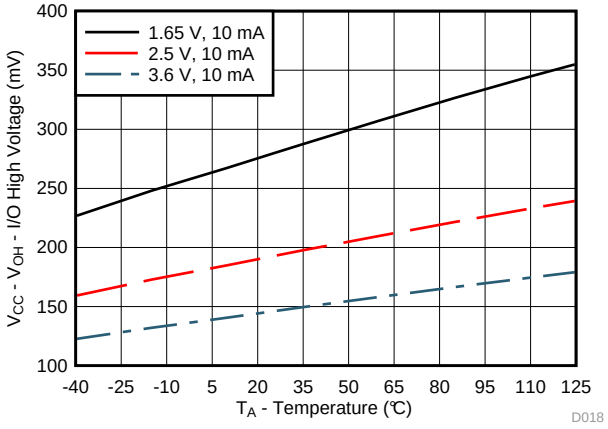


Figure 13. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

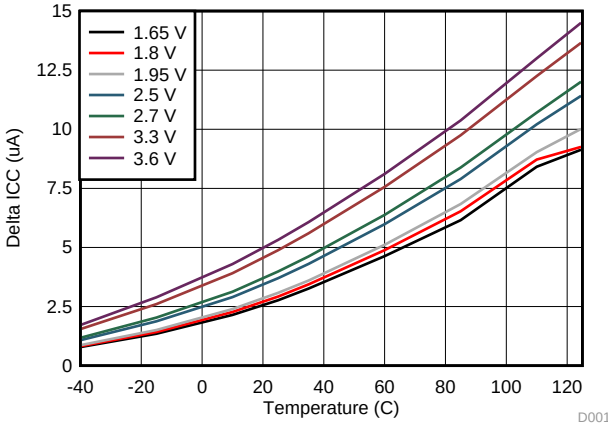
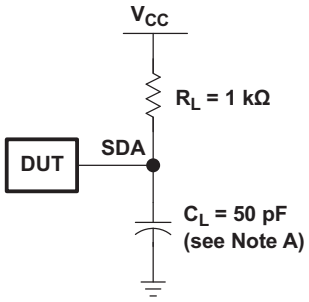
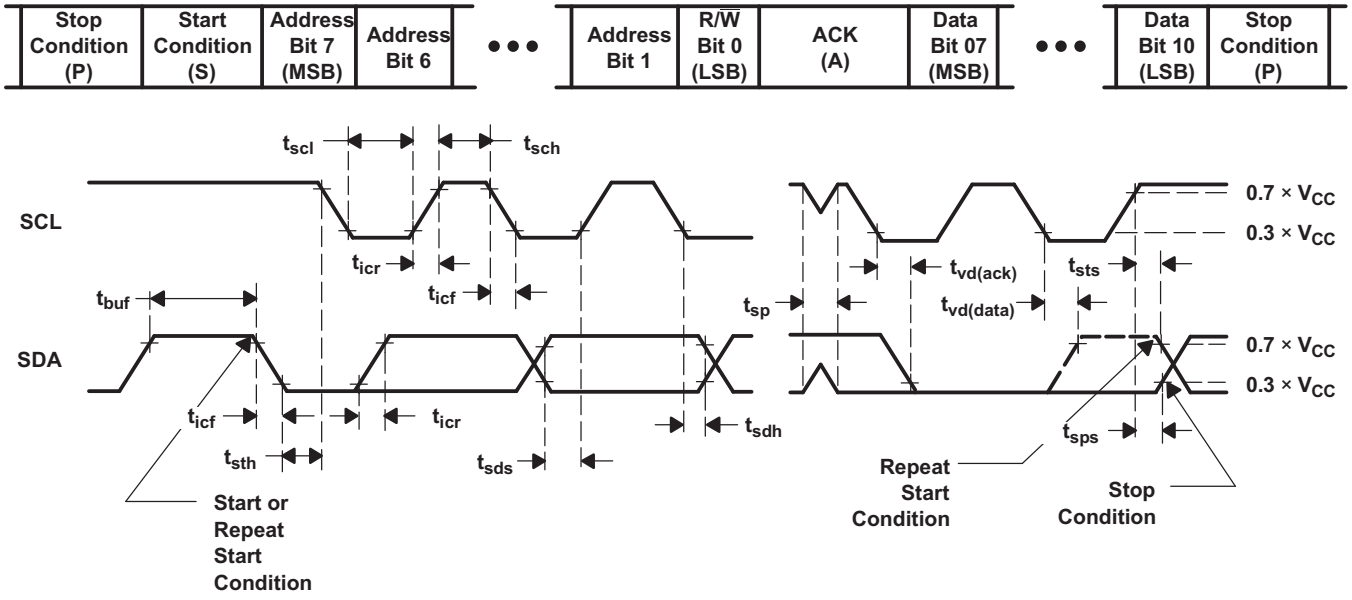


Figure 14. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

7 Parameter Measurement Information



SDA Load Configuration



Voltage Waveforms

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

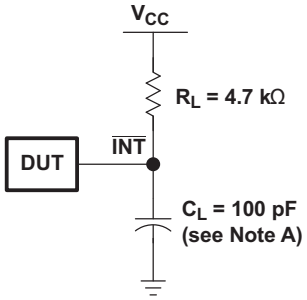
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

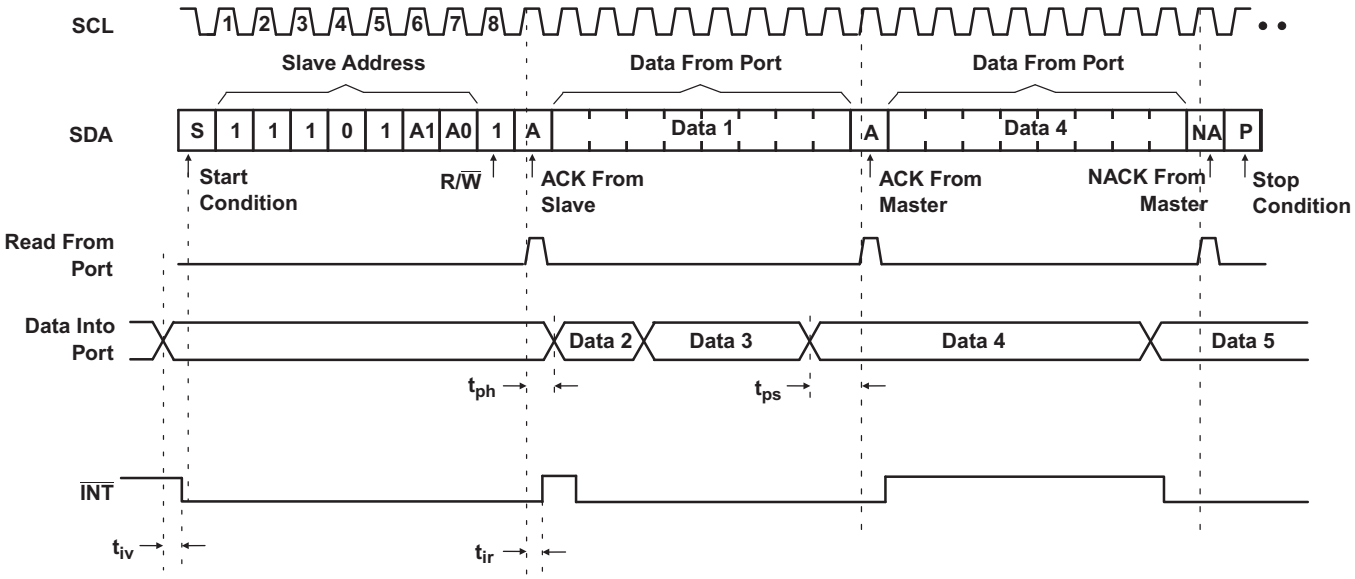
C. All parameters and waveforms are not applicable to all devices.

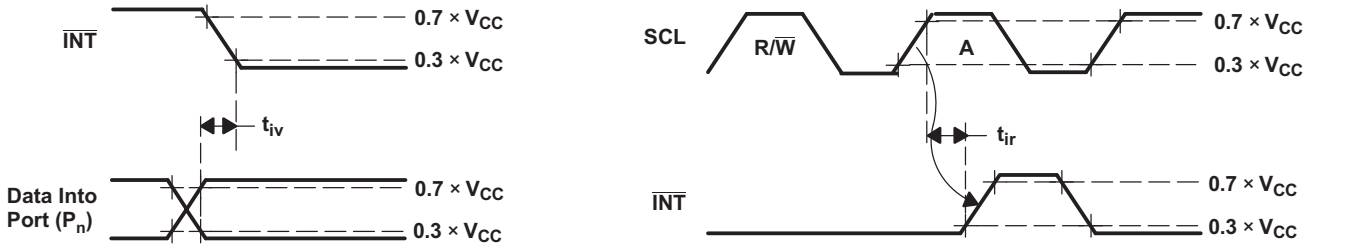
Figure 15. I^2C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



Interupt Load Configuration





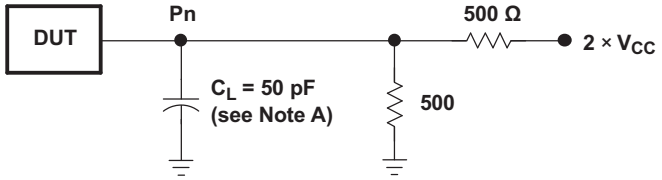
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 Hz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

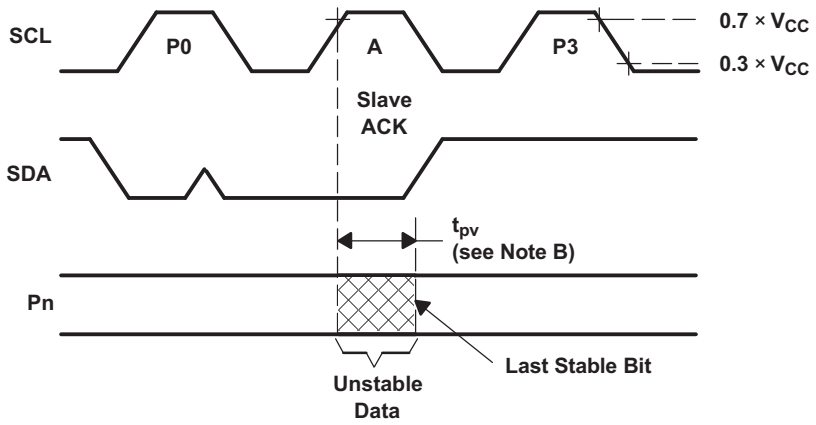
C. All parameters and waveforms are not applicable to all devices.

Figure 16. Interrupt Load Circuit and Voltage Waveforms

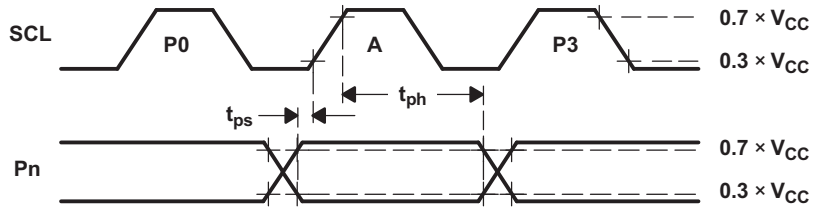
Parameter Measurement Information (continued)



P-Port Load Configuration



Write Mode (R/$\overline{W}$ = 0)



Read Mode (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (P_n) output.

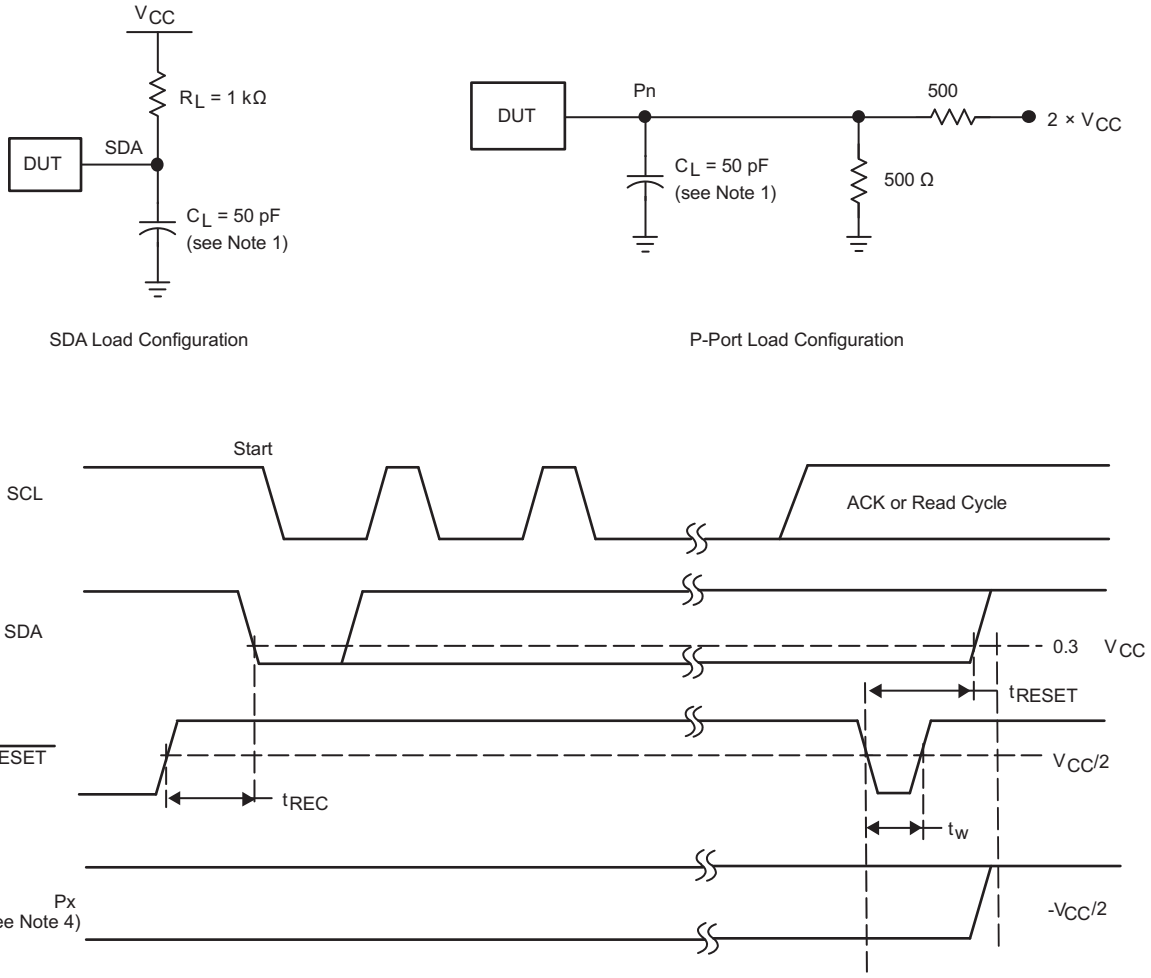
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 17. P-Port Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



(1) C_L includes probe and jig capacitance.

(2) All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

(3) The outputs are measured one at a time, with one transition per measurement.

(4) I/Os are configured as inputs.

(5) All parameters and waveforms are not applicable to all devices.

Figure 18. Reset Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9539-Q1 is a 16-bit I/O expander for the two-line bidirectional bus (I^2C) designed for 1.65 V to 3.6 V, V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface, serial clock (SCL) and serial data (SDA).

The TCA9539-Q1 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the TCA9539-Q1 in the event of a time-out or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I^2C-SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset-initialization to occur without depowering the part.

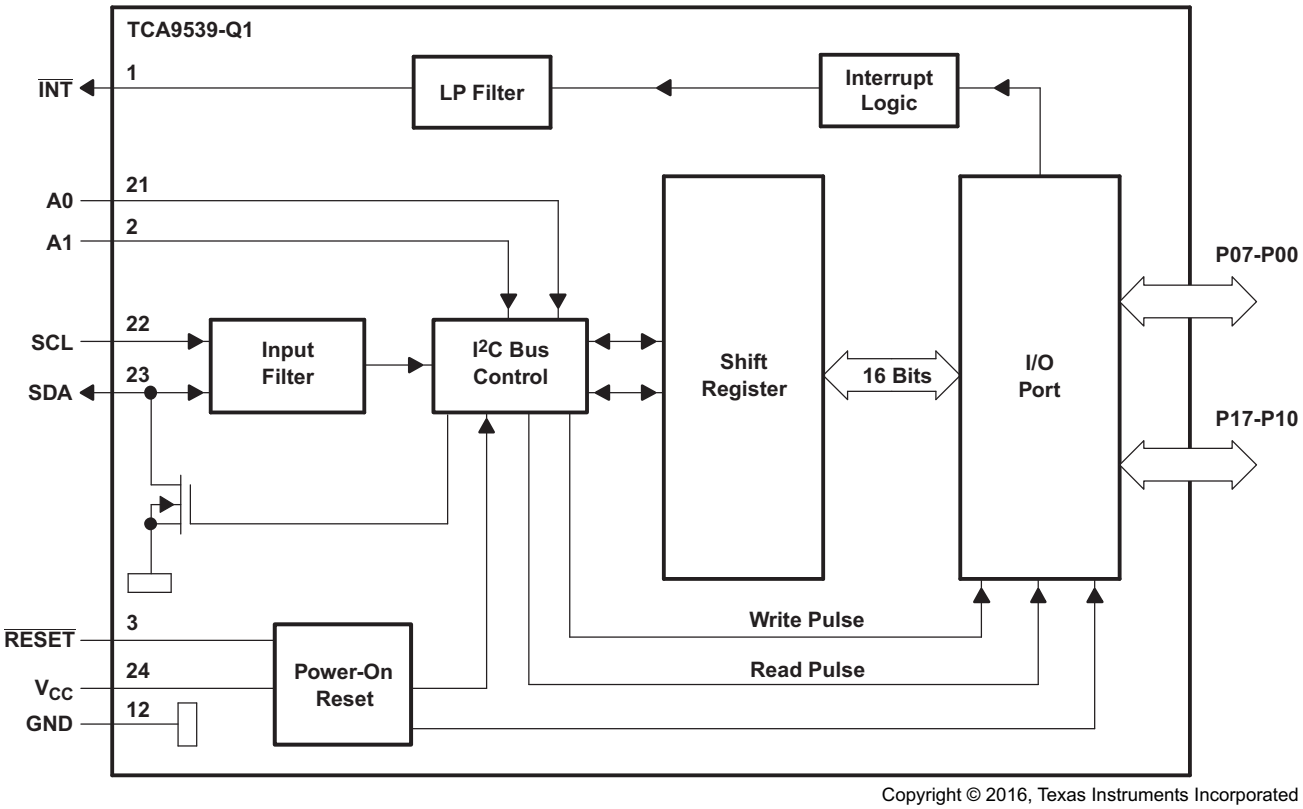
The TCA9539-Q1 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA9539-Q1 can remain a simple slave device.

The TCA9539-Q1 is similar to the TCA9555, except for the removal of the internal I/O pull-up resistor, which greatly reduces power consumption when the I/Os are held low, replacement of A2 with $\overline{\text{RESET}}$, and a different address range. The TCA9539-Q1 is similar to the PCA9539 with lower voltage support (down to V_{CC} = 1.65 V), and also improved power-on-reset circuitry for different application scenarios.

Two hardware pins (A0 and A1) are used to program and vary the fixed I^2C address and allow up to four devices to share the same I^2C bus or SMBus.

8.2 Functional Block Diagram

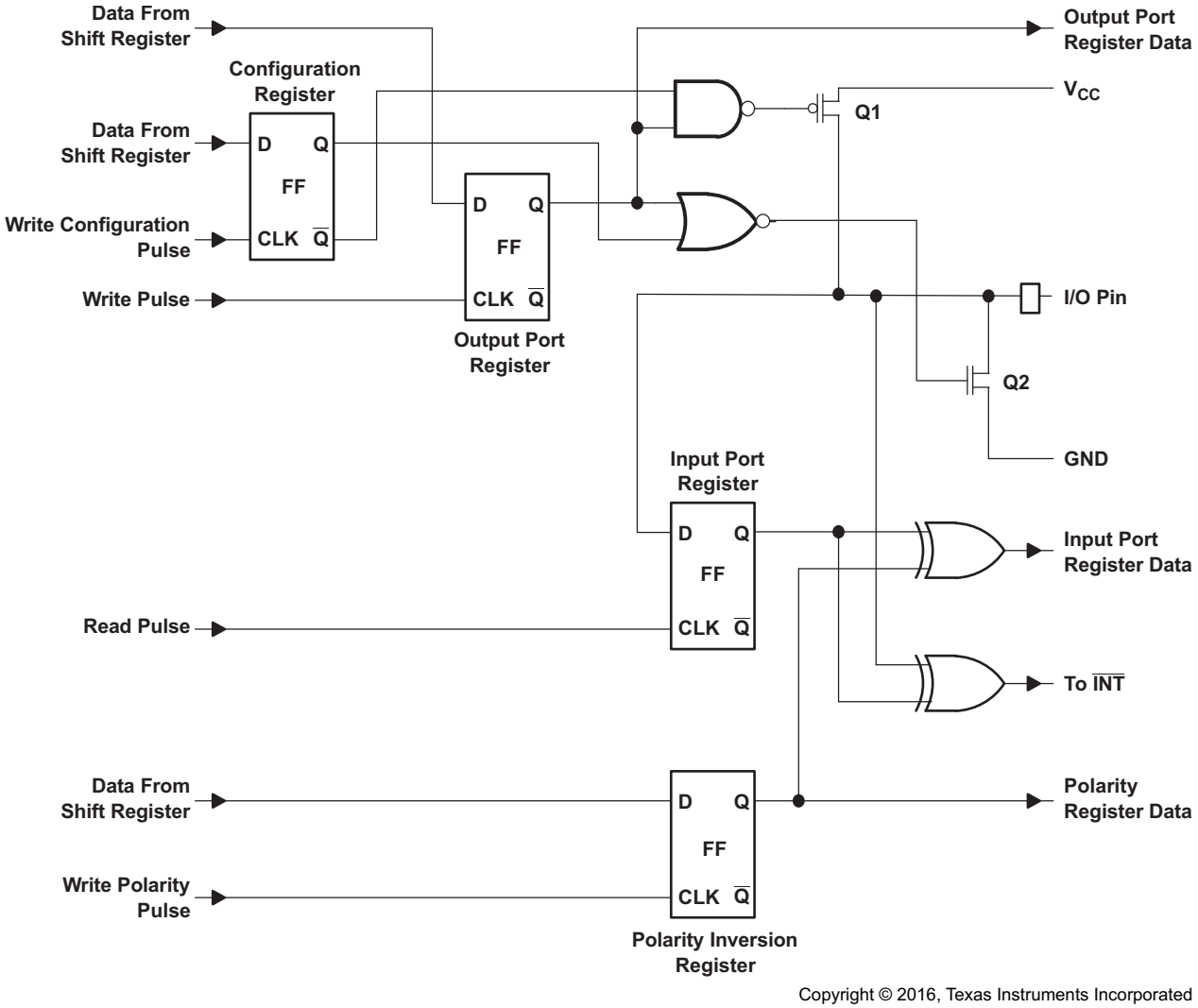


Pin numbers shown are for PW package.

All I/Os are set to inputs at reset.

Figure 19. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



At power-on reset, all registers return to default values.

Figure 20. Simplified Schematic of P-Port I/Os

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

8.3.2 $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TCA9539-Q1 registers and I^2C-SMBus state machine are held in their default states until $\overline{\text{RESET}}$ is once again high. This input requires a pull-up resistor to V_{CC}, if no active connection is used.

Feature Description (continued)

8.3.3 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the $\overline{INT}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{INT}$ has an open-drain structure and requires a pull-up resistor to V_{CC}.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA9539-Q1 in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the TCA9539-Q1 registers and I^2C-SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to V_{PORF} and then back up to the operating voltage for a power-reset cycle. See Figure 21.

8.5 Programming

8.5.1 I^2C Interface

The TCA9539-Q1 has a standard bidirectional I^2C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^2C bus has a specific device address to differentiate between other slave devices that are on the same I^2C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see *Understanding the I^2C Bus*, SLVA704.

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. For further details, see *I^2C Pull-up Resistor Calculation*, SLVA689. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See Table 1.

Figure 21 and Figure 22 show the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
   - Master-transmitter sends a START condition and addresses the slave-receiver.
   - Master-transmitter sends data to slave-receiver.
   - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
   - Master-receiver sends a START condition and addresses the slave-transmitter.
   - Master-receiver sends the requested register to read to slave-transmitter.
   - Master-receiver receives data from the slave-transmitter.

Programming (continued)

– Master-receiver terminates the transfer with a STOP condition.

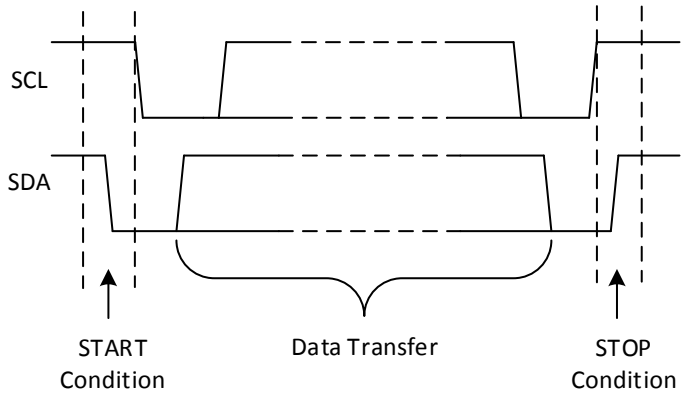


Figure 21. Definition of Start and Stop Conditions

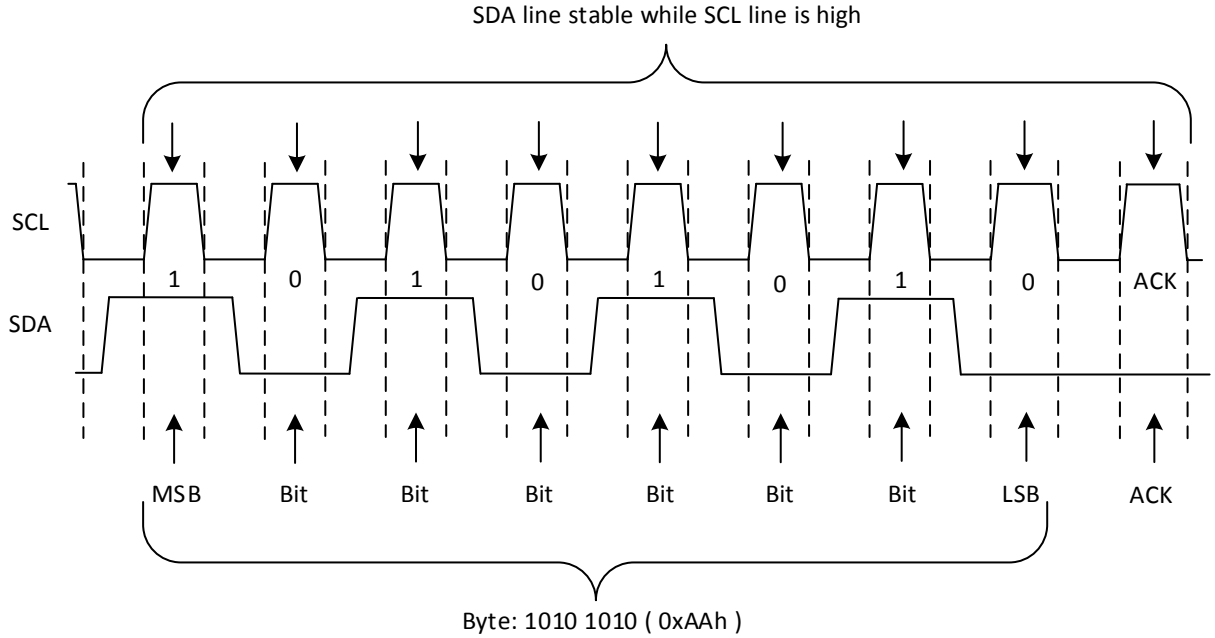


Figure 22. Bit Transfer

Table 1 shows the interface definition.

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	H	H	H	L	H	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.6 Register Maps

8.6.1 Device Address

Figure 23 shows the address byte of the TCA9539-Q1.

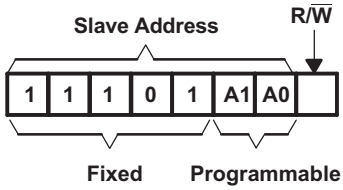


Figure 23. TCA9539-Q1 Address

Table 2 shows the address reference of the TCA9539-Q1.

Table 2. Address Reference

INPUTS		I^2C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 74 (hexadecimal)
L	H	117 (decimal), 75 (hexadecimal)
H	L	118 (decimal), 76 (hexadecimal)
H	H	119 (decimal), 77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.6.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte shown in Table 3 that is stored in the control register in the TCA9539-Q1. Three bits of this data byte state the operation (read or write) and the internal register (input, output, Polarity Inversion or Configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

When a command byte has been sent, the register pair that was addressed continues to be accessed by reads until a new command byte has been sent. Figure 24 shows the control register bits.

0	0	0	0	0	B2	B1	B0

Figure 24. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read-write byte	1111 1111
0	1	1	0x03	Output Port 1	Read-write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read-write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read-write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read-write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read-write byte	1111 1111

8.6.3 Register Descriptions

The Input Port registers (registers 0 and 1) shown in Table 4 reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next.

Table 4. Registers 0 And 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) shown in Table 5 show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Registers 2 And 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) shown in Table 6 allow Polarity Inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 6. Registers 4 And 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) shown in Table 7 configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Registers 6 And 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

8.6.3.1 Bus Transactions

Data is exchanged between the master and the TCA9539-Q1 through write and read commands, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

8.6.3.1.1 Writes

To write on the I^2C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See the *Control Register And Command Byte* section to see list of the TCA9539-Q1s internal registers and a description of each one.

Figure 25 shows an example of writing a single byte to a slave register.

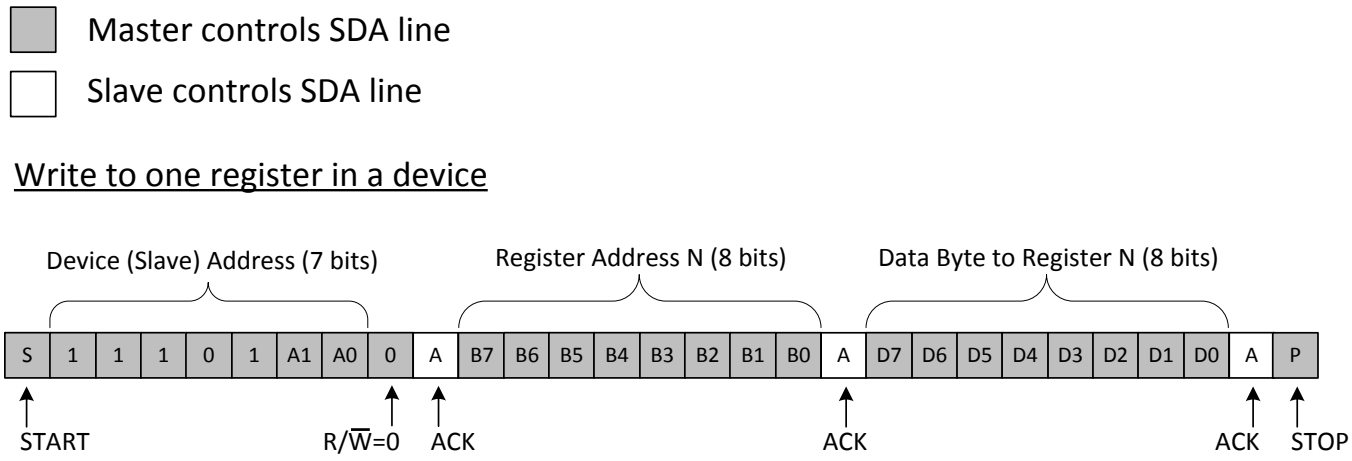


Figure 25. Write to Register

Figure 27 shows the Write to the Polarity Inversion Register.

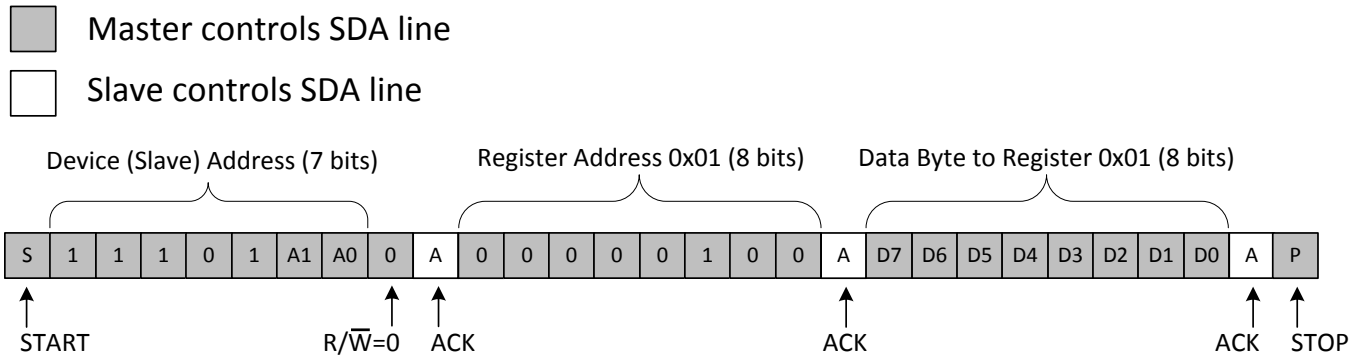


Figure 26. Write to the Polarity Inversion Register

Figure 27 shows the Write to Output Port Registers

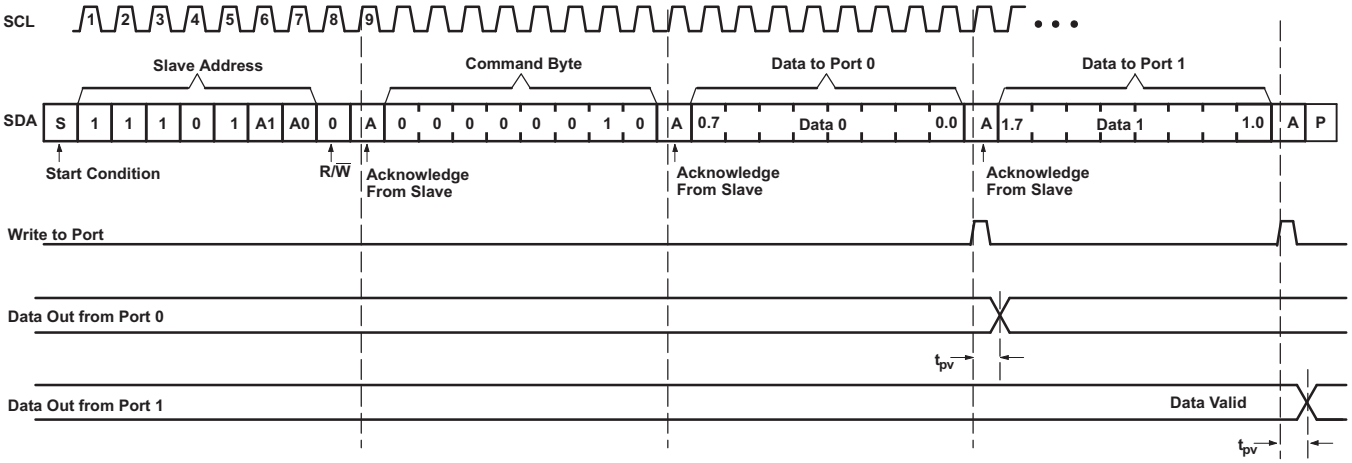


Figure 27. Write to Output Port Registers

8.6.3.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/$\overline{W}$ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

If a read is requested by the master after a POR without first setting the command byte via a write, the device NACKs until a command byte-register address is set as described above.

See the *Control Register And Command Byte* section to see list of the TCA9539-Q1s internal registers and a description of each one.

Figure 28 shows an example of reading a single byte from a slave register.

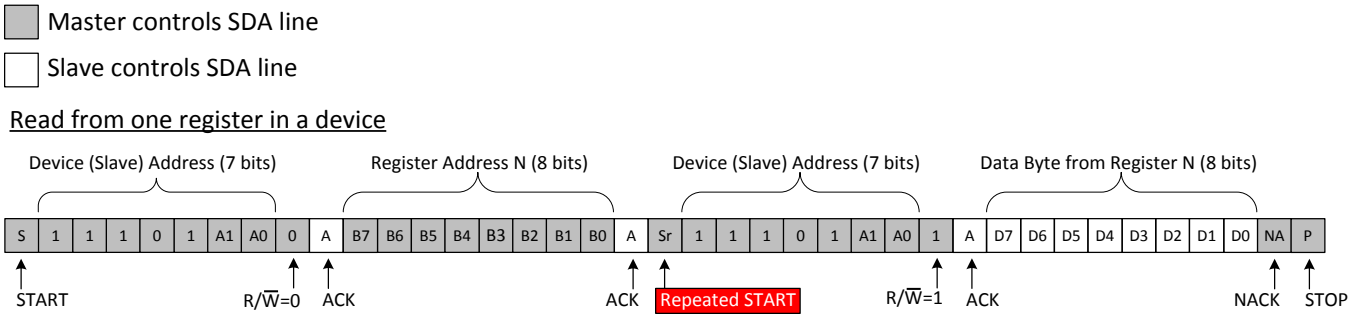
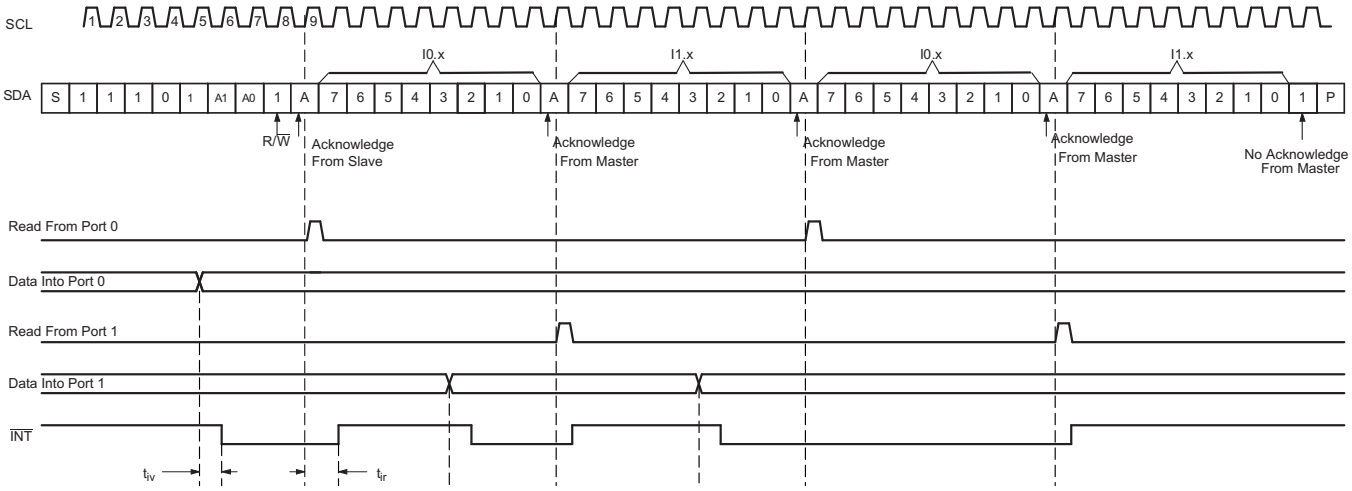


Figure 28. Read from Register

When a restart occurs after a single write request to a register, the requested register is used for the read request. Note that when reading multiple bytes of data. Data is clocked into the register on the rising edge of the ACK clock pulse before data is sent. The internal register value is also changed to the other register of the pair on the rising edge of the ACK clock pulse before data is sent. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. If a restart occurs during a read, the data is lost becuase the internal register already has been changed to the next register in the pair.

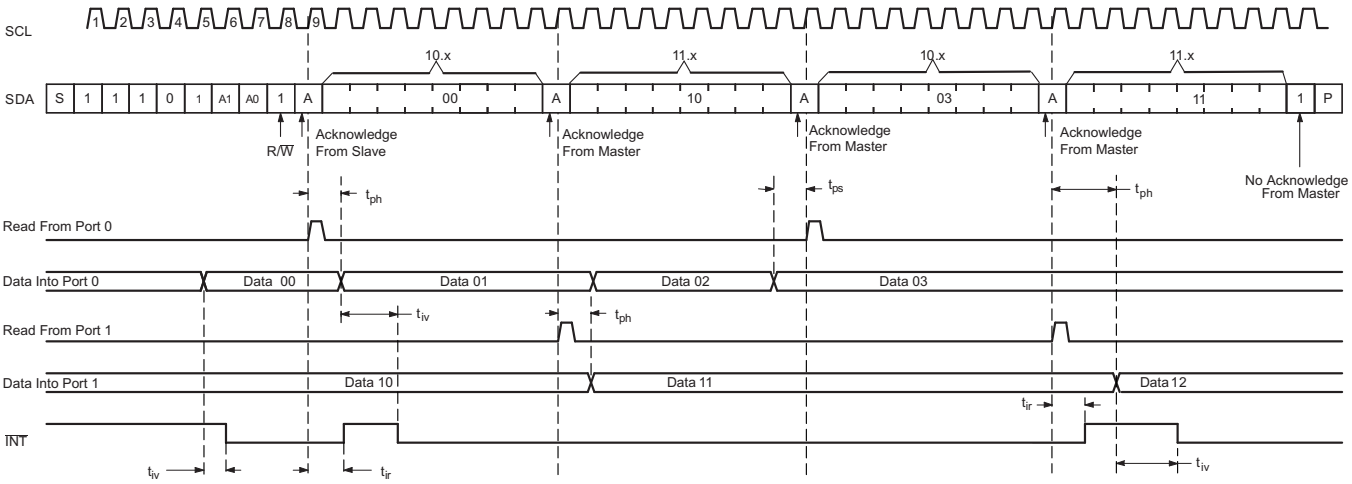
There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data. Figure 29 and Figure 30 show two different scenarios of Read Input Port Register.



Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see the *Reads* section for these details).

Figure 29. Read Input Port Register, Scenario 1



Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see the *Reads* section for these details).

Figure 30. Read Input Port Register, Scenario 2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

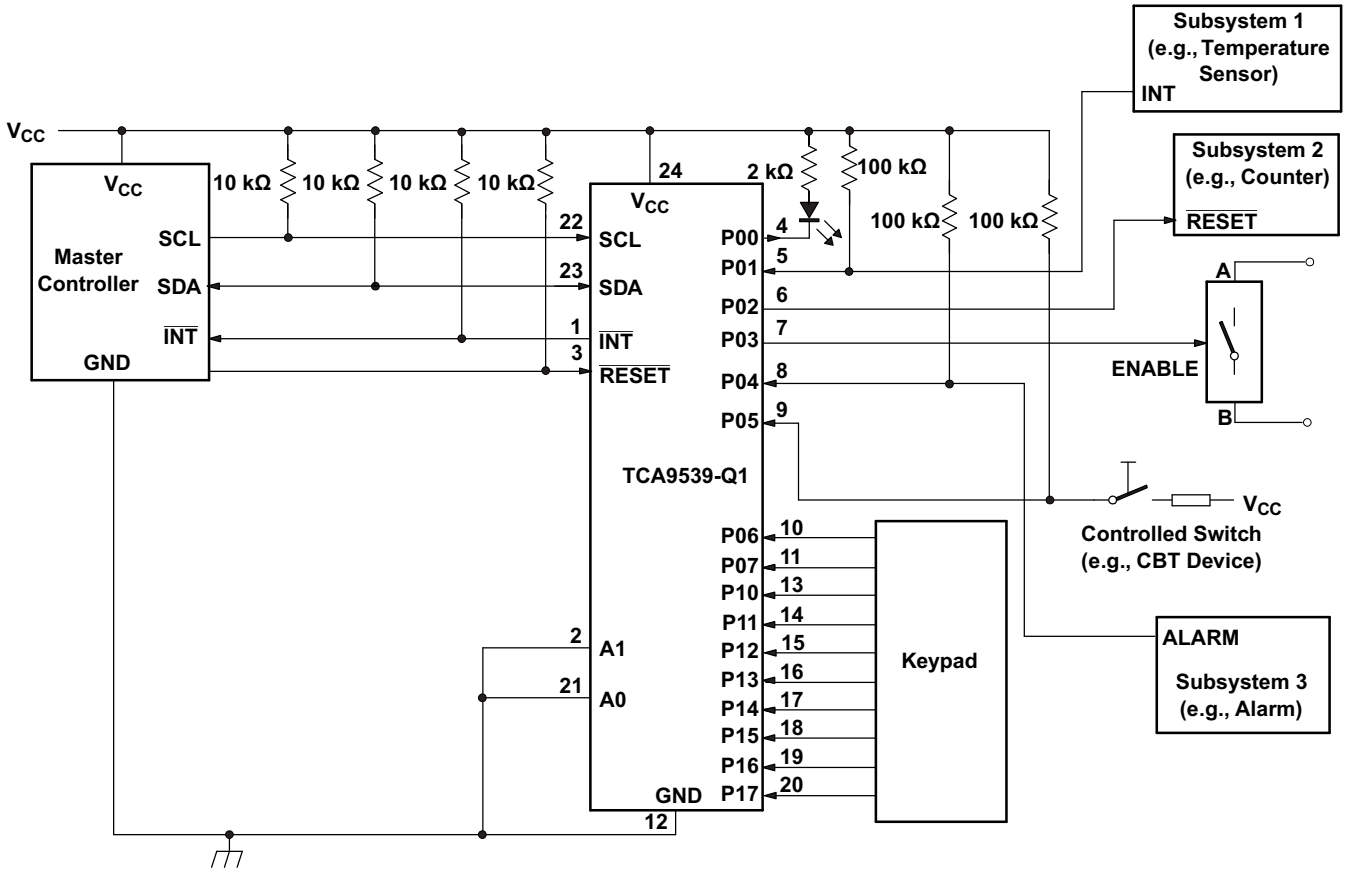
9.1 Application Information

Applications of the TCA9539-Q1 has this device connected as a slave to an I^2C master (processor), and the I^2C bus may contain any number of other slave devices. The TCA9539-Q1 is typically in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

IO Expanders such as the TCA9539-Q1 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

9.2 Typical Application

Figure 31 shows an application in which the TCA9539-Q1 can be used.



Device address is configured as 1110100 for this example.

P00, P02, and P03 are configured as outputs.

P01 and P04 to P17 are configured as inputs.

Pin numbers shown are for the PW package.

Figure 31. Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with the TCA9539-Q1, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in *Thermal Information* table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

9.2.1.2 Minimizing I_{CC} When I/Os Control LEDs

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor (see Figure 31). Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in the *Electrical Characteristics* table show how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC}, when the LED is off, to minimize current consumption.

Figure 32 shows a high-value resistor in parallel with the LED. Figure 33 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{CC} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

Take care to make sure that the recommended maximum I_{OL} through the ports not be violated based upon junction temperature. See the *Recommended Operating Conditions* for more information.

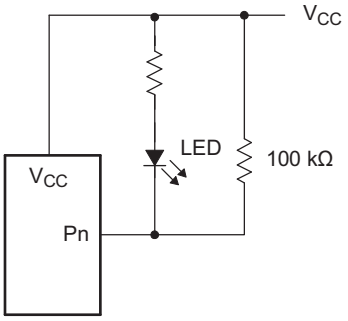


Figure 32. High-Value Resistor In Parallel With LED

Typical Application (continued)

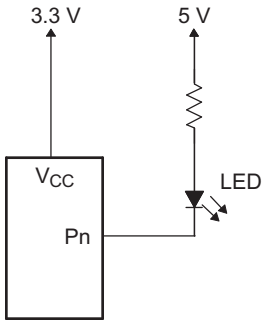


Figure 33. Device Supplied By Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 5.

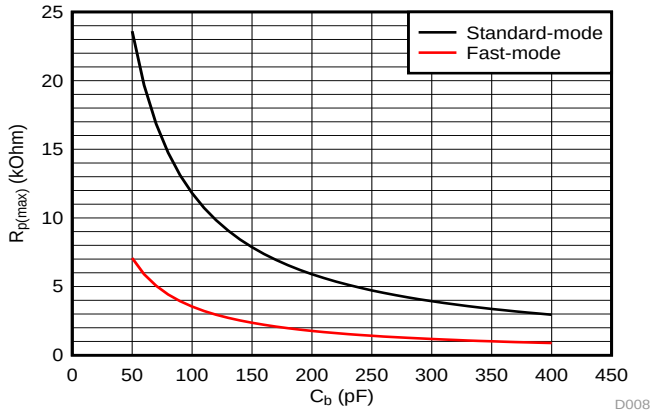
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9539-Q1, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections, traces, and the capacitance of additional slaves on the bus.

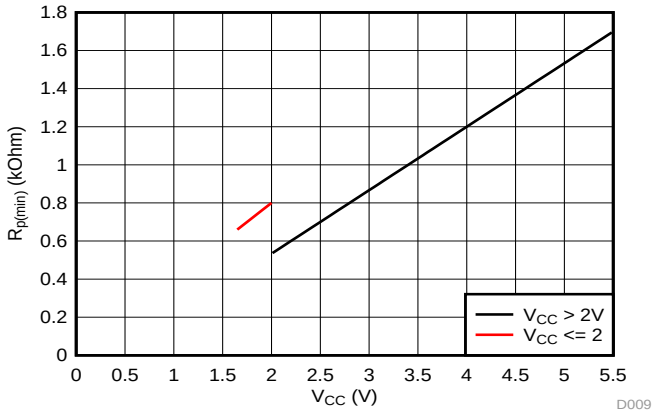
9.2.3 Application Curves



Standard-mode (f_{SCL} = 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 34. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 35. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9539-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The voltage waveform for a power-on reset is shown in Figure 36.

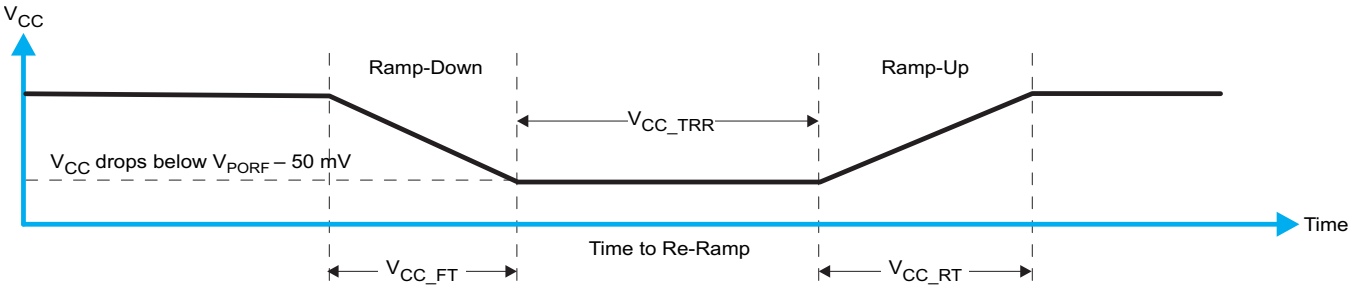


Figure 36. V_{CC} is Lowered Below the POR Threshold, then Ramped Back Up to V_{CC}

Table 8 specifies the performance of the power-on reset feature for TCA9539-Q1.

Table 8. Recommended Supply Sequencing And Ramp Rates (1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 36	0.1			ms
V_{CC_RT}	Rise rate	See Figure 36	0.1			ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 36	2			µs
V_{CC_GH}	The level (referenced to V_{CC}) that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW}	See Figure 37			1.2	V
V_{CC_MV}	The minimum voltage that V_{CC} can glitch down to without causing a reset (V_{CC_GH} must not be violated)	See Figure 37	1.5			V
V_{CC_GW}	Glitch width that does not cause a functional disruption	See Figure 37			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.75	1		V
V_{PORR}	Voltage trip point of POR on rising V_{CC}			1.2	1.5	V

(1) T_A = –40°C to +125°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 37 and Table 8 provide more information on how to measure these specifications.

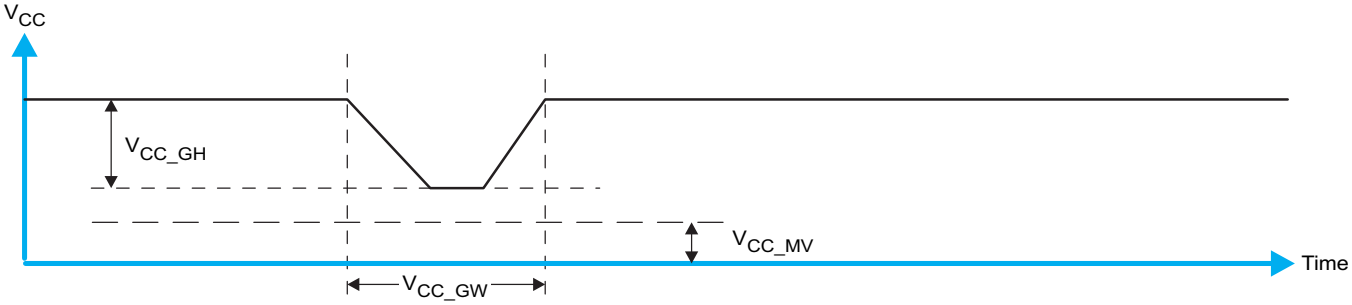


Figure 37. Glitch Width, Glitch Height, and Minimum Glitch Voltage

V_{POR} is critical to the power-on reset. V_{PORR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 38 and Table 8 provide more details on this specification.

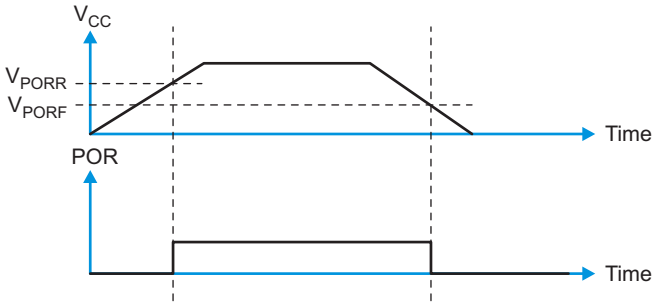


Figure 38. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9539-Q1, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9539-Q1 as possible. These best practices are shown in Figure 39.

For the layout example provided in Figure 39, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which must attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 39.

11.2 Layout Example

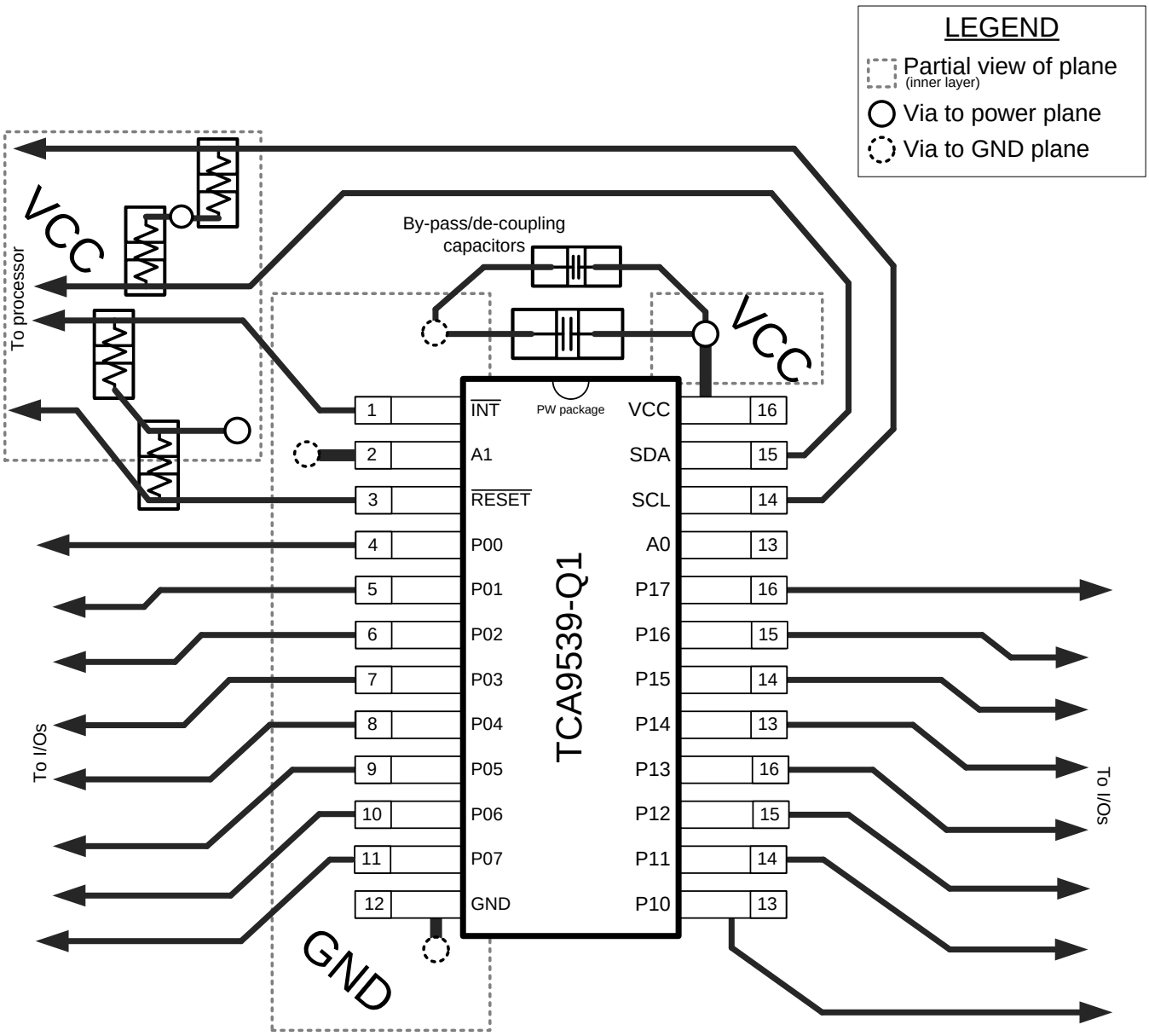


Figure 39. TCA9539-Q1 Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《理解 I2C 总线》*，SLVA704
- *《I2C 上拉电阻计算》*，SLVA689
- *《逻辑器件简介》*，SLVA700
- *《采用中继器时 I2C 总线的最大时钟频率》*，SLVA695
- *《I2C 总线上拉电阻计算》*，SLVA689

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9539QPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCA539Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

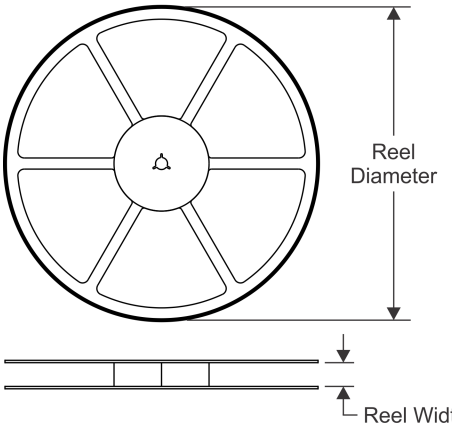
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

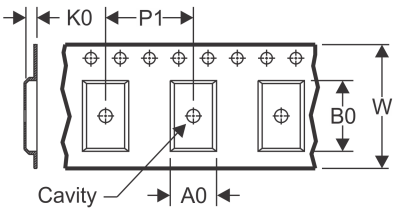
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

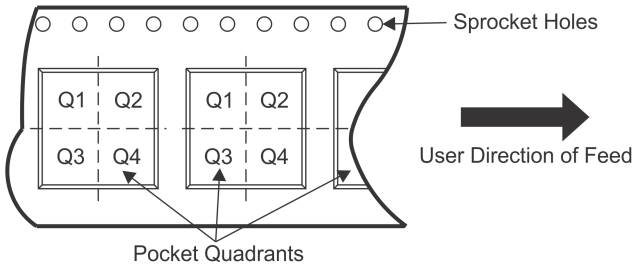


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

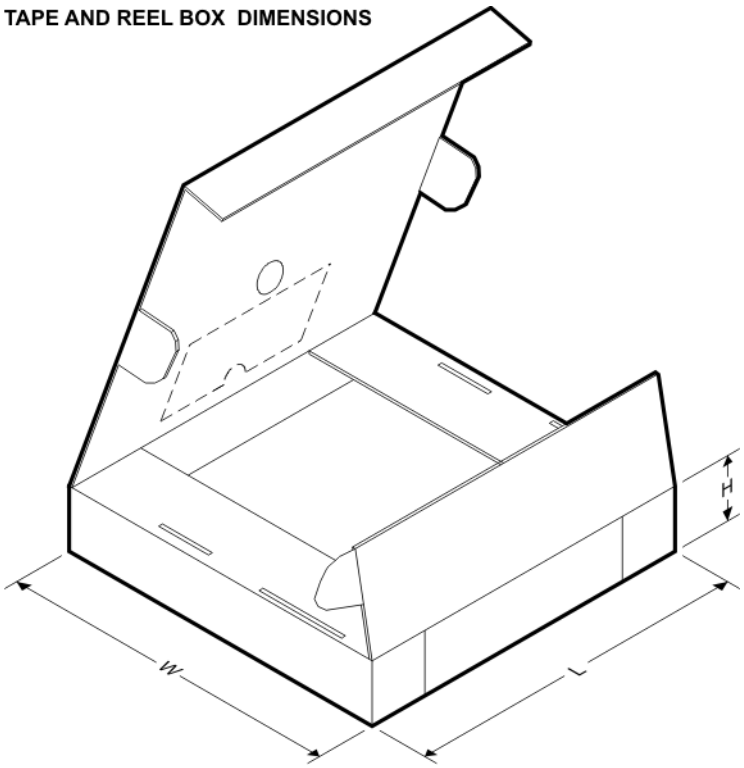
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9539QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

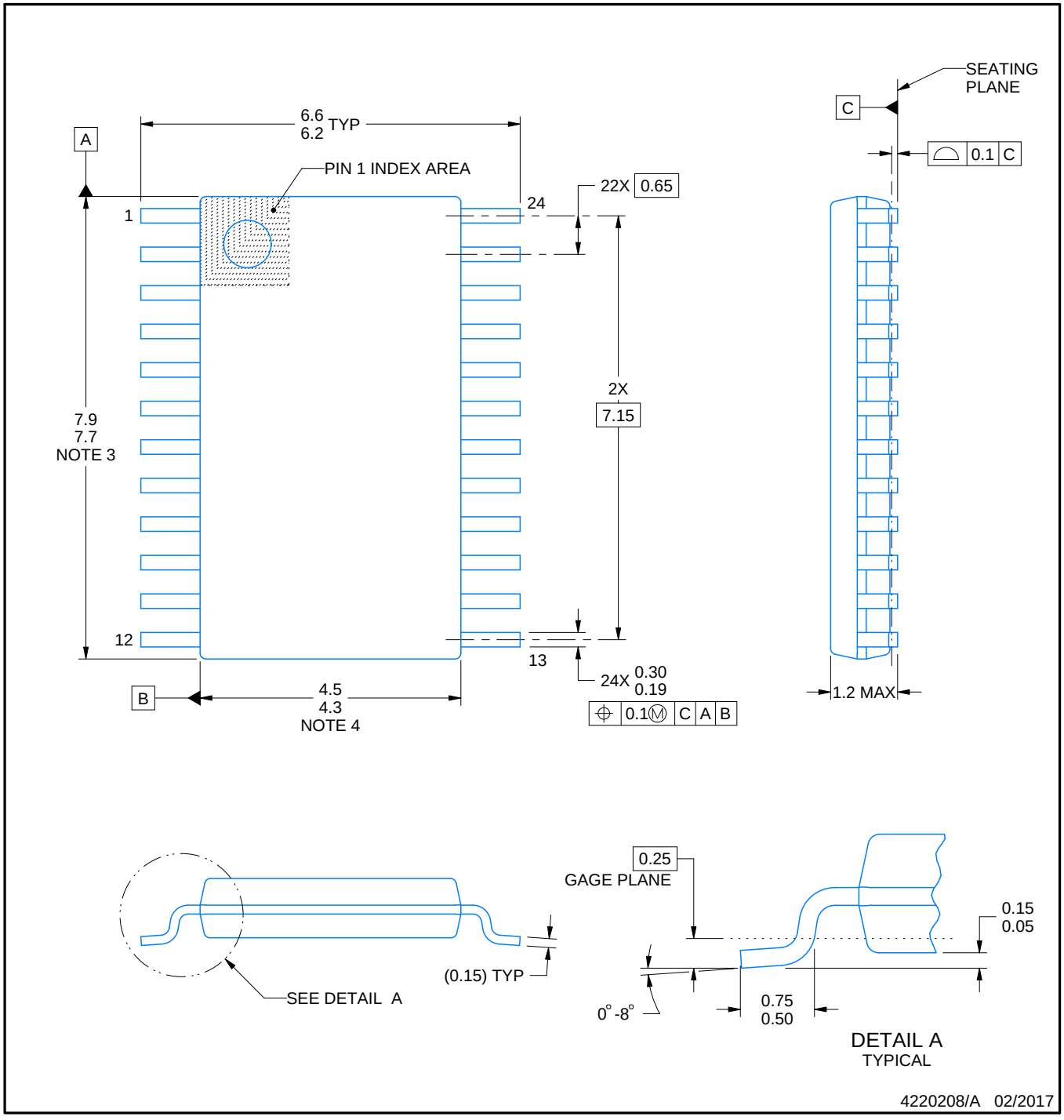
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9539QPWRQ1	TSSOP	PW	24	2000	853.0	449.0	35.0

PACKAGE OUTLINE

PW0024A

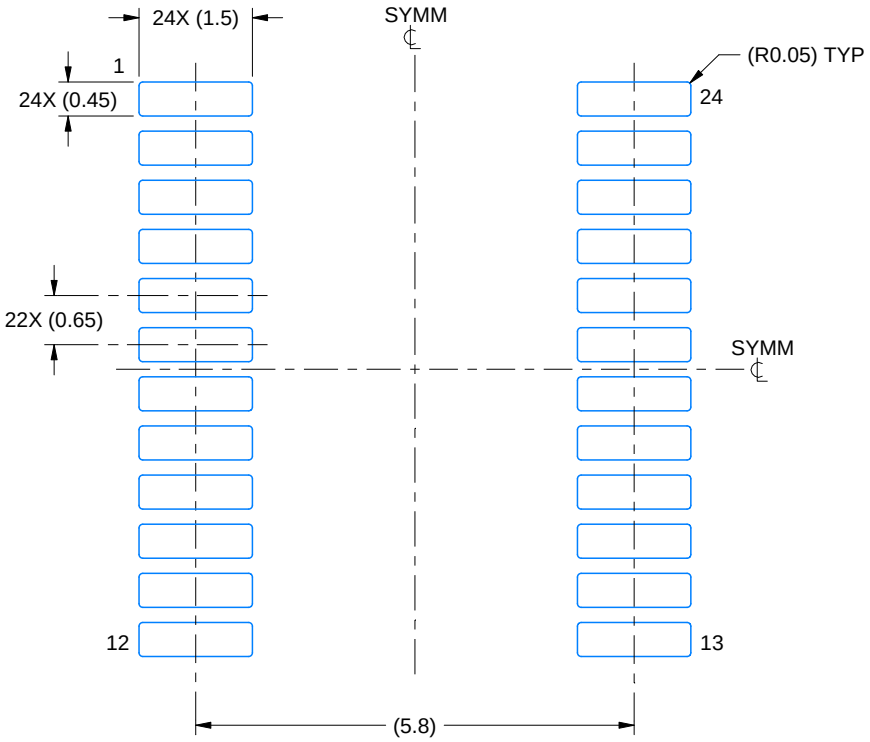
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

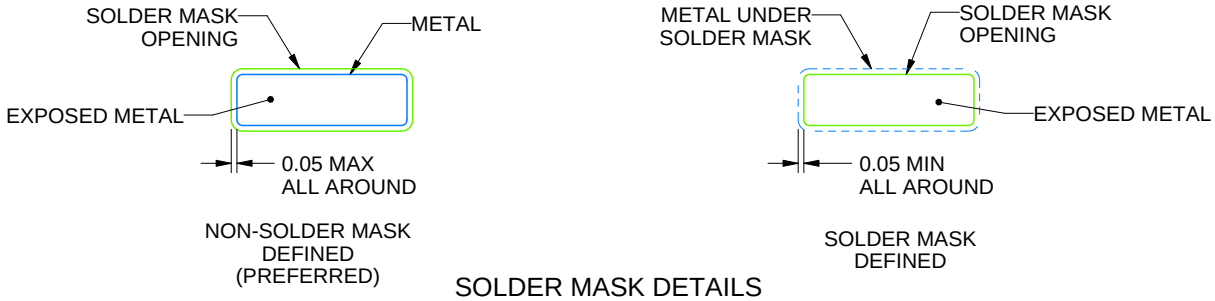


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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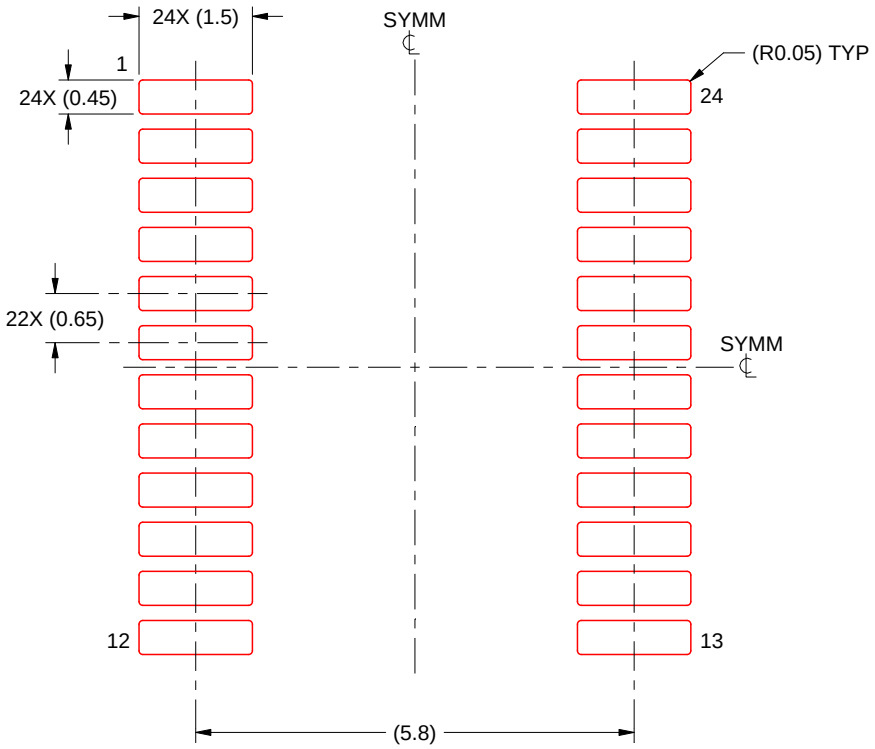
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122