SN65LVDS93A-Q1 FlatLink™ 发送器

1 特性

- 具有符合 AEC-Q100 标准的以下结果：
  - 温度等级 3：-40°C 至 85°C
  - 人体模型 (HBM) 静电放电 (ESD) 分类等级 3
  - 充电器件模型 (CDM) ESD 分类等级 C6
- 低压差分信号 (LVDS) 显示系列接口，可直接连接具有集成 LVDS 的 LCD 显示面板
- 封装：14mm x 6.1mm 薄型小外形尺寸 (TSSOP)
- 1.8V 至 3.3V 耐压数据输入，可直接连接低功耗、低压应用和图形处理器
- 传输速率高达 135Mpps（每秒百万像素）；像素时钟频率范围为 10MHz 至 135MHz
- 适合 HVGA 到高清 (HD) 范围内的显示分辨率，并且电磁干扰 (EMI) 较低
- 通过 3.3V 单电源供电运行，75MHz 频率下的功耗为 170mW（典型值）
- 28 个数据通道 + 时钟输入低压晶体管-晶体管逻辑 (TTL)，4 个数据通道 + 时钟输出低压差分
- 禁用时的功耗不到 1mW
- 可选择上升或下降时钟沿触发输入
- 支持扩频时钟 (SSC)
- 兼容所有 OMAP™ 2x、OMAP™ 3x 和 DaVinci™ 应用处理器

2 应用

- LCD 显示面板驱动器
- 超便携移动个人电脑 (UMPC) 和上网本
- 数码相框

3 说明

SN65LVDS93A-Q1 Flatlink™ 发送器在单个集成电路上包含了四个 7 位并联负载串行输出移位寄存器、一个 7X 时钟合成器以及五个低压差分信号 (LVDS) 线路驱动器。 凭借这些功能，该器件可通过 5 条平衡双股线同步发送 28 位单端低电压晶体管-晶体管逻辑 (LVTTL) 数据，这些数据将由 SN75LVDS94 和具有集成 LVDS 接收器的 LCD 面板等兼容接收器来接收。

发送数据时，数据位 D0 至 D27 会在输入时钟信号 (CLKIN) 边沿逐个载入寄存器。 可通过时钟选择 (CLKSEL) 引脚来选择时钟的上升沿或下降沿。 CLKIN 的频率会进行 7 倍倍频，然后用于以串行方式分 7 位时间片上传数据寄存器。 接着会将 4 个串行数据流和锁相时钟 (CLKOUT) 输出至 LVDS 输出驱动器。 CLKOUT 的频率与输入时钟 (CLKIN) 相同。

SN65LVDS93A-Q1 无需外部元件或者很少，而且也无需控制。 发送器输入端的数据总线与接收器输出端的相同，数据传输对于用户而言是透明的。 用户唯一能够干预的是选择时钟上升沿（向 CLKSEL 输入高电平）或下降沿（向 CLKSEL 输入低电平），以及能够使用关断/清零 ($\overline{\text{SHTDN}}$) 引脚。 $\overline{\text{SHTDN}}$ 是一个低电平有效输入，可禁用时钟并关断 LVDS 输出驱动器，从而降低功耗。 该信号为低电平时，可将所有内部寄存器置为低电平。

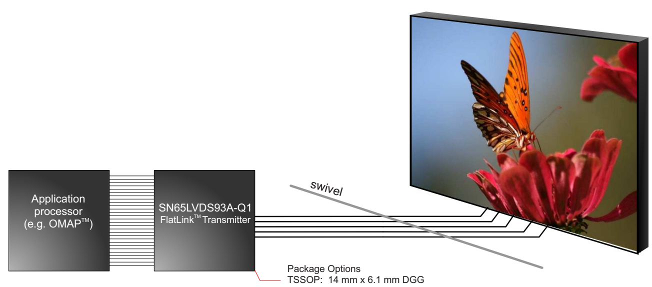
SN65LVDS93A-Q1 额定工作环境温度范围为 -40°C 至 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN65LVDS93A-Q1	TSSOP (56)	14.00mm x 6.10mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

Changes from Revision A (February 2015) to Revision B **Page**

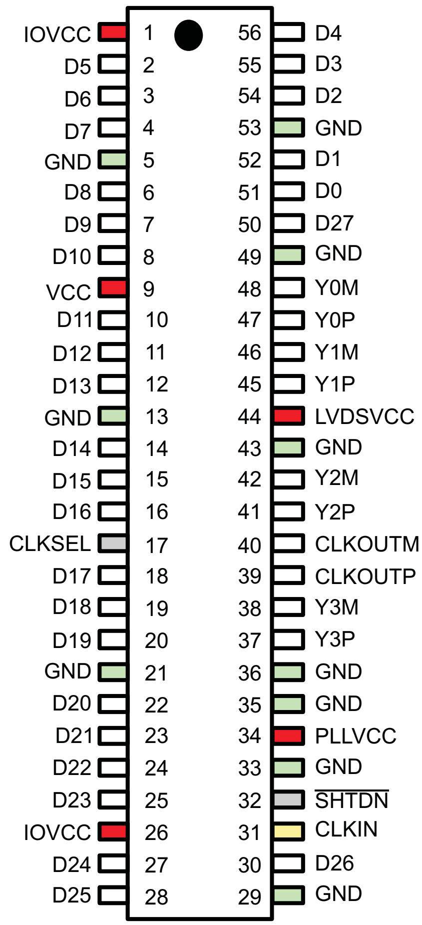
- Changed "Toggle LVDS83B" To "Toggle SN65LVDS93A-Q1" in item 4 in the *Power Up Sequence section* ... 17
- Changed "this allows the LVDS83B" To "this allows the SN65LVDS93A-Q1" in item 5 in the *Power Up Sequence section* ... 17

Changes from Original (February 2015) to Revision A **Page**

- 已将特性中的"人体模型 (HBM) 静电放电 (ESD) 分类等级 2"更改为"人体模型 (HBM) 静电放电 (ESD) 分类等级 3" ... 1
- 已删除特性中的"ESD：5kV HBM，1.5kV CDM" ... 1

5 Pin Configuration and Functions

56-PIN
DGG PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLKIN	31	CMOS IN with pulldn	Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
CLKOUTP, CLKOUTM	39 40	LVDS Out	Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
CLKSEL	17	CMOS IN with pulldn	Selects between rising edge input clock trigger (CLKSEL = V_{IH}) and falling edge input clock trigger (CLKSEL = V_{IL}).
D5, D6, D7, D8 D9, D10, D11, D12 D13, D14, D15, D16 D17, D18, D19, D20 D21, D22, D23, D24 D25, D26, D27 D0, D1, D2, D3, D4	2, 3, 4, 6 7, 8, 10, 11 12, 14, 15 , 16 18, 19, 20, 22 23, 24, 25, 27 28, 30, 50 51, 52, 54, 55, 56	CMOS IN with pulldn	Data inputs; supports 1.8 V to 3.3 V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). For input bit assignment see Figure 15 to Figure 18 for details. Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
GND	5, 13, 21, 29, 33, 35, 36, 43, 49, 53	Power Supply(1)	Supply ground for VCC, IOVCC, LVDSVCC, and PLLVCC.

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
IOVCC	1, 26	Power Supply(1)	I/O supply reference voltage (1.8 V up to 3.3 V matching the GPU data output signal swing)
LVDSVCC	44	Power Supply(1)	3.3 V LVDS output analog supply
PLLVCC	34	Power Supply(1)	3.3 V PLL analog supply
$\overline{\text{SHTDN}}$	32	CMOS IN with pulldn	Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
VCC	9	Power Supply(1)	3.3 V digital supply voltage
Y0P, Y0M Y1P, Y1M Y2P, Y2M	47, 48 45, 46 41, 42	LVDS Out	Differential LVDS data outputs. Outputs are high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted)
Y3P, Y3M	37, 38	LVDS Out	Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.

6 Specifications

6.1 Absolute Maximum Ratings[1]

	MIN	MAX	UNIT
Supply voltage range, VCC, IOVCC, LVDSVCC, PLLVCC[2]	–0.5	4	V
Voltage range at any output terminal	–0.5	VCC + 0.5	V
Voltage range at any input terminal	–0.5	IOVCC + 0.5	V
Continuous power dissipation	See *Thermal Information*		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to the GND terminals.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q200-002[1]	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q200-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, VCC		3	3.3	3.6	V
LVDS output Supply voltage, LVDSVCC		3	3.3	3.6	
PLL analog supply voltage, PLLVCC		3	3.3	3.6	
IO input reference supply voltage, IOVCC		1.62	1.8 / 2.5 / 3.3	3.6	
Power supply noise on any VCC terminal				0.1	
High-level input voltage, V_{IH}	IOVCC = 1.8 V	IOVCC/2 + 0.3 V			V
	IOVCC = 2.5 V	IOVCC/2 + 0.4 V			
	IOVCC = 3.3 V	IOVCC/2 + 0.5 V			
Low-level input voltage, V_{IL}	IOVCC = 1.8 V			IOVCC/2 - 0.3 V	V
	IOVCC = 2.5 V			IOVCC/2 - 0.4 V	
	IOVCC = 3.3 V			IOVCC/2 - 0.5 V	
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		–40		85	°C
Virtual junction temperature, T_J				105	°C

6.4 Thermal Information

THERMAL METRIC[1]		DGG 56 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	63.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	15.9	
$R_{θJB}$	Junction-to-board thermal resistance	32.5	
$ψ_{JT}$	Junction-to-top characterization parameter	0.4	
$ψ_{JB}$	Junction-to-board characterization parameter	32.2	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_T	Input voltage threshold			IOVCC/2		V
$\lvert V_{OD}\rvert$	Differential steady-state output voltage magnitude	R_L = 100Ω, See Figure 7	250		450	mV
$\Delta\lvert V_{OD}\rvert$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100Ω, See Figure 7		1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 7 $t_{R/F}$ (Dx, CLKin) = 1ns	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 7 $t_{R/F}$ (Dx, CLKin) = 1ns			35	mV
I_{IH}	High-level input current	V_{IH} = IOVCC			25	μA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	μA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	μA
R_{pdn}	Input pull-down integrated resistor on all inputs (Dx, CLKSEL, $\overline{SHTDN}$, CLKIN)	IOVCC = 1.8 V		200		kΩ
		IOVCC = 3.3 V		100		kΩ
I_Q	Quiescent current (average)	disabled, all inputs at GND; $\overline{SHTDN}$ = V_{IL}		2	100	μA
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), grayscale pattern (Figure 8) VCC = 3.3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)} + I_{(PLLVCC)} + I_{(LVDSVCC)}$		51.9		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.4		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.1		mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), 50% transition density pattern (Figure 8), VCC = 3.3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)} + I_{(PLLVCC)} + I_{(LVDSVCC)}$		53.3		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.6		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.2		mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 9), VCC = 3.6 V, f_{CLK} = 75 MHz				
		$I_{(VCC)} + I_{(PLLVCC)} + I_{(LVDSVCC)}$		63.7		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		1.3		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.5		mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 9), f_{CLK} = 100 MHz				
		$I_{(VCC)} + I_{(PLLVCC)} + I_{(LVDSVCC)}$		81.6		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		1.6		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.6		mA
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 9), f_{CLK} = 135 MHz				
		$I_{(VCC)} + I_{(PLLVCC)} + I_{(LVDSVCC)}$		102.2		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		2.1		mA
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.8		mA
C_I	Input capacitance			2		pF

(1) All typical values are at VCC = 3.3 V, T_A = 25°C.

6.6 Timing Requirements

PARAMETER		MIN	MAX	UNIT
Input clock period, t_c		7.4	100	ns
Input clock modulation	with modulation frequency 30 kHz		8%	
	with modulation frequency 50 kHz		6%	
High-level input clock pulse width duration, t_w		0.4 t_c	0.6 t_c	ns
Input signal transition time, t_t			3	ns
Data set up time, D0 through D27 before CLKIN (See Figure 6)		2		ns
Data hold time, D0 through D27 after CLKIN		0.8		ns

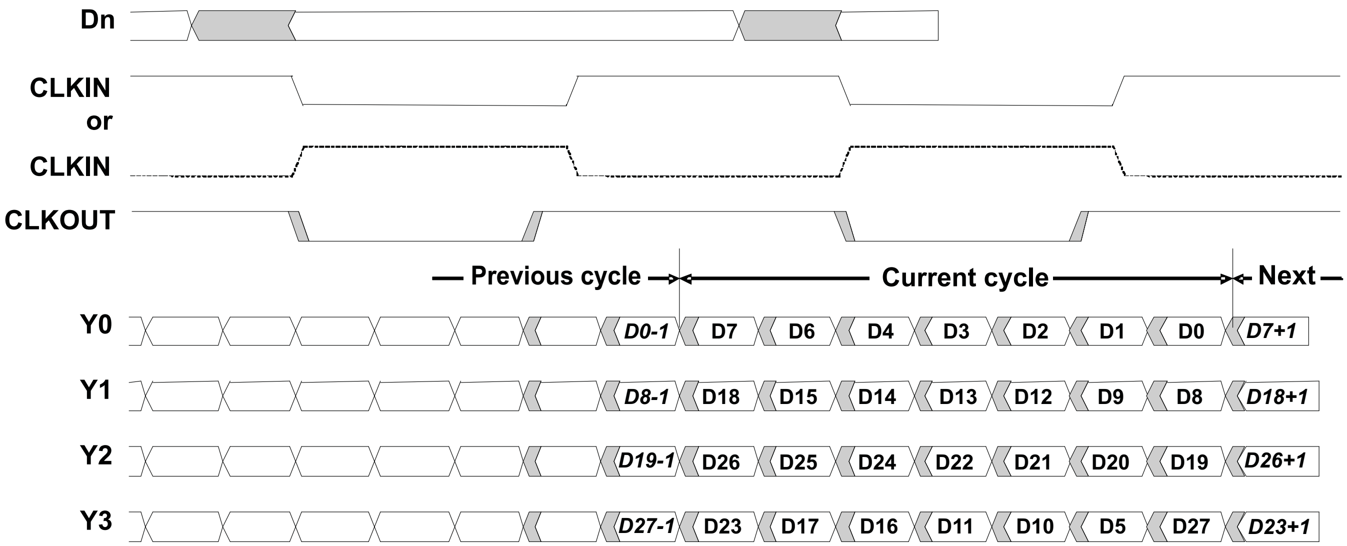


Figure 1. Typical SN65LVDS93A-Q1 Load and Shift Sequences

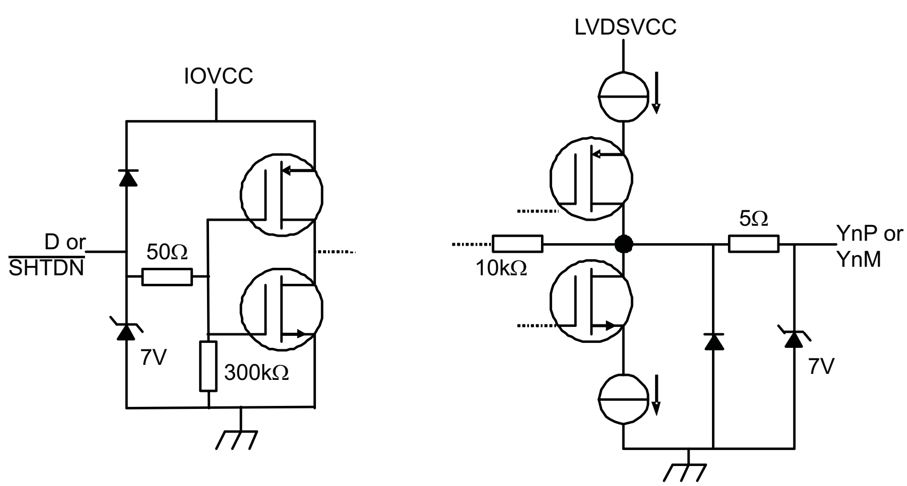


Figure 2. Equivalent Input and Output Schematic Diagrams

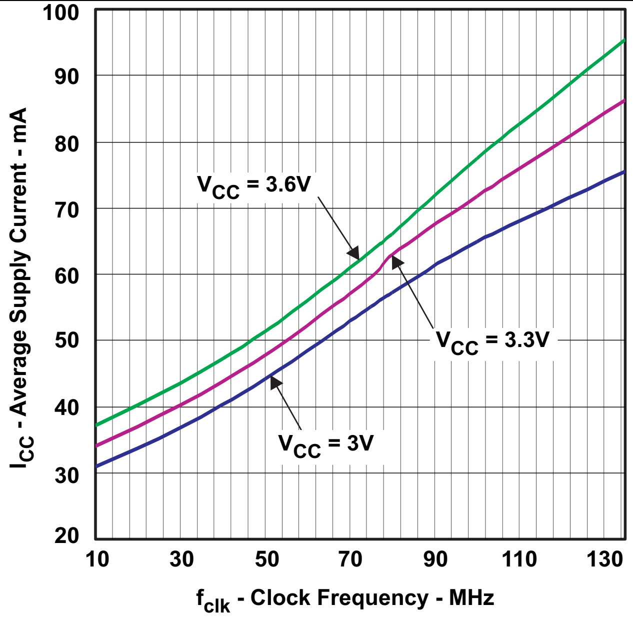
6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	See Figure 10, t_C = 10ns, |Input clock jitter| < 25ps (2)	-0.1	0	0.1	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)		$^1/_7\ t_c$ - 0.1		$^1/_7\ t_c$ + 0.1	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)		$^2/_7\ t_c$ - 0.1		$^2/_7\ t_c$ + 0.1	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)		$^3/_7\ t_c$ - 0.1		$^3/_7\ t_c$ + 0.1	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)		$^4/_7\ t_c$ - 0.1		$^4/_7\ t_c$ + 0.1	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)		$^5/_7\ t_c$ - 0.1		$^5/_7\ t_c$ + 0.1	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)		$^6/_7\ t_c$ - 0.1		$^6/_7\ t_c$ + 0.1	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter (3)	t_C = 10ns; clean reference clock, see Figure 11		±26		ps
		t_C = 10ns with 0.05UI added noise modulated at 3MHz, see Figure 11		±44		
		t_C = 7.4ns; clean reference clock, see Figure 11		±35		
		t_C = 7.4ns with 0.05UI added noise modulated at 3MHz, see Figure 11		±42		
t_w	High-level output clock pulse duration			$^4/_7\ t_c$		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	See Figure 7		225	500	ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$↑ to phase lock (Yn valid)	$f_{(clk)}$ = 135 MHz, See Figure 12		6		µs
t_{dis}	Disable time, $\overline{\text{SHTDN}}$↓ to off-state (CLKOUT high-impedance)	$f_{(clk)}$ = 135 MHz, See Figure 13		7		ns

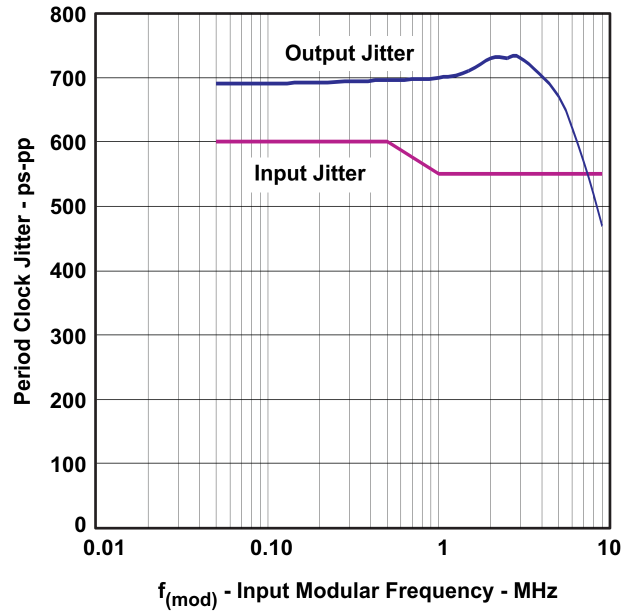
(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

6.8 Typical Characteristics



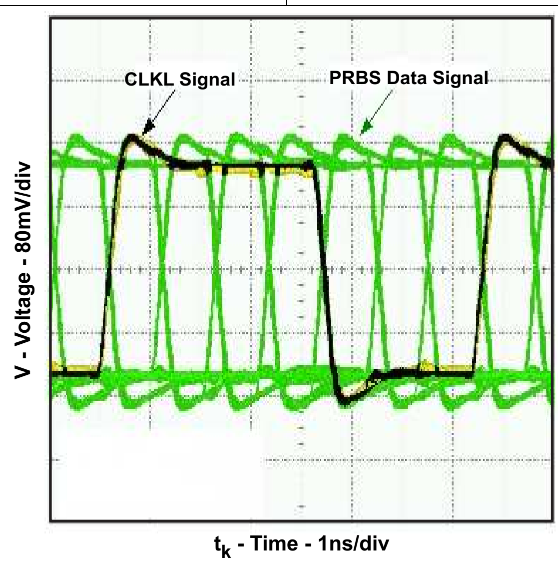
Total Device Current (Using Grayscale pattern) Over Pixel Clock Frequency

Figure 3. Average Grayscale I_{CC} vs Clock Frequency



CLK Frequency During Test = 100 MHz

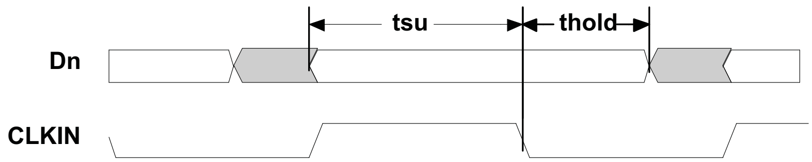
Figure 4. Output Clock Jitter vs Input Clock Jitter



Clock Signal = 135 MHz

Figure 5. Typical PRBS Output Signal Over One Clock Period

7 Parameter Measurement Information



All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns.
CLKSEL = 0 V.

Figure 6. Set Up and Hold Time Definition

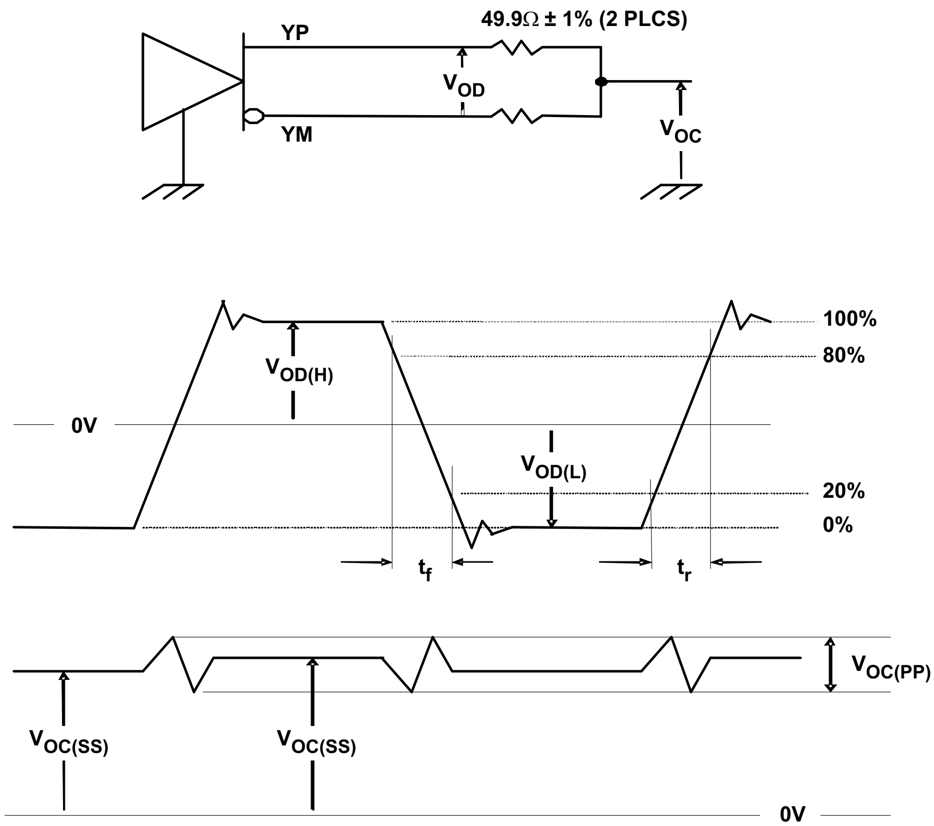
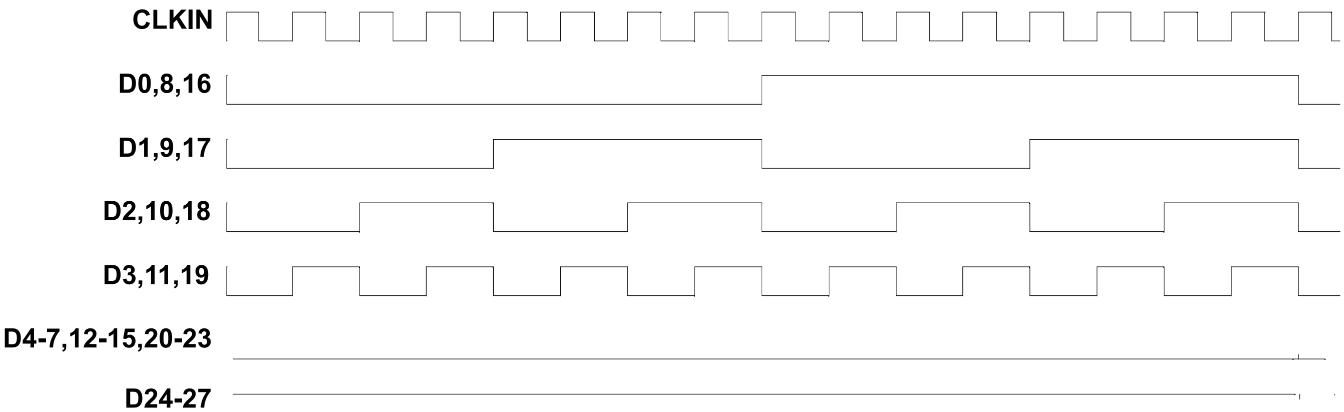


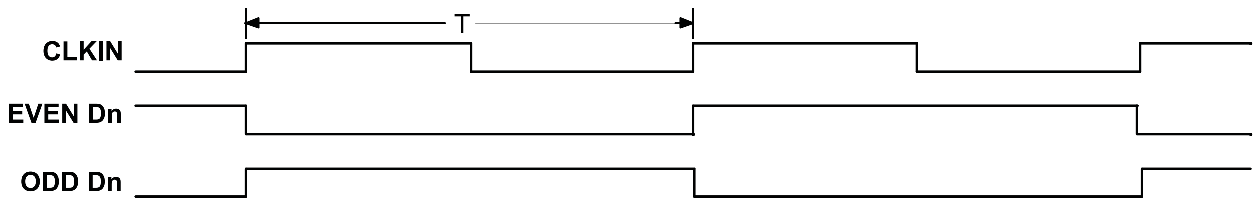
Figure 7. Test Load and Voltage Definitions for LVDS Outputs

Parameter Measurement Information (continued)



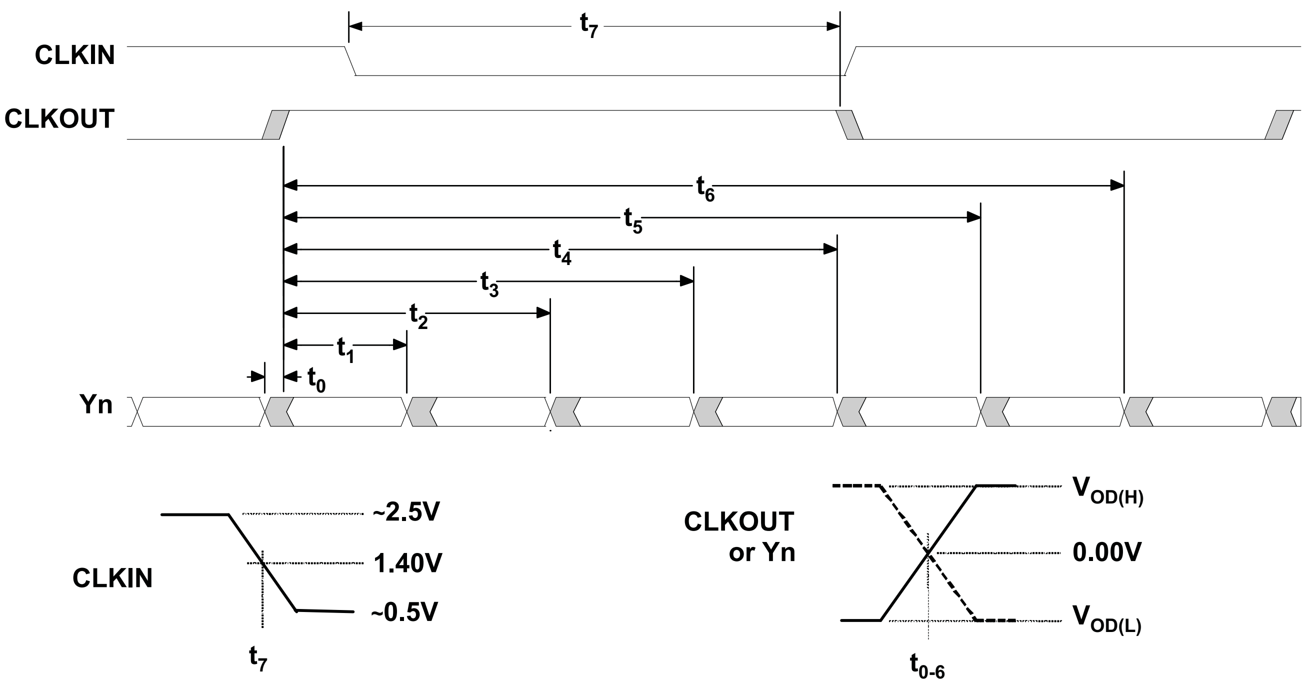
The 16 grayscale test pattern test device power consumption for a typical display pattern.

Figure 8. 16 Grayscale Test Pattern



The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

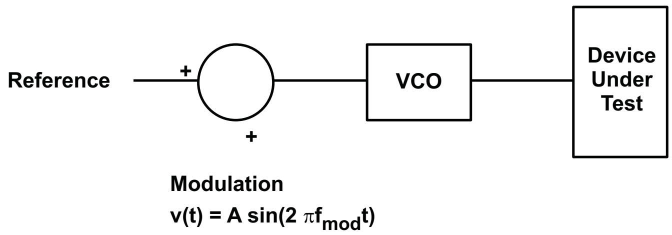
Figure 9. Worst-Case Power Test Pattern



CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 10. SN65LVDS93A-Q1 Timing Definitions

Parameter Measurement Information (continued)



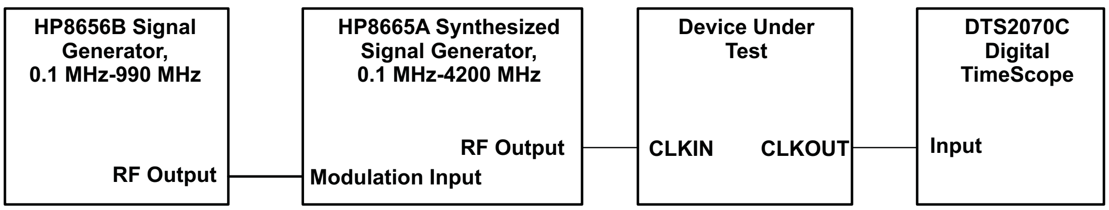


Figure 11. Output Clock Jitter Test Set Up

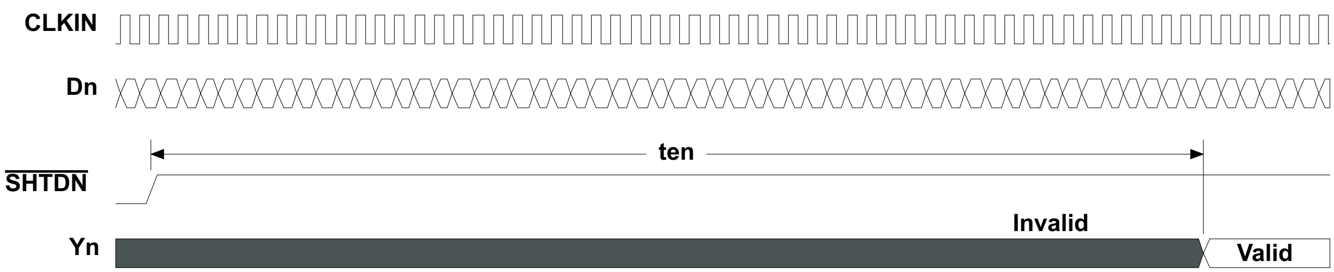


Figure 12. Enable Time Waveforms

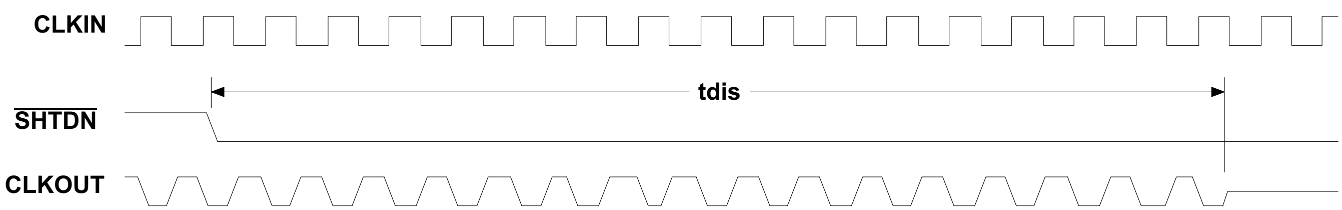


Figure 13. Disable Time Waveforms

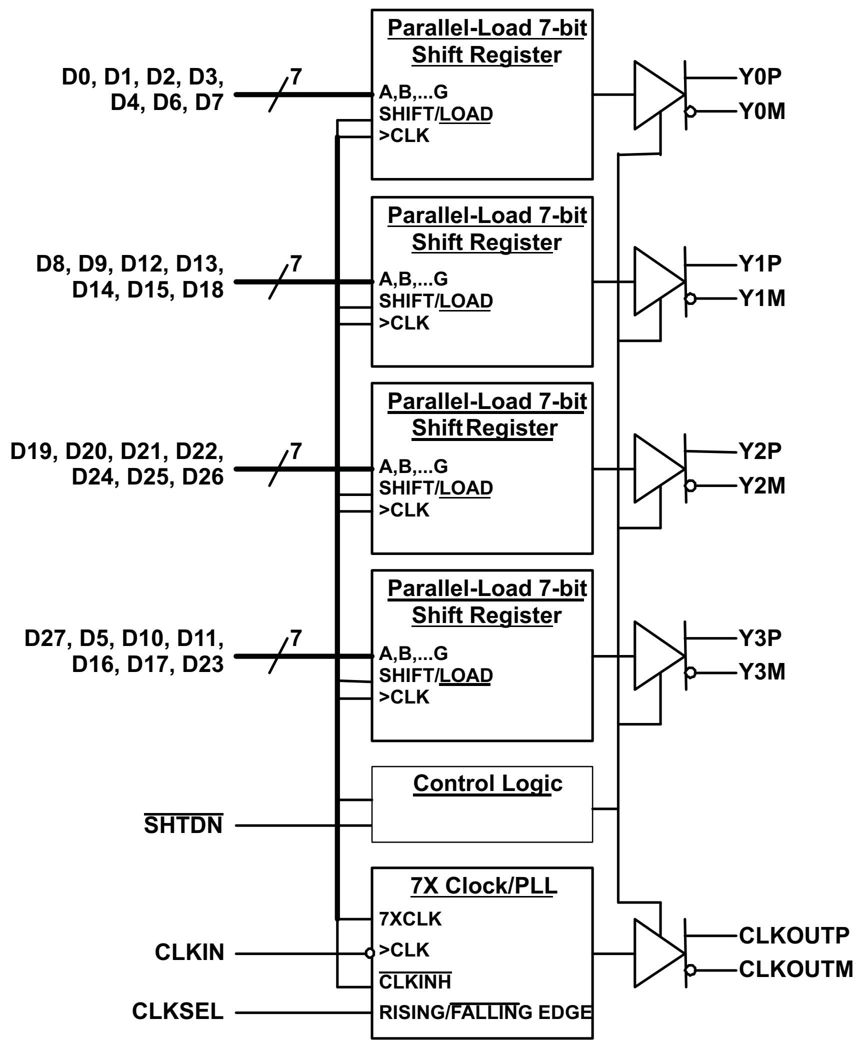
8 Detailed Description

8.1 Overview

FlatLink™ is an LVDS SerDes data transmission system. The SN65LVDS93A-Q1 takes in three (or four) data words each containing seven single-ended data bits and converts this to an LVDS serial output. Each serial output runs at seven times that of the parallel data rate. The deserializer (receiver) device operates in the reverse manner. The three (or four) LVDS serial inputs are transformed back to the original seven-bit parallel single-ended data. FlatLink™ devices are available in 21:3 or 28:4 SerDes ratios.

- The 21-bit devices are designed for 6-bit RGB video for a total of 18 bits in addition to three extra bits for horizontal synchronization, vertical synchronization, and data enable.
- The 28-bit devices are intended for 8-bit RGB video applications. Again, the extra four bits are for horizontal synchronization, vertical synchronization, data enable, and the remaining is the reserved bit. These 28-bit devices can also be used in 6-bit and 4-bit RGB applications as shown in the subsequent system diagrams.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit. The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the SN65LVDS93A-Q1 and can connect directly to low-power, low-voltage application and graphic processors. The bit mapping is listed in Table 1.

Table 1. Pixel Bit Ordering

	RED	GREEN	BLUE
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

8.3.2 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE

Table 2. Pixel Data Assignment (continued)

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

8.4 Device Functional Modes

8.4.1 Input Clock Edge

The transmission of data bits D0 through D27 occurs as each are loaded into registers upon the edge of the CLKIN signal, where the rising or falling edge of the clock may be selected via CLKSEL. The selection of a clock rising edge occurs by inputting a high level to CLKSEL, which is achieved by populating pull-up resistor to pull CLKSEL=high. Inputting a low level to select a clock falling edge is achieved by directly connecting CLKSEL to GND.

8.4.2 Low Power Mode

The SN65LVDS93A-Q1 can be put in low-power consumption mode by active-low input SHTDN#. Connecting pin SHTDN# to GND will inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level. Populate a pull-up to VCC on SHTDN# to enable the device for normal operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section describes the power up sequence, provides information on device connectivity to various GPU and LCD display panels, and offers a PCB routing example.

9.2 Typical Application

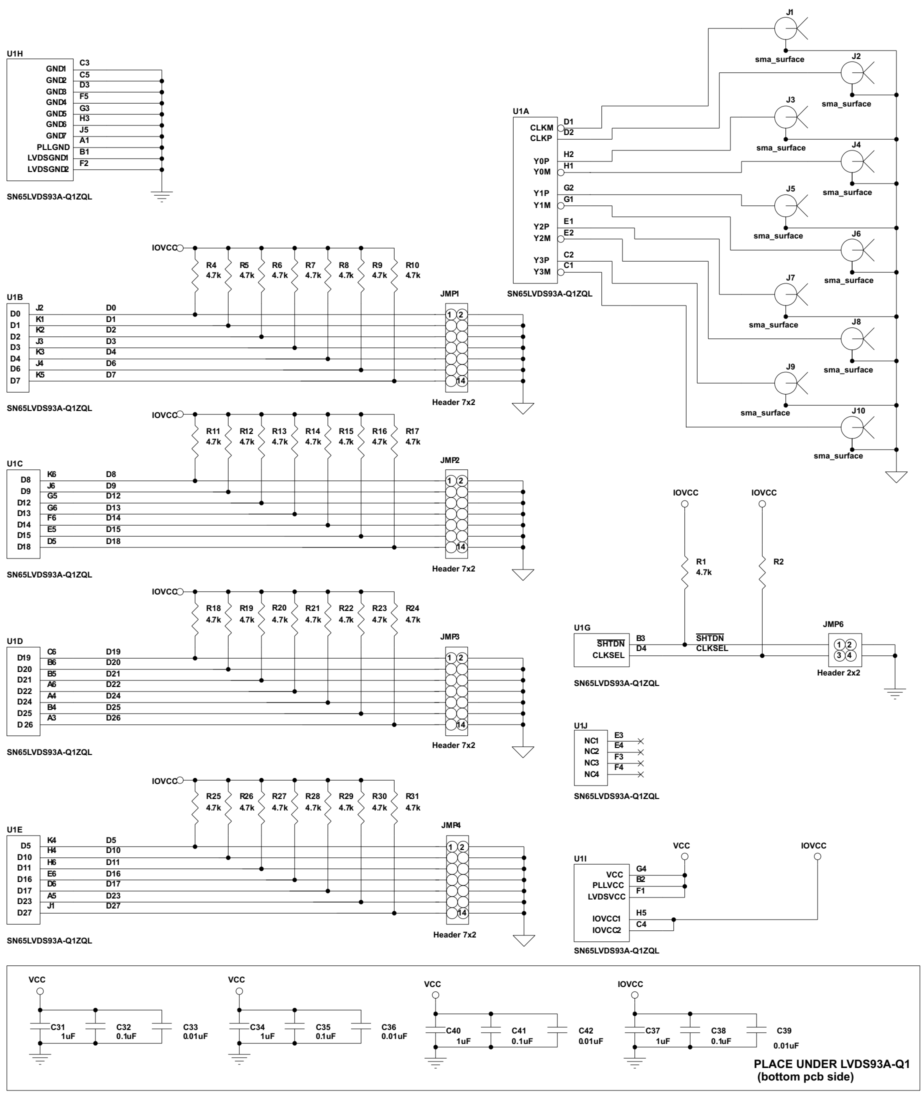


Figure 14. Schematic Example (SN65LVDS93A-Q1 Evaluation Board)

Typical Application (continued)

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
VCC	3.3 V
VCCIO	1.8 V
CLKIN	Falling edge
SHTDN#	High
Format	18-bit GPU to 24-bit LCD

9.2.2 Detailed Design Procedure

9.2.2.1 Power Up Sequence

The SN65LVDS93A-Q1 does not require a specific power up sequence.

It is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the SHTDN during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

It is also permitted to power up all 3.3V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting SHTDN to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (SN65LVDS93A-Q1 $\overline{\text{SHTDN}}$ input initially low):

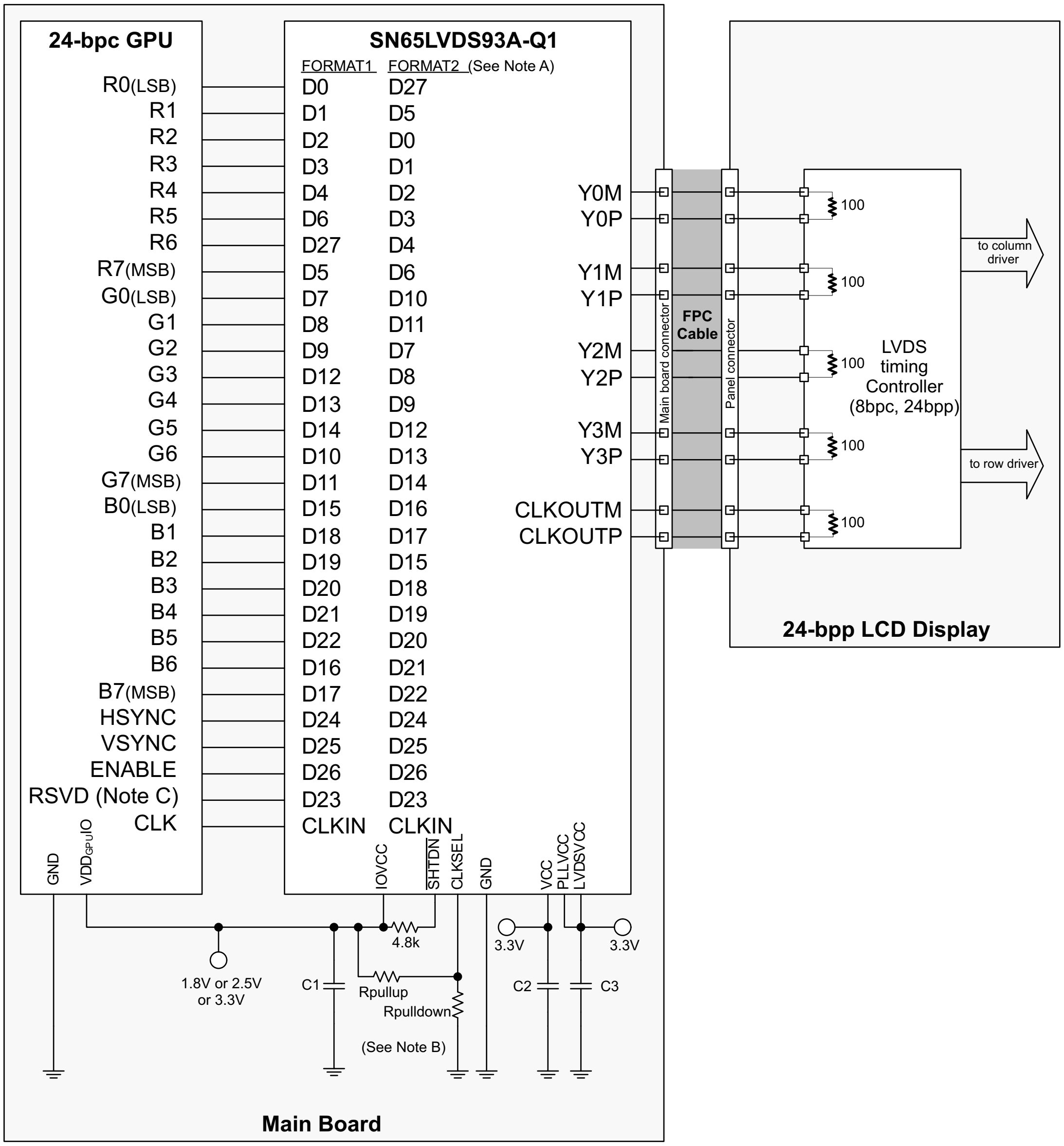
1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Enable video source output; start sending black video data.
4. Toggle SN65LVDS93A-Q1 shutdown to $\overline{\text{SHTDN}}$ = V_{IH}.
5. Send >1ms of black video data; this allows the SN65LVDS93A-Q1 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (SN65LVDS93A-Q1 $\overline{\text{SHTDN}}$ input initially high):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set SN65LVDS93A-Q1 input $\overline{\text{SHTDN}}$ = GND; wait for 250ns.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

9.2.2.2 Signal Connectivity

While there is no formal industry standardized specification for the input interface of LVDS LCD panels, the industry has aligned over the years on a certain data format (bit order). Figure 15 through Figure 18 show how each signal should be connected from the graphic source through the SN65LVDS93A-Q1 input, output and LVDS LCD panel input. Detailed notes are provided with each figure.



Note A. **FORMAT**: The majority of 24-bit LCD display panels require the two most significant bits (2 MSB) of each color to be transferred over the 4th serial data output Y3. A few 24-bit LCD display panels require the two LSBs of each color to be transmitted over the Y3 output. The system designer needs to verify which format is expected by checking the LCD display data sheet.

- Format 1: use with displays expecting the 2 MSB to be transmitted over the 4th data channel Y3. This is the dominate data format for LCD panels.
- Format 2: use with displays expecting the 2 LSB to be transmitted over the 4th data channel.

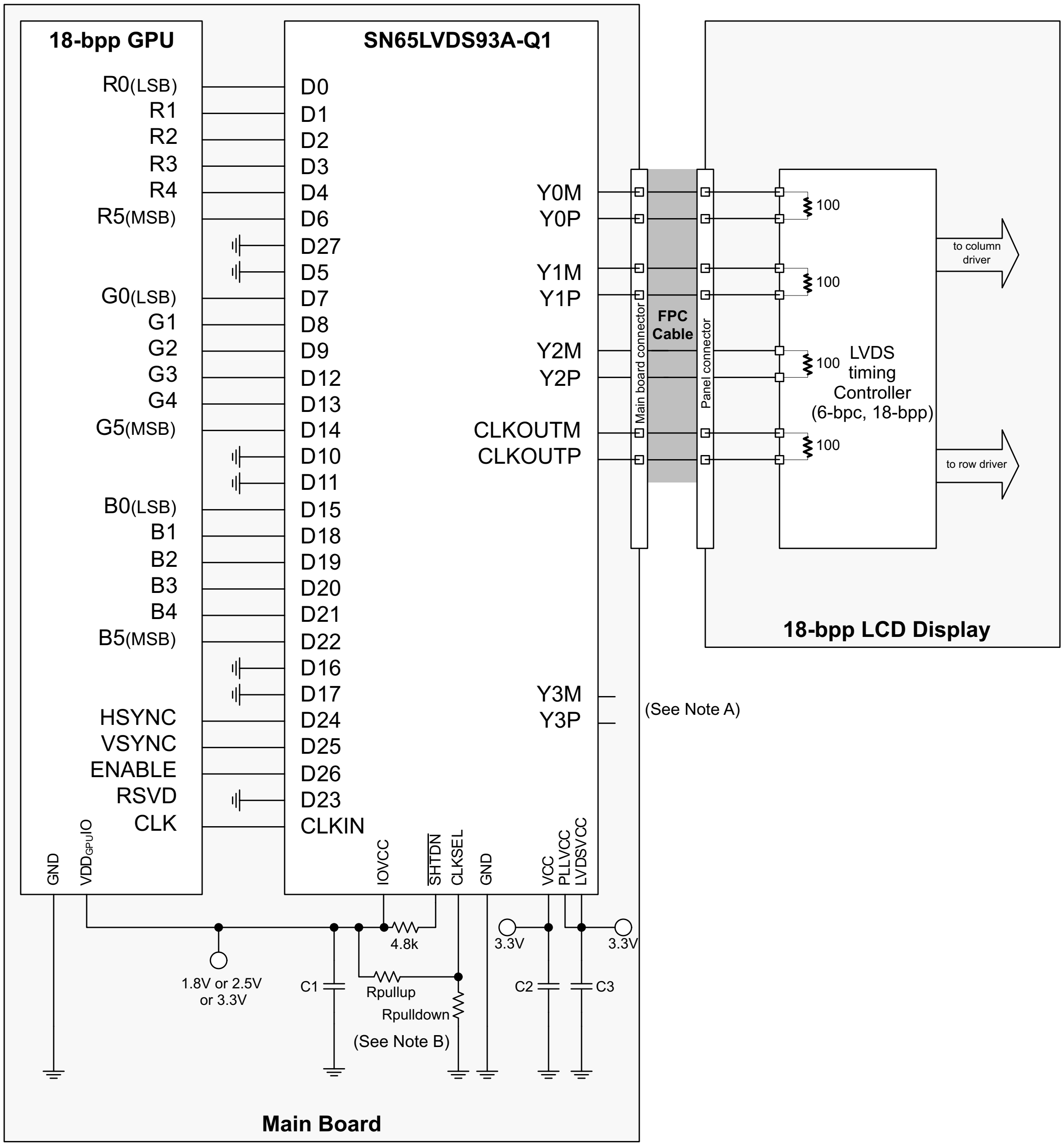
Note B. **Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Note C. If RSVD is not driven to a valid logic level, then an external connection to GND is recommended.

Note D. RSVD must be driven to a valid logic level. All unused SN65LVDS93A-Q1 inputs must be tied to a valid logic level.

Figure 15. 24-Bit Color Host to 24-Bit LCD Panel Application

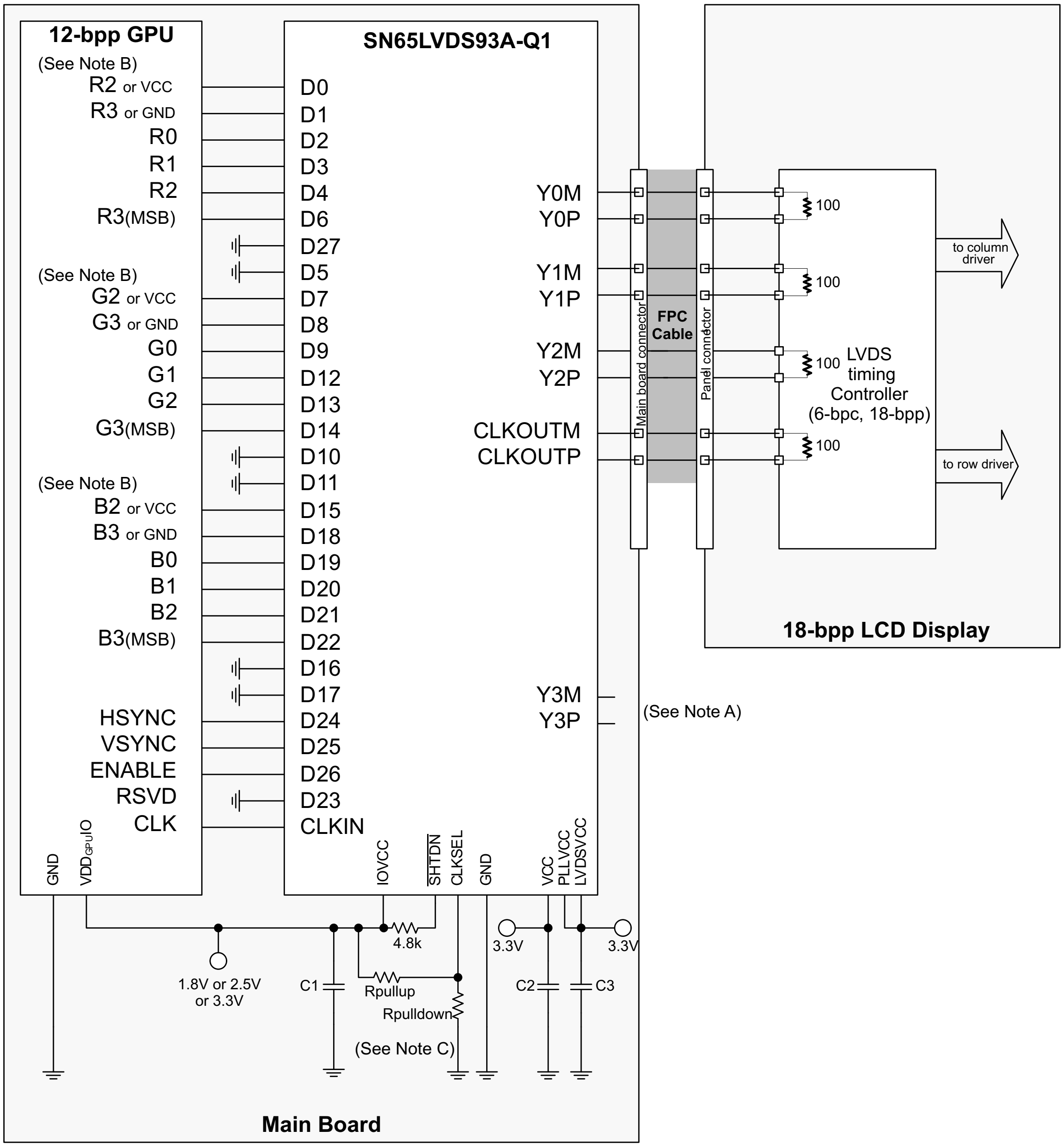


Note A. Leave output Y3 NC.

Note B.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 16. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application



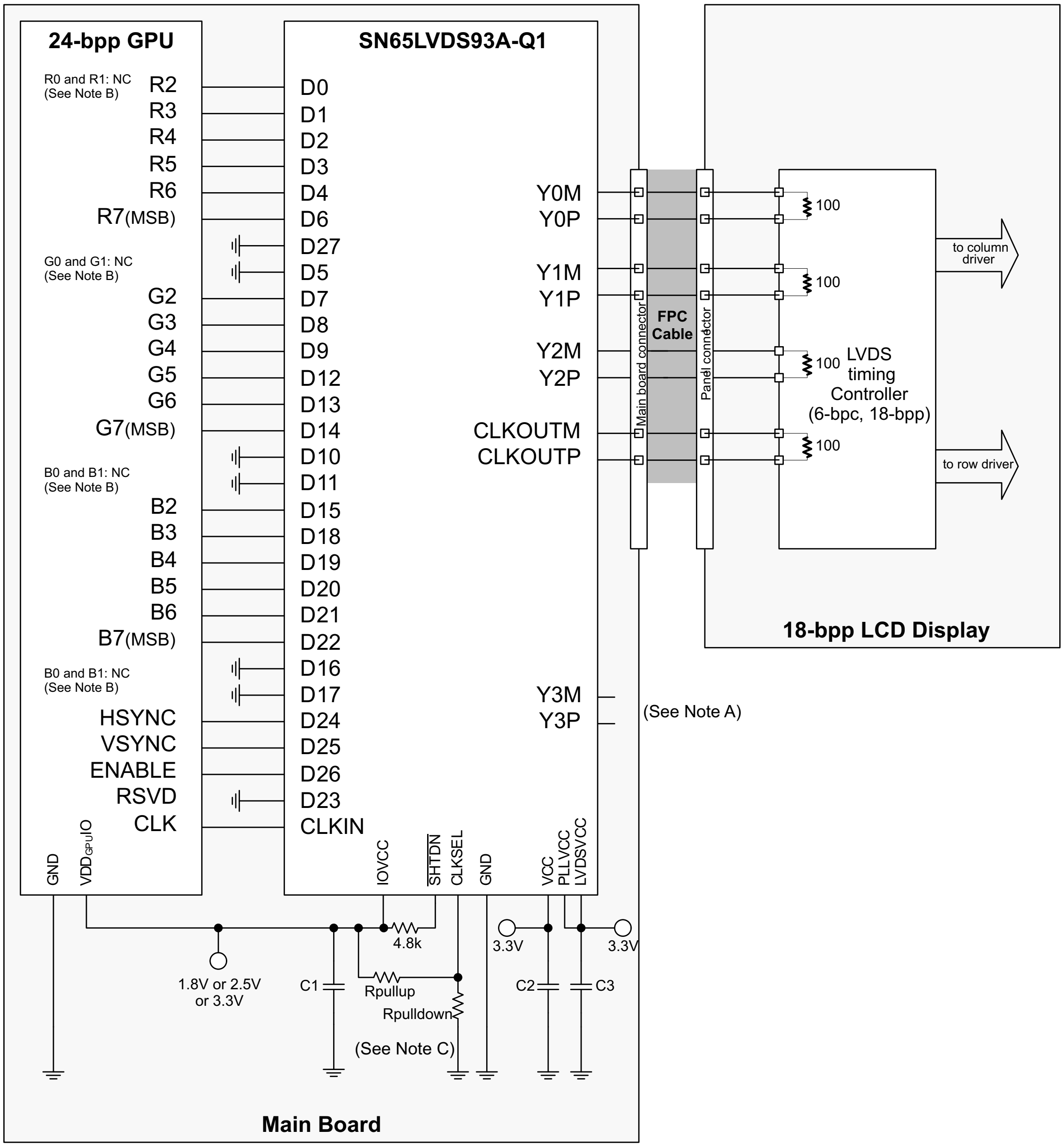
Note A. Leave output Y3 N.C.

Note B. **R3, G3, B3**: this MSB of each color also connects to the 5th bit of each color for increased dynamic range of the entire color space at the expense of none-linear step sizes between each step. For linear steps with less dynamic range, connect D1, D8, and D18 to GND.
R2, G2, B2: these outputs also connects to the LSB of each color for increased, dynamic range of the entire color space at the expense of none-linear step sizes between each step. For linear steps with less dynamic range, connect D0, D7, and D15 to VCC.

Note C.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 17. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application



Note A. Leave output Y3 NC.

Note B. **R0, R1, G0, G1, B0, B1**: For improved image quality, the GPU should dither the 24-bit output pixel down to18-bit per pixel.

NoteC.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 18. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

9.2.2.3 PCB Routing

Figure 19 shows a possible breakout of the data input and output signals on two layers of a printed circuit board.

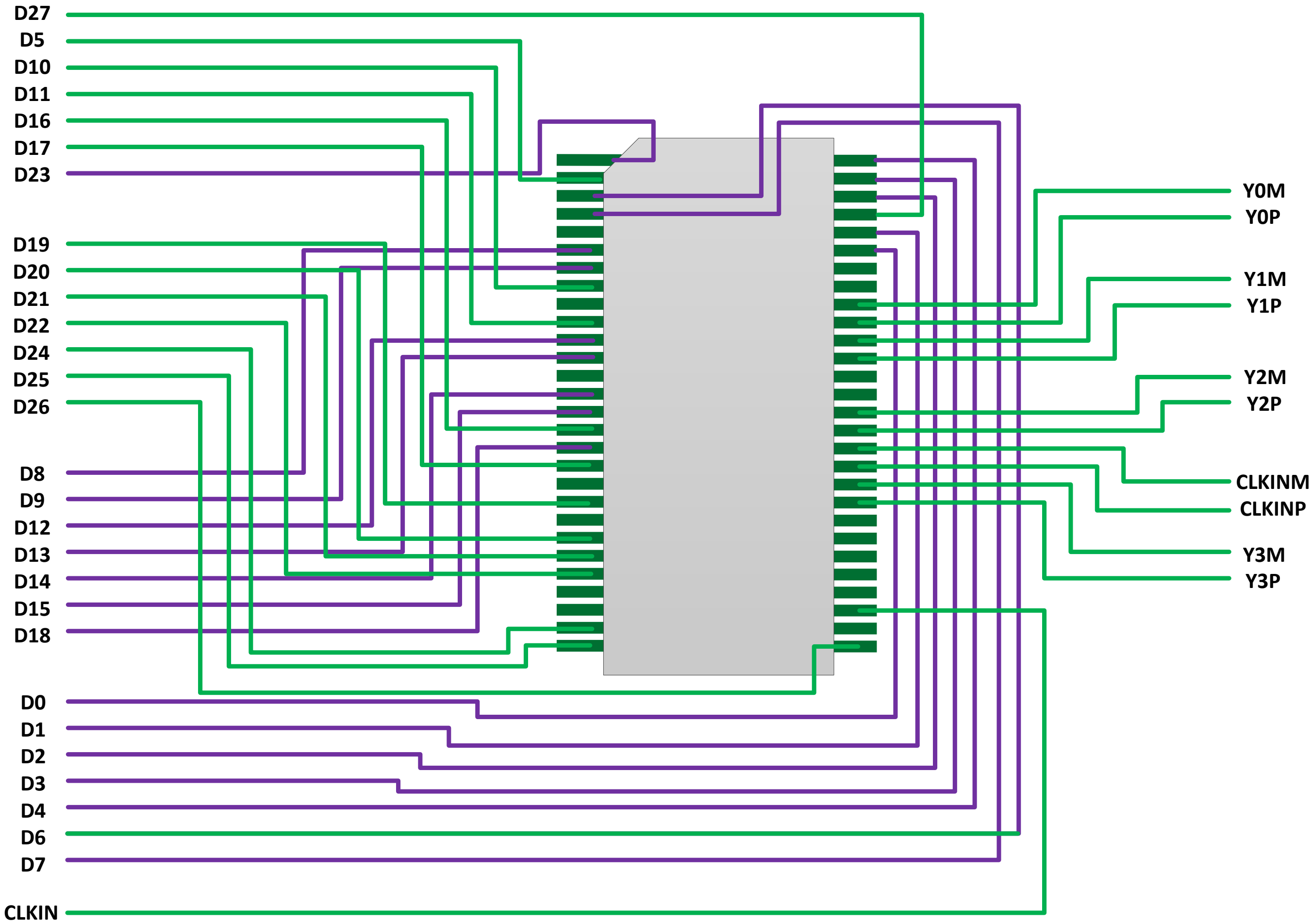


Figure 19. Printed Circuit Board Routing Example (See Figure 14 for the Schematic)

9.2.3 Application Curve

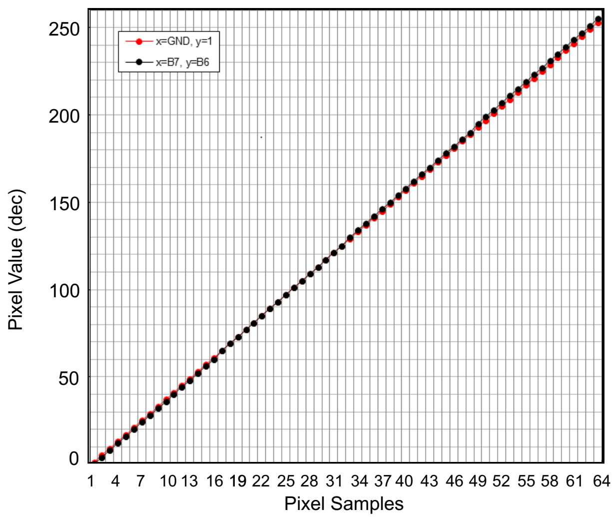


Figure 20. 18b GPU to 24b LCD

10 Power Supply Recommendations

Power supply PLL, IO, and LVDS pins must be uncoupled from each.

11 Layout

11.1 Layout Guidelines

11.1.1 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine *Elektronik Praxis* has published an article with an analysis of different board stackups. These are listed in Table 3. Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

Table 3. Possible Board Stackup on a Four-Layer PCB

	MODEL 1	MODEL 2	MODEL 3	MODEL 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal Integrity	Bad	Bad	Good	Bad
Self Disturbance	Satisfaction	Satisfaction	Satisfaction	High

11.1.2 Power and Ground Planes

A complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. What are the alternatives? Split the ground planes and the power planes? In a mixed-signal design, e.g., using data converters, the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part. Take care when using split ground planes because:

- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane (Figure 21).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (Figure 22).

For Figure 22, do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

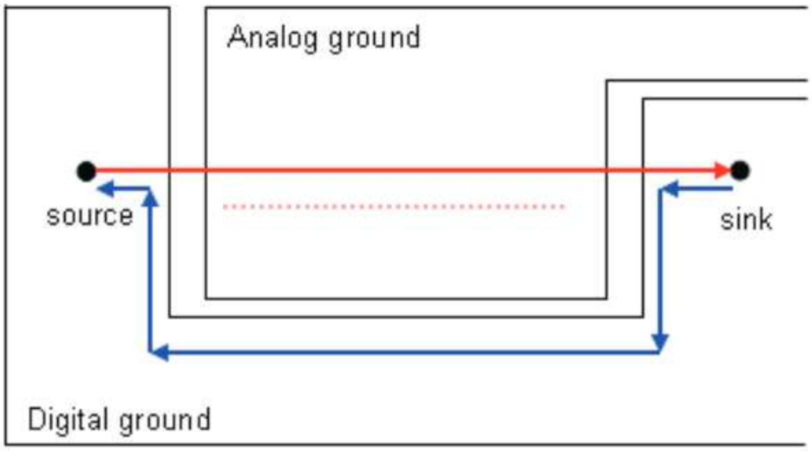


Figure 21. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

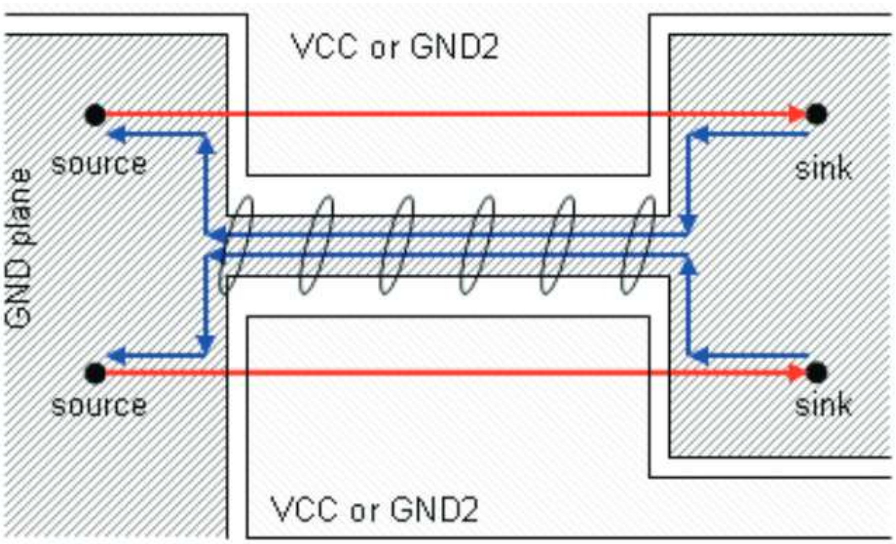


Figure 22. Crosstalk Induced by the Return Current Path

11.1.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 23).
- Separate high-speed signals (e.g., clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

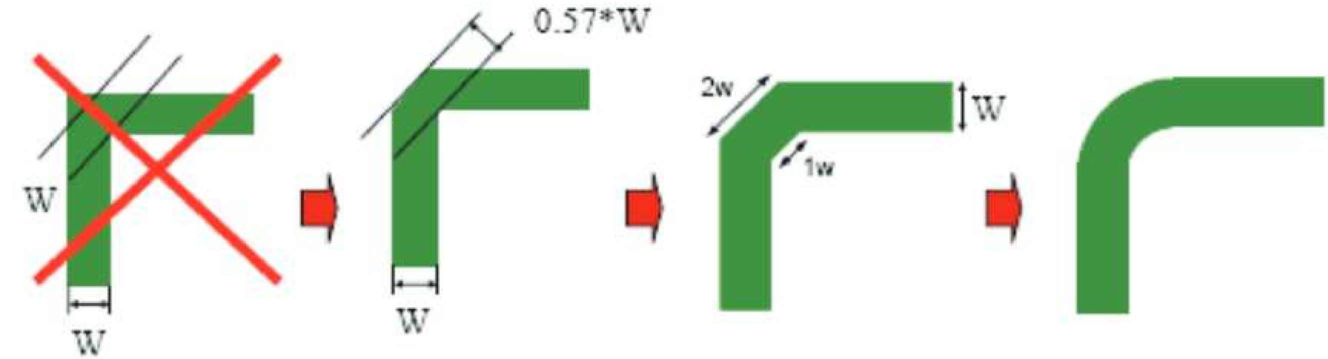


Figure 23. Poor and Good Right Angle Bends

11.2 Layout Example

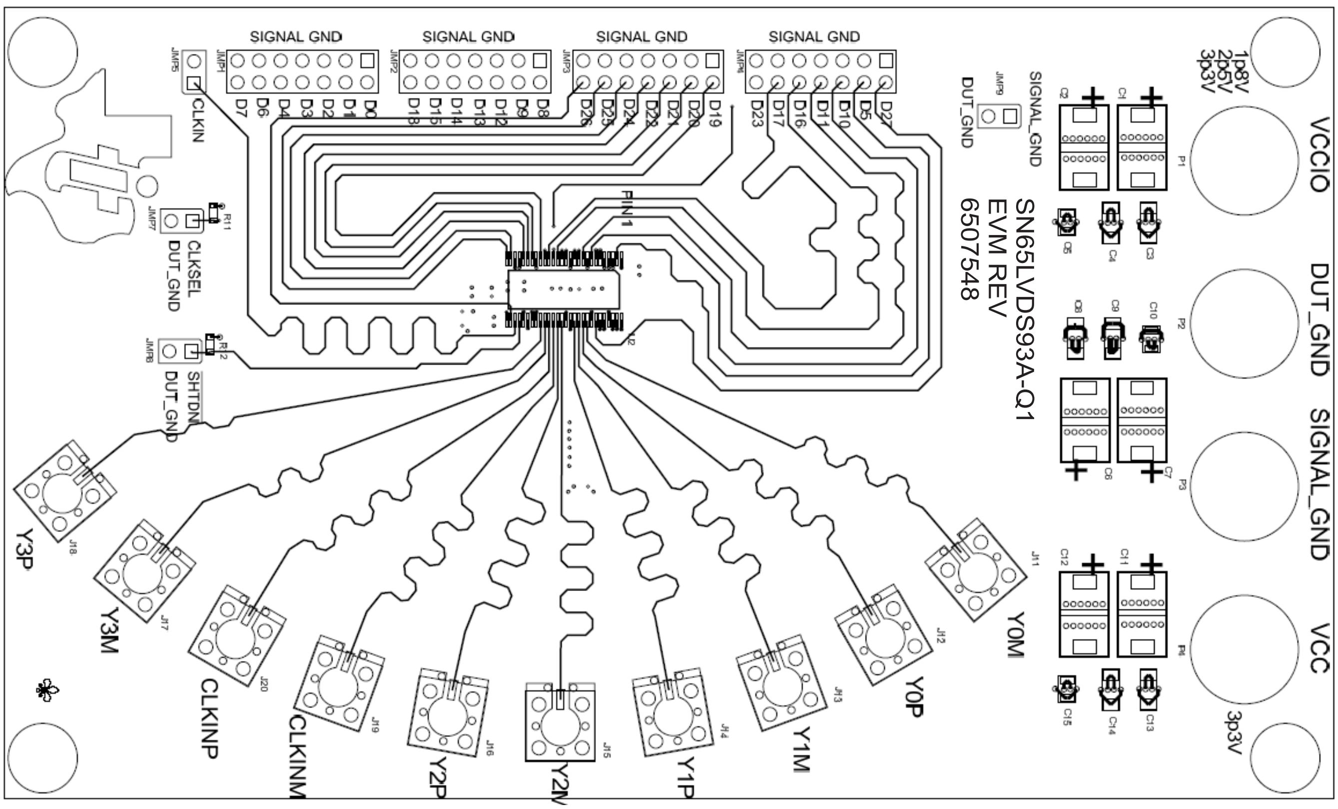


Figure 24. SN65LVDS93A-Q1 EVM Top Layer – TSSOP Package

Layout Example (continued)

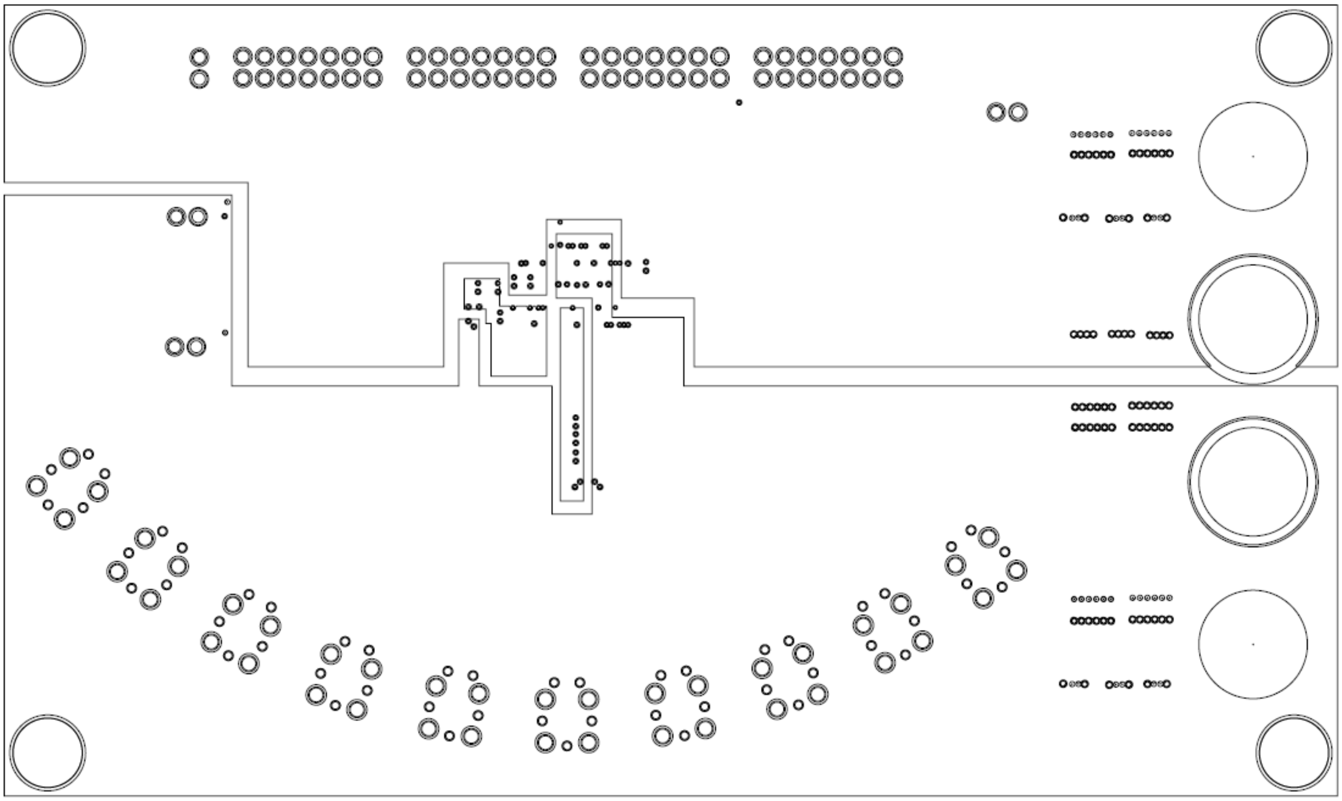


Figure 25. SN65LVDS93A-Q1 EVM VCC Layer – TSSOP Package

12 器件和文档支持

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12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS93AIDGGRQ1	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

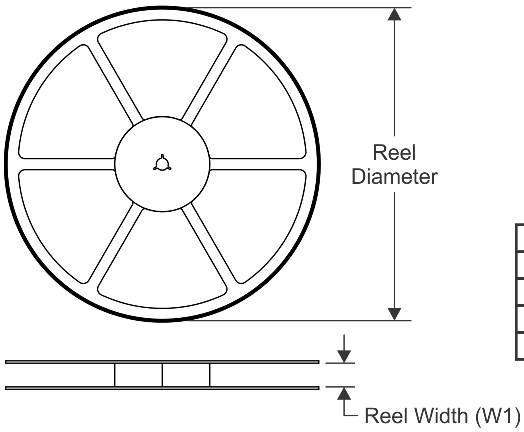
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

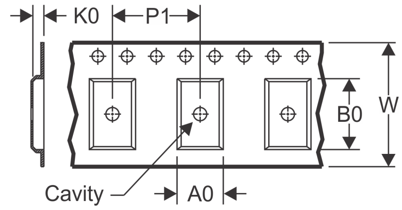
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

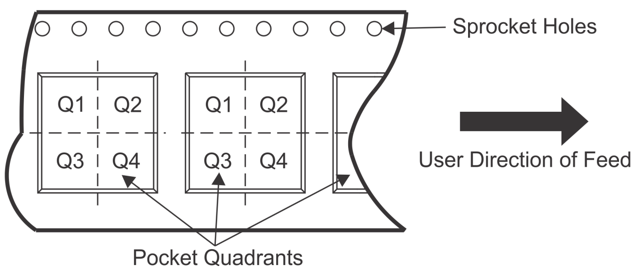


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

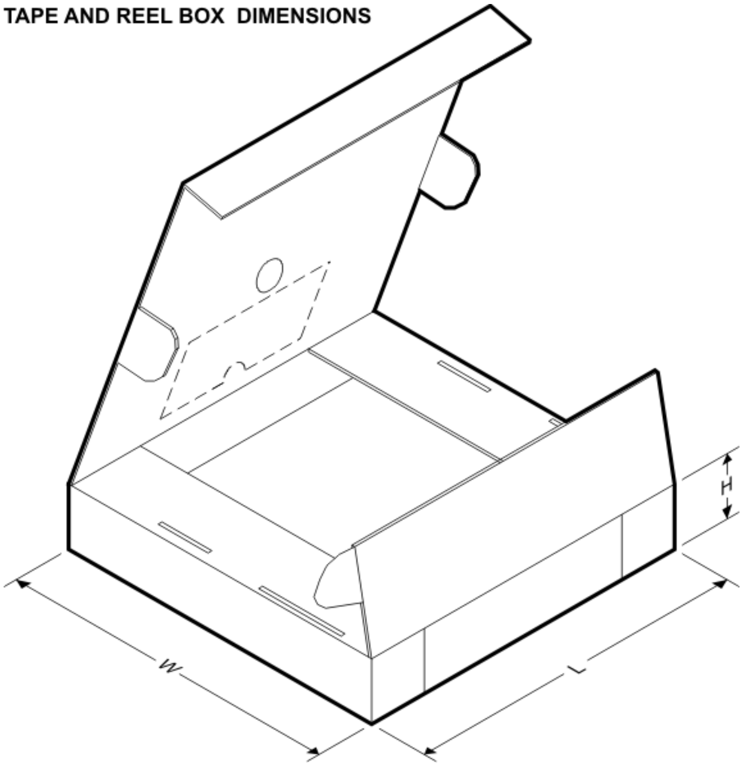
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

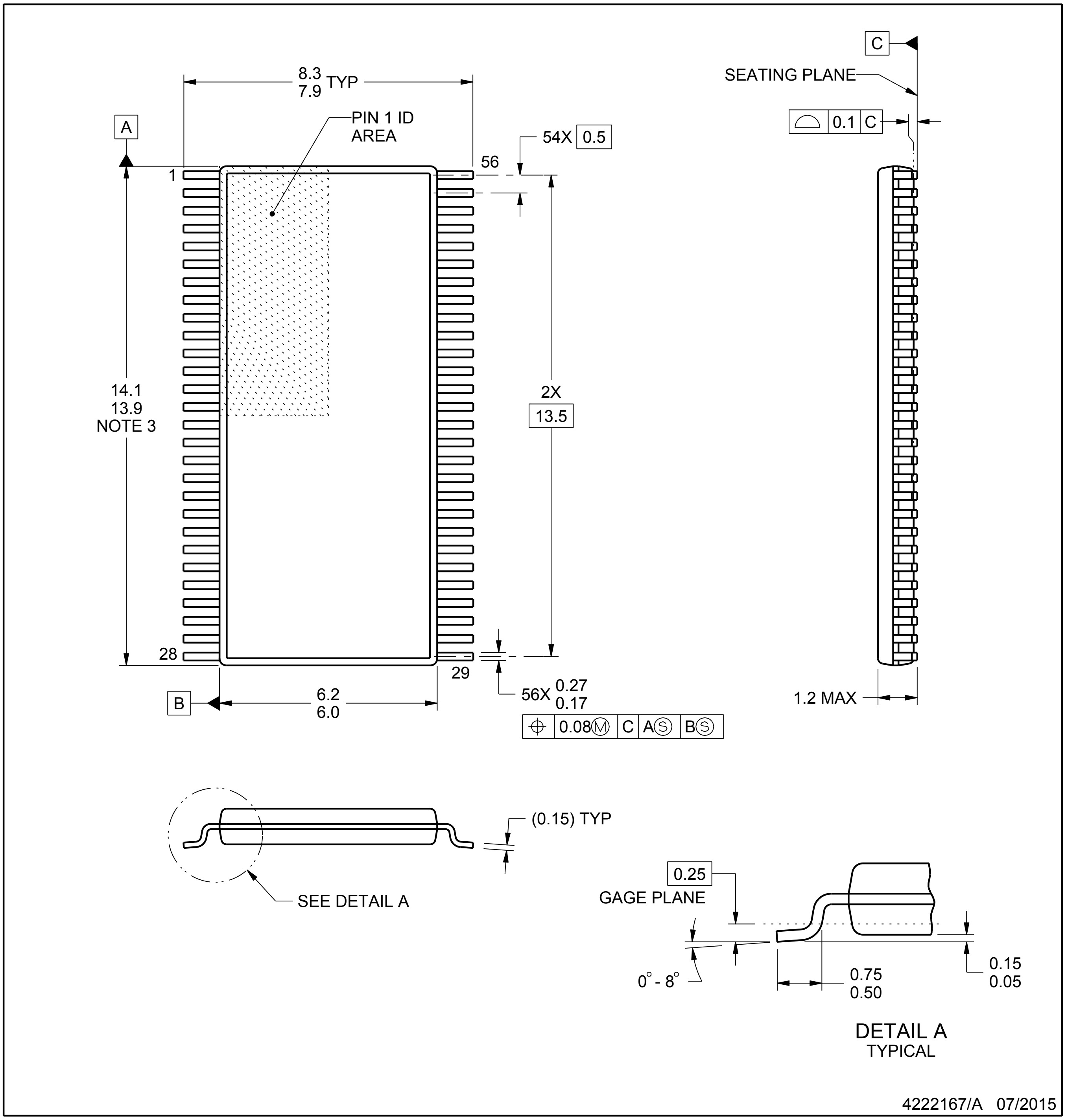
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS93AIDGGRQ1	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



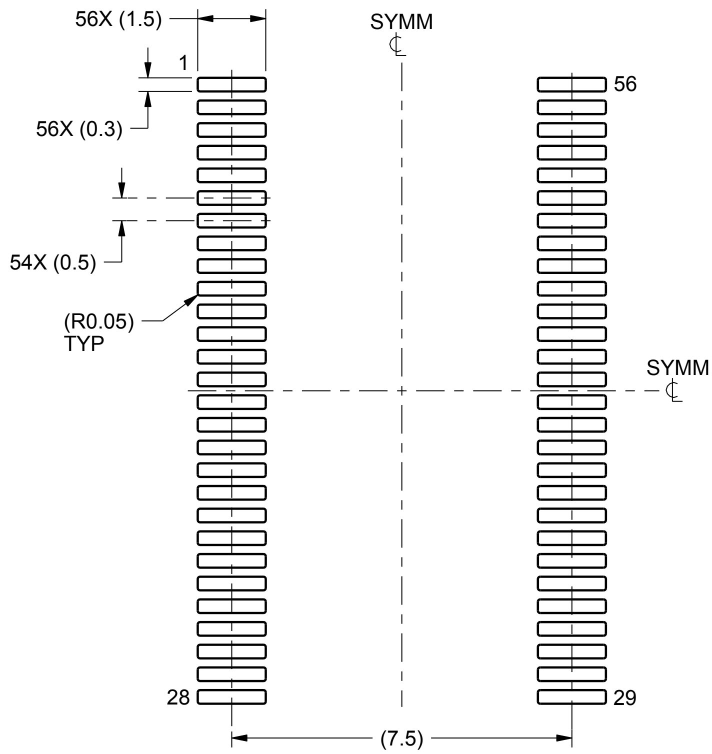
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS93AIDGGRQ1	TSSOP	DGG	56	2000	367.0	367.0	45.0

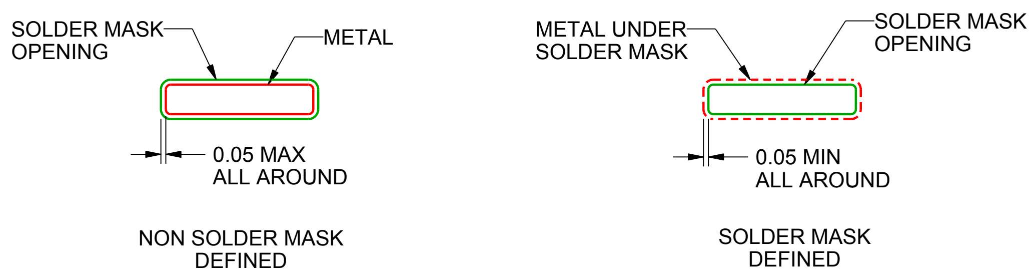


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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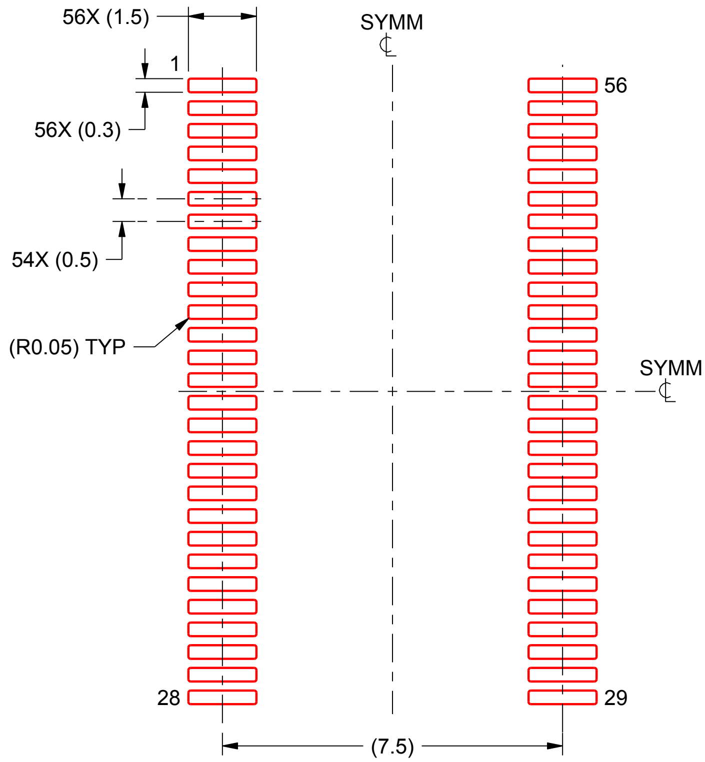
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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