具有视频分离功能的 DS90UB941AS-Q1 2K DSI 转 FPD-Link III 桥接串行器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准 的下列特性：
  - 器件温度 2 级：环境工作温度范围为 −40℃ 至 +105℃
- 针对具有 24 位色深的 30Hz、3K (2880x1620)、QXGA (2048x1536)、2K (2880x1080)、WUXGA (1920x1200) 或 1080p60 (1920x1080) 分辨率，支持高达 210MHz 的像素时钟频率
- MIPI D-PHY/显示串行接口 (DSI) 接收器可提供用于连接到视频处理器或 FPGA 的高带宽接口
  - 双 DSI 输入端口，每个端口具有多达 4 个数据通道
  - 每个通道的速率高达 1.5Gbps
  - 具有对称和非对称解包功能的超级帧
  - ECC 和 CRC 生成
  - 虚拟通道功能
- 单路和双路 FPD-Link III 输出
  - 单链路：高达 105MHz 的像素时钟
  - 双链路：高达 210MHz 的像素时钟
- 对称和非对称视频分离

2 应用

- 汽车信息娱乐：
  - IVI 音响主机和 HMI 模块
  - 中央信息显示屏
  - 数字仪表组
  - 后座娱乐系统

3 说明

DS90UB941AS-Q1 是专为汽车信息娱乐应用设计的双 DSI 转 FPD-Link III 桥接串行器。在与 FPD-Link III DS90UB940N-Q1、DS90UB948-Q1、DS90UB924-Q1、DS90UB926Q-Q1 或 DS90UB928Q-Q1 解串器配合使用时，DS90UB941AS-Q1 可通过具有成本效益的 50Ω 单端同轴电缆或 100Ω 差分屏蔽双绞线 (STP) 和屏蔽四路绞线 (STQ) 电缆提供单通道或双通道高速串行流。为了应对信息娱乐系统中显示器数量和差异的增加，DS90UB941AS-Q1 可以支持对称和非对称分离。

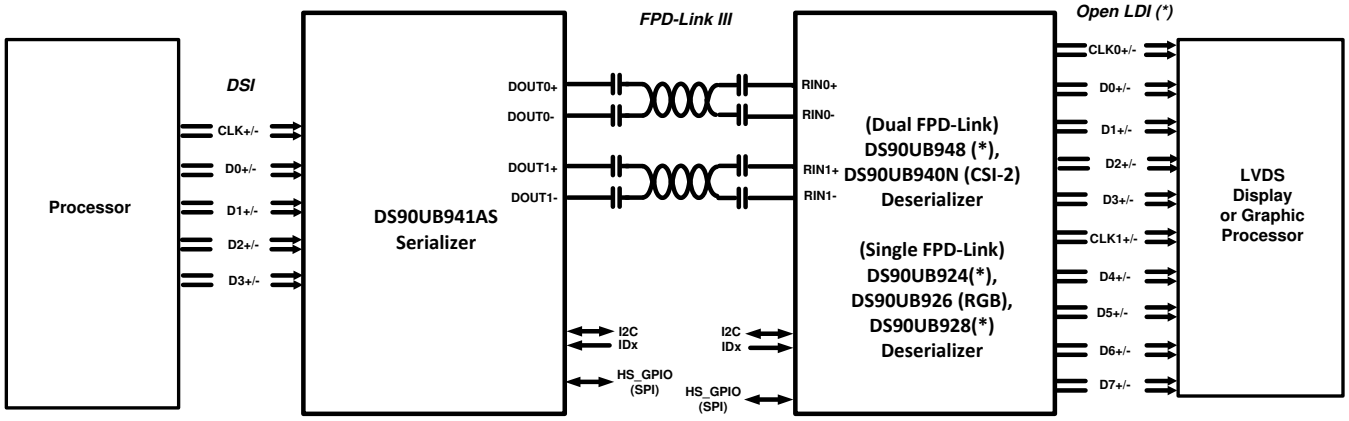
DS90UB941AS-Q1 可以通过两个差分对实现视频数据的整合，以简化系统设计并减小应用的互连线尺寸和重量。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS90UB941AS-Q1	VQFN (64)	9.00mm x 9.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

应用 图



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4 修订历史记录

Changes from Original (December 2018) to Revision A **Page**

- 将“预告信息”更改为“生产数据发布” ... 1

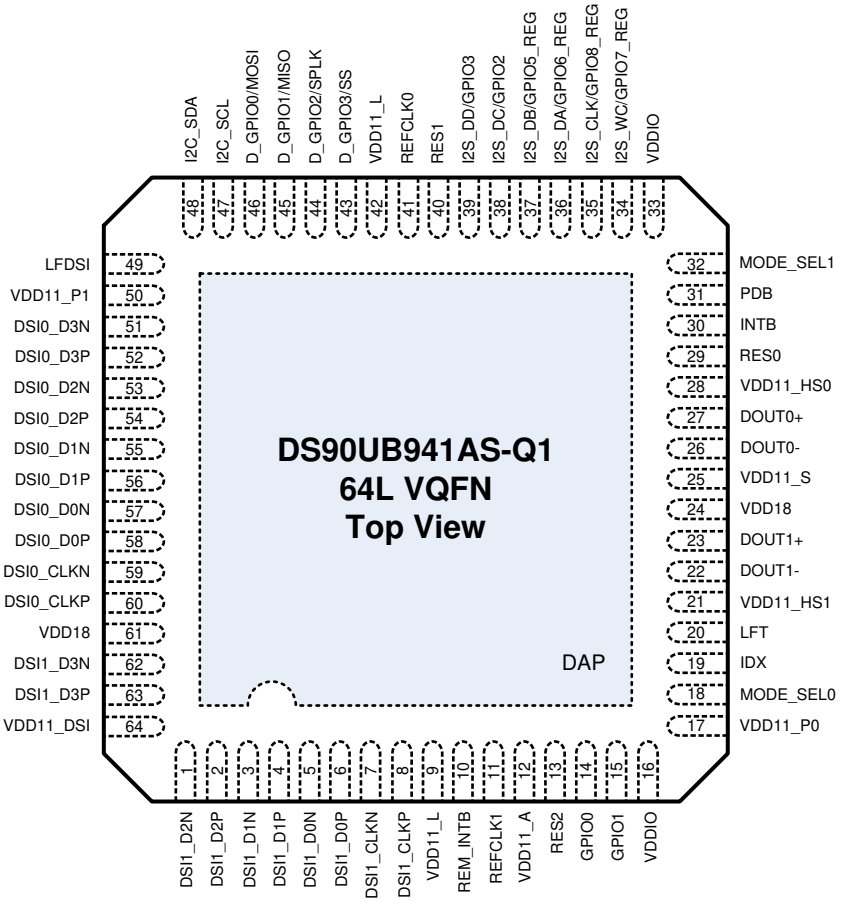
5 说明（续）

FPD-Link III 接口支持通过同一条高速串行链路进行视频和音频数据传输以及全双工控制（包括 I2C 通信和高达 8 个 I2S 音频通道）。通过使用低压差分信令、数据换序和随机生成最大限度地降低了 EMI。

DS90UB941AS-Q1 对 MIPI DSI 输入进行串行化处理，支持高达 2K、WUXGA 和 1080p60 的视频分辨率（24 位色深）。在向后兼容模式下，DS90UB941AS-Q1 在单一差分链路上最高可支持 WXGA 和 720p 分辨率（24 位色深）。

6 Pin Configuration and Functions

RTD Package
64-Pin VQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
MIPI DSI INPUT PINS			
DSI0_D0P	58	I	DSI RX Port 0 differential data input pins Use DEVICE_CFG (0x02h) and BRIDGE_CTL (0x4Fh) registers for the DSI RX control. If unused, these pins may be tied to Ground or left as No Connect pins.
DSI0_D0N	57	I	
DSI0_D1P	56	I	
DSI0_D1N	55	I	
DSI0_D2P	54	I	
DSI0_D2N	53	I	
DSI0_D3P	52	I	
DSI0_D3N	51	I	
DSI0_CLKP	60	I	DSI RX Port 0 differential clock input pins Use DEVICE_CFG (0x02h) and BRIDGE_CTL (0x4Fh) registers for the DSI RX control. If unused, these pins may be tied to Ground or left as No Connect pins.
DSI0_CLKN	59	I	

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
DSI1_D0P	6	I	DSI RX Port 1 differential data input pins Use DEVICE_CFG (0x02h) and BRIDGE_CTL (0x4Fh) registers for the DSI RX control. If unused, these pins may be tied to Ground or left as No Connect pins.
DSI1_D0N	5	I	
DSI1_D1P	4	I	
DSI1_D1N	3	I	
DSI1_D2P	2	I	
DSI1_D2N	1	I	
DSI1_D3P	63	I	
DSI1_D3N	62	I	
DSI1_CLKP	8	I	DSI RX Port 1 differential clock input pins Use DEVICE_CFG (0x02h) and BRIDGE_CTL (0x4Fh) registers for the DSI RX control. If unused, these pins may be tied to Ground or left as No Connect pins.
DSI1_CLKN	7	I	
LFDSI	49	D	DSI Loop Filter pin Connect a 10 nF capacitor between this pin and Ground.
FPD-LINK III INTERFACE PINS			
DOUT0–	26	I/O	FPD-Link III TX Port 0 pins The port transmits FPD-Link III high-speed forward channel video and control data and receives back channel control data. It can interface with a compatible FPD-Link III deserializer RX through a STP or coaxial cable. The I/O must be AC-coupled per 表 188. If port is unused, leave the pins as No Connect.
DOUT0+	27	I/O	
DOUT1–	22	I/O	FPD-Link III TX Port 1 pins The port transmits FPD-Link III high-speed forward channel video and control data and receives back channel control data. It can interface with a compatible FPD-Link III deserializer RX through a STP or coaxial cable. The I/O must be AC-coupled per 表 188. If port is unused, leave the pins as No Connect.
DOUT1+	23	I/O	
LFT	20	D	FPD-Link III Loop Filter pin Connect a 10 nF capacitor between this pin and Ground.
REFCLK0	41	I, PD	External reference clock input pin It is an external reference clock input pin for the FPD-LINK III Port 0 when in Independent 2:2 or Asymmetric Splitter modes. It is typically connected to a low jitter clock source. It has an internal 25 kΩ pulldown. If unused, the pin may be left as No Connect or tied to GND.
REFCLK1	11	I, PD	External reference clock input pin for the FPD-LINK III Port 1 when in Independent 2:2 or Asymmetric Splitter Modes It is typically connected to a low jitter clock source. It has an internal 25 kΩ pulldown. If unused, the pin may be left as No Connect or tied to GND.
CONTROL PINS			
I2C_SDA	48	I/O, OD	I2C Data Input / Output Interface pin Open drain. Recommend a 2.2 kΩ to 4.7 kΩ pullup(1) to 1.8 V or 3.3 V.
I2C_SCL	47	I/O, OD	I2C Clock Input / Output Interface pin Open drain. Recommend a 2.2 kΩ to 4.7 kΩ pullup(1) to 1.8 V or 3.3 V.
IDX	19	I, S	I2C Serial Control Bus Device ID Address Select configuration pin Connect to an external pullup to VDD18 and a pulldown to GND to create a voltage divider per 表 12. **DO NOT LEAVE OPEN OR NO CONNECT.**
MODE_SEL0	18	I, S	Mode Select 0 configuration pin Connect to an external pullup to VDD18 and a pulldown to GND to create a voltage divider per 表 8 and .
MODE_SEL1	32	I, S	Mode Select 1 configuration pin Connect to an external pullup to VDD18 and a pulldown to GND to create a voltage divider per 表 8 and .
PDB	31	I, PD	Inverted Power-Down input pin. Typically connected to a processor GPIO with a pulldown. When PDB input is brought HIGH, the device is enabled and internal registers and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN with an internal 50 kΩ internal pulldown enabled. PDB should remain low until after power supplies are applied and reach minimum required levels. PDB = 1, device is enabled (normal operation) PDB = 0, device is powered down.
INTB	30	O, OD	Interrupt output pin INTB is an active-low open drain and controlled by the status registers. See *Interrupt Support*. INTB = H, Normal Operation INTB = L, Interrupt Request Recommended pullup resistor is 4.7 kΩ to VDDIO.**DO NOT LEAVE OPEN OR NO CONNECT.**

(1) Optimal pullup resistor value depends on the I2C mode of operation, refer to *I2C Bus Pullup Resistor Calculation* (SLVA689)

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
REM_INTB	10	O	Remote Interrupt output pin REM_INTB will directly mirror the status of the INTB_IN signal from the remote device. No separate serializer register read is required to reset and change the status of this pin. If unused, leave the pin as No Connect.
SPI PINS (IN DUAL FPD-LINK III MODE)			
MOSI	46	I/O, PD	SPI Master Output Slave Input pin Only available in Dual Link Mode. Shared with D_GPIO0. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
MISO	45	I/O, PD	SPI Master Input Slave Output pin Only available in Dual Link Mode. Shared with D_GPIO1. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
SPLK	44	I/O, PD	SPI Clock pin Only available in Dual Link Mode. Shared with D_GPIO2. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
SS	43	I/O, PD	SPI Slave Select pin Only available in Dual Link Mode. Shared with D_GPIO3. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
HIGH-SPEED GPIO PINS			
D_GPIO0	46	I/O, PD	High-Speed GPIO0 pin Only available in Dual Link Mode. Shared with MOSI. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
D_GPIO1	45	I/O, PD	High-Speed GPIO1 pin Only available in Dual Link Mode. Shared with MISO. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
D_GPIO2	44	I/O, PD	High-Speed GPIO2 pin Only available in Dual Link Mode. Shared with SPLK. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
D_GPIO3	43	I/O, PD	High-Speed GPIO3 pin Only available in Dual Link Mode. Shared with SS. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO PINS			
GPIO0	14	I/O, PD	General-Purpose Input/Output 0 pin If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO1	15	I/O, PD	General-Purpose Input/Output 1 pin If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO2	38	I/O, PD	General-Purpose Input/Output 2 pin Shared with I2S_DC. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO3	39	I/O, PD	General-Purpose Input/Output 3 pin Shared with I2S_DD. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
REGISTER-ONLY GPIO PINS			
GPIO5_REG	37	I/O, PD	General-Purpose Input/Output 5 pin Local register control only. Shared with I2S_DB. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO6_REG	36	I/O, PD	General-Purpose Input/Output 6 pin Local register control only. Shared with I2S_DA. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO7_REG	34	I/O, PD	General-Purpose Input/Output 7 pin Local register control only. Shared with I2S_WC. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
GPIO8_REG	35	I/O, PD	General-Purpose Input/Output 8 pin Local register control only. Shared with I2S_CLK. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
SLAVE MODE LOCAL I2S CHANNEL PINS			
I2S_WC	34	I/O, PD	Slave Mode I2S Word Clock Input pin Shared with GPIO7_REG. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
I2S_CLK	35	I/O, PD	Slave Mode I2S Clock Input pin Shared with GPIO8_REG. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
I2S_DA	36	I/O, PD	Slave Mode I2S Data Input pin Shared with GPIO6_REG. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
I2S_DB	37	I/O, PD	Slave Mode I2S Data Input pin Shared with GPIO5_REG. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
I2S_DC	38	I/O, PD	Slave Mode I2S Data Input pin Shared with GPIO2. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
I2S_DD	39	I/O, PD	Slave Mode I2S Data Input pin Shared with GPIO3. If unused and in a default condition (a 25 kΩ pulldown resistor enabled), this pin may be left as a No Connect pin.
POWER AND GROUND PINS			
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to a Ground plane.
VDD18	24 61	P	1.8 V (±5%) Power Supply pins Require 0.1 μF or 0.01 μF capacitors to GND at each VDD pin. Additional 1 μF and 10 μF decoupling capacitors are recommended for the pin group.
VDD11_P0	17	P	1.1 V (±5%) Power Supply pins Require 0.1 μF or 0.01 μF capacitors to GND at each VDD pin. Additional 1 μF and 10 μF decoupling capacitors are recommended for the pin group.
VDD11_P1	50	P	
VDD11_DSI	64	P	1.1 V (±5%) Power Supply pins Require 0.1 μF or 0.01 μF capacitors to GND at each VDD pin. Additional 1 μF and 10 μF decoupling capacitors are recommended for the pin group.
VDD11_A	12	P	
VDD11_HS0	28	P	
VDD11_HS1	21	P	
VDD11_S	25	P	
VDD11_L	9 42	P	1.1 V (±5%) Power Supply pins Require 0.1 μF or 0.01 μF capacitors to GND at each VDD pin. Additional 1 μF and 10 μF decoupling capacitors are recommended for the pin group.
VDDIO	16, 33	P	1.8 V (±5%) OR 3.3 V (±10%) LVCMOS I/O Power Supply pins Require 0.1 μF or 0.01 μF capacitors to GND at each VDD pin. Additional 1 μF decoupling capacitor is recommended for the pin group. If 1.8 V VDDIO option is selected, the VDDIO and VDD18 need to be supplied from the same power source.
OTHER PINS			
RES0	29	—	Reserved. Tie to GND.
RES1	40	—	Reserved.
RES2	13	—	Reserved. Must be left as No Connect.

The definitions below define the functionality of the I/O cells for each pin.

TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- OD = Open Drain
- PD = Internal Pulldown
- P, G = Power supply, Ground
- D = Decoupling pin for internal LDO output
- S = Strap Input

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	VDD11 (VDD11_P0, VDD11_P1, VDD11_DSI, VDD11_A, VDD11_HS0, VDD11_HS1, VDD11_S, VDD11_L)	–0.3	1.32	V
	VDD18	–0.3	2.16	
	VDDIO	–0.3	3.96	
DSI input voltage	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	–0.3	2.16	V
LVCMOS IO voltage	PDB, GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REM_INTB, REFCLK0, REFCLK1	–0.3	$V_{(VDDIO)}$ + 0.3	V
Configuration input voltage	IDX, MODE_SEL0, MODE_SEL1	–0.3	2.16	V
Open-Drain voltage	I2C_SDA, I2C_SCL, INTB	–0.3	3.96	V
FPD-Link III output voltage	DOUT0+, DOUT0-, DOUT1+, DOUT1-	−0.3	1.7	V
Analog voltage	LFDSI, LFT	−0.3	1.7	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and *Absolute Maximum Ratings for Soldering* (SNOA549).

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	(D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±8000	V
			Other pins	±4000	
		Charged-device model (CDM), per AEC Q100-011		±1000	
		(IEC 61000-4-2) R_D = 330 Ω, C_S = 150 pF	Air Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±15000	
			Contact Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±10000	
		(ISO10605) R_D = 330 Ω, C_S = 150 pF R_D = 2 kΩ, C_S = 150 pF or 330 pF	Air Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±21000	
			Contact Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±10000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD11)}$	1.045	1.1	1.155	V
	$V_{(VDD18)}$	1.71	1.8	1.89	
LVCMOS I/O supply voltage	$V_{(VDDIO)}$ = 1.8 V	1.71	1.8	1.89	V
	OR $V_{(VDDIO)}$ = 3.3 V	3	3.3	3.6	
Open-drain voltage	INTB = $V_{(INTB)}$, I2C pins = $V_{(VDDI2C)}$	1.71		3.6	V
Operating Free Air Temperature, T_A		−40	25	105	°C
MIPI data rate (per DSI lane)		150		1500	Mbps
MIPI DSI HS clock frequency		75		750	MHz
Local I2C frequency, f_{I2C}				1	MHz
Reference clock frequency, f_{REFCLK}		25		210	MHz
Reference clock frequency stability including aging		-100		100	ppm

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
Spread-spectrum reference clock modulation percentage	REFCLK, center spread	-0.25		0.25	%
	REFCLK, up spread	0		0.5	%
	REFCLK, down spread	-0.5		0	%
Supply noise (DC - 50 MHz)	$V_{(VDD11)}$			25	mVp-p
	$V_{(VDD18)}$			50	
	$V_{(VDDIO)}$ = 1.8 V			50	
	$V_{(VDDIO)}$ = 3.3 V			50	
	$V_{(VDDI2C)}$ = 1.8 V			50	
	$V_{(VDDI2C)}$ = 3.3 V			100	

7.4 Thermal Information

THERMAL METRIC[1]		DS90UB941AS-Q1 RTD (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
P_T	Total power, normal operation	Single, 4-lane, DSI Input, f_{DSI_CLK} = 630 MHz (f_{PCLK} = 210 MHz), Dual-link FPD-Link III output, Line rate = 3.675 Gbps, Checkerboard pattern, R_L = 100 Ω	VDD11, VDD18, VDDIO			800	mW
SUPPLY CURRENT							
I_{DD}	Supply current, normal operation	Single, 4-lane, DSI Input, f_{DSI_CLK} = 630 MHz (f_{PCLK} = 210 MHz), Dual-link FPD-Link III output, Line rate = 3.675 Gbps, Checkerboard pattern, RL = 100 Ω	VDD11		165	500	mA
			VDD18		25	45	mA
			VDDIO		2	10	mA
I_{DDZ}	Supply current, power-down mode	PDB = L	VDD11			140	mA
			VDD18			15	mA
			VDDIO			4	mA
1.8 V LVCMOS I/O							
V_{IH}	High Level Input Voltage	$V_{(VDDIO)}$ = 1.71 V to 1.89 V	PDB, GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REFCLK0, REFCLK1	0.65 × $V_{(VDDIO)}$			V
V_{IL}	Low Level Input Voltage	$V_{(VDDIO)}$ = 1.71 V to 1.89 V		0		0.35 × $V_{(VDDIO)}$	V
I_{IH}	Input High Current	V_{IN} = $V_{(VDDIO)}$ = 1.71 V to 1.89 V, Internal Pulldown enabled		0		100	µA
		V_{IN} = $V_{(VDDIO)}$ = 1.71 V to 1.89 V, Internal Pulldown disabled	GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REFCLK0, REFCLK1	0		10	µA

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
I_{IL}	Input Low Current	V_{IN} = 0 V	PDB, GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REFCLK0, REFCLK1	-20		20	µA
$I_{IN-STRAP}$	Strap Pin Input Current	V_{IN} = 0 V or $V_{(VDDIO)}$ = 1.71 V to 1.89 V	IDX, MODE_SEL0, MODE_SEL1	-1		1	µA

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –2 mA, $V_{(VDDIO)}$ = 1.71 V to 1.89 V	GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REM_INTB	$V_{(VDDIO)}$ – 0.45			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA, $V_{(VDDIO)}$ = 1.71 V to 1.89 V		0		0.45	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			−35		mA
I_{OZ}	TRI-STATE™ output current	V_{OUT} = 0 V or V_{DDIO}, PDB = L		−20		20	µA
3.3 V LVCMOS I/O							
V_{IH}	High Level Input Voltage	$V_{(VDDIO)}$ = 3.0 V to 3.6 V	PDB, GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REFCLK0, REFCLK1	2.0		$V_{(VDDIO)}$	V
V_{IL}	Low Level Input Voltage	$V_{(VDDIO)}$ = 3.0 V to 3.6 V		0		0.8	V
I_{IH}	Input High Current	V_{IN} = $V_{(VDDIO)}$ = 3.0 V to 3.6 V, Internal Pulldown enabled		0		180	µA
		V_{IN} = $V_{(VDDIO)}$ = 3.0 V to 3.6 V, Internal Pulldown disabled	GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REFCLK0, REFCLK1			25	µA
I_{IL}	Input Low Current	V_{IN} = 0 V	PDB, GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REFCLK0, REFCLK1	−20		20	µA

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage	I_{OH} = –4 mA, $V_{(VDDIO)}$ = 3.0 V to 3.6 V		GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, MOSI, MISO, SPLK, SS, I2C_WC, I2S_CLK, I2S_DA, I2S_DB, I2S_DC, I2S_DD, REM_INTB	2.4		$V_{(VDDIO)}$	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA, $V_{(VDDIO)}$ = 3.0 V to 3.6 V			0		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V				−60		mA
I_{OZ}	TRI-STATE™ output current	V_{OUT} = 0 V or $V_{(VDDIO)}$, PDB = L			−20		20	µA
OPEN DRAIN OUTPUT								
V_{OL}	Output Low Level	$V_{(VDDIO)}$ = 3.0 V to 3.6 V, I_{OL} = 4 mA		INTB	0		0.4	V
		$V_{(VDDIO)}$ = 1.71 V to 1.89 V, I_{OL} = 2 mA			0		0.45	
I_{OH}	Output Leakage Current	$V_{(VDDIO)}$			−20		20	µA
SERIAL CONTROL BUS I/O								
V_{IH}	Input High Level			I2C_SCL, I2C_SDA	0.7 x $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Input Low Level				0		0.3 x $V_{(VDDIO)}$	V
V_{HYS}	Input Hysteresis					50		mV
V_{OL1}	Output Low Level	$V_{(VDDIO)}$ = 3.0 V to 3.6 V, I_{OL} = 3 mA	Standard-mode, Fast-mode		0		0.4	V
		$V_{(VDDIO)}$ = 3.0 V to 3.6 V, I_{OL} = 20 mA	Fast-mode Plus		0		0.4	V
V_{OL2}	Output Low Level	$V_{(VDDIO)}$ = 1.71 V to 1.89 V, I_{OL} = 2 mA	Fast-mode, Fast-mode Plus		0		0.2 x $V_{(VDDIO)}$	V
I_{IH}	Input Current High	V_{IN} = $V_{(VDDIO)}$			-10		10	µA
I_{IL}	Input Current Low	V_{IN} = 0 V			-10		10	µA
C_{IN}	Input Capacitance					5		pF
FPD-LINK III TRANSCEIVER								
V_{ODp-p}	Differential output voltage	R_L = 100 Ω Back channel disabled		DOUT0+, DOUT0-, DOUT1+, DOUT1-	900		1200	mV_{p-p}
V_{OUT}	Single-ended output voltage	R_L = 50 Ω Back channel disabled			450		600	mV
ΔV_{OD}	Output voltage unbalance	R_L = 100 Ω				1	50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω				550		mV
ΔV_{OS}	Offset voltage unbalance	R_L = 100 Ω				1	50	mV
I_{OS}	Output short-circuit current	FPD-link III outputs = 0 V				-20		mA
R_T	Termination resistance	Differential			80	100	120	Ω
		Single-ended			40	50	60	Ω
V_{ID-BC}	Differential back channel input amplitude	Back channel data rate = 5, 10, or 20 Mbps			170			mV
V_{IN-BC}	Single-ended back channel input amplitude				170			mV

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
DSI HSRX RECEIVER								
$V_{CMRX(DC)}$	Common-mode voltage, HS receive mode	Steady-state	Steady-state	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	70		330	mV
$V_{CMRX(DC)}$	Common-mode voltage, HS receive mode	Steady-state		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	70		330	mV
V_{IDTH}	Differential input high threshold	Data rates ≤ 1.5 Gbps					70	mV
V_{IDTL}	Differential input low threshold				−70			mV
V_{IH-HS}	Single-ended input high voltage						460	mV
V_{IL-HS}	Single-ended input low voltage				−40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable						450	mV
Z_{ID}	Differential input impedance				80	100	125	Ω
DSI LPRX RECEIVER								
V_{IH-LP}	LP logic 1 input voltage	Applicable when the supported data rate ≤ 1.5 Gbps		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	880			mV
V_{IL-LP}	LP logic 0 input voltage	Not in ULP state					550	mV
V_{HYST}	Input hysteresis				25			mV

7.6 AC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO Timing							
f_{GPIO_FC}	Maximum forward channel GPIO frequency	Single FPD-Link III	GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3		(1/4) × f_{PCLK}		MHz
		Dual FPD-Link III			(1/8) × f_{PCLK}		MHz
$t_{GPIO\_FC\_JIT}$	Forward channel GPIO jitter	Single FPD-Link III			1 / f_{PCLK}		ns
		Dual FPD-Link III			2 / f_{PCLK}		ns
f_{GPIO_BC}	Maximum back channel GPIO frequency	BC rate = 20 Mbps, Normal GPIO Mode (DES), 4 GPIOs			133		kHz
f_{GPIO_BC}		BC rate = 20 Mbps, Fast GPIO Mode, 4 GPIOs			800		kHz
f_{GPIO_BC}		BC rate = 20 Mbps, Fast GPIO Mode, 2 GPIOs			1.33		MHz
f_{GPIO_BC}		BC rate = 20 Mbps, Fast GPIO Mode, 1 GPIO			2		MHz
t_{GPIO_BC}	Back channel GPIO jitter	BC rate = 20 Mbps, Normal GPIO Mode (DES), 4 GPIOs			1900		ns
t_{GPIO_BC}		BC rate = 20 Mbps, Fast GPIO Mode, 4 GPIOs			320		ns
t_{GPIO_BC}		BC rate = 20 Mbps, Fast GPIO Mode, 2 GPIOs			190		ns
t_{GPIO_BC}		BC rate = 20 Mbps, Fast GPIO Mode, 1 GPIO			130		ns
t_{GPO_LHT}	GPO low-to-high transition time	C_L = 8 pF (lumped load), Default registers			2		ns
t_{GPO_HLT}	GPO high-to-low transition time				2		ns
FPD-LINK III TIMING							
t_{LHT}	Low voltage differential low-to-high transition time		DOUT0+, DOUT0-, DOUT1+, DOUT1–		80	120	ps
t_{HLT}	Low voltage differential high-to-low transition time				80	120	ps
t_{XZD}	Output active to OFF delay	PDB H -> L			100	300	ns
t_{PLD}	Lock time	PDB L -> H, with input clock active			5		ms
t_{SD}	Delay – latency				145 × T		ns
t_{JITR}	Output random jitter	0.3 UI Jitter applied, CDR BW = f/15 f_{DSI_CLK} = 510 MHz (f_{PCLK} = 170 MHz, Dual-link FPD-Link III, line rate = 2.975 Gbps), R_L = 100 Ω			3		ps(rms)
t_{JITD}	Output deterministic jitter				43		ps(p-p)
t_{JIT}	Output total jitter				0.17	0.24	UI_{FPD3} (1)
E_H	Eye height			660			mVpp
t_{JITR}	Output random jitter	0.3 UI Jitter applied, CDR BW = f/15 f_{DSI_CLK} = 630 MHz (f_{PCLK} = 210 MHz, Dual-link FPD-Link III, line rate = 3.675 Gbps), R_L = 100 Ω			3		ps(rms)
t_{JITD}	Output deterministic jitter				51		ps(p-p)
t_{JIT}	Output total jitter				0.22	0.31	UI_{FPD3} (1)
E_H	Eye height			580			mVpp
λ_{STXBW}	Jitter transfer function (–3 dB bandwidth)				960		kHz
δ_{STX}	Jitter transfer function peaking				0.1		dB
V_{BCDR}	Back channel data rate	Default (Deserializer)			5		Mbps
		HSCC_MODE (Deserializer)			10		
		HSCC_MODE (Deserializer)			20		

(1) UI_{FPD3} - FPD-Link III Unit Interval is equivalent to one serialized data bit width. For Single-link mode, 1 UI_{FPD3} = 1/(35*f_{PCLK}). For Dual-link mode, 1 UI_{FPD3} = 1/(35*f_{PCLK}/2). The UI_{FPD3} scales with PCLK frequency.

AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
DSI LPRX RECEIVER							
e_{SPIKE}	Input pulse rejection		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN			300	V*s
T_{MIN-RX}	Minimum pulse width response			20			ns
V_{INT}	Peak interference amplitude					200	mV
f_{INT}	Interference frequency			450			MHz
DSI HSRX RECEIVER							
$\Delta V_{CMRX(HF)}$	Common-mode Interference HF	Common-level variations above 450 MHz Data rates ≤ 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN			100	mV
$\Delta V_{CMRX(LF)}$	Common-mode Interference LF	Common-level variations between 50 to 450 MHz Data rates ≤ 1.5 Gbps		–50		50	mV
C_{CM}	Common-mode termination					60	pF
DSI CLOCK TIMING							
$UI_{DSI-INST}$	DSI UI instantaneous	150 Mbps to 1.5 Gbps	DSI0_CLKP, DS0_CLKN, DSI1_CLKP, DSI1_CLKN	0.667		66.7	ns
ΔUI_{DSI}	DSI UI variation	UI_{DSI} ≥ 1 ns		−0.1		0.1	UI_{DSI} (2)
		0.667 ns < UI_{DSI} < 1 ns		−0.05		0.05	UI_{DSI} (2)
t_{DSI_JIT}	DSI clock jitter	DSI Reference Clock Mode, BRIDGE_CFG2[1:0] = 00b f_{PCLK} / 40 < Jitter frequency < f_{PCLK} / 20, TJ@BER<1E-10				0.3	UI_{FPD3} (1)

(2) UI_{DSI} - DSI unit interval is equivalent to one bit period of the DSI input. 1 UI_{DSI} = 1/(2 * f_{DSI_CLK}).

AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
DSI DATA-CLOCK TIMING							
$t_{SETUP(RX)}$	Data-to-clock setup time	Data rate ≤ 1 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	−0.15		0.15	UI_{INST} (2)
		Data rate: 1 Gbps to 1.5 Gbps		−0.2		0.2	
$t_{HOLD(RX)}$	Data-to-clock hold time	Data rate ≤ 1 Gbps		−0.15		0.15	UI_{INST} (2)
		Data rate: 1 Gbps to 1.5 Gbps		−0.2		0.2	
DSI RECEIVER RETURN LOSS							
SDD_{RX}	RX differential return loss	f_{LPMAX}	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		>-18		dB
		f_H			>-9		dB
		f_{MAX}			>-3		dB
SCC_{RX}	RX common-mode return loss	1/4 $f_{INT, MIN}$			>0		dB
		$f_{INT, MIN}$			>-6		dB
		f_{MAX}			>-2.5		dB
SDC_{RX}	RX mode conversion	>0 to f_{MAX}			>-26		dB

7.7 Recommended Timing for External Clock Reference

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{REFCLK}	Reference clock frequency		25	f_{PCLK}	210	MHz
f_{REFCLK_STBL}	Reference clock frequency stability	Full temperature range and aging	-100		100	ppm
t_{REFCLK_P}	Reference clock period	$f_{REFCLK} = f_{PCLK}$ = 25 MHz - 210 MHz	4.76	T	40	ns
t_{REFCLK_H}	Reference clock high time		0.4T	0.5T	0.6T	ns
t_{REFCLK_L}	Reference clock low time		0.4T	0.5T	0.6T	ns
t_{REFCLK_JIT}	Reference clock jitter	f_{PCLK} / 40 < Jitter frequency < f_{PCLK} / 20, TJ@BER<1E-10			0.28	UI (1)

(1) UI_{FPD3} - FPD-Link III Unit Interval is equivalent to one serialized data bit width. For Single-link mode, 1 UI_{FPD3} = 1/(35*f_{PCLK}). For Dual-link mode, 1 UI_{FPD3} = 1/(35*f_{PCLK}/2). The UI_{FPD3} scales with PCLK frequency.

7.8 Recommended Timing for Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode Plus	>0		1	MHz
t_{LOW}	SCL low period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_{HIGH}	SCL high period	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{SU;STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode Plus	0			µs
$t_{SU;DAT}$	Data set up time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU;STO}$	Set up time for STOP condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_r	SCL and SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
t_f	SCL and SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode Plus			50	ns

7.9 Timing Diagrams

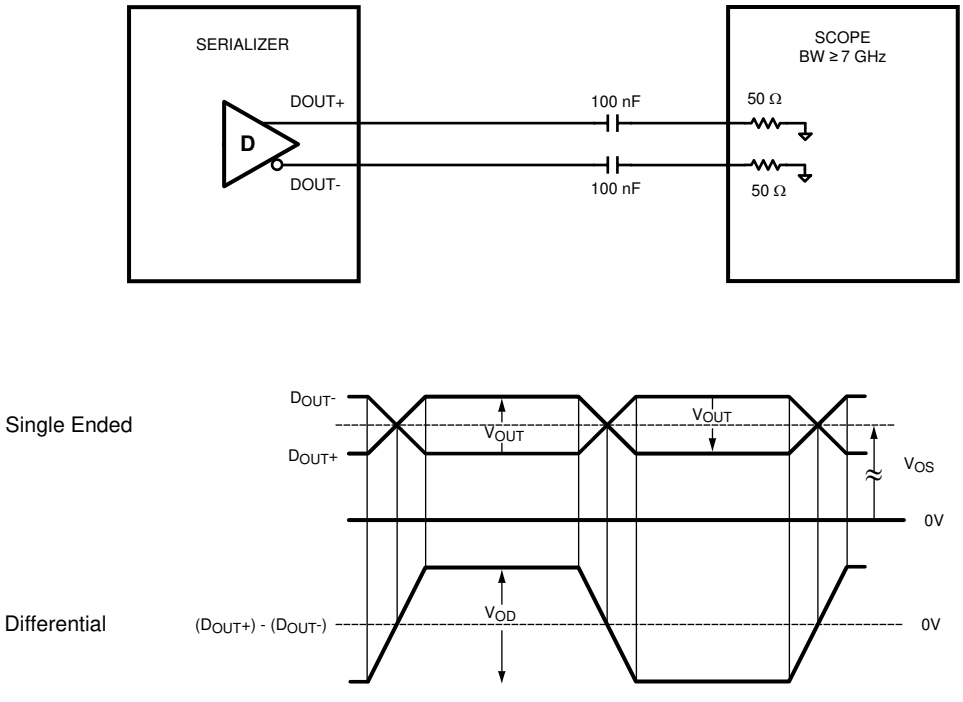


图 1. Serializer Output V_{OD}, V_{OUT}

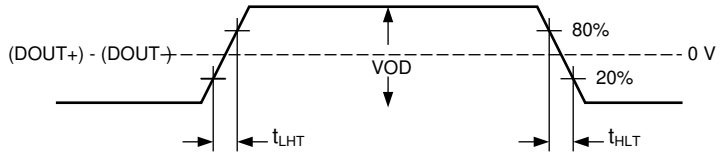


图 2. Output Transition Times

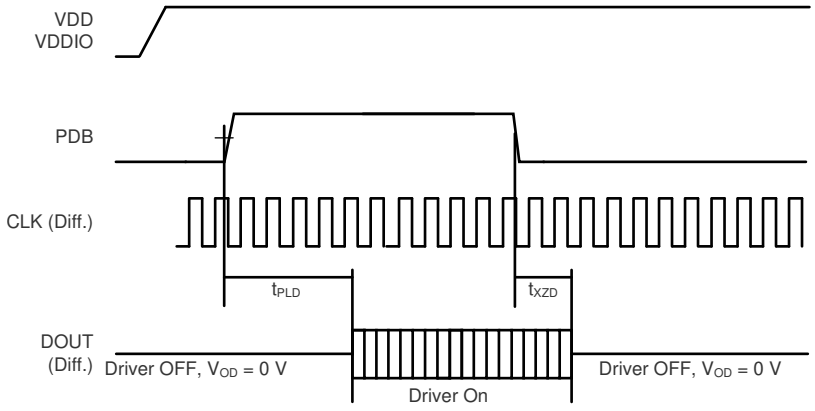


图 3. Serializer Lock Time

Timing Diagrams (接下页)

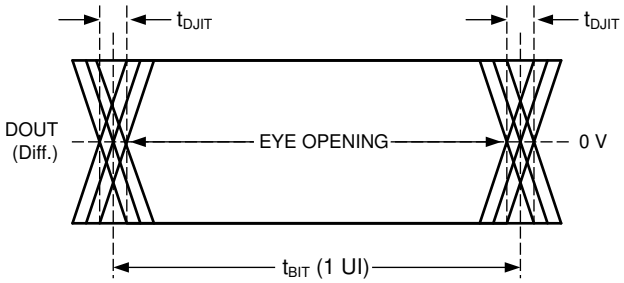


图 4. Serializer Output Jitter

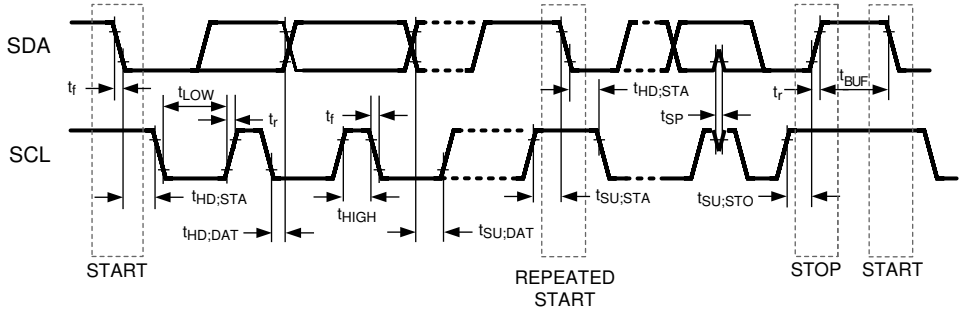


图 5. Serial Control Bus Timing Diagram

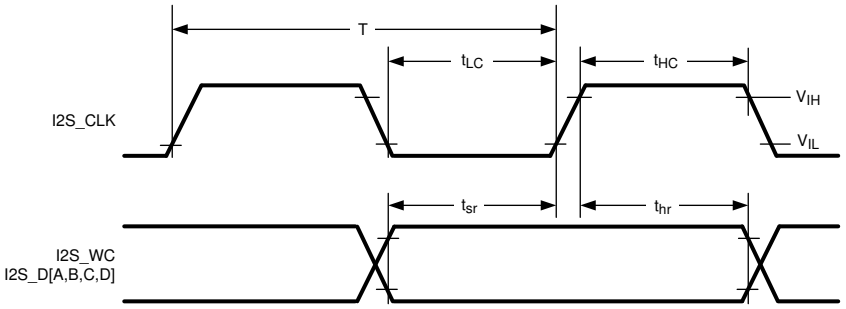


图 6. I2S Timing Diagram

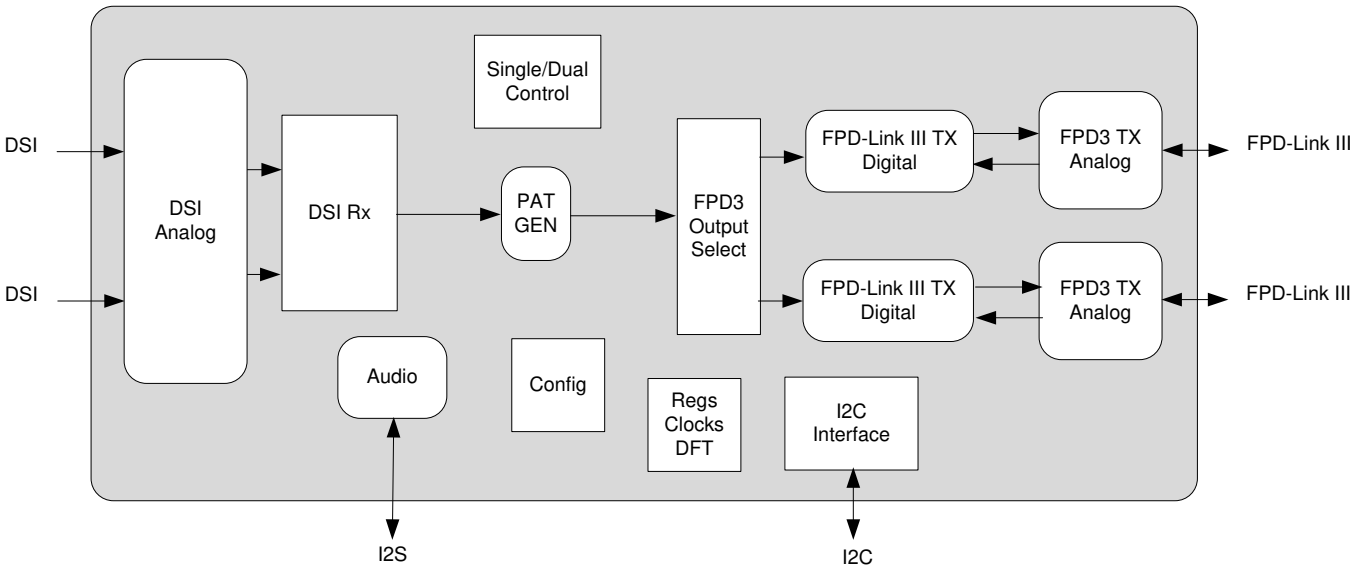
8 Detailed Description

8.1 Overview

The DS90UB941AS-Q1 is a Display Serial Interface (DSI) to FPD-Link III Bridge device that, in conjunction with the DS90UB940N-Q1, DS90UB948-Q1 deserializers over two low-cost, 50 Ω coaxial or two 100 Ω shielded twisted-pair (STP) cables, transmits high-resolution video, audio, and control information. Each of the dual DSI links has (4 lanes + 1 clock). They support video resolutions up to 2K with 24-bit color depth, and translates into dual-pair high-speed serialized interfaces. The serial bus scheme, FPD-Link III, supports video and audio data transmission and full duplex control including I2C communication over two differential links. Consolidation of video data and control over two differential pairs reduce the interconnect size and weight, while also eliminating skew issues and simplifying system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization. In backward-compatible mode, the device supports up to WXGA and 720p resolution with 24-bit color transmit over one differential link to the DS90UB924-Q1, DS90UB926-Q1 or DS90UB928-Q1 deserializers.

The DS90UB941AS-Q1 supports up to eight I2S audio channels. Audio data received from the I2S input is encrypted and sent over the FPD-Link III interfaces where it can be regenerated at an up to 8-channel I2S interface with maximum sample rate of 192 kHz.

8.2 Functional Block Diagram



8.3 Feature Description

The DS90UB941AS-Q1 implements a bridge between a DSI interface and dual FPD-Link III interface. The device integrates a DSI Receiver with the FPD-Link III Transmitters to provide audio and video transmission.

8.3.1 DSI Receiver

The DS90UB941AS-Q1 features two separate MIPI D-PHY v1.2 / DSI v1.3.1 compliant input ports. Selection of DSI input port is made through the DSI_PORT_SEL bit in the BRIDGE_CTL register. Each port allows 1 , 2 , 3 , or 4-lane operation. The number of lanes for both ports is controlled by the DSI_LANES field in the BRIDGE_CTL register, and may be set at power up through a strap option on the MODE_SEL0 pin. Automatic lane detection is not supported.

The DSI lane ordering can be reversed internally and independently for each of the two DSI ports, using the DSI1_LANE_REVERSE or DSI0_LANE_REVERSE fields in the DEVICE_CFG register:

- DEVICE_CFG:DSI0_LANE_REVERSE = 1:
  - DSI0_D3P/N -> Port 0 Lane 0
  - DSI0_D2P/N -> Port 0 Lane 1

Feature Description (接下页)

  - DSI0_D1P/N -> Port 0 Lane 2
  - DSI0_D0P/N -> Port 0 Lane 3
- DEVICE_CFG:DSI1_LANE_REVERSE = 1:
  - DSI1_D3P/N -> Port 1 Lane 0
  - DSI1_D2P/N -> Port 1 Lane 1
  - DSI1_D1P/N -> Port 1 Lane 2
  - DSI1_D0P/N -> Port 1 Lane 3

In addition, the DSI clock and data lane polarity can be inverted internally and independently for each of the two D-PHY ports:

- DEVICE_CFG:DSI0_DATA_PN_SWAP = 1:
  - DSI0_D3P/N -> DSI0_D3N/P
  - DSI0_D2P/N -> DSI0_D2N/P
  - DSI0_D1P/N -> DSI0_D1N/P
  - DSI0_D0P/N -> DSI0_D0N/P
- DEVICE_CFG:DSI0_CLK_PN_SWAP = 1:
  - DSI0_CLKP/N -> DSI0_CLKN/P
- DEVICE_CFG:DSI1_DATA_PN_SWAP = 1:
  - DSI1_D3P/N -> DSI1_D3N/P
  - DSI1_D2P/N -> DSI1_D2N/P
  - DSI1_D1P/N -> DSI1_D1N/P
  - DSI1_D0P/N -> DSI1_D0N/P
- DEVICE_CFG:DSI1_CLK_PN_SWAP = 1:
  - DSI1_CLKP/N -> DSI1_CLKN/P

8.3.1.1 DSI Operating Modes

The D-PHY receiver can be in High-Speed (HS) or Escape mode. During normal operation, a Data Lane will be in High-Speed mode. In Escape Mode, the D-PHY will be in a Low-Power (LP) State. In High-Speed mode, the data transmission happens in a burst and may start and end at a Stop state (LP-11), or remain in HS mode with null or blanking packets transmitted. There is a transition state to take the D-PHY from a Normal mode to the Escape mode or Low-Power state.

The sequence to enter High-Speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in High-Speed mode until a Stop state (LP-11) is received.

The sequence to enter Escape mode is: LP-11, LP-10, LP-00, LP-01, LP-00. As soon as the final Bridge state (LP-00) is observed, the Lane enters Escape Mode.

8.3.1.1.1 High-Speed Mode

During high-speed data transmission, the digital D-PHY will enable termination signal to allow proper termination of the HS RX, and the LP RX should stay at LP-00 state. Both DSI data lane and clock lane operate in the same manner. The DS90UB941AS-Q1supports DSI continuous clock lane mode where the clock LP RX stays at LP-00 state.

Feature Description (接下页)

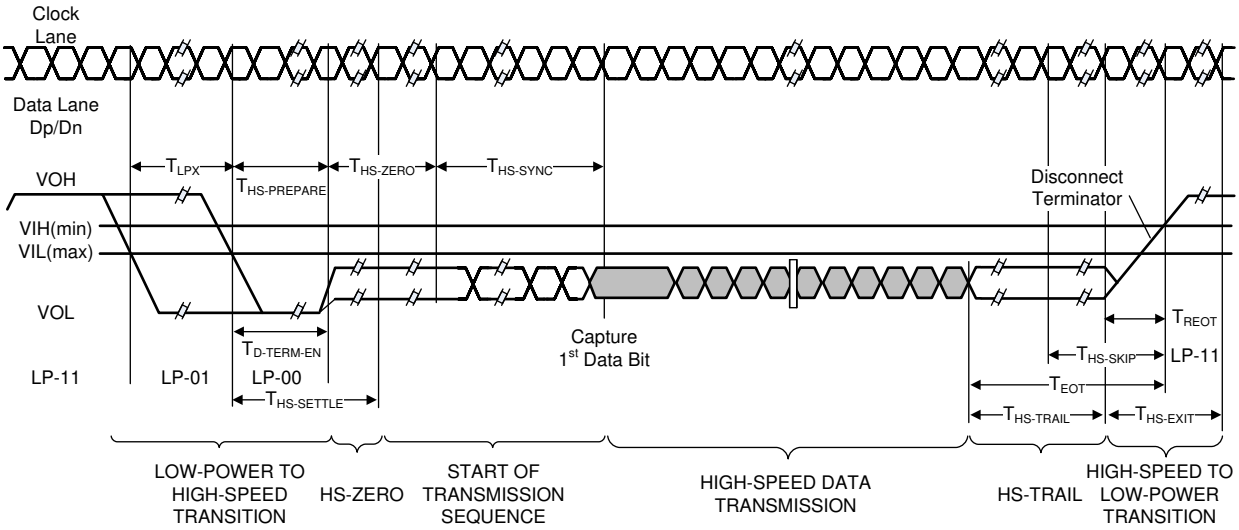


图 7. High-Speed Data Transmission in Bursts

Low power data transmission and low power escape modes are not supported.

8.3.1.1.2 Global Operation Timing Parameters

MIPI D-PHY v1.2 defines global operation timing for both D-PHY TX and RX. The DS90UB941AS-Q1 implements the following RX timing parameters:

- $t_{CLK-MISS}$
- $t_{CLK-SETTLE}$ (programmable)
- $t_{CLK-TERM-EN}$ (programmable)
- $t_{D-TERM-EN}$ (programmable)
- $t_{HS-SETTLE}$ (programmable)
- $t_{HS-SKIP}$ (programmable)
- t_{INIT} slave (programmable)
- t_{EOT} parameter is not supported.

Feature Description (接下页)

8.3.1.2 THS-SKIP Programming

The D-PHY data lanes include the ability to ignore the final data bits during HS data transfer. The number of bits to be ignored can be programmed into the DPHY_SKIP_TIMING register on Page1 of the device Indirect Registers.

The TSKIP_CNT field should be programmed based on the operating DSI clock frequency to meet the D-PHY THS-SKIP timing requirement. The TSKIP_CNT value (dec) is defined in 公式 1, where f_{DSI} is the DSI clock frequency in GHz. 表 1 shows a couple of example TSKIP_CNT values derived based on the given DSI clock frequency, f_{DSI}.

$$TSKIP\_CNT = Round(65 \cdot f_{DSI} - 5) \quad (1)$$

表 1. TSKIP_CNT Settings as a Function of f_{DSI} Examples

f_{DSI} [GHz]	TSKIP_CNT (dec)	DSI Indirect Register 0x05[6:1] (bin)	DSI Indirect Register 0x05 Setting (hex)
0.225	10	001010	0x14
0.315	15	001111	0x1E

8.3.1.3 DSI Errors and Status

8.3.1.3.1 DSI / DPHY Error Detection and Reporting

The DS90UB941AS-Q1 detects and reports DSI errors for each lane via the DPHY_DLANEx_ERR registers:

- SoT Error
- SoT Sync Error
- EoT Sync Error
- False Control Error

Escape Entry Command Error and LP Transmission Sync Error conditions are not supported.

8.3.1.3.2 DSI Protocol Error Detection

The DSI protocol logic provides a 3-bit status vector to indicate protocol errors. The three bits are:

- DSI_RD_WOUT_BTA: Read without Bus Turn-Around (BTA)
- DSI_EOT_ERR : End of Transmit without EOT packet
- DSI_CMD_OVER : Command FIFO Overflow

The DSI Protocol errors are available in the DSI_STATUS register. The error flags will be cleared on read of the DSI_STATUS register on Page 1 Indirect Registers.

8.3.1.3.3 DSI Error Reporting

The main register GENERAL_STS (0x0C) has two status bits related to DSI Errors. Bit 6 is the DSI_ERROR status bit, which ORs all of the DSI error bits within the indirect registers. If dual DSI is enabled, the DSI0 and DSI1 error bits are OR'd together. However, if only one DSI port is enabled, then the status bit only shows the error bits within that DSI port. This bit does not clear on read. All of the error status bits must be cleared within the DSI indirect registers. Bit 5 is the DPHY_ERROR status bit, which ORs all of the DPHY error bits within the indirect registers. It works similarly to the DSI_ERROR bit in that the DPHY_ERROR bit only shows the errors of the DPHY enabled and cannot be cleared on read.

There are three registers that show all of the errors that could be causing the DSI_ERROR_DET bit to be set. This error report comes from the DSI logic and is spread over DSI_ERR_RPT_0, DSI_ERR_RPT_1, and DSI_ERR_RPT_2 registers. The error report registers are cleared when reading the DSI_STS register. The optimal register read order for checking the DSI errors is to read the GENERAL_STS bit within the main registers, check the error report registers for an error, then read the DSI_STS register for other errors and to clear the error report registers.

8.3.1.3.4 DSI Error Counter

The DSI Error Counter increments on errors detected by the DSI Protocol logic. Each type of error can be enabled independently. If an error indication is enabled, the error counter increments if that condition is detected. Error conditions are enabled by setting the controls in the DIS_ERR_CFG0 and DSI_ERR_CFG1 registers on Page 1 Indirect Registers.

8.3.1.3.5 DSI to FPD-Link III Buffer Error

The DSI to FPD-Link III interface includes a buffer to handle transfer of data from the DSI protocol logic to the FPD-Link III transmit domain. If the interface detects a buffer overflow, the DSI_FPD3_ERR will be set in the DSI_STATUS register on Page 1 Indirect Registers.

8.3.1.4 Supported DSI Video Formats

The DS90UB941AS-Q1 supports four DSI RGB video formats:

- RGB888 (Packed Pixel Stream, 24-bit Format, Data Type 0x3E)
- RGB666 (Loosely Packed Pixel Stream, 18-bit format in Three Bytes, Data Type 0x2E)
- RGB666 (Packed Pixel Stream, 18-bit Format, Data Type 0x1E)
- RGB565 (Packed Pixel Stream, 16-bit Format, Data Type 0x0E)

The RGB video formats are automatically converted, if necessary, to 3-byte RGB888 for transmission over FPD-Link III.

The DS90UB941AS-Q1 also supports pass-through of four DSI YCbCr video formats:

- Packed Pixel Stream, 12-bit YCbCr 4:2:0 Format, Data Type 0x3D
- Packed Pixel Stream, 16-bit YCbCr 4:2:2 Format, Data Type 0x2C
- Packed Pixel Stream, 24-bit YCbCr 4:2:2 Format, Data Type 0x1C
- Loosely Packed Pixel Stream, 20-bit YCbCr 4:2:2 Format, Data Type 0x0C

Each of these formats is aligned to the 3-bytes-per-pixel forward channel but is not converted to RGB888.

The DS90UB941AS-Q1 also supports pass-through of Compressed Pixel Stream data, aligned to the 3-bytes-per-pixel for transmission over FPD-Link III. No decompression is done.

注

Normally, RGB pixel data is sent with one full horizontal video line of pixels in a single packet. The case of horizontal video line of active pixels divided into two or more packets is not supported.

8.3.2 High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel is composed of 35 bits of data containing RGB data, sync signals, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. 图 8 shows the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced, and scrambled.

图 8. FPD-Link III Serial Stream

The device supports pixel clocks in the range of 25 MHz to 105 MHz over one lane, or 50 MHz to 210 MHz over two lanes. The FPD-Link III serial stream rate is 3.675 Gbps maximum per lane (875 Mbps minimum).

8.3.3 Back Channel Data Transfer

The Backward Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, CRC and 4 bits of standard GPIO information with a 5 Mbps, 10 Mbps, or 20 Mbps line rate (configured by the compatible deserializer).

8.3.4 FPD-Link III Port Register Access

The DS90UB941AS-Q1 contains two downstream ports, and some registers need to be duplicated to allow control and monitoring of the two ports. To facilitate this, a TX_PORT_SEL register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) will be available independent of the settings in the TX_PORT_SEL register.

Setting the TX_PORT0_SEL or TX_PORT1_SEL bit will allow a read of the register for the selected port. If both bits are set, port1 registers will be returned. Writes to ports will occur on a port where the select bit is set, allowing simultaneous writes to both ports if both select bits are set.

Setting the PORT1_I2C_EN bit will enable a second I^2C slave address, allowing access to the second port registers through the second I^2C address. If this bit is set, the TX_PORT0_SEL and TX_PORT1_SEL bits will be ignored.

Note that in Forced Single FPD-Link III mode, access to port 1 registers will be disabled by preventing setting of the TX_PORT1_SEL register bit.

Additional port 1 registers are only available in Independent 2:2 and/or Splitter modes. If these modes are not enabled, all accesses to these registers will be to port 0 registers.

8.3.5 Video Control Signals

The video control signal bits embedded in the DSI interface are subject to certain limitations relative to the video pixel clock period (PCLK). By default, the DS90UB941AS-Q1 applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

- Horizontal Sync (HS): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). HS can have at most two transitions per 130 PCLKs.
- Vertical Sync (VS): The video control signal pulse is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
- Data Enable Input (DE): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). DE can have at most two transitions per 130 PCLKs.

8.3.6 Power Down Pin (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}. To save power, disable the link when the display is not needed (PDB = LOW). Ensure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, ensure that the pin is driven to 0 V for at least 2 ms before releasing it or driving it to high. In the case where PDB is pulled up to V_{DDIO} directly, a ≥10 kΩ pullup resistor and a >10 µF capacitor to ground are required (see *Power-Up and Initialization*).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held low for a minimum of 2 ms before going high again.

8.3.7 Serial Link Fault Detect

The DS90UB941AS-Q1 can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Register Maps). The DS90UB941AS-Q1 will detect any of the following conditions:

1. Cable open

2. “+” to “-” short
3. ”+” to GND short
4. ”-” to GND short
5. ”+” to battery short
6. ”-” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

注

The device will detect any of the above conditions, but does not report specifically which one has occurred.

8.3.8 Interrupt Support

8.3.8.1 Interrupt Pin (INTB)

The INTB pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions (see registers 0xC6 and 0xC7 in the *Register Maps*). For the remote interrupt condition, the INTB pin works in conjunction with the INTB_IN pin on the deserializer. This interrupt signal, when configured, will propagate from the deserializer to the serializer.

1. On the Serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN pin is set *LOW* by some downstream device.
3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read ISR register.
5. A read to ISR will clear the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTB_IN. This would be when the downstream device releases the INTB_IN pin on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

8.3.8.2 Remote Interrupt Pin (REM_INTB)

The DS90UB941AS-Q1 includes a dedicated REM_INTB (remote interrupt) pin. This pin provides a pass-through of the INTB signal from an attached FPD-Link III deserializer like the DS90UB948-Q1. During a valid link condition, the value on the deserializer INTB_IN pin will be reflected on the DS90UB941AS-Q1 REM_INTB pin.

In Dual FPD3 mode, the REM_INTB pin will indicate the INTB_IN from the attached dual-capable deserializer. In other modes, the REM_INTB pin will indicate a combined interrupt from the INTB_IN pins of multiple deserializers, if connected. The combined interrupt will be asserted if either connection reports a remote interrupt.

The REM_INTB_CTRL register allows bringing the remote interrupt indication to pins in addition to the REM_INTB pin. In addition, selection 0001 of the REM_INTB_MODE field allows bringing port 0 remote interrupt to REM_INTB and port 1 remote interrupt to the INTB pin.

8.3.9 GPIO Support

8.3.9.1 GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers. See 表 2 for GPIO enable and configuration.

表 2. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

8.3.9.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. These different modes are controlled by a compatible deserializer. Consult the appropriate deserializer datasheet for details on how to configure the back channel frequency. See 表 3 for details about D_GPIOs in various modes.

表 3. Back Channel D_GPIO Effective Frequency

HSCC_MODE (on DES)	MODE	NUMBER OF D_GPIOs	SAMPLES PER FRAME	D_GPIO Effective Frequency(1) (kHz)			D_GPIOs ALLOWED
				5 Mbps BC(2)	10 Mbps BC(3)	20 Mbps BC(4)	
000	Normal	4	1	33	66	133	D_GPIO[3:0]
011	Fast	4	6	200	400	800	D_GPIO[3:0]
010	Fast	2	10	333	666	1333	D_GPIO[1:0]
001	Fast	1	15	500	1000	2000	D_GPIO0

(1) The effective frequency assumes the worst-case back channel frequency (-20%) and a 4X sampling rate.
(2) 5 Mbps corresponds to BC FREQ SELECT = 0 and BC_HS_CTL = 0 on a compatible deserializer.
(3) 10 Mbps corresponds to BC FREQ SELECT = 1 & BC_HS_CTL = 0 on a compatible deserializer.
(4) 20 Mbps corresponds to BC FREQ SELECT = X & BC_HS_CTL = 1 on a compatible deserializer.

8.3.9.3 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I^2S input if enabled into GPIO_REG mode. See 表 4 for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

表 4. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG8	0x11[7:4] = 0x01	Output, L
	0x11[7:4] = 0x09	Output, H
	0x11[7:4] = 0x03	Input, Read: 0x1D[0]
GPIO_REG7	0x11[3:0] = 0x1	Output, L
	0x11[3:0] = 0x9	Output, H
	0x11[3:0] = 0x3	Input, Read: 0x1C[7]

表 4. GPIO_REG and GPIO Local Enable and Configuration (接下页)

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG6	0x10[7:4] = 0x1	Output, L
	0x10[7:4] = 0x9	Output, H
	0x10[7:4] = 0x3	Input, Read: 0x1C[6]
GPIO_REG5	0x10[3:0] = 0x1	Output, L
	0x10[3:0] = 0x9	Output, H
	0x10[3:0] = 0x3	Input, Read: 0x1C[5]
GPIO3	0x0F[3:0] = 0x1	Output, L
	0x0F[3:0] = 0x9	Output, H
	0x0F[3:0] = 0x3	Input, Read: 0x1C[3]
GPIO2	0x0E[7:4] = 0x1	Output, L
	0x0E[7:4] = 0x9	Output, H
	0x0E[7:4] = 0x3	Input, Read: 0x1C[2]
GPIO1	0x0E[3:0] = 0x1	Output, L
	0x0E[3:0] = 0x9	Output, H
	0x0E[3:0] = 0x3	Input, Read: 0x1C[1]
GPIO0	0x0D[3:0] = 0x1	Output, L
	0x0D[3:0] = 0x9	Output, H
	0x0D[3:0] = 0x3	Input, Read: 0x1C[0]

8.3.10 SPI Communication

The SPI Control Channel uses the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available, Forward Channel and Reverse Channel modes. In Forward Channel mode, the SPI Master is located at the Serializer, such that the direction of sending SPI data is in the same direction as the video data. In Reverse Channel mode, the SPI Master is located at the Deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI Control Channel can operate in a high-speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the slave to the master on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies where the MISO pin can be ignored by the master.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

注

SPI cannot be used to access Serializer / Deserializer registers.

8.3.10.1 SPI Mode Configuration

SPI is configured over I^2C using the High-Speed Control Channel Configuration (HSCC_CONTROL) register 0x43 on the compatible deserializer (DS90UB948-Q1 or DS90UB940N-Q1). HSCC_MODE (0x43[2:0]) must be configured for either High-Speed, Forward Channel SPI mode (110) or High-Speed, Reverse Channel SPI mode (111).

8.3.10.2 Forward Channel SPI Operation

In Forward Channel SPI operation, the SPI master located at the Serializer generates the SPI Clock (SPLK), Master Out / Slave In data (MOSI), and active-low Slave Select (SS). The Serializer over-samples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, MOSI, and SS are each sent on data bits in the forward channel frame. At the Deserializer, the SPI signals are regenerated using the pixel clock. To preserve setup and hold time, the Deserializer will hold MOSI data while the SPLK signal is high. In addition, it delays SPLK by one pixel clock relative to the MOSI data, increasing setup by one pixel clock.

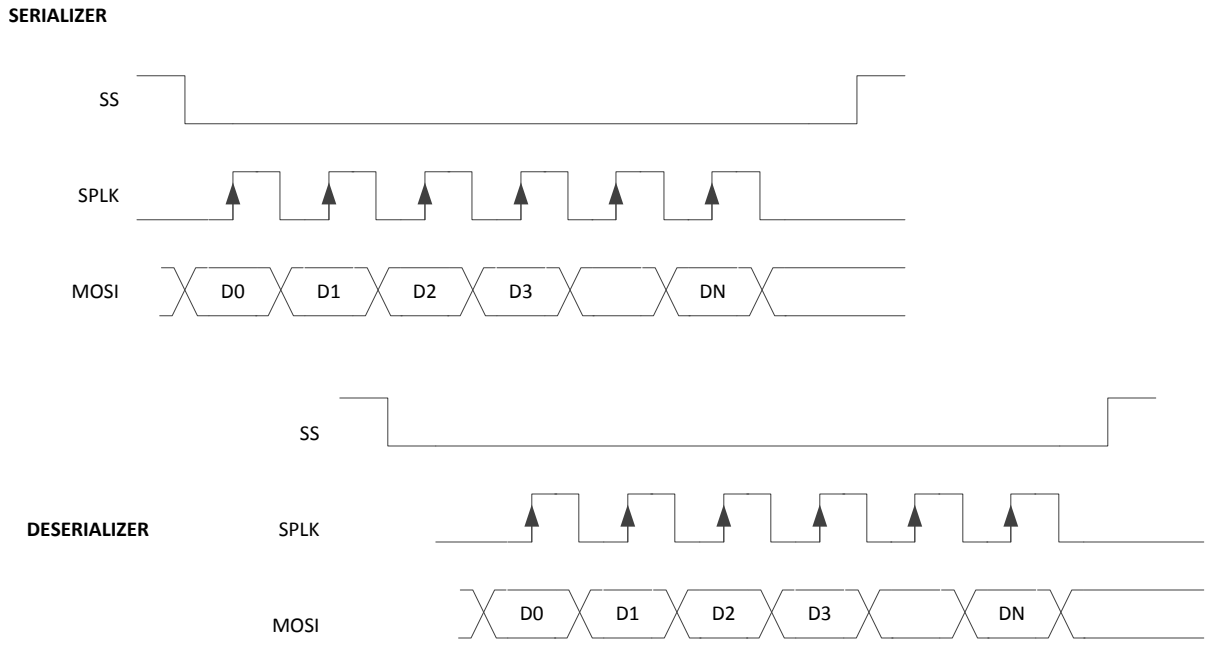


图 9. Forward Channel SPI Write

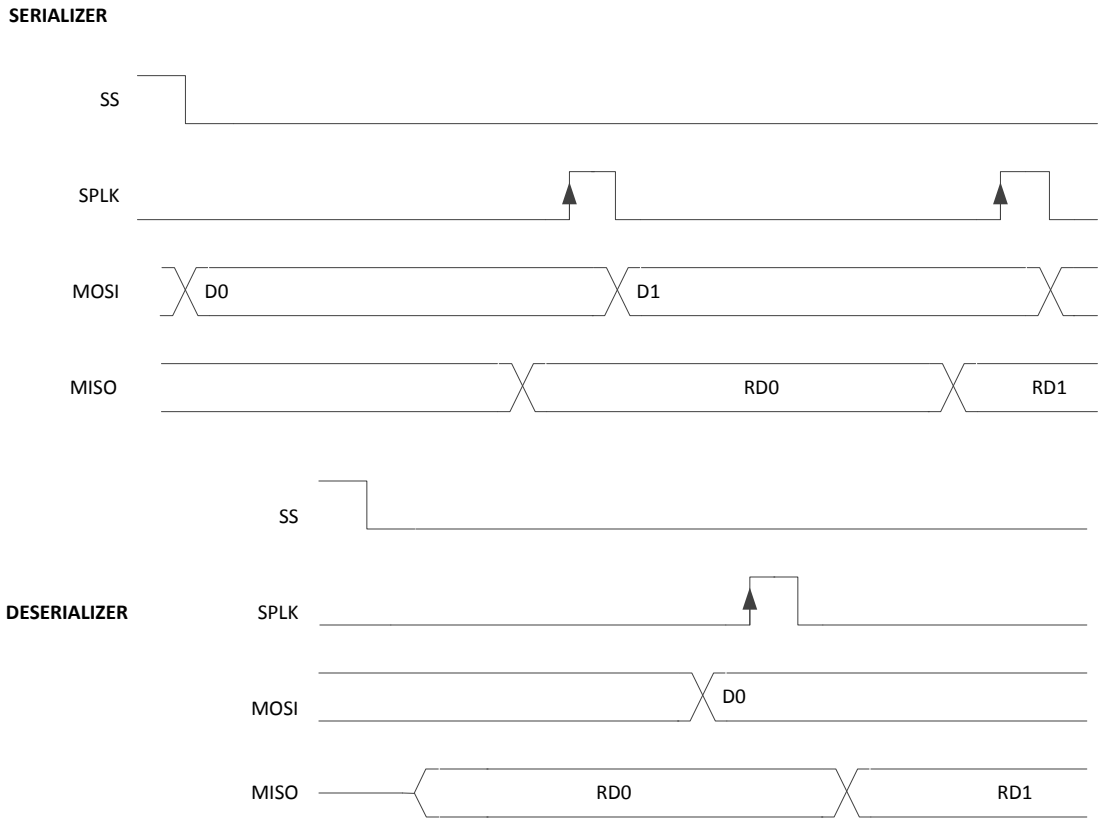


图 10. Forward Channel SPI Read

8.3.10.3 Reverse Channel SPI Operation

In Reverse Channel SPI operation, the Deserializer samples the Slave Select (SS), SPI clock (SCLK) into the internal oscillator clock domain. In addition, upon detection of the active SPI clock edge, the Deserializer samples the SPI data (MOSI). The SPI data samples are stored in a buffer to be passed to the Serializer over the back channel. The Deserializer sends SPI information in a back channel frame to the Serializer. In each back channel frame, the Deserializer sends an indication of the Slave Select value. The Slave Select should be inactive (high) for at least one back channel frame period to ensure propagation to the Serializer.

Because data is delivered in separate back channel frames and buffered, the data may be regenerated in bursts. 图 11 shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the SS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

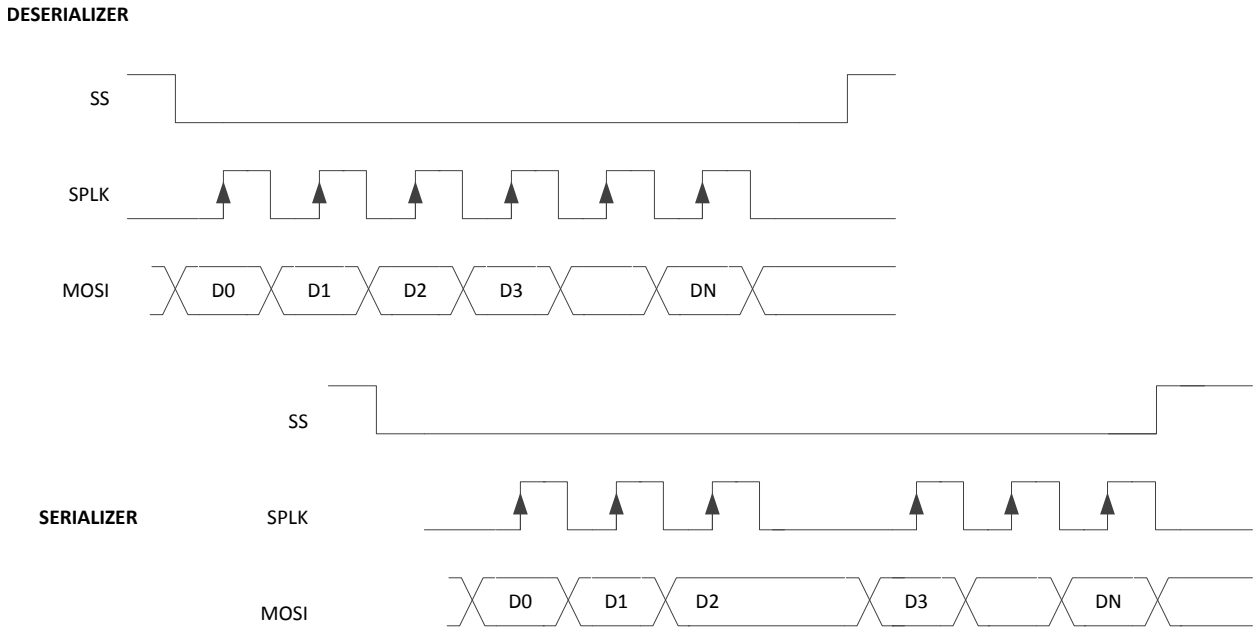


图 11. Reverse Channel SPI Write

For Reverse Channel SPI reads, the SPI master must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in Forward channel mode. Note that at most one data/clock sample will be sent per back channel frame.

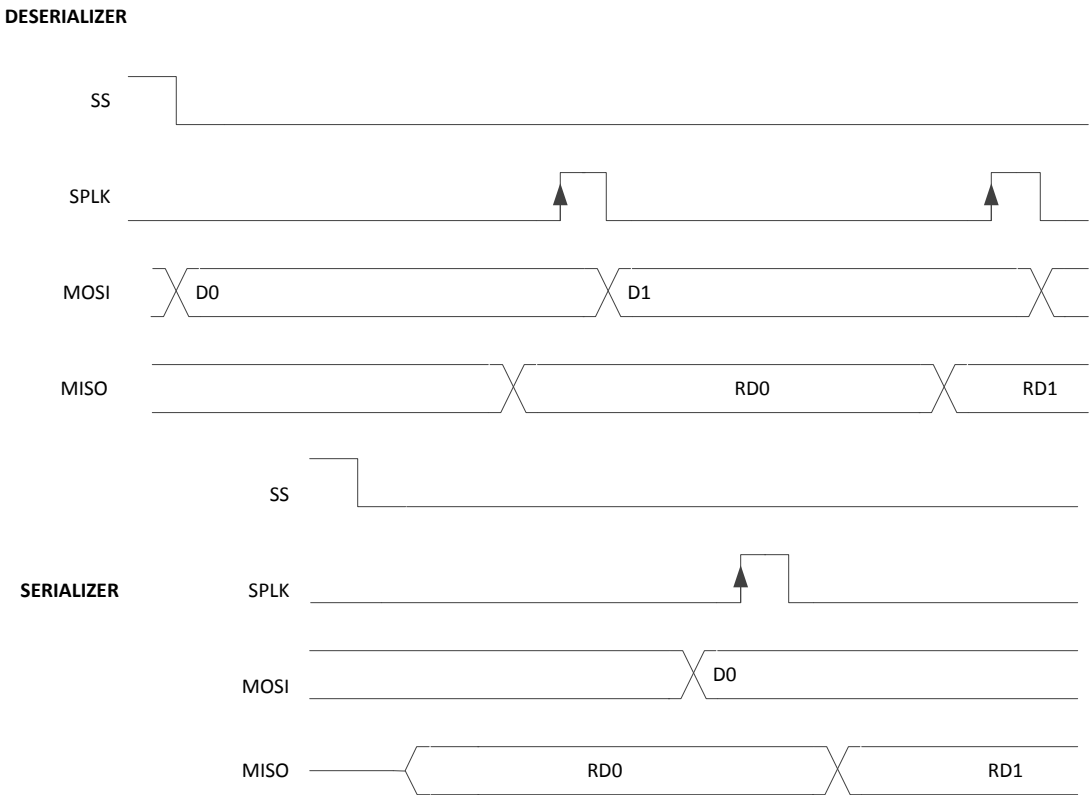


图 12. Reverse Channel SPI Read

For both Reverse Channel SPI writes and reads, the SPI_SS signal should be deasserted for at least one back channel frame period.

表 5. SPI SS Deassertion Requirement

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

8.3.11 Audio Modes

8.3.11.1 I2S Audio Interface

The DS90UB941AS-Q1 serializer features six I^2S input pins that, when paired with a compatible deserializer, supports 7.1 High-Definition (HD) Surround Sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the lesser of CLK/2 or 13 MHz. Four I^2S data inputs transport two channels of I^2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input. Refer to 图 13 and 图 14 for I2S connection diagram and timing information.

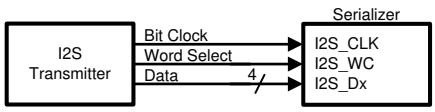


图 13. I^2S Connection Diagram

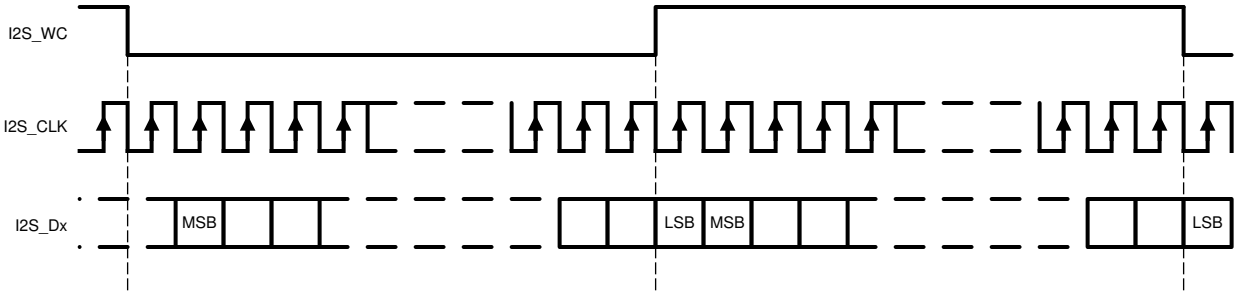


图 14. I2S Frame Timing Diagram

表 6 covers several common I^2S sample rates:

表 6. Audio Interface Frequencies

SAMPLE RATE (kHz)	I^2S DATA WORD SIZE (bits)	I^2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

8.3.11.1.1 I2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames may be disabled from control registers if Forward Channel Frame Transport of I^2S data is desired. In this mode, only I2S_DA is transmitted to a DS90UB928-Q1, DS90UB948-Q1, or DS90UB940N-Q1 deserializer. If connected to a DS90UB926-Q1 deserializer, I2S_DA and I2S_DB are transmitted. Surround Sound Mode, which transmits all four I^2S data inputs (I2S_D[A..D]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928-Q1, DS90UB948-Q1, or DS90UB940N-Q1 deserializer.

8.3.11.1.2 I2S Repeater

I^2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated through the Data Island Transport during the video blanking periods. If frame transport is desired, then the I^2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level deserializer automatically configures downstream serializers and deserializers for surround sound transport using Data Island Transport. If a 4-channel operation using I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree.

8.3.11.1.3 Audio During Splitter and Replicate Modes

During Splitter or Replicate modes, it is possible to send different audio on each downstream link. Operation is controlled by the SPLIT_AUDIO control in the AUDIO_CFG register.

If SPLIT_AUDIO is set to 0, the same audio will be sent on each port. The number of channels sent will depend on the DATAPATH_CTL register settings. Both ports will be configured the same.

If SPLIT_AUDIO is set to 1, the upper and lower channels will be swapped for port 1. This is done by swapping the I2S signals for I2S_A/B with I2S_C/D. In stereo mode, this will result in the I2S data on channel C being sent on port 1.

The mapping is shown in 表 7.

If the DS90UB941AS-Q1 is strapped into FPD3 Splitter mode at power-up, the AUDIO_SPLIT control will also be set to a 1. Otherwise, the AUDIO_SPLIT control will default to 0. The AUDIO_SPLIT register bit may be controlled by writing to the AUDIO_CFG register.

表 7. Splitter Audio Channel Mapping

SPLIT_AUDIO		PORT 0	PORT 1
0	A	I2S_DA	I2S_DA
	B	I2S_DB	I2S_DB
	C	I2S_DC	I2S_DC
	D	I2S_DD	I2S_DD
1	A	I2S_DA	I2S_DC
	B	I2S_DB	I2S_DD
	C	I2S_DC	I2S_DA
	D	I2S_DD	I2S_DB

8.3.11.2 TDM Audio Interface

In addition to the I^2S audio interface, the DS90UB941AS-Q1 serializer also supports TDM format. A number of specifications for TDM format are in common use, and the DS90UB941AS-Q1 offers flexible support for word length, bit clock, number of channels that can be multiplexed. For example, assume that word clock signal (I2S_WC) period = 256 × bit clock (I2S_CLK) time period. In this case, the DS90UB941AS-Q1 can multiplex 4 channels with maximum word length of 64 bits each, or 8 channels with maximum word length of 32 bits each. 图 15 shows the multiplexing of 8 channels with 24-bit word length, in a format similar to I2S.

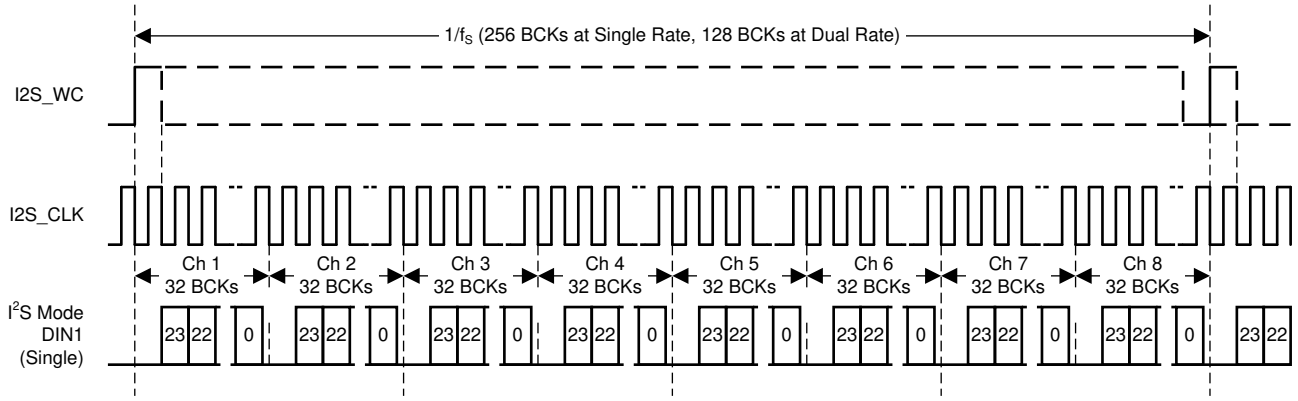


图 15. TDM Format

8.3.12 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

In BIST mode, the CRC Status for the back channel is brought out on either the MCLK or REM_INTB pin. In Splitter mode or Independent 2:2 mode, REM_INTB is used, otherwise MCLK is used. CRC Status for the second back channel is brought out on the SCLK pin.

In Splitter mode or Independent 2:2 mode, the BIST function is enabled independently for each port.

8.3.12.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external Pixel clock or the internal Oscillator clock (OSC) frequency. In the absence of the external pixel clock, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See 图 16 for the BIST mode flow diagram.

Step 1: The Serializer is paired with an FPD-Link III Deserializer, BIST Mode is enabled through the BISTEN pin or through register 0x24[0] on the Deserializer or 0x14[0] on the Serializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x04[5] be toggled locally on the Serializer (set 0x04[5]=1, then set 0x04[5]=0). The desired clock source is selected through the deserializer BISTC pin or through the register on the Deserializer.

Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there were one or more errors detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. The BIST duration is user-controlled by the duration of the BISTEN signal.

Step 4: The link returns to normal operation after the deserializer BISTEN pin is low. 图 17 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission, and so forth), thus they may be introduced by greatly extending the cable length or faulting the interconnect medium.

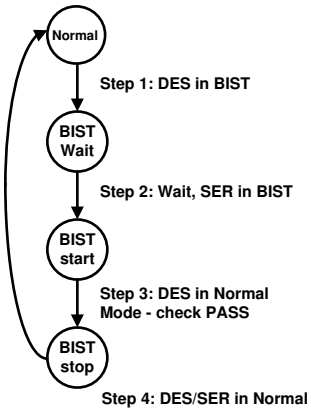


图 16. BIST Mode Flow Diagram

8.3.12.2 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sampling the DSI input pins and switches over to an internal all-zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, and so forth, and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back channel data is checked for CRC errors when the serializer locks onto the back channel serial stream, as indicated by link detect status (register bit 0x0C[0] - *Main Registers*). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.

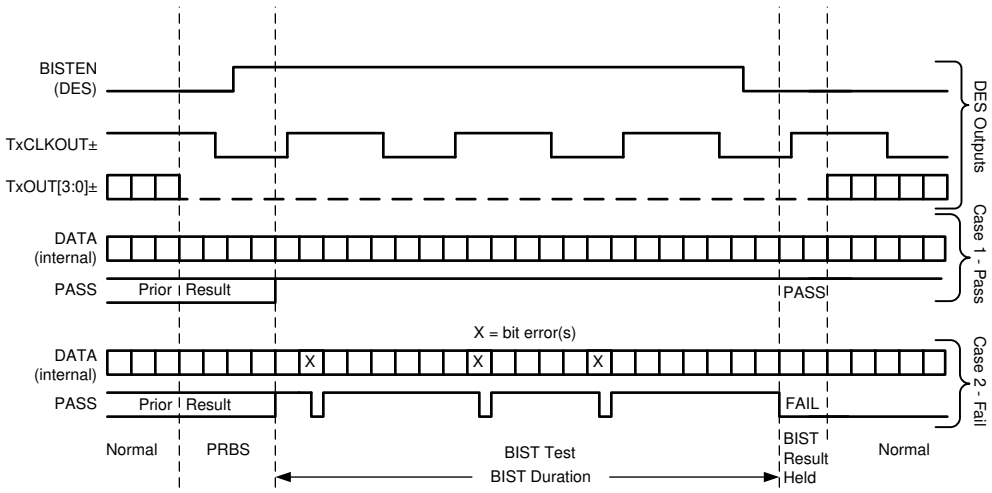


图 17. BIST Waveforms in Conjunction With Deserializer Signals

8.3.13 Internal Pattern Generation

The DS90UB941AS-Q1 serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power-down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to the *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices* application note (SNLA132).

In Pattern Generator BIST mode, the CRC Status for the back channel is brought out on either the MCLK or REM_INTB pin. In Splitter mode or Independent 2:2 mode, REM_INTB is used, otherwise MCLK is used. CRC Status for the second back channel is brought out on the SCLK pin.

8.3.13.1 Pattern Options

The DS90UB941AS-Q1 serializer pattern generator is capable of generating 17 default patterns for use in basic testing and debugging of panels. Each can be inverted using PATGEN_INV 0x65[1] register bit (see *Main Registers*). Patterns are shown below:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White

8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color (or its inversion) configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

Additionally, the Pattern Generator incorporates one user-configurable, full-screen, 24-bit color controlled by the PGRS, PGGS, and PGBS registers. This is pattern #14. One of the pattern options is statically selected in the PGCTL register when Auto-Scrolling is disabled. The PGTSC and PGTSO1-8 registers control the pattern selection and order when Auto-Scrolling is enabled.

8.3.13.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (*Main Registers*). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled. The 2 least significant bits will be 0.

8.3.13.3 Video Timing Modes

The Pattern Generator has two video timing modes – external and internal. In external timing mode, the Pattern Generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the Pattern Generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the Pattern Generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or Internal timing with External Clock are enabled by the control registers (*Main Registers*).

8.3.13.4 External Timing

In external timing mode, the Pattern Generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two pixel clock delay. It extracts the active frame dimensions from the incoming signals to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the Pattern Generator determines the Vertical Blank time by detecting a long period of pixel clocks where the DE is not asserted.

8.3.13.5 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

8.3.13.6 Auto-Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

8.3.13.7 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Registers (see Table 159).

8.3.14 EMI Reduction Features

8.3.14.1 Input SSC Tolerance

The DS90UB941AS-Q1 serializer is capable of tracking a triangular input spread spectrum clocking (SSC) profile up to ±0.25% amplitude deviations (center spread) or up to 0.5% amplitude deviations (up or down spread), up to 33 kHz modulation at 25 MHz - 210 MHz, from a host source.

8.4 Device Functional Modes

8.4.1 Mode Select Configuration Settings (MODE_SEL[1:0])

Configuration of the device may be done through the MODE_SEL[1:0] input pins, or through the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs. See and . These values will be latched into register location during power up:

表 8. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
DSI LANES	00	1 Lane
	01	2 Lanes
	10	3 Lanes
	11	4 Lanes
SPLITTER Mode	0	Normal operation.
	1	Split video (odd/even) to each FPD-Link III output port based on DSI virtual channels.
DISABLE DSI	0	DSI inputs enabled.
	1	DSI inputs disabled. This is a recommended strap option as any configuration of DSI inputs needs to be done while the inputs are disabled.
COAX Mode	0	Enable FPD-Link III for twisted pair cabling.
	1	Enable FPD-Link III for coaxial cabling.
CLOCK Mode	0	FPD-Link III is generated from DSI clock. The DSI clock has to be continuous.
	1	FPD-Link III is generated from external oscillator provided to REFCLK pin(s). The DSI clock may be continuous or discontinuous.

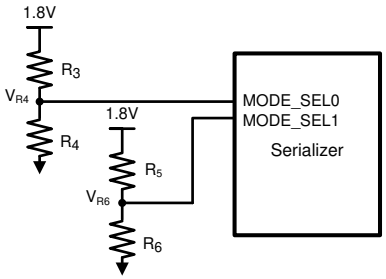


图 18. MODE_SEL[1:0] Connection Diagram

表 9. Strap Configuration MODE_SEL0

MODE NO.	V_{R4} VOLTAGE			V_{R4} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		SPLITTER	DSI LANES
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_3 (kΩ)	R_4 (kΩ)		
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	0	1
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.38	73.2	20.0	0	2
2	0.286 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	0	3

表 9. Strap Configuration MODE_SEL0 (接下页)

MODE NO.	V_{R4} VOLTAGE			V_{R4} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		SPLITTER	DSI LANES
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_3 (kΩ)	R_4 (kΩ)		
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	0	4
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	1	1
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	1	2
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	1	3
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	1	4

表 10. Strap Configuration MODE_SEL1

MODE NO.	V_{R6} VOLTAGE			V_{R6} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		CLOCK	COAX	DISABLE DSI
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_5 (kΩ)	R_6 (kΩ)			
0	0	0	0.126 × $V_{(VDD18)}$	0	OPEN	10.0	0	0	0
1	0.179 × $V_{(VDD18)}$	0.211 × $V_{(VDD18)}$	0.244 × $V_{(VDD18)}$	0.380	73.2	20.0	0	0	1
2	0.286 × $V_{(VDD18)}$	0.325 × $V_{(VDD18)}$	0.364 × $V_{(VDD18)}$	0.585	60.4	30.1	0	1	0
3	0.404 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.472 × $V_{(VDD18)}$	0.794	51.1	40.2	0	1	1
4	0.526 × $V_{(VDD18)}$	0.556 × $V_{(VDD18)}$	0.590 × $V_{(VDD18)}$	1.001	40.2	51.1	1	0	0
5	0.643 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.708 × $V_{(VDD18)}$	1.211	30.1	61.9	1	0	1
6	0.763 × $V_{(VDD18)}$	0.790 × $V_{(VDD18)}$	0.825 × $V_{(VDD18)}$	1.421	18.7	71.5	1	1	0
7	0.880 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	1	1	1

表 11. Mode Select [1.0] Registers

Strapping Value	Reg Name	Bit Field	Description
MODESEL0 - SPLITTER	DUAL_CTL1, AUDIO_CFG	[2:0], [4]	FPD3_TxMode, Split_Autio
MODESEL0 - DSI LANES	BRIDGE_CTL	[3:2]	number DSI lanes per port
MODESEL1 - CLOCK	BRIDGE_CTL, BRIDGE_CFG2	[7], [1:0]	DSI Continuous Clock, Bridge Clock Mode
MODESEL1 - COAX	DUAL_CTL1	[7]	FPD3_Coax or STP mode
MODESEL1 - DISABLE DSI	RESET_CTL	[7]	disable DSI for Mode change update

8.4.2 Clock Modes

8.4.2.1 DSI Clock Modes

The DS90UB941AS-Q1 supports both continuous and discontinuous clocking on the DSI interface. It may be set by selecting appropriate resistor on the MODE_SEL1 pin or configured in the BRIDGE_CTL register bit 7. Note: Clock selection for DSI clock, external clock for FPD3 are in I2C register writes for each Tx FPD3 port.

- 0: DISCONTINUOUS DSI CLOCK MODE: For operation with discontinuous DSI clock, set the MODEL_SEL1 pin to MODE 4, 5, 6, or 7 per or configure BRIDGE_CTL[7]=0.

- 1: CONTINUOUS DSI CLOCK MODE: For operation with continuous DSI clock, set the MODEL_SEL1 pin to MODE 0, 1, 2, or 3 per or configure BRIDGE_CTL[7]=1.

8.4.2.2 Pixel Clock Modes

The DS90UB941AS-Q1 supports four Pixel Clock modes. These modes determine the reference clock for the FPD-Link III interface. It may be configured in the BRIDGE_CFG2[1:0] register bits.

- 00: DSI Reference Clock Mode
- 01: External Reference Clock Mode
- 10: Internal Reference Clock Mode
- 11: External Reference Clock for Independent 2:2 Mode

8.4.2.2.1 DSI Reference Clock Mode

In this mode, the DSI clock is the reference clock for the FPD-Link III interface. The DSI clock must be continuous and BRIDGE_CTL[7] register bit set. The DSI clock needs to meet necessary jitter requirements. In this mode, FPD-Link III transmitter is synchronous to DSI clock. The pixel clock frequency is related to the DSI clock frequency as given in 公式 2.

$$f_{PCLK} = \frac{f_{DSI} \cdot N_{DSI\_Lanes}}{12} \quad (2)$$

Sync Pulses: In typical DSI Reference Clock mode operation, the Vertical Sync (VS) and Horizontal Sync (HS) signals are regenerated on FPD-Link III using their original timing on the DSI interface. The following DSI packets are used with Sync Pulses:

- 0x01: VSYNC_START (VSS); also implies HSS
- 0x11: VSYNC_END (VSE); also implies HSS
- 0x21: HSYNC_START (HSS)
- 0x31: HSYNC_END (HSE)

The VS pulse width (in lines) on FPD-Link III equals the total number of lines (that is, the total number of HSS packets including the VSS packet) between the VSS and VSE packet. When exact video timing is in the process of reconstruction, the VS pulse width must be an integer number of pixel clocks.

The HS pulse width (in pixel clocks) on FPD-Link III equals the number of pixel clocks between the end of the HSS packet and the end of the HSE packet. When exact video timing is in the process of reconstruction, the HS pulse width must be an integer number of pixel clocks.

Sync Events: If the DSI source is configured to only send Sync Events, the DS90UB941AS-Q1 generates VS and HS pulses on FPD-Link III as configured in registers. The following DSI packets are used with Sync Events:

- 0x01: VSYNC_START (VSS); also implies HSS
- 0x21: HSYNC_START (HSS)

Configuring Sync Events: Enabling Sync Event support is done in the DSI indirect register DSI_CONFIG_0 (0x20). The HS and VS pulse widths are independently configurable in the DSI indirect registers DSI_HSW_CFG and DSI_VSW_CFG.

8.4.2.2.2 External Reference Clock Mode

In this mode, an external reference clock provided to the REFCLK0 pin is the reference clock for the FPD-Link III interface. The external clock needs to meet necessary jitter requirements. In this mode, the DSI clock may be continuous or discontinuous.

8.4.2.2.3 Internal Reference Clock

In this mode, the reference clock for the FPD-Link III interface is derived from an internal Always-On clock. In this mode, the DSI clock may be continuous or discontinuous. Typically, this mode is used for debugging purposes as the internal reference clock does not meet the necessary jitter requirements.

8.4.2.2.4 External Reference Clock for Independent 2:2 Mode

This mode is used when external reference clocks are need for both channels in Independent 2:2 Mode. In this mode, an external reference clock provided to the REFCLK0 pin is the reference clock for the FPD-Link III Port0 interface while an external reference clock provided to the REFCLK1 pin is the reference clock for the FPD-Link III Port1 interface. Both external clocks need to meet necessary jitter requirements. In this mode, the DSI clock may be continuous or discontinuous.

8.4.3 Dual-DSI Input Mode

In Dual-DSI input mode, both DSI input ports are active, delivering a single video stream to the DS90UB941AS-Q1. The DS90UB941AS-Q1 merges the incoming video into a single image. This operation supports two basic types of video on the input:

- Single image, alternating pixels. First pixel is on DSI Port 0, second pixel is on DSI Port 1.
- Dual image (for example, 3D image) where Left image is on DSI Port 0 and Right image is on DSI Port 1

Processing for both of these conditions is the same. The input is merged into a single video image in an alternating pixel format, with a pixel clock period that is twice the frequency of the single-port DSI pixel clock frequency as shown in 图 19.

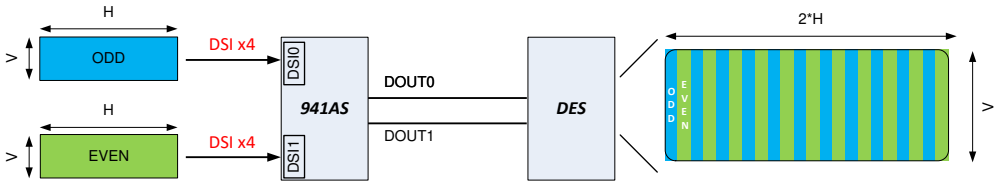


图 19. Aggregation of Dual-DSI Input into an Alternating Pixel Format

The third option merges a dual image into a Left/Right format rather than an alternating pixel format as shown in 图 20. This option results in an image that cannot easily be split by FPD-Link III devices. It can be used for forwarding the combined image to a downstream panel or processor that requires this format.

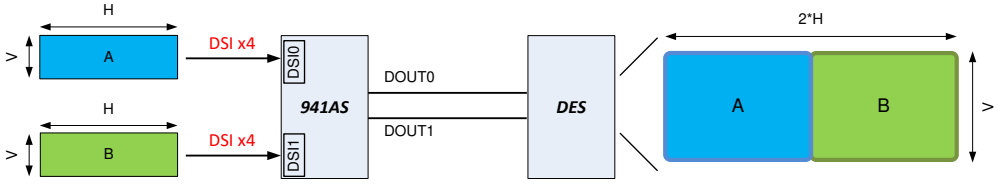


图 20. Aggregation of Dual-DSI Input into a Left/Right Format

8.4.3.1 Dual DSI Operation Requirements

The Dual-DSI input mode has the following requirements for proper operation:

- The DSI inputs must send identical framed video
- Skew between DSI ports must be less than two pixel clock periods (single DSI pixel clock frequency)
- The FPD-Link III Transmitter has to operate in Dual FPD-Link III mode
- DSI inputs must operate in Continuous DSI Clock mode

8.4.3.2 Enabling Dual-DSI Operation

Dual-DSI mode is enabled by setting the DUAL_DSI_EN bit in the BRIDGE_CTL register to 1. Enable this mode before enabling the DSI receiver.

The Left/Right merge option is enabled by setting the DUAL_DSI_LR_EN bit in the BRIDGE_CFG2 register. In addition, for Left/Right merge, line length and delay parameters must be set in the IMG_LINE_SIZE and IMG_DELAY registers. The IMG_LINE_SIZE is set to the 2D image line length. The IMG_DELAY value is typically set to the default setting of 12 pixels.

For Dual-DSI modes, the DSI_PORT_SEL bit in the BRIDGE_CTL register should be set to 0.

8.4.3.3 Dual-DSI Control and Status

The DUAL_DSI_CTL_STS register includes status for the skew between DSI input ports. If the skew is 3 pixels or less, it will be reported in this register. Status in this register is current status only, so it may not always report transient conditions if skew is varying from one video line to the next.

The DUAL_DSI_CTL_STS register also provides skew control for input paths. Each input port may be delayed by up to 3 pixels. This allows diagnostics checking of skew tolerance and skew detection. In addition, if the input streams have known skew, the skew control can be used to compensate for up to 3 pixels skew between the channels.

8.4.4 3D Format Support (Single-DSI Input)

The DS90UB941AS-Q1 supports three 3D format options for receiving video from a single DSI input.

- Left/Right 3D format
- Alternate Line 3D format
- Alternate Pixel 3D format

For the first two options, the DS90UB941AS-Q1 reorganizes the image into an alternating pixel format for easy splitting at the DS90UB941AS-Q1 output or at a downstream DS90UB948-Q1. For the Alternate Pixel option, the image is already in the proper format for splitting.

For proper transition between operating modes, enabling 3D modes should be done when the DSI input is disabled.

If Independent 2:2 Mode is enabled, Left/Right or Alternate Line processing is only available on the primary DSI to FPD-Link III path.

8.4.4.1 Left/Right 3D Format Support

The DS90UB941AS-Q1 supports reception of a dual-image video input where the dual-image is delivered as a side-by-side (left/right) image, consistent with the side-by-side 3D format specified in the HDMI 1.4b specification. The DS90UB941AS-Q1 can be programmed to merge the left/right formatted video into a single image with alternating pixels. The resultant image has same number of lines of same size, but pixels are reordered. This image can be split by the DS90UB941AS-Q1 and sent to two independent deserializers (using Splitter Mode), or may be sent to a downstream DS90UB948-Q1 for splitting into two images at the deserializer.

The following are requirements for proper operation:

- Images must have identical video format (lines, pixels, blanking intervals)
- Pixel clock used must be twice the frequency as needed for sending a single image
- Horizontal blanking components (front porch, sync period, back porch) must be twice the number of pixels as required for a single image
- Vertical blanking periods should be the same number as required for a single image
- Maximum line size of 8192 pixels (24-bit) for the combined image

Left/Right input mode is enabled by setting the LEFT_RIGHT_3D register bit in the BRIDGE_CFG2 register (register 0x56[7]). Software must also set the 2D image line size, IMG_LINE_SIZE (registers 0x32 and 0x33), as well as the IMG_DELAY control (registers 0x34 and 0x35). The IMG_DELAY is used to properly delay image regeneration and should typically be set to a small value (i.e. 12 clocks). The default settings of IMG_LINE_SIZE is based on default 720p60 timing (1280 x 720 at 60 fps), with line size of 1280. Note, if Splitter Mode is enabled, the IMG_DELAY may be set separately for each port.

Left/Right video processing status can be monitored in the VIDEO_3D_STS register (register 0x58).

The image may be split at the DS90UB941AS-Q1 or at a downstream Deserializer (i.e. DS90UB948-Q1). Examples of splitting are shown in 图 21 and 图 22.

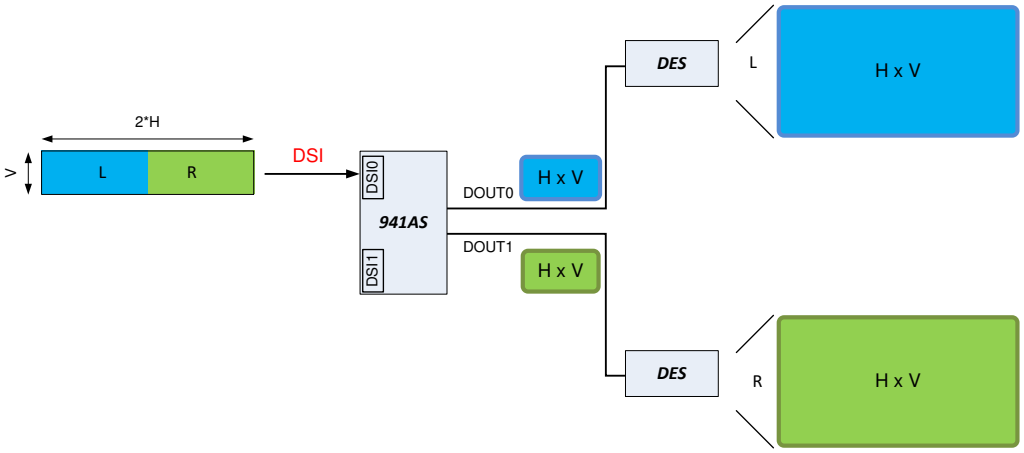


图 21. Splitting at Serializer Option

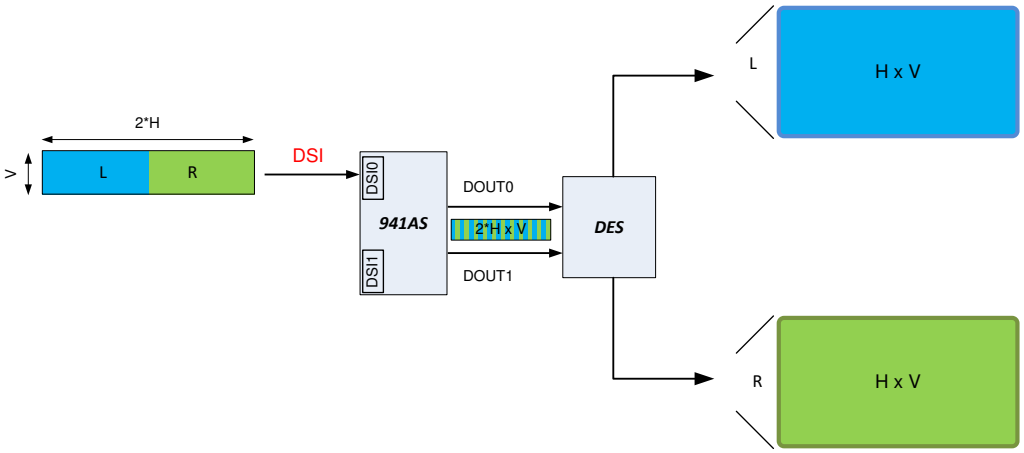


图 22. Splitting at Deserializer Option

8.4.4.2 Alternate Line 3D Format Support

The DS90UB941AS-Q1 supports reception of a dual-image video input where the dual-image is delivered as alternating lines of video data, consistent with the Line Alternate 3D format specified in the HDMI 1.4b specification. The DS90UB941AS-Q1 can be programmed to merge the alternate line formatted video into a single image with alternating pixels. The resultant image has ½ the number of video lines that are twice the length. This image can be split by the DS90UB941AS-Q1 at the FPD-Link III output and sent to two independent deserializers (using Splitter Mode), or may be sent to a downstream DS90UB948-Q1 for splitting into two images at the deserializer.

The following are requirements for proper operation:

- Images must have identical video format (lines, pixels, blanking intervals)
- Pixel clock used must be twice the frequency as needed for sending a single image
- Vertical blanking components (front porch, sync period, back porch) must be twice the number of video line periods as required for a single image
- Horizontal blanking periods should be the same number of pixels as required for a single image. Note, there are twice as many blanking periods for the dual image as there are for a single image.
- Maximum line size of 4095 pixels (24-bit)

Alternate Line mode is enabled by setting the ALT_LINES_3D register bit in the BRIDGE_CTL register (register 0x4F[4]).

Alternate Line video processing status can be monitored in the ALT_LINE_STS register (register 0x58).

8.4.4.3 Alternate Pixel 3D Format Support

The DS90UB941AS-Q1 supports reception of a dual-image video input where the dual-image is delivered as alternating pixels. The DS90UB941AS-Q1 does not need to do any special processing on this image format. This image can be split by the DS90UB941AS-Q1 and sent to two independent deserializers (using Splitter Mode), or may be sent to a downstream DS90UB948-Q1 for splitting into two images at the deserializer.

The following are requirements for proper operation:

- Images must have identical video format (lines, pixels, blanking intervals)
- Pixel clock used must be twice the frequency as needed for sending a single image
- Horizontal blanking components (front porch, sync period, back porch) must be twice the number of pixels as required for a single image
- Vertical blanking periods should be the same number as required for a single image
- Maximum line size of 4095 pixels (24-bit)

Alternate Pixel mode is the default mode of operation for the DS90UB941AS-Q1.

If Splitter Mode is enabled, to properly regenerate Horizontal Sync timing, there are two options. The preferred option is to use the default setting for the IMG_DELAY and enable register override of the Horizontal Sync and Horizontal Back porch periods for each port, using the IMG_HSYNC_CTLx registers. The second option is to allow automatic generation of the Horizontal Sync timing and set the IMG_DELAY value to greater than the Horizontal Sync period plus the Horizontal Back Porch period for the 3D image in pixels.

8.4.5 Independent 2:2 Mode

In Independent 2:2 mode, DS90UB941AS-Q1 DSI receiver accepts two independent DSI inputs (two streams) and outputs to two independent deserializers links. One video stream is input on DSI0 and output via a single link on DOUT0. Another video stream is input on DSI1 and output via a single link on DOUT1. In this mode, DSI0 and DSI1 can each have a different number of DSI data lanes enabled, different DSI clock frequency and the video format for each DSI can be different.

The DSI inputs may be swapped to map DSI0 to DOUT1, and DSI1 to DOUT0 by setting the DSI_PORT_SEL bit in the BRIDGE_CTL register.

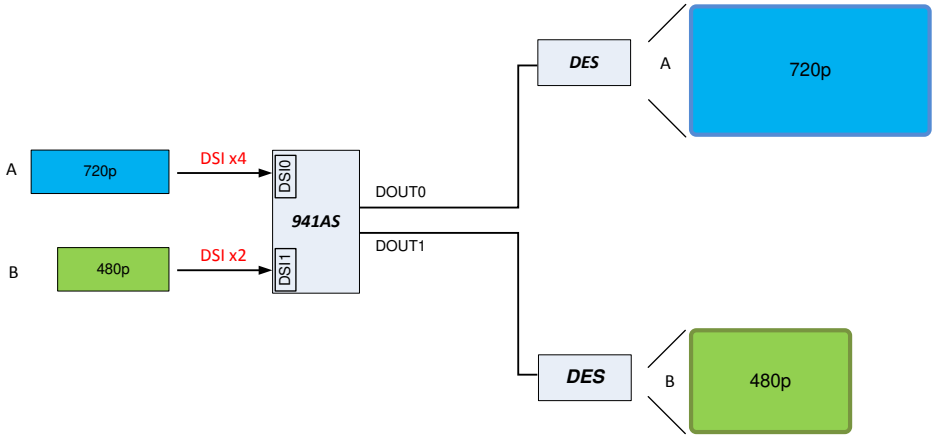


图 23. Independent 2:2 Mode With DSI Reference Clock

When in Continuous DSI Reference Clock mode (图 23), each DSI clock is used to determine the clock rate for each FPD-Link III lane. When in External Reference Clock mode, each external clock is used to determine the clock rate for each FPD-Link III lane. In this mode, Port0 clock is on the REFCLK0 pin, while Port1 clock is on the REFCLK1 pin as shown in 图 24.

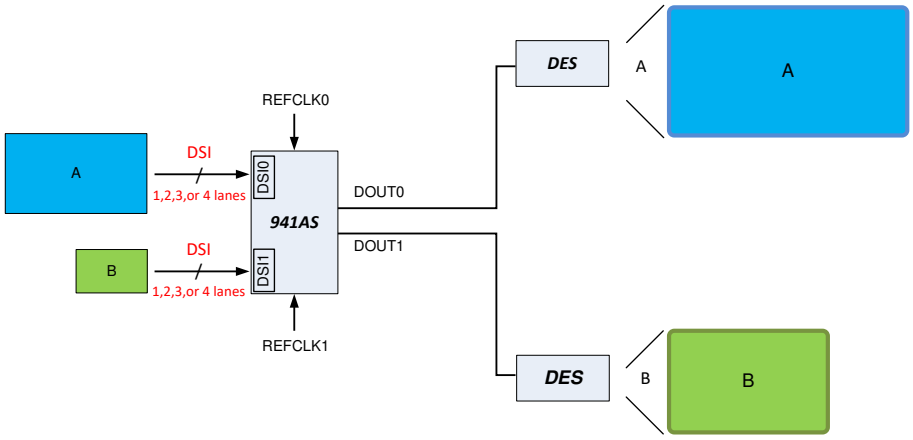


图 24. Independent 2:2 Mode With External Reference Clocks

In addition, when operating in the Independent 2:2 Mode, the device may use an internal reference clocks derived from the internal Always-On clock. Each port can operate with an independent timing based on an M/N clock divider from the 800 MHz internal reference.

8.4.5.1 Configuration of Independent 2:2 Mode

Independent 2:2 mode should be enabled while the DSI inputs are disabled. This ensures proper startup of the device. The device should initially be strapped in the DSI Disabled state, configured to Independent 2:2 mode by setting the FPD3_TX_MODE[2:0] bits in register DUAL_CTL1 (0x5B) to 101, and then DSI enabled by setting the DISABLE_DSI bit in the RESET_CTL register to 0. The device will not allow writing to Port1 registers unless the device is configured for Independent 2:2 mode. Thus, Independent 2:2 mode should be enabled prior to configuring port 1 registers.

The following options may be configured for each port:

- DSI_CONTINUOUS_CLK – register 0x4F[7]
- DSI_LANES – register 0x4F[3:2]
- DSI_BYTES_PER_PIXEL – register 0x54[5:4]
- BRIDGE_CLK_MODE – register 0x56[1:0]
- FREQ_STBL_THR – register 0x5C[4:3]
- FREQ_HYST – register 0x5C[2:0]
- PatternGen direct and indirect registers – 0x64-0x69
- DPHY and DSI configurations via DSI indirect register page

The following Status is available for each port:

- FPD3_LINK_RDY – register 0x5A[7]
- FPD3_TX_STS – register 0x5A[6]
- DSI_CLK_DET – register 0x5A[3]
- NO_DSI_CLK – register 0x5A[1]
- FREQ_STABLE – register 0x5A[0]
- DPHY and DSI status via DSI indirect register page

8.4.5.2 Example Code for Configuring Independent 2:2 Mode

The example code configures the devices for transmitting 1080p video data from a 4-Lane DSI source to a remote display connected to FPD-Link Port 0 and 720p video data from another 4-Lane DSI source to another remote display connected to FPD-Link Port 1.

```
WriteI2C (0x01,0x08)    //Disable DSI
```

```
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x1E,0x04)    //Use I2D ID+1 for FPD-Link III Port 1 register access
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x03,0x9A)    //Enable I2C_PASSTHROUGH, FPD-Link III Port 0
WriteI2C (0x1E,0x02)    //Select FPD-Link III Port 1
WriteI2C (0x03,0x9A)    //Enable I2C_PASSTHROUGH, FPD-Link III Port 1
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x40,0x05)    //Select DSI Port 0 digital registers
WriteI2C (0x41,0x21)    //Select DSI_CONFIG_1 register
WriteI2C (0x42,0x60)    //Set DSI_VS_POLARITY=DSI_HS_POLARITY=1
WriteI2C (0x1E,0x02)    //Select FPD-Link III Port 1
WriteI2C (0x40,0x09)    //Select DSI Port 1 digital registers
WriteI2C (0x41,0x21)    //Select DSI_CONFIG_1 register
WriteI2C (0x42,0x60)    //Set DSI_VS_POLARITY=DSI_HS_POLARITY=1
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x5B,0x05)    //Force Independent 2:2 mode
WriteI2C (0x4F,0x8C)    //Set DSI_CONTINUOUS_CLOCK, 4 lanes, DSI Port 0
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x40,0x04)    //Select DSI Port 0 digital registers
WriteI2C (0x41,0x05)    //Select DPHY_SKIP_TIMING register
WriteI2C (0x42,0x16)    //Write TSKIP_CNT value for 315 MHz DSI clock frequency (1080p, PCLK = 105 MHz)
WriteI2C (0x1E,0x02)    //Select FPD-Link III Port 1
WriteI2C (0x4F,0x8C)    //Set DSI_CONTINUOUS_CLOCK, 4 lanes, DSI Port 1
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x40,0x08)    //Select DSI Port 1 digital registers
WriteI2C (0x41,0x05)    //Select DPHY_SKIP_TIMING register
WriteI2C (0x42,0x0C)    //Write TSKIP_CNT value for 225 MHz DSI clock frequency (720p, PCLK = 75 MHz)
WriteI2C (0x01,0x00)    //Enable DSI
```

8.4.6 FPD-Link III Modes of Operation

The FPD-Link III transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The following modes are supported:

8.4.6.1 Single-Link Mode

Single-Link mode transmits the video over a single FPD-Link III to a single receiver. Single-link mode supports frequencies up to 105 MHz for 24-bit video. This mode is compatible with the DS90UB926, DS90UB928 when operating at or below 85Mhz. This mode is compatible with the DS90UB948 when operating at or below 96 MHz.

If the downstream device is capable, the secondary FPD-Link III can be used for high-speed control.

In Forced Single-Link mode (set through the DUAL_CTL1 register), the secondary TX PHY and back channel are disabled. In addition, access to port 1 registers is prevented.

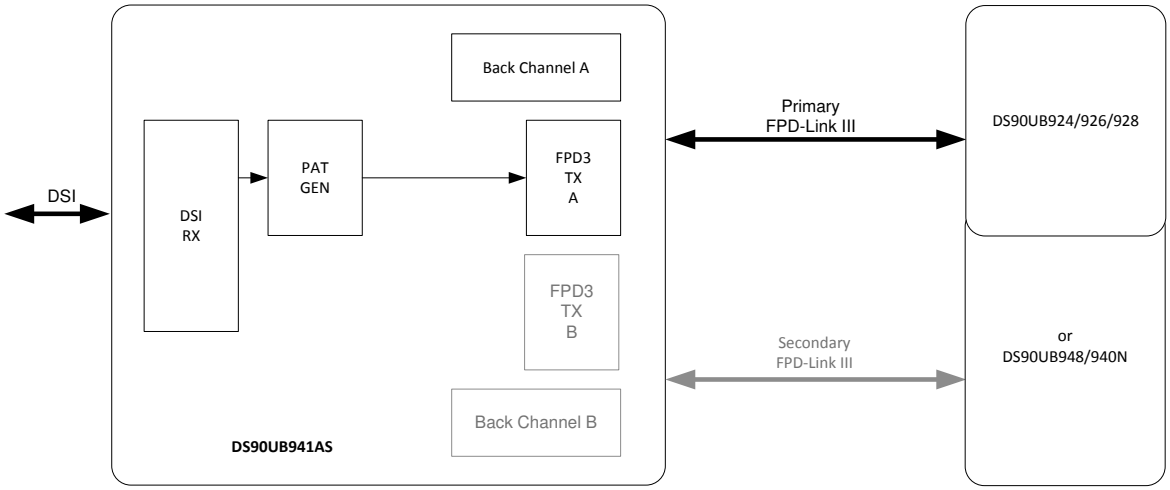


图 25. Single-Link, 1:1 Mode

8.4.6.2 Dual-Link Mode

In Dual-link mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links. The receiver must be a DS90UB948-Q1 or DS90UB940N-Q1 (up to 170-MHz pixel clock) capable of receiving the dual-stream video. Dual-link mode is capable of supporting a pixel clock frequency of up to 210 MHz, with each FPD-Link III TX port running at one-half the frequency. The secondary FPD-Link III may be used for high-speed control.

Dual-link mode may be automatically configured when connected to a DS90UB948-Q1 or DS90UB940N-Q1, if the video meets the minimum frequency requirements. Dual Link mode may also be forced using the DUAL_CTL1 register.

In Dual-link mode, Bidirectional Control Channel operation is available only on the primary link.

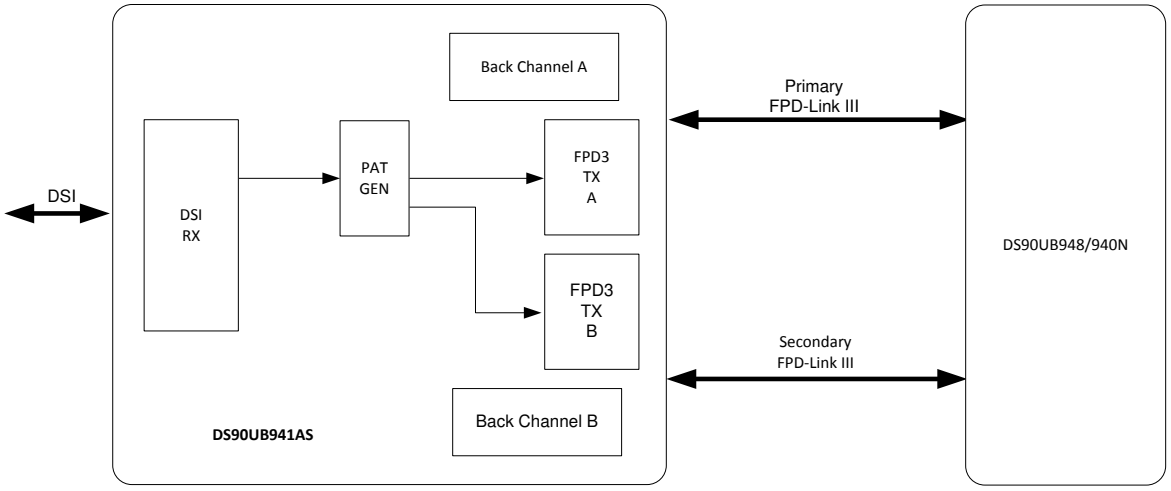


图 26. Dual-Link, 1:2 Mode

8.4.6.3 Replicate Mode

In this mode, the same video is delivered to each receiver. Tthe FPD-Link III TX operates as a 1:2 Repeater. The same video (up to 105 MHz, 24-bit color) is delivered to each receiver.

Replication mode may be automatically configured when connected to two independent Deserializers.

During Replication mode, Bidirectional Control Channel operation is available on both links independently.

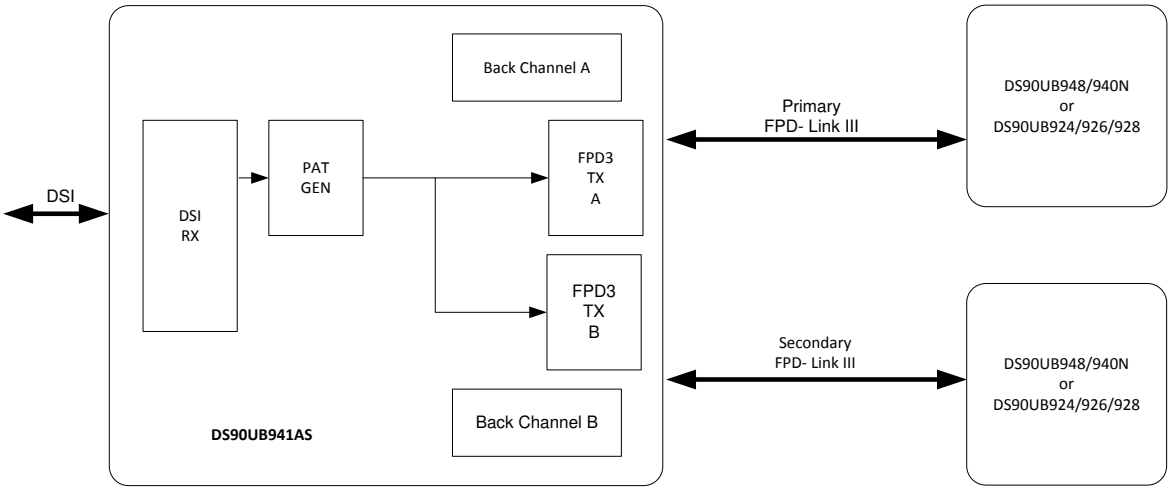


图 27. Replicate Mode

8.4.6.4 Splitter Mode

In Splitter Mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links to two independent Deserializers. Each path has a Pattern Generator to generate the video stream for that FPD-Link III output. Splitter Mode cannot be used with the auto-detect feature. Instead, the device needs to be programmed into Splitter mode through either the registers or strap options at power up. Note: the DS90Ux941AS-Q1 Cropping Calculator, on the TI website, can be used to help setup the splitter and cropping register programming.

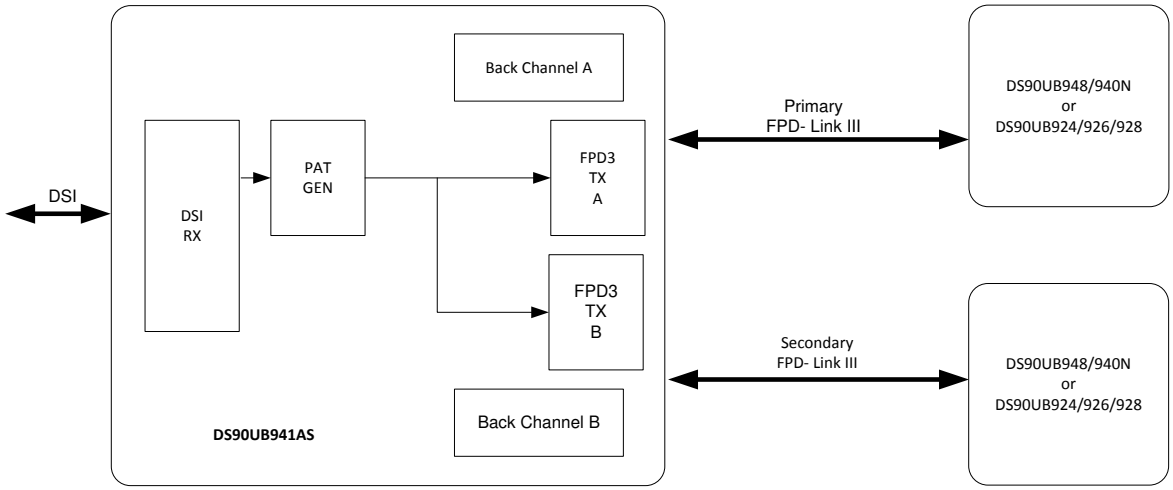


图 28. Splitter Mode

Splitter mode does not operate with Dual-DSI inputs. For sending multiple video frames, the source should use Independent 2:2 mode instead.

In Splitter mode, Bidirectional Control Channel operation is available on both links independently.

8.4.6.4.1 DSI Symmetric Splitting

The DS90UB941AS-Q1 DSI receiver supports asymmetric video frame and splits the content into separate video streams. In this mode, stream A outputs on DOUT0 and stream B outputs on DOUT1. The following subsections describe possible implementations.

8.4.6.4.1.1 Symmetric Splitting – Left/Right

Single Input on DSI0 or DSI1 (side by side) with Left pixels received on DOUT0 and Right pixels received on DOUT1. The following are the requirements:

- DSI input horizontal total pixel is twice the number of Left or Right pixel.
- The split of Left and Right video must contain identical video formats and parameters.
- Hactive(A) = Hactive(B); Vactive(A) = Vactive(B)

  The dual-image video input is arranged as a side-by-side (left/right) image packed based on side-by-side 3D format specified in the HDMI 1.4b specification.

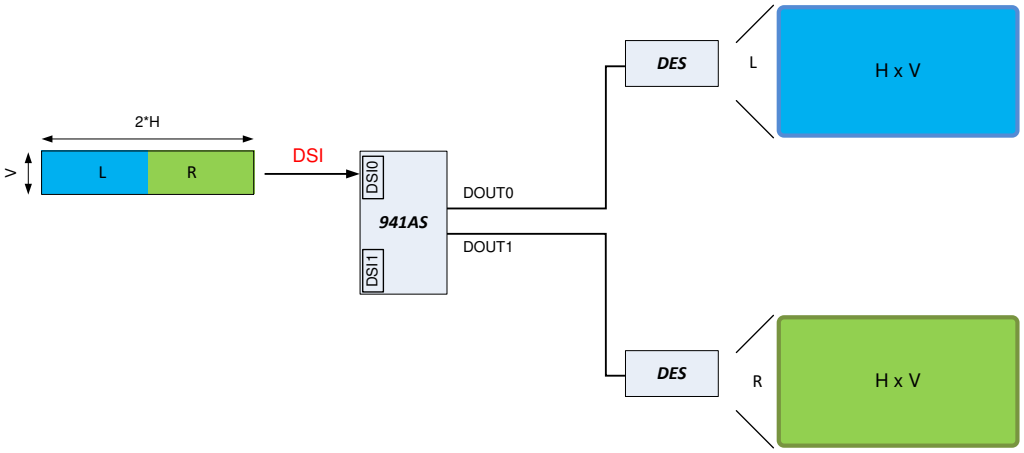


图 29. Single DSI Input to Left/Right (Side by Side) Splitting

8.4.6.4.1.2 Symmetric Splitting – Alternate Pixel Splitting

Single Input on DSI0 or DSI1 with alternating pixels carrying A+B video stream. A pixels output on DOUT0 and B pixels output on DOUT1. DSI0 or DSI1 must have same number of data lanes and video formats. The following are the requirements:

- DSI input horizontal total pixel is twice the number of Left or Right pixel.
- The split of A and B video must contain identical video formats and parameters.
- Hactive(A) = Hactive(B); Vactive(A) = Vactive(B)

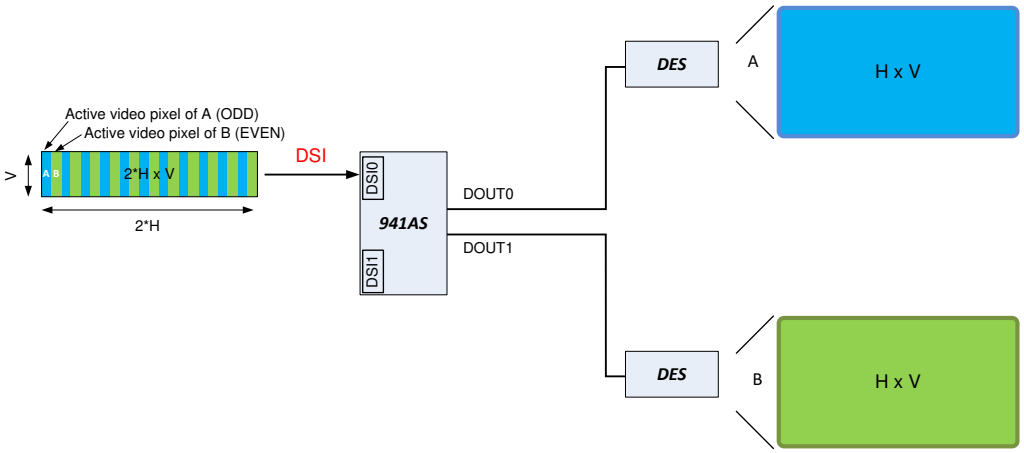


图 30. Alternate Pixel Splitting

8.4.6.4.1.3 Symmetric Splitting – Alternate Line Splitting

Single Input on DSI0 or DSI1 with alternating lines carrying A+B video stream. A lines output on DOUT0 and B lines output on DOUT1. DSI0 or DSI1 must have same number of data lanes and video formats. The following are the requirements:

- DSI input vertical total is twice the number of A or B vertical lines.
- The split of A and B video must contain identical video formats and parameters.
- Hactive(A) = Hactive(B); Vactive(A) = Vactive(B)

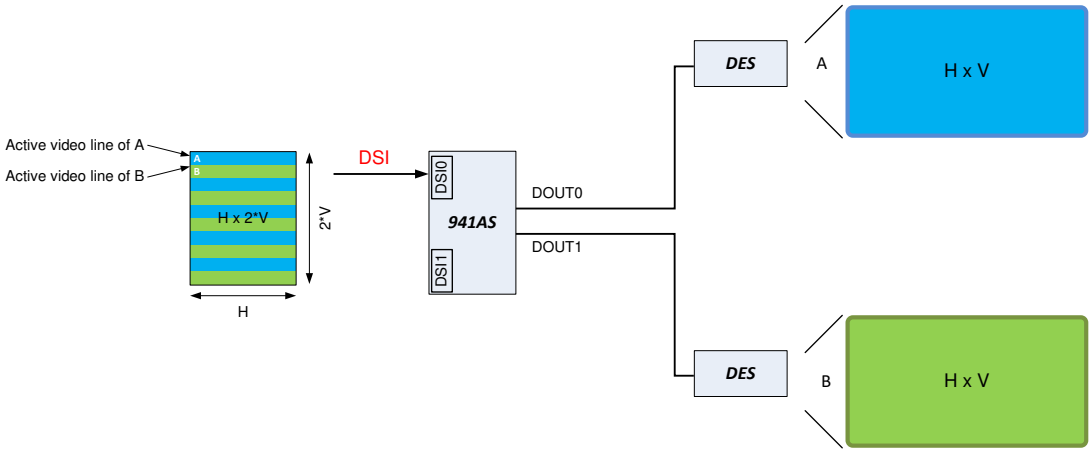


图 31. Alternate Line Splitting

8.4.6.4.2 DSI Asymmetric Splitting

The DS90UB941AS-Q1 DSI receiver supports asymmetric video frame and splits the content into separate video streams. In this mode, stream A outputs on DOUT0 and stream B outputs on DOUT1. The following subsections describe possible implementations.

8.4.6.4.2.1 Asymmetric Splitting With Cropping

图 32 shows one DSI asymmetric video stream input on DSI0 (DSI1 also possible) and split into 2 different video resolutions.

In this mode, a single DSI video input may contain two sets of video data with different formats and parameters. The cropped image at the output has a reduced size, but keeps line timing, resulting in a larger vertical blanking.

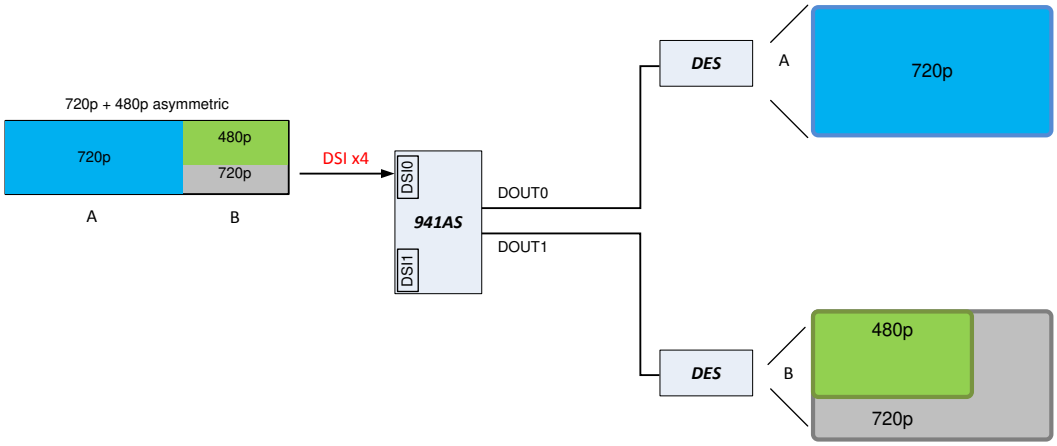


图 32. Asymmetric Splitting With Cropping

Asymmetric splitting of frames can be accomplished by cropping the resultant output images. The input video requirements are the same for the symmetric splitting. The superframe must include two identical size images. Those images will be cropped in both the horizontal and vertical dimensions to produce reduced size images. Note, the clock frequency remains ½ the frequency of the superframe. In addition, the horizontal and vertical blanking intervals are increased by the magnitude of the cropping.

Configuration of asymmetric splitting is handled by enabling image cropping for each of the images. For each image to be cropped, the horizontal and vertical dimensions must be programmed.

Cropping is controlled by the CROP_START_X/Y and CROP_STOP_X/Y registers for each port. For each port, the CROP_ENABLE is bit 7 of the CROP_START_X1 register.

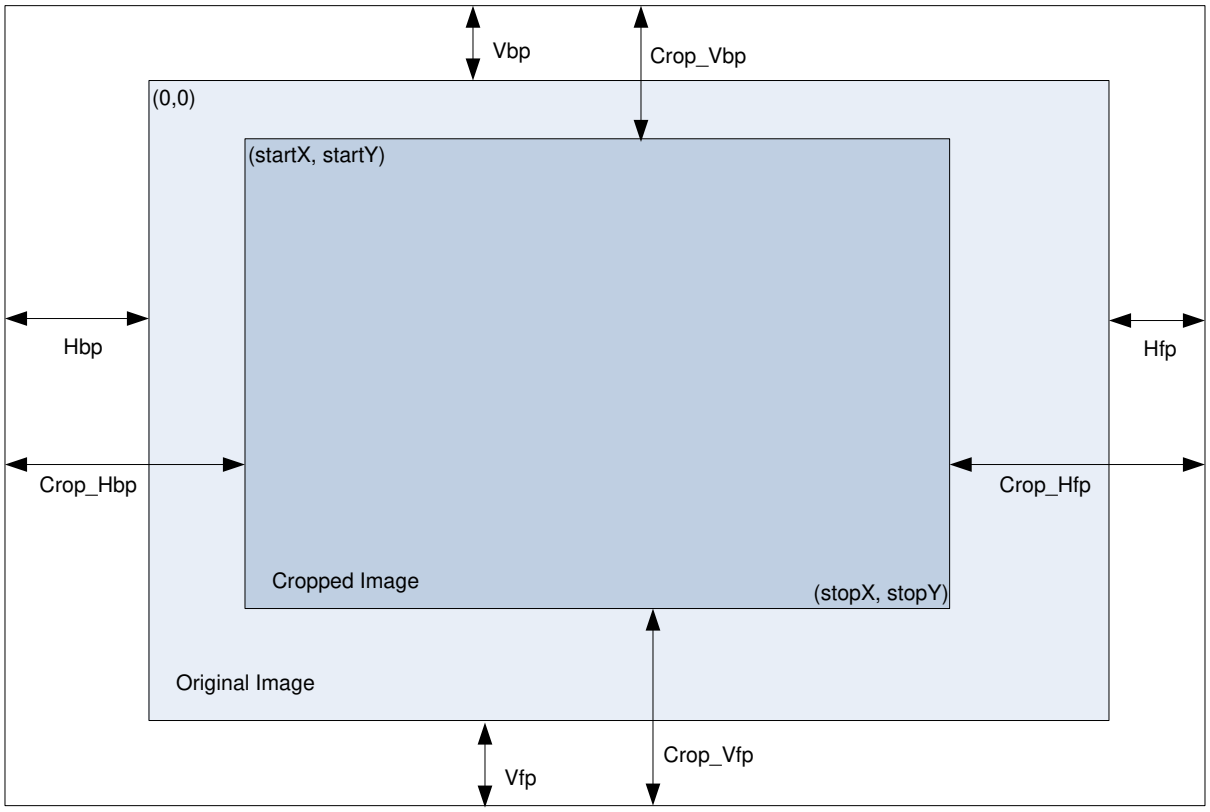


图 33. Cropping Example

In addition to cropping options, the Horizontal Sync width and Horizontal Back Porch period may be modified. Typically, these values are automatically generated based on the input video (1/2 of the values in the dual-image), but these can be overridden by setting the IMG_HSYNC_CTL registers. The Horizontal Sync period and the Horizontal Back Porch can be individually overridden by setting the HSYNC_OV_EN or HBACK_OV_EN controls as well as the IMG_HSYNC and IMG_HBACK parameters.

By default, asymmetric splitting generates each resultant image at ½ frequency of the superframe image. Options exist to use externally supplied reference clocks or 1/N divided versions of the DPHY Lane clock for each resultant image.

8.4.6.4.2.2 Asymmetric Splitting With DSI VC-IDs

The DS90UB941AS-Q1 can split images based on the DSI Virtual Channel ID. In this mode, the DSI input (single DSI only, not Dual-DSI) can include two images delineated by the Virtual Channel ID. These virtual channel images should each include proper vertical and horizontal sync pulses as well as independent video data. It is recommended that the images have identical line rates so that the merged image can still have accurate timing information. The DS90UB941AS-Q1 will split the two images onto separate FPD-Link III outputs based on the VC-ID.

An option exists to use a shared VSYNC for the two images. The two images should always have independent HSYNC controls.

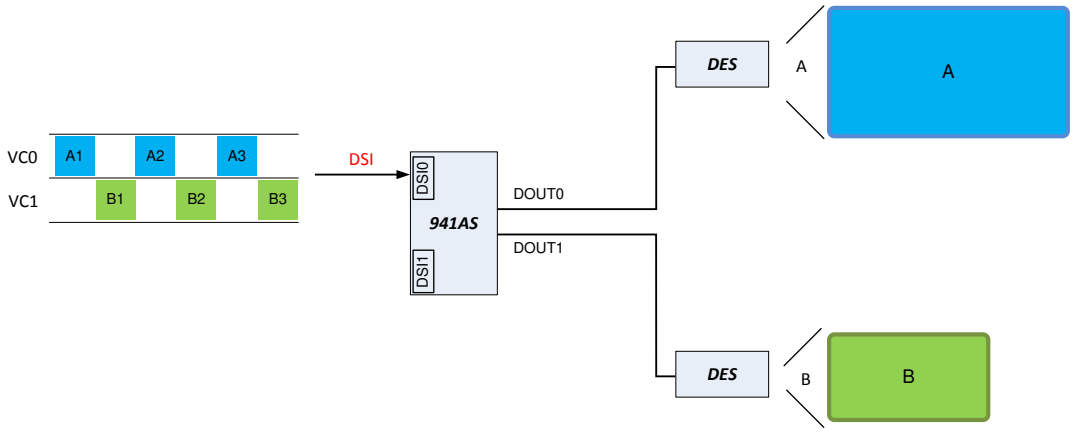


图 34. Asymmetric Splitting With VC-IDs

VC-ID splitting will reproduce video timing based on the received HSYNC timing on each port. By default, each port will begin forwarding delayed from the rising HSYNC edge. It will regenerate HSYNC width and back porch based on received values. To properly regenerate Horizontal Sync timing, there are two options. The preferred option is to use the default setting for the IMG_DELAY and enable register override of the Horizontal Sync and Horizontal Back porch periods for each port, using the IMG_HSYNC_CTLx registers. The second option is to allow automatic generation of the Horizontal Sync timing and set the IMG_DELAY value to greater than the Horizontal Sync period plus the Horizontal Back Porch period for the 3D image in pixels.

To maintain proper video timing, it is recommended that two images be sent via DSI in consistent packet order as follows (using Sync Event nomenclature from the DSI specification):

VSS_VCID0 – vertical sync start

VSS_VCID1 HSS_VCID0 – vertical blanking

HSS_VCID1
HSS_VCID0
HBP_VCID0

RGB_VCID0 -- video line for VCID0

HSS_VCID1
HBP_VCID1

RGB_VCID1 – video line for VCID1

….

In all cases, each video line should be sent as a single packet.

8.4.6.4.3 Configuration of Splitter Operation

Splitter operation should be configured prior to enabling the DSI inputs. This ensures the device enters the appropriate mode prior to forwarding video.

Splitter mode is enabled by selecting the Forced Splitter Mode selection on the FPD3_TX_MODE control in the DUAL_CTL1 register.

As described below, the device should be configured for proper splitter operation, dependent on dual-image process modes. The device will not allow writing to port 1 registers unless the device is configured for Splitter mode. Thus, Splitter mode should be enabled prior to configuring port 1 registers.

For Splitter mode, the IMG_DELAY value should be programmed to allow proper buffering of video. For Left/Right image processing or Alternate Line image processing, the default setting of 12 pixels is adequate, but cropping of output video may require setting of a larger value to prevent transmission before valid data is available. For Alternate Pixel format or VC-ID based splitting, the IMG_DELAY field should be programmed to be greater than the sum of the Horizontal Sync period plus the Horizontal Back porch period for the 3D image in pixels. The IMG_DELAY is programmable for each port.

For Left/Right image processing or Alternate Line image processing, the image processing requirements in the 3D Format section of this document should be followed.

For VC-ID based splitting, set the VCID_SPLIT_EN control in the VCID_SPLIT_CTL register and also program the VC-ID value for each port using the VCID_SEL_P0 and VCID_SEL_P1 field. These settings should be done prior to enabling the Forced Splitter Mode in the FPD3_TX_MODE control register.

Regeneration of HSYNC active width and back porch width can be overridden by the IMG_HSYNC_CTLx registers.

Splitter clock generation is controlled by the SPLIT_CLK_CTLx registers.

8.5 Programming

8.5.1 Serial Control Bus

This serializer may also be configured by the use of a I2C-compatible serial control bus. Multiple devices may share the serial control bus (up to 8 device addresses supported). The device address is set through a resistor divider (R1 and R2 — see 图 35) connected to the IDX pin.

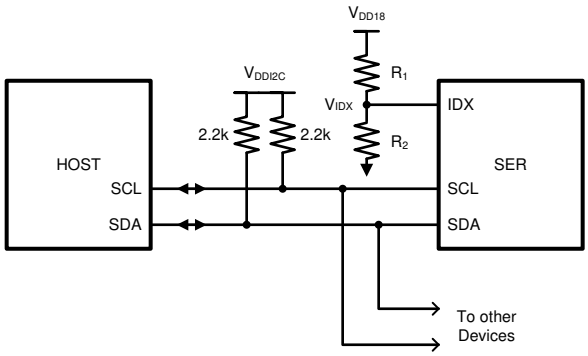


图 35. Serial Control Bus Connection

The serial control bus consists of two signals: SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{DD18} or V_{DD33}. For most applications, a 2.2-kΩ pullup resistor is recommended. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. See *I2C Bus Pullup Resistor Calculation.* The signals are either pulled High or driven Low.

The IDX pin configures the control interface to one of eight possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage on the IDX input pin. See 表 12.

表 12. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD18)}$ = 1.8 V	R_1 (kΩ)	R_2 (kΩ)	7-BIT	8-BIT
0	0	0	0.135 × $V_{(VDD18)}$	0	OPEN	10.0	0x0C	0x18
1	0.176 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.384	73.2	20.0	0x0E	0x1C
2	0.289 × $V_{(VDD18)}$	0.327 × $V_{(VDD18)}$	0.363 × $V_{(VDD18)}$	0.589	60.4	30.1	0x10	0x20
3	0.407 × $V_{(VDD18)}$	0.441 × $V_{(VDD18)}$	0.467 × $V_{(VDD18)}$	0.793	51.1	40.2	0x12	0x24
4	0.526 × $V_{(VDD18)}$	0.555 × $V_{(VDD18)}$	0.584 × $V_{(VDD18)}$	0.999	40.2	51.1	0x14	0x28
5	0.640 × $V_{(VDD18)}$	0.671 × $V_{(VDD18)}$	0.701 × $V_{(VDD18)}$	1.208	30.1	61.9	0x16	0x2C
6	0.757 × $V_{(VDD18)}$	0.787 × $V_{(VDD18)}$	0.814 × $V_{(VDD18)}$	1.417	18.7	71.5	0x18	0x30
7	0.877 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	0x1A	0x34

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See 图 36

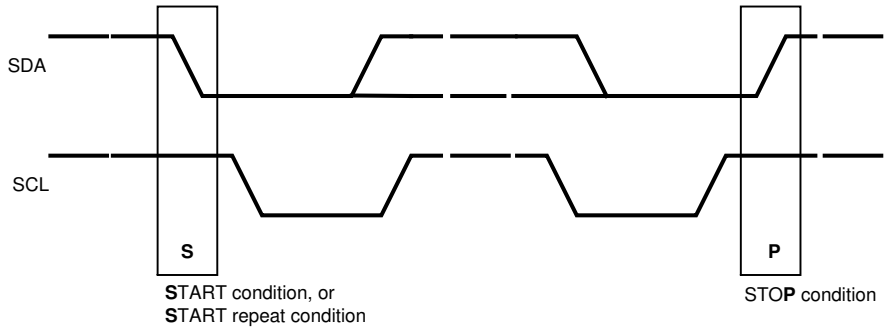


图 36. Start and Stop Conditions

To communicate with an I^2C slave, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match a any slave address of the device, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in 图 37 and a WRITE is shown in 图 38.

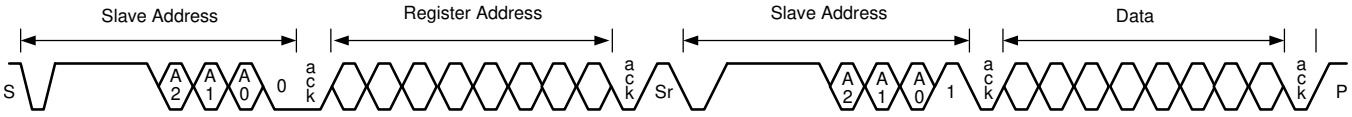


图 37. Serial Control Bus — Read

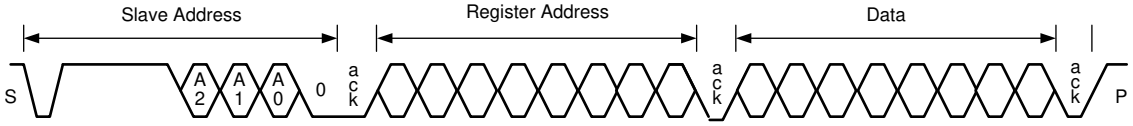


图 38. Serial Control Bus — Write

The I^2C Master located at the serializer must support I^2C clock stretching. For more information on I^2C interface requirements and throughput considerations, refer to the *I2C Communication Over FPD-Link III With Bidirectional Control Channel* application note (SNLA131).

8.5.2 Multi-Master Arbitration Support

The Bidirectional Control Channel in the FPD-Link III devices implements I^2C compatible bus arbitration in the proxy I^2C master implementation. When sending a data bit, each I^2C master senses the value on the SDA line. If the master is sending a logic 1 but senses a logic 0, the master has lost arbitration. It will stop driving SDA, retrying the transaction when the bus becomes idle. Thus, multiple I^2C masters may be implemented in the system.

Ensure that all I^2C masters on the bus support multi-master arbitration.

Assign I^2C addresses with more than a single bit set to 1 for all devices on the I^2C bus. 0x6A, 0x7B, and 0x37 are examples of good choices for an I^2C address. 0x40 and 0x20 are examples of bad choices for an I^2C address.

If the system does require master-slave operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available read/write registers in the deserializer to allow masters to communicate with each other to pass control between the two masters. An example would be to use register 0x18 or 0x19 in the deserializer as a mailbox register to pass control of the channel from one master to another.

8.5.3 I2C Restrictions on Multi-Master Operation

The I^2C specification does not provide for arbitration between masters under certain conditions. The system should make sure the following conditions cannot occur to prevent undefined conditions on the I^2C bus:

- One master generates a repeated Start while another master is sending a data bit.
- One master generates a Stop while another master is sending a data bit.
- One master generates a repeated Start while another master sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I^2C slave.

8.5.4 Multi-Master Access to Device Registers for Newer FPD-Link III Devices

When using the latest generation of FPD-Link III devices such as the DS90UB941AS-Q1, registers may be accessed simultaneously from both local and remote I^2C masters. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I^2C slaves would still be allowed in only one direction at a time.

8.5.5 Multi-Master Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices, simultaneous access to serializer or deserializer registers from both local and remote I^2C masters may cause incorrect operation, thus restrictions should be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in an errored read or write.

Two basic options are recommended. The first is to allow device register access only from one controller. This would allow only the Host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer would not be allowed to access the deserializer or serializer registers.

The second basic option is to allow local register access only, with no access to remote serializer or deserializer registers. The Host controller would be allowed to access the serializer registers while a controller at the deserializer could access those register only. Access to remote I^2C slaves would still be allowed in one direction.

In a very limited case, remote and local access could be allowed to the deserializer registers at the same time. Register access will work correctly if both local and remote masters are accessing the same deserializer register. This allows a simple method of passing control of the Bidirectional Control Channel from one master to another.

8.5.6 Restrictions on Control Channel Direction for Multi-Master Operation

Only one direction should be active at any time across the Bidirectional Control Channel. If both directions are required, some method of transferring control between I^2C masters should be implemented.

8.6 Register Maps

The DS90UB941AS-Q1 implements the following register blocks, accessible through the I2C, as well as the bidirectional control channel:

- Main Registers, summarized in Table 13
- DSI Indirect Registers (separate register block for each of the two DSI ports), summarized in Table 121
- Pattern Generator Indirect Registers (separate register block for each of the two FPD-Link III ports), summarized in Table 159

Register Maps (continued)

8.6.1 Main Registers

Table 13 summarizes the memory-mapped registers for the DS90UB941AS-Q1. These registers are accessible through Serial Control Interface (I2C) as well as the bidirectional control channel. All register offset addresses not listed in Table 13 should be considered as reserved locations and the register contents should not be modified.

Table 13. Main Registers Summary

Address	Acronym	Register Name	Section
0h	I2C_DEVICE_ID		Go
1h	RESET_CTL		Go
2h	DEVICE_CFG		Go
3h	GENERAL_CFG		Go
4h	GENERAL_CFG2		Go
5h	I2C_MASTER_CFG		Go
6h	DES_ID_DES_ID_1		Go
7h	SlaveID_0		Go
8h	SlaveAlias_0		Go
9h	SDA_SETUP		Go
Ah	CRC_ERROR0		Go
Bh	CRC_ERROR1		Go
Ch	GENERAL_STS		Go
Dh	GPIO_0_Config		Go
Eh	GPIO_1_and_GPIO_2_Config		Go
Fh	GPIO_3_Config		Go
10h	GPIO_5_and_GPIO_6_Config		Go
11h	GPIO_7_and_GPIO_8_Config		Go
12h	DATAPATH_CTL		Go
13h	TX_MODE_STS		Go
14h	TX_BIST_CTL		Go
16h	BCC_WDOG_CTL		Go
17h	I2C_CONTROL		Go
18h	SCL_HIGH_TIME		Go
19h	SCL_LOW_TIME		Go
1Ah	DATAPATH_CTL2		Go
1Bh	BIST_BC_ERRORS		Go
1Ch	GPI_PIN_STS1		Go
1Dh	GPI_PIN_STS2		Go
1Eh	TX_PORT_SEL		Go
1Fh	FREQ_COUNTER		Go
20h	DES_CAP1		Go
21h	DES_CAP2		Go
26h	LINK_DET_CTL		Go
2Eh	MAILBOX_2E		Go
2Fh	MAILBOX_2F		Go
30h	REM_INTB_CTRL		Go
32h	IMG_LINE_SIZE0		Go
33h	IMG_LINE_SIZE1		Go
34h	IMG_DELAY0 _IMG_DELAY0_P1		Go
35h	IMG_DELAY1_IMG_DELAY_P1		Go

Table 13. Main Registers Summary (continued)

Address	Acronym	Register Name	Section
36h	CROP_START_X0_CROP_START_X0_P1		Go
37h	CROP_START_X1_CROP_START_X1_P1		Go
38h	CROP_STOP_X0_CROP_STOP_X0_P1		Go
39h	CROP_STOP_X1_CROP_STOP_X1_P1		Go
3Ah	CROP_START_Y0_CROP_START_Y0_P1		Go
3Bh	CROP_START_Y1_CROP_START_Y1_P1		Go
3Ch	CROP_STOP_Y0_CROP_STOP_Y0_P1		Go
3Dh	CROP_STOP_Y1_CROP_STOP_Y1_P1		Go
3Eh	SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1		Go
3Fh	SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1		Go
40h	IND_ACC_CTL		Go
41h	IND_ACC_ADDR		Go
42h	IND_ACC_DATA		Go
4Fh	BRIDGE_CTL		Go
50h	BRIDGE_STS		Go
54h	BRIDGE_CFG		Go
55h	AUDIO_CFG		Go
56h	BRIDGE_CFG2		Go
57h	TDM_CONFIG		Go
58h	VIDEO_3D_STS		Go
59h	DUAL_DSI_CTL_STS		Go
5Ah	DUAL_STS_DUAL_STS_P1		Go
5Bh	DUAL_CTL1		Go
5Ch	DUAL_CTL2		Go
5Dh	FREQ_LOW		Go
5Eh	FREQ_HIGH		Go
5Fh	DSI_FREQ_DSI_FREQ_P1		Go
60h	SPI_TIMING1		Go
61h	SPI_TIMING2		Go
62h	SPI_CONFIG		Go
63h	VCID_SPLIT_CTL		Go
64h	PGCTL_PGCTL_P1		Go
65h	PGCFG_PGCFG_P1		Go
66h	PGIA_PGIA_P1		Go
67h	PGID_PGID_P1		Go
6Ah	IMG_HSYNC_CTL0_IMG_HSYNC_CTL0_P1		Go
6Bh	IMG_HSYNC_CTL1_IMG_HSYNC_CTL1_P1		Go
6Ch	IMG_HSYNC_CTL2_IMG_HSYNC_CTL2_P1		Go

Table 13. Main Registers Summary (continued)

Address	Acronym	Register Name	Section
6Dh	BCC_STATUS		Go
6Eh	BCC_CONFIG		Go
6Fh	FC_BCC_TEST		Go
70h	SlaveID_1		Go
71h	SlaveID_2		Go
72h	SlaveID_3		Go
73h	SlaveID_4		Go
74h	SlaveID_5		Go
75h	SlaveID_6		Go
76h	SlaveID_7		Go
77h	SlaveAlias_1		Go
78h	SlaveAlias_2		Go
79h	SlaveAlias_3		Go
7Ah	SlaveAlias_4		Go
7Bh	SlaveAlias_5		Go
7Ch	SlaveAlias_6		Go
7Dh	SlaveAlias_7		Go
C2h	CFG		Go
C4h	STS		Go
C6h	ICR		Go
C7h	ISR		Go
F0h	TX_ID0		Go
F1h	TX_ID1		Go
F2h	TX_ID2		Go
F3h	TX_ID3		Go
F4h	TX_ID4		Go
F5h	TX_ID5		Go

Table 14 shows the codes that are used for access types in this section.

Table 14. Register Access Type Codes

Access Type	Code	Description
R	R	Read only access
R/S	R/S	Read only access / set based on Strap pin configuration at startup
R/W	R/W	Read / Write access
R/COR	R/COR	Read to Clear / then Read for Status
R/W/RC	R/W/RC	Read / Write access / Read to Clear
R/W/S	R/W/S	Read / Write access / Set based on strap pin configuration at startup

8.6.1.1 I2C_DEVICE_ID Register (Address = 0h) [reset = Strap]

I2C_DEVICE_ID is described in Table 15.

Return to Summary Table.

Table 15. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	DEVICE_ID DEVICE_ID_P1	R/W/S	Strap	7-bit address of Serializer: Defaults to address configured by the IDx strap pin If PORT1_I2C_EN is set, this value defaults to the IDx strap value + 1 for Port1. When programming this value, the least significant bit of the DEVICE_ID value should be set to 0 to allow proper configuration of the second port I2C address.
0	SER_ID	R/W	0h	0: Device ID is from IDX pin (default) 1: Device ID is from 0x00[7:1]

8.6.1.2 RESET_CTL Register (Address = 1h) [reset = Strap]

RESET_CTL is described in Table 16.

Return to Summary Table.

This register is read only

Table 16. RESET_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	DISABLE_DSI	R/W/S	Strap	DSI Reset: Resets the analog DSI and digital DSI. This bit is NOT self-clearing. It is a strap option on the MODE_SEL1 pin. 1: Reset 0: Normal operation
2	DSI_RESET	R/W	0h	DSI Reset: Resets the analog DSI and digital DSI with a short pulse. This bit is self-clearing. 1: Reset 0: Normal operation
1	DIGITAL_RESET1	R/W	0h	Digital Reset: Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET0	R/W	0h	Digital Reset: Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table.

8.6.1.3 DEVICE_CFG Register (Address = 2h) [reset = 0h]

DEVICE_CFG is described in Table 17.

Return to Summary Table.

Table 17. DEVICE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

Table 17. DEVICE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DSI1_CLK_PN_SWAP	R/W	0h	Reverse P/N pin order for DSI Port 1 clock lane: 0: DSI Port 1 Clock Lane P input mapped to P, N input mapped to N 1: DSI Port 1 Clock Lane P input mapped to N, N input mapped to P
5	DSI1_DATA_PN_SWAP	R/W	0h	Reverse P/N pin order for DSI Port 1 data lanes: 0: DSI Port 1 Data Lane P inputs mapped to P, N inputs mapped to N 1: DSI Port 1 Data Lane P inputs mapped to N, N inputs mapped to P
4	DSI1_LANE_REVERSE	R/W	0h	Reverse lane order for DSI Port 1: 0: DSI Port 1 Lanes 3, 2, 1, 0 inputs are mapped to Lanes 3, 2, 1, 0 1: DSI Port 1 Lanes 3, 2, 1, 0 inputs are mapped to Lanes 0, 1, 2, 3
3	RESERVED	R	0h	Reserved
2	DSI0_CLK_PN_SWAP	R/W	0h	Reverse P/N pin order for DSI Port 0 clock lane: 0: DSI Port 0 Clock Lane P input mapped to P, N input mapped to N 1: DSI Port 0 Clock Lane P input mapped to N, N input mapped to P
1	DSI0_DATA_PN_SWAP	R/W	0h	Reverse P/N pin order for DSI Port 0 data lanes: 0: DSI Port 0 Data Lane P inputs mapped to P, N inputs mapped to N 1: DSI Port 0 Data Lane P inputs mapped to N, N inputs mapped to P
0	DSI0_LANE_REVERSE	R/W	0h	Reverse lane order for DSI Port 0: 0: DSI Port 0 Lanes 3, 2, 1, 0 inputs are mapped to Lanes 3, 2, 1, 0 1: DSI Port 0 Lanes 3, 2, 1, 0 inputs are mapped to Lanes 0, 1, 2, 3

8.6.1.4 GENERAL_CFG Register (Address = 3h) [reset = 92h]

GENERAL_CFG is described in Table 18.

Return to Summary Table.

Table 18. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_CRC_CHECKER_ENABLE	R/W	1h	CRC Checker Enable 0: Disable 1: Enable
6	IO_PULLDOWN_DIS	R/W	0h	I/O Pulldown Disable If set, disable internal pull-down resistors on the following digital I/O pins: GPIO0, GPIO1, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, I2S_CLK, I2S_WC, I2S_DA, I2S_DB, I2S_DC, and I2S_DD
5	TX_AUTO_ACK TX_AUTO_ACK_P1	R/W	0h	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. 1: Enable 0: Disable If PORT1_SEL is set, this register controls Port1 operation
4	FILTER_ENABLE	R/W	1h	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected. 1: Filtering enable 0: Filtering disable
3	I2C_PASS_THROUGH I2C_PASS_THROUGH_P1	R/W	0h	I2C Pass-Through Mode 0: Pass-Through Disabled 1: Pass-Through Enabled If PORT1_SEL is set, this register controls Port1 operation
2	RESERVED	R	0h	Reserved

Table 18. GENERAL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PCLK_AUTO	R/W	1h	Switch over to Always On clock in the absence of PCLK 1: Enable auto-switch 0: Disable auto-switch
0	RESERVED	R	0h	Reserved

8.6.1.5 GENERAL_CFG2 Register (Address = 4h) [reset = 0h]

GENERAL_CFG2 is described in Table 19.

Return to Summary Table.

Table 19. GENERAL_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	CRC_ERROR_RESET	R/W	0h	Clear CRC Error Counters. This bit is NOT self-clearing. 1: Clear Counters 0: Normal Operation
4	DE_GATE_RGB	R/W	0h	Gate RGB data with DE signal. RGB data is not gated with DE by default. To enable packetized audio in the DS90UB941AS-Q1, this bit must be set. 1: Gate RGB data with DE in DS90UB941AS-Q1 0: Pass RGB data independent of DE in DS90UB941AS-Q1
3-2	RESERVED	R	0h	Reserved
1	FC_BCC_CRC6_OV FC_BCC_CRC6_OV_P1	R/W	0h	Override Enable for Enhanced Forward Channel CRC and Start Sequence 1: Use FC_BCC_CRC6_OV_VAL value to enable or disable support for Enhanced Forward Channel CRC and Start Sequence 0: Use Deserializer Capabilities list to enable or disable support for Enhanced Forward Channel CRC and Start Sequence If PORT1_SEL is set, this register controls Port1 operation
0	FC_BCC_CRC6_OV_VAL FC_BCC_CRC6_OV_VAL_P1	R/W	0h	Enable Enhanced Forward Channel CRC and Start Sequence When FC_BCC_CRC6_OV is 1, use this value to control support for Enhanced Forward Channel CRC and Start Sequence 1: Enable Enhanced Forward Channel CRC and Start Sequence 0: Disable Enhanced Forward Channel CRC and Start Sequence If PORT1_SEL is set, this register controls Port1 operation

8.6.1.6 I2C_MASTER_CFG Register (Address = 5h) [reset = 0h]

I2C_MASTER_CFG is described in Table 20.

Return to Summary Table.

Table 20. I2C_MASTER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-3	SDA_OUT_DELAY	R/W	0h	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 40 ns. Nominal output delay values for SCL to SDA are: 00: 200 ns 01: 240 ns 10: 280 ns 11: 320 ns Actual delays may be larger dependent on system capacitances and signal rise/fall times.

Table 20. I2C_MASTER_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOCAL_WRITE_DIS	R/W	0h	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer.
1	I2C_BUS_TIMER _SPEEDUP	R/W	0h	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 µs 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER _DISABLE	R/W	0h	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL.

8.6.1.7 DES_ID_DES_ID_1 Register (Address = 6h) [reset = 0h]

DES_ID_DES_ID_1 is described in Table 21.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 21. DES_ID_DES_ID_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	DES_DEV_ID DES_DEV_ID_P1	R/W	0h	7-bit Deserializer Device ID Configures the I2C Slave ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates the Deserializer Device ID for the Deserializer attached to Port 1
0	FREEZE_DEVICE_ID FREEZE_DEVICE_ID_P1	R/W	0h	Freeze Deserializer Device ID Prevent auto-loading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. If PORT1_SEL is set, this bit controls DES_DEV_ID_P1.

8.6.1.8 SlaveID_0 Register (Address = 7h) [reset = 0h]

SlaveID_0 is described in Table 22.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 22. SlaveID_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID0 SLAVE_ID0_P1	R/W	0h	If PORT1_SEL is set, this register controls Port1 SLAVE_ID0. 7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.

Table 22. SlaveID_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R/W	0h	Reserved.

8.6.1.9 SlaveAlias_0 Register (Address = 8h) [reset = 0h]

SlaveAlias_0 is described in Table 23.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 23. SlaveAlias_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID0 SLAVE_ALIAS_ID0_P1	R/W	0h	If PORT1_SEL is set, this register controls Port1 SLAVE_ALIAS_ID0. 7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be re-mapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.10 SDA_SETUP Register (Address = 9h) [reset = 1h]

SDA_SETUP is described in Table 24.

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Table 24. SDA_SETUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	TX_SDA_SETUP	R/W	1h	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640 ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80 ns.

8.6.1.11 CRC_ERROR0 Register (Address = Ah) [reset = 0h]

CRC_ERROR0 is described in Table 25.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 25. CRC_ERROR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CRC_ERROR_7:0 _CRC_ERROR_P1_7:0	R	0h	Back Channel CRC Error counter If PORT1_SEL is set, this register indicates Port1 Status. Number of Back Channel CRC errors – 8 least significant bits. This register is cleared using the CRC ERROR RESET in register 0x04.

8.6.1.12 CRC_ERROR1 Register (Address = Bh) [reset = 0h]

CRC_ERROR1 is described in Table 26.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 26. CRC_ERROR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CRC_ERROR_15:8 _CRC_ERROR_P1_15:8	R	0h	Back Channel CRC Error counter If PORT1_SEL is set, this register indicates Port1 Status Number of Back Channel CRC errors – 8 most significant bits. This register is cleared using the CRC ERROR RESET in register 0x04.

8.6.1.13 GENERAL_STS Register (Address = Ch) [reset = 0h]

GENERAL_STS is described in Table 27.

Some bits in this register are FPD-Link III TX port-specific. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 27. GENERAL_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	General Status Register If PORT1_SEL is set, this register indicates Port1 Status as indicated. Reserved.
6	DSI_ERROR	R	0h	OR of DSI_FPD3_ERR, DSI_CMD_OVER, DSI_EOT_ERR, DSI_READ_WOUT_BTA, and DSI_ERROR_DET from DSI indirect registers. Will not clear on read. In Dual DSI or Independent DSI to FPD-Link III modes, this bit will indicate an error was detected on either DSI input.
5	DPHY_ERROR	R	0h	OR of LANE_SYNC_ERROR and DPHY_LANE_ERROR from DSI indirect registers. Will not clear on read. In Dual DSI or Independent 2:2 modes, this bit will indicate an error was detected on either DPHY input.
4	LINK_LOST LINK_LOST_P1	R	0h	Link Lost Flag for selected port: This bit indicates that loss of link has been detected. This register bit will stay high until cleared using the CRC ERROR RESET in register 0x04. If PORT1_SEL is set, this register indicates Port1 Status as indicated.
3	BIST_CRC_ERROR BIST_CRC_ERROR_P1	R	0h	CRC error during BIST communication with Deserializer. This bit is cleared upon restart of BIST or assertion of CRC ERROR RESET in register 0x04. If PORT1_SEL is set, this register indicates Port1 Status as indicated.
2	PCLK_DETECT PCLK_DETECT_P1	R	0h	Pixel Clock Detect: The frequency detect circuit has detected a valid pixel clock meeting the frequency requirements in the FREQ_LOW register. 1: Valid pixel clock detected 0: Valid pixel clock not detected In Splitter or Independent 2:2 modes, this indicates status for the selected port. If PORT1_SEL is set, this register indicates Port1 Status as indicated.
1	DES_ERROR DES_ERROR_P1	R	0h	Deserializer Error detect for selected port: CRC error during communication with Deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x04.
0	LINK_DETECT LINK_DETECT_P1	R	0h	Link Detect status for selected port: 1: Cable link detected 0: Cable link not detected

8.6.1.14 GPIO_0_Config Register (Address = Dh) [reset = 20h]

GPIO_0_Config is described in Table 28.

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Table 28. GPIO_0_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID	R	2h	GPIO0 and D_GPIO0] Configuration If PORT1_SEL is set, this register controls the D_GPIO0 pin Revision ID 0010: DS90Ux941AS-Q1
3	GPIO0_OUTPUT_VALUE D_GPIO0_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if link is lost.
2-0	GPIO0_MODE D_GPIO0_MODE	R/W	0h	GPIO 0 Mode Determines operating mode for the GPIO pin: x00 : Functional input mode, GPIO0 input x10 : Tri-state 001 : GPIO mode, output 011 : GPIO mode, input 101 : Remote-Hold - output remote data, maintain data on link-loss 111 : Remote-Default - output remote data, Drive default data (OUTPUT VALUE) on link-loss

8.6.1.15 GPIO_1_and_GPIO_2_Config Register (Address = Eh) [reset = 0h]

GPIO_1__and_GPIO_2_Config is described in Table 29.

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Table 29. GPIO_1_and_GPIO_2_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO2_OUTPUT_VALUE D_GPIO2_OUTPUT_VALUE	R/W	0h	GPIO1/GPIO2 and D_GPIO1/D_GPIO2 Configuration If PORT1_SEL is set, this register controls the D_GPIO1 and D_GPIO2 pins Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if link is lost.
6-4	GPIO2_MODE D_GPIO2_MODE	R/W	0h	GPIO 2 Mode Determines operating mode for the GPIO pin: x00 : Functional input mode, I2S_DC input x10 : Tri-state 001 : GPIO mode, output 011 : GPIO mode, input 101 : Remote-Hold - output remote data, maintain data on link-loss 111 : Remote-Default - output remote data, Drive default data (OUTPUT VALUE) on link-loss
3	GPIO1_OUTPUT_VALUE D_GPIO1_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if link is lost.

Table 29. GPIO_1_and_GPIO_2_Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	GPIO1_MODE D_GPIO1_MODE	R/W	0h	GPIO 1 Mode Determines operating mode for the GPIO pin: x00 : Functional input mode, GPIO1 input x10 : Tri-state 001 : GPIO mode, output 011 : GPIO mode, input 101 : Remote-Hold - output remote data, maintain data on link-loss 111 : Remote-Default - output remote data, Drive default data (OUTPUT VALUE) on link-loss

8.6.1.16 GPIO_3_Config Register (Address = Fh) [reset = 0h]

GPIO_3_Config is described in Table 30.

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Table 30. GPIO_3_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	GPIO3 and D_GPIO3 Configuration If PORT1_SEL is set, this register controls the D_GPIO3 pin Reserved
3	GPIO3_OUTPUT_VALUE D_GPIO3_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if link is lost.
2-0	GPIO3_MODE D_GPIO3_MODE	R/W	0h	GPIO 3 Mode Determines operating mode for the GPIO pin: x00 : Functional input mode, I2S_DD input x10 : Tri-state 001 : GPIO mode, output 011 : GPIO mode, input 101 : Remote-Hold - output remote data, maintain data on link-loss 111 : Remote-Default - output remote data, Drive default data (OUTPUT VALUE) on link-loss

8.6.1.17 GPIO_5_and_GPIO_6_Config Register (Address = 10h) [reset = 0h]

GPIO_5_and_GPIO_6_Config is and described in Table 31.

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Table 31. GPIO_5_and_GPIO_6_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO6_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is Output.
6	RESERVED	R	0h	Reserved
5-4	GPIO6_DIR	R/W	0h	The GPIO 6 MODE configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode input 10: Tri-state 01: GPIO mode output 11: GPIO mode input
3	GPIO5_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is Output.
2	RESERVED	R	0h	Reserved

Table 31. GPIO_5_and_GPIO_6_Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	GPIO5_MODE	R/W	0h	The GPIO 5 MODE configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode input 10: Tri-state 01: GPIO mode output 11: GPIO mode input

8.6.1.18 GPIO_7_and_GPIO_8_Config Register (Address = 11h) [reset = 0h]

GPIO_7_and_GPIO_8_Config is described in Table 32.

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Table 32. GPIO_7_and_GPIO_8_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is Output.
6	RESERVED	R	0h	Reserved
5-4	GPIO8_MODE	R/W	0h	The GPIO 8 MODE configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode input 10: Tri-state 01: GPIO mode output 11: GPIO mode input
3	GPIO7_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is Output.
2	RESERVED	R	0h	Reserved
1-0	GPIO7_MODE	R/W	0h	The GPIO 7 MODE configures the pad in input direction or output direction for functional mode or GPIO mode. {GPIO DIR, GPIO EN} 00: Functional mode input 10: Tri-state 01: GPIO mode output 11: GPIO mode input

8.6.1.19 DATAPATH_CTL Register (Address = 12h) [reset = 0h]

DATAPATH_CTL is described in Table 33.

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Table 33. DATAPATH_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	DE_POLARITY	R/W	0h	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low)
4	I2S_RPTR_REGEN	R/W	0h	1: Repeater regenerate I2S from I2S pins 0: Repeater pass-through I2S from video pins
3	I2S_B_OVERRIDE	R/W	0h	I2S Channel B Override 1: Set I2S Channel B Enable from reg_12[0] 0: I2S Channel B Disabled

Table 33. DATAPATH_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	VIDEO_18B_EN	R/W	0h	18-bit Video Select 1: Select 18-bit video mode 0: Select 24-bit video mode
1	I2S_TRANSPORT_SEL	R/W	0h	1: Enable I2S Data Forward Channel Frame Transport 0: Enable I2S Data Island Transport
0	I2S_B_EN	R/W	0h	I2S Channel B Enable 1: Enable I2S Channel B on B1 input 0: I2S Channel B disabled Note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

8.6.1.20 TX_MODE_STS Register (Address = 13h) [reset = Strap]

TX_MODE_STS is described in Table 34.

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Table 34. TX_MODE_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MODE_SEL1_DONE	R	1h	Indicates MODE_SEL1 value has stabilized and been latched
6-4	MODE_SEL1_DECODE	R/S	Strap	Returns the 3-bit decode of the MODE_SEL1 pin
3	MODE_SEL0_DONE	R	1h	Indicates MODE_SEL0 value has stabilized and been latched
2-0	MODE_SEL0_DECODE	R/S	Strap	Returns the 3-bit decode of the MODE_SEL0 pin

8.6.1.21 TX_BIST_CTL Register (Address = 14h) [reset = 0h]

TX_BIST_CTL is described in Table 35.

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Table 35. TX_BIST_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	DOPL_MODE	R/W	0h	DOPL Mode Enable 1: Enabled 0: Disabled This bit cannot be written remotely through the Bidirectional Control Channel
3	RESERVED	R	0h	Reserved
2-1	CLOCK_SOURCE CLOCK_SOURCE_P1	R/W	0h	Clock Source in BIST mode (When 0x14[0]=1) 00: External Pixel Clock 01: 33-MHz Oscillator 1x: 100-MHz Oscillator In Splitter or Independent 2:2 mode, this field controls the selected port.
0	BIST_EN BIST_EN_P1	R/W	0h	BIST Control 1: Enabled 0: Disabled In Splitter or Independent 2:2 mode, this field controls the selected port.

8.6.1.22 BCC_WDOG_CTL Register (Address = 16h) [reset = FEh]

BCC_WDOG_CTL is described in Table 36.

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Table 36. BCC_WDOG_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BCC_WATCHDOG _TIMER	R/W	7Fh	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 ms. This field should not be set to 0. It is recommended to set this field to 0x01.
0	BCC_WDOG_DIS	R/W	0h	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

8.6.1.23 I2C_CONTROL Register (Address = 17h) [reset = 1Eh]

I2C_CONTROL is described in Table 37.

Some bits in this register are FPD-Link III TX port-specific. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 37. I2C_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_PASS_ALL I2C_PASS_ALL_P1	R/W	0h	1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID. 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID. If PORT1_SEL is set, this bit controls I2C PASS ALL P1
6-4	SDA_HOLD_TIME	R/W	1h	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 ns.
3-0	I2C_FILTER_DEPTH	R/W	Eh	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 ns.

8.6.1.24 SCL_HIGH_TIME Register (Address = 18h) [reset = 7Fh]

SCL_HIGH_TIME is described in Table 38.

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Table 38. SCL_HIGH_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_SCL_HIGH	R/W	7Fh	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5-µs SCL high time with the internal oscillator clock running at 26.25 MHz rather than the nominal 25 MHz. Delay includes 5 additional oscillator clock periods. Min_delay = 38.0952 ns × (TX_SCL_HIGH + 5)

8.6.1.25 SCL_LOW_TIME Register (Address = 19h) [reset = 7Fh]

SCL_LOW_TIME is described in Table 39.

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Table 39. SCL_LOW_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_SCL_LOW	R/W	7Fh	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5-µs SCL low time with the internal oscillator clock running at 26.25 MHz rather than the nominal 25 MHz. Delay includes 5 additional clock periods. Min_delay = 38.0952 ns × (TX_SCL_LOW + 5)

8.6.1.26 DATAPATH_CTL2 Register (Address = 1Ah) [reset = 1h]

DATAPATH_CTL2 is described in Table 40.

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Table 40. DATAPATH_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BLOCK_REPEATER_I2S_MODE	R/W	0h	Block automatic I2S mode configuration in repeater 0: I2S mode (2-channel, 4-channel, or surround) is detected from the in-band audio signaling in a repeater. 1: Disable automatic detection of I2S mode
6-4	RESERVED	R	0h	Reserved
3	SECONDARY_AUDIO	R	0h	Enable Secondary Audio This register indicates that the AUX audio channel is enabled. The control for this function is through the AUX_AUDIO_EN bit in the BRIDGE_CFG register, register offset 0x54).
2-1	RESERVED	R	0h	Reserved
0	I2S_SURROUND	R/W	1h	Enable 5.1- or 7.1-channel I2S audio transport 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0 1: 5.1- or 7.1-channel audio is enabled Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

8.6.1.27 BIST_BC_ERRORS Register (Address = 1Bh) [reset = 0h]

BIST_BC_ERRORS is described in Table 41.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 41. BIST_BC_ERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BIST_BC_ERROR_COUNT BIST_BC_ERROR_COUNT_P1	R	0h	BIST Back Channel CRC Error Counter This register is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04. If PORT1_SEL is set, this register indicates port 1 status

8.6.1.28 GPIO_PIN_STS1 Register (Address = 1Ch) [reset = 0h]

GPIO_PIN_STS1 is described in Table 42.

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Table 42. GPIO_PIN_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO7_PIN_STS	R	0h	GPIO7/I2S_WC pin status If PORT1_SEL is set, this register reads 0
6	GPIO6_PIN_STS	R	0h	GPIO6/I2S_DA pin status If PORT1_SEL is set, this register reads 0
5	GPIO5_PIN_STS	R	0h	GPIO5/I2S_DB pin status If PORT1_SEL is set, this register reads 0
4	RESERVED	R	0h	Reserved
3	GPIO3_PIN_STS D_GPIO3_PIN_STS	R	0h	GPIO3 / I2S_DD pin status If PORT1_SEL is set, this register indicates D_GPIO3 pin status
2	GPIO2_PIN_STS D_GPIO2_PIN_STS	R	0h	GPIO2 / I2S_DC pin status If PORT1_SEL is set, this register indicates D_GPIO2 pin status
1	GPIO1_PIN_STS D_GPIO1_PIN_STS	R	0h	GPIO1 pin status If PORT1_SEL is set, this register indicates D_GPIO1 pin status
0	GPIO0_PIN_STS D_GPIO0_PIN_STS	R	0h	GPIO0 pin status If PORT1_SEL is set, this register indicates D_GPIO0 pin status

8.6.1.29 GPIO_PIN_STS2 Register (Address = 1Dh) [reset = 0h]

GPIO_PIN_STS2 is described in Table 43.

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Table 43. GPIO_PIN_STS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	GPIO8_PIN_STS	R	0h	GPIO8/I2S_CLK pin status

8.6.1.30 TX_PORT_SEL Register (Address = 1Eh) [reset = 1h]

TX_PORT_SEL is described in Table 44.

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Table 44. TX_PORT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	PORT1_I2C_EN	R/W	0h	Port1 I2C Enable: Enables secondary I2C address. The second I2C address provides access to port1 registers as well as registers that are shared between ports 0 and 1. The second I2C address value will be set to DeviceID + 1 (7-bit format). The PORT1_I2C_EN bit must also be set to allow accessing remote devices over the second link when the device is in Replicate mode.
1	PORT1_SEL	R/W	0h	Selects Port 1 for Register Access from primary I2C Address For writes, port1 registers and shared registers will both be written. For reads, port1 registers and shared registers will be read. This bit must be cleared to read port0 registers. This bit is ignored if PORT1_I2C_EN is set.

Table 44. TX_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PORT0_SEL	R/W	1h	Selects Port 0 for Register Access from primary I2C Address For writes, port0 registers and shared registers will both be written. For reads, port0 registers and shared registers will be read. Note that if PORT1_SEL is also set, then port1 registers will be read. This bit is ignored if PORT1_I2C_EN is set.

8.6.1.31 FREQ_COUNTER Register (Address = 1Fh) [reset = 0h]

FREQ_COUNTER is described in Table 45.

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Table 45. FREQ_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FREQ_COUNT	R/W	0h	Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 40 ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.

8.6.1.32 DES_CAP1 Register (Address = 20h) [reset = 0h]

DES_CAP1 is described in Table 46.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 46. DES_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FREEZE_DES_CAP FREEZE_DES_CAP_P1	R/W	0h	If PORT1_SEL is set, this register indicates Port1 Capabilities Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x20 and 0x21.
6	HSCC_MODE_0 _HSCC_MODE_P1_0	R/W	0h	High-Speed Control Channel bit 0 Lowest bit of the 3-bit HSCC indication. The other 2 bits are contained in Deserializer Capabilities 2. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	DUAL_LINK_CAP DUAL_LINK_CAP_P1	R/W	0h	Dual link Capabilities Indicates if the Deserializer is capable of dual link operation. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

Table 46. DES_CAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DUAL_CHANNEL DUAL_CHANNEL_P1	R/W	0h	Dual Channel 0/1 Indication In a dual-link capable device, indicates if this is the primary or secondary channel. 0: Primary channel (channel 0) 1: Secondary channel (channel 1) This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
1	VID_24B_HD_AUD VID_24B_HD_AUD_P1	R/W	0h	Deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
0	DES_CAP_FC_GPIO DES_CAP_FC_GPIO_P1	R/W	0h	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

8.6.1.33 DES_CAP2 Register (Address = 21h) [reset = 0h]

DES_CAP2 is described in Table 47.

FPD-Link III TX port-specific register. The FPD-Link III Port Select register 0x1E configures which unique TX port registers can be accessed by I2C read and write commands.

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Table 47. DES_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	FC_BCC_CRC6	R/W	0h	Enable enhanced CRC and start sequence
2	RESERVED	R	0h	Reserved
1-0	HSCC_MODE_2:1 HSCC_MODE_P1_2:1	R/W	0h	High-Speed Control Channel bit 0 Upper bits of the 3-bit HSCC indication. The lowest bit is contained in Deserializer Capabilities 1. 000: Normal back channel frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode In Single Link devices, only Normal back channel frame modes are supported.

8.6.1.34 LINK_DET_CTL Register (Address = 26h) [reset = 0h]

LINK_DET_CTL is described in Table 48.

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Table 48. LINK_DET_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved

Table 48. LINK_DET_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LINK_DETECT_TIMER	R/W	0h	Bidirectional Control Channel Link Detect Timer This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 000: 162 ms 001: 325 ms 010: 650 ms 011: 1.3 ms 100: 10.25 µs 101: 20.5 µs 110: 41 µs 111: 82 µs

8.6.1.35 MAILBOX_2E Register (Address = 2Eh) [reset = A5h]

MAILBOX_2E is described in Table 49.

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Table 49. MAILBOX_2E Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAILBOX_2E	R/W	A5h	Mailbox Register This register is an unused read/write register that can be used for any purpose.

8.6.1.36 MAILBOX_2F Register (Address = 2Fh) [reset = 5Ah]

MAILBOX_2F is described in Table 50.

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Table 50. MAILBOX_2F Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAILBOX_2F	R/W	5Ah	Mailbox Register This register is an unused read/write register that can be used for any purpose.

8.6.1.37 REM_INTB_CTRL Register (Address = 30h) [reset = 0h]

REM_INTB_CTRL is described in Table 51.

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Table 51. REM_INTB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved

Table 51. REM_INTB_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	REM_INTB_MODE	R/W	0h	Allows choosing different pins to output the remote interrupt. If multiple links are available (not in Dual FPD-Link III operation), the REM_INTB is typically a combined interrupt from both ports. See selection 0001 below for the exception that allows independent remote interrupts from both ports. Determines the pin that the Remote Interrupt will output on: 0000: NOT ENABLED 0001: REM_INTB indicates port 0 remote interrupt, INTB indicates port 1 remote interrupt 001x,01xx Reserved 1000:GPIO0 1001:GPIO1 1010:GPIO2 1011:GPIO3 1100:D_GPIO0 1101:D_GPIO1 1110:D_GPIO2 1111:D_GPIO3

8.6.1.38 IMG_LINE_SIZE0 Register (Address = 32h) [reset = 0h]

IMG_LINE_SIZE0 is described in Table 52.

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Table 52. IMG_LINE_SIZE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMG_LINE_SIZE_7:0	R/W	0h	Dual Image Line Size Register 0 Dual Image line size (bits 7:0) For processing Left/Right or Alternate Pixel 3D pixel format images for splitting, this parameter provides the line size for the equivalent 2D image in pixels. For the default setting, a 2D image with 1280 pixels per line would have a combined Left/Right format image of 2560 pixels. The default is set to 1280 pixels (0x500). This parameter is also used as the 2D image line size in pixels for the Dual-DSI Left/Right mode. The Dual Image Line Size should be programmed to a maximum value of 4096 pixels.

8.6.1.39 IMG_LINE_SIZE1 Register (Address = 33h) [reset = 5h]

IMG_LINE_SIZE1 is described in Table 53.

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Table 53. IMG_LINE_SIZE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	IMG_LINE_SIZE_12:8	R/W	5h	Dual Image line size (bits 12:8) For processing Left/Right or Alternate Pixel 3D pixel format images for splitting, this parameter provides the line size for the equivalent 2D image in pixels. For the default setting, a 2D image with 1280 pixels per line would have a combined Left/Right format image of 2560 pixels. The default is set to 1280 pixels (0x500). This parameter is also used as the 2D image line size in pixels for the Dual-DSI Left/Right mode. The Dual Image Line Size should be programmed to a maximum value of 4096 pixels.

8.6.1.40 IMG_DELAY0_IMG_DELAY0_P1 Register (Address = 34h) [reset = Ch]

IMG_DELAY0_IMG_DELAY0_P1 is described in Table 54.

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Table 54. IMG_DELAY0_IMG_DELAY0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMG_DELAY_7:0 IMG_DELAY_P1_7:0	R/W	Ch	Dual Image Delay Register 0 In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Dual Image Delay (bits 7:0) For processing Left/Right or Alternate Pixel 3D format images for splitting, this parameter provides a delay for buffering data prior to generation of 2D image data in alternating pixel format or for splitting images. For Left/Right 3D images, this parameter is typically set to a value of 12 pixels (0x00C). For splitting Alternate Pixel 3D format images, this parameter will typically be set to a value of 12 pixels (0x00C) if the IMG_HSYNC_CTL registers are used to set HSYNC timing. If the IMG_HSYNC_CTL registers are not used to set HSYNC timing, this value should be set to the Horizontal Sync period plus the Horizontal Back Porch period in pixels. Depending on cropping options, this value may need to be modified to ensure proper operation. The Dual Image Delay should be programmed to a maximum value of 4096 pixels.

8.6.1.41 IMG_DELAY1_IMG_DELAY_P1 Register (Address = 35h) [reset = 0h]

IMG_DELAY1_IMG_DELAY_P1 is described in Table 55.

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Table 55. IMG_DELAY1_IMG_DELAY_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	IMG_DELAY_12:8 IMG_DELAY_P1_12:8	R/W	0h	Dual Image Delay (bits 12:8) For processing Left/Right or Alternate Pixel 3D format images for splitting, this parameter provides a delay for buffering data prior to generation of Left/Right data in alternating pixel format or for splitting images. For Left/Right 3D images, this parameter is typically set to a value of 12 pixels (0x00C). For splitting Alternate Pixel 3D format images, this parameter will typically be set to a value of 12 pixels (0x00C) if the IMG_HSYNC_CTL registers are used to set HSYNC timing. If the IMG_HSYNC_CTL registers are not used to set HSYNC timing, this value should be set to the Horizontal Sync period plus the Horizontal Back Porch period in pixels. Depending on cropping options, this value may need to be modified to ensure proper operation. The Dual Image Delay should be programmed to a maximum value of 4096 pixels.

8.6.1.42 CROP_START_X0_CROP_START_X0_P1 Register (Address = 36h) [reset = 0h]

CROP_START_X0_CROP_START_X0_P1 is described in Table 56.

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Table 56. CROP_START_X0_CROP_START_X0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_START_X_7:0 CROP_START_X_P1_7:0	R/W	0h	Crop Start X0 Register In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be de-asserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

8.6.1.43 CROP_START_X1_CROP_START_X1_P1 Register (Address = 37h) [reset = 0h]

CROP_START_X1_CROP_START_X1_P1 is described in Table 57.

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Table 57. CROP_START_X1_CROP_START_X1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CROP_ENABLE CROP_ENABLE_P1	R/W	0h	Crop Start X1 Register In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Enable Video Cropping: Setting this bit to a 1 will enabling cropping of video for the selected port. Cropping is controlled by setting the X,Y start and stop positions using the CROP_START_X/Y and CROP_STOP_X/Y registers.
6-5	RESERVED	R	0h	Reserved
4-0	CROP_START_X_12:8 CROP_START_X_P1_12:8	R/W	0h	Image Cropping Start X position (bits 12:8) In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be de-asserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

8.6.1.44 CROP_STOP_X0_CROP_STOP_X0_P1 Register (Address = 38h) [reset = 0h]

CROP_STOP_X0_CROP_STOP_X0_P1 is described in Table 58.

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Table 58. CROP_STOP_X0_CROP_STOP_X0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_STOP_X_7:0 CROP_STOP_X_P1_7:0	R/W	0h	Image Cropping Stop X position (bits 7:0) In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be de-asserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

8.6.1.45 CROP_STOP_X1_CROP_STOP_X1_P1 Register (Address = 39h) [reset = 0h]

CROP_STOP_X1_CROP_STOP_X1_P1 is described in Table 59.

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Table 59. CROP_STOP_X1_CROP_STOP_X1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	CROP_STOP_X_12:8 CROP_STOP_X_P1_12:8	R/W	0h	Image Cropping Stop X position (bits 12:8) In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be de-asserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

8.6.1.46 CROP_START_Y0_CROP_START_Y0_P1 Register (Address = 3Ah) [reset = 0h]

CROP_START_Y0_CROP_START_Y0_P1 is described in Table 60.

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Table 60. CROP_START_Y0_CROP_START_Y0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_START_Y_7:0 CROP_START_Y_P1_7:0	R/W	0h	Crop Start Y0 Register In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be de-asserted). Line positions range from 0 to N-1 where N is the number of lines in the frame. In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port.

8.6.1.47 CROP_START_Y1_CROP_START_Y1_P1 Register (Address = 3Bh) [reset = 0h]

CROP_START_Y1_CROP_START_Y1_P1 is described in Table 61.

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Table 61. CROP_START_Y1_CROP_START_Y1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	CROP_START_Y_12:8 CROP_START_Y_P1_12:8	R/W	0h	Image Cropping Start Y position (bits 12:8) In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be de-asserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

8.6.1.48 CROP_STOP_Y0_CROP_STOP_Y0_P1 Register (Address = 3Ch) [reset = 0h]

CROP_STOP_Y0_CROP_STOP_Y0_P1 is described in Table 62.

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Table 62. CROP_STOP_Y0_CROP_STOP_Y0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_STOP_Y_7:0 CROP_STOP_Y_P1_7:0	R/W	0h	Crop Stop Y0 Register In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be de-asserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

8.6.1.49 CROP_STOP_Y1_CROP_STOP_Y1_P1 Register (Address = 3Dh) [reset = 0h]

CROP_STOP_Y1_CROP_STOP_Y1_P1 is described in Table 63.

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Table 63. CROP_STOP_Y1_CROP_STOP_Y1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	CROP_STOP_Y_12:8 CROP_STOP_Y_P1_12:8	R/W	0h	Image Cropping Stop Y position (bits 12:8) In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be de-asserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

8.6.1.50 SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 Register (Address = 3Eh) [reset = 81h]

SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 is described in Table 64.

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Table 64. SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPLIT_CLK_DIV_EN SPLIT_CLK_DIV_EN_P1	R/W	1h	Splitter Mode Clock Control Register 0 This controls the selected FPD-Link III port. Splitter mode clock divider enable This register enables the splitter mode clock divider. In splitter mode, if this register is set to 0, the pixel clock for splitter operation is disabled. The divider should be disabled prior to changing the Splitter Divider settings, SPLIT_CLK_SEL, SPLIT_CLK_DIV_M, and SPLIT_CLK_DIV_N. In addition, changes to divider settings should only be done when the DSI input is disabled to ensure proper mode transition. These values are ignored if Splitter mode is disabled. This controls the selected FPD-Link III port.
6-5	SPLIT_CLK_SEL	R/W	0h	Splitter mode clock select This register selects the clock source for the FPD-Link III transmit side of the splitter operation for the selected port. 00 : Input pixel clock divided by 2 (default) 01 : M/N divider from the DPHY input clock 10 : M/N divider from the external clock on the REFCLK0 pin 11 : M/N divider from the external clock on the REFCLK1 pin

Table 64. SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	SPLIT_CLK_DIV_M SPLIT_CLK_DIV_M_P1	R/W	1h	Splitter mode clock divider M value This register controls the M setting for the M/N divider used to generate the splitter mode pixel clock from the selected input clock. The default settings for M/N provide a 1/2 clock frequency normally required for splitting symmetric video. These values are ignored if Splitter mode is disabled. This controls the selected FPD-Link III port.

8.6.1.51 SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1 Register (Address = 3Fh) [reset = 2h]

SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1 is described in Table 65.

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Table 65. SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPLIT_CLK_DIV_N SPLIT_CLK_DIV_N_P1	R/W	2h	Splitter Mode Clock Control Register 1 This controls the selected FPD-Link III port. Splitter mode clock divider N value This register controls the N setting for the M/N divider used to generate the splitter mode pixel clock from the selected input clock. The default settings for M/N provide a 1/2 clock frequency normally required for splitting symmetric video. These values are ignored if Splitter mode is disabled. This controls the selected FPD-Link III port.

8.6.1.52 IND_ACC_CTL Register (Address = 40h) [reset = 0h]

IND_ACC_CTL is described in Table 66.

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Table 66. IND_ACC_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-2	IND_ACC_SEL	R/W	0h	Indirect Access Register Select: Selects target page for register access 000 : Disabled 001 : DSI/D-PHY Port 0 Digital Registers 010 : DSI/D-PHY Port 1 Digital Registers 011 : Reserved 100 : Reserved 101 : Reserved 110 : Reserved 111 :Reserved
1	IND_ACC_AUTO_INC	R/W	0h	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1. For auto-increment on reads, the IND_ACC_READ bit should also be set.

Table 66. IND_ACC_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IND_ACC_READ	R/W	0h	Indirect Access Register Read: Typically, this bit should be set to 1 when reading indirect access registers. It should be set to 0 when writing to indirect access registers. For access to page 1 registers (DSI/D-PHY digital registers), setting this bit allows Clear-on-read of status registers. If this bit is set to 0, the status registers may be read, but will not be cleared on read. For access to analog registers that require prefetch, setting this allows generation of a read strobe to the analog block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register.

8.6.1.53 IND_ACC_ADDR Register (Address = 41h) [reset = 0h]

IND_ACC_ADDR is described in Table 67.

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Table 67. IND_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IND_ACC_ADDR	R/W	0h	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

8.6.1.54 IND_ACC_DATA Register (Address = 42h) [reset = 0h]

IND_ACC_DATA is described in Table 68.

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Table 68. IND_ACC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IND_ACC_DATA	R/W	0h	Indirect Access Register Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register

8.6.1.55 BRIDGE_CTL Register (Address = 4Fh) [reset = Strap]

BRIDGE_CTL is described in Table 69.

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Table 69. BRIDGE_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DSI_CONTINUOUS_CLK DSI_CONTINUOUS_CLK_P1	R/W	Strap	DSI Continuous Clock Mode This bit controls handling of the DSI Clock lane. If in continuous clock mode, the DSI logic will assume the clock input is always in HS Mode and will bypass initialization requirements for the clock lane. In Independent 2:2 mode, this controls the selected FPD-Link III port. DSI_CONTINUOUS_CLK is initially loaded from the MODE_SEL1 strap options.
6	DUAL_DSI_EN	R/W	0h	Dual DSI input mode: Determines operating mode of dual DSI Receive interface 1: Dual-DSI mode 0: Single-DSI mode This bit should be set to 0 for Independent 2:2 mode

Table 69. BRIDGE_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DSI_PORT_SEL	R/W	0h	DSI Receive input select In Single DSI mode, this control selects the active input DSI Port. 0 : Select DSI Input port 0 1 : Select DSI Input port 1 In Independent 2:2 mode, setting this bit to 1 will swap the DSI ports such that DSI port 0 will map to FPD-Link III port 1 and DSI port 1 will map to FPD-Link III port 0. If DUAL_DSI_EN is set to 1, DSI_PORT_SEL should be set to 0.
4	ALT_LINES_3D	R/W	0h	Enable Alternate Lines 3D mode If set to a 1, the video input is handled as two images based on an alternating line format. The device will merge the images into a single image with an alternating pixel format that can then be split into two images either at the FPD-Link III transmit outputs or at a downstream device. To split the images at the FPD-Link III transmit ports, it is necessary to set the FPD3_TX_MODE in the DUAL_CTL1 register to the Forced Splitter Mode.
3-2	DSI_LANES DSI_LANES_P1	R/W/S	Strap	DSI Lane Selection Indicates number of DSI Lanes that are active. 00 : 1 Lane (DSI Lane 0) 01 : 2 Lanes 10 : 3 Lanes 11 : 4 Lanes DSI_LANES is initially loaded from the MODE_SEL0 pin strap options. To avoid video errors, the DSI_LANES field should only be changed when the DSI input is inactive. In Independent 2:2 mode, this controls the selected FPD-Link III port.
1	CFG_INIT	R/W	0h	Initialize Configuration from Non-Volatile Memory: Causes a reload of the configuration data from the non-volatile memory. In addition, strap options will be restored to their initial strapped value. This bit will be cleared when the initialization is complete.
0	RESERVED	R	0h	Reserved

8.6.1.56 BRIDGE_STS Register (Address = 50h) [reset = 2h]

BRIDGE_STS is described in Table 70.

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Table 70. BRIDGE_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	INIT_DONE	R	0h	Initialization Done: Initialization sequence has completed. This step will complete after configuration complete (CFG_DONE)
3	RESERVED	R	0h	Reserved
2	CFG_DONE	R	0h	Configuration Complete: Indicates automatic configuration has completed. This step will complete prior to initialization complete (INIT_DONE).
1	CFG_CKSUM	R	1h	Configuration checksum status: Indicates result of Configuration checksum during initialization. The device verifies the 2 's complement checksum in the last 128 bytes of the NVM. A value of 1 indicates the checksum passed.
0	RESERVED	R	0h	Reserved

8.6.1.57 BRIDGE_CFG Register (Address = 54h) [reset = 2h]

BRIDGE_CFG is described in Table 71.

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Table 71. BRIDGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	DSI_BYTES_PER_PIXEL DSI_BYTES_PER_PIXEL_P1	R/W	0h	Number of DSI Bytes Per Pixel: For Continuous Clock Mode, selects the number of DSI bytes per pixel for the desired DSI Data Type 00: 3 bytes/pixel (RGB888, RGB666 loosely packed, 20b YCbCr 4:2:2, 24b YCbCr 4:2:2, 12b YCbCr 4:2:0, Compressed) 01: 2.25 bytes/pixel (RGB666 packed) 10: 2 bytes/pixel (RGB565, 16b YCbCr 4:2:2) 11: Reserved Notes: All RGB formats are converted to RGB888. YCbCr and Compressed formats are passed through unconverted. In Independent 2:2 mode, this controls the selected port.
3	RESERVED	R	0h	Reserved
2	AUDIO_TDM	R/W	0h	Enable TDM Audio: Setting this bit to a 1 will enable TDM audio for the I2S audio. Parallel I2S data on the I2S pins will be serialized onto a single I2S_DA signal for sending over the serial link.
1	AUDIO_MODE	R/W	1h	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0: Disabled 1: I2S audio from I2S pins
0	AUX_AUDIO_EN	R/W	0h	AUX Audio Channel Enable: Setting this bit to a 1 will enable the AUX audio channel. This allows sending additional 2-channel audio in addition to the I2S audio.

8.6.1.58 AUDIO_CFG Register (Address = 55h) [reset = Strap]

AUDIO_CFG is described in Table 72.

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Table 72. AUDIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TDM_2_PARALLEL	R/W	0h	Enable TDM to parallel I2S audio conversion: When this bit is set, the TDM to parallel I2S conversion is enabled. TDM audio data on the I2S_DA pin will be split onto four I2S data signals.
6	RESERVED	R	0h	Reserved
5	SWC_EDGE	R/W	0h	Secondary WC edge sampling: Setting this bit to a 1 will change the sampling edge for the secondary WC from the posedge of the I2S_CLK to the negedge. 1: Sample word clock on the negedge of the I2S CLK 0: Sample word clock on the posedge of the I2S CLK
4	SPLIT_AUDIO	R/W/S	Strap	Split Audio across ports When the FPD-Link III Transmit is in Replicate or Splitter mode, setting this bit will split the I2S audio across the two ports. This bit will have no effect in Single or Dual FPD-Link III Transmit modes 0 : Audio signals will be mapped to both ports (up to 8 channel audio) 1 : Split audio: Port 0 gets I2S_DA/I2S_DB, Port 1 gets I2S_DC/I2S_DD signals The SPLIT_AUDIO control is strapped from the MODE_SEL0 pin at power-up. If Splitter Mode is strapped, SPLIT_AUDIO will be set to 1.

Table 72. AUDIO_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	RESERVED	R	0h	Reserved

8.6.1.59 BRIDGE_CFG2 Register (Address = 56h) [reset = Strap]

BRIDGE_CFG2 is described in Table 73.

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Table 73. BRIDGE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LEFT_RIGHT_3D	R/W	0h	Enable Left/Right 3D processing: Setting this bit to a 1 enables conversion of a Left/Right (side-by-side) 3D image into an alternating pixel image. This conversion allows splitting of the 3D image at the serializer FPD-Link III output or at a downstream deserializer. In addition to setting this bit, software should also set the IMG_LINE_SIZE and IMG_DELAY parameters.
6	DUAL_DSI_LR_EN	R/W	0h	Dual-DSI Left/Right format enable: Setting this bit to a 1 enables the serializer to arrange the Dual-DSI input into a single frame with Left/Right (side-by-side) format. The left image is received from DSI port 0 while the right image is received on DSI port 1. This mode also requires setting the DUAL_DSI_EN control in the BRIDGE_CTL register.
5-2	RESERVED	R	0h	Reserved
1-0	BRIDGE_CLK_MODE BRIDGE_CLK_MODE_P1	R/W/S	Strap	Bridge Clocking Mode 00: DSI Reference Clock Mode. The FPD-Link III transmitter will be synchronous to the DSI clock. In this mode, the DSI clock must be continuous and BRIDGE_CTL:DSI_CONTINUOUS_CLK must be set. 01: External Reference Clock Mode. The FPD-Link III transmitter is sourced from an external pixel clock present on the REFCLK pin. The DSI clock may be continuous or discontinuous. 10: Internal Reference Clock Mode. The FPD-Link III transmitter is sourced from an internal pixel clock generated from the always-on clock. The DSI clock may be continuous or discontinuous. 11: External Reference Clock Mode for Independent 2:2 Mode. The FPD-Link III Port0 transmitter is sourced from an external pixel clock present on the REFCLK0 pin while the Port1 transmitter is sourced from an external pixel clock present on the REFCLK1 pin. The DSI clock may be continuous or non-continuous. This option is only available when in Independent 2:2 mode. In Independent 2:2 mode, this controls the selected FPD-Link III port. If device is strapped for continuous clock mode on MODE_SEL1, BRIDGE_CLK_MODE will be set to 00. If device is strapped for Discontinuous clock mode, BRIDGE_CLK_MODE will be set to 01.

8.6.1.60 TDM_CONFIG Register (Address = 57h) [reset = Ah]

TDM_CONFIG is described in Table 74.

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Table 74. TDM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved

Table 74. TDM_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TDM_FS_MODE	R/W	1h	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0 : Active high Frame Sync 1 : Active low Frame Sync (similar to I2S word select) This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
2	TDM_DELAY	R/W	0h	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0 : Data is not delayed from Frame Sync (data is left justified) 1 : Data is delayed 1 bit from Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
1-0	TDM_FS_WIDTH	R/W	2h	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion 00 : FS is 50/50 duty cycle 01 : FS is one slot/channel wide 1x : FS is 1 clock pulse wide

8.6.1.61 VIDEO_3D_STS Register (Address = 58h) [reset = 0h]

VIDEO_3D_STS is described in Table 75.

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Table 75. VIDEO_3D_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	LINE_OV_ERR	R/COR	0h	Line Buffer Overflow: When set to a 1, an error has been detected in the 3D video Line buffers due to receiving a video line that was too long for the buffer. For Alternate Line 3D mode, this flag will be set if a video line contains 4096 or more pixels. For Left/Right 3D, or Alternate Pixel 3D modes, this flag will be set if a video line contains 8192 or more pixels. This flag will be cleared on read.
1	LINE_VID_ERR	R/COR	0h	Line Video Error: When set to a 1, an error has been detected in the 3D video processing likely due to invalid line length or blanking intervals. This flag will be cleared on read.
0	LINE_MISMATCH	R/COR	0h	Line Mismatch Error Alternate Line 3D mode: When set to a 1, odd/even video line length mismatch has been detected. This will occur if the odd and even lines of video are not the same length. This flag will be cleared on read. Left/Right 3D mode: When set to a 1, a line length error has been detected. This will occur if the received video line is not twice the IMG_LINE_SIZE value. If the received line length is less than IMG_LINE_SIZE, an error may not be detected. This flag will be cleared on read. If the image is cropped in the horizontal dimension, this error flag may not be accurate.

8.6.1.62 DUAL_DSI_CTL_STS Register (Address = 59h) [reset = 0h]

DUAL_DSI_CTL_STS is described in Table 76.

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Table 76. DUAL_DSI_CTL_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DSI1_DELAY	R/W	0h	DSI Port 1 input delay The DSI Port 1 input can be delayed by up to 3 pixel clocks prior to merging dual DSI video data. This can be done for diagnostic purposes or to compensate for known skew between DSI ports.
5-4	DSI0_DELAY	R/W	0h	DSI Port 0 input delay The DSI Port 0 input can be delayed by up to 3 pixel clocks prior to merging dual DSI video data. This can be done for diagnostic purposes or to compensate for known skew between DSI ports.
3	DUAL_DSI_OK	R	0h	Dual DSI Status This register indicates if both DSI lanes are active and the skew is within a measurable range.
2	DSI_SKEW_NEG	R	0h	Dual Skew Negative indication In Dual DSI mode, this bit indicates if the skew between DSI Ports is positive or negative 0 : DSI Port 0 leads DSI Port 1 (or skew is 0) 1 : DSI Port 1 leads DSI Port 1
1-0	DSI_SKEW_MAG	R	0h	Dual DSI Skew Magnitude This register indicates the magnitude of detected skew between DSI ports in pixel clocks.

8.6.1.63 DUAL_STS_DUAL_STS_P1 Register (Address = 5Ah) [reset = 0h]

DUAL_STS_DUAL_STS_P1 is described in Table 77.

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Table 77. DUAL_STS_DUAL_STS_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FPD3_LINK_RDY FPD3_LINK_RDY_P1	R	0h	FPD-Link III Link Ready status for selected port: This bit indicates that the FPD-Link III link has detected a valid downstream connection and determined capabilities for the downstream link. In Independent 2:2 mode, this shows status for the selected FPD-Link III port.
6	FPD3_TX_STS FPD3_TX_STS_P1	R	0h	FPD-Link III Transmit status for selected port: This bit indicates that the FPD-Link III Transmitter is active and the receiver is locked to the transmit clock. It is only asserted once a valid input has been detected, and the FPD-Link III Transmit connection has entered the correct mode (that is, Single vs Dual mode). In Independent 2:2 mode, this shows status for the selected FPD-Link III port.
5-4	FPD3_PORT_STS	R	0h	FPD-Link III Port Status for selected port: If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 00: Dual FPD-Link III Transmitter mode 01: Single FPD-Link III Transmit on port 0 10: Single FPD-Link III Transmit on port 1 11: FPD-Link III Transmit on both ports (Independent 2:2, Replicate, or Splitter mode)
3	DSI_CLK_DET DSI_CLK_DET_P1	R	0h	DSI Clock Detect for selected port: DSI Clock Detect indication from the DSI PLL controller. In Independent 2:2 mode, this shows status for the selected FPD-Link III port.

Table 77. DUAL_STS_DUAL_STS_P1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DSI_PLL_LOCK DSI_PLL_LOCK_P1	R	0h	DSI PLL lock status for selected port: Indicates the DSI PLL has locked to the incoming DSI clock. In Independent 2:2 mode, this shows status for the selected FPD-Link III port.
1	NO_DSI_CLK NO_DSI_CLK_P1	R	0h	No DSI Clock Detected for selected port: This bit indicates the Frequency Detect circuit did not detect a DSI clock greater than the value specified in the FREQ_LOW register. In Independent 2:2 mode, this shows status for the selected FPD-Link III port.
0	FREQ_STABLE FREQ_STABLE_P1	R	0h	DSI Frequency is Stable: Indicates the Frequency Detection circuit has detected a stable DSI clock frequency. In Independent 2:2 mode, this shows status for the selected FPD-Link III port.

8.6.1.64 DUAL_CTL1 Register (Address = 5Bh) [reset = Strap]

DUAL_CTL1 is described in Table 78.

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Table 78. DUAL_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FPD3_COAX_MODE	R/W	Strap	FPD-Link III Coax Mode: Enables configuration for the FPD-Link III Interface cabling type 0 : Twisted Pair 1 : Coax This bit is loaded from the MODE_SEL1 pin at power-up.
6	DUAL_SWAP	R/W	0h	Dual Swap Control: Indicates current status of the Dual Swap control. If automatic correction of Dual Swap is disabled through the DISABLE_DUAL_SWAP control, this bit may be modified by software.
5	RST_PLL_FREQ	R/W	0h	Reset FPD-Link III PLL on Frequency Change: When set to a 1, frequency changes detected by the Frequency Detect circuit will result in a reset of the FPD-Link III PLL.
4	FREQ_DET_PLL	R/W	0h	Frequency Detect Select PLL Clock: Determines the clock source for the Frequency detection circuit: 0 : DSI clock (prior to PLL) 1: DSI PLL clock
3	DUAL_ALIGN_DE	R/W	0h	Dual Align on DE: In dual-link mode, if this bit is set to a 1, the odd/even data will be sent on the primary/secondary links respectively, based on the assertion of DE. If this bit is set to a 0, data will be sent on alternating links without regard to odd/even pixel position.

Table 78. DUAL_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	FPD3_TX_MODE	R/W/S	Strap	FPD-Link III TX Mode: This register controls the operating mode of the FPD-Link III Transmit function. By default, the FPD-Link III Transmitter auto-detects the best operating mode based on attached device(s). The FPD-Link III Transmit can also be forced to specific operation. 000 : Auto-Detect FPD-Link III mode (Single, Dual, or Replicate) 001 : Forced Single FPD-Link III Transmitter mode (Port 1 disabled) 010 : Reserved 011 : Forced Dual FPD-Link III Transmitter mode 100 : Auto-Detect FPD-Link III mode (Single or Replicate only, Dual disabled) 101 : Forced Independent 2:2 mode 110 : Reserved 111 : Forced Splitter Mode (half of video stream on each port) This field is loaded from MODE_SEL0 pin at power-up. Setting at power-up is either 000 or 111. Note: Independent 2:2 mode should only be enabled while the DSI inputs are disabled through the DISABLE_DSI control in the RESET_CTL register.

8.6.1.65 DUAL_CTL2 Register (Address = 5Ch) [reset = 7h]

DUAL_CTL2 is described in Table 79.

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Table 79. DUAL_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DISABLE_DUAL_SWAP	R/W	0h	Disable Dual Swap: Prevents automatic correction of swapped Dual link connection. Setting this bit allows writes to the DUAL_SWAP control in the DUAL_CTL1 register
6	FORCE_LINK_RDY FORCE_LINK_RDY_P1	R/W	0h	Force Link Ready: Forces link ready indication, bypassing back channel link detection. To enable desired operation, it may be necessary to force the Deserializer capabilites registers (DES_CAP1 and DES_CAP2) for each port. In Independent 2:2 mode, this controls the selected FPD-Link III port.
5	FORCE_CLK_DET FORCE_CLK_DET_P1	R/W	0h	Force Clock Detect: Forces the DSI clock detect circuit to indicate presence of a valid input clock. This bypasses the clock detect circuit, allowing operation with an input clock that does not meet frequency or stability requirements. In Independent 2:2 mode, this controls the selected FPD-Link III port.
4-3	FREQ_STBL_THR FREQ_STBL_THR_P1	R/W	0h	Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40us 01 : 80us 10 : 320us 11 : 1.28ms In Independent 2:2 mode, this controls the selected FPD-Link III port.
2-0	FREQ_HYST FREQ_HYST_P1	R/W	7h	Frequency Detect Hysteresis: The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz. In Independent 2:2 mode, this controls the selected FPD-Link III port.

8.6.1.66 FREQ_LOW Register (Address = 5Dh) [reset = 6h]

FREQ_LOW is described in Table 80.

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Table 80. FREQ_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FREQ_HYST_MODE	R/W	0h	Frequency Detect Hysteresis Mode: 0 : When frequency is not stable, allow saved frequency to update as long as within hysteresis from previous measurement 1 : Legacy operation. When frequency is not stable, maintain initial frequency measurement as long as within hysteresis from initial measurement.
6	DSI_RST_MODE	R/W	0h	DSI Phy Reset Mode: 0 : Reset DSI Phy on change in mode or frequency 1 : Don't reset DSI Phy on change in mode or frequency
5-0	FREQ_LO_THR	R/W	6h	Frequency Low Threshold: Sets the low threshold for the DSI Clock frequency detect circuit in MHz. This value is used to determine if the DSI clock frequency is too low for proper operation.

8.6.1.67 FREQ_HIGH Register (Address = 5Eh) [reset = 2Ch]

FREQ_HIGH is described in Table 81.

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Table 81. FREQ_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	FREQ_HI_THR	R/W	2Ch	Frequency High Threshold: Sets the high threshold for the DSI Clock frequency detect circuit in MHz.

8.6.1.68 DSI_FREQ_DSI_FREQ_P1 Register (Address = 5Fh) [reset = 0h]

DSI_FREQ_DSI_FREQ_P1 is described in Table 82.

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Table 82. DSI_FREQ_DSI_FREQ_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DSI_FREQ	R	0h	DSI Pixel Frequency: Returns the value of the DSI pixel Frequency of the video data in MHz for the selected port. This register indicates the pixel rate for the incoming data (pixel size is 24-bits). DSI Lane frequency in Mbps can be determined through the following ratio based on the number of lanes: 1 lane: DSI lane frequency = DSI Pixel frequency * 24 2 lanes: DSI lane frequency = DSI Pixel frequency * 12 3 lanes: DSI lane frequency = DSI Pixel frequency * 8 4 lanes: DSI lane frequency = DSI Pixel frequency * 6 A value of 0 indicates the DSI receiver is not detecting a valid signal. In External or Internal Reference Clock modes, the register will report the pixel clock frequency used to forward the video rather than the DSI pixel clock. In Dual-DSI mode, the DSI Pixel frequency is the frequency for the two ports combined, or twice the frequency for a single DSI port. In that case, the DSI Lane frequency is 1/2 of the values computed above. In Splitter Mode, this register reports the FPD-Link III pixel clock frequency for the selected port rather than the DSI input frequency.

8.6.1.69 SPI_TIMING1 Register (Address = 60h) [reset = 22h]

SPI_TIMING1 is described in Table 83.

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Table 83. SPI_TIMING1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SPI_HOLD	R/W	2h	SPI Data Hold from SPI clock: These bits set the minimum hold time for SPI data following the SPI clock sampling edge. In addition, this also sets the minimum active pulse width for the SPI output clock. Hold = (SPI_HOLD + 1) * 40ns For example, default setting of 2 will result in 120ns data hold time.
3-0	SPI_SETUP	R/W	2h	SPI Data Setup to SPI Clock: These bits set the minimum setup time for SPI data to the SPI clock active edge. In addition, this also sets the minimum inactive width for the SPI output clock. Hold = (SPI_SETUP + 1) * 40ns For example, default setting of 2 will result in 120ns data setup time.

8.6.1.70 SPI_TIMING2 Register (Address = 61h) [reset = 2h]

SPI_TIMING2 is described in Table 84.

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Table 84. SPI_TIMING2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	SPI_SS_SETUP	R/W	2h	SPI Slave Select Setup: This field controls the delay from assertion of the Slave Select low to initial data timing. Delays are in units of 40ns. Delay = (SPI_SS_SETUP + 1) * 40 ns

8.6.1.71 SPI_CONFIG Register (Address = 62h) [reset = 0h]

SPI_CONFIG is described in Table 85.

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Table 85. SPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_MSTR_OVER	R	0h	SPI Master Overflow Detection: This flag is set if the SPI Master detects an overflow condition. This occurs if the SPI Master is unable to regenerate the remote SPI data at a fast enough rate to keep up with data arriving from the remote Deserializer. If this condition occurs, it suggests the SPI_SETUP and SPI_HOLD times should be set to smaller values. This flag is cleared by setting the SPI_CLR_OVER bit in this register.
6-3	RESERVED	R	0h	Reserved
2	SPI_CLR_OVER	R/W	0h	Clear SPI Master Overflow Flag: Setting this bit to 1 will clear the SPI Master Overflow Detection flag (SPI_MSTR_OVER). This bit is not self-clearing and must be set back to 0.
1	SPI_CPHA	R	0h	SPI Clock Phase setting: Determines which phase of the SPI clock is used for sampling data. 0: Data sampled on leading (first) clock edge 1: Data sampled on trailing (second) clock edge This bit is read-only, with a value of 0. The DS90UB949 does not support CPHA of 1.

Table 85. SPI_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SPI_CPOL	R/W	0h	SPI Clock Polarity setting: Determines the base (inactive) value of the SPI clock. 0: base value of the clock is 0 1: base value of the clock is 1 This bit affects both capture and propagation of SPI signals.

8.6.1.72 VCID_SPLIT_CTL Register (Address = 63h) [reset = 0h]

VCID_SPLIT_CTL is described in Table 86.

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Table 86. VCID_SPLIT_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	VCID_SHARE_VS	R/W	0h	VC-ID Splitter mode, Share VS: During VC-ID Splitter mode, setting this bit allows both ports to use a shared VSYNC signal. The VC-ID will be ignored for VSYNC detection in the DSI input.
4-3	VCID_SEL_P1	R/W	0h	VC-ID Select during VC-ID Split Mode: These fields select the VC-ID for port 0 during VC-ID Split Mode.
2-1	VCID_SEL_P0	R/W	0h	VC-ID Select during VC-ID Split Mode: These fields select the VC-ID for port 1 during VC-ID Split Mode.
0	VCID_SPLIT_EN	R/W	0h	Enable VC-ID Split: Setting this bit to a 1 will enabling the DS90UB941AS-Q1 to split a 3D image based on the Virtual Channel ID (VC-ID) for each video line.

8.6.1.73 PGCTL_PGCTL_P1 Register (Address = 64h) [reset = 10h]

PGCTL_PGCTL_P1 is described in Table 87.

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Table 87. PGCTL_PGCTL_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_SEL	R/W	1h	In Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode: 0000: Checkerboard 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/White to Cyan 1000: Horizontally Scaled Black to Green/White to Magenta 1001: Horizontally Scaled Black to Blue/White to Yellow 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertically Scaled Black to Green/White to Magenta 1101: Vertically Scaled Black to Blue/White to Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: VCOM In Independent 2:2 mode, this controls the selected FPD-Link III port.

Table 87. PGCTL_PGCTL_P1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0h	Reserved
2	PATGEN_COLOR_BARS	R/W	0h	Enable Color Bars 0: Color Bars disabled 1: Color Bars enabled (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)
1	RESERVED	R	0h	Reserved
0	PATGEN_EN	R/W	0h	Pattern Generator Enable: 1: Enable Pattern Generator 0: Disable Pattern Generator

8.6.1.74 PGCFG_PGCFG_P1 Register (Address = 65h) [reset = 0h]

PGCFG_PGCFG_P1 is described in Table 88.

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Table 88. PGCFG_PGCFG_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	PATGEN_SCALE_CHKR	R/W	0h	Scale Checkered Patterns: 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels 0: Normal operation (each square is 1x1 pixel) Setting this bit allows better visibility of the checkered patterns. In Independent 2:2 mode, this controls the selected FPD-Link III port.
5	PATGEN_CUST_CHKR	R/W	0h	Use Custom Checkerboard Color 1: Use the Custom Color (Pattern Type 14) and black in the Checkerboard pattern 0: Use white and black in the Checkerboard pattern In Independent 2:2 mode, this controls the selected FPD-Link III port.
4	PATGEN_18B	R/W	0h	18-bit Mode Select: 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. In Independent 2:2 mode, this controls the selected FPD-Link III port.
3	PATGEN_EXTCLK	R/W	0h	Select External Clock Source: 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0). In Independent 2:2 mode, this controls the selected FPD-Link III port.
2	PATGEN_TSEL	R/W	0h	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. In Independent 2:2 mode, this controls the selected FPD-Link III port.
1	PATGEN_INV	R/W	0h	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output. In Independent 2:2 mode, this controls the selected FPD-Link III port.
0	PATGEN_ASCRL	R/W	0h	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern. In Independent 2:2 mode, this controls the selected FPD-Link III port.

8.6.1.75 PGIA_PGIA_P1 Register (Address = 66h) [reset = 0h]

PGIA_PGIA_P1 is described in Table 89.

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Table 89. PGIA_PGIA_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_IA	R/W	0h	Indirect Address: This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. In Independent 2:2 mode, this controls the selected FPD-Link III port.

8.6.1.76 PGID_PGID_P1 Register (Address = 67h) [reset = 0h]

PGID_PGID_P1 is described in Table 90.

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Table 90. PGID_PGID_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_ID	R/W	0h	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value. In Independent 2:2 mode, this controls the selected FPD-Link III port.

8.6.1.77 IMG_HSYNC_CTL0_IMG_HSYNC_CTL0_P1 Register (Address = 6Ah) [reset = 0h]

IMG_HSYNC_CTL0_IMG_HSYNC_CTL0_P1 is described in Table 91.

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Table 91. IMG_HSYNC_CTL0_IMG_HSYNC_CTL0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HBACK_OV_EN HBACK_OV_EN_P1	R/W	0h	Dual-Image HSync Control Register 0 Provides control of HSync generation for Dual-Image operation including splitter mode. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port. HBACK Override Enable During dual-image processing (3D images or splitter operation), the device regenerates the horizontal sync back porch from the input data. Setting this bit to 1 will use the IMG_HBACK value instead of the measured value. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port.
6	RESERVED	R	0h	Reserved
5-4	IMG_HBACK_9:8 IMG_HBACK_P1_9:8	R/W	0h	HBACK Override value (bits 9:8) During dual-image processing (3D images or splitter operation), the device regenerates the horizontal sync back porch from the input data. Setting the HBACK_OV_EN control to 1 will use the IMG_HBACK value instead of the measured value. The IMG_HBACK value should be set to the value of the 3D image horizontal back porch, or twice the 2D image value. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port.
3	HSYNC_OV_EN HSYNC_OV_EN_P1	R/W	0h	HSYNC Override Enable During dual-image processing (3D images or splitter operation), the device regenerates the horizontal sync pulse-width from the input data. Setting this bit to 1 will use the IMG_HSYNC value instead of the measured value. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port.
2	RESERVED	R	0h	Reserved

Table 91. IMG_HSYNC_CTL0_IMG_HSYNC_CTL0_P1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	IMG_HSYNC_9:8 IMG_HSYNC_P1_9:8	R/W	0h	HSYNC Override value (bits 9:8) During dual-image processing (3D images or splitter operation), the device regenerates the horizontal sync pulse-width from the input data. Setting the HSYNC_OV_EN control to 1 will use the IMG_HSYNC value instead of the measured value. The IMG_HBACK value should be set to the value of the 3D image horizontal back porch, or twice the 2D image value. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port.

8.6.1.78 IMG_HSYNC_CTL1_IMG_HSYNC_CTL1_P1 Register (Address = 6Bh) [reset = 0h]

IMG_HSYNC_CTL1_IMG_HSYNC_CTL1_P1 is described in Table 92.

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Table 92. IMG_HSYNC_CTL1_IMG_HSYNC_CTL1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMG_HSYNC_7:0 IMG_HSYNC_P1_7:0	R/W	0h	Dual-Image HSync Control Register 1 Provides control of HSync generation for Dual-Image operation including splitter mode. HSYNC Override value (bits 7:0) During dual-image processing (3D images or splitter operation), the device regenerates the horizontal sync pulse-width from the input data. Setting the HSYNC_OV_EN control to 1 will use the IMG_HSYNC value instead of the measured value. The IMG_HBACK value should be set to the value of the 3D image horizontal back porch, or twice the 2D image value. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port.

8.6.1.79 IMG_HSYNC_CTL2_IMG_HSYNC_CTL2_P1 Register (Address = 6Ch) [reset = 0h]

IMG_HSYNC_CTL2_IMG_HSYNC_CTL2_P1 is described in Table 93.

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Table 93. IMG_HSYNC_CTL2_IMG_HSYNC_CTL2_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMG_HBACK_7:0 IMG_HBACK_P1_7:0	R/W	0h	Dual-Image HSync Control Register 2 Provides control of HSync back porch generation for Dual-Image operation including splitter mode. HBACK Override value (bits 7:0) During dual-image processing (3D images or splitter operation), the device regenerates the horizontal sync back porch from the input data. Setting the HBACK_OV_EN control to 1 will use the IMG_HBACK value instead of the measured value. The IMG_HBACK value should be set to the value of the 3D image horizontal back porch, or twice the 2D image value. In Independent 2:2 or Splitter modes, this register controls the selected FPD-Link III port.

8.6.1.80 BCC_STATUS Register (Address = 6Dh) [reset = 0h]

BCC_STATUS is described in Table 94.

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Table 94. BCC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	BCC Status Register This register provides error status for the Bidirectional Control Channel. Reserved
4	BCC_MASTER_ERR	R/COR	0h	BCC Master Error This flag indicates a back channel CRC error or loss of back channel Lock occurred while waiting for a response from the Deserializer while the BCC I2C Master is active. This flag is cleared on read of this register.
3	BCC_MASTER_TO	R/COR	0h	BCC Slave Timeout Error This bit will be set if the BCC Watchdog Timer expires. Will wait for a response from the Deserializer while the BCC I2C Master is active. This flag is cleared on read of this register.
2	BCC_SLAVE_ERR	R/COR	0h	BCC Slave Error This flag indicates a back channel CRC error or loss of back channel Lock occurred while waiting for a response from the Deserializer while the BCC I2C Slave is active. This flag is cleared on read of this register.
1	BCC_SLAVE_TO	R/COR	0h	BCC Slave Timeout Error This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the Deserializer while the BCC I2C Slave is active. This flag is cleared on read of this register.
0	BCC_RESP_ERR	R/COR	0h	This flag indicates an error has been detected in response to a command on the Bidirectional Control Channel. When the Serializer sends a control channel frame, the Deserializer should return the 8-bit data field in the subsequent response. The Serializer checks the returned data for errors, and will set this flag if an error is detected. This flag is cleared on read of this register.

8.6.1.81 BCC_CONFIG Register (Address = 6Eh) [reset = 20h]

BCC_CONFIG is described in Table 95.

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Table 95. BCC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	I2C_Master_Disable	R/W	1h	This bit will disable the remote reads and writes from the I2C master. I2C master writes and reads to the local registers will still work, but remote writes and reads will not 1: I2C master remote read/writes is disabled 0: I2C master remote read/write is enabled
4	BCC_TERM_ON_ERR	R/RC	0h	Terminate Control Channel transactions on CRC Error detection During control channel operations, if a CRC Error occurs, it is unlikely to affect control channel operation. Setting this bit will allow more conservative operation that terminates any active Control Channel operation if an error is detected in the back channel. 0 : Don't terminate BCC transactions on CRC Errors 1 : Terminate BCC transactions on CRC Errors This bit will have no effect if Enhanced Error checking is disabled (BCC_EN_ENH_ERROR set to 0).
3	RESERVED	R/W	0h	Reserved

Table 95. BCC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BCC_ACK_REMOTE_READ	R/RC	0h	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Serializer to generate an internal acknowledge to the beginning of a remote I2C slave read. This allows additional error detection at the Deserializer. This bit should not be set when operating with Deserializers that do not support Enhanced Error Checking. 0: Disable 1: Enable
1	BCC_EN_DATA_CHK	R/RC	0h	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, if an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit should not be set when operating with Deserializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. 0: Disable returned data error detection 1: Enable returned data error detection
0	BCC_EN_ENH_ERROR	R/RC	0h	Enable Enhanced Error checking in Bidirectional Control Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0: Disable Enhanced Error checking 1: Enable Enhanced Error checking

8.6.1.82 FC_BCC_TEST Register (Address = 6Fh) [reset = 0h]

FC_BCC_TEST is described in Table 96.

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Table 96. FC_BCC_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	FORCE_BCC_ERROR	SC	0h	Force an error on forward channel BCC frame Setting the FORCE_BCC_ERROR bit will cause an error to be forced on a forward channel BCC frame. The BCC_ERROR_SEL and BCC_FRAME_SEL fields in this register determine the type of error to be forced and which frame will include the error. This bit is self-clearing and will always return 0.
5-3	BCC_ERROR_SEL	R/W	0h	BCC Error Select The BCC Error Select determines which type of error is forced on a forward channel BCC frame. 000 : No error 001 : Force CRC Error 010 : Force Sequence Error (skips one sequence number) 011 : Drop BCC Frame (results in sequence error at Deserializer) 100 : Force error on Data field (random bit 1 through 7) 101 : Force error on Data field, bit 0 (RW bit if during Start command) 110 - 111 : Reserved
2-0	BCC_FRAME_SEL	R/W	0h	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

8.6.1.83 SlaveID_1 Register (Address = 70h) [reset = 0h]

SlaveID_1 is described in Table 97.

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Table 97. SlaveID_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID1	R/W	0h	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0h	Reserved

8.6.1.84 SlaveID_2 Register (Address = 71h) [reset = 0h]

SlaveID_2 is described in Table 98.

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Table 98. SlaveID_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID2	R/W	0h	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0h	Reserved

8.6.1.85 SlaveID_3 Register (Address = 72h) [reset = 0h]

SlaveID_3 is described in Table 99.

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Table 99. SlaveID_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID3	R/W	0h	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0h	Reserved

8.6.1.86 SlaveID_4 Register (Address = 73h) [reset = 0h]

SlaveID_4 is described in Table 100.

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Table 100. SlaveID_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID4	R/W	0h	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.

Table 100. SlaveID_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0h	Reserved

8.6.1.87 SlaveID_5 Register (Address = 74h) [reset = 0h]

SlaveID_5 is described in Table 101.

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Table 101. SlaveID_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID5	R/W	0h	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0h	Reserved

8.6.1.88 SlaveID_6 Register (Address = 75h) [reset = 0h]

SlaveID_6 is described in Table 102.

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Table 102. SlaveID_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID6	R/W	0h	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0h	Reserved

8.6.1.89 SlaveID_7 Register (Address = 76h) [reset = 0h]

SlaveID_7 is described in Table 103.

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Table 103. SlaveID_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID7	R/W	0h	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	RESERVED	R	0h	Reserved

8.6.1.90 SlaveAlias_1 Register (Address = 77h) [reset = 0h]

SlaveAlias_1 is described in Table 104.

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Table 104. SlaveAlias_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID1	R/W	0h	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.91 SlaveAlias_2 Register (Address = 78h) [reset = 0h]

SlaveAlias_2 is described in Table 105.

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Table 105. SlaveAlias_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID2	R/W	0h	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.92 SlaveAlias_3 Register (Address = 79h) [reset = 0h]

SlaveAlias_3 is described in Table 106.

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Table 106. SlaveAlias_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID3	R/W	0h	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.93 SlaveAlias_4 Register (Address = 7Ah) [reset = 0h]

SlaveAlias_4 is described in Table 107.

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Table 107. SlaveAlias_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID4	R/W	0h	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.

Table 107. SlaveAlias_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0h	Reserved

8.6.1.94 SlaveAlias_5 Register (Address = 7Bh) [reset = 0h]

SlaveAlias_5 is described in Table 108.

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Table 108. SlaveAlias_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID5	R/W	0h	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.95 SlaveAlias_6 Register (Address = 7Ch) [reset = 0h]

SlaveAlias_6 is described in Table 109.

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Table 109. SlaveAlias_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID6	R/W	0h	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.96 SlaveAlias_7 Register (Address = 7Dh) [reset = 0h]

SlaveAlias_7 is described in Table 110.

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Table 110. SlaveAlias_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID7	R/W	0h	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.97 CFG Register (Address = C2h) [reset = 82h]

CFG is described in Table 111.

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Table 111. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	1h	Reserved
6	Reserved	R/W	0h	Reserved
5	Reserved	R/W	0h	Reserved
4-3	Reserved	R/W	0h	Reserved
2	Reserved	R/W	0h	Reserved
1	RX_DET_SEL	R/W	1h	RX Detect Select: Controls assertion of the Receiver Detect Interrupt. If set to 0, the Receiver Detect Interrupt will be asserted on detection of an FPD-Link III Receiver. If set to 1, the Receiver Detect Interrupt will also require a receive lock indication from the receiver.
0	Reserved	R/W	0h	Reserved

8.6.1.98 STS Register (Address = C4h) [reset = 0h]

STS is described in Table 112.

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Table 112. STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/COR	0h	Reserved
6	RX_INT	R	0h	RX Interrupt : Status of the RX Interrupt signal. The signal is received from the attached Receiver and is the status on the INTB_IN pin of the Receiver. The signal is active low, so a 0 indicates an interrupt condition.
5	RX_LOCK_DET	R	0h	Receiver Lock Detect : This bit indicates that the downstream Receiver has indicated Receive Lock to incoming serial data.
4	Reserved	R/COR	0h	Reserved
3	RX_DETECT	R	0h	Receiver Detect : This bit indicates that a downstream Receiver has been detected.
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

8.6.1.99 ICR Register (Address = C6h) [reset = 0h]

ICR is described in Table 113.

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Table 113. ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/RC	0h	Reserved
6	IE_RXDET_INT	R/W	0h	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.

Table 113. ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	IE_RX_INT	R/W	0h	Interrupt on Receiver interrupt: Enables interrupt on indication from the Receiver. Allows propagation of interrupts from downstream devices.
4	Reserved	R/RC	0h	Reserved
3	Reserved	R/W	0h	Reserved
2	Reserved	R/W	0h	Reserved
1	Reserved	R/W	0h	Reserved
0	INT_EN	R/W	0h	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

8.6.1.100 ISR Register (Address = C7h) [reset = 0h]

ISR is described in Table 114.

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Table 114. ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	IS_RXDET_INT	R	0h	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected.If CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
5	IS_RX_INT	R	0h	Interrupt on Receiver interrupt: Receiver has indicated an interrupt request from down-stream device.
4	Reserved	R	0h	Reserved
3	Reserved	R	0h	Reserved
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	INT	R	0h	Global Interrupt: Set if any enabled interrupt is indicated.

8.6.1.101 TX_ID0 Register (Address = F0h) [reset = 5Fh]

TX_ID0 is described in Table 115.

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Table 115. TX_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_ID0	R	5Fh	TX_ID0: First byte ID code, '_ '

8.6.1.102 TX_ID1 Register (Address = F1h) [reset = 55h]

TX_ID1 is described in Table 116.

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Table 116. TX_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_ID1	R	55h	TX_ID1: 2nd byte of ID code, 'U '

8.6.1.103 TX_ID2 Register (Address = F2h) [reset = 42h]

TX_ID2 is described in Table 117.

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Table 117. TX_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_ID2	R	42h	TX_ID2: 3rd byte of ID code. 'B'

8.6.1.104 TX_ID3 Register (Address = F3h) [reset = 39h]

TX_ID3 is described in Table 118.

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Table 118. TX_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_ID3	R	39h	TX_ID3: 4th byte of ID code, '9 '

8.6.1.105 TX_ID4 Register (Address = F4h) [reset = 34h]

TX_ID4 is described in Table 119.

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Table 119. TX_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_ID4	R	34h	TX_ID4: 5th byte of ID code, '4'

8.6.1.106 TX_ID5 Register (Address = F5h) [reset = 31h]

TX_ID5 is described in Table 120.

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Table 120. TX_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_ID5	R	31h	TX_ID5: 6th byte of ID code, '1'

8.6.2 DSI Port 0 and Port 1 Indirect Registers

Table 121 summarizes the DS90UB941AS-Q1 indirect DSI registers. All register offset addresses not listed in Table 121 should be considered as reserved locations and the register contents should not be modified.

Register access is provided through an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0x40-0x42 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
   – For selecting DSI/D-PHY Port 0 Indirect Registers set 0x40 = 0x04
   – For selecting DSI/D-PHY Port 1 Indirect Registers set 0x40 = 0x08
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
   – For selecting and reading from DSI/D-PHY Port 0 Indirect Registers set 0x40 = 0x05
   – For selecting and reading from DSI/D-PHY Port 1 Indirect Registers set 0x40 = 0x09
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will read additional data bytes from subsequent register offset locations.

Table 121. DSI Indirect Registers Summary

Offset	Acronym	Register Name	Section
0h	DSI_ERR_COUNT		Go
1h	DPHY_TINIT_TIMING		Go
2h	DPHY_TERM_TIMING		Go
3h	DPHY_CLK_SETTLE_TIMING		Go
4h	DPHY_HS_SETTLE_TIMING		Go
5h	DPHY_SKIP_TIMING		Go
6h	DPHY_LP_POLARITY		Go
7h	DPHY_BYPASS		Go
8h	HSRX_TO_CNT		Go
Fh	DPHY_STATUS		Go
10h	DPHY_DLANE0_ERR		Go
11h	DPHY_DLANE1_ERR		Go
12h	DPHY_DLANE2_ERR		Go
13h	DPHY_DLANE3_ERR		Go
14h	DPHY_ERR_CLK_LANE		Go
15h	DPHY_SYNC_STS		Go
20h	DSI_CONFIG_0		Go
21h	DSI_CONFIG_1		Go
22h	DSI_ERR_CFG_0		Go

Table 121. DSI Indirect Registers Summary (continued)

Offset	Acronym	Register Name	Section
23h	DSI_ERR_CFG_1		Go
28h	DSI_STATUS		Go
2Ah	DSI_VC_DTYPE		Go
2Bh	DSI_ERR_RPT_0		Go
2Ch	DSI_ERR_RPT_1		Go
2Dh	DSI_ERR_RPT_2		Go
30h	DSI_HSW_CFG_HI		Go
31h	DSI_HSW_CFG_LO		Go
32h	DSI_VSW_CFG_HI		Go
33h	DSI_VSW_CFG_LO		Go
34h	DSI_SYNC_DLY_CFG_HI		Go
35h	DSI_SYNC_DLY_CFG_LO		Go
36h	DSI_EN_HSRX		Go
37h	DSI_EN_LPRX		Go
38h	DSI_EN_RXTERM		Go
3Ah	DSI_PCLK_DIV_M		Go
3Bh	DSI_PCLK_DIV_N		Go

Table 160 shows the codes that are used for access types in this section.

Table 122. Register Access Type Codes

Access Type	Code	Description
R	R	Read only access
R/W	R/W	Read / Write access
R/W/RC	R/W/RC	Read / Write access / Read to Clear

8.6.2.1 DSI_ERR_COUNT Register (Offset = 0h) [reset = 0h]

DSI_ERR_COUNT is described in Table 123.

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Table 123. DSI_ERR_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DSI_ERROR_COUNT	R/W/RC	0h	DSI Error Count This register reports the number of DSI errors that have been detected. This value will be cleared on read. The DSI Error counter is for diagnostic purposes only and may not be an accurate count of the number of errors detected. For accurate reading of error counts, disable error counting by clearing the DSI_ERR_CFG_0/1 registers prior to reading the counter.

8.6.2.2 DPHY_TINIT_TIMING Register (Offset = 1h) [reset = 0h]

DPHY_TINIT_TIMING is described in Table 124.

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Table 124. DPHY_TINIT_TIMING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2-0	TINIT_TIME	R/W	0h	D-PHY Initialization Time after power up in 100-µs units Initialization time = (TINIT_TIME + 1) * 100 µs

8.6.2.3 DPHY_TERM_TIMING Register (Offset = 2h) [reset = 0h]

DPHY_TERM_TIMING is described in Table 125.

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Table 125. DPHY_TERM_TIMING Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	DPHY_TERM_DATA _TIMING	R/W	0h	TD TermEn terminal Count

8.6.2.4 DPHY_CLK_SETTLE_TIMING Register (Offset = 3h) [reset = 1Dh]

DPHY_CLK_SETTLE_TIMING is described in Table 126.

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Table 126. DPHY_CLK_SETTLE_TIMING Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	TCLK_SETTLE_CNT	R/W	1Dh	TCLK-SETTLE Tclk Settle terminal Count in units of 10ns

8.6.2.5 DPHY_HS_SETTLE_TIMING Register (Offset = 4h) [reset = 14h]

DPHY_HS_SETTLE_TIMING is described in Table 127.

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Table 127. DPHY_HS_SETTLE_TIMING Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-0	THS_SETTLE_CNT	R/W	14h	THS-SETTLE Settle terminal Count in units of 10ns.

8.6.2.6 DPHY_SKIP_TIMING Register (Offset = 5h) [reset = 3Ah]

DPHY_SKIP_TIMING is described in Table 128.

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Table 128. DPHY_SKIP_TIMING Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-1	TSKIP_CNT	R/W	1Dh	Tskip Count This register controls the amount of data that will be ignored at the end of transmission detection. This value is in units of the DDR clock (that is, two UI intervals). Setting of this register will be dependent on the D-PHY lane frequency.
0	RESERVED	R	0h	Reserved

8.6.2.7 DPHY_LP_POLARITY Register (Offset = 6h) [reset = 0h]

DPHY_LP_POLARITY is described in Table 129.

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Table 129. DPHY_LP_POLARITY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	POL_LP_CLK0	R/W	0h	LP Clock 0 Polarity
3-0	POL_LP_DATA	R/W	0h	LP Data Polarity

8.6.2.8 DPHY_BYPASS Register (Offset = 7h) [reset = 0h]

DPHY_BYPASS is described in Table 130.

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Table 130. DPHY_BYPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BYPASS_TINIT	R/W	0h	Bypass Tinit wait time
6	BYPASS_TCK_MISS	R/W	0h	Bypass Tck Miss time
5	BYPASS_ULPS_CK0	R/W	0h	Bypass ULPS for CLK0
4-0	BYPASS_LP	R/W	0h	Bypass Lp on clk and data lanes 3,2,1,0

8.6.2.9 HSRX_TO_CNT Register (Offset = 8h) [reset = 0h]

HSRX_TO_CNT is described in Table 131.

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Table 131. HSRX_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HSRX_TO_CNT	R/W	0h	Timeout counter in ms. The timer will have a 1-ms range Example: if HSRX_TO_CNT = 1, then the timeout will occur between 0-1 ms and if HSRX_TO_CNT = 255, then the timeout will occur between 254-255 ms. If the register value is 0, then the timeout will be off.

8.6.2.10 DPHY_STATUS Register (Offset = Fh) [reset = 0h]

DPHY_STATUS is described in Table 132.

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Table 132. DPHY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	LANE_SYNC_ERROR	R/ROC	0h	D-PHY Lane Sync Error This flag indicates the proper synchronization was not detected on all data lanes at the same time. Each enabled lane is expected to detect the sync sequence at the same time. If this does not occur correctly, this flag will be set. In addition, the DPHY_SYNC_STS register may be read to determine the synchronization status at the most recent error condition.
5	DPHY_LANE_ERROR	R	0h	D-PHY Lane Error Detected If this bit is set, one or more of the clock or data lanes has detected an error. To determine the error, read the DPHY_DLANEx_ERR ane DPHY_CLANE_ERR registers. This flag will be cleared when the Lane Error registers have been read.

Table 132. DPHY_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	C_LANE_ACTIVE	R	0h	Clock Lane Active 0 : Clock Lane not active 1 : Clock Lane active
3-0	D_LANE_ACTIVE	R	0h	Data Lanes Active For each data lane, this register reports if the lane is detected as active. 0 : Data Lane is not active 1 : Data Lane is active

8.6.2.11 DPHY_DLANE0_ERR Register (Offset = 10h) [reset = 0h]

DPHY_DLANE0_ERR is described in Table 133.

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Table 133. DPHY_DLANE0_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	EOT_SYNC_ERROR_0	R/ROC	0h	End of transmission sync error - Uncorrectable
3	SOT_ERROR_0	R/ROC	0h	Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_0	R/ROC	0h	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_0	R/ROC	0h	Control Error in HS Request Mode
0	HS_RX_TO_ERROR_0	R/ROC	0h	HS Transmission timeout error

8.6.2.12 DPHY_DLANE1_ERR Register (Offset = 11h) [reset = 0h]

DPHY_DLANE1_ERR is described in Table 134.

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Table 134. DPHY_DLANE1_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	EOT_SYNC_ERROR_1	R/ROC	0h	End of transmission sync error - Uncorrectable
3	SOT_ERROR_1	R/ROC	0h	Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_1	R/ROC	0h	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_1	R/ROC	0h	Control Error in HS Request Mode
0	HS_RX_TO_ERROR_1	R/ROC	0h	HS Transmission timeout error

8.6.2.13 DPHY_DLANE2_ERR Register (Offset = 12h) [reset = 0h]

DPHY_DLANE2_ERR is described in Table 135.

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Table 135. DPHY_DLANE2_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	EOT_SYNC_ERROR_2	R/ROC	0h	End of transmission sync error - Uncorrectable
3	SOT_ERROR_2	R/ROC	0h	Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_2	R/ROC	0h	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_2	R/ROC	0h	Control Error in HS Request Mode
0	HS_RX_TO_ERROR_2	R/ROC	0h	HS Transmission timeout error

8.6.2.14 DPHY_DLANE3_ERR Register (Offset = 13h) [reset = 0h]

DPHY_DLANE3_ERR is described in Table 136.

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Table 136. DPHY_DLANE3_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	EOT_SYNC_ERROR_3	R/ROC	0h	End of transmission sync error - Uncorrectable
3	SOT_ERROR_3	R/ROC	0h	Bit Error in SYNC Sequence - Correctable
2	SOT_SYNC_ERROR_3	R/ROC	0h	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_3	R/ROC	0h	Control Error in HS Request Mode
0	HS_RX_TO_ERROR_3	R/ROC	0h	HS Transmission timeout error

8.6.2.15 DPHY_ERR_CLK_LANE Register (Offset = 14h) [reset = 0h]

DPHY_ERR_CLK_LANE is described in Table 137.

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Table 137. DPHY_ERR_CLK_LANE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	CNTRL_ERR_ULPRQST_CLK	R/ROC	0h	Control Error in ULP Request Mode
2	CNTRL_ERR_HSRQST_CLK	R/ROC	0h	Control Error in HS Request Mode
1	ULPS_INVALID_ERR_CLK	R/ROC	0h	Invalid ULP state Detected in ULP Mode
0	HS_RX_TO_ERROR_CLK	R/ROC	0h	HS Transmission timeout error

8.6.2.16 DPHY_SYNC_STS Register (Offset = 15h) [reset = 0h]

DPHY_SYNC_STS is described in Table 138.

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Table 138. DPHY_SYNC_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	DLANE3_SYNC_STS	R	0h	Sync Status for DLANE 3 Reports synchronization status for Data Lane 3 during most recent Synchronization error
2	DLANE2_SYNC_STS	R	0h	Sync Status for DLANE 2 Reports synchronization status for Data Lane 3 during most recent Synchronization error
1	DLANE1_SYNC_STS	R	0h	Sync Status for DLANE 1 Reports synchronization status for Data Lane 3 during most recent Synchronization error
0	DLANE0_SYNC_STS	R	0h	Sync Status for DLANE 0 Reports synchronization status for Data Lane 3 during most recent Synchronization error

8.6.2.17 DSI_CONFIG_0 Register (Offset = 20h) [reset = 7Fh]

DSI_CONFIG_0 is described in Table 139.

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Table 139. DSI_CONFIG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	DSI_TRY_RECOVERY	R/W	1h	DSI Attempt Recovery When set to a 1, the DSI Protocol module will attempt to recover from error conditions.
5	DSI_IGNORE_HS_CMD	R/W	1h	Ignore DSI HS Commands 0 : Process HS Commands 1 : Ignore HS Commands
4	DSI_SYNC_PULSES	R/W	1h	Controls generation of Sync Pulses 0 : Don't regenerate original VS/HS timing 1 : Regenerate original VS/HS timing
3-0	DSI_VC_ENABLE	R/W	Fh	Enable VC-IDs Each bit in this four bit field enables one of the four Virtual Channel IDs. If a packet was received without an expected VC-ID, an error will be reported. For the error to be reported in the DSI_ERR_DET bit, the DSI_INV_VC_ERR_EN bit must also be set. These controls do not filter out packets with invalid VC-IDs.

8.6.2.18 DSI_CONFIG_1 Register (Offset = 21h) [reset = 0h]

DSI_CONFIG_1 is described in Table 140.

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Table 140. DSI_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DSI_NO_GRAYSCALE	R/W	0h	Disable Grayscale Interpolation For DSI RGB data types less than 24 bits, the conversion to RGB888 replicates the most significant subpixel bits on the otherwise-unused least significant subpixel bits to achieve a higher grayscale range. 0 : Enable Grayscale Interpolation 1 : Disable Grayscale Interpolation
6	DSI_VS_POLARITY	R/W	0h	DSI VS Polarity Control 0 : VS signal is active high 1 : VS signal is active low
5	DSI_HS_POLARITY	R/W	0h	DSI HS Polarity Control 0 : HS signal is active high 1 : HS signal is active low
4	DSI_HOLD_ERR	R/W	0h	Hold Error When set to 1, latched error conditions will be indicated on the dsi_err status indication rather than pulses.
3	DSI_NULL_CRC_DIS	R/W	0h	Error reporting for NULL and BLANK long packets
2	RESERVED	R/W	0h	Reserved
1	DSI_NO_FILTER	R/W	0h	Disable Filter on packet word count
0	DSI_NO_EOTPKT	R/W	0h	No EOT Packet mode If set to 0, the device will indicate and error if an End of Transmission occurs without an EOT Packet. If set to 0, no error will be indicated. The error is indicated in the DSI_EOT_ERR bit in the DSI_STATUS register.

8.6.2.19 DSI_ERR_CFG_0 Register (Offset = 22h) [reset = FFh]

DSI_ERR_CFG_0 is described in Table 141.

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Table 141. DSI_ERR_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DSI_ECC1_ERR_EN	R/W	1h	Enable Single-bit ECC errors on dsi_err status
6	DSI_CONT_LP1_ERR_EN	R/W	1h	Enable LP-1 Contention error on dsi_err status
5	DSI_CONT_LP0_ERR_EN	R/W	1h	Enable LP-0 Contention error on dsi_err status
4	DSI_LP_SYNC_ERR_EN	R/W	1h	Enable LP Sync error on dsi_err status
3	DSI_HSRX_TO_ERR_EN	R/W	1h	Enable HS Receive timeout error on dsi_err status
2	DSI_ESC_ENTRY_ERR_EN	R/W	1h	Enable escape Entry error on dsi_err status
1	DSI_SOT_SYNC_ERR_EN	R/W	1h	Enable SOT Sync error on dsi_err status
0	DSI_SOT_ERR_EN	R/W	1h	Enable SOT error on dsi_err status

8.6.2.20 DSI_ERR_CFG_1 Register (Offset = 23h) [reset = 7Fh]

DSI_ERR_CFG_1 is described in Table 142.

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Table 142. DSI_ERR_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	DSI_EOT_SYNC_ERR_EN	R/W	1h	Enable EOT Sync error on dsi_err status
5	DSI_PROT_ERR_EN	R/W	1h	Enable DSI Protocol errors on dsi_err status
4	DSI_INV_LEN_ERR_EN	R/W	1h	Enable Invalid Length errors on dsi_err status
3	DSI_INV_VC_ERR_EN	R/W	1h	Enable Invalid VC errors on dsi_err status
2	DSI_INV_DT_ERR_EN	R/W	1h	Enable Invalid DT errors on dsi_err status
1	DSI_CHKSUM_ERR_EN	R/W	1h	Enable 16-bit CRC Checksum errors on dsi_err status
0	DSI_ECC2_ERR_EN	R/W	1h	Enable Multi-bit ECC errors on dsi_err status

8.6.2.21 DSI_STATUS Register (Offset = 28h) [reset = 0h]

DSI_STATUS is described in Table 143.

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Table 143. DSI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

Table 143. DSI_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DSI_FIFO_OVERFLOW	R/ROC	0h	DSI to FPD-Link III FIFO Overflow When 1, this bit indicates one or more FIFO overflow errors have occurred in the video data crossing between the DSI and FPD-Link III domains. This bit is cleared on read unless another overflow occurs.
5	DSI_FIFO_UNDERFLOW	R/ROC	0h	
4	DSI_FPD3_ERR	R/ROC	0h	DSI to FPD-Link III Buffer Error This flag indicates a buffer overflow has occurred between the DSI Protocol logic and the FPD-Link III Transmitter. This flag will be cleared on read.
3	DSI_CMD_OVER	R/ROC	0h	DSI Command FIFO Overflow If the DSI Command FIFO Overflows, this bit will be set. This flag will be cleared on read. This is not supported because command mode is not implemented.
2	DSI_EOT_ERR	R/ROC	0h	DSI EOT Error detected If this bit is set, a DSI End-of-Transmission (EOT) has been detected without an EOT Packet. This bit will only be set of DSI_NO_EOTPKT is set to 0. This flag will be cleared on read.
1	DSI_READ_WOUT_BTA	R/ROC	0h	DSI Read without Bus Turn-Around (BTA) If this bit is set, a DSI Read has been detected without a Bus Turn-Around. This flag will be cleared on read. This is not supported because command mode is not implemented.
0	DSI_ERROR_DET	R/ROC	0h	DSI Error Detected If this bit is set, one or more DSI Errors has been detected. Error conditions that can cause a DSI error are configured through the DSI_ERR_CFG_0/1 registers. This flag will be cleared on read. The number of DSI error events may be read from the DSI_ERR_COUNT register.

8.6.2.22 DSI_VC_DTYPE Register (Offset = 2Ah) [reset = 0h]

DSI_VC_DTYPE is described in Table 144.

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Table 144. DSI_VC_DTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DSI_VC	R	0h	DSI Virtual Channel ID This field returns the Virtual Channel ID for the most recently received pixel stream packet. This field is updated by the DSI Protocol logic whenever a packet header is detected with the lower 4 bits of the DTYPE in the range of 0xB to 0xE.
5-0	DSI_DTYPE	R	0h	DSI Data Type This field returns the Data Type for the most recently received pixel stream packet. This field is updated by the DSI Protocol logic whenever a packet header is detected with the lower 4 bits of the DTYPE in the range of 0xB to 0xE.

8.6.2.23 DSI_ERR_RPT_0 Register (Offset = 2Bh) [reset = 0h]

DSI_ERR_RPT_0 is described in Table 145.

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Table 145. DSI_ERR_RPT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DSI_PROT_ERR	R	0h	DSI Protocol errors on dsi_err status
6	RESERVED	R	0h	Reserved
5	DSI_INV_LEN_ERR	R	0h	Invalid Length errors on dsi_err status

Table 145. DSI_ERR_RPT_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DSI_INV_VC_ERR	R	0h	Invalid VC errors on dsi_err status
3	DSI_INV_DT_ERR	R	0h	Invalid DT errors on dsi_err status
2	DSI_CHKSUM_ERR	R	0h	16-bit CRC Checksum errors on dsi_err status
1	DSI_ECC_MULTI_ERR	R	0h	Multi-bit ECC errors on dsi_err status
0	DSI_ECC_SINGLE_ERR	R	0h	Single-bit ECC errors on dsi_err status

8.6.2.24 DSI_ERR_RPT_1 Register (Offset = 2Ch) [reset = 0h]

DSI_ERR_RPT_1 is described in Table 146.

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Table 146. DSI_ERR_RPT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	DSI_CTRL_ERR	R	0h	EOT Sync error on dsi_err status
5	DSI_HSRX_TO_ERR	R	0h	HS Receive timeout error on dsi_err status
4	DSI_LP_SYNC_ERR	R	0h	LP Sync error on dsi_err status
3	DSI_ESC_ENTRY_ERR	R	0h	Escape Entry error on dsi_err status
2	DSI_EOT_SYNC_ERR	R	0h	EOT Sync error on dsi_err status
1	DSI_SOT_SYNC_ERR	R	0h	SOT Sync error on dsi_err status
0	DSI_SOT_ERR	R	0h	SOT error on dsi_err status

8.6.2.25 DSI_ERR_RPT_2 Register (Offset = 2Dh) [reset = 0h]

DSI_ERR_RPT_2 is described in Table 147.

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Table 147. DSI_ERR_RPT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	CMD_FIFO_ OVERFLOW_ERR	R	0h	Command FIFO overflow error
1	EOT_WITHOUT_ EOT_PKT_ERR	R	0h	EOT without EOT packet error
0	READ_WITHOUT_ BTA_ERR	R	0h	Read without Bit Turn-Around error

8.6.2.26 DSI_HSW_CFG_HI Register (Offset = 30h) [reset = 0h]

DSI_HSW_CFG_HI is described in Table 148.

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Table 148. DSI_HSW_CFG_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	DSI_HSYNC_WIDTH_HI	R/W	0h	Hsync Pulse Width When DSI Sync Events are enabled (DSI_CONFIG_0:DSI_SYNC_PULSES = 0), this field configures the width, in pixel clocks, of the generated Hsync pulse This register contains bits 9:8 of DSI_HSYNC_WIDTH

8.6.2.27 DSI_HSW_CFG_LO Register (Offset = 31h) [reset = 20h]

DSI_HSW_CFG_LO is described in Table 149.

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Table 149. DSI_HSW_CFG_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DSI_HSYNC_WIDTH_LO	R/W	20h	Hsync Pulse Width When DSI Sync Events are enabled (DSI_CONFIG_0:DSI_SYNC_PULSES = 0), this field configures the width, in pixel clocks, of the generated Hsync pulse This register contains bits 7:0 of DSI_HSYNC_WIDTH

8.6.2.28 DSI_VSW_CFG_HI Register (Offset = 32h) [reset = 0h]

DSI_VSW_CFG_HI is described in Table 150.

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Table 150. DSI_VSW_CFG_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	DSI_VSYNC_WIDTH_HI	R/W	0h	Vsync Pulse Width When DSI Sync Events are enabled (DSI_CONFIG_0:DSI_SYNC_PULSES = 0), this field configures the width, in lines (that is, the number of Hsync pulses), of the generated Vsync pulse This register contains bits 9:8 of DSI_VSYNC_WIDTH

8.6.2.29 DSI_VSW_CFG_LO Register (Offset = 33h) [reset = 4h]

DSI_VSW_CFG_LO is described in Table 151.

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Table 151. DSI_VSW_CFG_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DSI_VSYNC_WIDTH_LO	R/W	4h	Vsync Pulse Width When DSI Sync Events are enabled (DSI_CONFIG_0:DSI_SYNC_PULSES = 0), this field configures the width, in lines (that is, the number of Hsync pulses), of the generated Vsync pulse This register contains bits 7:0 of DSI_VSYNC_WIDTH

8.6.2.30 DSI_SYNC_DLY_CFG_HI Register (Offset = 34h) [reset = 0h]

DSI_SYNC_DLY_CFG_HI is described in Table 152.

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Table 152. DSI_SYNC_DLY_CFG_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	DSI_SYNC_DELAY_HI	R/W	0h	Sync Delay This 10-bit field configures the delay, in pixel clocks, from the detection of Hsync or Vsync in the DSI protocol logic, to the output of the DSI-to-FPD-Link III FIFO, and as such, sets the depth of the FIFO between the domains. This register contains bits 9:8 of DSI_SYNC_DELAY The maximum value of DSI_SYNC_DELAY is 766 (0x2FE)

8.6.2.31 DSI_SYNC_DLY_CFG_LO Register (Offset = 35h) [reset = 20h]

DSI_SYNC_DLY_CFG_LO is described in Table 153.

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Table 153. DSI_SYNC_DLY_CFG_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DSI_SYNC_DELAY_LO	R/W	20h	Sync Delay This 10-bit field configures the delay, in pixel clocks, from the detection of Hsync or Vsync in the DSI protocol logic, to the output of the DSI-to-FPD-Link III FIFO, and as such, sets the depth of the FIFO between the domains. This register contains bits 7:0 of DSI_SYNC_DELAY The maximum value of DSI_SYNC_DELAY is 766 (0x2FE)

8.6.2.32 DSI_EN_HSRX Register (Offset = 36h) [reset = 0h]

DSI_EN_HSRX is described in Table 154.

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Table 154. DSI_EN_HSRX Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	EN_HSRX_OV	R/W	0h	Overwrite to enable CSI RX HS receiver
5	RESERVED	R/W	0h	Reserved
4	EN_HSRX_CLK0	R/W	0h	Enable HSRX CLK0
3	EN_HSRX_D3	R/W	0h	Enable HSRX D3
2	EN_HSRX_D2	R/W	0h	Enable HSRX D2
1	EN_HSRX_D1	R/W	0h	Enable HSRX D1
0	EN_HSRX_D0	R/W	0h	Enable HSRX D0

8.6.2.33 DSI_EN_LPRX Register (Offset = 37h) [reset = 0h]

DSI_EN_LPRX is described in Table 155.

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Table 155. DSI_EN_LPRX Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	EN_LPRX_OV	R/W	0h	Overwrite CSI LP Receiver
5	RESERVED	R	0h	Reserved
4	EN_LPRX_CLK0	R/W	0h	Enable LP Receiver for CLK0
3	EN_LPRX_D3	R/W	0h	Enable LP Receiver for D3
2	EN_LPRX_D2	R/W	0h	Enable LP Receiver for D2
1	EN_LPRX_D1	R/W	0h	Enable LP Receiver for D1
0	EN_LPRX_D0	R/W	0h	Enable LP Receiver for D0

8.6.2.34 DSI_EN_RXTERM Register (Offset = 38h) [reset = 0h]

DSI_EN_RXTERM is described in Table 156.

Return to Summary Table.

Table 156. DSI_EN_RXTERM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	EN_RXTERM_OV	R/W	0h	Overwrite CSI RX HS Termination
5	RESERVED	R	0h	Reserved
4	EN_RXTERM_CLK0	R/W	0h	Enable RX Termination for CSI CLK0
3	EN_RXTERM_D3	R/W	0h	Enable RX Termination for CSI D3
2	EN_RXTERM_D2	R/W	0h	Enable RX Termination for CSI D2
1	EN_RXTERM_D1	R/W	0h	Enable RX Termination for CSI D1
0	EN_RXTERM_D0	R/W	0h	Enable RX Termination for CSI D1

8.6.2.35 DSI_PCLK_DIV_M Register (Offset = 3Ah) [reset = X]

DSI_PCLK_DIV_M is described in Table 157.

Return to Summary Table.

Table 157. DSI_PCLK_DIV_M Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_PCLK_DIV_OV	R/W	0h	Enable Override of DSI PCLK M/N divider When set to 1, the DSI_DIV_M and DSI_DIV_N register values will be used for the M/N divider used to generate the pixel clock from the DSI clock.
6-5	RESERVED	R	0h	Reserved
4-0	DSI_DIV_M	R/W	X	DSI Pclk divider M value This register controls the M setting for the M/N divider used to generate the pixel clock from the DSI input clock. Normally this value is based on the number of DSI lanes, the number of bytes per pixel, and the DSI input mode (single vs dual). If the EN_PCLK_DIV_OV is set to 0, this register returns the automatically determined M setting for the M/N divider. If EN_PCLK_DIV_OV is set to 1, this register value is used as the M setting for the M/N divider

8.6.2.36 DSI_PCLK_DIV_N Register (Offset = 3Bh) [reset = X]

DSI_PCLK_DIV_N is described in Table 158.

Return to Summary Table.

Table 158. DSI_PCLK_DIV_N Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DSI_DIV_N	R/W	X	DSI Pclk divider N value This register controls the N setting for the M/N divider used to generate the pixel clock from the DSI input clock. Normally, the M/N settings are based on the number of DSI lanes, the number of bytes per pixel, and the DSI input mode (single vs dual). If EN_PCLK_DIV_OV is set to 1, the DSI_DIV_M and DSI_DIV_N values are used. If the EN_PCLK_DIV_OV is set to 0, this register returns the automatically determined M setting for the M/N divider. If EN_PCLK_DIV_OV is set to 1, this register value is used as the M setting for the M/N divider

8.6.3 Port 0 and Port 1 Pattern Generator Indirect Registers

Table 159 summarizes the memory-mapped registers for the DS90UB941AS-Q1 pattern generator. All register offset addresses not listed in Table 159 should be considered as reserved locations and the register contents should not be modified.

Register access is provided through an indirect access mechanism through the Pattern Generator Indirect Access registers (PGIA and PGID). These registers are located at offsets 0x66 and 0x67 in the main register space.

The indirect address mechanism involves setting the register offset address and reading or writing the data register.

For writes, the process is as follows:

1. Write to the TX_PORT_SEL register to select the desired FPD-Link III Port
   - For selecting Port 0 set PORT0_SEL bit in the TX_PORT_SEL (0x1E) register (default)
   - For selecting Port 1 set PORT1_SEL bit in the TX_PORT_SEL (0x1E) register
2. Write to the PGIA register to set the register offset
3. Write the data value to the PGID register

For reads, the process is as follows:

1. Write to the TX_PORT_SEL register to select the desired FPD-Link III Port
   - For selecting Port 0 set PORT0_SEL bit in the TX_PORT_SEL (0x1E) register (default)
   - For selecting Port 1 set PORT1_SEL bit in the TX_PORT_SEL (0x1E) register
2. Write to the PGIA register to set the register offset
3. Read from the PGID register

Table 159. Pattern Generator Indirect Registers Summary

Offset	Acronym	Register Name	Section
0h	PGRS		Go
1h	PGGS		Go
2h	PGBS		Go
3h	PGCDC1		Go
4h	PGTFS1		Go
5h	PGTFS2		Go
6h	PCTFS3		Go
7h	PGAFS1		Go
8h	PGAFS2		Go
9h	PGAFS3		Go
Ah	PGHSW		Go
Bh	PGVSW		Go
Ch	PGHBP		Go
Dh	PGVBP		Go
Eh	PBSC		Go
Fh	PGFT		Go
10h	PGTSC		Go
11h	PGTSO1		Go
12h	PGTSO2		Go
13h	PGTSO3		Go
14h	PGTSO4		Go
15h	PGTSO5		Go
16h	PGTSO6		Go
17h	PGTSO7		Go

Table 159. Pattern Generator Indirect Registers Summary (continued)

Offset	Acronym	Register Name	Section
18h	PGTSO8		Go
19h	PGBE		Go
1Ah	PGCDC2		Go

Table 160 shows the codes that are used for access types in this section.

Table 160. Register Access Type Codes

Access Type	Code	Description
R	R	Read only access
R/W	R/W	Read / Write access
R/W/RC	R/W/RC	Read / Write access / Read to Clear

8.6.3.1 PGRS Register (Offset = 0h) [reset = 0h]

PGRS is described in Table 161.

Return to Summary Table.

Table 161. PGRS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_RSP	R/W	0h	Red Sub-Pixel: This field is the 8-bit Red sub-pixel for the custom color

8.6.3.2 PGGS Register (Offset = 1h) [reset = 0h]

PGGS is described in Table 162.

Return to Summary Table.

Table 162. PGGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_GSP	R/W	0h	Green Sub-Pixel: This field is the 8-bit Green sub-pixel for the custom color

8.6.3.3 PGBS Register (Offset = 2h) [reset = 0h]

PGBS is described in Table 163.

Return to Summary Table.

Table 163. PGBS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_BSP	R/W	0h	Blue Sub-Pixel: This field is the 8-bit Blue sub-pixel for the custom color

8.6.3.4 PGCDC1 Register (Offset = 3h) [reset = 8h]

PGCDC1 is described in Table 164.

Return to Summary Table.

Table 164. PGCDC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved

Table 164. PGCDC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PATGEN_CDIV_N	R/W	8h	Clock Divider: This field configures the clock divider for the internally generated pixel clock. If PGCDC2:PGEN_CDIV_M is 1, the internal pixel clock frequency is nominally (200/N) MHz. If PGCDC2:PGEN_CDIV_M is greater than 1, the internal pixel clock frequency is nominally (800*M/N) MHz.

8.6.3.5 PGTFS1 Register (Offset = 4h) [reset = 48h]

PGTFS1 is described in Table 165.

Return to Summary Table.

Table 165. PGTFS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_THW_7:0	R/W	48h	Total Horizontal Width: This field is the 8 least significant bits of the 12-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.3.6 PGTFS2 Register (Offset = 5h) [reset = 53h]

PGTFS2 is described in Table 166.

Return to Summary Table.

Table 166. PGTFS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TVW_3:0	R/W	5h	Total Vertical Width: This field is the 4 least significant bits of the 12-bit Total Vertical Wdith of the frame, in units of lines. This field should only be written when the pattern generator is disabled
3-0	PATGEN_THW_11:8	R/W	3h	Total Horizontal Width: This field is the 4 most significant bits of the 12-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.3.7 PCTFS3 Register (Offset = 6h) [reset = 1Eh]

PCTFS3 is described in Table 167.

Return to Summary Table.

Table 167. PCTFS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_TVW_11:4	R/W	1Eh	Total Vertical Width: This field is the 8 most significant bits of the 12-bit Total Vertical Wdith of the frame, in units of lines. This field should only be written when the pattern generator is disabled

8.6.3.8 PGAFS1 Register (Offset = 7h) [reset = 20h]

PGAFS1 is described in Table 168.

Return to Summary Table.

Table 168. PGAFS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_AHW_7:0	R/W	20h	Active Horizontal Width: This field is the 8 least significant bits of the 12-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.3.9 PGAFS2 Register (Offset = 8h) [reset = 3h]

PGAFS2 is described in Table 169.

Return to Summary Table.

Table 169. PGAFS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_AVW_3:0	R/W	0h	Active Vertical Width: This field is the 4 least significant bits of the 12-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.
3-0	PATGEN_AHW_11:8	R/W	3h	Active Horizontal Width: This field is the 4 most significant bits of the 12-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.3.10 PGAFS3 Register (Offset = 9h) [reset = 1Eh]

PGAFS3 is described in Table 170.

Return to Summary Table.

Table 170. PGAFS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_AVW_11:4	R/W	1Eh	Active Vertical Width: This field is the 8 most significant bits of the 12-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.3.11 PGHSW Register (Offset = Ah) [reset = Ah]

PGHSW is described in Table 171.

Return to Summary Table.

Table 171. PGHSW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_HSW	R/W	Ah	Horizontal Sync Width: This field controls the width of the Horizontal Sync pulse, in units of pixels. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

8.6.3.12 PGVSW Register (Offset = Bh) [reset = 2h]

PGVSW is described in Table 172.

Return to Summary Table.

Table 172. PGVSW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_VSW	R/W	2h	Vertical Sync Width: This field controls the width of the Vertical Sync pulse, in units of lines. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

8.6.3.13 PGHBP Register (Offset = Ch) [reset = Ah]

PGHBP is described in Table 173.

Return to Summary Table.

Table 173. PGHBP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_HBP	R/W	Ah	Horizontal Back Porch Width: This field controls the width of the Horizontal Back Porch, in units of pixels. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

8.6.3.14 PGVBP Register (Offset = Dh) [reset = 2h]

PGVBP is described in Table 174.

Return to Summary Table.

Table 174. PGVBP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_VBP	R/W	2h	Vertical back Porch Width: This field controls the width of the Vertical Back Porch, in units of lines. Valid values are 1-255. This field should only be written when the pattern generator is disabled.

8.6.3.15 PBSC Register (Offset = Eh) [reset = 3h]

PBSC is described in Table 175.

Return to Summary Table.

Table 175. PBSC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	PATGEN_HS_DIS	R/W	0h	Horizontal Sync Disable: Disable Horizontal Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
1	PATGEN_VS_POL	R/W	1h	Vertical Sync Polarity: When 1, the pattern generator will invert the Vertical Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.

Table 175. PBSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PATGEN_HS_POL	R/W	1h	Horizontal Sync Polarity: When 1, the pattern generator will invert the Horizontal Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled

8.6.3.16 PGFT Register (Offset = Fh) [reset = 1Eh]

PGFT is described in Table 176.

Return to Summary Table.

Table 176. PGFT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_FTIME	R/W	1Eh	Frame Time: When Auto-Scrolling is enabled, this field controls the number of frames to display each pattern in increments of two frames. Valid register values are 1-255, giving a programmable range of even numbers between 2 and 510, inclusive.

8.6.3.17 PGTSC Register (Offset = 10h) [reset = Ch]

PGTSC is described in Table 177.

Return to Summary Table.

Table 177. PGTSC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	PATGEN_TSLOT	R/W	Ch	Time Slots: This field configures the number of enabled time slots for Auto-Scrolling. Valid Values are 1-16

8.6.3.18 PGTSO1 Register (Offset = 11h) [reset = 21h]

PGTSO1 is described in Table 178.

Return to Summary Table.

Table 178. PGTSO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS2	R/W	2h	Time Slot 2 Pattern: This field configures the pattern enabled in Time Slot 2. Valid values are 0-15
3-0	PATGEN_TS1	R/W	1h	Time Slot 1 Pattern: This field configures the pattern enabled in Time Slot 1. Valid values are 0-15

8.6.3.19 PGTSO2 Register (Offset = 12h) [reset = 43h]

PGTSO2 is described in Table 179.

Return to Summary Table.

Table 179. PGTSO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS4	R/W	4h	Time Slot 4 Pattern: This field configures the pattern enabled in Time Slot 4. Valid values are 0-15
3-0	PATGEN_TS3	R/W	3h	Time Slot 3 Pattern: This field configures the pattern enabled in Time Slot 3. Valid values are 0-15

8.6.3.20 PGTSO3 Register (Offset = 13h) [reset = 65h]

PGTSO3 is described in Table 180.

Return to Summary Table.

Table 180. PGTSO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS6	R/W	6h	Time Slot 6 Pattern: This field configures the pattern enabled in Time Slot 6. Valid values are 0-15
3-0	PATGEN_TS5	R/W	5h	Time Slot 5 Pattern: This field configures the pattern enabled in Time Slot 5. Valid values are 0-15

8.6.3.21 PGTSO4 Register (Offset = 14h) [reset = 87h]

PGTSO4 is described in Table 181.

Return to Summary Table.

Table 181. PGTSO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS8	R/W	8h	Time Slot 8 Pattern: This field configures the pattern enabled in Time Slot 8. Valid values are 0-15
3-0	PATGEN_TS7	R/W	7h	Time Slot 7 Pattern: This field configures the pattern enabled in Time Slot 7. Valid values are 0-15

8.6.3.22 PGTSO5 Register (Offset = 15h) [reset = A9h]

PGTSO5 is described in Table 182.

Return to Summary Table.

Table 182. PGTSO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS10	R/W	Ah	Time Slot 10 Pattern: This field configures the pattern enabled in Time Slot 10. Valid values are 0-15
3-0	PATGEN_TS9	R/W	9h	Time Slot 9 Pattern: This field configures the pattern enabled in Time Slot 9. Valid values are 0-15

8.6.3.23 PGTSO6 Register (Offset = 16h) [reset = CBh]

PGTSO6 is described in Table 183.

Return to Summary Table.

Table 183. PGTSO6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS12	R/W	Ch	Time Slot 12 Pattern: This field configures the pattern enabled in Time Slot 12. Valid values are 0-15
3-0	PATGEN_TS11	R/W	Bh	Time Slot 11 Pattern: This field configures the pattern enabled in Time Slot 11. Valid values are 0-15

8.6.3.24 PGTSO7 Register (Offset = 17h) [reset = EDh]

PGTSO7 is described in Table 184.

Return to Summary Table.

Table 184. PGTSO7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS14	R/W	Eh	Time Slot 14 Pattern: This field configures the pattern enabled in Time Slot 14. Valid values are 0-15
3-0	PATGEN_TS13	R/W	Dh	Time Slot 13 Pattern: This field configures the pattern enabled in Time Slot 13. Valid values are 0-15

8.6.3.25 PGTSO8 Register (Offset = 18h) [reset = Fh]

PGTSO8 is described in Table 185.

Return to Summary Table.

Table 185. PGTSO8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_TS16	R/W	0h	Time Slot 16 Pattern: This field configures the pattern enabled in Time Slot 16. Valid values are 0-15
3-0	PATGEN_TS15	R/W	Fh	Time Slot 15 Pattern: This field configures the pattern enabled in Time Slot 15. Valid values are 0-15

8.6.3.26 PGBE Register (Offset = 19h) [reset = 0h]

PGBE is described in Table 186.

Return to Summary Table.

Table 186. PGBE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_BIST_ERRS	R	0h	Clear on read

8.6.3.27 PGCDC2 Register (Offset = 1Ah) [reset = 1h]

PGCDC2 is described in Table 187.

Return to Summary Table.

Table 187. PGCDC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4-0	PATGEN_CDIV_M	R/W	1h	Clock Divider: This field configures the clock divider for the internally generated pixel clock. If PGCDC2:PGEN_CDIV_M is 1, the internal pixel clock frequency is nominally (200/N) MHz. If PGCDC2:PGEN_CDIV_M is greater than 1, the internal pixel clock frequency is nominally (800*M/N) MHz.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UB941AS-Q1, in conjunction with the DS90UB940N-Q1 or DS90UB948-Q1 deserializer, is intended to interface between a host (graphics processor) and a display, supporting 24-bit color depth (RGB888) and high-definition (1080p) digital video format. It can receive an 8-bit RGB stream with a pixel clock rate up to 210 MHz together with four I2S audio streams. The DS90UB941AS-Q1 can support up to 170MHz pixel clock when paired with DS90UB940N-Q1 , and up to 192MHz pixel clock when paired with a DS90UB948-Q1.

9.2 Typical Application

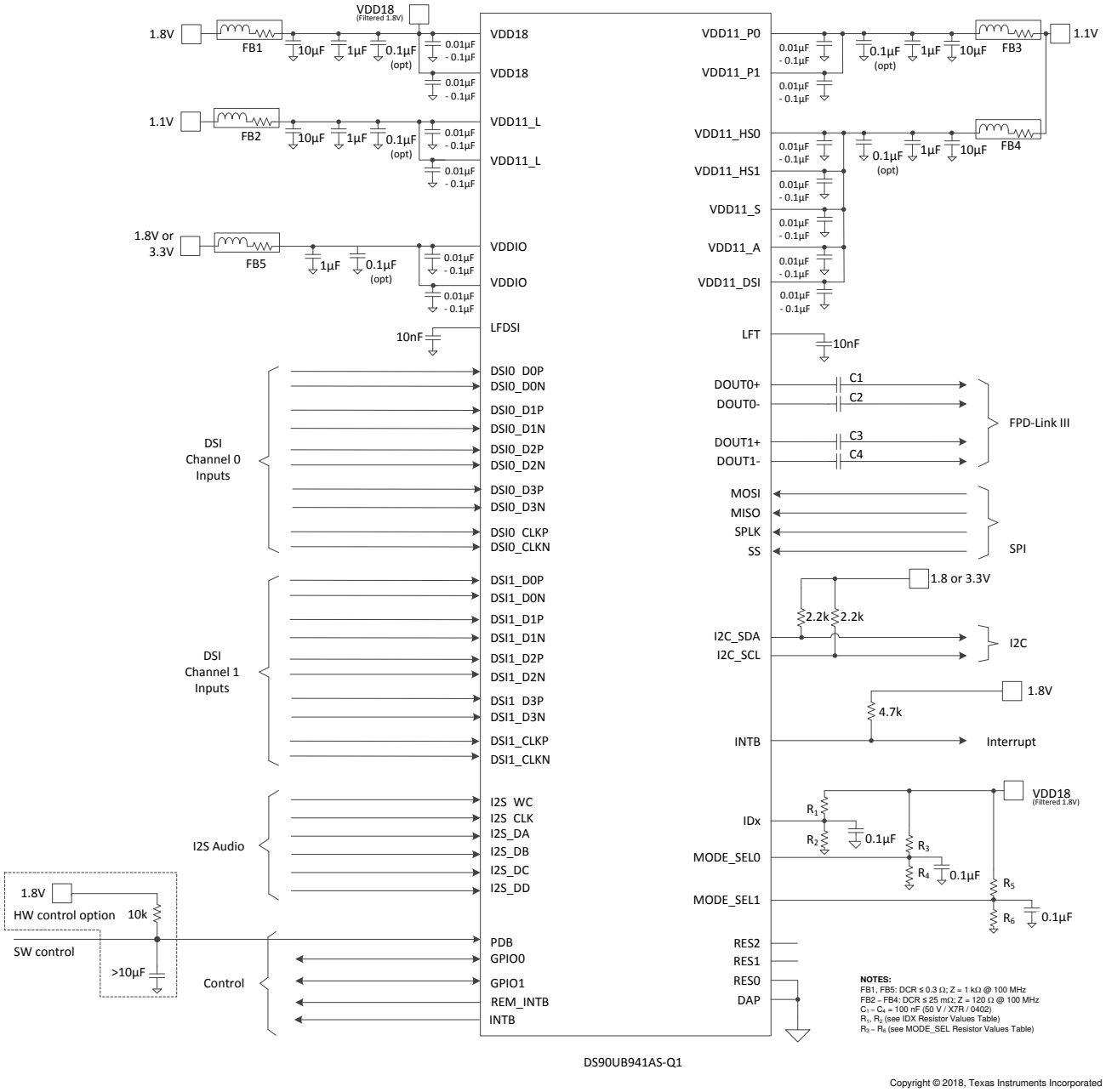


图 39. Typical Connection Diagram - STP

Typical Application（接下页）

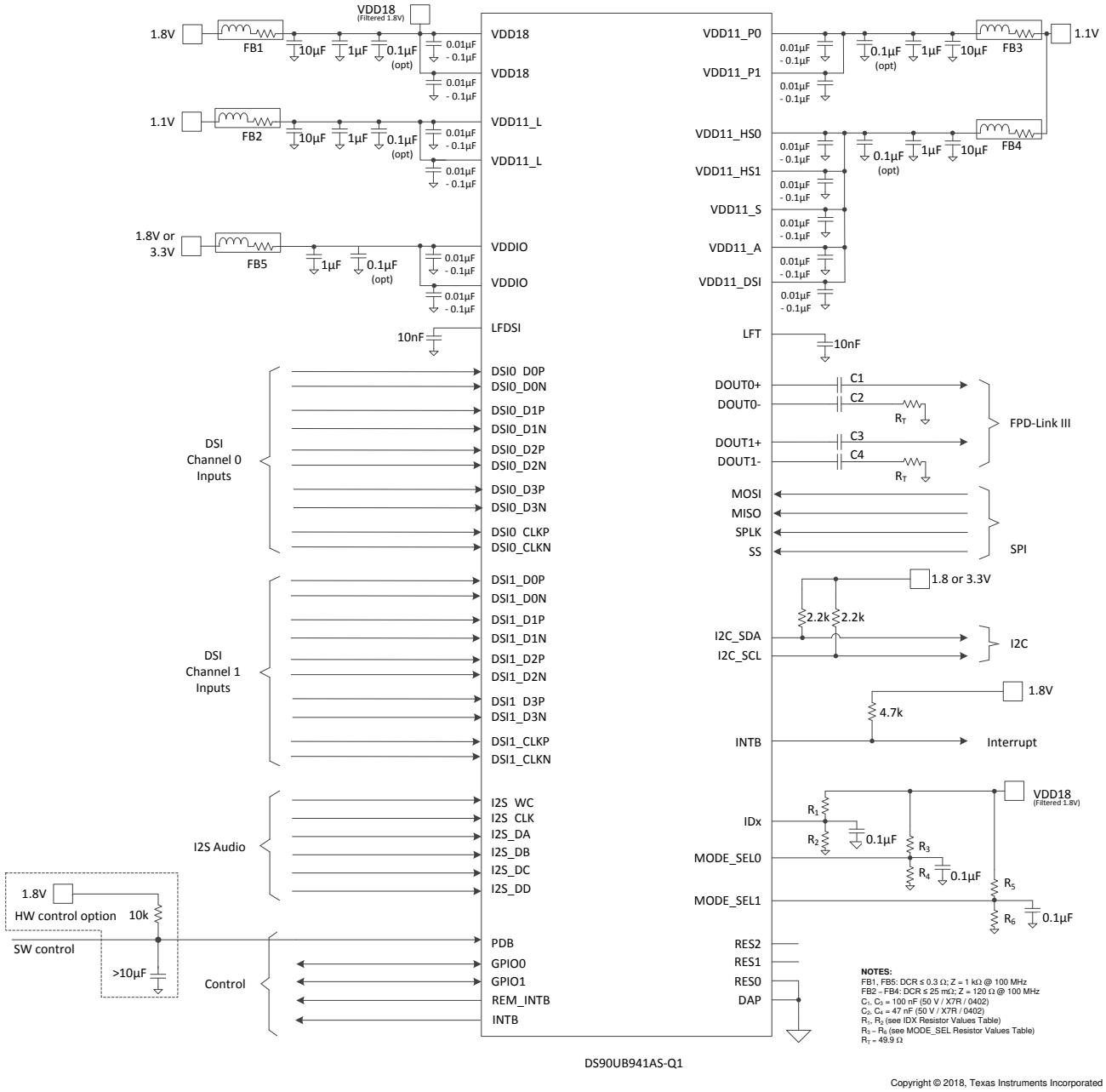


图 40. Typical Connection Diagram - Coaxial

Typical Application (接下页)

9.2.1 Design Requirements

The FPD-Link III interface supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in 图 41 and 图 42.

表 188. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V
AC Coupling Capacitor for STP: DOUT0± and DOUT1±	100 nF (50V / X7R / 0402)
AC Coupling Capacitor for Coaxial: DOUT0+ and DOUT1+	100 nF (50V / X7R / 0402)
AC Coupling Capacitor for Coaxial: DOUT0- and DOUT1-	47 nF (50V / X7R / 0402)

For applications using single-ended, 50 Ω coaxial cables, terminate the unused data pins (DOUT0-, DOUT1-) with an AC-coupling capacitor and a 50 Ω resistor.

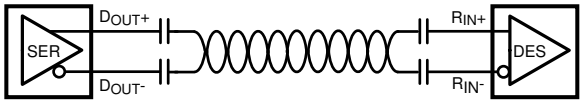


图 41. AC-Coupled Connection (STP)

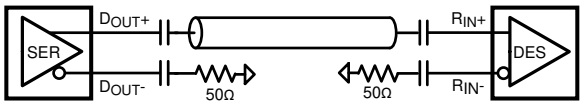


图 42. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC-coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

9.2.2 Detailed Design Procedure

9.2.2.1 High-Speed Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *AN-905 Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100 Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the *LVDS Owner's Manual* (SNLA187) on ti.com.

9.2.3 Application Curves

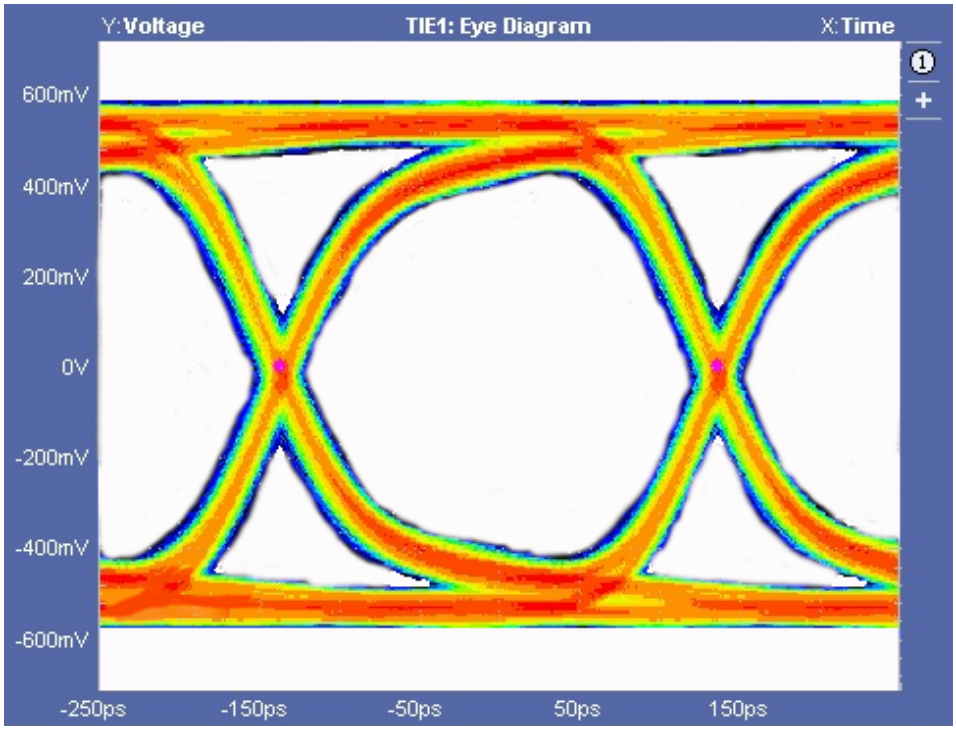


图 43. Serializer Output at 3.675Gbps, Dual FPD-Link 210 Mhz PCLK

10 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The section provides guidance on which circuit blocks are connected to which power pins. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

10.1 VDD Power Supply

Each VDD power supply pin must have a 10 nF (or 100 nF) capacitor to ground connected as close as possible to the DS90UB941AS-Q1 device. TI recommends having additional decoupling capacitors (1 µF and 10 µF) and the pins connected to a solid power plane.

10.2 Power-Up and Initialization

There are two recommended power up sequences that can be used for the DS90UB941AS-Q1.

Sequence A:

1. Apply V_{DDIO} and V_{DD18}
   - If 1.8 V V_{DDIO} option is selected, V_{DDIO} and V_{DD18} need to be supplied from the same power source.
   - If 3.3 V V_{DDIO} option is selected, power to the V_{DDIO} may be applied before or after V_{DD18}.
2. V_{DD11}
3. Wait until all supplies have settled
4. Apply Pixel clock (either DSI clock or REFCLK(s))
5. Wait for the Pixel clock to stabilize within 0.5% of the target frequency
6. Assert PDB
7. Apply DSI inputs
8. Initialize the device

See 图 45.

The initialization sequence 941AS Init shown in 图 45 consists of any user-defined device configurations and the following:

1. If the device is powered up with the DSI inputs enabled (MODE_SEL1 strap option), disable the DSI inputs by setting DISABLE_DSI 0x01[3]=1 in the RESET_CTL register.
2. Insert any user defined device configurations here.
3. Set TSKIP_CNT field in DSI Indirect Register 0x05 based on the operating DSI clock frequency. See *THS-SKIP Programming* for more information.
4. Enable the DSI inputs by setting DISABLE_DSI 0x01[3]=0 in the RESET_CTL register.

Sequence B:

1. Apply V_{DDIO} and V_{DD18}
   - If 1.8 V V_{DDIO} option is selected, V_{DDIO} and V_{DD18} need to be supplied from the same power source.
   - If 3.3 V V_{DDIO} option is selected, power to the V_{DDIO} may be applied before or after V_{DD18}.
2. V_{DD11}
3. Wait until all supplies have settled
4. Assert PDB
5. Apply Pixel clock (either DSI clock or REFCLK(s))
6. Apply DSI inputs
7. Wait for the Pixel clock to stabilize within 0.5% of the target frequency
8. Initialize the device

See 图 46.

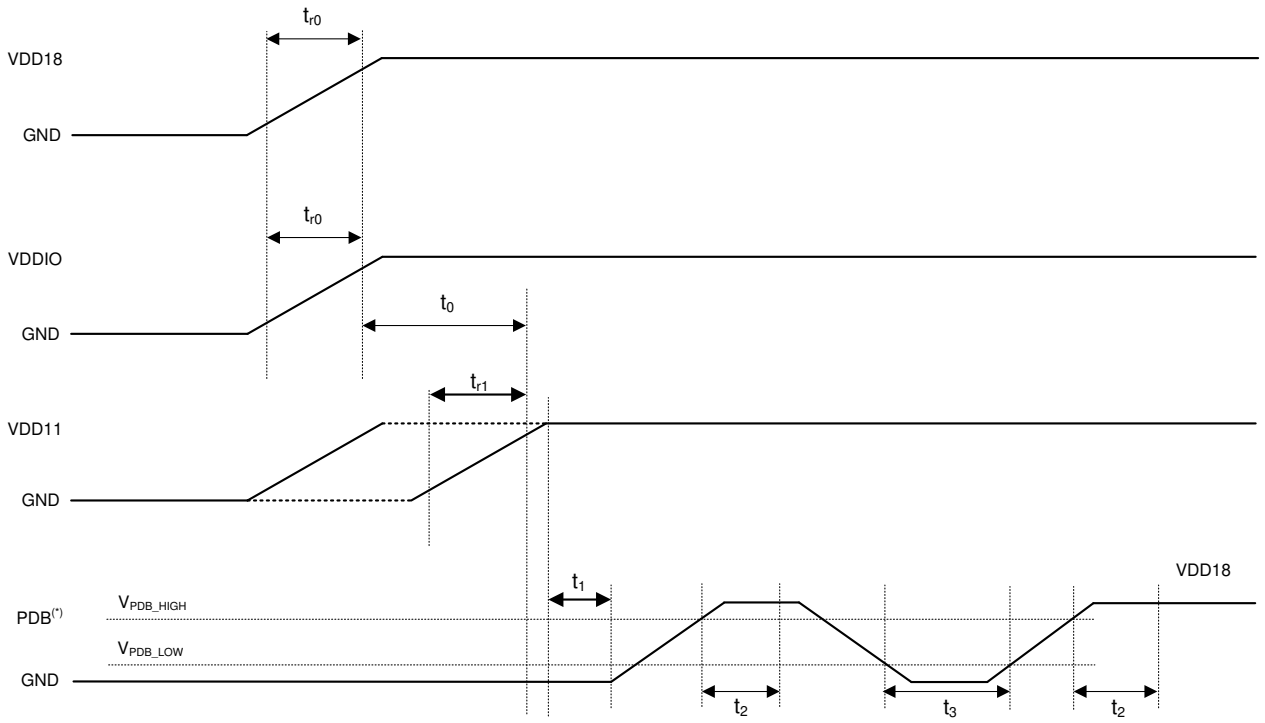
Power-Up and Initialization (接下页)

The initialization sequence 941AS Init shown in 图 45 consists of any user-defined device configurations and the following:

1. Reset the device by setting DIGITAL_RESET1 0x01[1]=1 in the RESET_CTL register.
2. If the device is powered up with the DSI inputs enabled (MODE_SEL1 strap option), disable the DSI inputs by setting DISABLE_DSI 0x01[3]=1 in the RESET_CTL register.
3. Insert any user defined device configurations here.
4. Set TSKIP_CNT field in DSI Indirect Register 0x05 based on the operating DSI clock frequency. See *THS-SKIP Programming* for more information.
5. Enable the DSI inputs by setting DISABLE_DSI 0x01[3]=0 in the RESET_CTL register.

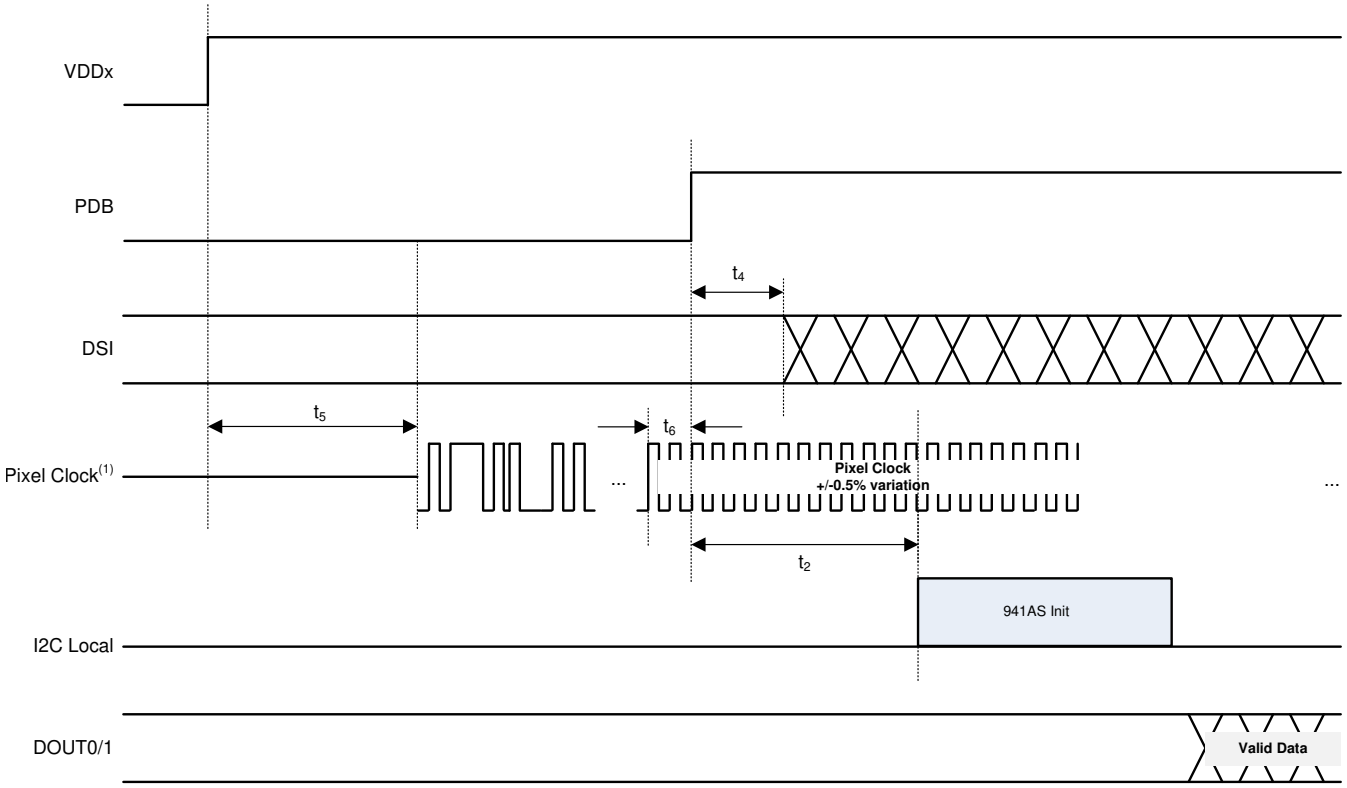
表 189. Timing Diagram for the Power-Up and Initialization Sequences

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
t_{r0}	VDD18 / VDDIO rise time	0.2			ms	@10/90%
t_{r1}	VDD11 rise time	0.05			ms	@10/90%
t_0	VDD18 / VDDIO to VDD11 delay	0			ms	
t_1	VDDx to PDB delay	0			ms	Release PDB after all supplies are up and stable.
t_2	PDB to I2C ready (IDX and MODE valid) delay	2			ms	
t_3	PDB negative pulse width required for the device reset	2			ms	Hard reset
t_4	DSI delay time	0			ms	Apply DSI after PDB is released.
t_5	Pixel Clock delay time	0			ms	Apply Pixel clock (DSI Clock or REFCLK(s)) after all supplies are up. The clock may be applied independent of PDB state, however, if applied before PDB, then Sequence A should be followed, or else, sequence B should be followed.
t_6	Pixel Clock Stable to Initialization delay time	1			µs	Pixel clock (DSI Clock or REFCLK(s)) frequency must be within 0.5% of the target frequency and stable before device initialization (Sequence B) or PDB release (Sequence A).



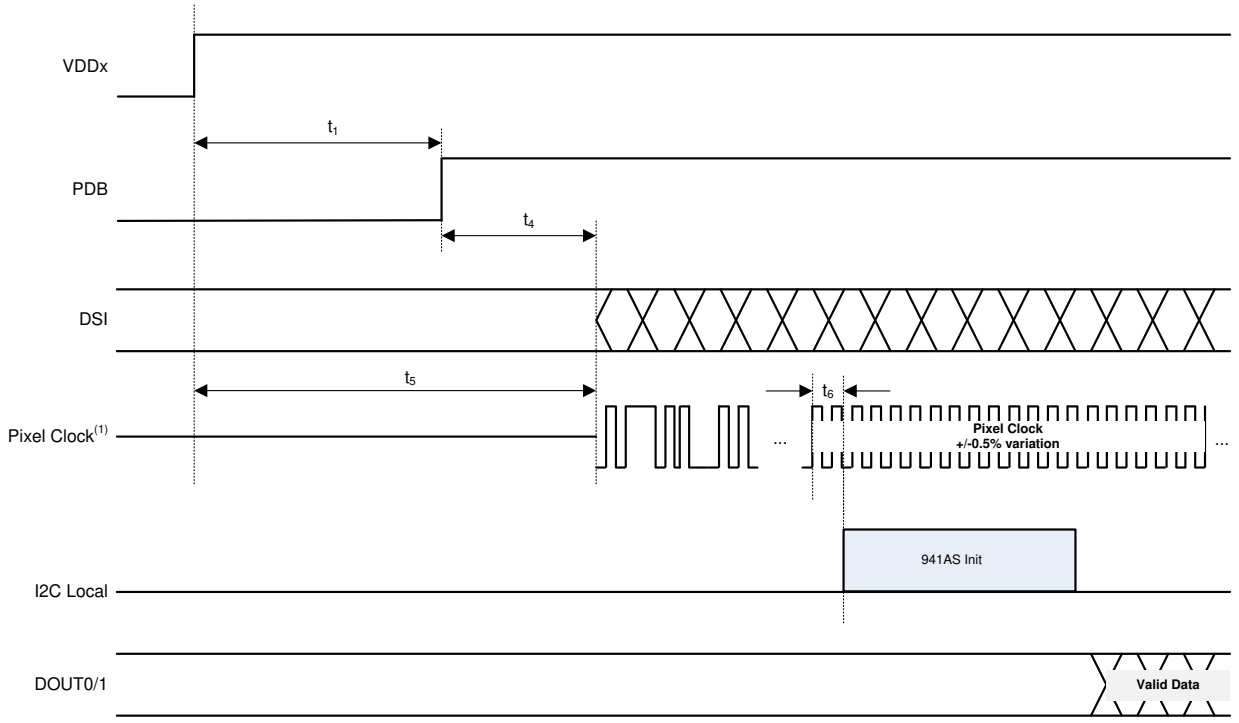
(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

图 44. Power-Up Sequence



(1) Pixel clock is a clock reference for the FPD-Link III transceiver. Depending on the mode of operation, the pixel clock may be derived from a DSI clock, an external clock source, or an internal clock reference.

图 45. Initialization Sequence A



(1) Pixel clock is a clock reference for the FPD-Link III transceiver. Depending on the mode of operation, the pixel clock may be derived from a DSI clock, an external clock source, or an internal clock reference.

图 46. Initialization Sequence B

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement uses the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μF to 0.1 μF. Tantalum capacitors may be in the 2.2 μF to 10 μF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

TI recommends surface mount capacitors due to their smaller parasitic properties. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 μF to 100 μF range and smooths low-frequency switching noise. TI recommends that the user connect the power and ground pins directly to the power and ground planes, and place a via on both ends of the bypass capacitors connected to the plane. Connecting the power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also common practice to use two vias from the power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate the switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. See the Pin Functions table in the *Pin Configuration and Functions* section for guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Place DSI signals away from the FPD-Link III lines to prevent coupling from the DSI lines to the FPD-Link III lines. A single-ended impedance of 50 Ω for coaxial interconnect and a differential impedance of 100 Ω are typically recommended for STP interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

11.1.1 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane.

Connect the thermal pad of the DS90UB941AS-Q1 to this plane with vias. At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. Information on the VQFN style package is provided in the TI *AN-1187 Leadless Leadframe Package (LLP)* application note (SNOA401).

11.1.2 Routing FPD-Link III Signal Traces

Routing the FPD-Link III signal traces between the DOUT± pins and the connector is one of the most critical pieces of a successful DS90UB941AS-Q1 PCB layout. 图 47 shows an example PCB layout of the DS90UB941AS-Q1 configured for interface to a companion deserializer module over a STQ cable. For additional PCB layout details of the example, check the DS90Ux941AS-Q1EVM User's Guide.

Layout Guidelines（接下页)

The following list provides essential recommendations for routing the FPD-Link III signal traces between the DS90UB941AS-Q1 TX pins (DOUT±) and the connector.

- The routing of the FPD-Link III traces may be all on the top layer or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors should be on the top layer and close to the DS90UB941AS-Q1 TX pins.
- Route the DOUT traces between the AC-coupling capacitor and the connector as a 100 Ω differential or 50 Ω single-ended micro-strips with tight impedance control (±10%). Calculate the proper width of the traces based on the PCB stack-up.
- If routing as 100 Ω, differential micro-strips, keep intra-pair length mismatch to < 5 mils.
- If routing as 50 Ω, single-ended micro-strips, route the DOUT+ traces with minimum coupling to the DOUT+ traces (S > 3W).
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the through-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.
- When choosing to implement a common mode choke for common mode noise reduction, minimize the effects of any mismatch.

11.1.3 Routing DSI Signal Traces

1. Route DSI signal pairs with controlled 100 Ω differential impedance (±20%) or 50 Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep intra-pair length mismatch to < 5 mils.
4. Keep inter-pair length mismatch to < 50 mils within a single DSI RX port. DSI RX Port 0 differential traces do not need to match DSI Port 1 differential traces.
5. Length matching should be near the location of mismatch.
6. Each pair should be separated at least by 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Keep the number of VIAS to a minimum. TI recommends keeping the VIA count to 2 or fewer.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane splits.
11. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

11.2 Layout Example

图 47 PCB layout example is derived from the layout design of the DS90UB941AS-Q1EVM Evaluation Board. The graphic and layout description are used to determine proper routing when designing the Serializer board. The high-speed FPD-Link III traces are routed differentially to the connector. The traces are buried in an internal layer with a GND layer and power layer on each adjacent layer. Burying the traces helps reduce emissions, and it is important not to route other high-speed signals near these critical signal traces. The 100 Ω, differential characteristic impedance and 50 Ω, single-ended characteristic impedance traces are maintained as much as possible for both STP and coax applications. For layout of a coax board, 100 Ω coupled traces should be used with the DOUT- termination near to the connector.

图 47 shows the high-speed FPD-Link III traces close to the DOUT± pins. The AC-coupling capacitors and the common-mode choke are placed closely together so that the impedance discontinuity appears as tightly grouped as possible.

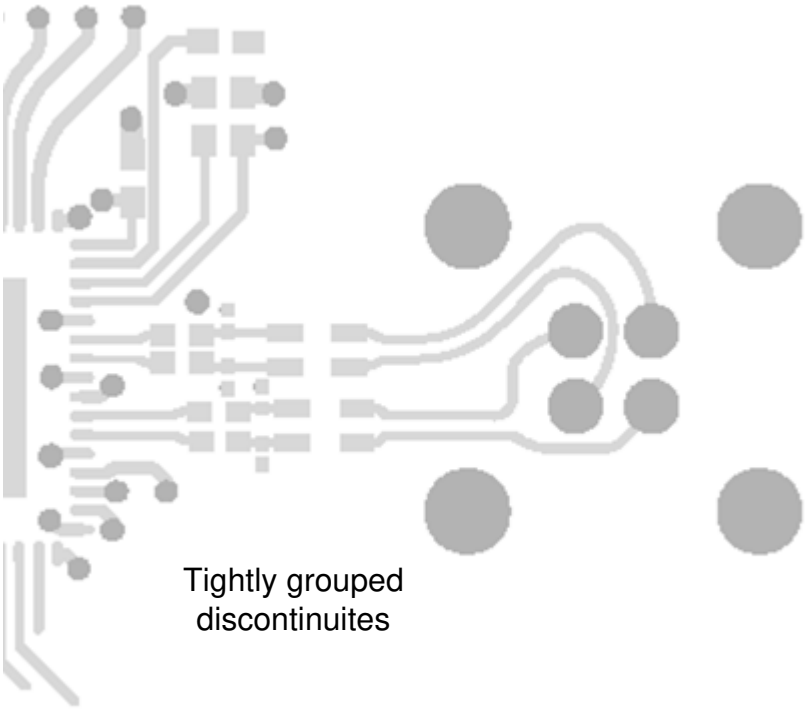


图 47. DS90UB941AS-Q1 Serializer Example Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《焊接规格应用报告》*，SNOA549
- *《IC 封装热指标应用报告》*，SPRA953
- *《通道链路 PCB 和互连设计指南》*，SNLA008
- *《传输线路 RAPIDESIGNER 操作和应用指南》*，SNLA035
- *《LVDS 用户手册》*，SNLA187
- *《通过具有双向控制通道的 FPD-Link III 进行 I2C 通信》*，SNLA131
- *《使用 DS90Ux92x FPD-Link III 器件的 I2S 音频接口》*，SNLA221
- *《探索 720p FPD-Link III 器件的内部测试图案生成特性》*，SNLA132
- *《I2C 总线上拉电阻器计算》*(SLVA689)
- FPD-Link 学习中心
- *《一种适用于 FPD-Link III SerDes 的 EMC/EMI 系统设计和测试方法》*(SLYT719)
- *《按照车用 EMC/EMI 要求进行成功设计的 10 个技巧》*(SLYT636)

12.2 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB941ASRTDRQ1	ACTIVE	VQFN	RTD	64	2000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UB941ASQ	Samples
DS90UB941ASRTDTQ1	ACTIVE	VQFN	RTD	64	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UB941ASQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

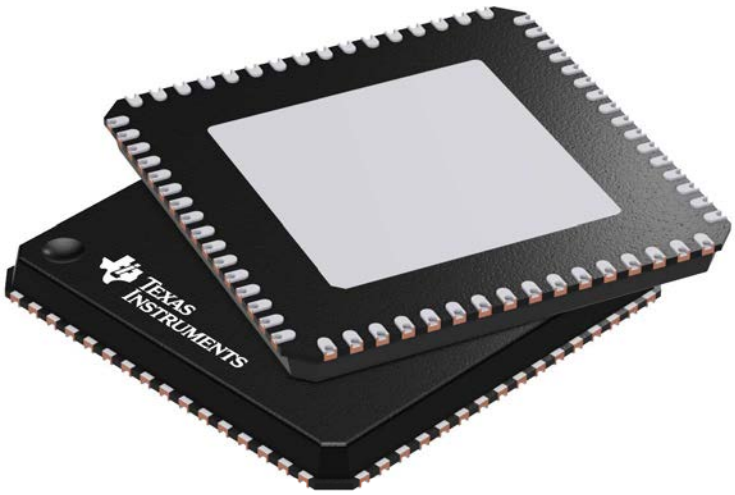
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

RTD 64 VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



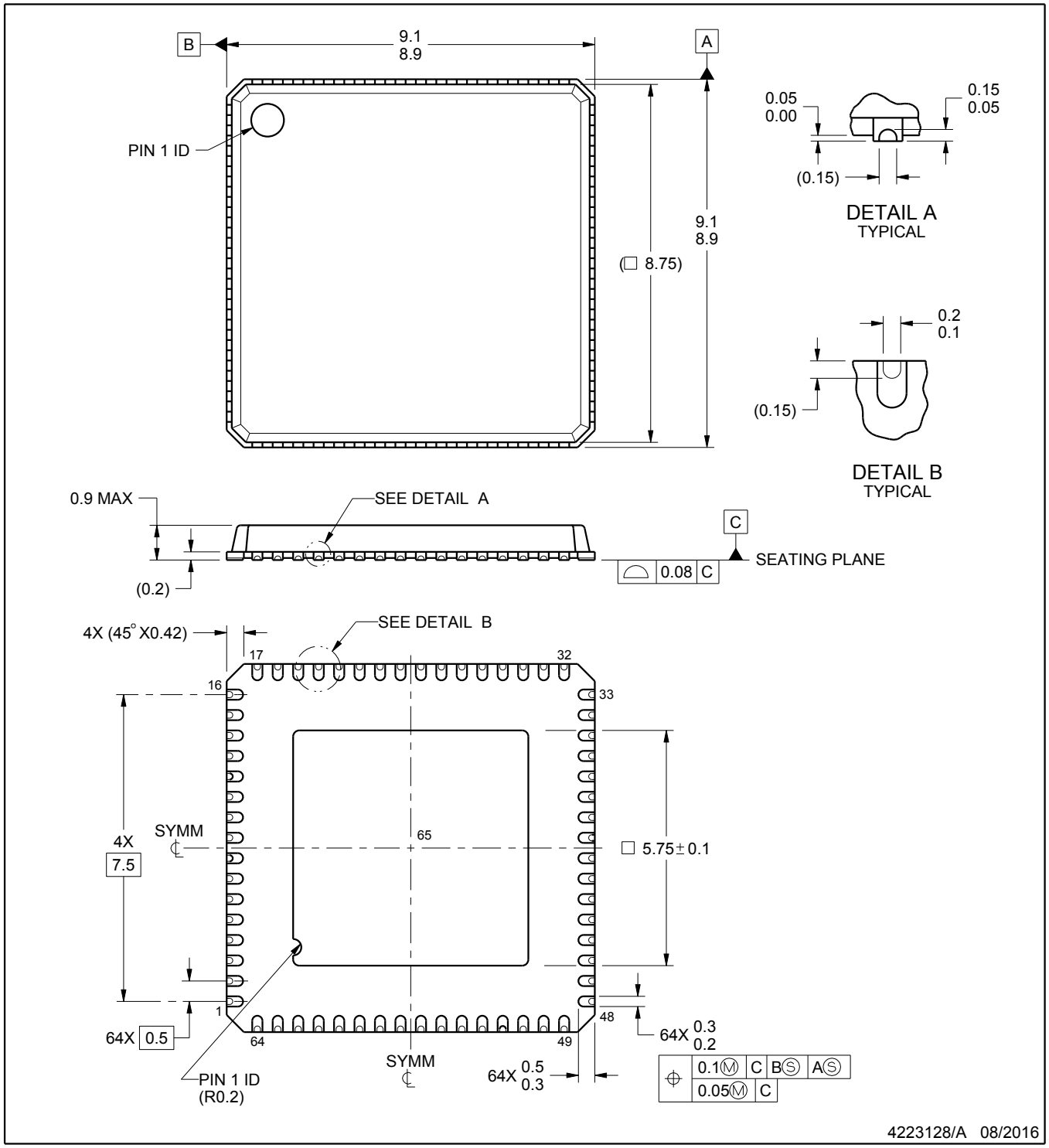
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RTD0064F

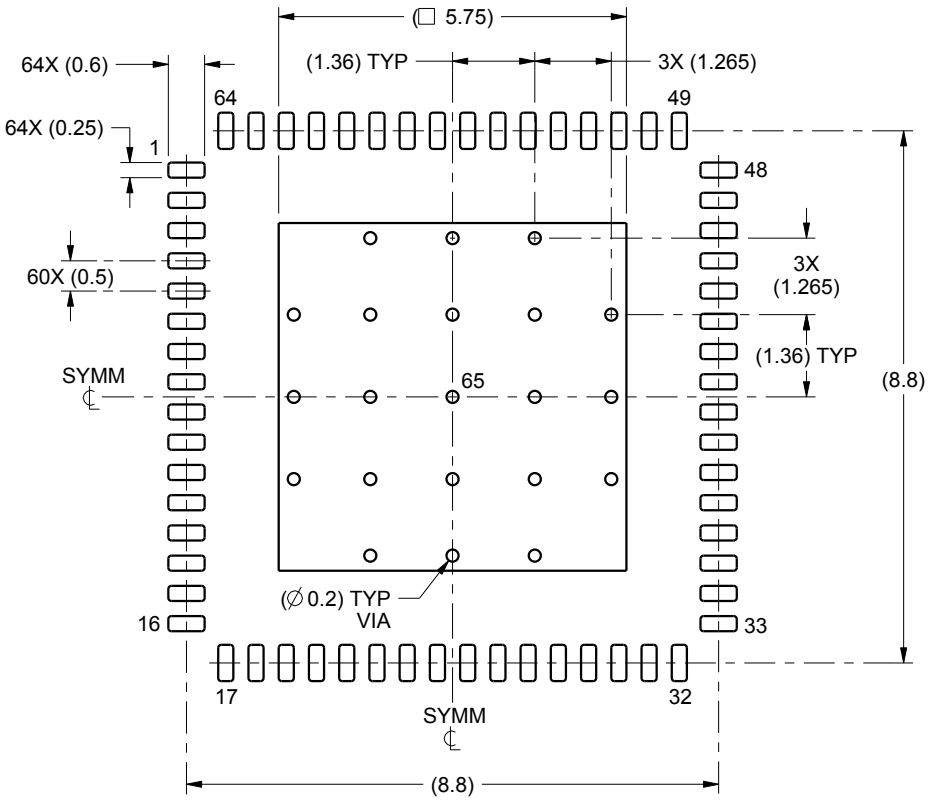
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

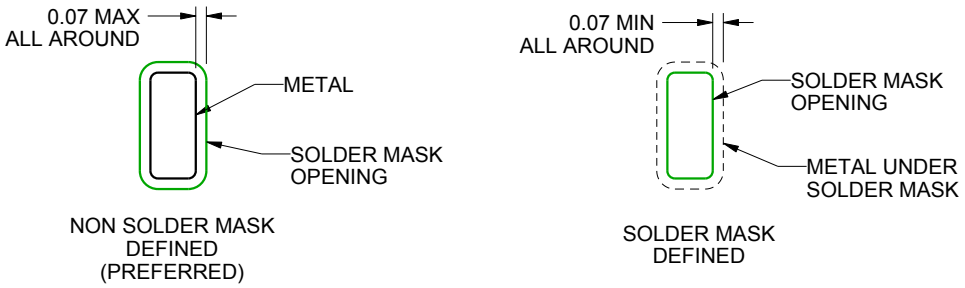


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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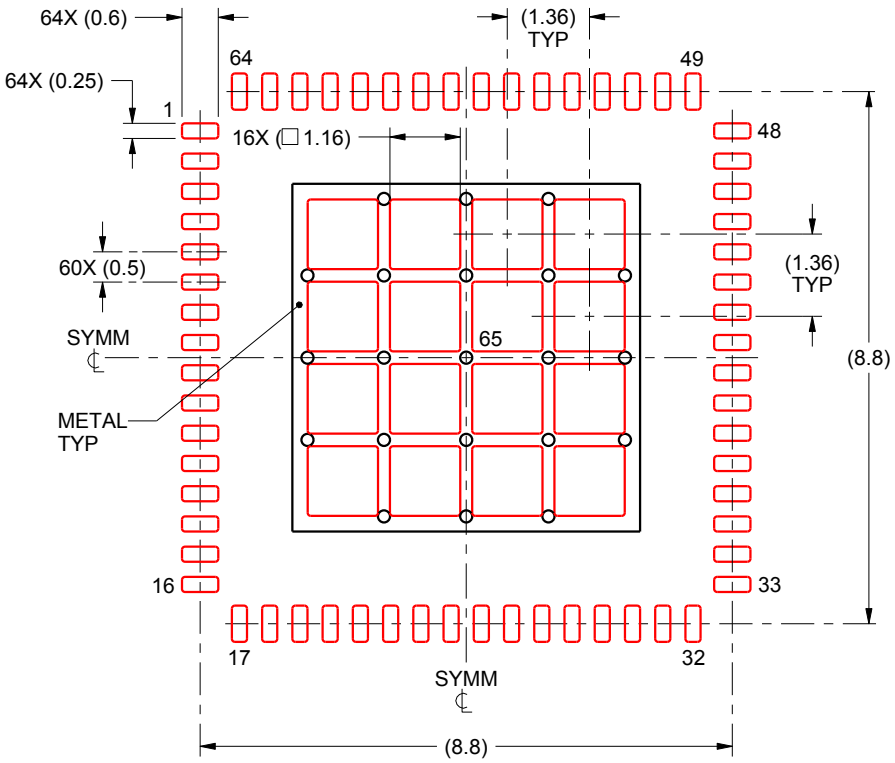
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

4223128/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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