

MSP430FR247x 混合信号微控制器

1 器件概述

1.1 特性

- 嵌入式微控制器
 - 16 位 RISC 架构
 - 支持的时钟频率最高可达 16MHz
 - 3.6V 至 1.8V 的宽电源电压范围（最低电源电压受限于 SVS 电平，请参阅 [SVS 规格](#)）
- 优化的超低功耗模式
 - 激活模式：135 μ A/MHz（典型值）
 - 待机：LPM3.5，采用 32768Hz 晶振的实时时钟 (RTC) 计数器：710nA（典型值）
 - 关断 (LPM4.5)：37nA，无 SVS
- 低功耗铁电 RAM (FRAM)
 - 容量高达 64KB 的非易失性存储器
 - 内置错误修正码 (ECC)
 - 可配置的写保护
 - 对程序、常量和存储的统一存储
 - 耐写次数达 10^{15} 次
 - 抗辐射和非磁性
- 智能数字外设
 - 四个 16 位计时器，每个计时器有 3 个捕捉/比较寄存器 (Timer_A3)
 - 一个 16 位计时器，具有 7 个捕捉/比较寄存器 (Timer_B7)
 - 一个仅用作计数器的 16 位 RTC
 - 16 位循环冗余校验 (CRC)
- 增强型串行通信，支持引脚重映射功能
 - 两个 eUSCI_A 接口，支持 UART、IrDA 和 SPI
 - 两个 eUSCI_B 接口，支持 SPI 和 I²C
- 高性能模拟
 - 高达 12 通道 12 位模数转换器 (ADC)
 - 内部共享基准 (1.5、2.0 或 2.5V)
 - 采样与保持 200ksp/s
 - 一个增强型比较器 (eCOMP)
 - 集成 6 位 DAC 作为基准电压
 - 可编程迟滞
 - 可配置的高功率和低功率模式
- 时钟系统 (CS)
 - 片上 32kHz RC 振荡器 (REFO)（具有 1 μ A 支持）
 - 带有锁频环 (FLL) 的片上 16MHz 数控振荡器 (DCO)
 - 室温下的精度为 $\pm 1\%$ （具有片上基准）
 - 片上超低频 10kHz 振荡器 (VLO)
 - 片上高频调制振荡器 (MODOSC)
 - 外部 32kHz 晶振 (LFXT)
 - 可编程 MCLK 预分频器（1 至 128）
 - 通过可编程预分频器（1、2、4 或 8）从 MCLK 获得的 SMCLK
- 通用输入/输出和引脚功能
 - LQFP-48 封装上的 43 个 I/O
 - 所有 GPIO 上的 43 个中断引脚可以将 MCU 从低功耗模式下唤醒
- 开发工具和软件
 - 开发工具
 - 目标开发板 [MSP-TS430PT48A](#)
 - LaunchPad™ 开发套件 [LP-MSP430FR2476](#)
- 系列成员（另请参阅 [器件比较](#)）
 - MSP430FR2476：64KB 程序 FRAM、512B 信息 FRAM、8KB RAM
 - MSP430FR2475：32KB 程序 FRAM、512B 信息 FRAM、4KB RAM
- 封装选项
 - 48 引脚：LQFP (PT)
 - 40 引脚：VQFN (RHA)
 - 32 引脚：VQFN (RHB)

1.2 应用

- 小型工业传感器
- 低功耗医疗、健康和健身器材
- 电池组
- EPOS
- 电器
- 恒温器
- 电动牙刷
- PC 配件

1.3 说明

MSP430FR247x 微控制器 (MCU) 是 MSP430™ MCU 超值系列超低功耗低成本器件产品系列的一部分，该产品系列用于检测和测量应用中的数字输入 D 类音频放大器。MSP430FR247x MCU 集成了一个 12 位 SAR ADC 和一个比较器。所有 MSP430FR247x MCU 均支持 -40° 至 105°C 的工作温度范围，因此这些器件的 FRAM 数据记录功能对更高温度的工业应用来说意义重大。

MSP430FR247x MCU 由一系列由软、硬件组成的生态系统提供支持，并提供有参考设计和代码示例，可帮助您快速开展设计。开发套件包括 [MSP-TS430PT48 48 引脚目标开发板](#)。TI 还提供免费的 [MSP430Ware™ 软件](#)，该软件以 [Code Composer Studio™ IDE](#) 台式机和云端版本组件的形式在 [TI Resource Explorer](#) 内部提供。MSP430 MCU 还通过 [E2E™ 社区论坛](#) 提供广泛的在线配套资料、培训和在线支持。

MSP430 超低功耗 (ULP) FRAM 微控制器平台将独特的嵌入式 FRAM 和整体超低功耗系统架构相结合，从而使系统设计人员能够在降低能耗的情况下提升性能。FRAM 技术将 RAM 的低功耗快速写入、灵活性和耐用性与闪存的非易失性相结合。

TI MSP430 系列低功耗微控制器包含多种器件，其中配备了不同的外设集以满足各类应用的需求。该架构与多种低功耗模式配合使用，经过优化，可在便携式测量应用延长电池寿命中的数字输入 D 类音频放大器。该 MCU 具有一个强大的 16 位精简指令集 (RISC) CPU，使用 16 位寄存器以及常数发生器，以便获得最高编码效率。数控振荡器 (DCO) 可使 MCU 在不到 10μs（典型值）的时间内从低功耗模式唤醒至活动模式。

有关完整的模块说明，请参阅 [《MSP430FR4xx 和 MSP430FR2xx 系列器件用户指南》](#)。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 ⁽²⁾
MSP430FR2476TPT	LQFP (48)	7mm × 7mm
MSP430FR2475TPT	LQFP (48)	7mm × 7mm
MSP430FR2476TRHA	VQFN (40)	6mm × 6mm
MSP430FR2475TRHA	VQFN (40)	6mm × 6mm
MSP430FR2476TRHB	VQFN (32)	5mm × 5mm
MSP430FR2475TRHB	VQFN (32)	5mm × 5mm

(1) 要获得最新的产品、封装和订购信息，请参见 [封装选项附录（节 9）](#)，或者访问德州仪器 (TI) 网站 [www.ti.com.cn](#)。

(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见 [机械数据（节 9 中）](#)。

CAUTION

系统级静电放电 (ESD) 保护必须符合器件级 ESD 规范，以防发生电气过载或对数据或代码存储器造成干扰。有关更多信息，请参阅 [《MSP430 系统级 ESD 注意事项》](#)。

1.4 功能方框图

图 1-1 给出了功能框图。

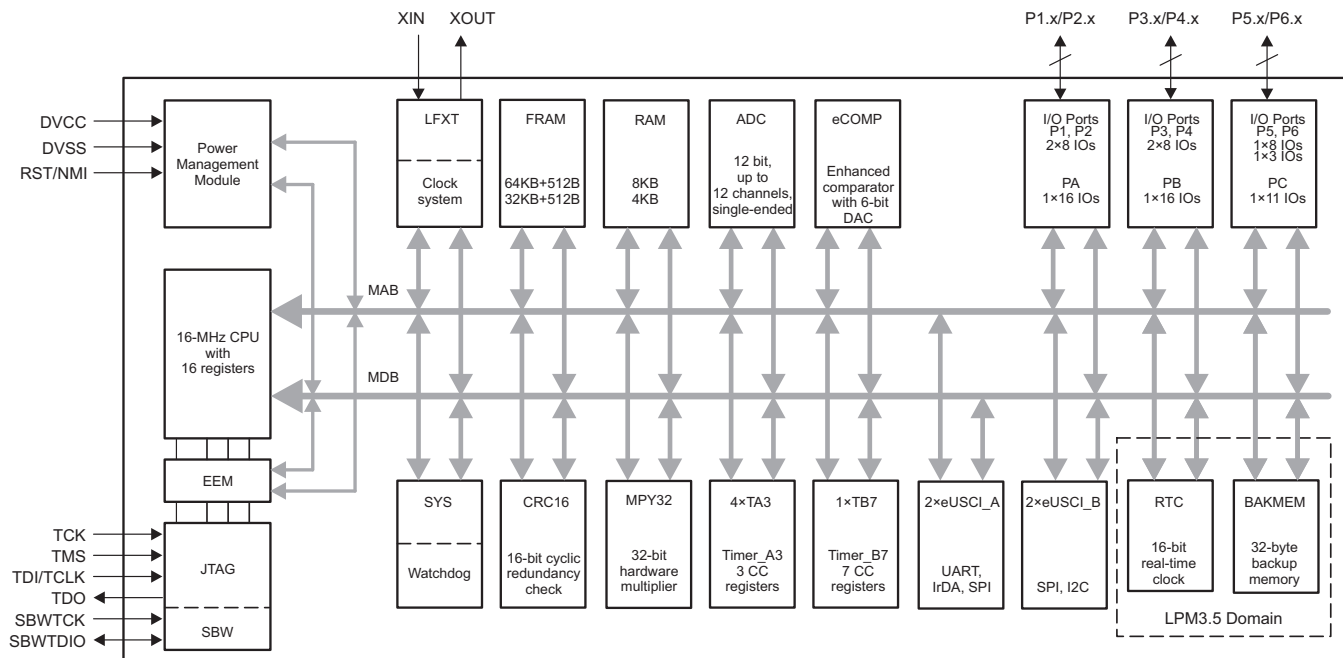


图 1-1. 功能框图

- MCU 的主电源对 DVCC 和 DVSS 分别为数字模块和模拟模块供电。推荐的旁路电容和去耦电容分别为 4.7 μ F 至 10 μ F 和 0.1 μ F，精度为 $\pm 5\%$ 。
- 所有 GPIO 均具备引脚中断功能，可将 MCU 从所有 LPM 模式唤醒。
- 在 LPM3.5 模式下，RTC 模块可在其他外设停止工作的情况下继续工作。

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2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

从修订版本 A 更改为修订版本 B

Changes from April 26, 2019 to December 10, 2019	Page
- Changed the note that begins "Supply voltage changes faster than 0.2 V/μs can trigger a BOR reset..." in Section 5.3, Recommended Operating Conditions 21 - Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, Recommended Operating Conditions 21 - Changed the note that begins "A capacitor tolerance of $\pm 20\%$ or better is required..." in Section 5.3, Recommended Operating Conditions 21 - Added the note "See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing" to Table 5-4, XT1 Crystal Oscillator (Low Frequency) 28 - Changed the note that begins "Requires external capacitors at both terminals..." in Table 5-4, XT1 Crystal Oscillator (Low Frequency) 28 - Added the $t_{TA, cap}$ parameter in Table 5-13, Timer_A 35 - Added the $t_{TB, cap}$ parameter in Table 5-14, Timer_B 35 - Corrected the test conditions for the R_I parameter in Table 5-21, ADC, Power Supply and Input Range Conditions . 42 - Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$..." in Table 5-22, ADC, Timing Parameters 42 - Changed CRC covered end address to 0x1AF7 in table note (1) in Table 6-30, Device Descriptors 72	

从初始发行版更改为修订版本 A

Changes from March 12, 2019 to April 25, 2019	Page
- 将文档状态更改为“生产数据” 1 - Updated Section 5.7 Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current with production values 23 - Updated Table 5-5 DCO FLL, Frequency with production values 28	

3 Device Comparison

Table 3-1 summarizes the features of the available family members.

Table 3-1. Device Comparison⁽¹⁾⁽²⁾

DEVICE	PROGRAM FRAM + INFORMATION FRAM (KB)	SRAM (KB)	TA0, TA1, TA2, TA3	TB0	eUSCI_A0 eUSCI_A1	eUSCI_B0 eUSCI_B1	12-BIT ADC CHANNELS	eCOMP	GPIOs	PACKAGE
MSP430FR2476TPT	64 + 0.5	8	4, 3 × CCR ⁽³⁾	1, 7 × CCR ⁽⁴⁾	2	2	12	1	43	48 LQFP (PT)
MSP430FR2475TPT	32 + 0.5	4	4, 3 × CCR ⁽³⁾	1, 7 × CCR ⁽⁴⁾	2	2	12	1	43	48 LQFP (PT)
MSP430FR2476TRHA	64 + 0.5	8	4, 3 × CCR ⁽³⁾	1, 7 × CCR ⁽⁴⁾	2	2	10	1	35	40 VQFN (RHA)
MSP430FR2475TRHA	32 + 0.5	4	4, 3 × CCR ⁽³⁾	1, 7 × CCR ⁽⁴⁾	2	2	10	1	35	40 VQFN (RHA)
MSP430FR2476TRHB	64 + 0.5	8	4, 3 × CCR ⁽³⁾	1, 7 × CCR ⁽⁵⁾	2	2	8	1	27	32 VQFN (RHB)
MSP430FR2475TRHB	32 + 0.5	4	4, 3 × CCR ⁽³⁾	1, 7 × CCR ⁽⁵⁾	2	2	8	1	27	32 VQFN (RHB)

(1) For the most current package and ordering information, see the *Package Option Addendum* in § 9, or see the TI website at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs. TA0 and TA1 are externally connected on CCR1, CCR2. TA2 and TA3 are externally connected on CCR0 to CCR2.

(4) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs. TB0 is externally connected on CCR0 to CCR6.

(5) A CCR register is a configurable register that provides internal capture only, CCR0 to CCR6 registers can only be used for period timing and interrupt generation, NO PWM outputs functionality.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

[Products for 16-bit and 32-bit microcontrollers](#)

High-performance, low-power solutions to enable the autonomous future

[Products for MSP430 ultra-low-power sensing & measurement microcontrollers](#)

One platform. One ecosystem. Endless possibilities.

[Companion products for MSP430FR2476](#)

Review products that are frequently purchased or used in conjunction with this product.

[Reference designs for MSP430FR2476](#)

Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 48-pin PT package.

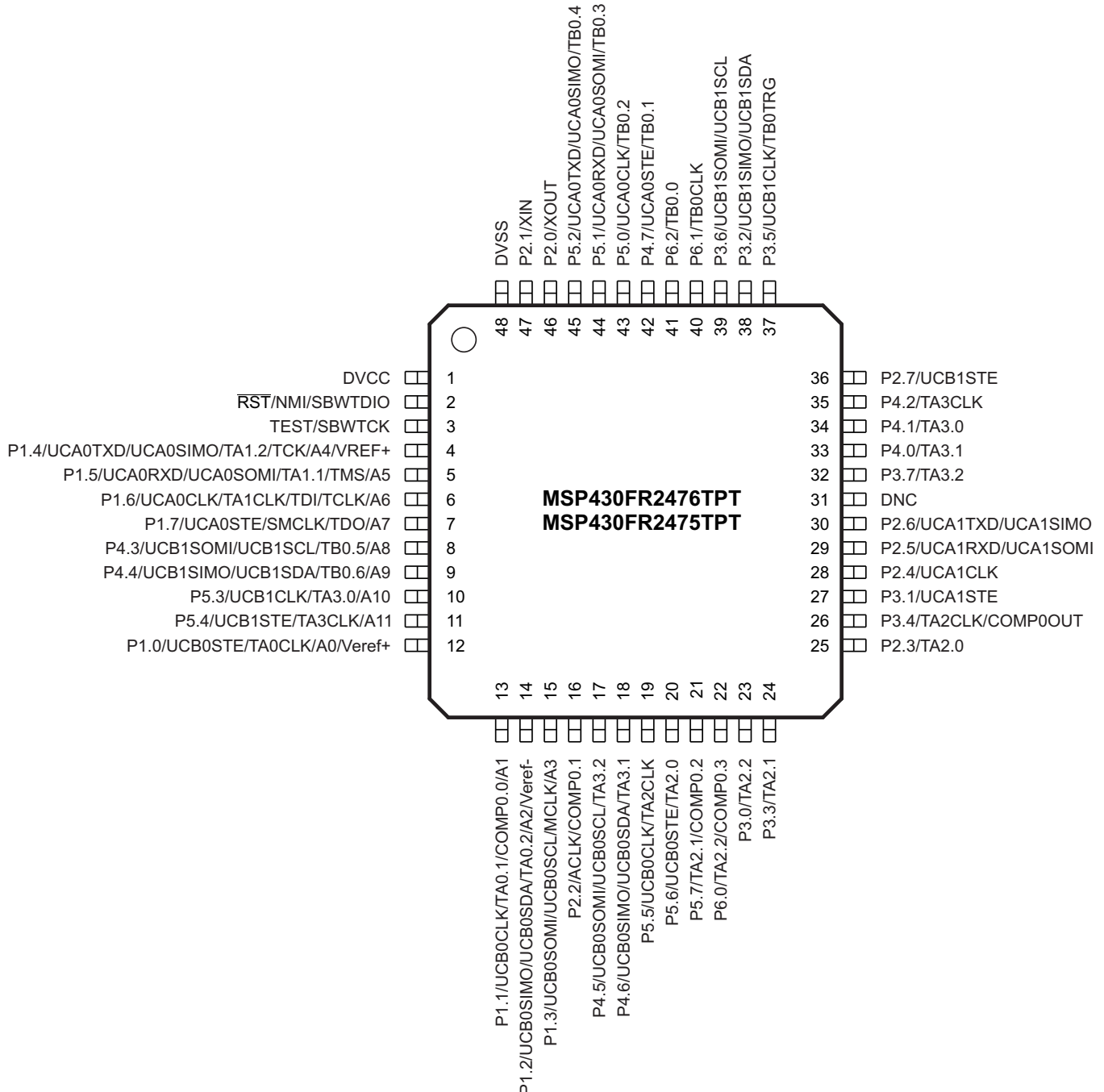


Figure 4-1. 48-Pin PT Package (Top View)

Figure 4-2 shows the pinout of the 40-pin RHA package.

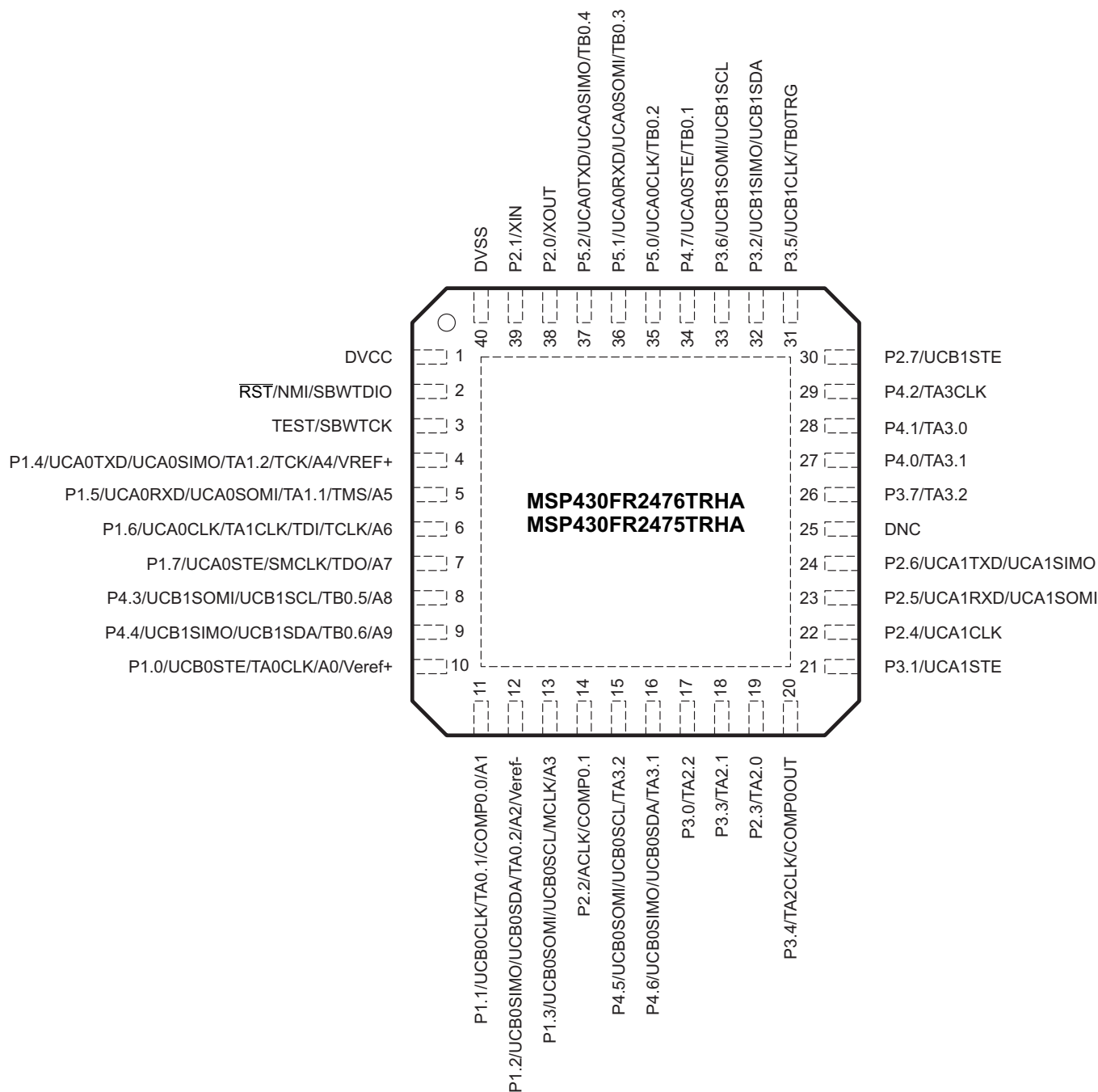


Figure 4-2. 40-Pin RHA Package (Top View)

Figure 4-3 shows the pinout of the 32-pin RHB package.

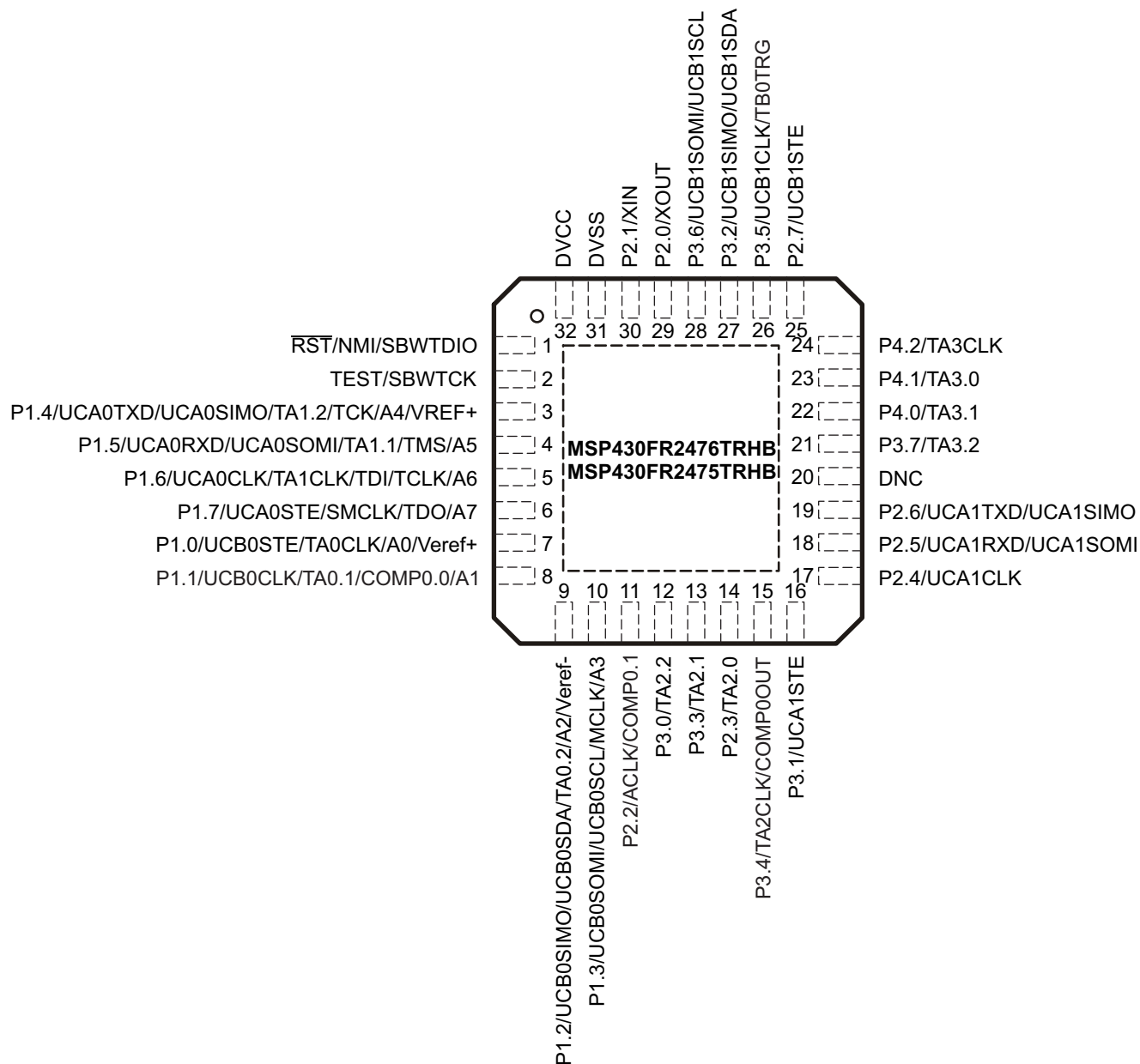


Figure 4-3. 32-Pin RHB Package (Top View)

4.2 Pin Attributes

Table 4-1 lists the attributes of all pins.

Table 4-1. Pin Attributes

PIN NUMBER			SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
PT	RHA	RHB					
1	1	32	DVCC	P	Power	DVCC	N/A
2	2	1	$\overline{\text{RST}}$ (RD)	I	LVC MOS	DVCC	PU
			NMI	I	LVC MOS	DVCC	–
			SBWTDIO	I/O	LVC MOS	DVCC	–
3	3	2	TEST (RD)	I	LVC MOS	DVCC	PD
			SBWTCK	I	LVC MOS	DVCC	–
4	4	3	P1.4 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0TXD	O	LVC MOS	DVCC	–
			UCA0SIMO	I/O	LVC MOS	DVCC	–
			TA1.2	I/O	LVC MOS	DVCC	–
			TCK	I	LVC MOS	DVCC	–
			A4	I	Analog	DVCC	–
			VREF+	O	Power	DVCC	–
5	5	4	P1.5 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0RXD	I	LVC MOS	DVCC	–
			UCA0SOMI	I/O	LVC MOS	DVCC	–
			TA1.1	I/O	LVC MOS	DVCC	–
			TMS	I	LVC MOS	DVCC	–
			A5	I	Analog	DVCC	–
6	6	5	P1.6 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0CLK	I/O	LVC MOS	DVCC	–
			TA1CLK	I	LVC MOS	DVCC	–
			TDI	I	LVC MOS	DVCC	–
			TCLK	I	LVC MOS	DVCC	–
			A6	I	Analog	DVCC	–
7	7	6	P1.7 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0STE	I/O	LVC MOS	DVCC	–
			SMCLK	O	LVC MOS	DVCC	–
			TDO	O	LVC MOS	DVCC	–
			A7	I	Analog	DVCC	–
8	8	–	P4.3 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SOMI	I/O	LVC MOS	DVCC	–
			UCB1SCL	I/O	LVC MOS	DVCC	–
			TB0.5	I/O	LVC MOS	DVCC	–
			A8	I	Analog	DVCC	–

(1) Signals names with (RD) denote the reset default pin name.

(2) To determine the pin mux encodings for each pin, see Section 6.11.

(3) Signal types: I = input, O = output, I/O = input or output

(4) Buffer types: LVC MOS, Analog, or Power (see Table 4-3)

(5) The power source shown in this table is the I/O power source, which may differ from the module power source.

(6) Reset States:

OFF = High impedance with Schmitt trigger and pullup or pulldown (if available) disabled

PU = Pullup is enabled

PD = Pulldown is enabled

N/A = Not applicable

Table 4-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
PT	RHA	RHB					
9	9	–	P4.4 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SIMO	I/O	LVC MOS	DVCC	–
			UCB1SDA	I/O	LVC MOS	DVCC	–
			TB0.6	I/O	LVC MOS	DVCC	–
			A9	I	Analog	DVCC	–
10	–	–	P5.3 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1CLK	I/O	LVC MOS	DVCC	–
			TA3.0	I/O	LVC MOS	DVCC	–
			A10	I	Analog	DVCC	–
11	–	–	P5.4 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1STE	I/O	LVC MOS	DVCC	–
			TA3CLK	I/O	LVC MOS	DVCC	–
			A11	I	Analog	DVCC	–
12	10	7	P1.0 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB0STE	I/O	LVC MOS	DVCC	–
			TA0CLK	I	LVC MOS	DVCC	–
			A0	I	Analog	DVCC	–
			Veref+	I	Power	DVCC	–
13	11	8	P1.1 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB0CLK	I/O	LVC MOS	DVCC	–
			TA0.1	I/O	LVC MOS	DVCC	–
			A1	I	Analog	DVCC	–
			COMP0.0	I	Analog	DVCC	–
14	12	9	P1.2 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB0SIMO	I/O	LVC MOS	DVCC	–
			UCB0SDA	I/O	LVC MOS	DVCC	–
			TA0.2	I/O	LVC MOS	DVCC	–
			A2	I	Analog	DVCC	–
			Veref-	I	Power	DVCC	–
15	13	10	P1.3 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB0SOMI	I/O	LVC MOS	DVCC	–
			UCB0SCL	I/O	LVC MOS	DVCC	–
			MCLK	O	LVC MOS	DVCC	–
			A3	I	Analog	DVCC	–
16	14	11	P2.2 (RD)	I/O	LVC MOS	DVCC	OFF
			ACLK	O	LVC MOS	DVCC	–
			COMP0.1	I	Analog	DVCC	–
17	15	–	P4.5 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB0SOMI	I/O	LVC MOS	DVCC	–
			UCB0SCL	I/O	LVC MOS	DVCC	–
			TA3.2	I/O	LVC MOS	DVCC	–
18	16	–	P4.6 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB0SIMO	I/O	LVC MOS	DVCC	–
			UCB0SDA	I/O	LVC MOS	DVCC	–
			TA3.1	I/O	LVC MOS	DVCC	–

Table 4-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
PT	RHA	RHB					
19	–	–	P5.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0CLK	I/O	LVCMOS	DVCC	–
			TA2CLK	I/O	LVCMOS	DVCC	–
20	–	–	P5.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB0STE	I/O	LVCMOS	DVCC	–
			TA2.0	I/O	LVCMOS	DVCC	–
21	–	–	P5.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.1	I/O	LVCMOS	DVCC	–
			COMP0.2	I	Analog	DVCC	–
22	–	–	P6.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.2	I/O	LVCMOS	DVCC	–
			COMP0.3	I	Analog	DVCC	–
23	17	12	P3.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.2	I/O	LVCMOS	DVCC	–
24	18	13	P3.3 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.1	I/O	LVCMOS	DVCC	–
25	19	14	P2.3 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2.0	I/O	LVCMOS	DVCC	–
26	20	15	P3.4 (RD)	I/O	LVCMOS	DVCC	OFF
			TA2CLK	I/O	LVCMOS	DVCC	–
			COMP0OUT	O	LVCMOS	DVCC	–
27	21	16	P3.1 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1STE	I/O	LVCMOS	DVCC	–
28	22	17	P2.4 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1CLK	I/O	LVCMOS	DVCC	–
29	23	18	P2.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1RXD	I	LVCMOS	DVCC	–
			UCA1SOMI	I/O	LVCMOS	DVCC	–
30	24	19	P2.6 (RD)	I/O	LVCMOS	DVCC	OFF
			UCA1TXD	O	LVCMOS	DVCC	–
			UCA1SIMO	I/O	LVCMOS	DVCC	–
31	25	20	DNC ⁽⁷⁾	–	–	–	–
32	26	21	P3.7 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.2	I/O	LVCMOS	DVCC	–
33	27	22	P4.0 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.1	I/O	LVCMOS	DVCC	–
34	28	23	P4.1 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3.0	I/O	LVCMOS	DVCC	–
35	29	24	P4.2 (RD)	I/O	LVCMOS	DVCC	OFF
			TA3CLK	I/O	LVCMOS	DVCC	–
36	30	25	P2.7 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1STE	I/O	LVCMOS	DVCC	–
37	31	26	P3.5 (RD)	I/O	LVCMOS	DVCC	OFF
			UCB1CLK	I/O	LVCMOS	DVCC	–
			TB0TRG	I	LVCMOS	DVCC	–

(7) DNC = do not connect

Table 4-1. Pin Attributes (continued)

PIN NUMBER			SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE ⁽⁵⁾	RESET STATE AFTER BOR ⁽⁶⁾
PT	RHA	RHB					
38	32	27	P3.2 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SIMO	I/O	LVC MOS	DVCC	–
			UCB1SDA	I/O	LVC MOS	DVCC	–
39	33	28	P3.6(RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SOMI	I/O	LVC MOS	DVCC	–
			UCB1SCL	I/O	LVC MOS	DVCC	–
40	–	–	P6.1 (RD)	I/O	LVC MOS	DVCC	OFF
			TB0CLK	I/O	LVC MOS	DVCC	–
41	–	–	P6.2 (RD)	I/O	LVC MOS	DVCC	OFF
			TB0.0	I/O	LVC MOS	DVCC	–
42	34	–	P4.7 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0STE	I/O	LVC MOS	DVCC	–
			TB0.1	I/O	LVC MOS	DVCC	–
43	35	–	P5.0 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0CLK	I/O	LVC MOS	DVCC	–
			TB0.2	I	LVC MOS	DVCC	–
44	36	–	P5.1 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0RXD	I	LVC MOS	DVCC	–
			UCA0SOMI	I/O	LVC MOS	DVCC	–
			TB0.3	I/O	LVC MOS	DVCC	–
45	37	–	P5.2 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0TXD	O	LVC MOS	DVCC	–
			UCA0SIMO	I/O	LVC MOS	DVCC	–
			TB0.4	I/O	LVC MOS	DVCC	–
46	38	29	P2.0 (RD)	I/O	LVC MOS	DVCC	OFF
			XOUT	O	LVC MOS	DVCC	–
47	39	30	P2.1 (RD)	I/O	LVC MOS	DVCC	OFF
			XIN	I	LVC MOS	DVCC	–
48	40	31	DVSS	P	Power	DVCC	N/A

4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

Table 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE ⁽¹⁾	DESCRIPTION
		PT	RHA	RHB		
ADC	A0	12	10	7	I	Analog input A0
	A1	13	11	8	I	Analog input A1
	A2	14	12	9	I	Analog input A2
	A3	15	13	10	I	Analog input A3
	A4	4	4	3	I	Analog input A4
	A5	5	5	4	I	Analog input A5
	A6	6	6	5	I	Analog input A6
	A7	7	7	6	I	Analog input A7
	A8	8	8	–	I	Analog input A8
	A9	9	9	–	I	Analog input A9
	A10	10	–	–	I	Analog input A10
	A11	11	–	–	I	Analog input A11
	Veref+	12	10	10	I	ADC positive reference
	Veref-	14	12	12	I	ADC negative reference
eCOMP0	COMP0.0	13	11	8	I	Enhanced comparator input channel C0
	COMP0.1	16	14	11	I	Enhanced comparator input channel C1
	COMP0.2	21	–	–	I	Enhanced comparator input channel C2
	COMP0.3	22	–	–	I	Enhanced comparator input channel C3
	COMP0OUT	26	20	15	O	Enhanced comparator output channel COUT
Clock	ACLK	16	14	11	I/O	ACLK output
	MCLK	15	13	10	O	MCLK output
	SMCLK	7	7	6	O	SMCLK output
	XIN	47	39	30	I	Input terminal for crystal oscillator
	XOUT	46	38	29	O	Output terminal for crystal oscillator
Debug	SBWTCK	3	3	2	I	Spy-Bi-Wire input clock
	SBWTDIO	2	2	1	I/O	Spy-Bi-Wire data input/output
	TCK	4	4	3	I	Test clock
	TCLK	6	6	5	I	Test clock input
	TDI	6	6	5	I	Test data input
	TDO	7	7	6	O	Test data output
	TEST	3	3	2	I	Test Mode pin – selected digital I/O on JTAG pins
	TMS	5	5	4	I	Test mode select

(1) Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE ⁽¹⁾	DESCRIPTION
		PT	RHA	RHB		
GPIO, Port 1	P1.0	12	10	7	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.1	13	11	8	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.2	14	12	9	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.3	15	13	10	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P1.4	4	4	3	I/O	General-purpose I/O with port interrupt and wake from LPMx.5 ⁽²⁾
	P1.5	5	5	4	I/O	General-purpose I/O with port interrupt and wake from LPMx.5 ⁽²⁾
	P1.6	6	6	5	I/O	General-purpose I/O with port interrupt and wake from LPMx.5 ⁽²⁾
	P1.7	7	7	6	I/O	General-purpose I/O with port interrupt and wake from LPMx.5 ⁽²⁾
GPIO, Port 2	P2.0	46	38	29	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.1	47	39	30	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.2	16	14	11	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.3	25	19	14	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.4	28	22	17	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.5	29	23	18	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.6	30	24	19	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P2.7	36	30	25	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 3	P3.0	23	17	12	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.1	27	21	16	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.2	38	32	27	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.3	24	18	13	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.4	26	20	15	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.5	37	31	26	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.6	39	33	28	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P3.7	32	26	21	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 4	P4.0	33	27	22	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.1	34	28	23	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.2	35	29	24	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.3	8	8	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.4	9	9	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.5	17	15	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.6	18	16	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P4.7	42	34	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
GPIO, Port 5	P5.0	43	35	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.1	44	36	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.2	45	37	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.3	10	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.4	11	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.5	19	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.6	20	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P5.7	21	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5

(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE ⁽¹⁾	DESCRIPTION
		PT	RHA	RHB		
GPIO, Port 6	P6.0	22	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P6.1	40	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
	P6.2	41	–	–	I/O	General-purpose I/O with port interrupt and wake from LPMx.5
I ² C	UCB0SCL ⁽³⁾	15	13	10	I/O	eUSCI_B0 I ² C clock
	UCB0SDA ⁽³⁾	14	12	9	I/O	eUSCI_B0 I ² C data
	UCB0SCL ⁽⁴⁾	17	15	–	I/O	eUSCI_B0 I ² C clock
	UCB0SDA ⁽⁴⁾	18	16	–	I/O	eUSCI_B0 I ² C data
	UCB1SCL ⁽³⁾	39	33	28	I/O	eUSCI_B1 I ² C clock
	UCB1SDA ⁽³⁾	38	32	27	I/O	eUSCI_B1 I ² C data
	UCB1SCL ⁽⁴⁾	8	8	–	I/O	eUSCI_B1 I ² C clock
	UCB1SDA ⁽⁴⁾	9	9	–	I/O	eUSCI_B1 I ² C data
Power	DVCC	1	1	32	P	Power supply
	DVSS	48	40	31	P	Power ground
	VREF+	4	4	3	P	Output of positive reference voltage with ground as reference

(3) This is the remapped default functionality controlled by the USCIBRMP or USCIRAMP bit of the SYSCFG2 or SYSCFG3 register. Only one selected port is valid at any time.

(4) This is the remapped functionality controlled by the USCIBRMP or USCIRAMP bit of the SYSCFG2 or SYSCFG3 register. Only one selected port is valid at any time.

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE ⁽¹⁾	DESCRIPTION
		PT	RHA	RHB		
SPI	UCA0STE ⁽³⁾	7	7	6	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0CLK ⁽³⁾	6	6	5	I/O	eUSCI_A0 SPI clock input/output
	UCA0SOMI ⁽³⁾	5	5	4	I/O	eUSCI_A0 SPI slave out/master in
	UCA0SIMO ⁽³⁾	4	4	3	I/O	eUSCI_A0 SPI slave in/master out
	UCA0STE ⁽⁴⁾	42	34	–	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0CLK ⁽⁴⁾	43	35	–	I/O	eUSCI_A0 SPI clock input/output
	UCA0SOMI ⁽⁴⁾	44	36	–	I/O	eUSCI_A0 SPI slave out/master in
	UCA0SIMO ⁽⁴⁾	45	37	–	I/O	eUSCI_A0 SPI slave in/master out
	UCA1STE	27	21	16	I/O	eUSCI_A1 SPI slave transmit enable
	UCA1CLK	28	22	17	I/O	eUSCI_A1 SPI clock input/output
	UCA1SOMI	29	23	18	I/O	eUSCI_A1 SPI slave out/master in
	UCA1SIMO	30	24	19	I/O	eUSCI_A1 SPI slave in/master out
	UCB0STE ⁽³⁾	12	10	7	I/O	eUSCI_B0 slave transmit enable
	UCB0CLK ⁽³⁾	13	11	8	I/O	eUSCI_B0 clock input/output
	UCB0SOMI ⁽³⁾	15	13	10	I/O	eUSCI_B0 SPI slave out/master in
	UCB0SIMO ⁽³⁾	14	12	9	I/O	eUSCI_B0 SPI slave in/master out
	UCB0STE ⁽⁴⁾	20	–	–	I/O	eUSCI_B0 slave transmit enable
	UCB0CLK ⁽⁴⁾	19	–	–	I/O	eUSCI_B0 clock input/output
	UCB0SOMI ⁽⁴⁾	17	–	–	I/O	eUSCI_B0 SPI slave out/master in
	UCB0SIMO ⁽⁴⁾	18	–	–	I/O	eUSCI_B0 SPI slave in/master out
	UCB1STE ⁽³⁾	36	30	25	I/O	eUSCI_B1 slave transmit enable
	UCB1CLK ⁽³⁾	37	31	26	I/O	eUSCI_B1 clock input/output
	UCB1SOMI ⁽³⁾	39	33	28	I/O	eUSCI_B1 SPI slave out/master in
	UCB1SIMO ⁽³⁾	38	32	27	I/O	eUSCI_B1 SPI slave in/master out
	UCB1STE ⁽⁴⁾	11	–	–	I/O	eUSCI_B1 slave transmit enable
	UCB1CLK ⁽⁴⁾	10	–	–	I/O	eUSCI_B1 clock input/output
	UCB1SOMI ⁽⁴⁾	8	–	–	I/O	eUSCI_B1 SPI slave out/master in
	UCB1SIMO ⁽⁴⁾	9	–	–	I/O	eUSCI_B1 SPI slave in/master out
System	NMI	2	2	1	I	Nonmaskable interrupt input
	RST	2	2	1	I	Active-low reset input

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER			PIN TYPE ⁽¹⁾	DESCRIPTION
		PT	RHA	RHB		
Timer_A	TA0.1	13	11	8	I/O	Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA0.2	14	12	9	I/O	Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA0CLK	12	10	7	I	Timer clock input TACLK for TA0
	TA1.1	5	5	4	I/O	Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA1.2	4	4	3	I/O	Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA1CLK	6	6	5	I	Timer clock input TACLK for TA1
	TA2.0 ⁽⁵⁾	25	19	14	I/O	Timer TA2 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA2.1 ⁽⁵⁾	24	18	13	I/O	Timer TA2 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA2.2 ⁽⁵⁾	23	17	12	I/O	Timer TA2 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA2CLK ⁽⁵⁾	26	20	15	I	Timer clock input TACLK for TA2
	TA2.0 ⁽⁶⁾	20	–	–	I/O	Timer TA2 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA2.1 ⁽⁶⁾	21	–	–	I/O	Timer TA2 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA2.2 ⁽⁶⁾	22	–	–	I/O	Timer TA2 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA2CLK ⁽⁶⁾	19	–	–	I	Timer clock input TACLK for TA2
	TA3.0 ⁽⁵⁾	34	28	23	I/O	Timer TA3 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA3.1 ⁽⁵⁾	33	27	22	I/O	Timer TA3 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA3.2 ⁽⁵⁾	32	26	21	I/O	Timer TA3 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA3CLK ⁽⁵⁾	35	29	24	I	Timer clock input TACLK for TA3
	TA3.0 ⁽⁶⁾	10	–	–	I/O	Timer TA3 CCR0 capture: CCI0A input, compare: Out0 outputs
	TA3.1 ⁽⁶⁾	18	16	–	I/O	Timer TA3 CCR1 capture: CCI1A input, compare: Out1 outputs
	TA3.2 ⁽⁶⁾	17	15	–	I/O	Timer TA3 CCR2 capture: CCI2A input, compare: Out2 outputs
	TA3CLK ⁽⁶⁾	11	–	–	I	Timer clock input TACLK for TA3
Timer_B	TB0.0	41	–	–	I/O	Timer TB0 CCR0 capture: CCI0A input, compare: Out0 outputs
	TB0.1	42	34	–	I/O	Timer TB0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TB0.2	43	35	–	I/O	Timer TB0 CCR2 capture: CCI2A input, compare: Out2 outputs
	TB0.3	44	36	–	I/O	Timer TB0 CCR3 capture: CCI3A input, compare: Out3 outputs
	TB0.4	45	37	–	I/O	Timer TB0 CCR4 capture: CCI4A input, compare: Out4 outputs
	TB0.5	8	8	–	I/O	Timer TB0 CCR5 capture: CCI5A input, compare: Out5 outputs
	TB0.6	9	9	–	I/O	Timer TB0 CCR6 capture: CCI6A input, compare: Out6 outputs
	TB0CLK	40	–	–	I	Timer clock input TBCLK for TB0
	TB0TRG	37	31	26		Timer TB0 external trigger input for TB0OUTH
UART	UCA0RXD ⁽³⁾	5	5	4	I	eUSCI_A0 UART receive data
	UCA0TXD ⁽³⁾	4	4	3	O	eUSCI_A0 UART transmit data
	UCA0RXD ⁽⁴⁾	44	36	–	I	eUSCI_A0 UART receive data
	UCA0TXD ⁽⁴⁾	45	37	–	O	eUSCI_A0 UART transmit data
	UCA1RXD	29	23	18	I	eUSCI_A1 UART receive data
	UCA1TXD	30	24	19	O	eUSCI_A1 UART transmit data
DNC	Do not connect	31	25	20	–	Do not connect
VQFN pad	VQFN thermal pad	–	PAD	PAD	–	VQFN package exposed thermal pad. TI recommends connecting to V _{SS}

(5) This is the remapped default functionality controlled by the TARMP bit of the SYSCFG3 register. Only one selected port is valid at any time.

(6) This is the remapped functionality controlled by the TARMP bit of the SYSCFG3 register. Only one selected port is valid at any time.

4.4 Pin Multiplexing

Pin multiplexing for this MCU is controlled by both register settings and operating modes (for example, if the MCU is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see [Section 6.11](#).

4.5 Buffer Types

[Table 4-3](#) defines the pin buffer types that are listed in [Table 4-1](#)

Table 4-3. Buffer Types

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (μ A)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
LVC MOS	3.0 V	$\gamma^{(1)}$	Programmable	See Section 5.11.4	See Section 5.11.4	
Analog	3.0 V	N	N/A	N/A	N/A	See analog modules in Section 5 for details.
Power (DVCC)	3.0 V	N	N/A	N/A	N/A	SVS enables hysteresis on DVCC.
Power (AVCC)	3.0 V	N	N/A	N/A	N/A	

(1) Only for input pins.

4.6 Connection of Unused Pins

[Table 4-4](#) lists the correct termination of unused pins.

Table 4-4. Connection of Unused Pins⁽¹⁾

PIN	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Switched to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}/\text{NMI}$	DV _{CC}	47-k Ω pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown ⁽²⁾
TEST	Open	This pin always has an internal pulldown enabled.

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
- (2) The pulldown capacitor should not exceed 1.1 nF when using MCUs with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC pin to V _{SS}	−0.3	4.1	V
Voltage applied to any other pin ⁽²⁾	−0.3	V _{CC} + 0.3 (4.1 V Max)	V
Diode current at any device pin		±2	mA
Junction temperature, T _J		115	°C
Storage temperature, T _{stg} ⁽³⁾	−40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS}.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage applied at DVCC pin ⁽¹⁾⁽²⁾⁽³⁾	1.8 ⁽⁴⁾		3.6	V
V _{SS} Supply voltage applied at DVSS pin		0		V
T _A Operating free-air temperature	−40		105	°C
T _J Operating junction temperature	−40		115	°C
C _{DVCC} Recommended capacitor at DVCC ⁽⁵⁾	4.7	10		μF
f _{SYSTEM} Processor frequency (MCLK frequency) ⁽⁴⁾⁽⁶⁾	No FRAM wait states (NWAITSx = 0)		0	MHz
	With FRAM wait states (NWAITSx = 1) ⁽⁷⁾		16 ⁽⁸⁾	
f _{ACLK} ACLK frequency			40	kHz
f _{SMCLK} SMCLK frequency			16 ⁽⁸⁾	MHz

- (1) Supply voltage changes faster than 0.2 V/μs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C_{DVCC} limits the slopes accordingly.
- (2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
- (4) The minimum supply voltage is defined by the SVS levels. Refer to the SVS threshold parameters in [Table 5-2](#).
- (5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
- (6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
- (8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

 See ⁽¹⁾

PARAMETER	EXECUTION MEMORY	TEST CONDITION	FREQUENCY (f _{MCLK} = f _{SMCLK})						UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	
I _{AM, FRAM} (0%)	FRAM 0% cache hit ratio	3 V, 25°C	567		3208		3472		μA
		3 V, 85°C	578		3226		3471		
		3 V, 105°C	593		3249		3496	3750	
I _{AM, FRAM} (75%)	FRAM 75% cache hit ratio	3 V, 25°C	324		1272		2022		μA
		3 V, 85°C	340		1304		2065		
		3 V, 105°C	354		1321		2085		
I _{AM, FRAM} (100%)	FRAM 100% cache hit ratio	3 V, 25°C	241		604		1016		μA
		3 V, 85°C	255		624		1041		
		3 V, 105°C	270		641		1060	1150	
I _{AM, RAM} ⁽²⁾	RAM	3 V, 25°C	268		821		1446		μA

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. Characterized with program executing typical data processing.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency

Program and data entirely reside in FRAM. All execution is from FRAM.

(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

5.5 Active Mode Supply Current Per MHz

$V_{CC} = 3$ V, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
$dI_{AM,FRAM}/df$	Active mode current consumption per MHz, execution from FRAM, no wait states I_{AM} (75% cache hit rate) at 8 MHz – I_{AM} (75% cache hit rate) at 1 MHz / 7 MHz	135	$\mu A/MHz$

5.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

$V_{CC} = 3$ V, $T_A = 25^\circ C$ (unless otherwise noted) ⁽¹⁾⁽²⁾

PARAMETER	V _{CC}	FREQUENCY (f _{SMCLK})						UNIT
		1 MHz		8 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM0}	2 V	204		312		437		μA
	3 V	215		325		450		

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, f_{SMCLK} at specified frequency.

5.7 Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER	V_{CC}	–40°C		25°C		85°C		105°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT1}$ Low-power mode 3, 12.5-pF crystal, includes SVS ⁽²⁾⁽³⁾⁽⁴⁾	3 V	1.2		1.48		7.82		17.12	46	μA
	2 V	1.17		1.46		7.75		16.99		
$I_{LPM3, REFO}$ Low-power mode 3, RTC, excludes SVS ⁽⁵⁾	3 V	1.87		2.20		8.53		17.76		μA
	2 V	1.85		2.18		8.47		17.65		
$I_{LPM3,VLO}$ Low-power mode 3, VLO, excludes SVS ⁽⁶⁾	3 V	0.92		1.20		7.54		16.83	45.8	μA
	2 V	0.90		1.17		7.47		16.70		
$I_{LPM3, RTC}$ Low-power mode 3, RTC, excludes SVS ⁽⁷⁾	3 V	0.99		1.27		7.6		16.9		μA
	2 V	0.97		1.24		7.53		16.77		
$I_{LPM4, SVS}$ Low-power mode 4, includes SVS ⁽⁸⁾	3 V	0.65		0.90		7.19		16.41		μA
	2 V	0.64		0.89		7.13		16.30		
I_{LPM4} Low-power mode 4, excludes SVS ⁽⁸⁾	3 V	0.50		0.74		7.02		16.24		μA
	2 V	0.49		0.73		6.96		16.13		
$I_{LPM4,VLO}$ Low-power mode 4, RTC is sourced from VLO, excludes SVS ⁽⁹⁾	3 V	0.59		0.83		7.12		16.35		μA
	2 V	0.58		0.82		7.06		16.24		
$I_{LPM4,XT1}$ Low-power mode 4, RTC is sourced from XT1, excludes SVS ⁽¹⁰⁾	3 V	0.92		1.2		7.54		16.84		μA
	2 V	0.90		1.18		7.47		16.70		

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Not applicable for MCUs with HF crystal oscillator only.

(3) Characterized with a Seiko Crystal SC-32S MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.

(4) Low-power mode 3, 12.5-pF crystal, includes SVS test conditions:

Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

$f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(5) RTC periodically wakes up every second with internal REFO 32768-Hz input as source.

(6) Low-power mode 3, VLO, excludes SVS test conditions:

Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0). CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3)

$f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(7) RTC periodically wakes up every second with external 32768-Hz input as source.

(8) Low-power mode 4, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), CPU and all clocks are disabled, WDT and RTC disabled

(9) Low-power mode 4, VLO, excludes SVS test conditions:

Current for RTC clocked by VLO included. Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4)

$f_{XT1} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(10) Low-power mode 4, XT1, excludes SVS test conditions:

Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4)

$f_{XT1} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

5.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	–40°C		25°C		85°C		105°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5, XT1}$	Low-power mode 3.5, 12.5-pF crystal, includes SVS ^{(1)(2) (3)} (also see Figure 5-3)	3 V	0.60		0.66		0.96		1.41	2.95	μA
		2 V	0.58		0.65		0.92		1.33		
$I_{LPM4.5, SVS}$	Low-power mode 4.5, includes SVS ⁽⁴⁾	3 V	0.24		0.26		0.40		0.61	1.10	μA
		2 V	0.23		0.25		0.37		0.56		
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS ⁽⁵⁾	3 V	0.029		0.041		0.161		0.361	0.80	μA
		2 V	0.027		0.037		0.137		0.31		

(1) Not applicable for MCUs with HF crystal oscillator only.

(2) Characterized with a Seiko Crystal SC-32S MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.

(3) Low-power mode 3.5, 12.5-pF crystal, includes SVS test conditions:

Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

f_{XT1} = 32768 Hz, f_{ACLK} = 0, f_{MCLK} = f_{SMCLK} = 0 MHz

(4) Low-power mode 4.5, includes SVS test conditions:

Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)

f_{XT1} = 0 Hz, f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

(5) Low-power mode 4.5, excludes SVS test conditions:

Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)

f_{XT1} = 0 Hz, f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

5.9 Typical Characteristics – Low-Power Mode Supply Currents

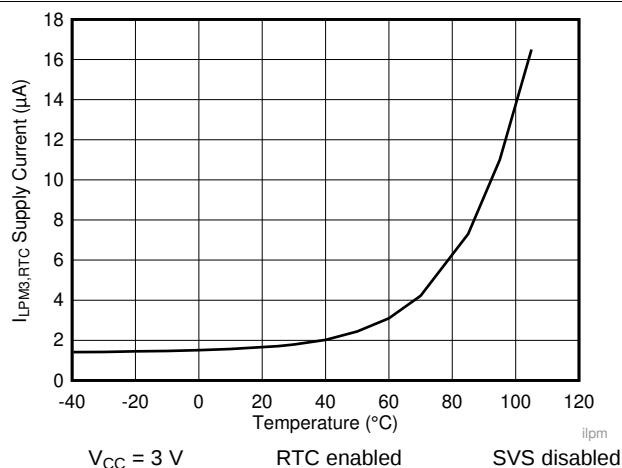


Figure 5-1. LPM3 Supply Current vs Temperature

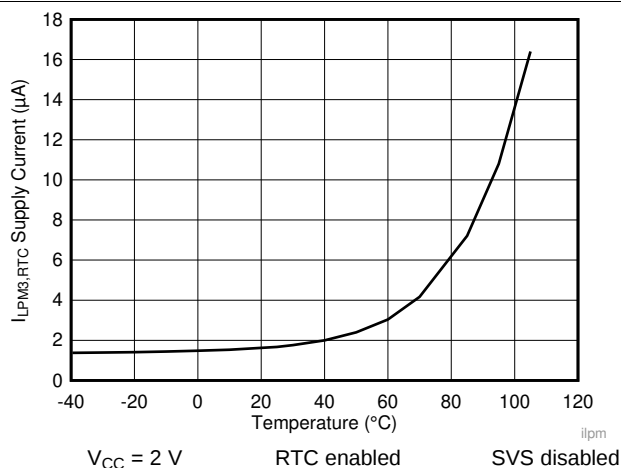


Figure 5-2. LPM3 Supply Current vs Temperature

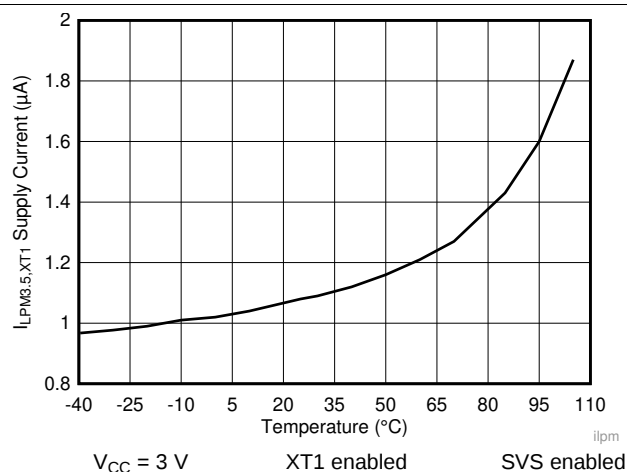


Figure 5-3. LPM3.5 Supply Current vs Temperature

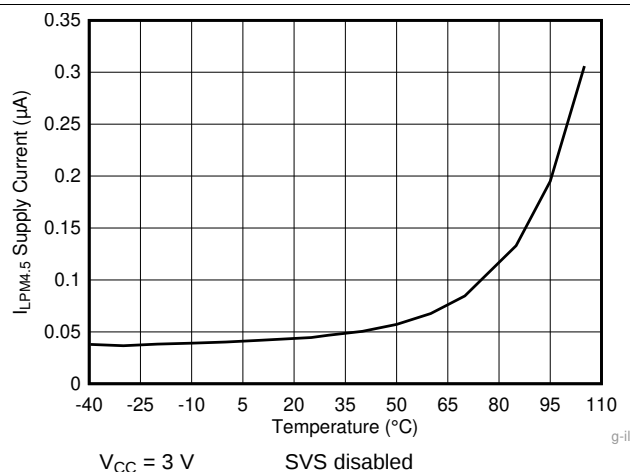


Figure 5-4. LPM4.5 Supply Current vs Temperature

Table 5-1. Typical Characteristics – Current Consumption Per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		5		µA/MHz
eUSCI_A	UART mode	Module input clock		7		µA/MHz
eUSCI_A	SPI mode	Module input clock		5		µA/MHz
eUSCI_B	SPI mode	Module input clock		5		µA/MHz
eUSCI_B	I ² C mode, 100 kbaud	Module input clock		5		µA/MHz
RTC		32 kHz		85		nA
CRC	From start to end of operation	MCLK		8.5		µA/MHz

5.10 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		VALUE ⁽²⁾	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	LQFP 48 pin (PT)	62.4
		VQFN 40 pin (RHA)	31.0
		VQFN 32 pin (RHB)	30.8
$R\theta_{JC}$	Junction-to-case (top) thermal resistance	LQFP 48 pin (PT)	22.1
		VQFN 40 pin (RHA)	22.3
		VQFN 32 pin (RHB)	20.8
$R\theta_{JB}$	Junction-to-board thermal resistance	LQFP 48 pin (PT)	26.3
		VQFN 40 pin (RHA)	12.3
		VQFN 32 pin (RHB)	11.6

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
 - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages*
 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages*
 - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

5.11 Timing and Switching Characteristics

5.11.1 Power Supply Sequencing

Table 5-2 lists the characteristics of the SVS and BOR.

Table 5-2. PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR, safe}$	Safe BOR power-down level ⁽¹⁾		0.1			V
$t_{BOR, safe}$	Safe BOR reset delay ⁽²⁾		10			ms
$I_{SVSH, AM}$	SVS _H current consumption, active mode	$V_{CC} = 3.6\text{ V}$			1.5	μA
$I_{SVSH, LPM}$	SVS _H current consumption, low-power modes	$V_{CC} = 3.6\text{ V}$		240		nA
V_{SVSH-}	SVS _H power-down level ⁽³⁾		1.71	1.80	1.87	V
V_{SVSH+}	SVS _H power-up level ⁽³⁾		1.76	1.88	1.99	V
$V_{SVSH, hys}$	SVS _H hysteresis			100		mV
$t_{PD, SVSH, AM}$	SVS _H propagation delay, active mode				10	μs
$t_{PD, SVSH, LPM}$	SVS _H propagation delay, low-power modes				100	μs

- (1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
- (2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+} .
- (3) For additional information, see the [Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design](#).

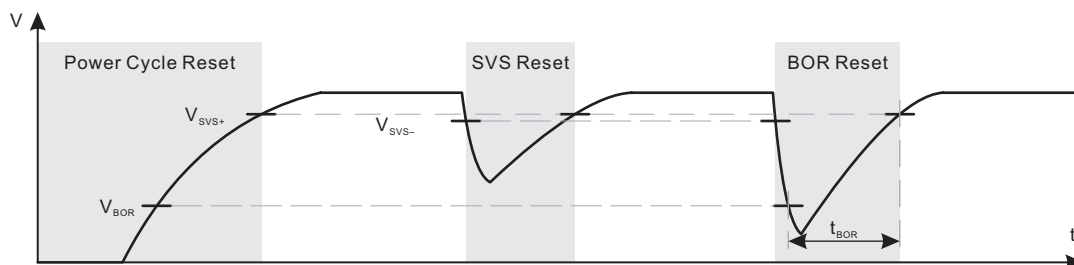


Figure 5-5. Power Cycle, SVS, and BOR Reset Conditions

5.11.2 Reset Timing

Table 5-3 lists the timing characteristics of wakeup from LPMs and reset.

Table 5-3. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{WAKE-UP FRAM}	Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wakeup ⁽¹⁾		3 V		10		μs
t _{WAKE-UP LPM0}	Wake-up time from LPM0 to active mode ⁽¹⁾		3 V		200 + 2.5 / f _{DCO}		ns
t _{WAKE-UP LPM3}	Wake-up time from LPM3 to active mode ⁽²⁾		3 V		10		μs
t _{WAKE-UP LPM4}	Wake-up time from LPM4 to active mode		3 V		10		μs
t _{WAKE-UP LPM3.5}	Wake-up time from LPM3.5 to active mode ⁽²⁾		3 V		350		μs
t _{WAKE-UP LPM4.5}	Wake-up time from LPM4.5 to active mode ⁽²⁾	SVSHE = 1	3 V		350		μs
		SVSHE = 0			1		ms
t _{WAKE-UP-RESET}	Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽²⁾		3 V		1		ms
t _{RESET}	Pulse duration required at $\overline{\text{RST}}$ /NMI pin to accept a reset		3 V		2		μs

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
- (2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

5.11.3 Clock Specifications

Table 5-4 lists the characteristics of the LF XT1.

Table 5-4. XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{XT1, LF}	XT1 oscillator crystal, low frequency	LFXTBYPASS = 0			32768		Hz
DC _{XT1, LF}	XT1 oscillator LF duty cycle	Measured at MCLK, f _{LFXT} = 32768 Hz		30%		70%	
f _{XT1, SW}	XT1 oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 ⁽³⁾⁽⁴⁾			32.768		kHz
DC _{XT1, SW}	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		40%		60%	
OA _{LFXT}	Oscillation allowance for LF crystals ⁽⁵⁾	LFXTBYPASS = 0, LFXTDRIVE = {3}, f _{LFXT} = 32768 Hz, C _{L,eff} = 12.5 pF			200		kΩ
C _{L,eff}	Integrated effective load capacitance ⁽⁶⁾	See ⁽⁷⁾			1		pF
t _{START, LFXT}	Start-up time ⁽⁸⁾	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF			1000		ms
f _{Fault, LFXT}	Oscillator fault frequency ⁽⁹⁾	XTS = 0 ⁽¹⁰⁾		0		3500	Hz

- (1) To improve EMI on the LFXT oscillator, observe the following guidelines:
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) See [MSP430 32-kHz Crystal Oscillators](#) for details on crystal section, layout, and testing.
- (3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by DC_{LFXT, SW}.
- (4) Maximum frequency of operation of the entire device cannot be exceeded.
- (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For LFXTDRIVE = {0}, C_{L,eff} = 3.7 pF
 - For LFXTDRIVE = {1}, 6 pF ≤ C_{L,eff} ≤ 9 pF
 - For LFXTDRIVE = {2}, 6 pF ≤ C_{L,eff} ≤ 10 pF
 - For LFXTDRIVE = {3}, 6 pF ≤ C_{L,eff} ≤ 12 pF
- (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
- (7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
- (8) Includes start-up counter of 1024 clock cycles.
- (9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.
- (10) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the frequency characteristics of the FLL.

Table 5-5. DCO FLL, Frequency

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{DCO, FLL}	FLL lock frequency, 16 MHz, 25°C	Measured at MCLK, Internal trimmed REFO as reference	3 V	–1.0%		1.0%	
	FLL lock frequency, 16 MHz, –40°C to 105°C		3 V	–3.0%		3.0%	
	FLL lock frequency, 16 MHz, –40°C to 105°C	Measured at MCLK, XT1 crystal as reference	3 V	–0.5%		0.5%	

Table 5-5. DCO FLL, Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{DUTY} Duty cycle	Measured at MCLK, XT1 crystal as reference	3 V	40%	50%	60%	
Jitter _{cc} Cycle-to-cycle jitter, 16 MHz		3 V		0.25%		
Jitter _{long} Long term jitter, 16 MHz		3 V		0.022%		
t _{FLL, lock} FLL lock time, 16MHz		3 V		200		ms

Table 5-6 lists the characteristics of the DCO.

Table 5-6. DCO Frequency

over recommended operating free-air temperature (unless otherwise noted) (see [Figure 5-6](#))

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
f _{DCO, 16MHz} DCO frequency, 16 MHz	DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	8.5	MHz
	DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		13.9	
	DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		20	
	DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		32.7	
f _{DCO, 12MHz} DCO frequency, 12 MHz	DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	6.4	MHz
	DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		10.5	
	DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		15.4	
	DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		24.8	
f _{DCO, 8MHz} DCO frequency, 8 MHz	DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	4.3	MHz
	DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		7.1	
	DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		10.4	
	DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		16.9	
f _{DCO, 4MHz} DCO frequency, 4 MHz	DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	2.1	MHz
	DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		3.5	
	DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		5.2	
	DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		8.5	
f _{DCO, 2MHz} DCO frequency, 2 MHz	DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	1.1	MHz
	DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		1.8	
	DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		2.6	
	DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		4.3	

Table 5-6. DCO Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted) (see [Figure 5-6](#))

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
f _{DCO, 1MHz}	DCO frequency, 1 MHz	DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0	3 V	0.5	MHz
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511		0.9	
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0		1.3	
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511		2.2	

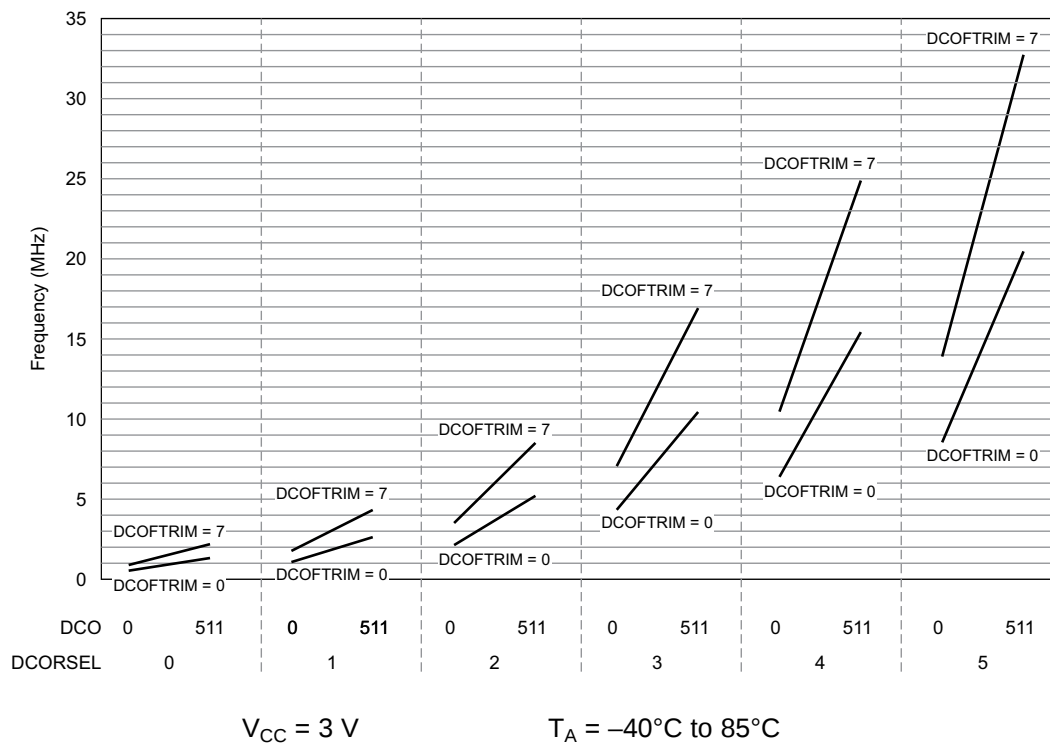


Figure 5-6. Typical DCO Frequency

Table 5-7 lists the characteristics of the REFO.

Table 5-7. REFO

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{REFO}	REFO oscillator current consumption	T _A = 25°C	3 V	1			μA
f _{REFO}	REFO calibrated frequency	Measured at MCLK	3 V	32768			Hz
	REFO absolute calibrated tolerance	−40°C to 105°C	1.8 V to 3.6 V	−3.5%	+3.5%		
df _{REFO} /dT	REFO frequency temperature drift	Measured at MCLK ⁽¹⁾	3 V	0.01			%/°C
df _{REFO} /dV _{CC}	REFO frequency supply voltage drift	Measured at MCLK at 25°C ⁽²⁾	1.8 V to 3.6 V	1			%/V
f _{DC}	REFO duty cycle	Measured at MCLK	1.8 V to 3.6 V	40%	50%	60%	
t _{START}	REFO start-up time	40% to 60% duty cycle		50			μs

(1) Calculated using the box method: $(\text{MAX}(-40^{\circ}\text{C to } 105^{\circ}\text{C}) - \text{MIN}(-40^{\circ}\text{C to } 105^{\circ}\text{C})) / \text{MIN}(-40^{\circ}\text{C to } 105^{\circ}\text{C}) / (105^{\circ}\text{C} - (-40^{\circ}\text{C}))$

(2) Calculated using the box method: $(\text{MAX}(1.8 \text{ V to } 3.6 \text{ V}) - \text{MIN}(1.8 \text{ V to } 3.6 \text{ V})) / \text{MIN}(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

Table 5-8 lists the characteristics of the VLO.

Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
f _{VLO} VLO frequency	Measured at MCLK	3 V	10	kHz
df _{VLO} /dT VLO frequency temperature drift	Measured at MCLK ⁽¹⁾	3 V	0.5	%/°C
df _{VLO} /dV _{CC} VLO frequency supply voltage drift	Measured at MCLK ⁽²⁾	1.8 V to 3.6 V	4	%/V
f _{VLO,DC} Duty cycle	Measured at MCLK	3 V	50%	

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

NOTE

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-8).

Table 5-9 lists the characteristics of the MODOSC.

Table 5-9. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{MODOSC} MODOSC frequency		3 V	3.0	3.8	4.6	MHz
f _{MODOSC} /dT MODOSC frequency temperature drift		3 V		0.102		%/°C
f _{MODOSC} /dV _{CC} MODOSC frequency supply voltage drift		1.8 V to 3.6 V		1.17		%/V
f _{MODOSC,DC} Duty cycle		3 V	40%	50%	60%	

5.11.4 Digital I/Os

Table 5-10 lists the characteristics of the digital inputs.

Table 5-10. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+} Positive-going input threshold voltage		2 V	0.90		1.50	V
		3 V	1.35		2.25	
V _{IT-} Negative-going input threshold voltage		2 V	0.50		1.10	V
		3 V	0.75		1.65	
V _{hys} Input voltage hysteresis (V _{IT+} – V _{IT-})		2 V	0.3		0.8	V
		3 V	0.4		1.2	
R _{Pull} Pullup or pulldown resistor	For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _{I,dig} Input capacitance, digital only port pins	V _{IN} = V _{SS} or V _{CC}			3		pF
C _{I,ana} Input capacitance, port pins with shared analog functions	V _{IN} = V _{SS} or V _{CC}			5		pF
I _{lkg(Px.y)} High-impedance leakage current of GPIO Pins	See ⁽¹⁾ ⁽²⁾	2 V, 3 V	–20		20	nA
t _(int) External interrupt timing (external trigger pulse duration to set interrupt flag) ⁽³⁾	Ports with interrupt capability (see block diagram and terminal function descriptions)	2 V, 3 V	50			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Table 5-11 lists the characteristics of the digital outputs.

Table 5-11. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = –3 mA ⁽¹⁾	2 V	1.4		2.0	V
	I _(OHmax) = –5 mA ⁽¹⁾	3 V	2.4		3.0	
V _{OL} Low-level output voltage	I _(OLmax) = 3 mA ⁽¹⁾	2 V	0.0		0.60	V
	I _(OHmax) = 5 mA ⁽¹⁾	3 V	0.0		0.60	
f _{Port_CLK} Clock output frequency	C _L = 20 pF ⁽²⁾	2 V	16			MHz
		3 V	16			
t _{rise,dig} Port output rise time, digital only port pins	C _L = 20 pF	2 V		10		ns
		3 V		7		
t _{fall,dig} Port output fall time, digital only port pins	C _L = 20 pF	2 V		10		ns
		3 V		5		

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

5.11.4.1 Typical Characteristics – Outputs at 3 V and 2 V

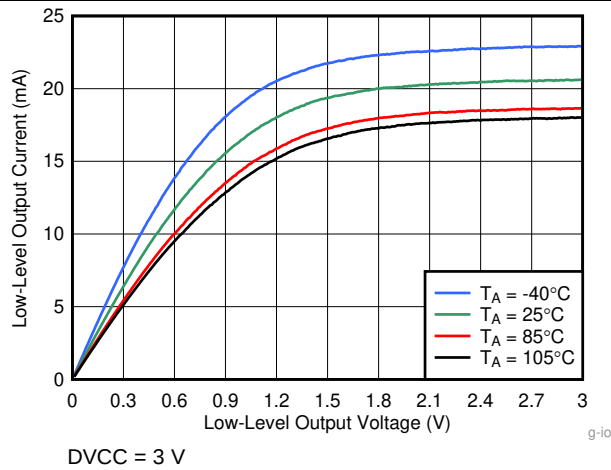


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

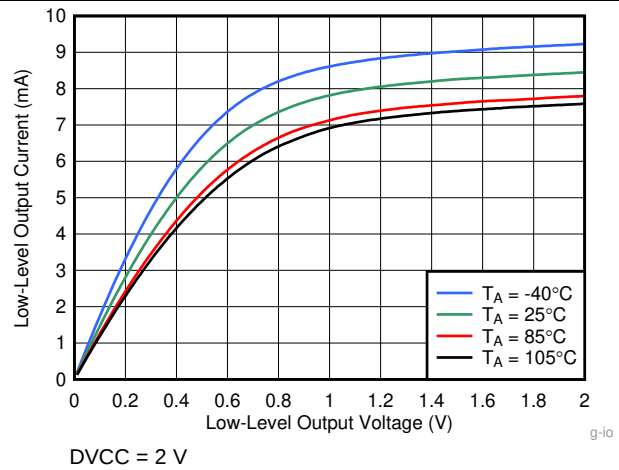


Figure 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

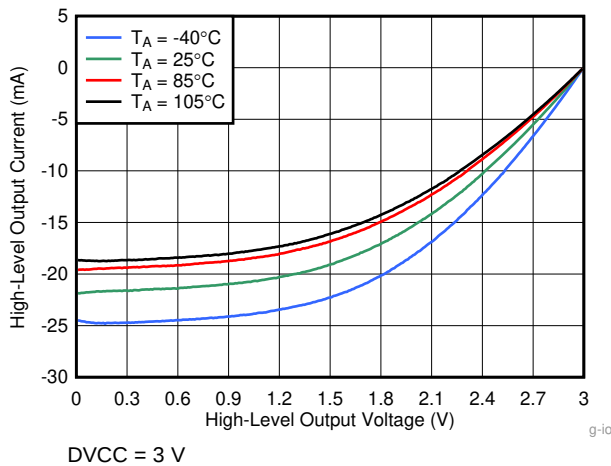


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

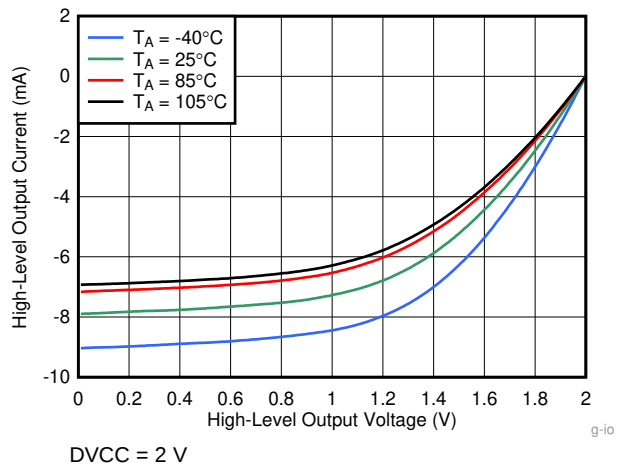


Figure 5-10. Typical High-Level Output Current vs High-Level Output Voltage

5.11.5 Internal Shared Reference

Table 5-12 lists the characteristics of the internal shared reference.

Table 5-12. Internal Shared Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{SENSOR}	Temperature sensor voltage	T _J = 30°C	2.0 V, 3.0 V		788		mV
TC _{SENSOR}	Temperature sensor coefficient	T _J = 30°C			2.5		mV/°C
V _{eCOMP, LP}	Low-power threshold for eCOMP	T _J = 30°C	2.0 V, 3.0 V		1.20		V
V _{REF+, 1.2V Output}	Positive built-in reference output at VREF+ pin with 1-mA load current to ground	EXTREFEN = 1 with 1-mA load current	2.0 V, 3.0 V	1.16	1.20	1.24	V
TC _{REF+, 1.2V}	Temperature coefficient of VREF+ = 1.2 V built-in reference	EXTREFEN = 1 with 1-mA load current	3.0 V		30		μV/°C
The following parameters are for the 1.5-V, 2.0-V, and 2.5-V internal reference only and cannot be output to the VREF+ pin.							
V _{REF+, 1.5V, 2.0V, 2.5V}	Positive built-in reference voltage as internal reference	REFVSEL = {2} for 2.5 V, INTREFEN = 1	3.0 V		2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, INTREFEN = 1	2.5 V		2.0	±1.5%	
		REFVSEL = {0} for 1.5 V, INTREFEN = 1	2.0 V		1.5	±1.8%	
Noise	RMS noise at VREF ⁽¹⁾	From 0.1 Hz to 10 Hz, REFVSEL = {0}			30	130	μV
DV _{CC(min)}	DVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V			1.8		V
		REFVSEL = {1} for 2.0 V			2.2		
		REFVSEL = {2} for 2.5 V			2.7		
I _{REF+}	Operating supply current into DVCC terminal ⁽²⁾	INTREFEN = 1	3 V		19	26	μA
I _{REF+_ADC_BUF}	Operating supply current into AVCC terminal ⁽²⁾	ADC ON, REFVSEL = {0, 1, 2}	3 V		247	400	μA
I _{O(VREF+)}	VREF (1.5V, 2.0V, 2.5V) maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, INTREFEN = 1	3 V		-1000	+10	μA
ΔV _{out} / ΔI _o (VREF+)	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, I _{O(VREF+)} = +10 μA or -1000 μA AVCC = AVCC(min) for each reference level, INTREFEN = 1	3 V			1500	μV/mA
C _{VREF+/-}	Capacitance at VREF+ and VREF- terminals	INTREFEN = 1	3 V		0	100	pF
TC _{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, INTREFEN = 1, T _A = -40°C to 105°C ⁽³⁾	3 V		24	50	ppm/K
PSRR_DC	Power supply rejection ratio (DC)	AV _{CC} = AV _{CC} (min) to AV _{CC} (max), T _A = 25°C REFVSEL = {0, 1, 2}, INTREFEN = 1	3 V		100	420	μV/V
PSRR_AC	Power supply rejection ratio (AC)	ΔAV _{CC} = 0.1 V at 1 kHz	3 V		3.0		mV/V

(1) The internal reference noise affects ADC performance when the ADC uses the internal reference.

(2) The internal reference current is supplied through the AVCC terminal.

(3) Calculated using the box method: (MAX(-40°C to 105°C) – MIN(-40°C to 105°C)) / (MIN(-40°C to 105°C) / (105°C – (-40°C)))

Table 5-12. Internal Shared Reference (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{SETTLE}	Settling time of reference voltage ⁽⁴⁾	AV _{CC} = AV _{CC} (min) to AV _{CC} (max), REFVSEL = {0, 1, 2}, INTREFEN = 0 → 1	3 V	75	100	μs

(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.11.6 Timer_A and Timer_B

Table 5-13 lists the characteristics of Timer_A. Table 5-14 lists the characteristics of Timer_B.

Table 5-13. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10%	2 V, 3 V	16	MHz
t _{TA,cap}	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	2 V, 3 V	20	ns

Table 5-14. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ±10%	2 V, 3 V	16	MHz
t _{TB,cap}	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2 V, 3 V	20	ns

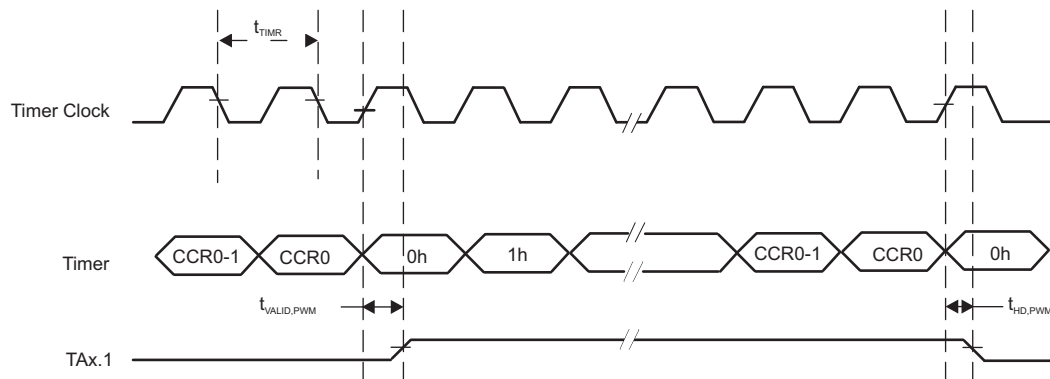
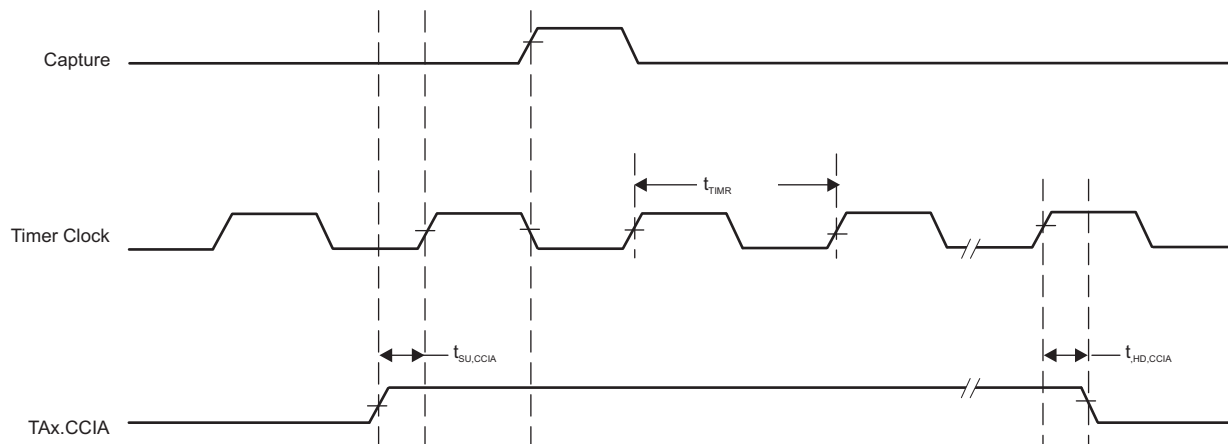


Figure 5-11. Timer PWM Mode

**Figure 5-12. Timer Capture Mode**

5.11.7 eUSCI

Table 5-15 lists the supported frequencies of the eUSCI in UART mode.

Table 5-15. eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{eUSCI} eUSCI input clock frequency	Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10%	2 V, 3 V		16	MHz
f _{BITCLK} BITCLK clock frequency (equals baud rate in Mbaud)		2 V, 3 V		5	MHz

Table 5-16 lists the characteristics of the eUSCI in UART mode.

Table 5-16. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
t _t UART receive deglitch time ⁽¹⁾	UCGLITx = 0	2 V, 3 V	12	ns
	UCGLITx = 1		40	
	UCGLITx = 2		68	
	UCGLITx = 3		110	

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-17 lists the supported frequencies of the eUSCI in SPI master mode.

Table 5-17. eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f _{eUSCI} eUSCI input clock frequency	Internal: SMCLK, MODCLK Duty cycle = 50% ±10%		8	MHz

Table 5-18 lists the characteristics of the eUSCI in SPI master mode.

Table 5-18. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _{STE,LEAD} STE lead time, STE active to clock	UCSTEM = 0, UCMODEx = 01 or 10		1		UCxCLK cycles
	UCSTEM = 1, UCMODEx = 01 or 10				
t _{STE,LAG} STE lag time, last clock to STE inactive	UCSTEM = 0, UCMODEx = 01 or 10		1		UCxCLK cycles
	UCSTEM = 1, UCMODEx = 01 or 10				
t _{SU,MI} SOMI input data setup time		2 V	58		ns
		3 V	40		
t _{HD,MI} SOMI input data hold time		2 V	0		ns
		3 V	0		
t _{VALID,MO} SIMO output data valid time ⁽²⁾	UCLK edge to SIMO valid, C _L = 20 pF	2 V		20	ns
		3 V		20	
t _{HD,MO} SIMO output data hold time ⁽³⁾	C _L = 20 pF	2 V	-3		ns
		3 V	-3		

- (1) f_{UCxCLK} = 1/2t_{LO/HI} with t_{LO/HI} = max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave)). For the slave parameters t_{SU,SI}(Slave) and t_{VALID,SO}(Slave), see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 5-13 and Figure 5-14.

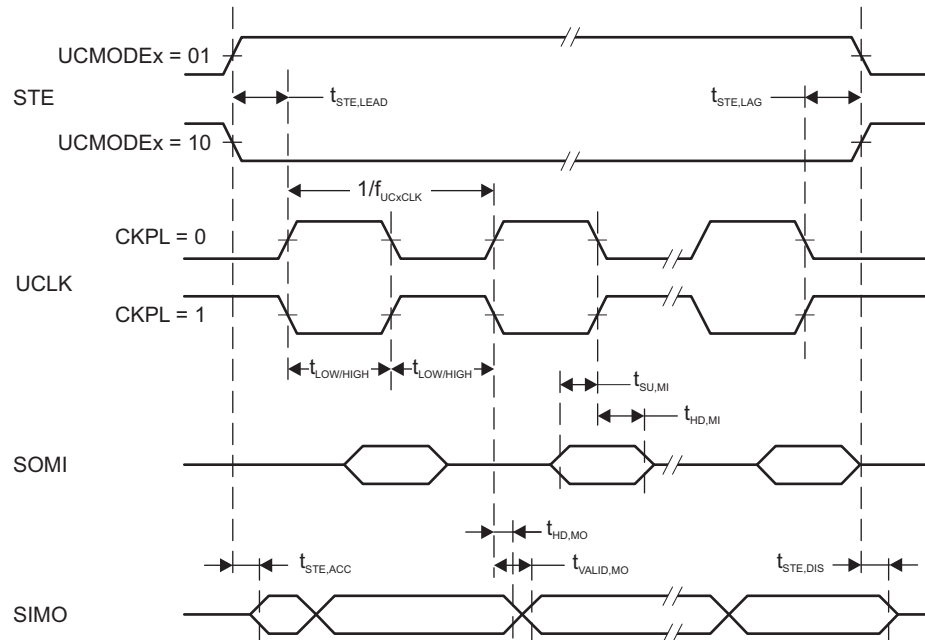


Figure 5-13. SPI Master Mode, CKPH = 0

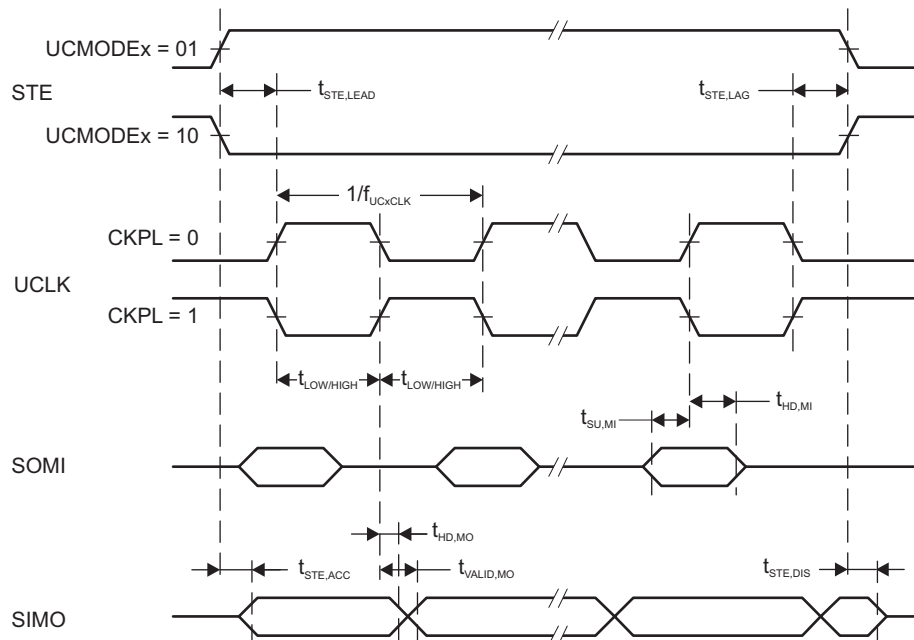


Figure 5-14. SPI Master Mode, CKPH = 1

Table 5-19 lists the characteristics of the eUSCI in SPI slave mode.

Table 5-19. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE active to clock		2 V	55		ns
			3 V	45		
t _{STE,LAG}	STE lag time, Last clock to STE inactive		2 V	20		ns
			3 V	20		
t _{STE,ACC}	STE access time, STE active to SOMI data out		2 V		65	ns
			3 V		40	
t _{STE,DIS}	STE disable time, STE inactive to SOMI high impedance		2 V		40	ns
			3 V		35	
t _{SU,SI}	SIMO input data setup time		2 V	15		ns
			3 V	6		
t _{HD,SI}	SIMO input data hold time		2 V	12		ns
			3 V	12		
t _{VALID,SO}	SOMI output data valid time ⁽²⁾	UCLK edge to SOMI valid, C _L = 20 pF	2 V		71	ns
			3 V		42	
t _{HD,SO}	SOMI output data hold time ⁽³⁾	C _L = 20 pF	2 V	5		ns
			3 V	5		

- (1) $f_{UCXCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-15](#) and [Figure 5-16](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-15](#) and [Figure 5-16](#).

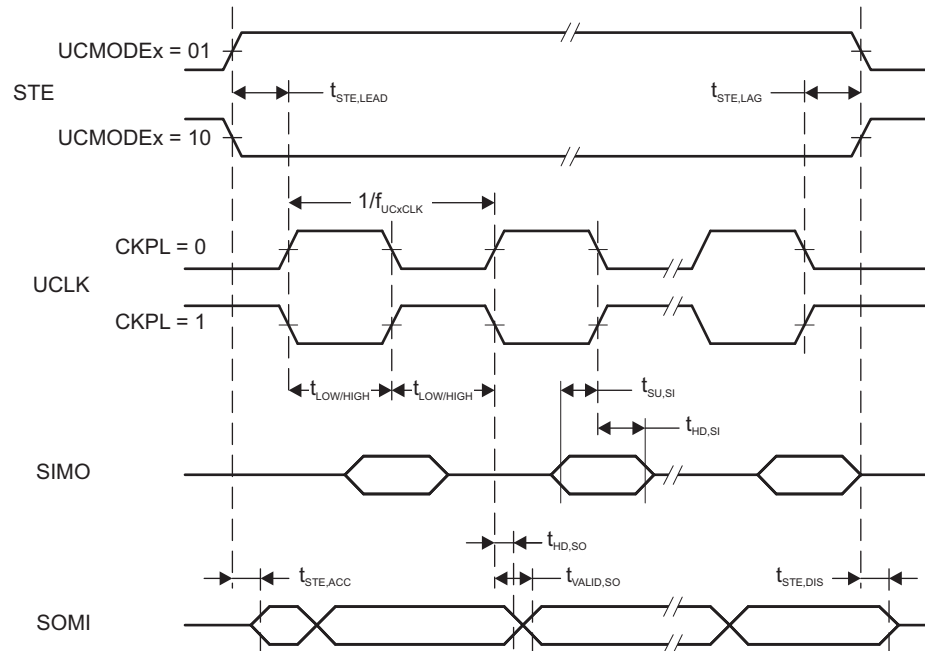


Figure 5-15. SPI Slave Mode, CKPH = 0

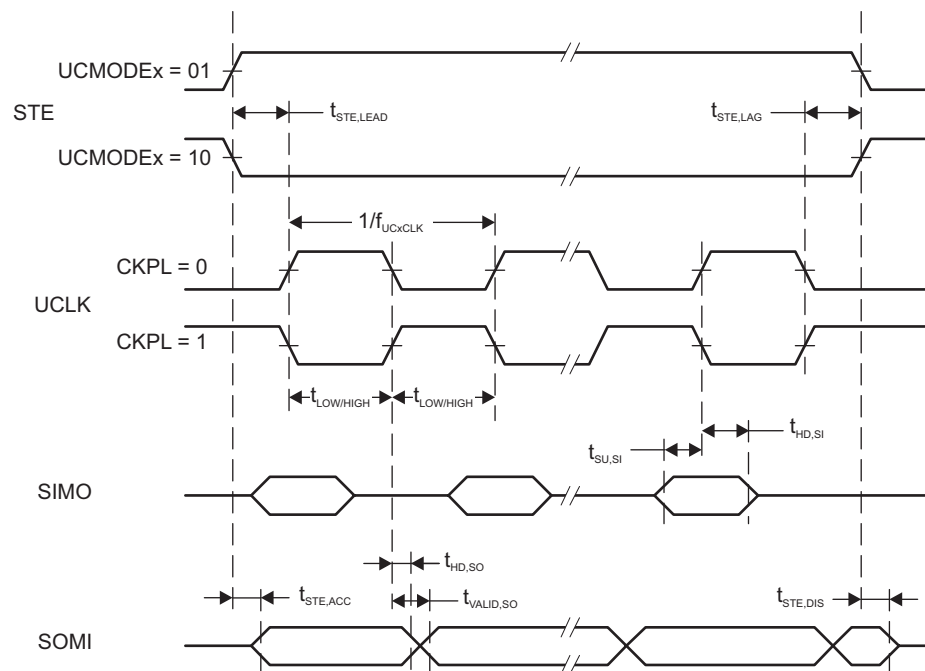


Figure 5-16. SPI Slave Mode, CKPH = 1

Table 5-20 lists the characteristics of the eUSCI in I²C mode.

Table 5-20. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-17)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{eUSCI} eUSCI input clock frequency	Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10%				16	MHz
f _{SCL} SCL clock frequency		2 V, 3 V	0		400	kHz
t _{HD,STA} Hold time (repeated) START	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	2 V, 3 V	4.0 0.6			μs
t _{SU,STA} Setup time for a repeated START	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	2 V, 3 V	4.7 0.6			μs
t _{HD,DAT} Data hold time		2 V, 3 V	0			ns
t _{SU,DAT} Data setup time		2 V, 3 V	250			ns
t _{SU,STO} Setup time for STOP	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	2 V, 3 V	4.0 0.6			μs
t _{SP} Pulse duration of spikes suppressed by input filter	UCGLITx = 0 UCGLITx = 1 UCGLITx = 2 UCGLITx = 3	2 V, 3 V	50 25 12.5 6.3		600 300 150 75	ns
t _{TIMEOUT} Clock low time-out	UCCLTOx = 1 UCCLTOx = 2 UCCLTOx = 3	2 V, 3 V		27 30 33		ms

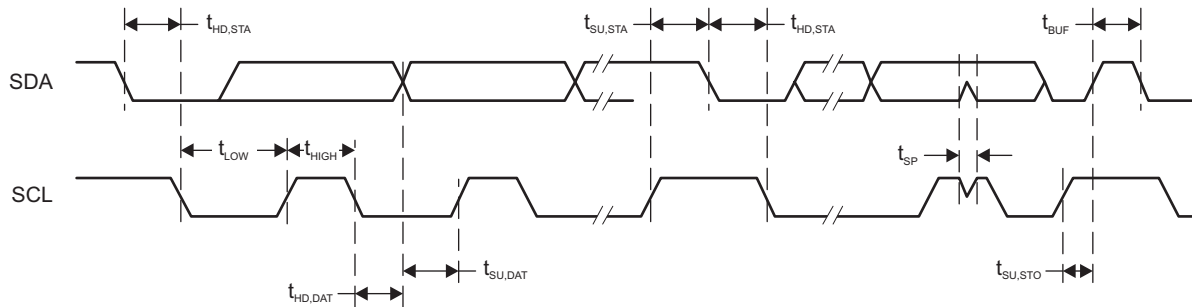


Figure 5-17. I²C Mode Timing

5.11.8 ADC

Table 5-21 lists the input characteristics of the ADC.

Table 5-21. ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
DV _{CC} ADC supply voltage			2.0		3.6	V
V _(Ax) Analog input voltage range	All ADC pins		0		DV _{CC}	V
I _{ADC} Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode	f _{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b	2.0 V		220		μA
		3.0 V		277		
C _I Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad	2.2 V		4.5	5.5	pF
R _I Input MUX ON resistance	DV _{CC} = 2 V, 0 V ≤ V _{Ax} ≤ DV _{CC}				2	kΩ

Table 5-22 lists the timing parameters of the ADC.

Table 5-22. ADC, Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADCCLK}	For specified performance of ADC linearity parameters, 10-bit mode	2.4 V to 3.6 V		6		MHz
	For specified performance of ADC linearity parameters, 12-bit mode	2.4 V to 3.6 V		4.4		
t _{CONVERT} Conversion time	External f _{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0	2.4 V to 3.6 V		(1)		μs
t _{ADCON} Turn-on settling time of the ADC	The error in a conversion started after t _{ADCON} is less than ±0.5 LSB, Reference and input signal already settled				100	ns
t _{Sample} Sampling time	R _S = 1000 Ω, R _I = 20000 Ω, C _I = 5.5 pF, C _{EXT} = 8 pF, Approximately 7.62 Tau (t) are required for an error of less than ±0.5 LSB, 10-bit mode. ⁽²⁾	2.4 V to 3.6 V	0.52			μs
	R _S = 1000 Ω, R _I = 40000 Ω, C _I = 5.5 pF, C _{EXT} = 8 pF, Approximately 9.01 Tau (t) are required for an error of less than ±0.5 LSB, 12-bit mode. ⁽²⁾	2.4 V to 3.6 V	0.61			

(1) $(n + 2) \times 1/f_{ADCCLK}$, n = ADC resolution (8, 10, 12)

(2) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

Table 5-23 lists the linearity parameters of the ADC.

Table 5-23. ADC, Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I	Integral linearity error (12-bit mode)	V _{ref+} reference	2.4 V to 3.6 V	–2.5		2.5	LSB
	Integral linearity error (10-bit mode)	V _{ref+} reference	2.4 V to 3.6 V	–2		2	
E _D	Differential linearity error (12-bit mode)	V _{ref+} reference	2.4 V to 3.6 V	–1		1.5	LSB
	Differential linearity error (10-bit mode)	V _{ref+} reference	2.4 V to 3.6 V	–1		1.5	
E _O	Offset error (12-bit mode)	V _{ref+} reference, TLV calibration data can be used to improve the parameter ⁽¹⁾	2.4 V to 3.6 V	–4.0		4.0	mV
	Offset error (10-bit mode)	V _{ref+} reference, TLV calibration data can be used to improve the parameter ⁽¹⁾	2.4 V to 3.6 V	–4.0		4.0	
E _G	Gain error (12-bit mode)	V _{ref+} as reference, TLV calibration data can be used to improve the parameter ⁽¹⁾	2.4 V to 3.6 V	–9.0		9.0	LSB
	Gain error (10-bit mode)	V _{ref+} as reference, TLV calibration data can be used to improve the parameter ⁽¹⁾	2.4 V to 3.6 V	–3.0		3.0	LSB
E _T	Total unadjusted error (12-bit mode)	V _{ref+} as reference, TLV calibration data can be used to improve the parameter ⁽¹⁾	2.4 V to 3.6 V	–5.0		5.0	LSB
	Total unadjusted error (10-bit mode)	V _{ref+} as reference, TLV calibration data can be used to improve the parameter ⁽¹⁾	2.4 V to 3.6 V	–2.0		2.0	LSB

- (1) For details, see the device descriptor in the [MP430FR4xx and MP430FR2xx Family User's Guide](#), and see [Designing With the MP430FR4xx and MP430FR2xx ADC](#) for details on optimizing ADC performance for your application with the choice of internal or external reference.

5.11.9 Enhanced Comparator (eCOMP)

Table 5-24 lists the characteristics of eCOMP0.

Table 5-24. eCOMP0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	2.0		3.6	V
V_{IC}	Common mode input range	0		V_{CC}	V
V_{HYS}	DC input hysteresis	CPEN = 1, CPHSEL = 00		0	mV
		CPEN = 1, CPHSEL = 01		10	
		CPEN = 1, CPHSEL = 10		20	
		CPEN = 1, CPHSEL = 11		30	
V_{OFFSET}	Input offset voltage	CPEN = 1, CPMSEL = 0		–30	mV
		CPEN = 1, CPMSEL = 1		–40	
I_{COMP}	Quiescent current draw from V_{CC} , only comparator	$V_{IC} = V_{CC}/2$, CPEN = 1, CPMSEL = 0		24	μA
		$V_{IC} = V_{CC}/2$, CPEN = 1, CPMSEL = 1		1.6	
C_{IN}	Input channel capacitance ⁽¹⁾		1		pF
R_{IN}	Input channel series resistance	On (switch closed)		10	k Ω
		Off (switch open)		50	
t_{PD}	Propagation delay, response time	CPMSEL = 0, CPFLT = 0, Overdrive = 20 mV		1	μs
		CPMSEL = 1, CPFLT = 0, Overdrive = 20 mV		3.2	
t_{EN_CP}	Comparator enable time	CPEN = 0→1, CPMSEL = 0, V+ and V- from pads, Overdrive = 20 mV		10.91	μs
		CPEN = 0→1, CPMSEL = 1, V+ and V- from pads, Overdrive = 20 mV		36.78	
$t_{EN_CP_DAC}$	Comparator with reference DAC enable time	CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 0, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV		11	μs
		CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 1, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV		36.82	
t_{FDLY}	Propagation delay with analog filter active	CPMSEL = 0, CPFLTDY = 00, Overdrive = 20 mV, CPFLT = 1		0.7	μs
		CPMSEL = 0, CPFLTDY = 01, Overdrive = 20 mV, CPFLT = 1		1.1	
		CPMSEL = 0, CPFLTDY = 10, Overdrive = 20 mV, CPFLT = 1		1.9	
		CPMSEL = 0, CPFLTDY = 11, Overdrive = 20 mV, CPFLT = 1		3.4	
INL	Integral nonlinearity		–0.5	0.5	LSB
DNL	Differential nonlinearity		–0.5	0.5	LSB

(1) See Figure 5-18 for eCOMP C_{IN} model. Figure 5-18

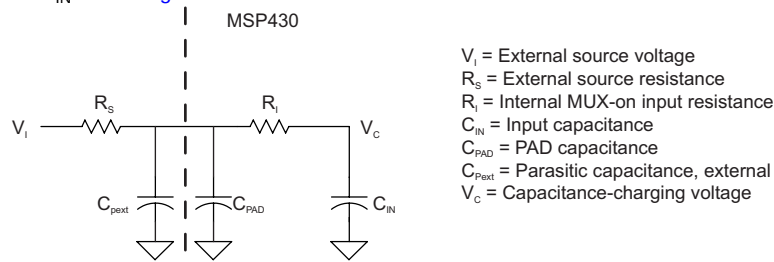


Figure 5-18. eCOMP Input Circuit

5.11.10 FRAM

Table 5-25 lists the characteristics of the FRAM.

Table 5-25. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Read and write endurance		10 ¹⁵			cycles
t _{Retention} Data retention duration	T _J = 25°C	100			years
	T _J = 70°C	40			
	T _J = 95°C	10			
	T _J = 115°C	10			
I _{WRITE} Current to write into FRAM			I _{READ} ⁽¹⁾		nA
I _{ERASE} Erase current			N/A ⁽²⁾		nA
t _{WRITE} Write time			t _{READ} ⁽³⁾		ns
t _{READ} Read time	NWAITSx = 0		1 / f _{SYSTEM} ⁽⁴⁾		ns
	NWAITSx = 1		2 / f _{SYSTEM} ⁽⁴⁾		

- (1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption parameter I_{AM,FRAM}.
- (2) FRAM does not require a special erase sequence.
- (3) Writing into FRAM is as fast as reading.
- (4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

5.11.11 Debug and Emulation

Table 5-26 lists the characteristics of the 4-wire and Spy-Bi-Wire JTAG interface.

Table 5-26. JTAG, 4-Wire and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	V _{CC}	MIN	TYP	MAX	UNIT
f _{SBW} Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		8	MHz
t _{SBW,Low} Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	μs
t _{SBW,En} Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾	2.2 V, 3.0 V			100	μs
t _{SBW,Rst} Spy-Bi-Wire return to normal operation time		15		100	μs
f _{TCK} TCK input frequency, 4-wire JTAG ⁽²⁾	2.2 V	0		10	MHz
	3.0 V	0		10	MHz
R _{internal} Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	kΩ
f _{TCLK} TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f _{SYSTEM})				16	MHz
t _{TCLK,Low/High} TCLK low or high clock pulse duration, no FRAM access				25	ns
f _{TCLK,FRAM} TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f _{SYSTEM} with no FRAM wait states)				4	MHz
t _{TCLK,FRAM,Low/High} TCLK low or high clock pulse duration, including FRAM accesses				100	ns

- (1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the t_{SBW,En} time after the first transition of the TEST/SBW/TCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The MSP430FR247x is an ultra-low-power MCU. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in, for example, portable measurement applications. The MCU features five 16-bit timers, four eUSCs that support UART, SPI, and I²C, a hardware multiplier, an RTC module, and a high-performance 12-bit ADC, an enhanced comparator with built in 6-bit DAC for internal voltage reference .

6.2 CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be handled with all instructions.

6.3 Operating Modes

The MSP430 has one active mode and several software-selectable low-power modes of operation (see [Table 6-1](#)). An interrupt event can wake the MCU from low-power mode LPM0, LPM3 or LPM4, service the request, and restore the MCU back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

NOTE

XT1CLK and VLOCLK can be active during LPM4 mode if requested by low-frequency peripherals, such as RTC and WDT.

Table 6-1. Operating Modes

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE (FRAM ON)	CPU OFF	STANDBY	OFF	ONLY RTC	SHUTDOWN
Maximum system clock		16 MHz	16 MHz	40 kHz	0	40 kHz	0
Power consumption at 25°C, 3 V		135 μ A/MHz	40 μ A/MHz	1.48 μ A with RTC counter only in LFXT	0.74 μ A without SVS	0.66 μ A with RTC counter only in LFXT	41 nA without SVS
Wake-up time		N/A	Instant	10 μ s	10 μ s	350 μ s	350 μ s
Wake-up events		N/A	All	All	I/O	RTC or I/O	I/O
Power	Regulator	Full regulation	Full regulation	Partial power down	Partial power down	Partial power down	Power down
	SVS	On	On	Optional	Optional	Optional	Optional
	Brownout	On	On	On	On	On	On
Clock ⁽¹⁾	MCLK	Active	Off	Off	Off	Off	Off
	SMCLK	Optional	Optional	Off	Off	Off	Off
	FLL	Optional	Optional	Off	Off	Off	Off
	DCO	Optional	Optional	Off	Off	Off	Off
	MODCLK	Optional	Optional	Off	Off	Off	Off
	REFO	Optional	Optional	Optional	Off	Off	Off
	ACLK	Optional	Optional	Optional	Off	Off	Off
	XT1CLK	Optional	Optional	Optional	Off	Optional	Off
Core	VLOCLK	Optional	Optional	Optional	Off	Optional	Off
	CPU	On	Off	Off	Off	Off	Off
	FRAM	On	On	Off	Off	Off	Off
	RAM	On	On	On	On	Off	Off
Peripherals	Backup memory ⁽²⁾	On	On	On	On	On	Off
	Timer0_A3	Optional	Optional	Optional	Off	Off	Off
	Timer1_A3	Optional	Optional	Optional	Off	Off	Off
	Timer2_A3	Optional	Optional	Optional	Off	Off	Off
	Timer3_A3	Optional	Optional	Optional	Off	Off	Off
	Timer0_B7	Optional	Optional	Optional	Off	Off	Off
	WDT	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A0	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A1	Optional	Optional	Optional	Off	Off	Off
	eUSCI_B0	Optional	Optional	Optional	Off	Off	Off
	eUSCI_B1	Optional	Optional	Optional	Off	Off	Off
	CRC	Optional	Optional	Off	Off	Off	Off
	ADC	Optional	Optional	Optional	Off	Off	Off
	RTC	Optional	Optional	Optional	Off	Optional	Off
I/O	GPIO	On	Optional	State held	State held	State held	State held

(1) The status shown for LPM4 applies to internal clocks only.

(2) Backup memory contains 32 bytes of register space in peripheral memory. See [Table 6-32](#) and [Table 6-54](#) for its memory allocation.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-2](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, Brownout, Supply supervisor External reset RST Watchdog time-out, key violation FRAM uncorrectable bit error detection Software POR, BOR FLL unlock error	SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLUNLOCKIFG	Reset	FFFEh	63, Highest
System NMI Vacant memory access JTAG mailbox FRAM access time error FRAM bit error detection	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG	Nonmaskable	FFFCh	62
User NMI External NMI Oscillator fault	NMIIFG OFIFG	Nonmaskable	FFFAh	61
Timer0_A3	TA0CCR0 CCIFG0	Maskable	FFF8h	60
Timer0_A3	TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)	Maskable	FFF6h	59
Timer1_A3	TA1CCR0 CCIFG0	Maskable	FFF4h	58
Timer1_A3	TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV)	Maskable	FFF2h	57
Time2_A3	TA2CCR0 CCIFG0	Maskable	FFF0h	56
Timer2_A3	TA2CCR1 CCIFG1, TA2CCR2 CCIFG2, TA2IFG (TA2IV)	Maskable	FFEEh	55
Timer3_A3	TA3CCR0 CCIFG0	Maskable	FFECCh	54
Timer3_A3	TA3CCR1 CCIFG1, TA3CCR2 CCIFG2, TA3IFG (TA3IV)	Maskable	FFEAh	53
Timer0_B7	TB0CCR0 CCIFG0	Maskable	FFE8h	52
Timer0_B7	TB0CCR1 CCIFG1, TB0CCR2 CCIFG2, TB0CCR3 CCIFG3, TB0CCR4 CCIFG4, TB0CCR5 CCIFG5, TB0CCR6 CCIFG6, TB0IFG (TB0IV)	Maskable	FFE6h	51
RTC	RTCIFG	Maskable	FFE4h	50
Watchdog timer interval mode	WDTIFG	Maskable	FFE2h	49
eUSCI_A0 receive or transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV)	Maskable	FFE0h	48
eUSCI_A1 receive or transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV)	Maskable	FFDEh	47
eUSCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB0IV)	Maskable	FFDCh	46

Table 6-2. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB0IV)	Maskable	FFDAh	45
ADC	ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV)	Maskable	FFD8h	44
P1	P1IFG.0 to P1IFG.7 (P1IV)	Maskable	FFD6h	43
P2	P2IFG.0 to P2IFG.7 (P2IV)	Maskable	FFD4h	42
P3	P3IFG.0 to P2IFG.7 (P3IV)	Maskable	FFD2h	41
P4	P4IFG.0 to P4IFG.7 (P4IV)	Maskable	FFD0h	40
P5	P5IFG.0 to P5IFG.7 (P5IV)	Maskable	FFCEh	39
P6	P6IFG.0 to P6IFG.2 (P6IV)	Maskable	FFCCh	38
eCOMP0	CPIIFG, CPIFG (CP0IV)	Maskable	FFCAh	37, Lowest
Reserved	Reserved	Maskable	FFC6h–FF88h	

Table 6-3. Signatures

SIGNATURE	WORD ADDRESS
BSL I2C Address ⁽¹⁾	0FFA0h
BSL Config	0FF8Ah
BSL Config Signature	0FF88h
BSL Signature2	0FF86h
BSL Signature1	0FF84h
JTAG Signature2	0FF82h
JTAG Signature1	0FF80h

(1) 7-bit address BSL I²C interface

6.5 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using either the UART serial interface or the I²C interface. Access to the MCU memory through the BSL is protected by a user-defined password. Use of the BSL requires four pins (see [Table 6-4](#) and [Table 6-5](#)). The BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and $\text{TEST}/\text{SBWTCK}$ pins. This device can support the blank device detection automatically to invoke the BSL with bypass this special entry sequence for saving time and on board programmable. For the complete description of the feature of the BSL, see the [MSP430FR4xx and MSP430FR2xx Bootloader \(BSL\) User's Guide](#).

Table 6-4. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
$\text{TEST}/\text{SBWTCK}$	Entry sequence signal
P1.4	Data transmit
P1.5	Data receive
VCC	Power supply
VSS	Ground supply

Table 6-5. I²C BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
$\text{TEST}/\text{SBWTCK}$	Entry sequence signal
P1.2	Data transmit and receive
P1.3	Clock
VCC	Power supply
VSS	Ground supply

6.6 JTAG Standard Interface

The MSP low-power microcontrollers support the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The $\text{TEST}/\text{SBWTCK}$ pin enables the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. [Table 6-6](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For details on using the JTAG interface, see [MSP430 Programming With the JTAG Interface](#).

Table 6-6. JTAG Pin Requirements and Function

DEVICE SIGNAL	DIRECTION	JTAG FUNCTION
P1.4/.../TCK	IN	JTAG clock input
P1.5/.../TMS	IN	JTAG state control
P1.6/.../TDI/TCLK	IN	JTAG data input, TCLK input
P1.7/.../TDO	OUT	JTAG data output
$\text{TEST}/\text{SBWTCK}$	IN	Enable JTAG pins
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN	External reset
DVCC	–	Power supply
DVSS	–	Ground supply

6.7 Spy-Bi-Wire Interface (SBW)

The MSP low-power microcontrollers support the 2-wire SBW interface. SBW can be used to interface with MSP development tools and device programmers. [Table 6-7](#) lists the SBW interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For details on using the SBW interface, see the [MSP430 Programming With the JTAG Interface](#).

Table 6-7. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SBW FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN, OUT	Spy-Bi-Wire data input and output
DVCC	–	Power supply
DVSS	–	Ground supply

6.8 FRAM

The FRAM can be programmed using the JTAG port, SBW, the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

6.9 Memory Protection

The device features memory protection for user access authority and write protection, including options to:

- Secure the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Enable write protection to prevent unwanted write operation to FRAM contents by setting the control bits in the System Configuration 0 register. For detailed information, see the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10.1 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as [Equation 1](#) by using ADC sampling 1.5-V reference without any external components support.

$$\text{DVCC} = (1023 \times 1.5 \text{ V}) \div 1.5\text{-V reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered, when EXTREFEN = 1 on PMMCTL2 register, and it can be output to P1.4/./A1/VREF+ , meanwhile the ADC channel 1 can also be selected to monitor this voltage. For more detailed information, see the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

6.10.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and an on-chip asynchronous high-speed clock (MODOSC). The clock system is designed for cost-effective designs with minimal external components. A fail-safe mechanism is included for XT1. The clock system module offers the following clock signals.

- **Main Clock (MCLK):** The system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- **Sub-Main Clock (SMCLK):** The subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- **Auxiliary Clock (ACLK):** This clock is derived from the external XT1 clock, internal VLO or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. [Table 6-8](#) lists the clock distribution used in this device.

Table 6-8. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	XT1CLK	VLOCLK	EXTERNAL PIN
Frequency range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	5 MHz $\pm 10\%$	DC to 40 kHz	10 kHz $\pm 50\%$	–
CPU	N/A	Default	–	–	–	–	–	–
FRAM	N/A	Default	–	–	–	–	–	–
RAM	N/A	Default	–	–	–	–	–	–
CRC	N/A	Default	–	–	–	–	–	–
MPY32	N/A	Default	–	–	–	–	–	–
I/O	N/A	Default	–	–	–	–	–	–
TA0	TASSEL	–	10b	01b	–	–	11b	00b (TA0CLK pin)
TA1	TASSEL	–	10b	01b	–	–	–	00b (TA1CLK pin)
TA2	TASSEL	–	10b	01b	–	–	11b	00b (TA2CLK pin)
TA3	TASSEL	–	10b	01b	–	–	–	00b (TA3CLK pin)
TB0	TBSSEL	–	10b	01b	–	–	–	00b (TB0CLK pin)
eUSCI_A0	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCA0CLK pin)
eUSCI_A1	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCA1CLK pin)
eUSCI_B0	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCB0CLK pin)
eUSCI_B1	UCSSEL	–	10b or 11b	01b	–	–	–	00b (UCB1CLK pin)
WDT	WDTSEL	–	00b	01b	–	–	10b	–
ADC	ADCSEL	–	10b or 11b	01b	00b	–	–	–
RTC	RTCSS	–	01b ⁽¹⁾	01b ⁽¹⁾	–	10b	11b	–

(1) Controlled by the RTCKSEL bit in the SYSCFG2 register.

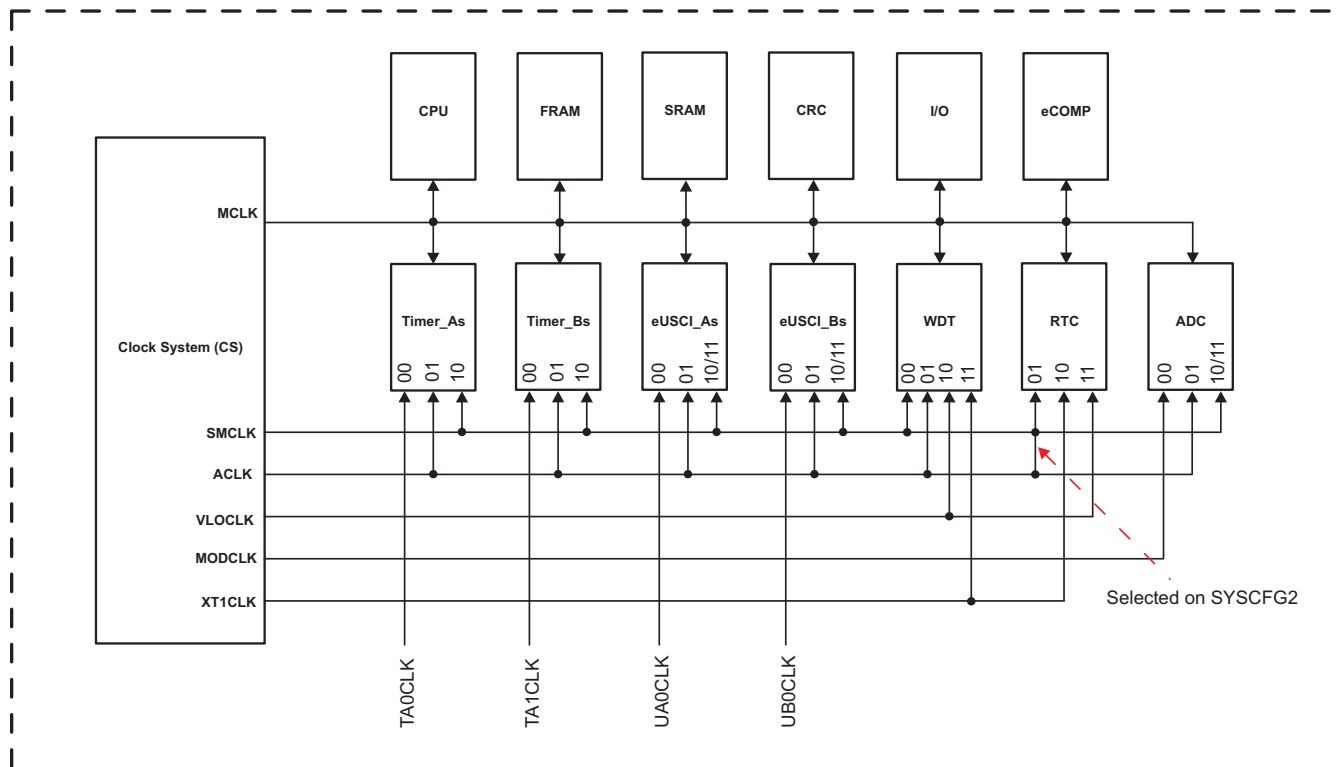


Figure 6-1. Clock Distribution Block Diagram

6.10.3 General-Purpose Input/Output Port (I/O)

Up to 43 I/O ports are implemented.

- P1/P3/P4/P5 implements 8 bits, P2 implements 6 excluding the IO multiplexed with XIN/XOUT, P6 implements 3 bits,
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPMx.5 wake-up input capability are available for all GPIOs (up to 43)
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise as a pair.

NOTE

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. [Table 6-9](#) lists the system clocks that can be used to source the WDT.

Table 6-9. WDT Clocks

WDTSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	Reserved

6.10.5 System (SYS) Module

The SYS module handles many of the system functions within the device. These features include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application. [Table 6-10](#) summarizes the interrupts that are managed by the SYS module.

Table 6-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	015Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$ /NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		FLL unlock (PUC)	24h	
		Reserved	22h, 26h to 3Eh	Lowest

Table 6-10. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSSNIV, System NMI	015Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah	
		Reserved	0Ch	
		Reserved	0Eh	
		Reserved	10h	
		VMAIFG vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	015Ah	No interrupt pending	00h	
		NMIIFG NMI pin or SVS _H event	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h to 1Eh	Lowest

6.10.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

6.10.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I²C communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA. The eUSCI_A and eUSCI_B are connected either from P1 port or P2 port, it can be selected from the USCIRAMP of SYSCFG3 or USCIBRMP bit of SYSCFG2. [Table 6-11](#) lists the pin configurations that are required for each eUSCI mode.

Table 6-11. eUSCI Pin Configurations

eUSCI_A0	PIN (PxSEL Selection)	UART	SPI
	P1.4 ⁽¹⁾	TXD	SIMO
	P1.5 ⁽¹⁾	RXD	SOMI
	P1.6 ⁽¹⁾	–	SCLK
	P1.7 ⁽¹⁾	–	STE
	PIN (PxSEL Selection)	UART	SPI
	P5.2 ⁽²⁾	TXD	SIMO
	P5.1 ⁽²⁾	RXD	SOMI
	P5.0 ⁽²⁾	–	SCLK
	P4.7 ⁽²⁾	–	STE

- (1) This is the remapped default functionality controlled by the USCIBRMP or USCIRAMP bit of the SYSCFG2 or SYSCFG3 register. Only one selected port is valid at any time.
- (2) This is the remapped functionality controlled by the USCIBRMP or USCIRAMP bit of the SYSCFG2 or SYSCFG3 register. Only one selected port is valid at any time.

Table 6-11. eUSCI Pin Configurations (continued)

eUSCI_A1	PIN (PxSEL Selection)	UART	SPI
	P2.6	TXD	SIMO
	P2.5	RXD	SOMI
	P2.4	–	SCLK
	P3.1	–	STE
eUSCI_B0	PIN (PxSEL Selection)	I ² C	SPI
	P1.0 ⁽¹⁾	–	STE
	P1.1 ⁽¹⁾	–	SCLK
	P1.2 ⁽¹⁾	SDA	SIMO
	P1.3 ⁽¹⁾	SCL	SOMI
	PIN (PxSEL Selection)	I ² C	SPI
	P5.6 ⁽²⁾	–	STE
	P5.5 ⁽²⁾	–	SCLK
	P4.6 ⁽²⁾	SDA	SIMO
	P4.5 ⁽²⁾	SCL	SOMI
eUSCI_B1	PIN (PxSEL Selection)	I ² C	SPI
	P2.7 ⁽¹⁾	–	STE
	P3.5 ⁽¹⁾	–	SCLK
	P3.2 ⁽¹⁾	SDA	SIMO
	P3.6 ⁽¹⁾	SCL	SOMI
	PIN (PxSEL Selection)	I ² C	SPI
	P5.4 ⁽²⁾	–	STE
	P5.3 ⁽²⁾	–	SCLK
	P4.4 ⁽²⁾	SDA	SIMO
	P4.3 ⁽²⁾	SCL	SOMI

6.10.8 Timers (TA0, TA1, TA2, TA3 and TB0)

The TA0, TA1, TA2 and TA3 modules are 16-bit timers and counters with three capture/compare registers each. Each timer supports multiple captures or compares, PWM outputs, and interval timing (see [Table 6-12](#) and [Table 6-13](#)). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both TA0 and TA2 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up mode, they can be used to set the overflow value of the counter.

Table 6-12. Timer0_A0 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P1.0	TA0CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	VLO (internal)	INCLK			
	ACLK (internal)	CCI0A	CCR0	TA0	Not used
	VLO (internal)	CCI0B			Timer1_A1 CCI0B input
	DVSS	GND			
	DVCC	V _{CC}			
P1.1	TA0.1	CCI1A	CCR1	TA1	TA0.1
	RTC (internal)	CCI1B			Timer1_A1 CCI1B input
	DVSS	GND			
	DVCC	V _{CC}			
P1.2	TA0.2	CCI2A	CCR2	TA2	TA0.2
	N/A	CCI2B			Timer1_A1 INCLK Timer1_A1 CCI2B input, IR carrier input
	DVSS	GND			
	DVCC	V _{CC}			

Table 6-13. Timer0_A1 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P1.6	TA1CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer0_A3 CCR2B output (internal)	INCLK			
	N/A	CCI0A	CCR0	TA0	Not used
	Timer0_A3 CCR0B output (internal)	CCI0B			Not used
	DVSS	GND			
	DVCC	V _{CC}			
P1.5	TA1.1	CCI1A	CCR1	TA1	TA1.1
	Timer0_A3 CCR1B output (internal)	CCI1B			To ADC trigger
	DVSS	GND			
	DVCC	V _{CC}			
P1.4	TA1.2	CCI2A	CCR2	TA2	TA1.2
	Timer0_A3 CCR2B output (internal)	CCI2B			IR coding input
	DVSS	GND			
	DVCC	V _{CC}			

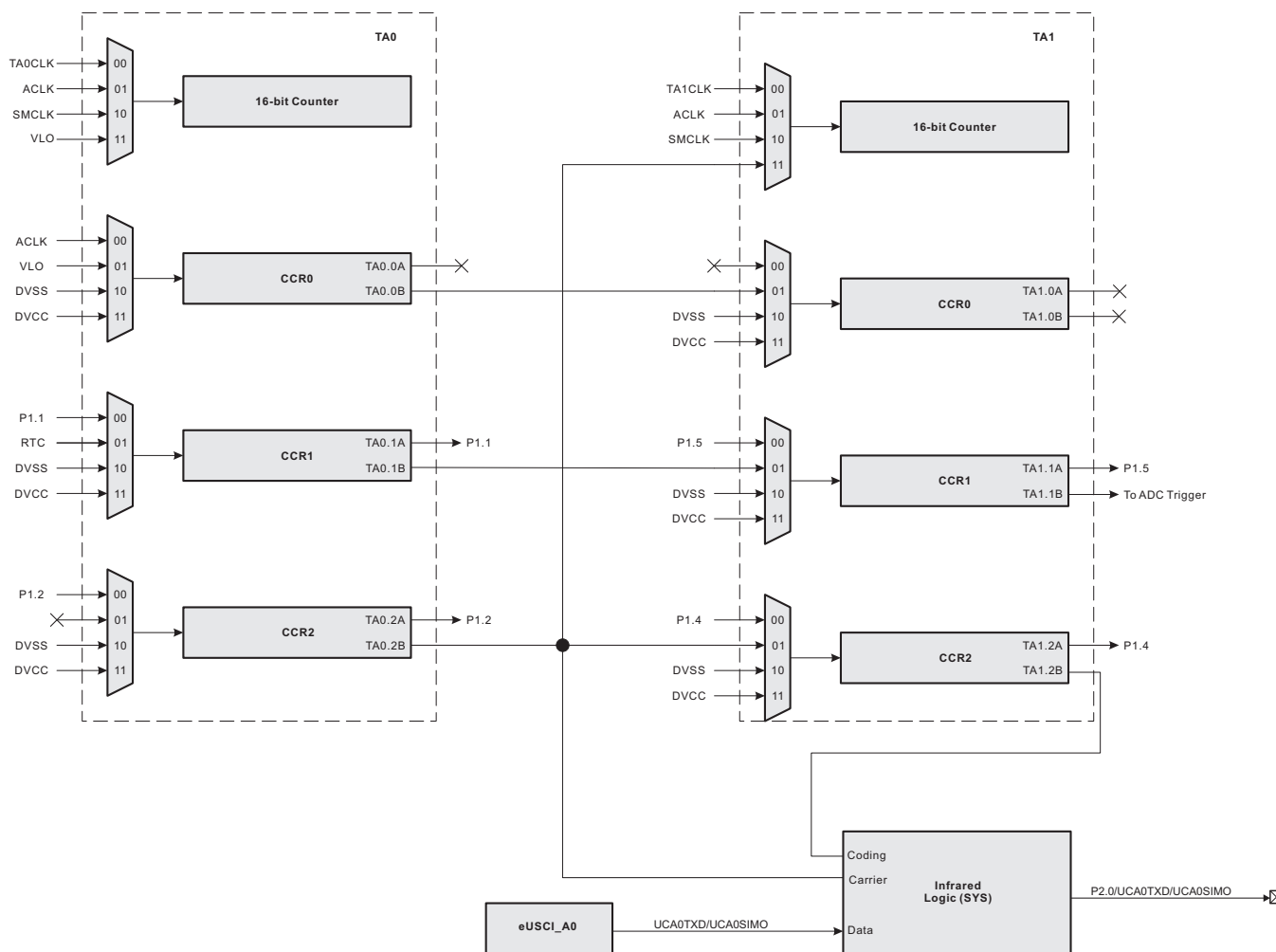


Figure 6-2. TA0 and TA1 Signal Connections

Table 6-14. Timer2_A3 and Timer3_A3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P3.4	TA2CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	VLO (internal)	INCLK			
P2.3	TA2.0	CCI0A	CCR0	TA0	TA2.0
	VLO (internal)	CCI0B			Timer3_A3 CCI0B input
	DVSS	GND			
	DVCC	V _{CC}			
P3.3	TA2.1	CCI1A	CCR1	TA1	TA2.1
	RTC (internal)	CCI1B			Timer3_A3 CCI1B input
	DVSS	GND			
	DVCC	V _{CC}			
P3.0	TA2.2	CCI2A	CCR2	TA2	TA2.2
	N/A	CCI2B			Timer3_A3 CCI2B input
	DVSS	GND			
	DVCC	V _{CC}			
P4.2	TA3CLK	TACLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	Timer2_A3 CCR2B output (internal)	INCLK			
P4.1	TA3.0	CCI0A	CCR0	TA0	TA3.0
	Timer2_A3 CCR0B output (internal)	CCI0B			Timer3_B0 CCI0B input
	DVSS	GND			
	DVCC	V _{CC}			
P4.0	TA3.1	CCI1A	CCR1	TA1	TA3.1
	Timer2_A3 CCR1B output (internal)	CCI1B			Timer3_B0 CCI1B input
	DVSS	GND			
	DVCC	V _{CC}			
P3.7	TA3.2	CCI2A	CCR2	TA2	TA3.2
	Timer2_A3 CCR2B output (internal)	CCI2B			Timer3_B0 CCI2B input
	DVSS	GND			
	DVCC	V _{CC}			

Table 6-15. Timer0_B7 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P6.1	TB0CLK	TBCLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	N/A	INCLK			
P6.2	TB0.0	CCI0A	CCR0	TB0	TB0.0
	Timer3_A3 CCI0B input (internal)	CCI0B			
	DVSS	GND			
	DVCC	V _{CC}			
P4.7	TB0.1	CCI1A	CCR1	TB1	TB0.1
	Timer3_A3 CCI1B input (internal)	CCI1B			
	DVSS	GND			
	DVCC	V _{CC}			
P5.0	TB0.2	CCI2A	CCR2	TB2	TB0.2
	Timer3_A3 CCI2B input (internal)	CCI2B			
	DVSS	GND			
	DVCC	V _{CC}			
P5.1	TB0.3	CCI1A	CCR3	TB3	TB0.3
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V _{CC}			
P5.2	TB0.4	CCI1A	CCR4	TB4	TB0.4
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V _{CC}			
P4.3	TB0.5	CCI1A	CCR5	TB5	TB0.5
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V _{CC}			
P4.4	TB0.6	CCI1A	CCR6	TB6	TB0.6
	N/A	CCI1B			
	DVSS	GND			
	DVCC	V _{CC}			

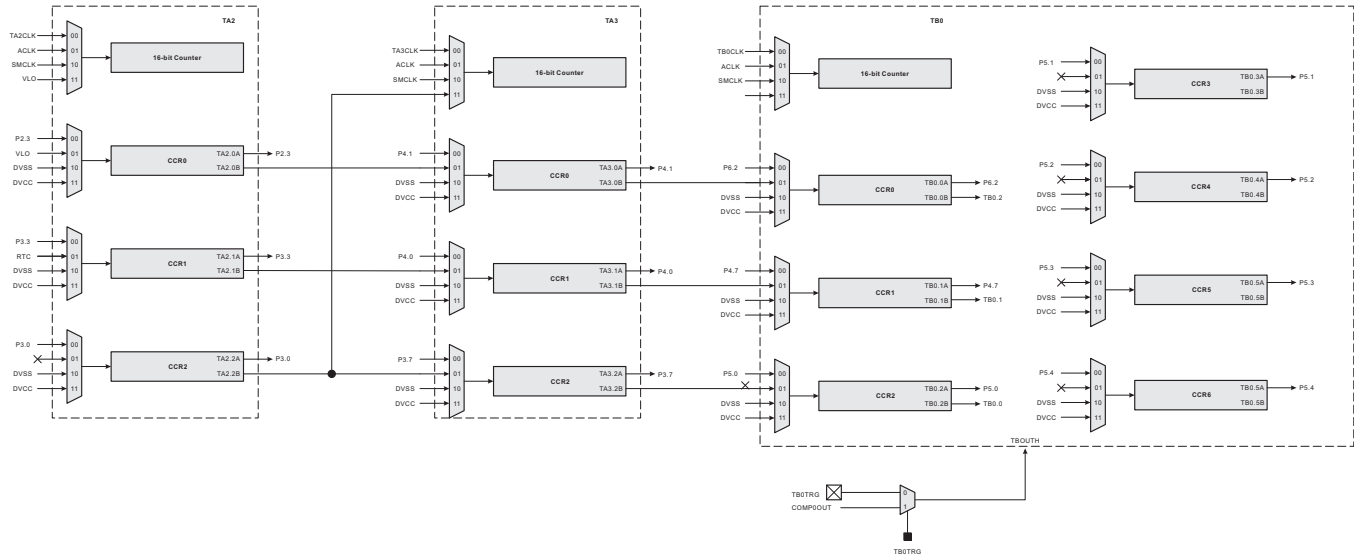


Figure 6-3. TA2, TA3 and TB0 Signal Connections

Table 6-16. TA2 and TA3 Pin Configurations of Remap Functionality

	PIN (PxSEL Selection)	DEVICE INPUT/OUTPUT SIGNAL
TA2	P3.4 ⁽¹⁾	TA2CLK
	P2.3 ⁽¹⁾	TA2.0
	P3.3 ⁽¹⁾	TA2.1
	P3.0 ⁽¹⁾	TA2.2
	PIN (PxSEL Selection)	DEVICE INPUT/OUTPUT SIGNAL
	P5.5 ⁽²⁾	TA2CLK
	P5.6 ⁽²⁾	TA2.0
	P5.7 ⁽²⁾	TA2.1
	P6.0 ⁽²⁾	TA2.2
TA3	PIN (PxSEL Selection)	DEVICE INPUT/OUTPUT SIGNAL
	P4.2 ⁽¹⁾	TA3CLK
	P4.1 ⁽¹⁾	TA3.0
	P4.0 ⁽¹⁾	TA3.1
	P3.7 ⁽¹⁾	TA3.2
	PIN (PxSEL Selection)	DEVICE INPUT/OUTPUT SIGNAL
	P5.4 ⁽²⁾	TA3CLK
	P5.3 ⁽²⁾	TA3.0
	P4.6 ⁽²⁾	TA3.1
	P4.5 ⁽²⁾	TA3.2

(1) This is the remapped default functionality controlled by the TARMP bit of the SYSCFG3 register. Only one selected port is valid at any time.

(2) This is the remapped functionality controlled by the TARMP bit of the SYSCFG3 register. Only one selected port is valid at any time.

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

The Timer_B module feature the function to put Timer_B all outputs into a high impedance state when the selected source is triggered. The source can be selected from external pin or internal of the device, it is controlled by TBxTRG in SYS. For more information, see the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

Table 6-17 lists the Timer_B high-impedance trigger source selections.

Table 6-17. TB0OUTH Selection

TB0TRGSEL	TB0OUTH TRIGGER SOURCE SELECTION	Timer_B PAD OUTPUT HIGH IMPEDANCE
TB0TRGSEL = 0	eCOMP0 output (internal)	P6.2, P4.7, P5.0, P5.1, P5.2, P4.3, P4.4
TB0TRGSEL = 1	P3.5	

6.10.9 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The MPY module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

6.10.10 Backup Memory (BAKMEM)

The BAKMEM supports data retention during LPM3.5. This device provides up to 32 bytes that are retained during LPM3.5.

6.10.11 Real-Time Clock (RTC)

The RTC is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3 and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. RTC also can be sourced from ACLK controlled by RTCKSEL in SYSCFG2. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_B3 CCI1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

Table 6-18. RTC Clock Source

RTCSS	CLOCK SOURCE
00	Reserved
01	SMCLK, or ACLK is selected
10	XT1CLK
11	VLOCLK

6.10.12 12-Bit Analog-to-Digital Converter (ADC)

The 12-bit ADC module supports fast 12-bit analog-to-digital conversions with single-ended input. The module implements a 12-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 12 external inputs and four internal inputs (see [Table 6-19](#)).

Table 6-19. ADC Channel Connections

ADCINCHx	ADC CHANNELS	EXTERNAL PIN OUTPUT
0	A0/V _{ref} +	P1.0
1	A1/	P1.1
2	A2/V _{ref} -	P1.2
3	A3	P1.3
4	A4 ⁽¹⁾	P1.4
5	A5	P1.5
6	A6	P1.6
7	A7	P1.7
8	A8	P4.3
9	A9	P4.4
10	A10	P5.3
11	A11	P5.4
12	On-chip temperature sensor	N/A
13	Internal shared reference voltage (1.5, 2.0, or 2.5-V)	N/A
14	DVSS	N/A
15	DVCC	N/A

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be measured by channel A4.

The analog-to-digital conversion can be started by software or a hardware trigger. [Table 6-20](#) shows the trigger sources that are available.

Table 6-20. ADC Trigger Signal Connections

ADC SHSx		TRIGGER SOURCE
BINARY	DECIMAL	
00	0	ADCSC bit (software trigger)
01	1	RTC event
10	2	TA1.1B
11	3	eCOMP0 COUT

6.10.13 eCOMP0

This device features one enhanced comparator. The enhanced comparator is an analog voltage comparator with a built-in 6-bit DAC as an internal voltage reference. The integrated 6-bit DAC can be set to 64 steps for the comparator reference voltage. This module has 4-level programmable hysteresis and configurable power modes: high-power and low-power modes.

The eCOMP0 supports a propagation delay up to 1 μ s in high-power mode. In low-power mode, eCOMP0 supports 3.2- μ s delay with 1.5- μ A leakage at room temperature, which can be an ideal wake-up source in LPM3 for a voltage monitor.

eCOMP0 contains a programmable 6-bit DAC that can use the internal shared reference (1.5 V, 2.0 V, or 2.5 V) for a high-precision comparison threshold. In addition to the internal shared reference, a low-power 1.2-V reference is fixed at channel 2 of both the inverting and noninverting paths and allows the DAC to be turned off to reduce power consumption.

The eCOMP0 supports external inputs and internal inputs (see [Table 6-21](#)) and outputs (see [Table 6-22](#))

Table 6-21. eCOMP0 Input Channel Connections

CPPSEL OR CPNSSEL	eCOMP0 CHANNELS
000	P1.1/.../COMP0.0
001	P2.2/.../COMP0.1
010	Low-power 1.2-V reference
011	P5.7/.../COMP0.2
100	P6.0/.../COMP0.3
101	N/A
110	eCOMP0 6-bit DAC

Table 6-22. eCOMP0 Output Channel Connections

ECOMP0 OUT	EXTERNAL PINOUT, MODULE
1	P3.4
2	TB0 (TB0OUTH), TB1 (TB1OUTH), ADC trigger

6.10.14 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level
- EEM version: S

6.11 Input/Output Diagrams

Figure 6-4 shows the overall port diagram.

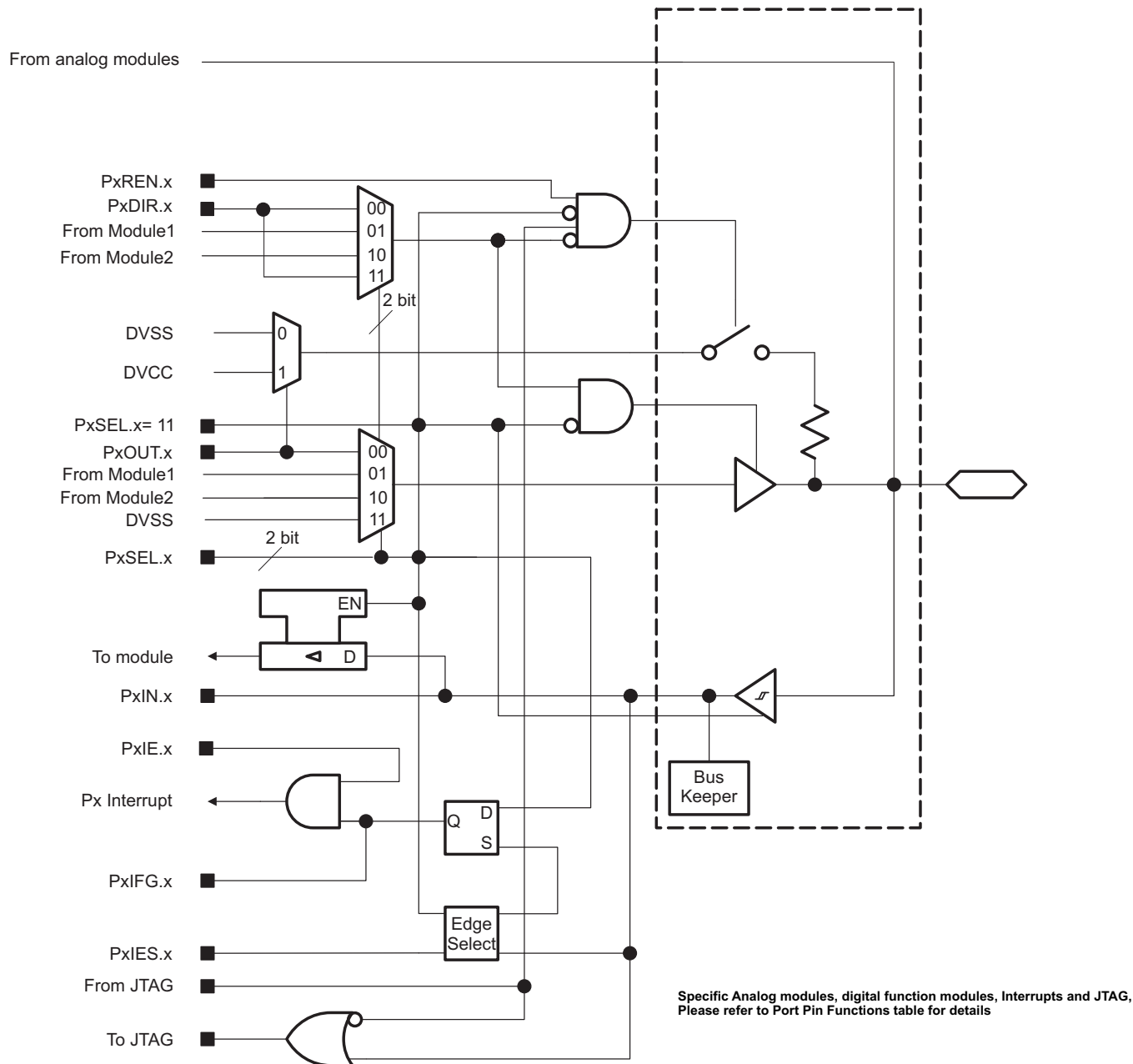


Figure 6-4. Port Input/Output With Schmitt Trigger

6.11.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Table 6-23 summarizes the selection of the pin functions.

Table 6-23. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾		
			P1DIR.x	P1SELx	JTAG
P1.0/UCB0STE/TA0CLK/A0/Veref+	0	P1.0 (I/O)	I: 0; O: 1	00	0
		UCB0STE	X	01	0
		TA0CLK	0	10	0
		A0, Veref+	X	11	N/A
P1.1/UCB0CLK/TA0.1/COMP0.0/A1	1	P1.1 (I/O)	I: 0; O: 1	00	0
		UCB0CLK	X	01	0
		TA0.CCI1A	0	10	0
		TA0.1	1		
		A1, COMP0.0	X	11	N/A
P1.2/UCB0SIMO/UCB0SDA/TA0.2/A2/Veref-	2	P1.2 (I/O)	I: 0; O: 1	00	0
		UCB0SIMO/UCB0SDA	X	01	0
		TA0.CCI2A	0	10	0
		TA0.2	1		
		A2, Veref-	X	11	N/A
P1.3/UCB0SOMI/UCB0SCL/MCLK/A3	3	P1.3 (I/O)	I: 0; O: 1	00	0
		UCB0SOMI/UCB0SCL	X	01	0
		MCLK	1	10	0
		A3	X	11	N/A
P1.4/UCATXD/UCASIMO/TA1.2/TCK/A4/VREF+	4	P1.4 (I/O)	I: 0; O: 1	00	Disabled
		UCATXD/UCASIMO	X	01	Disabled
		TA1.CCI2A	0	10	Disabled
		TA1.2	1		
		A4, VREF+	X	11	Disabled
		JTAG TCK	X	X	TCK
P1.5/UCARXD/UCASOMI/TA1.1/TMS/A5	5	P1.5 (I/O)	I: 0; O: 1	00	Disabled
		UCARXD/UCASOMI	X	01	Disabled
		TA1.CCI1A	0	10	Disabled
		TA1.1	1		
		A5	X	11	Disabled
		JTAG TMS	X	X	TMS
P1.6/UCACLK/TA1CLK/TDI/TCLK/A6	6	P1.6 (I/O)	I: 0; O: 1	00	Disabled
		UCACLK	X	01	Disabled
		TA1CLK	0	10	Disabled
		A6	X	11	Disabled
		JTAG TDI/TCLK	X	X	TDI/TCLK
P1.7/UCASTE/SMCLK/TDO/A7	7	P1.7 (I/O)	I: 0; O: 1	00	Disabled
		UCASTE	X	01	Disabled
		SMCLK	1	10	Disabled
		A7	X	11	Disabled
		JTAG TDO	X	X	TDO

(1) X = don't care

6.11.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Table 6-24 summarizes the selection of the pin functions.

Table 6-24. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾	
			P2DIR.x	P2SELx
P2.0/XOUT	0	P2.0 (I/O)	I: 0; O: 1	00
		XOUT	X	01
P2.1/XIN	1	P2.1 (I/O)	I: 0; O: 1	00
		XIN	X	01
P2.2/ACLK/COMP0.1	2	P2.2 (I/O)	I: 0; O: 1	00
		ACLK	1	10
		COMP0.1	X	11
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	00
		TA2.CCI0A	0	01
		TA2.0	1	
P2.4/UCA1CLK	4	P2.4 (I/O)	I: 0; O: 1	00
		UCA1CLK	X	01
P2.5/UCA1RXD/UCA1SOMI	5	P2.5 (I/O)	I: 0; O: 1	00
		UCA1RXD/UCA1SOMI	X	01
P2.6/UCA1TXD/UCA1SIMO	6	P2.6 (I/O)	I: 0; O: 1	00
		UCA1TXD/UCA1SIMO	X	01
P2.7/UCB1STE	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB1STE	X	01

(1) X = don't care

6.11.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Table 6-25 summarizes the selection of the pin functions.

Table 6-25. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾	
			P3DIR.x	P3SEL.x
P3.0/TA2.2	0	filter9	I: 0; O: 1	00
		TA2.CCI2A	0	01
		TA2.2	1	
P3.1/UC1STE	1	P3.1 (I/O)	I: 0; O: 1	00
		UC1STE	X	01
P3.2/UCB1SIMO/UCB1SDA	2	P3.2 (I/O)	I: 0; O: 1	00
		UCB1SIMO/UCB1SDA	X	01
P3.3/TA2.1	3	P3.3 (I/O)	I: 0; O: 1	00
		TA2.CCI1A	0	01
		TA2.1	1	
P3.4/TA2CLK/COMP0OUT	4	P3.4 (I/O)	I: 0; O: 1	00
		TA2CLK	0	01
		COMP0OUT	1	10
P3.5/UCB1CLK/TB0TRG	5	P3.5 (I/O)	I: 0; O: 1	00
		UCB1CLK	X	01
		TB0TRG	0	10
P3.6/UCB1SOMI/UCB1SCL	6	P3.6 (I/O)	I: 0; O: 1	00
		UCB1SOMI/UCB1SCL	X	01
P3.7/TA3.2	7	P3.7 (I/O)	I: 0; O: 1	00
		TA3.CCI2A	0	01
		TA3.2	1	

(1) X = don't care

6.11.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Table 6-26 summarizes the selection of the pin functions.

Table 6-26. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾	
			P4DIR.x	P4SEL.x
P4.0/TA3.1	0	P4.0 (I/O)	I: 0; O: 1	00
		TA3.CCI1A	0	01
		TA3.1	1	
P4.1/TA3.0	1	P4.1 (I/O)	I: 0; O: 1	00
		TA3.CCI0A	0	01
		TA3.0	1	
P4.2/TA3CLK	2	P4.2 (I/O)	I: 0; O: 1	00
		TA3CLK	0	01
P4.3/UCB1SOMI/UCB1SCL/TB0.5/A8	3	P4.3 (I/O)	I: 0; O: 1	00
		UCB1SOMI/UCB1SCL	X	01
		TB0.CCI5A	0	10
		TB0.5	1	
		A8	X	11
P4.4/UCB1SIMO/UCB1SDA/TB0.6/A9	4	P4.4 (I/O)	I: 0; O: 1	00
		UCB1SIMO/UCB1SDA	X	01
		TB0.CCI6A	0	10
		TB0.6	1	
		A9	X	11
P4.5/UCB0SOMI/UCB0SCL/TA3.2	5	P4.5 (I/O)	I: 0; O: 1	00
		UCB0SOMI/UCB0SCL	X	01
		TA3.CCI2A	0	10
		TA3.2	1	
P4.6/UCB0SIMO/UCB0SDA/TA3.1	6	P4.6 (I/O)	I: 0; O: 1	00
		UCB0SIMO/UCB0SDA	X	01
		TA3.CCI1A	0	10
		TA3.1	1	
P4.7/UCA0STE/TB0.1	7	P4.7 (I/O)	I: 0; O: 1	00
		UCA0STE	X	01
		TB0.CCI1A	0	10
		TB0.1	1	

(1) X = don't care

6.11.5 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

Table 6-27 summarizes the selection of the pin functions.

Table 6-27. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾	
			P5DIR.x	P5SEL.x
P5.0/UCA0CLK/TB0.2	0	P5.0 (I/O)	I: 0; O: 1	00
		UCA0CLK	X	01
		TB0.CCI2A	0	10
		TB0.2	1	
P5.1/UCA0RXD/UCA0SOMI/TB0.3	1	P5.1 (I/O)	I: 0; O: 1	00
		UCA0RXD/UCA0SOMI	X	01
		TB0.CCI3A	0	10
		TB0.3	1	
P5.2/UCA0TXD/UCA0SIMO/TB0.4	2	P5.2 (I/O)	I: 0; O: 1	00
		UCA0TXD/UCA0SIMO	X	01
		TB0.CCI4A	0	10
		TB0.4	1	
P5.3/UCB1CLK/TA3.0/A10	3	P5.3 (I/O)	I: 0; O: 1	00
		UCB1CLK	X	01
		TA3.CCI0A	0	01
		TA3.0	1	
		A10	X	11
P5.4/UCB1STE/TA3CLK/A11	4	P5.4 (I/O)	I: 0; O: 1	00
		UCB1STE	X	01
		TA3CLK	0	01
		A11	X	11
P5.5/UCB0CLK/TA2CLK	5	P5.5 (I/O)	I: 0; O: 1	00
		UCB0CLK	X	01
		TA2CLK	0	10
P5.6/UCB0STE/TA2.0	6	P5.6 (I/O)	I: 0; O: 1	00
		UCB0STE	X	01
		TA2.CCI0A	0	10
		TA2.0	1	
P5.7/TA2.1/COMP0.2	7	P5.7 (I/O)	I: 0; O: 1	00
		TA2.CCI1A	0	01
		TA2.1	1	
		COMP0.2	X	11

(1) X = don't care

6.11.6 Port P6 (P6.0 to P6.2) Input/Output With Schmitt Trigger

Table 6-28 summarizes the selection of the pin functions.

Table 6-28. Port P6 (P6.0 to P6.2) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS AND SIGNALS ⁽¹⁾	
			P6DIR.x	P6SEL.x
P6.0/TA2.2/COMP0.3	0	P6.0 (I/O)	I: 0; O: 1	00
		TA2.CCI2A	0	01
		TA2.2	1	
		COMP0.3	X	11
P6.1/TB0CLK	1	P6.1 (I/O)	I: 0; O: 1	00
		TB0CLK	0	01
P6.2/TB0.0	2	P6.2 (I/O)	I: 0; O: 1	00
		TB0.CCI0A	0	01
		TB0.0	1	

(1) X = don't care

6.12 Device Descriptors

Table 6-29 lists the Device IDs. Table 6-30 lists the contents of the device descriptor tag-length-value (TLV) structure.

Table 6-29. Device IDs

DEVICE	DEVICE ID	
	1A05h	1A04h
MSP430FR2476	83h	2A
MSP430FR2475	83h	2B

Table 6-30. Device Descriptors

DESCRIPTION		ADDRESS	VALUE
Information block	Info length	1A00h	06h
	CRC length	1A01h	06h
	CRC value ⁽¹⁾	1A02h	Per unit
		1A03h	Per unit
	Device ID	1A04h	See Table 6-29
		1A05h	
	Hardware revision	1A06h	Per unit
	Firmware revision	1A07h	Per unit
Die record	Die record tag	1A08h	08h
	Die record length	1A09h	0Ah
	Lot wafer ID	1A0Ah	Per unit
		1A0Bh	Per unit
		1A0Ch	Per unit
		1A0Dh	Per unit
	Die X position	1A0Eh	Per unit
		1A0Fh	Per unit
	Die Y position	1A10h	Per unit
		1A11h	Per unit
	Test result	1A12h	Per unit
		1A13h	Per unit

(1) CRC value covers the checksum from 0x1A04h to 0x1AF7h by applying CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$.

Table 6-30. Device Descriptors (continued)

DESCRIPTION		ADDRESS	VALUE
ADC calibration	ADC calibration tag	1A14h	11h
	ADC calibration length	1A15h	10h
	ADC gain factor ⁽²⁾	1A16h	Per unit
		1A17h	Per unit
	ADC offset ⁽³⁾	1A18h	Per unit
		1A19h	Per unit
	ADC internal shared 1.5-V reference, temperature sensor 30°C	1A1Ah	Per unit
		1A1Bh	Per unit
	ADC internal shared 1.5-V reference, temperature sensor 105°C	1A1Ch	Per unit
		1A1Dh	Per unit
	ADC internal shared 2.0-V reference, temperature sensor 30°C	1A1Eh	Per unit
		1A1Fh	Per unit
	ADC internal shared 2.0-V reference, temperature sensor 105°C	1A20h	Per unit
		1A21h	Per unit
	ADC internal shared 2.5-V reference, temperature sensor 30°C	1A22h	Per unit
		1A23h	Per unit
Reference and DCO calibration	ADC internal shared 2.5-V reference, temperature sensor 105°C	1A24h	Per unit
		1A25h	Per unit
	Internal shared reference Calibration tag	1A26h	12h
	Internal shared reference Calibration length	1A27h	0Ah
	Internal shared 1.5-V reference factor	1A28h	Per unit
		1A29h	Per unit
	Internal shared 2.0-V reference factor	1A2Ah	Per unit
		1A2Bh	Per unit
	Internal shared 2.5-V reference factor	1A2Ch	Per unit
		1A2Dh	Per unit
	DCO tap settings for 16 MHz, temperature 30°C	1A2Eh	Per unit
		1A2Fh	Per unit
	DCO tap settings for 24 MHz, temperature 30°C ⁽⁴⁾	1A30h	Per unit
		1A31h	Per unit

- (2) ADC gain: the gain correction factor is measured at 2.4 V and room temperature using ADCSREFx = 0x7, an external reference without internal buffer. $V_{R+} = V_{\text{eref+}}$, $V_{R-} = V_{\text{eref-}}$. Other settings can result in different factors.
- (3) ADC offset: the offset correction factor is measured at 2.4 V and room temperature using ADCSREFx = 0x7, an external reference without internal buffer. $V_{R+} = V_{\text{eref+}}$, $V_{R-} = V_{\text{eref-}}$. Other settings can result in different factors.
- (4) This value can be directly loaded into the DCO bits in the CSCTL0 register to get an accurate 24-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. TI also suggests to use a predivider to decrease the frequency if the temperature drift might result an overshoot faster than 24 MHz.

6.13 Memory

6.13.1 Memory Organization

Table 6-31 summarizes the memory organization of the devices.

Table 6-31. Memory Organization

	ACCESS	MSP430FR2476	MSP430FR2475
Bootloader (BSL2) memory (ROM)	Read only	1KB FFFFFh to FFC00h	1KB FFFFFh to FFC00h
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Read/Write (Optional Write Protect) ⁽¹⁾	64KB FFFFFh to FF80h 17FFFh to 8000h	32KB FFFFFh to FF80h FFFFFh to 8000h
RAM	Read/Write	8KB 3FFFh to 2000h	4KB 2FFFh to 2000h
Information memory (FRAM)	Read/Write (Optional Write Protect) ⁽²⁾	512B 19FFh to 1800h	512B 19FFh to 1800h
Bootloader (BSL1) memory (ROM)	Read only	2KB 17FFh to 1000h	2KB 17FFh to 1000h
Peripherals	Read/Write	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h
Tiny RAM	Read/Write	26 bytes 001Fh to 0006h	26 bytes 001Fh to 0006h
Reserved ⁽³⁾	Read only	6 bytes 0005h to 0000h	6 bytes 0005h to 0000h

- (1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#) for more details
- (2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#) for more details
- (3) Read as: D032h at 00h (Opcode: BIS.W LPM4, SR), 00F0h at 02h (Opcode: BIS.W LPM4, SR), 3FFFh at 04h (Opcode: JMP\$)

6.13.2 Peripheral File Map

Table 6-32 lists the available peripherals and the register base address for each.

Table 6-32. Peripherals Summary

MODULE NAME	BASE ADDRESS	SIZE
Special Functions (see Table 6-33)	0100h	0010h
PMM (see Table 6-34)	0120h	0020h
SYS (see Table 6-35)	0140h	0040h
CS (see Table 6-36)	0180h	0020h
FRAM (see Table 6-37)	01A0h	0010h
CRC (see Table 6-38)	01C0h	0008h
WDT (see Table 6-39)	01CCh	0002h
Port P1, P2 (see Table 6-40)	0200h	0020h
Port P3, P4 (see Table 6-41)	0220h	0020h
Port P5, P6 (see Table 6-42)	0240h	0020h
RTC (see Table 6-43)	0300h	0010h
Timer0_A3 (see Table 6-44)	0380h	0030h
Timer1_A3 (see Table 6-45)	03C0h	0030h
Timer2_A3 (see Table 6-46)	0400h	0030h
Timer3_A3 (see Table 6-47)	0440h	0030h
Timer0_B7 (see Table 6-48)	0480h	0030h
MPY32 (see Table 6-49)	04C0h	0030h
eUSCI_A0 (see Table 6-50)	0500h	0020h
eUSCI_A1 (see Table 6-51)	0520h	0020h
eUSCI_B0 (see Table 6-52)	0540h	0030h
eUSCI_B1 (see Table 6-53)	0580h	0030h
Backup Memory (see Table 6-54)	0660h	0020h
ADC (see Table 6-55)	0700h	0040h
eCOMP0 (see Table 6-56)	08E0h	0020h

Table 6-33. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-34. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
PMM control 2	PMMCTL2	04h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

Table 6-35. SYS Registers (Base Address: 0140h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h

Table 6-35. SYS Registers (Base Address: 0140h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh
System configuration 0	SYSCFG0	20h
System configuration 1	SYSCFG1	22h
System configuration 2	SYSCFG2	24h

Table 6-36. CS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch
CS control 7	CSCTL7	0Eh
CS control 8	CSCTL8	10h

Table 6-37. FRAM Registers (Base Address: 01A0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 6-38. CRC Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCNIRE	04h
CRC result reverse byte	CRCRESR	06h

Table 6-39. WDT Registers (Base Address: 01CCh)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-40. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h

Table 6-40. Port P1, P2 Registers (Base Address: 0200h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P1 direction	P1DIR	04h
Port P1 pulling enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pulling enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-41. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pulling enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pulling enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 interrupt vector word	P4IV	1Eh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

Table 6-42. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pulling enable	P5REN	06h
Port P5 selection 0	P5SEL0	0Ah
Port P5 selection 1	P5SEL1	0Ch
Port P5 interrupt vector word	P5IV	0Eh
Port P5 complement selection	P5SELC	16h
Port P5 interrupt edge select	P5IES	18h
Port P5 interrupt enable	P5IE	1Ah
Port P5 interrupt flag	P5IFG	1Ch
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pulling enable	P6REN	07h
Port P6 selection 0	P6SEL0	0Bh
Port P6 selection 1	P6SEL1	0Dh
Port P6 interrupt vector word	P6IV	1Eh
Port P6 complement selection	P6SELC	17h
Port P6 interrupt edge select	P6IES	19h
Port P6 interrupt enable	P6IE	1Bh
Port P6 interrupt flag	P6IFG	1Dh

Table 6-43. RTC Registers (Base Address: 0300h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
RTC control	RTCCTL	00h
RTC interrupt vector	RTCIV	04h
RTC modulo	RTCMOD	08h
RTC counter	RTCCNT	0Ch

Table 6-44. Timer0_A3 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-45. Timer1_A3 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-46. Timer2_A3 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 6-47. Timer3_A3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h
Capture/compare control 1	TA3CCTL1	04h
Capture/compare control 2	TA3CCTL2	06h
TA3 counter	TA3R	10h
Capture/compare 0	TA3CCR0	12h
Capture/compare 1	TA3CCR1	14h
Capture/compare 2	TA3CCR2	16h
TA3 expansion 0	TA3EX0	20h
TA3 interrupt vector	TA3IV	2Eh

Table 6-48. Timer0_B7 Registers (Base Address: 0480h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch

Table 6-48. Timer0_B7 Registers (Base Address: 0480h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Capture/compare control 6	TB0CTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-49. MPY32 Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP6	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 6-50. eUSCI_A0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A control rate 0	UCA0BR0	06h
eUSCI_A control rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch

Table 6-50. eUSCI_A0 Registers (Base Address: 0500h) (continued)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	IUCA0IRTCTL	12h
eUSCI_A IrDA receive control	IUCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 6-51. eUSCI_A1 Registers (Base Address: 0520h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI_A control word 1	UCA1CTLW1	02h
eUSCI_A control rate 0	UCA1BR0	06h
eUSCI_A control rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status	UCA1STAT	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	IUCA1IRTCTL	12h
eUSCI_A IrDA receive control	IUCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

Table 6-52. eUSCI_B0 Registers (Base Address: 0540h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0BCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B receive address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

Table 6-53. eUSCI_B1 Registers (Base Address: 0580h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
eUSCI_B control word 0	UCB1CTLW0	00h
eUSCI_B control word 1	UCB1CTLW1	02h
eUSCI_B bit rate 0	UCB1BR0	06h
eUSCI_B bit rate 1	UCB1BR1	07h
eUSCI_B status word	UCB1STATW	08h
eUSCI_B byte counter threshold	UCB1TBCNT	0Ah
eUSCI_B receive buffer	UCB1RXBUF	0Ch
eUSCI_B transmit buffer	UCB1TXBUF	0Eh
eUSCI_B I2C own address 0	UCB1I2COA0	14h
eUSCI_B I2C own address 1	UCB1I2COA1	16h
eUSCI_B I2C own address 2	UCB1I2COA2	18h
eUSCI_B I2C own address 3	UCB1I2COA3	1Ah
eUSCI_B receive address	UCB1ADDRX	1Ch
eUSCI_B address mask	UCB1ADDMASK	1Eh
eUSCI_B I2C slave address	UCB1I2CSA	20h
eUSCI_B interrupt enable	UCB1IE	2Ah
eUSCI_B interrupt flags	UCB1IFG	2Ch
eUSCI_B interrupt vector word	UCB1IV	2Eh

Table 6-54. Backup Memory Registers (Base Address: 0660h)

REGISTER DESCRIPTION	ACRONYM	OFFSET
Backup memory 0	BAKMEM0	00h
Backup memory 1	BAKMEM1	02h
Backup memory 2	BAKMEM2	04h
Backup memory 3	BAKMEM3	06h
Backup memory 4	BAKMEM4	08h
Backup memory 5	BAKMEM5	0Ah
Backup memory 6	BAKMEM6	0Ch
Backup memory 7	BAKMEM7	0Eh
Backup memory 8	BAKMEM8	10h
Backup memory 9	BAKMEM9	12h
Backup memory 10	BAKMEM10	14h
Backup memory 11	BAKMEM11	16h
Backup memory 12	BAKMEM12	18h
Backup memory 13	BAKMEM13	1Ah
Backup memory 14	BAKMEM14	1Ch
Backup memory 15	BAKMEM15	1Eh

Table 6-55. ADC Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control 0	ADCCTL0	00h
ADC control 1	ADCCTL1	02h
ADC control 2	ADCCTL2	04h
ADC window comparator low threshold	ADCLO	06h
ADC window comparator high threshold	ADCHI	08h
ADC memory control 0	ADCMCTL0	0Ah
ADC conversion memory	ADCMEM0	12h

Table 6-55. ADC Registers (Base Address: 0700h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC interrupt enable	ADCIE	1Ah
ADC interrupt flags	ADCIFG	1Ch
ADC interrupt vector word	ADCIV	1Eh

Table 6-56. eCOMP Registers (Base Address: 08E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator control 0	CP0CTL0	00h
Comparator control 1	CP0CTL1	02h
Comparator interrupt	CP0INT	06h
Comparator interrupt vector	CP0IV	08h
Comparator built-in DAC control	CP0DACCTL	10h

6.14 Identification

6.14.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entries in [Section 6.12](#).

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entries in [Section 6.12](#).

6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in [MSP430 Programming With the JTAG Interface](#).

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430 devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10- μ F plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and to achieve high analog accuracy.

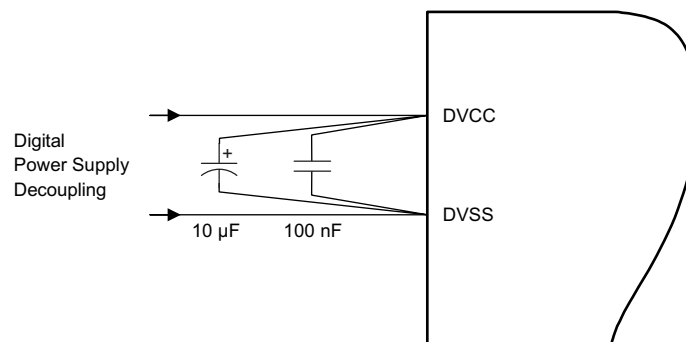


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If the XIN and XOUT pins are not used, they must be terminated according to [Section 4.6](#).

[Figure 7-2](#) shows a typical connection diagram.

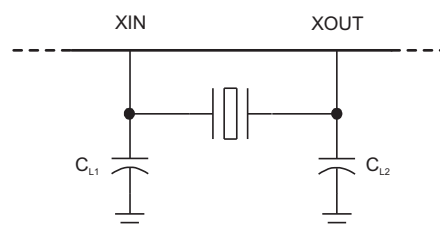


Figure 7-2. Typical Crystal Connection

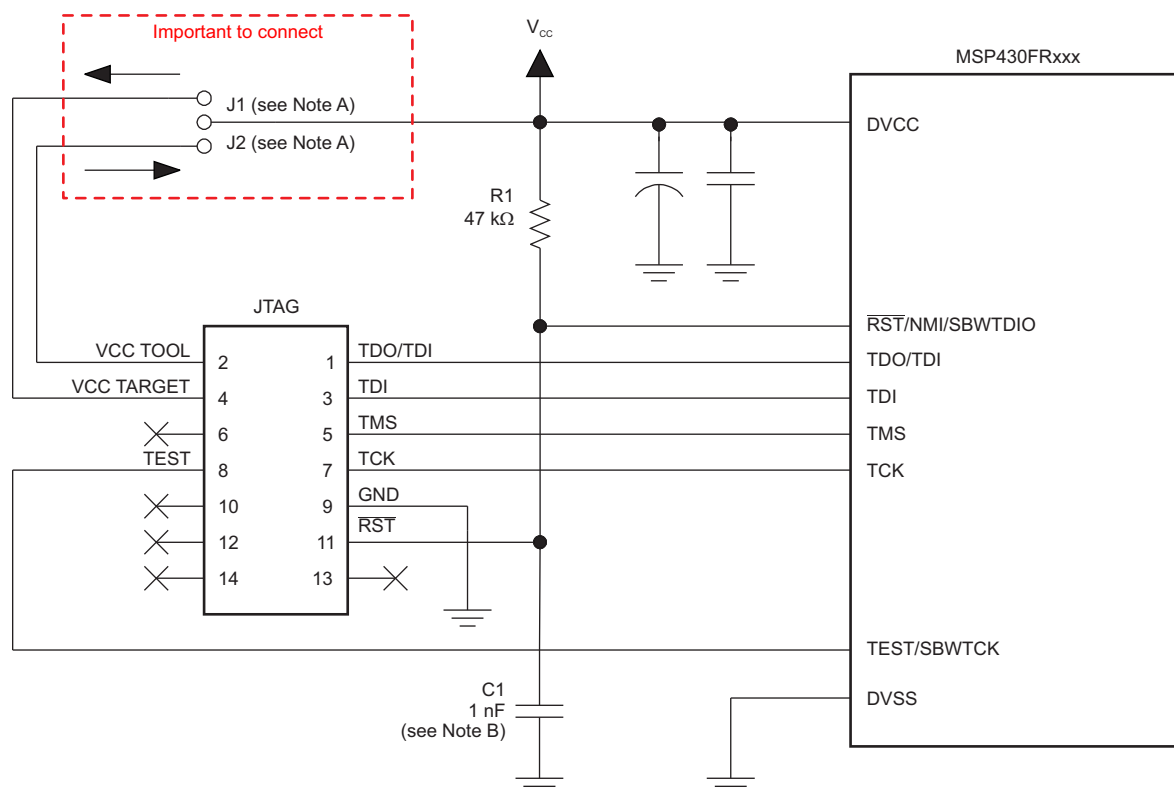
See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. [Figure 7-3](#) shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. [Figure 7-4](#) shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

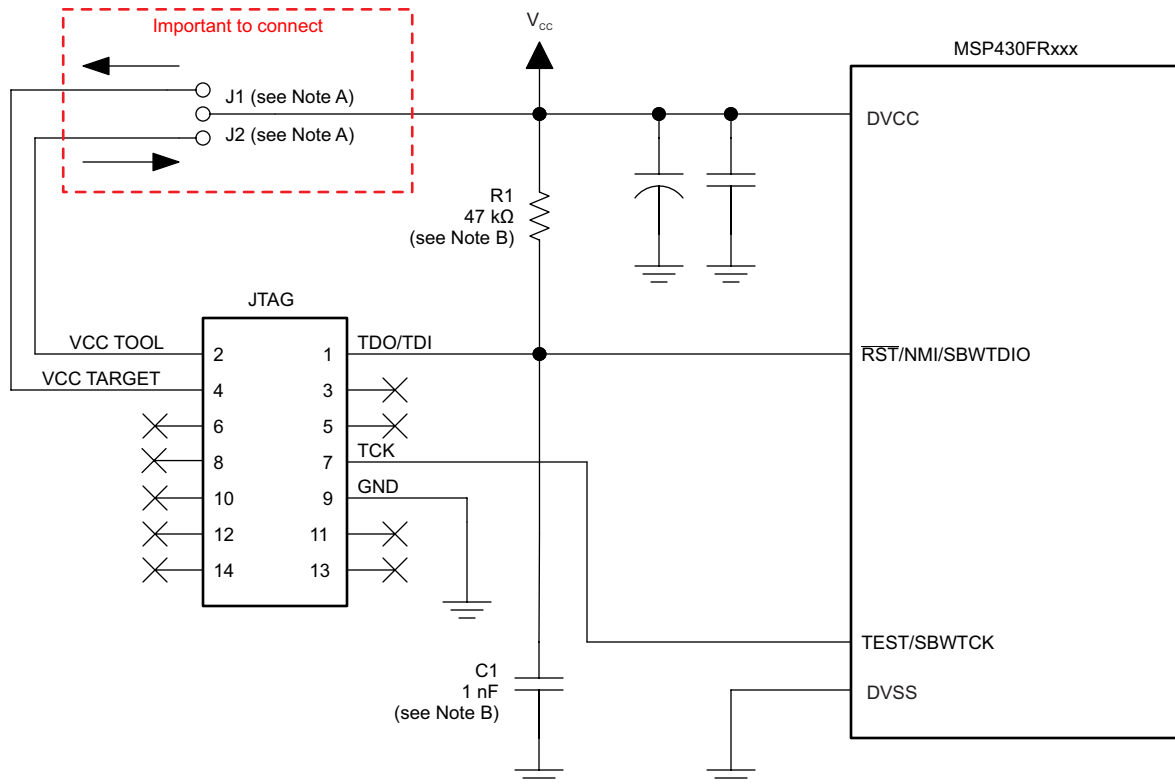
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC} sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC} sense feature detects the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. [Figure 7-3](#) and [Figure 7-4](#) show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device $\overline{\text{RST}}/\text{NMI}/\text{SBWDIO}$ pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR .

In reset mode, the $\overline{\text{RST}}/\text{NMI}$ pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}/\text{NMI}$ pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES . Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}/\text{NMI}$ pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}/\text{NMI}$ pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-k Ω pullup resistor to the $\overline{\text{RST}}/\text{NMI}$ pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MP430FR4xx and MP430FR2xx Family User's Guide](#) for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.6](#).

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in [Section 5.1, Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC Peripheral

7.2.1.1 Partial Schematic

[Figure 7-5](#) shows the recommended decoupling circuit when an external voltage reference is used.

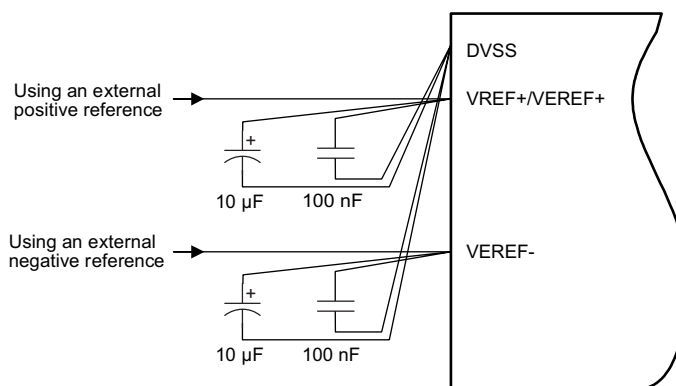


Figure 7-5. ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 7.1.1](#) combined with the connections shown in [Figure 7-5](#) prevent this.

Quickly switching digital signals and noisy power supply lines can corrupt the conversion results, so keep the ADC input trace shielded from those digital and power supply lines. Putting the MCU in low-power mode during the ADC conversion improves the ADC performance in a noisy environment. If the device includes the analog power pair inputs (AVCC and AVSS), TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

[Figure 7-5](#) shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- μ F capacitor buffers the reference pin and filters low-frequency ripple. A 100-nF bypass capacitor filters high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 7-5](#)) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

8 器件和文档支持

8.1 入门和后续步骤

更过有关 MSP 低功耗微控制器以及开发协助工具和库的信息，请访问《[MSP430™ 超低功耗传感和测量 MCU 概述](#)》。

8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品发展的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

XMS - 实验器件，不一定代表最终器件的电气规格

MSP - 完全合格的生产器件

XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 8-1 提供了解读完整器件名称的图例。

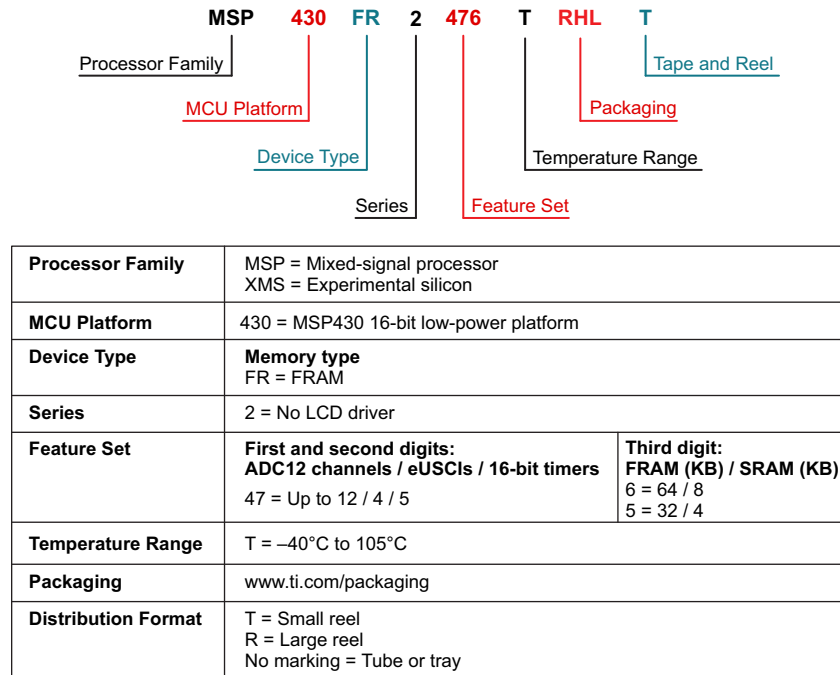


图 8-1. 器件命名规则

8.3 工具和软件

表 8-1 列出 调试 的调试功能。请参阅《适用于 MSP430™ MCU 的 Code Composer Studio™ IDE 用户指南》，以了解有关可用 功能）的详细信息。

表 8-1. 硬件 特性

MSP430 架构	四线制 JTAG	两线制 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMx.5 调试支持	EEM 版本
MSP430xv2	有	有	3	有	有	无	无	无	S

设计套件与评估模块

MSP430FR2476 LaunchPad™ 开发套件

LP-MSP430FR2476 LaunchPad 开发套件是基于 MSP430FR2476 超值系列感应微控制器 (MCU) 的易用型评估模块 (EVM)。它包含在超低功耗 MSP430FR2x 超值系列感应 MCU 平台上进行开发所需的全部资源，包括用于编程、调试和能量测量的板载调试探针。

适用于 MSP430FR2476 MCU 的目标开发板

MSP-TS430PT48A 微控制器开发板是独立的 ZIF 插座目标板，用于通过 JTAG 接口或 Spy Bi-Wire（两线制 JTAG）协议对 MSP430 器件进行系统内编程和调试。该开发板支持采用 48 引脚 QFP 封装（TI 封装代码：PT）的 MSP430FR2476 FRAM 器件。

软件

MSP430Ware™ 软件

MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP430 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430FR267x、MSP430FR247x 代码示例

根据不同应用需求配置各集成外设的 C 代码示例。

MSP 驱动程序库

驱动程序库的抽象化 API 通过提供易于使用的函数调用使您不再拘泥于 MSP430 硬件的细节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可使用驱动程序库函数以尽可能低的费用编写全部项目。

MSP EnergyTrace™ 技术

MSP430 微控制器的 EnergyTrace 技术是基于能量的代码分析工具，用于测量和显示应用的能量配置，同时协助优化应用以实现超低功耗。

ULP（超低功耗）Advisor

ULP Advisor™ 软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP 和 MSP432 微控制器独特的超低功耗功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地利用应用程序。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

适用于 MSP 超低功耗微控制器的 FRAM 嵌入式软件实用程序

FRAM 实用程序旨在作为不断扩充的嵌入式软件实用程序集合，其中的实用程序充分利用 FRAM 的超低功耗和近乎无限次的写入寿命。这些实用程序适用于 MSP430FRxx FRAM 微控制器并提供示例代码协助应用程序开发。其中的实用程序包含功耗计算实用程序 (CTPL)。CTPL 是一套实用程序 API 集，通过 CTPL 能够轻松使用 LPMx.5 低功耗模式以及强大的关断模式，允许应用程序在检测到功率损耗时节约能耗并恢复关键的系统元件。

IEC60730 软件包

IEC60730 MSP430 软件包可帮助您遵循 IEC 60730-1:2010（家用和类似用途的自动电气控制设备 - 第 1 部分：一般要求）对 B 类产品的要求，B 类产品包括家用电器、电弧检测器、电源转换器、电动工具、电动自行车和其他诸多产品。IEC60730 MSP430 软件包可嵌入至在 MSP430 MCU 上运行的应用，有助于简化消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证过程。

适用于 MSP 的定点数学库

MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时应用，而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学库

TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。这是标量函数的浮点数学库，能够充分利用器件的智能外设，使性能提升高达 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境

Code Composer Studio 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。Code Composer Studio IDE 包含一整套用于开发和调试嵌入式应用的嵌入式软件实用工具的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种功能。

IAR Embedded Workbench® IDE

适用于 MSP430 MCU 的 IAR Embedded Workbench IDE 是一套用于构建和调试基于 MSP430 微控制器的嵌入式应用的完整 C/C++ 编译器工具链。该调试器可用于源代码和反汇编代码，而且支持复杂代码和数据断点。它还提供了硬件仿真器，可在未连接实际目标的情况下进行调试。

Uniflash 独立闪存工具

CCS Uniflash 是一个独立的工具，用于在 TI MCU 上对片上闪存进行编程。Uniflash 具有 GUI、命令行和脚本界面。Uniflash 软件工具支持两种使用方式：TI 云工具或者从 TI 网页下载的桌面应用。

MSP MCU 编程器和调试器

MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可让用户在 MSP 低功耗微控制器 (MCU) 上快速进行应用开发。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件，以进行验证和调试。MSP-FET 在主机和目标 MSP 间提供调试通信通道。此外，MSP-FET 还在计算机的 USB 接口和 MSP UART 之间提供反向通道 UART 连接。这为 MSP 编程器提供了一种便捷方法，实现了 MSP 和在计算机上运行的终端之间的串行通信。

MSP-GANG 生产编程器

MSP Gang 编程器可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。MSP Gang 编程器配有扩展板“Gang 分离器”，可在 MSP Gang 编程器和多个目标器件间实现互连。

TIREX Resource Explorer (TIRex)

用于查找器件和开发板的示例、库、可执行代码和文档的在线门户。您可以直接在 Code Composer Studio IDE 内访问 TIRex，也可以在“TI 云工具”中访问 TIRex。

TI 云工具

快速在 dev.ti.com 上开始开发。首先使用 Resource Explorer 界面快速找到您需要的所有文件。然后使用行业领先的 Code Composer Studio Cloud IDE 在云中编辑、生成和调试嵌入式应用。

GCC - 适用于 MSP 的编译器

MSP430 和 MSP432 GCC 开源包是一个完整的调试器和开源 C/C++ 编译器工具链，用于基于 MSP430 和 MSP432 微控制器构建和调试嵌入式应用。这些免费的 GCC 编译器支持所有 MSP430 和 MSP432 器件且没有代码大小限制。此外，这些编译器可以通过命令行独立使用，也可在 Code Composer Studio v6.0 或更高版本中使用。不管您使用的是 Windows®、Linux® 还是 macOS® 环境，马上开始吧。

8.4 文档支持

以下文档介绍了 MSP430FR247x 微控制器。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP430FR2476 器件勘误表》

说明了功能规格的已知例外情况。

《MSP430FR2475 器件勘误表》

说明了功能规格的已知例外情况。

用户指南

《[MSP430FR4xx 和 MSP430FR2xx 系列用户指南](#)》

可说明。

《[MSP430™ FRAM 器件引导加载程序 \(BSL\) 用户指南](#)》

MSP430 微控制器 (MCU) 上的引导加载程序 (BSL) 允许用户在原型设计、最终生产和使用期间与 MSP430 MCU 中的嵌入式存储器进行通信。可编程存储器 (FRAM 存储器) 和数据存储器 (RAM) 均可按要求予以修改。

通过 JTAG 接口进行 MSP430™ 编程

此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。

《[MSP430™ 硬件工具用户指南](#)》

此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

《[MSP430 32kHz 晶体振荡器](#)》

选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《[MSP430 系统级 ESD 注意事项](#)》

随着芯片技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

表 8-2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
MSP430FR2476	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430FR2475	单击此处	单击此处	单击此处	单击此处	单击此处

8.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的《使用条款》。

TI E2E™ 社区

TI 的工程师交流 (E2E) 社区。此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页

德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

8.7 商标

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.

macOS is a registered trademark of Apple, Inc.

IAR Embedded Workbench is a registered trademark of IAR Systems.

Linux is a registered trademark of Linus Torvalds.

Windows is a registered trademark of Microsoft Corporation.

8.8 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR2475TPT	ACTIVE	LQFP	PT	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2475	Samples
MSP430FR2475TPTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2475	Samples
MSP430FR2475TRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2475	Samples
MSP430FR2475TRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2475	Samples
MSP430FR2475TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2475	Samples
MSP430FR2475TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2475	Samples
MSP430FR2476TPT	ACTIVE	LQFP	PT	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2476	Samples
MSP430FR2476TPTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	430FR2476	Samples
MSP430FR2476TRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2476	Samples
MSP430FR2476TRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2476	Samples
MSP430FR2476TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2476	Samples
MSP430FR2476TRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	FR2476	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

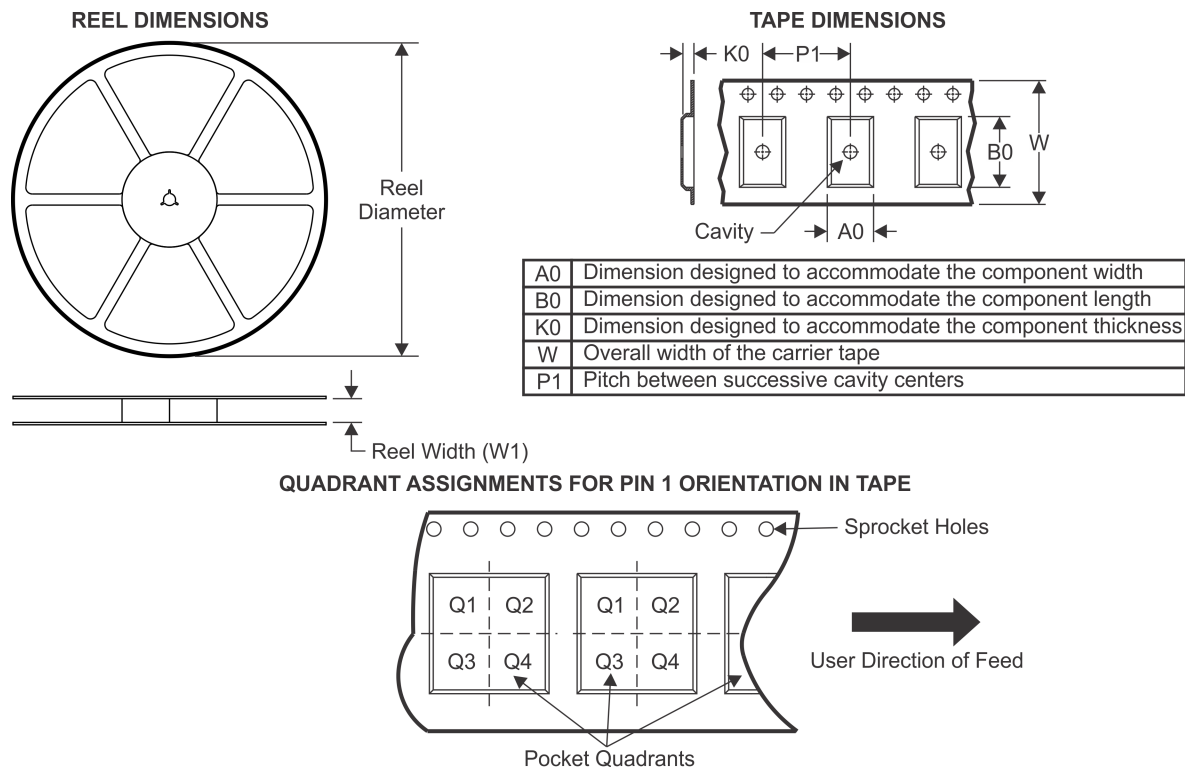
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

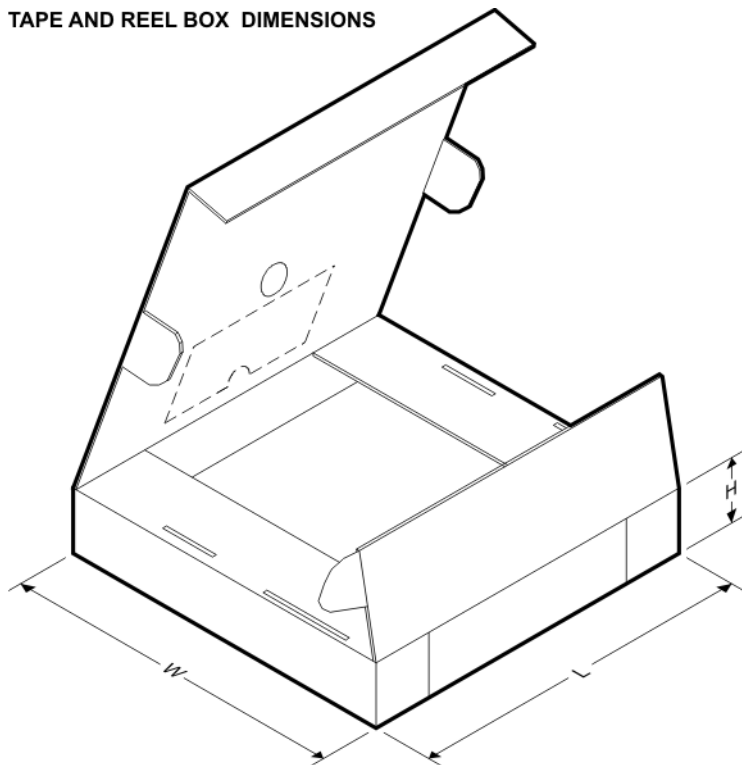
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR2475TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2475TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2475TRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2475TRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2475TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2475TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2476TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2476TPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
MSP430FR2476TRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2476TRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR2476TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430FR2476TRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR2475TPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSP430FR2475TPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430FR2475TRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
MSP430FR2475TRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR2475TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430FR2475TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430FR2476TPTR	LQFP	PT	48	1000	336.6	336.6	31.8
MSP430FR2476TPTR	LQFP	PT	48	1000	350.0	350.0	43.0
MSP430FR2476TRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
MSP430FR2476TRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR2476TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430FR2476TRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

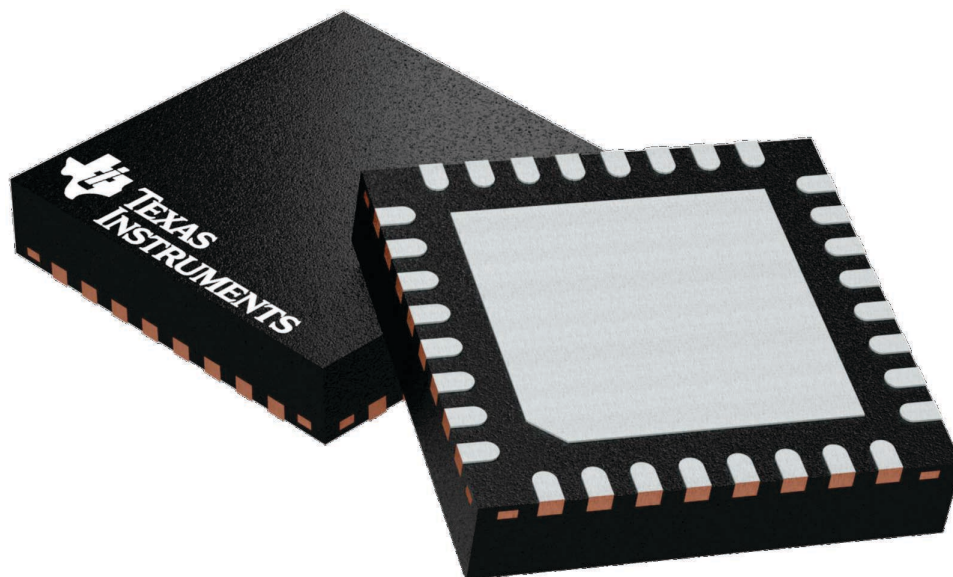
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



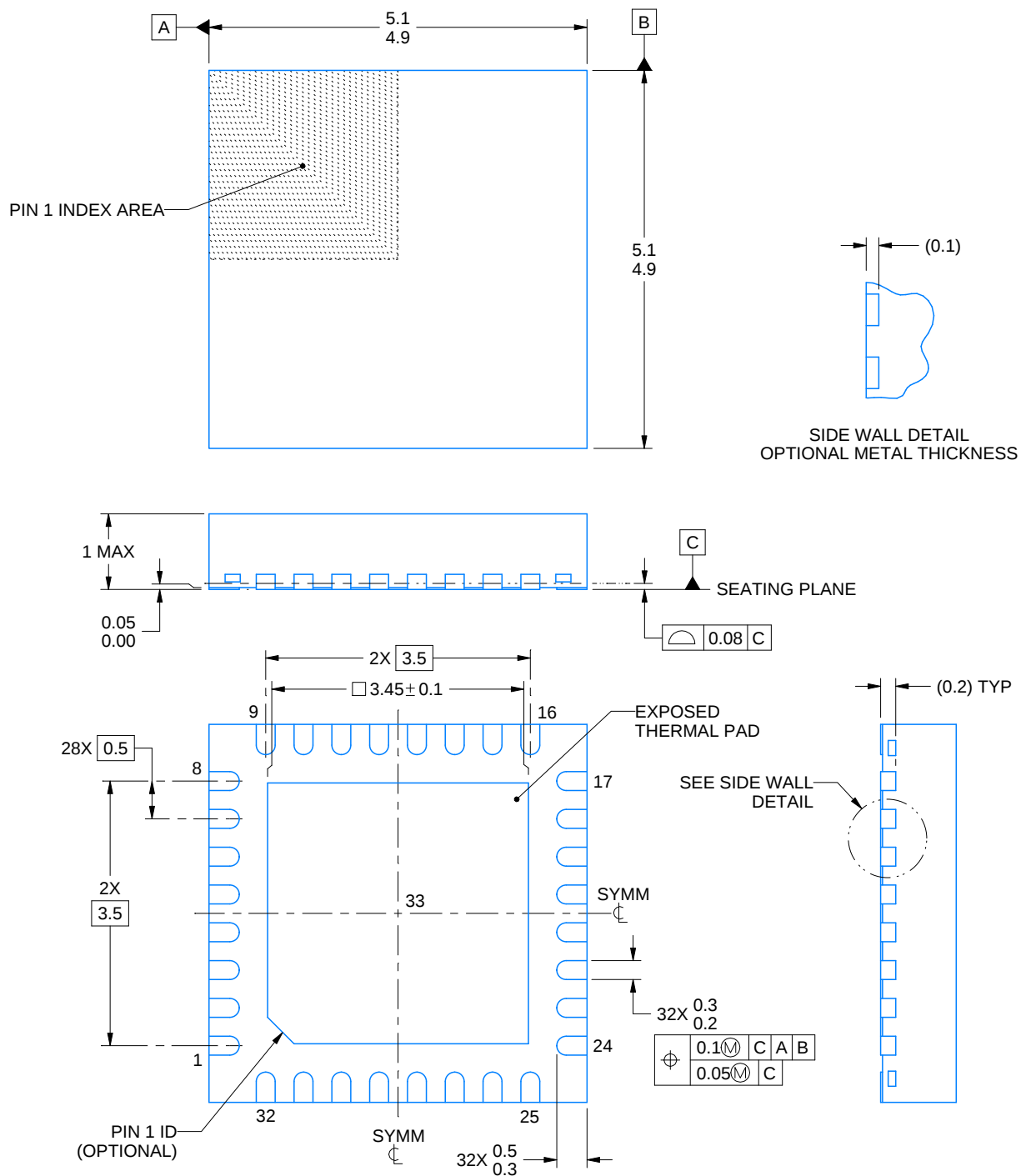
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223442/B 08/2019

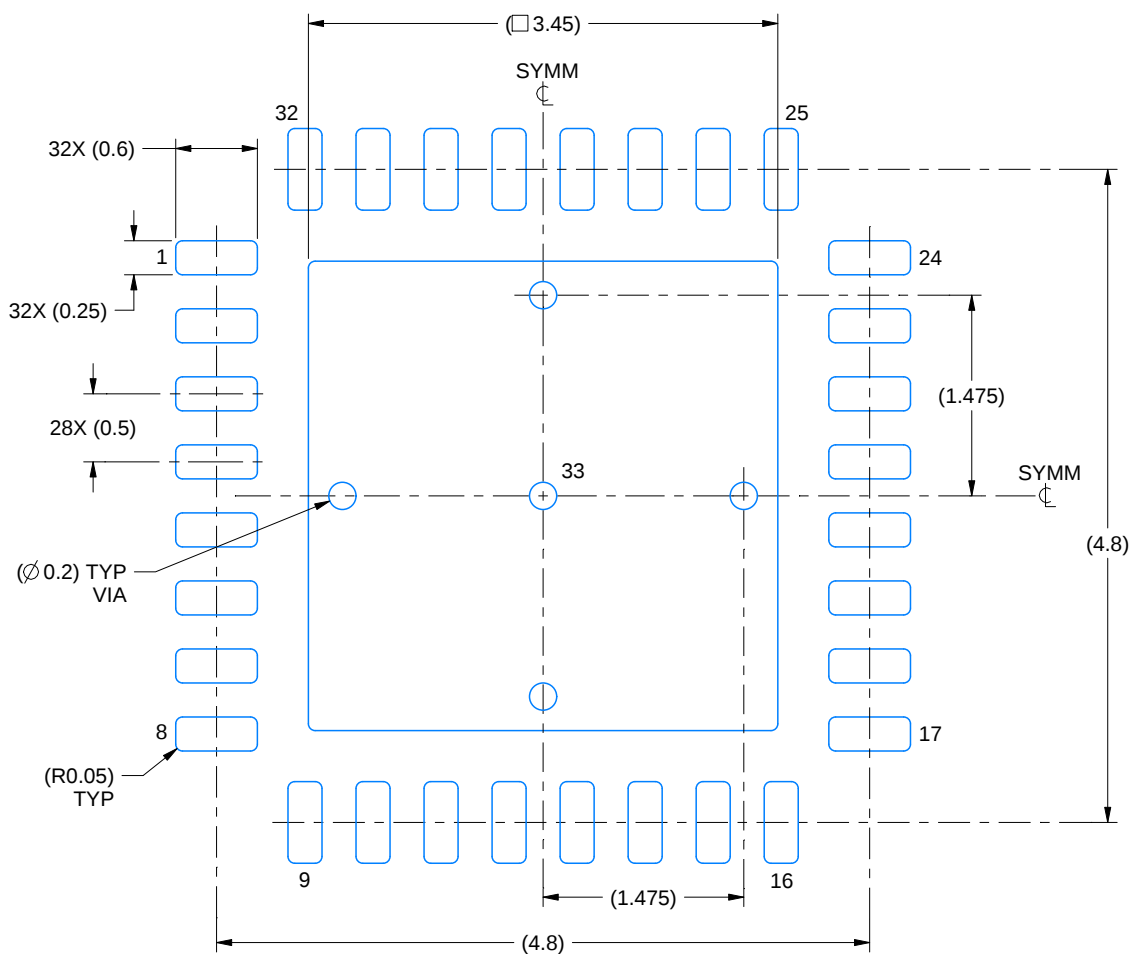
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

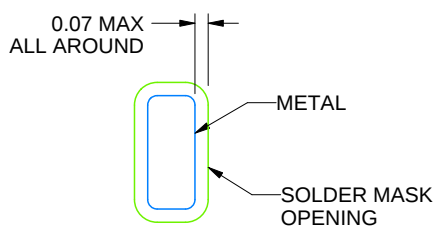
RHB0032E

VQFN - 1 mm max height

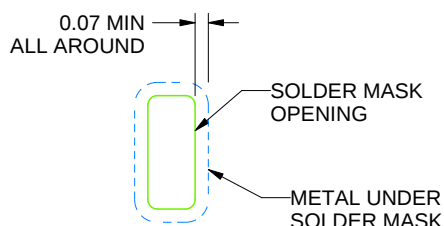
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

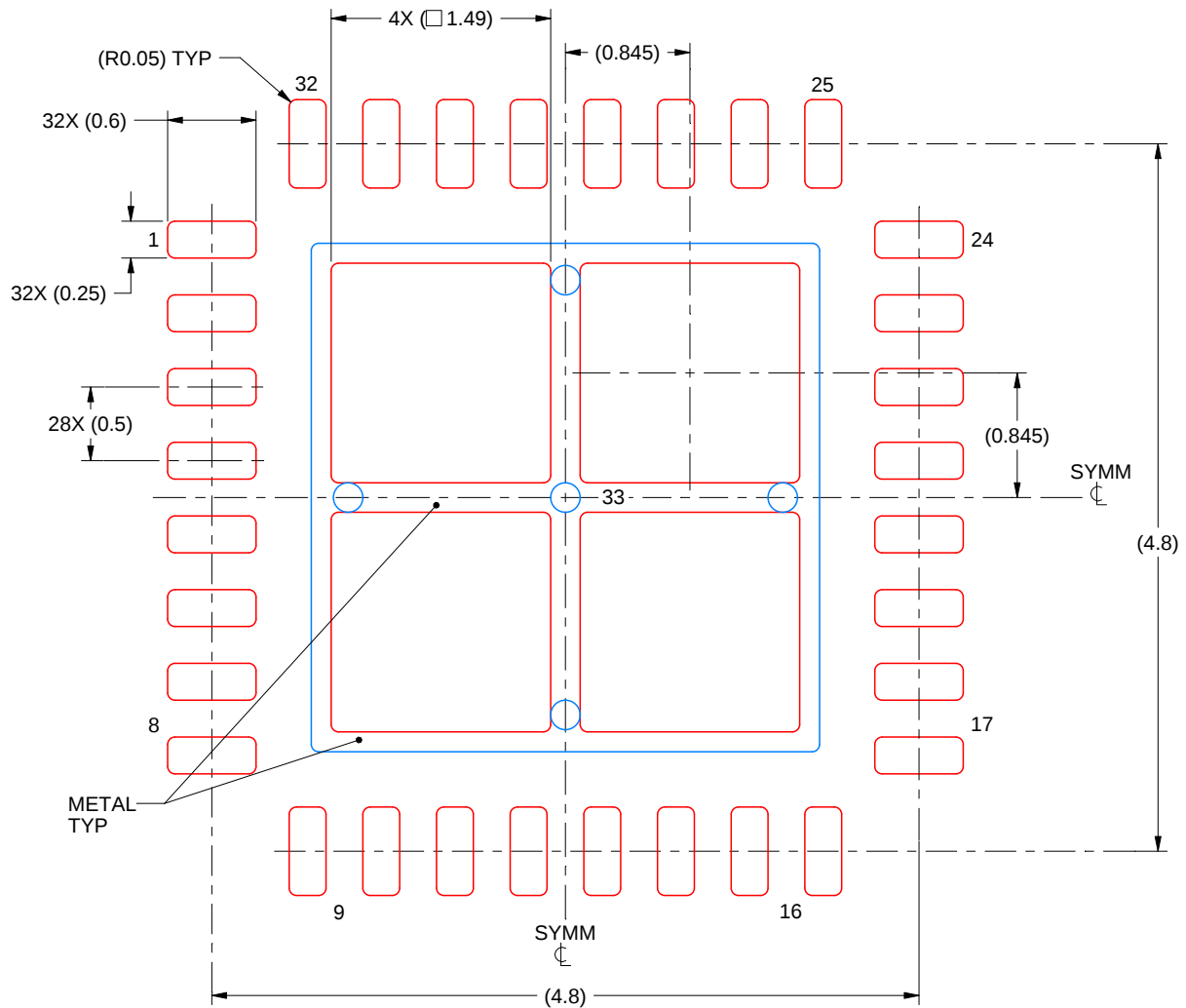
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

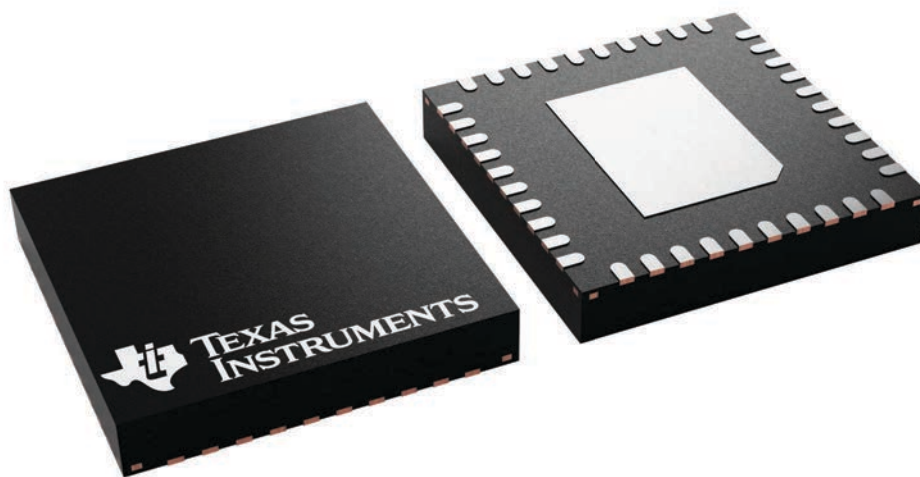
RHA 40

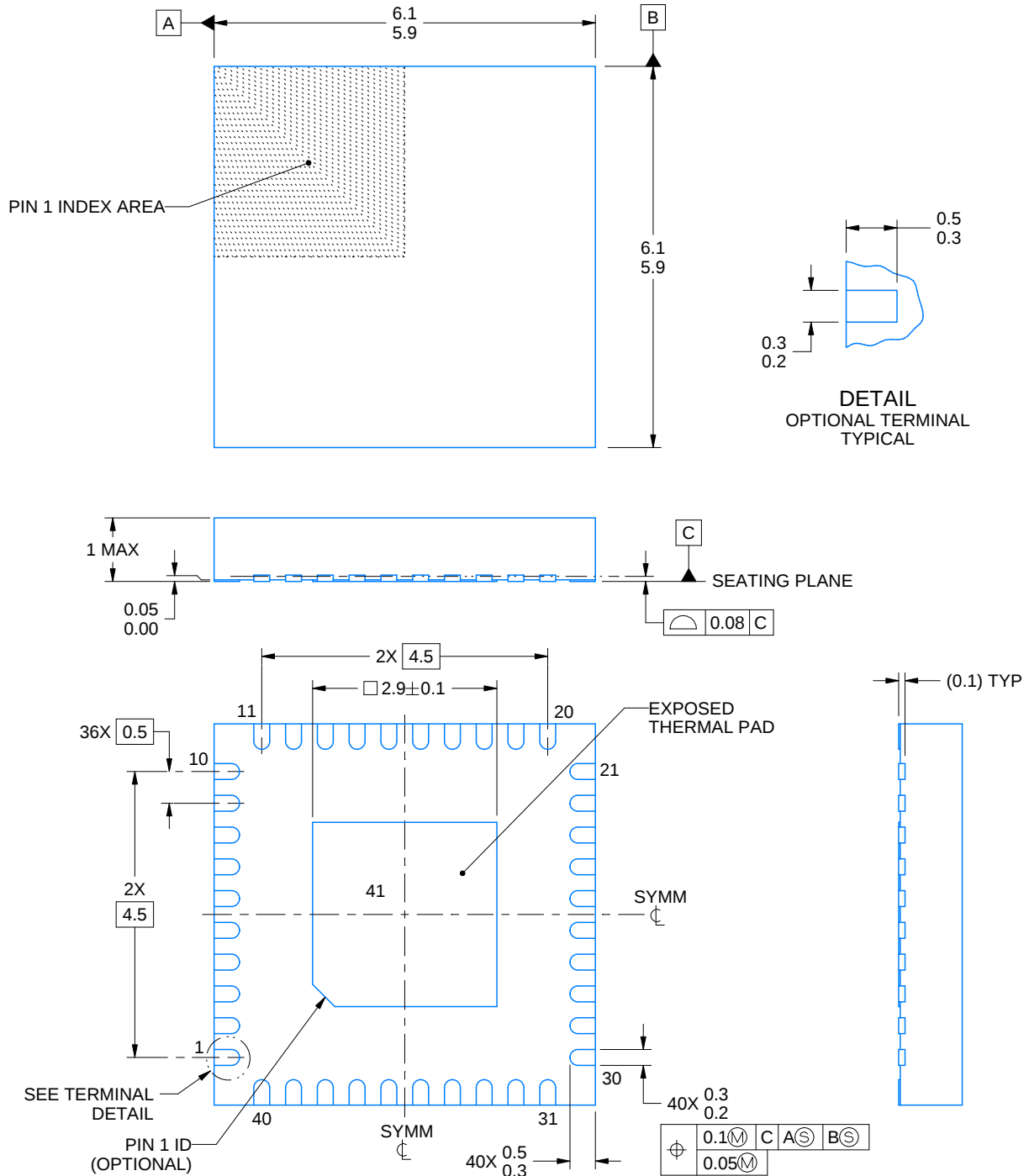
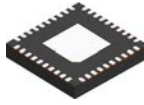
VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4225822/A 03/2020

NOTES:

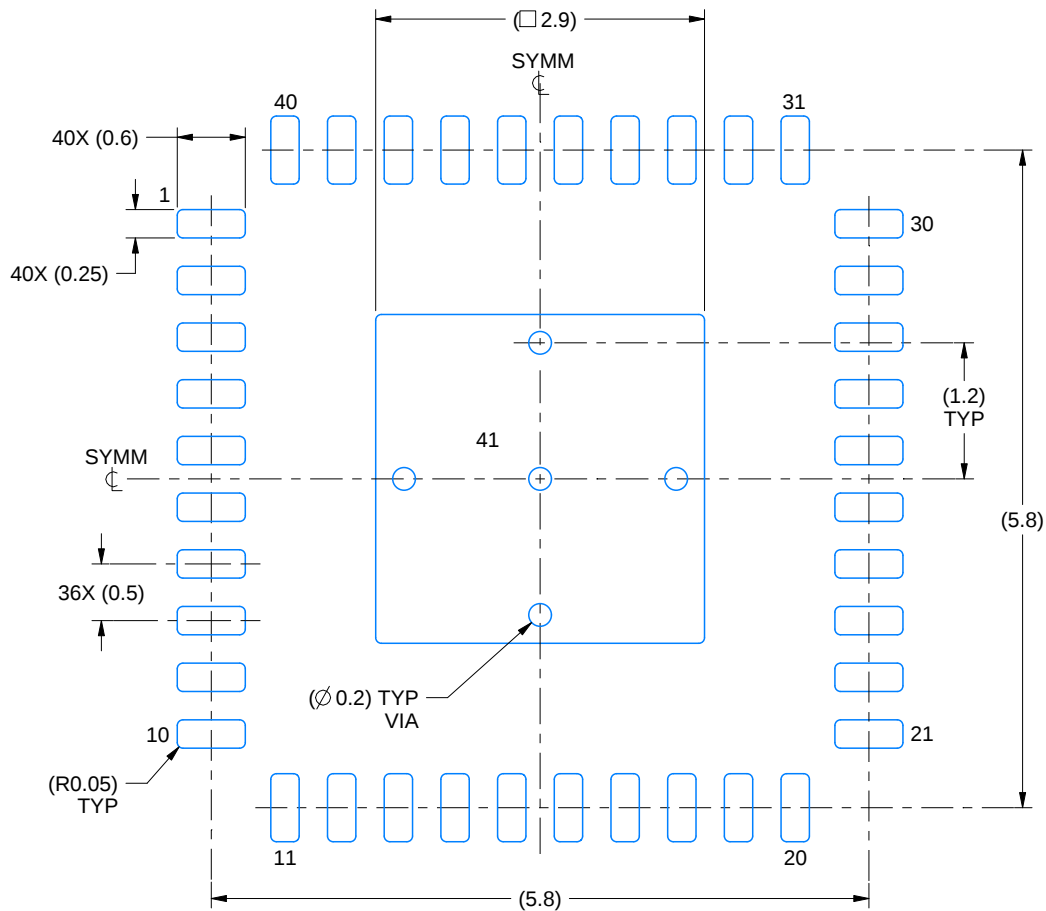
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

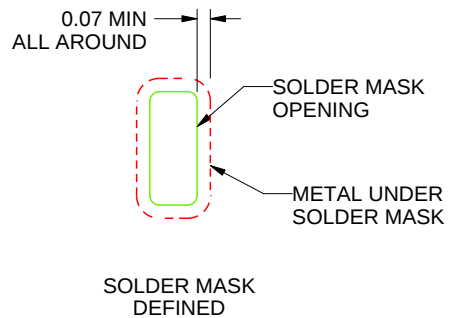
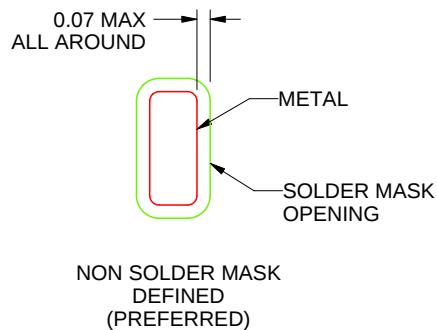
RHA0040D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4225822/A 03/2020

NOTES: (continued)

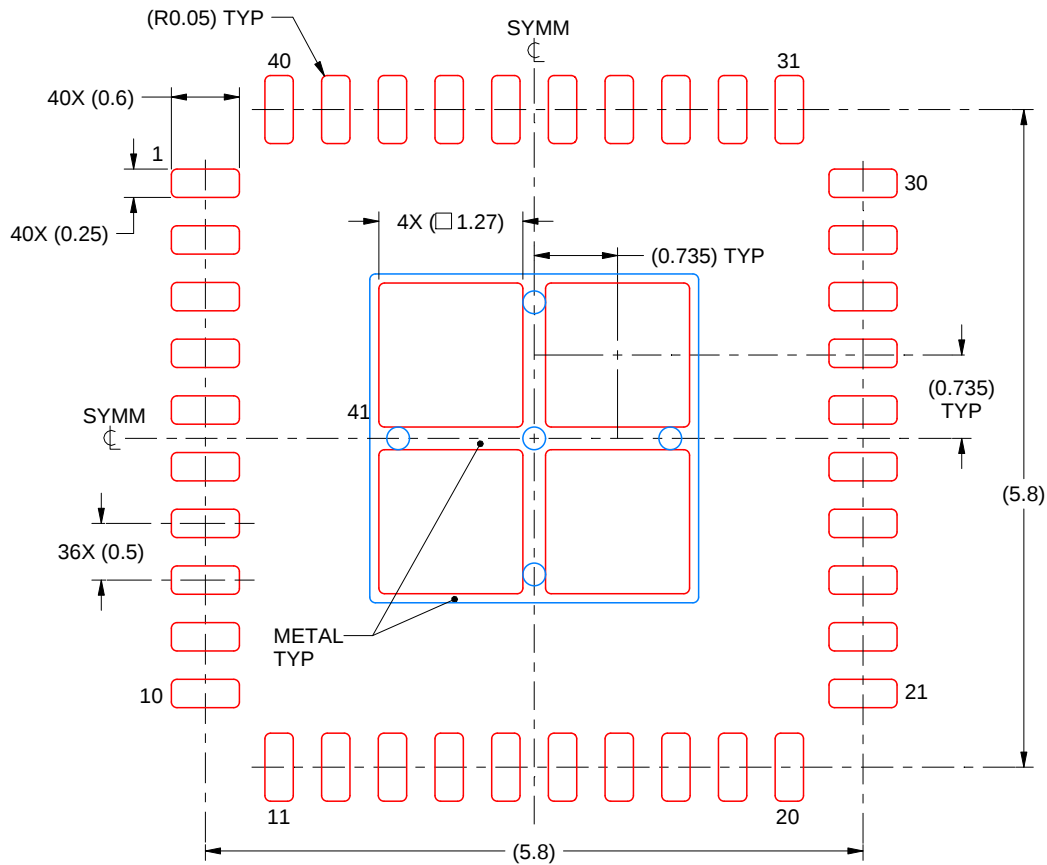
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.

EXAMPLE STENCIL DESIGN

RHA0040D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

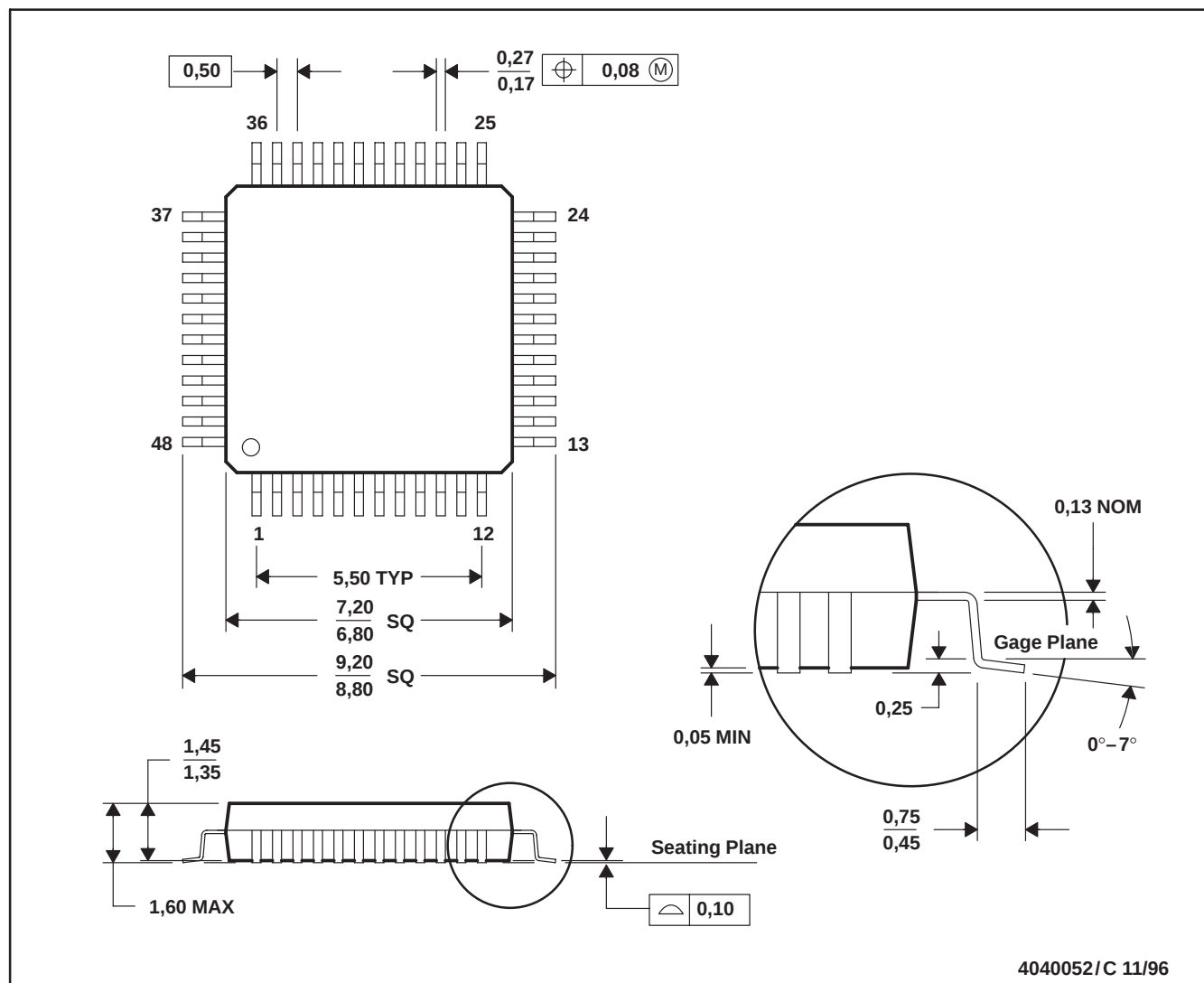
4225822/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PT (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-026
 - This may also be a thermally enhanced plastic package with leads connected to the die pads.

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