

# MSP430FG662x、MSP430FG642x 混合信号微控制器

## 1 器件概述

### 1.1 特性

- 低电源电压范围：  
3.6V 到低至 1.8V
- 超低功耗
  - 激活模式 (AM):  
所有系统时钟激活：  
在 8MHz、3.0V 且闪存程序执行时为  
250 $\mu$ A/MHz（典型值）
  - 待机模式 (LPM3):  
看门狗（采用晶振）和电源监控器工作，完全  
RAM 保持，快速唤醒：  
2.2V 时为 3.2 $\mu$ A，3.0V 时为 3.4 $\mu$ A（典型值）
  - 关断 RTC 模式 (LPM 3.5):  
关断模式，实时时钟（采用晶振）工作：  
3.0V 时为 0.9 $\mu$ A（典型值）
  - 关断模式 (LPM4.5):  
3.0V 时为 0.2 $\mu$ A（典型值）
- 在 3 $\mu$ s（典型值）内从待机模式唤醒
- 16 位精简指令集 (RISC) 架构、扩展存储器、高达  
20MHz 的系统时钟
- 灵活的电源管理系统
  - 内置可编程的低压降稳压器 (LDO)
  - 电源电压监控、监视、和临时限电
- 统一时钟系统
  - 针对频率稳定的锁相环 (FLL) 控制环路
  - 低功耗低频内部时钟源 (VLO)
  - 低频修整内部基准源 (REFO)
  - 32kHz 晶振 (XT1)
  - 高达 32MHz 的高频晶振 (XT2)
- 4 个定时器，分别配有 3、5 或 7 个捕捉/比较寄存  
器
- 2 个通用串行通信接口
  - USCI\_A0 和 USCI\_A1 均支持
    - 具有自动波特率检测功能的增强型通用异步收  
发器 (UART)
    - IrDA 编码和解码
    - 同步串行外设接口 (SPI)
  - USCI\_B0 和 USCI\_B1 均支持
    - I<sup>2</sup>C
    - 同步串行外设接口 (SPI)
- 全速通用串行总线 (USB)
  - 集成的 USB - 物理层 (PHY)
  - 集成 3.3V 和 1.8V USB 电源系统
  - 集成 USB-PLL
  - 8 输入和 8 输出端点
- 连续时间  $\Sigma$ - $\Delta$  16 位模数转换器 (ADC)，具有内部参  
考电压和 10 个外部模拟输入，其中 6 个单端输入  
和 4 个可选差分或单端输入
- 双通道低功耗运算放大器
- 四通道低阻抗接地开关
- 具有同步功能的双通道 12 位数模转换器 (DAC)
- 电压比较器
- 具有高达 160 段对比度控制的集成 LCD 驱动器
- 硬件乘法器支持 32 位运算
- 串行板上编程，无需外部编程电压
- 六通道内部直接存储器访问 (DMA)
- 配有电源电压备用开关的实时时钟 (RTC) 模块
- [器件比较](#) 汇总了系列产品成员

### 1.2 应用

- 模拟传感器系统
- 数字传感器系统
- 手持式仪表
- 医疗诊断仪表
- 手持式工业测试仪
- 测量设备

### 1.3 说明

TI MSP 系列超低功耗微控制器种类繁多，各成员器件配备不同的外设集以满足各类应用的需求。该架构与五种低功耗模式配合使用，是延长便携式测量应用电池寿命的最优选择。该器件具有一个强大的 16 位精简指令集 (RISC) 中央处理器 (CPU)，使用 16 位寄存器以及常数发生器，以便获得最高编码效率。该数控振荡器 (DCO) 可在 3 $\mu$ s（典型值）内从低功率模式唤醒至激活模式。

MSP430FG6626 和 MSP430FG6625 微控制器配有以下外设：1 个高性能 16 位模数转换器 (ADC)、2 个 12 位数模转换器 (DAC)、2 个运算放大器、1 个比较器、2 个通用串行通信接口 (USCI)、USB 2.0、1 个硬件乘法器、DMA、4 个 16 位定时器、1 个具有报警功能的实时时钟 (RTC) 模块、1 个 LCD 驱动器和多达 73 个 I/O 引脚。

MSP430FG6426 和 MSP430FG6425 微控制器配有以下外设：1 个高性能 16 位 ADC、2 个 12 位 DAC、2 个运算放大器、1 个比较器、2 个 USCI、1 个 3.3V LDO、1 个硬件乘法器、DMA、4 个 16 位定时器、1 个具有报警功能的 RTC 模块、1 个 LCD 驱动器和多达 73 个 I/O 引脚。

这些器件的典型应用包括：模拟和数字传感器系统、手持式仪表（例如医疗诊断仪表）、测量设备以及手持式工业测试仪。

有关完整的模块说明，请参阅《MSP430F5xx 和 MSP430F6xx 系列用户指南》

器件信息<sup>(1)</sup>

| 器件型号             | 封装        | 封装尺寸 <sup>(2)</sup> |
|------------------|-----------|---------------------|
| MSP430FG6626IPZ  | PZ (100)  | 14mm x 14mm         |
| MSP430FG6626IZQW | ZQW (113) | 7mm x 7mm           |

(1) 要获得所有可用器件的最新部件、封装和订购信息，请参见封装选项附录（节 9）或浏览 TI 网站 [www.ti.com.cn](http://www.ti.com.cn)。

(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见机械数据（节 9）。

## 1.4 功能方框图

图 1-1 给出了 MSP430FG6626 和 MSP430FG6625 器件的功能方框图。

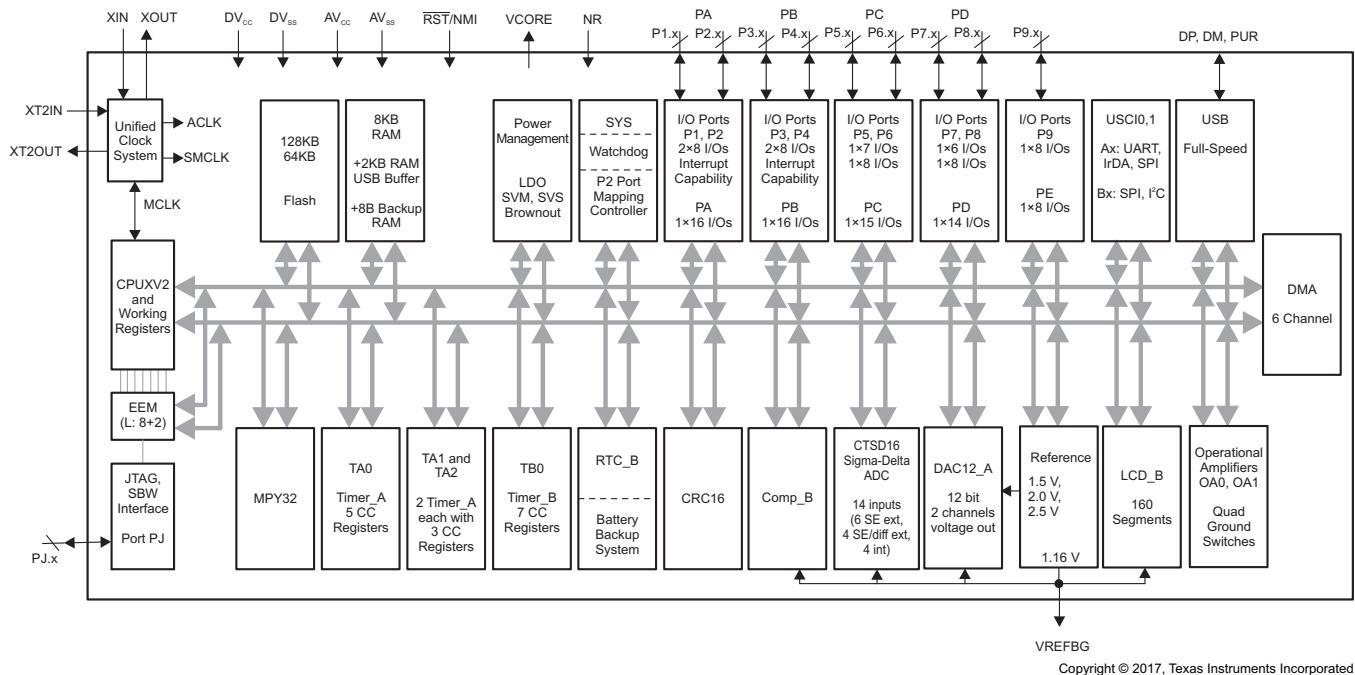


图 1-1. 功能方框图 - MSP430FG6626 和 MSP430FG6625

图 1-2 给出了 MSP430FG6426 和 MSP430FG6425 器件的功能方框图。

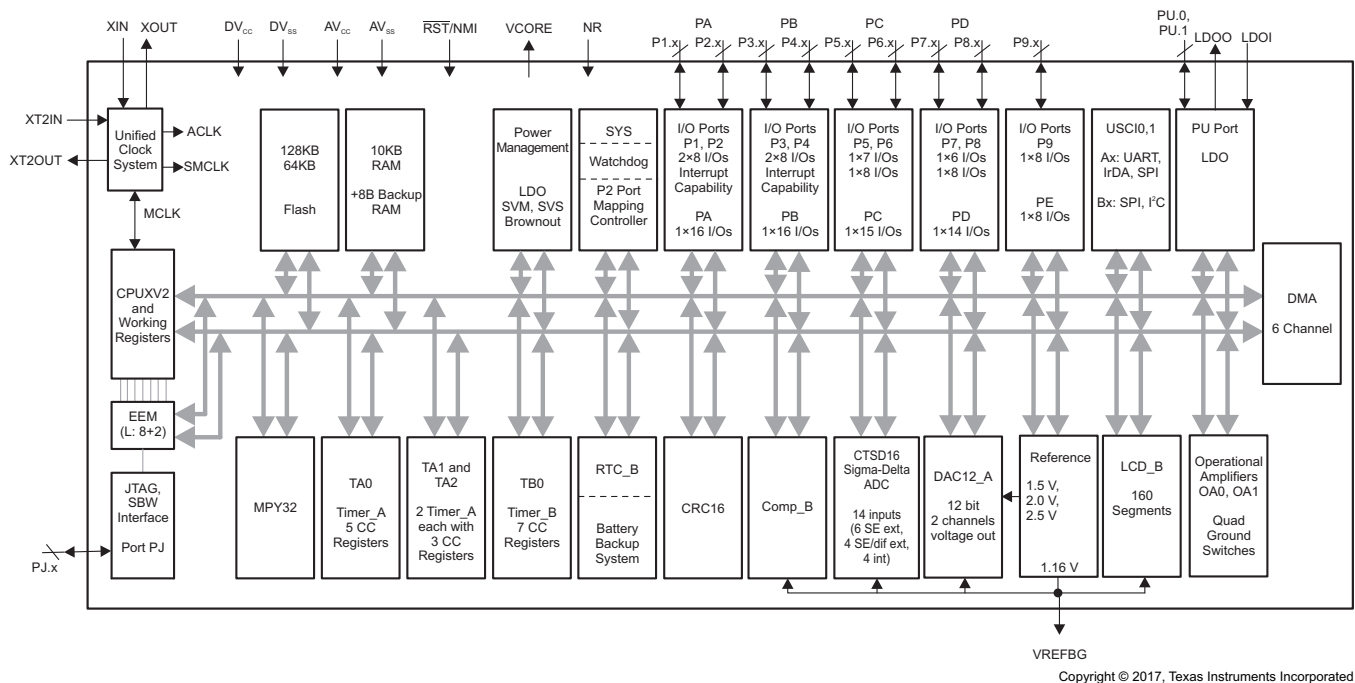


图 1-2. 功能方框图 - MSP430FG6426 和 MSP430FG6425

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## 2 修订历史记录

| Changes from May 23, 2015 to September 26, 2018                                                                                                                                                                                                           | Page                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| • Added <a href="#">Section 3.1, Related Products</a> .....                                                                                                                                                                                               | <a href="#">7</a>   |
| • Added typical conditions statements at the beginning of <a href="#">Section 5, Specifications</a> .....                                                                                                                                                 | <a href="#">27</a>  |
| • Updated notes (1) and (2) and added note (3) in <a href="#">表 5-8, Wake-up Times From Low-Power Modes and Reset</a> .....                                                                                                                               | <a href="#">37</a>  |
| • Removed duplicate symbol and removed note (5) on $R_{i(VREFBG)}$ , $R_{i(VREF+)}$ parameter in <a href="#">Table 5-40, 12-Bit DAC, Reference Input Specifications</a> .....                                                                             | <a href="#">62</a>  |
| • Added "CBPWRMD = 00 or 01" to Test Conditions of the first row of the $t_{EN\_CMP}$ parameter; Added second row for $t_{EN\_CMP}$ with Test Conditions of "CBPWRMD = 10" and MAX value of 100 $\mu$ s in <a href="#">Table 5-47, Comparator_B</a> ..... | <a href="#">68</a>  |
| • Added <a href="#">Section 5.8.18, LDO-PWR (LDO Power System)</a> .....                                                                                                                                                                                  | <a href="#">71</a>  |
| • Throughout document, changed all instances of "bootstrap loader" to "bootloader" .....                                                                                                                                                                  | <a href="#">82</a>  |
| • Changed decoupling capacitor recommendation from "one 10 $\mu$ F and one 100 nF" to "one 1 $\mu$ F and one 100 nF" for consistency with <a href="#">节 7.1.1</a> .....                                                                                   | <a href="#">155</a> |
| • Changed decoupling capacitor recommendation from "one 10 $\mu$ F and one 100 nF" to "one 1 $\mu$ F and one 100 nF" for consistency with <a href="#">节 7.1.1</a> .....                                                                                   | <a href="#">156</a> |
| • Changed decoupling capacitor recommendation from "one 10 $\mu$ F and one 100 nF" to "one 1 $\mu$ F and one 100 nF" for consistency with <a href="#">节 7.1.1</a> .....                                                                                   | <a href="#">159</a> |
| • Added <a href="#">节 7.2.5, DAC12 Peripheral</a> .....                                                                                                                                                                                                   | <a href="#">163</a> |
| • Added <a href="#">节 7.2.6, USB Module</a> .....                                                                                                                                                                                                         | <a href="#">164</a> |
| • Added <a href="#">节 7.2.7, LDO Module</a> .....                                                                                                                                                                                                         | <a href="#">165</a> |
| • 将先前的开发工具支持 部分替换成了 <a href="#">节 8.3, 工具与软件</a> .....                                                                                                                                                                                                    | <a href="#">168</a> |
| • 更改了格式并在 <a href="#">节 8.4 文档支持</a> 中添加了内容 .....                                                                                                                                                                                                         | <a href="#">170</a> |

### 3 Device Comparison

Table 3-1 summarizes the available family members.

**Table 3-1. Device Comparison<sup>(1)(2)</sup>**

| DEVICE       | FLASH<br>(KB) | SRAM<br>(KB) <sup>(3)</sup> | Timer_A <sup>(4)</sup> | Timer_B <sup>(5)</sup> | USCI                             |                                     | CTSD16<br>(Ch) <sup>(6)</sup> | DAC12_A<br>(Ch) | OA | Comp_B<br>(Ch) | USB | I/Os | PACKAGE           |
|--------------|---------------|-----------------------------|------------------------|------------------------|----------------------------------|-------------------------------------|-------------------------------|-----------------|----|----------------|-----|------|-------------------|
|              |               |                             |                        |                        | CHANNEL A:<br>UART, IrDA,<br>SPI | CHANNEL B:<br>SPI, I <sup>2</sup> C |                               |                 |    |                |     |      |                   |
| MSP430FG6626 | 128           | 8 + 2                       | 5, 3, 3                | 7                      | 2                                | 2                                   | 10 ext,<br>5 int              | 2               | 2  | 12             | 1   | 73   | 100 PZ<br>113 ZQW |
| MSP430FG6625 | 64            | 8 + 2                       | 5, 3, 3                | 7                      | 2                                | 2                                   | 10 ext,<br>5 int              | 2               | 2  | 12             | 1   | 73   | 100 PZ<br>113 ZQW |
| MSP430FG6426 | 128           | 10                          | 5, 3, 3                | 7                      | 2                                | 2                                   | 10 ext,<br>5 int              | 2               | 2  | 12             | 0   | 73   | 100 PZ<br>113 ZQW |
| MSP430FG6425 | 64            | 10                          | 5, 3, 3                | 7                      | 2                                | 2                                   | 10 ext,<br>5 int              | 2               | 2  | 12             | 0   | 73   | 100 PZ<br>113 ZQW |

- (1) For the most current package and ordering information, see the *Package Option Addendum* in 节 9, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) The additional 2KB of USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.
- (4) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (5) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (6) ADC inputs consist of a mix of single ended and differential. See the pinning for available input pairs and types.

### 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**Products for TI Microcontrollers** TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

**Products for MSP430 Ultra-Low-Power Microcontrollers** One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

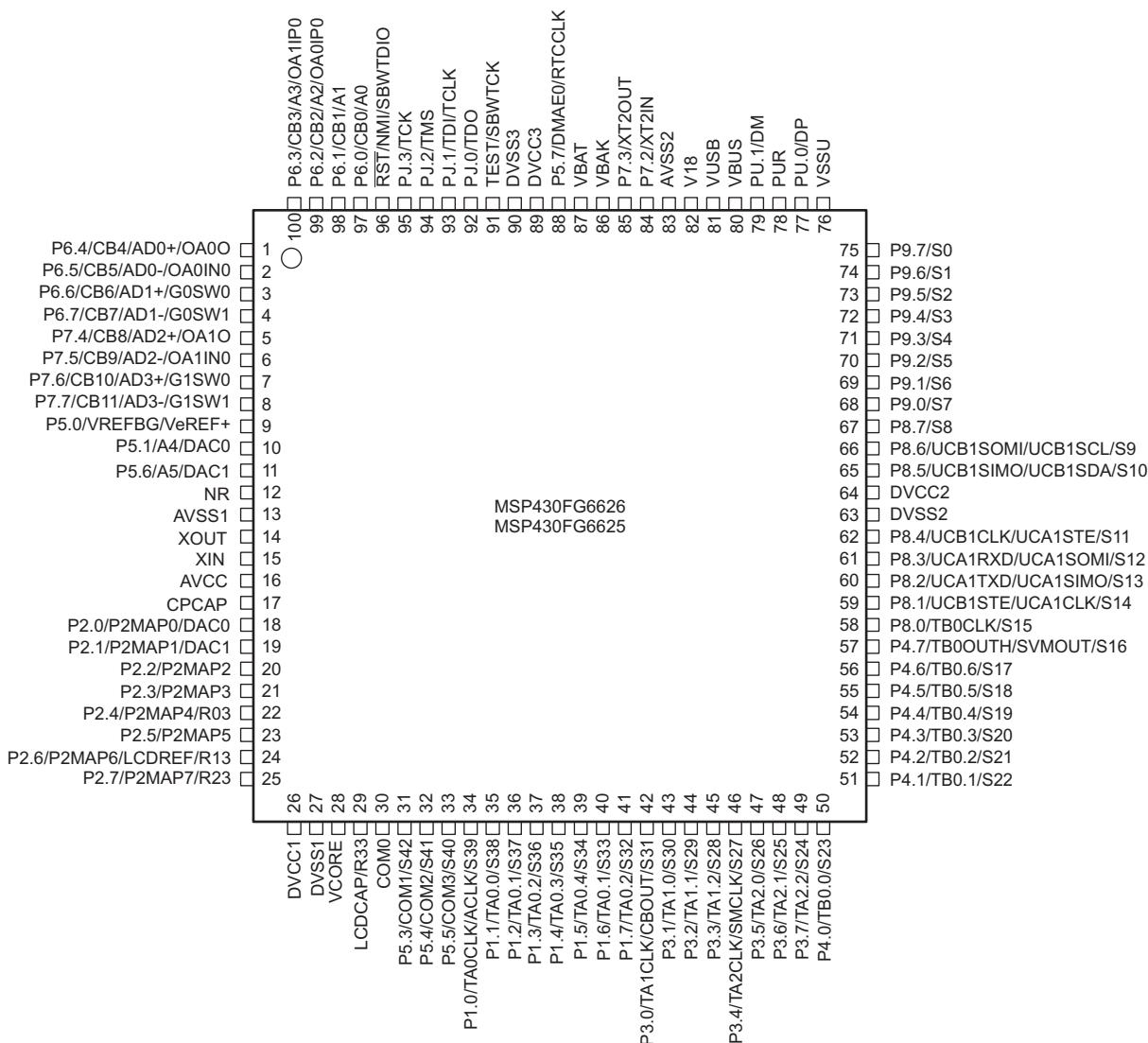
**Companion Products for MSP430FG6626** Review products that are frequently purchased or used with this product.

**Reference Designs for MSP430FG6626** Find reference designs that leverage the best in TI technology to solve your system-level challenges.

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagrams

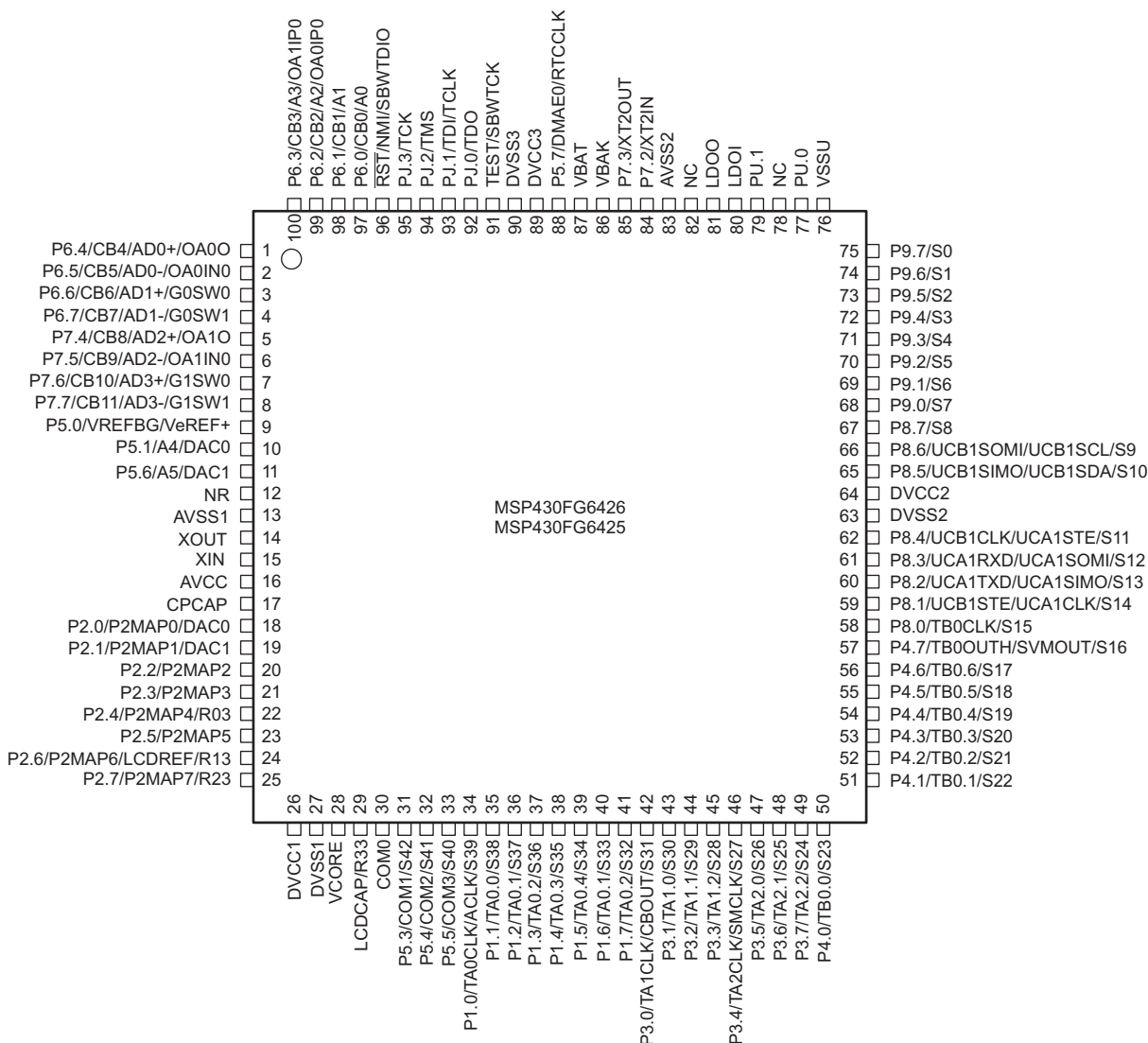
Figure 4-1 shows the pinout for the MSP430FG6626 and MSP430FG6625 devices in the 100-pin PZ package.



CAUTION: LCDCAP/R33 must be connected to DV<sub>SS</sub> if not used.

Figure 4-1. 100-Pin PZ Package (Top View), MSP430FG6626IPZ, MSP430FG6625IPZ

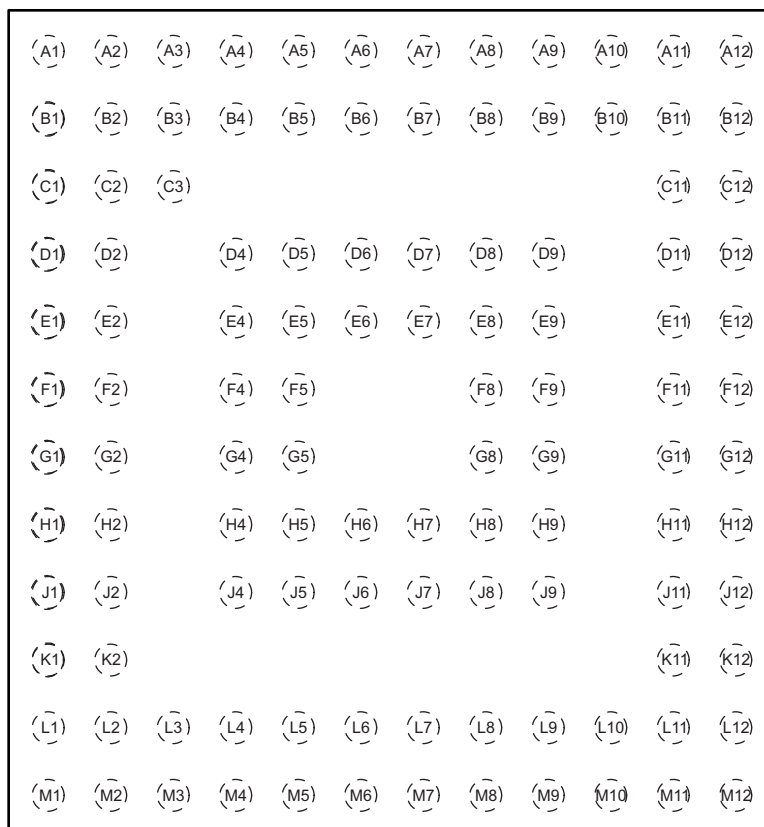
Figure 4-2 shows the pinout for the MSP430FG6426 and MSP430FG6425 devices in the 100-pin PZ package.



CAUTION: LCDCAP/R33 must be connected to DV<sub>SS</sub> if not used.

**Figure 4-2. 100-Pin PZ Package (Top View), MSP430FG6426IPZ, MSP430FG6425IPZ**

Figure 4-3 shows the pinout for the 113-pin ZQW package.



NOTE: For terminal assignments, see [Table 4-2](#).

**Figure 4-3. 113-Pin ZQW Package (Top View), MSP430FG6626IZQW, MSP430FG6625IZQW, MSP430FG6426IZQW, MSP430FG6425IZQW**

## 4.2 Pin Attributes

Table 4-1 describes the attributes of the pins.

**Table 4-1. Pin Attributes**

| PIN NO. |     | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6) (7)</sup> |
|---------|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|------------------------------------------|
| PZ      | ZQW |                                |                            |                            |                             |                                          |
| 1       | A1  | P6.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB4                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD0+                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | OA0O                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 2       | B2  | P6.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB5                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD0-                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | OA0IN0                         | I                          | Analog                     | DVCC                        | N/A                                      |
| 3       | B1  | P6.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB6                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD1+                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | G0SW0                          | I                          | Analog                     | DVCC                        | N/A                                      |
| 4       | C3  | P6.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB7                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD1-                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | G0SW1                          | I                          | Analog                     | DVCC                        | N/A                                      |
| 5       | C2  | P7.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB8                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD2+                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | OA1O                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 6       | C1  | P7.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB9                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD2-                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | OA1IN0                         | I                          | Analog                     | DVCC                        | N/A                                      |
| 7       | D4  | P7.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB10                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD3+                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | G1SW0                          | I                          | Analog                     | DVCC                        | N/A                                      |
| 8       | D2  | P7.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB11                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | AD3-                           | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | G1SW1                          | I                          | Analog                     | DVCC                        | N/A                                      |

(1) For each multiplexed pin, the signal that is listed first in this table is the reset default.

(2) To determine the pin mux encodings for each pin, refer to [§ 6.13, Input/Output Schematics](#).

(3) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power

(4) Buffer Types: LVC MOS, HVC MOS, Analog, or Power (see [Table 4-3](#) for details).

(5) The power source shown in this table is the I/O power source, which may differ from the module power source.

(6) Reset States:

OFF = High-impedance input with pullup or pulldown disabled (if available)

HiZ = High-impedance (neither input nor output)

PD = High-impedance input with pulldown enabled

PU = High-impedance input with pullup enabled

DRIVE0 = Drive output low

DRIVE1 = Drive output high

N/A = Not applicable

(7) For Debug pins: Emu = with emulator attached at reset, No Emu = without emulator attached at reset

**Table 4-1. Pin Attributes (continued)**

| PIN NO. |        | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6) (7)</sup> |
|---------|--------|--------------------------------|----------------------------|----------------------------|-----------------------------|------------------------------------------|
| PZ      | ZQW    |                                |                            |                            |                             |                                          |
| 9       | D1     | P5.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | VREFBG                         | O                          | Analog                     | DVCC                        | N/A                                      |
|         |        | VeREF+                         | I                          | Analog                     | N/A                         | N/A                                      |
| 10      | E4     | P5.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | A4                             | I                          | Analog                     | DVCC                        | N/A                                      |
|         |        | DAC0                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 11      | E2     | P5.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | A5                             | I                          | Analog                     | DVCC                        | N/A                                      |
|         |        | DAC1                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 12      | E1     | NR                             | I                          | Analog                     | N/A                         | N/A                                      |
| 13      | F2     | AVSS1                          | P                          | Power                      | N/A                         | N/A                                      |
| 14      | F1     | XOUT                           | O                          | Analog                     | N/A                         | N/A                                      |
| 15      | G1     | XIN                            | I                          | Analog                     | N/A                         | N/A                                      |
| 16      | H1, G2 | AVCC                           | P                          | Power                      | N/A                         | N/A                                      |
| 17      | G4     | CPCAP                          | I/O                        | Analog                     | DVCC                        | N/A                                      |
| 18      | H2     | P2.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP0                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |        | DAC0                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 19      | J1     | P2.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP1                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |        | DAC1                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 20      | H4     | P2.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP2                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
| 21      | J2     | P2.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP3                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
| 22      | K1     | P2.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP4                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |        | R03                            | I/O                        | Analog                     | DVCC                        | N/A                                      |
| 23      | K2     | P2.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP5                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
| 24      | L2     | P2.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP6                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |        | LCDREF                         | I                          | Analog                     | N/A                         | N/A                                      |
|         |        | R13                            | I/O                        | Analog                     | DVCC                        | N/A                                      |
| 25      | L3     | P2.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | P2MAP7                         | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |        | R23                            | I/O                        | Analog                     | DVCC                        | N/A                                      |
| 26      | L1     | DVCC1                          | P                          | Power                      | N/A                         | N/A                                      |
| 27      | M1     | DVSS1                          | P                          | Power                      | N/A                         | N/A                                      |
| 28      | M2     | VCORE                          | P                          | Power                      | DVCC                        | N/A                                      |
| 29      | M3     | LCDCAP                         | I/O                        | Analog                     | DVCC                        | N/A                                      |
|         |        | R33                            | I/O                        | Analog                     | DVCC                        | N/A                                      |
| 30      | J4     | COM0                           | O                          | Analog                     | DVCC                        | N/A                                      |
| 31      | L4     | P5.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |        | COM1                           | O                          | Analog                     | DVCC                        | N/A                                      |
|         |        | S42                            | O                          | Analog                     | DVCC                        | N/A                                      |

**Table 4-1. Pin Attributes (continued)**

| PIN NO. |     | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6) (7)</sup> |
|---------|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|------------------------------------------|
| PZ      | ZQW |                                |                            |                            |                             |                                          |
| 32      | M4  | P5.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | COM2                           | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S41                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 33      | J5  | P5.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | COM3                           | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S40                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 34      | L5  | P1.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0CLK                         | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | ACLK                           | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S39                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 35      | M5  | P1.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.0                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | BSLTX                          | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S38                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 36      | J6  | P1.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.1                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | BSLRX                          | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S37                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 37      | H6  | P1.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.2                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S36                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 38      | M6  | P1.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.3                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S35                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 39      | L6  | P1.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.4                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S34                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 40      | J7  | P1.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.1                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S33                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 41      | M7  | P1.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA0.2                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S32                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 42      | L7  | P3.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA1CLK                         | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | CBOUT                          | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S31                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 43      | H7  | P3.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA1.0                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S30                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 44      | M8  | P3.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA1.1                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S29                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 45      | L8  | P3.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA1.2                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S28                            | O                          | Analog                     | DVCC                        | N/A                                      |

**Table 4-1. Pin Attributes (continued)**

| PIN NO. |     | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6) (7)</sup> |
|---------|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|------------------------------------------|
| PZ      | ZQW |                                |                            |                            |                             |                                          |
| 46      | J8  | P3.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA2CLK                         | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | SMCLK                          | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S27                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 47      | M9  | P3.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA2.0                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S26                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 48      | L9  | P3.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA2.1                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S25                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 49      | M10 | P3.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TA2.2                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S24                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 50      | J9  | P4.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.0                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S23                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 51      | M11 | P4.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.1                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S22                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 52      | L10 | P4.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.2                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S21                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 53      | M12 | P4.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.3                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S20                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 54      | L12 | P4.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.4                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S19                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 55      | L11 | P4.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.5                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S18                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 56      | K11 | P4.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0.6                          | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S17                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 57      | K12 | P4.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0OUTH                        | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | SVMOUT                         | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S16                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 58      | J11 | P8.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TB0CLK                         | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S15                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 59      | J12 | P8.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | UCB1STE                        | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | UCA1CLK                        | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | S14                            | O                          | Analog                     | DVCC                        | N/A                                      |

**Table 4-1. Pin Attributes (continued)**

| PIN NO. |          | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6) (7)</sup> |
|---------|----------|--------------------------------|----------------------------|----------------------------|-----------------------------|------------------------------------------|
| PZ      | ZQW      |                                |                            |                            |                             |                                          |
| 60      | H11      | P8.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | UCA1TXD                        | O                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | UCA1SIMO                       | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | S13                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 61      | H12      | P8.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | UCA1RXD                        | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | UCA1SOMI                       | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | S12                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 62      | G11      | P8.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | UCB1CLK                        | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | UCA1STE                        | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | S11                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 63      | G12      | DVSS2                          | P                          | Power                      | N/A                         | N/A                                      |
| 64      | F12      | DVCC2                          | P                          | Power                      | N/A                         | N/A                                      |
| 65      | F11      | P8.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | UCB1SIMO                       | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | UCB1SDA                        | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | S10                            | O                          | Analog                     | DVCC                        | N/A                                      |
| 66      | G9       | P8.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | UCB1SOMI                       | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | UCB1SCL                        | I/O                        | LVC MOS                    | DVCC                        | N/A                                      |
|         |          | S9                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 67      | E12      | P8.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S8                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 68      | E11      | P9.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S7                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 69      | F9       | P9.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S6                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 70      | D12      | P9.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S5                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 71      | D11      | P9.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S4                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 72      | E9       | P9.4                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S3                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 73      | C12      | P9.5                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S2                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 74      | C11      | P9.6                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S1                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 75      | D9       | P9.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |          | S0                             | O                          | Analog                     | DVCC                        | N/A                                      |
| 76      | B11, B12 | VSSU                           | P                          | Power                      | N/A                         | N/A                                      |
| 77      | A12      | PU.0                           | I/O                        | HVC MOS                    | VBUS                        | HiZ                                      |
|         |          | DP                             | I/O                        | HVC MOS                    | VBUS                        | N/A                                      |
| 78      | B10      | PUR (FG662x only)              | I/O                        | HVC MOS/open-drain         | VBUS                        | HiZ                                      |
|         |          | NC (FG642x only)               | I/O                        | N/A                        | N/A                         | N/A                                      |

**Table 4-1. Pin Attributes (continued)**

| PIN NO. |     | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6) (7)</sup> |
|---------|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|------------------------------------------|
| PZ      | ZQW |                                |                            |                            |                             |                                          |
| 79      | A11 | PU.1                           | I/O                        | HVCMOS                     | VBUS                        | HiZ                                      |
|         |     | DM                             | I/O                        | HVCMOS                     | VBUS                        | N/A                                      |
| 80      | A10 | VBUS                           | I                          | Power                      | N/A                         | N/A                                      |
|         |     | LDOI                           | I                          | Analog                     | External                    | N/A                                      |
| 81      | A9  | VUSB                           | O                          | Power                      | N/A                         | N/A                                      |
|         |     | LDOO                           | O                          | Analog                     | VBUS                        | N/A                                      |
| 82      | B9  | V18 (FG662x only)              | O                          | Power                      | N/A                         | N/A                                      |
|         |     | NC (FG642x only)               | –                          | N/A                        | N/A                         | N/A                                      |
| 83      | A8  | AVSS2                          | P                          | Power                      | N/A                         | N/A                                      |
| 84      | B8  | P7.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | XT2IN                          | I                          | Analog                     | DVCC                        | N/A                                      |
| 85      | B7  | P7.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | XT2OUT                         | O                          | Analog                     | DVCC                        | N/A                                      |
| 86      | A7  | VBAK                           | I/O                        | Analog                     | N/A                         | N/A                                      |
| 87      | D8  | VBAT                           | P                          | Power                      | N/A                         | N/A                                      |
| 88      | D7  | P5.7                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | DMAE0                          | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | RTCCLK                         | O                          | LVC MOS                    | DVCC                        | N/A                                      |
| 89      | A6  | DVCC3                          | P                          | Power                      | N/A                         | N/A                                      |
| 90      | A5  | DVSS3                          | P                          | Power                      | N/A                         | N/A                                      |
| 91      | B6  | TEST                           | I                          | LVC MOS                    | DVCC                        | No Emu: PD<br>Emu: PD                    |
|         |     | SBWTCK                         | I                          | LVC MOS                    | DVCC                        | N/A                                      |
| 92      | B5  | PJ.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TDO                            | O                          | LVC MOS                    | DVCC                        | No Emu: OFF<br>Emu: DRIVE0               |
| 93      | A4  | PJ.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TDI                            | I                          | LVC MOS                    | DVCC                        | No Emu: OFF<br>Emu: PU                   |
|         |     | TCLK                           | I                          | LVC MOS                    | DVCC                        | No Emu: OFF<br>Emu: OFF                  |
| 94      | E7  | PJ.2                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TMS                            | I                          | LVC MOS                    | DVCC                        | No Emu: OFF<br>Emu: PU                   |
| 95      | D6  | PJ.3                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | TCK                            | I                          | LVC MOS                    | DVCC                        | No Emu: OFF<br>Emu: PU                   |
| 96      | A3  | $\overline{\text{RST}}$        | I/O                        | LVC MOS                    | DVCC                        | PU                                       |
|         |     | NMI                            | I                          | LVC MOS                    | DVCC                        | N/A                                      |
|         |     | SBWTDIO                        | I/O                        | LVC MOS                    | DVCC                        | PU                                       |
| 97      | B4  | P6.0                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB0                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | A0                             | I                          | Analog                     | DVCC                        | N/A                                      |
| 98      | B3  | P6.1                           | I/O                        | LVC MOS                    | DVCC                        | OFF                                      |
|         |     | CB1                            | I                          | Analog                     | DVCC                        | N/A                                      |
|         |     | A1                             | I                          | Analog                     | DVCC                        | N/A                                      |

**Table 4-1. Pin Attributes (continued)**

| PIN NO. |                                                     | SIGNAL NAME <sup>(1)</sup> <sup>(2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6)</sup> <sup>(7)</sup> |
|---------|-----------------------------------------------------|-------------------------------------------|----------------------------|----------------------------|-----------------------------|-----------------------------------------------------|
| PZ      | ZQW                                                 |                                           |                            |                            |                             |                                                     |
| 99      | A2                                                  | P6.2                                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                                 |
|         |                                                     | CB2                                       | I                          | Analog                     | DVCC                        | N/A                                                 |
|         |                                                     | A2                                        | I                          | Analog                     | DVCC                        | N/A                                                 |
|         |                                                     | OA0IP0                                    | I                          | Analog                     | DVCC                        | N/A                                                 |
| 100     | D5                                                  | P6.3                                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                                 |
|         |                                                     | CB3                                       | I                          | Analog                     | DVCC                        | N/A                                                 |
|         |                                                     | A3                                        | I                          | Analog                     | DVCC                        | N/A                                                 |
|         |                                                     | OA1IP0                                    | I                          | Analog                     | DVCC                        | N/A                                                 |
| N/A     | E5, E6, E8,<br>F4, F5, F8,<br>G5, G8, H5,<br>H8, H9 | Reserved                                  | -                          | —                          | —                           | —                                                   |

### 4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

**Table 4-2. Signal Descriptions**

| FUNCTION    | SIGNAL NAME | PIN NO. |     | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                       |
|-------------|-------------|---------|-----|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             |             | PZ      | ZQW |                         |                                                                                                                                                                   |
| ADC         | A0          | 97      | B4  | I                       | ADC analog single ended input A0                                                                                                                                  |
|             | A1          | 98      | B3  | I                       | ADC analog single ended input A1                                                                                                                                  |
|             | A2          | 99      | A2  | I                       | ADC analog single ended input A2                                                                                                                                  |
|             | A3          | 100     | D5  | I                       | ADC analog single ended input A3                                                                                                                                  |
|             | A4          | 10      | E4  | I                       | ADC analog single ended input A4                                                                                                                                  |
|             | A5          | 11      | E2  | I                       | ADC analog single ended input A5                                                                                                                                  |
|             | AD0+        | 1       | A1  | I                       | ADC positive analog differential input AD0+                                                                                                                       |
|             | AD0-        | 2       | B2  | I                       | ADC negative analog differential input AD0-                                                                                                                       |
|             | AD1+        | 3       | B1  | I                       | ADC positive analog differential input AD1+                                                                                                                       |
|             | AD1-        | 4       | C3  | I                       | ADC negative analog differential input AD1-                                                                                                                       |
|             | AD2+        | 5       | C2  | I                       | ADC positive analog differential input AD2+                                                                                                                       |
|             | AD2-        | 6       | C1  | I                       | ADC negative analog differential input AD2-                                                                                                                       |
|             | AD3+        | 7       | D4  | I                       | ADC positive analog differential input AD3+                                                                                                                       |
|             | AD3-        | 8       | D2  | I                       | ADC negative analog differential input AD3-                                                                                                                       |
|             | VeREF+      | 9       | D1  | I                       | Input for an external reference voltage to the ADC and DAC                                                                                                        |
| BSL         | BSLRX       | 36      | J6  | I                       | BSL receive input                                                                                                                                                 |
|             | BSLTX       | 35      | M5  | O                       | BSL transmit output                                                                                                                                               |
| Backup      | VBAK        | 86      | A7  | I/O                     | Capacitor for backup subsystem. Do not load this pin externally. For capacitor values, see C <sub>BAK</sub> in <a href="#">Recommended Operating Conditions</a> . |
|             | VBAT        | 87      | D8  | P                       | Backup or secondary supply voltage. If backup voltage is not supplied, connect to DVCC externally.                                                                |
| Charge Pump | CPCAP       | 17      | G4  | I/O                     | Capacitor for op amp and CTSD16 rail-to-rail charge pump                                                                                                          |
| Clock       | ACLK        | 34      | L5  | O                       | ACLK output (divided by 1, 2, 4, 8, 16, or 32)                                                                                                                    |
|             | RTCCLK      | 88      | D7  | O                       | RTCCLK output                                                                                                                                                     |
|             | SMCLK       | 46      | J8  | O                       | SMCLK output                                                                                                                                                      |
|             | XIN         | 15      | G1  | I                       | Input terminal for crystal oscillator XT1                                                                                                                         |
|             | XOUT        | 14      | F1  | O                       | Output terminal of crystal oscillator XT1                                                                                                                         |
|             | XT2IN       | 84      | B8  | I                       | Input terminal for crystal oscillator XT2                                                                                                                         |
|             | XT2OUT      | 85      | B7  | O                       | Output terminal of crystal oscillator XT2                                                                                                                         |
| Comparator  | CB0         | 97      | B4  | I                       | Comparator_B input CB0                                                                                                                                            |
|             | CB1         | 98      | B3  | I                       | Comparator_B input CB1                                                                                                                                            |
|             | CB2         | 99      | A2  | I                       | Comparator_B input CB2                                                                                                                                            |
|             | CB3         | 100     | D5  | I                       | Comparator_B input CB3                                                                                                                                            |
|             | CB4         | 1       | A1  | I                       | Comparator_B input CB4                                                                                                                                            |
|             | CB5         | 2       | B2  | I                       | Comparator_B input CB5                                                                                                                                            |
|             | CB6         | 3       | B1  | I                       | Comparator_B input CB6                                                                                                                                            |
|             | CB7         | 4       | C3  | I                       | Comparator_B input CB7                                                                                                                                            |
|             | CB8         | 5       | C2  | I                       | Comparator_B input CB8                                                                                                                                            |
|             | CB9         | 6       | C1  | I                       | Comparator_B input CB9                                                                                                                                            |
|             | CB10        | 7       | D4  | I                       | Comparator_B input CB10                                                                                                                                           |
|             | CB11        | 8       | D2  | I                       | Comparator_B input CB11                                                                                                                                           |
|             | CBOUT       | 42      | L7  | O                       | Comparator_B output                                                                                                                                               |

(1) I = input, O = output, I/O = input or output, P = power

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO.  |          | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                                                     |
|----------|-------------|----------|----------|-------------------------|---------------------------------------------------------------------------------|
|          |             | PZ       | ZQW      |                         |                                                                                 |
| DAC      | DAC0        | 10<br>18 | E4<br>H2 | O                       | DAC output channel 0                                                            |
|          | DAC1        | 11<br>19 | E2<br>J1 | O                       | DAC output channel 1                                                            |
| DMA      | DMAE0       | 88       | D7       | I                       | DMA external trigger input                                                      |
| Debug    | SBWTCK      | 91       | B6       | I                       | Spy-Bi-Wire input clock                                                         |
|          | TCK         | 95       | D6       | I                       | Test clock                                                                      |
|          | TCLK        | 93       | A4       | I                       | Test clock input                                                                |
|          | TDI         | 93       | A4       | I                       | Test data input                                                                 |
|          | TDO         | 92       | B5       | O                       | Test data output                                                                |
|          | TEST        | 91       | B6       | I                       | Test mode pin; selects digital I/O on JTAG pins                                 |
|          | TMS         | 94       | E7       | I                       | Test mode select                                                                |
|          | SBWTDIO     | 96       | A3       | I/O                     | Spy-Bi-Wire data input/output                                                   |
| GPIO     | P1.0        | 34       | L5       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.1        | 35       | M5       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.2        | 36       | J6       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.3        | 37       | H6       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.4        | 38       | M6       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.5        | 39       | L6       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.6        | 40       | J7       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P1.7        | 41       | M7       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P2.0        | 18       | H2       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.1        | 19       | J1       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.2        | 20       | H4       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.3        | 21       | J2       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.4        | 22       | K1       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.5        | 23       | K2       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.6        | 24       | L2       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P2.7        | 25       | L3       | I/O                     | General-purpose digital I/O with port interrupt and mappable secondary function |
|          | P3.0        | 42       | L7       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.1        | 43       | H7       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.2        | 44       | M8       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.3        | 45       | L8       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.4        | 46       | J8       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.5        | 47       | M9       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.6        | 48       | L9       | I/O                     | General-purpose digital I/O with port interrupt                                 |
|          | P3.7        | 49       | M10      | I/O                     | General-purpose digital I/O with port interrupt                                 |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO. |     | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                     |
|----------|-------------|---------|-----|-------------------------|-------------------------------------------------|
|          |             | PZ      | ZQW |                         |                                                 |
| GPIO     | P4.0        | 50      | J9  | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.1        | 51      | M11 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.2        | 52      | L10 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.3        | 53      | M12 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.4        | 54      | L12 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.5        | 55      | L11 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.6        | 56      | K11 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P4.7        | 57      | K12 | I/O                     | General-purpose digital I/O with port interrupt |
|          | P5.0        | 9       | D1  | I/O                     | General-purpose digital I/O                     |
|          | P5.1        | 10      | E4  | I/O                     | General-purpose digital I/O                     |
|          | P5.3        | 31      | L4  | I/O                     | General-purpose digital I/O                     |
|          | P5.4        | 32      | M4  | I/O                     | General-purpose digital I/O                     |
|          | P5.5        | 33      | J5  | I/O                     | General-purpose digital I/O                     |
|          | P5.6        | 11      | E2  | I/O                     | General-purpose digital I/O                     |
|          | P5.7        | 88      | D7  | I/O                     | General-purpose digital I/O                     |
|          | P6.0        | 97      | B4  | I/O                     | General-purpose digital I/O                     |
|          | P6.1        | 98      | B3  | I/O                     | General-purpose digital I/O                     |
|          | P6.2        | 99      | A2  | I/O                     | General-purpose digital I/O                     |
|          | P6.3        | 100     | D5  | I/O                     | General-purpose digital I/O                     |
|          | P6.4        | 1       | A1  | I/O                     | General-purpose digital I/O                     |
|          | P6.5        | 2       | B2  | I/O                     | General-purpose digital I/O                     |
|          | P6.6        | 3       | B1  | I/O                     | General-purpose digital I/O                     |
|          | P6.7        | 4       | C3  | I/O                     | General-purpose digital I/O                     |
|          | P7.2        | 84      | B8  | I/O                     | General-purpose digital I/O                     |
|          | P7.3        | 85      | B7  | I/O                     | General-purpose digital I/O                     |
|          | P7.4        | 5       | C2  | I/O                     | General-purpose digital I/O                     |
|          | P7.5        | 6       | C1  | I/O                     | General-purpose digital I/O                     |
|          | P7.6        | 7       | D4  | I/O                     | General-purpose digital I/O                     |
|          | P7.7        | 8       | D2  | I/O                     | General-purpose digital I/O                     |
|          | P8.0        | 58      | J11 | I/O                     | General-purpose digital I/O                     |
|          | P8.1        | 59      | J12 | I/O                     | General-purpose digital I/O                     |
|          | P8.2        | 60      | H11 | I/O                     | General-purpose digital I/O                     |
|          | P8.3        | 61      | H12 | I/O                     | General-purpose digital I/O                     |
|          | P8.4        | 62      | G11 | I/O                     | General-purpose digital I/O                     |
|          | P8.5        | 65      | F11 | I/O                     | General-purpose digital I/O                     |
|          | P8.6        | 66      | G9  | I/O                     | General-purpose digital I/O                     |
|          | P8.7        | 67      | E12 | I/O                     | General-purpose digital I/O                     |
|          | P9.0        | 68      | E11 | I/O                     | General-purpose digital I/O                     |
|          | P9.1        | 69      | F9  | I/O                     | General-purpose digital I/O                     |
|          | P9.2        | 70      | D12 | I/O                     | General-purpose digital I/O                     |
|          | P9.3        | 71      | D11 | I/O                     | General-purpose digital I/O                     |
|          | P9.4        | 72      | E9  | I/O                     | General-purpose digital I/O                     |
|          | P9.5        | 73      | C12 | I/O                     | General-purpose digital I/O                     |
|          | P9.6        | 74      | C11 | I/O                     | General-purpose digital I/O                     |
|          | P9.7        | 75      | D9  | I/O                     | General-purpose digital I/O                     |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION         | SIGNAL NAME | PIN NO. |     | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                |
|------------------|-------------|---------|-----|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
|                  |             | PZ      | ZQW |                         |                                                                                                                                            |
| GPIO             | PJ.0        | 92      | B5  | I/O                     | General-purpose digital I/O                                                                                                                |
|                  | PJ.1        | 93      | A4  | I/O                     | General-purpose digital I/O                                                                                                                |
|                  | PJ.2        | 94      | E7  | I/O                     | General-purpose digital I/O                                                                                                                |
|                  | PJ.3        | 95      | D6  | I/O                     | General-purpose digital I/O                                                                                                                |
|                  | PU.0        | 77      | A12 | I/O                     | General-purpose digital I/O - controlled by USB control register (FG662x devices) or PU control register                                   |
|                  | PU.1        | 79      | A11 | I/O                     | General-purpose digital I/O - controlled by USB control register (FG662x devices) or PU control register                                   |
| Ground Switch    | G0SW0       | 3       | B1  | I                       | Analog switch to AVSS. Internally connected to ADC positive analog differential input AD1+.                                                |
|                  | G0SW1       | 4       | C3  | I                       | Analog switch to AVSS. Internally connected to ADC negative analog differential input AD1-.                                                |
|                  | G1SW0       | 7       | D4  | I                       | Analog switch to AVSS. Internally connected to ADC positive analog differential input AD3+.                                                |
|                  | G1SW1       | 8       | D2  | I                       | Analog switch to AVSS. Internally connected to ADC negative analog differential input AD3-.                                                |
| I <sup>2</sup> C | UCB1SCL     | 66      | G9  | I/O                     | USCI_B1 I <sup>2</sup> C clock                                                                                                             |
|                  | UCB1SDA     | 65      | F11 | I/O                     | USCI_B1 I <sup>2</sup> C data                                                                                                              |
| LCD              | COM0        | 30      | J4  | O                       | LCD common output COM0 for LCD backplane                                                                                                   |
|                  | COM1        | 31      | L4  | O                       | LCD common output COM1 for LCD backplane                                                                                                   |
|                  | COM2        | 32      | M4  | O                       | LCD common output COM2 for LCD backplane                                                                                                   |
|                  | COM3        | 33      | J5  | I/O                     | LCD common output COM3 for LCD backplane                                                                                                   |
|                  | LDCAP       | 29      | M3  | I/O                     | LCD capacitor connection<br><b>CAUTION:</b> LDCAP/R33 must be connected to DV <sub>SS</sub> if not used.                                   |
|                  | LCDREF      | 24      | L2  | I                       | External reference voltage input for regulated LCD voltage                                                                                 |
|                  | R03         | 22      | K1  | I/O                     | Input/output port of lowest analog LCD voltage (V5)                                                                                        |
|                  | R13         | 24      | L2  | I/O                     | Input/output port of third most positive analog LCD voltage (V3 or V4)                                                                     |
|                  | R23         | 25      | L3  | I/O                     | Input/output port of second most positive analog LCD voltage (V2)                                                                          |
|                  | R33         | 29      | M3  | I/O                     | Input/output port of most positive analog LCD voltage (V1)<br><b>CAUTION:</b> LDCAP/R33 must be connected to DV <sub>SS</sub> if not used. |
|                  | S0          | 75      | D9  | O                       | LCD segment output S0                                                                                                                      |
|                  | S1          | 74      | C11 | O                       | LCD segment output S1                                                                                                                      |
|                  | S2          | 73      | C12 | O                       | LCD segment output S2                                                                                                                      |
|                  | S3          | 72      | E9  | O                       | LCD segment output S3                                                                                                                      |
|                  | S4          | 71      | D11 | O                       | LCD segment output S4                                                                                                                      |
|                  | S5          | 70      | D12 | O                       | LCD segment output S5                                                                                                                      |
|                  | S6          | 69      | F9  | O                       | LCD segment output S6                                                                                                                      |
|                  | S7          | 68      | E11 | O                       | LCD segment output S7                                                                                                                      |
|                  | S8          | 67      | E12 | O                       | LCD segment output S8                                                                                                                      |
|                  | S9          | 66      | G9  | O                       | LCD segment output S9                                                                                                                      |
|                  | S10         | 65      | F11 | O                       | LCD segment output S10                                                                                                                     |
|                  | S11         | 62      | G11 | O                       | LCD segment output S11                                                                                                                     |
|                  | S12         | 61      | H12 | O                       | LCD segment output S12                                                                                                                     |
|                  | S13         | 60      | H11 | O                       | LCD segment output S13                                                                                                                     |
|                  | S14         | 59      | J12 | O                       | LCD segment output S14                                                                                                                     |
|                  | S15         | 58      | J11 | O                       | LCD segment output S15                                                                                                                     |
|                  | S16         | 57      | K12 | O                       | LCD segment output S16                                                                                                                     |
|                  | S17         | 56      | K11 | O                       | LCD segment output S17                                                                                                                     |
|                  | S18         | 55      | L11 | O                       | LCD segment output S18                                                                                                                     |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION        | SIGNAL NAME | PIN NO. |     | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                    |
|-----------------|-------------|---------|-----|-------------------------|--------------------------------------------------------------------------------------------------------------------------------|
|                 |             | PZ      | ZQW |                         |                                                                                                                                |
| LCD             | S19         | 54      | L12 | O                       | LCD segment output S19                                                                                                         |
|                 | S20         | 53      | M12 | O                       | LCD segment output S20                                                                                                         |
|                 | S21         | 52      | L10 | O                       | LCD segment output S21                                                                                                         |
|                 | S22         | 51      | M11 | O                       | LCD segment output S22                                                                                                         |
|                 | S23         | 50      | J9  | O                       | LCD segment output S23                                                                                                         |
|                 | S24         | 49      | M10 | O                       | LCD segment output S24                                                                                                         |
|                 | S25         | 48      | L9  | O                       | LCD segment output S25                                                                                                         |
|                 | S26         | 47      | M9  | O                       | LCD segment output S26                                                                                                         |
|                 | S27         | 46      | J8  | O                       | LCD segment output S27                                                                                                         |
|                 | S28         | 45      | L8  | O                       | LCD segment output S28                                                                                                         |
|                 | S29         | 44      | M8  | O                       | LCD segment output S29                                                                                                         |
|                 | S30         | 43      | H7  | O                       | LCD segment output S30                                                                                                         |
|                 | S31         | 42      | L7  | O                       | LCD segment output S31                                                                                                         |
|                 | S32         | 41      | M7  | O                       | LCD segment output S32                                                                                                         |
|                 | S33         | 40      | J7  | O                       | LCD segment output S33                                                                                                         |
|                 | S34         | 39      | L6  | O                       | LCD segment output S34                                                                                                         |
|                 | S35         | 38      | M6  | O                       | LCD segment output S35                                                                                                         |
|                 | S36         | 37      | H6  | O                       | LCD segment output S36                                                                                                         |
|                 | S37         | 36      | J6  | O                       | LCD segment output S37                                                                                                         |
|                 | S38         | 35      | M5  | O                       | LCD segment output S38                                                                                                         |
|                 | S39         | 34      | L5  | O                       | LCD segment output S39                                                                                                         |
|                 | S40         | 33      | J5  | O                       | LCD segment output S40                                                                                                         |
|                 | S41         | 32      | M4  | O                       | LCD segment output S41                                                                                                         |
|                 | S42         | 31      | L4  | O                       | LCD segment output S42                                                                                                         |
| Mappable        | P2MAP0      | 18      | H2  | I/O                     | Default mapping: USCI_B0 SPI slave transmit enable; USCI_A0 clock input/output<br>Mapping Options: See <a href="#">表 6-8</a>   |
|                 | P2MAP1      | 19      | J1  | I/O                     | Default mapping: USCI_B0 SPI slave in/master out; USCI_B0 I <sup>2</sup> C data<br>Mapping Options: See <a href="#">表 6-8</a>  |
|                 | P2MAP2      | 20      | H4  | I/O                     | Default mapping: USCI_B0 SPI slave out/master in; USCI_B0 I <sup>2</sup> C clock<br>Mapping Options: See <a href="#">表 6-8</a> |
|                 | P2MAP3      | 21      | J2  | I/O                     | Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable<br>Mapping Options: See <a href="#">表 6-8</a>   |
|                 | P2MAP4      | 22      | K1  | I/O                     | Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in/master out<br>Mapping Options: See <a href="#">表 6-8</a>     |
|                 | P2MAP5      | 23      | K2  | I/O                     | Default mapping: USCI_A0 UART receive data; USCI_A0 slave out/master in<br>Mapping Options: See <a href="#">表 6-8</a>          |
|                 | P2MAP6      | 24      | L2  | I/O                     | Default mapping: no secondary function<br>Mapping Options: See <a href="#">表 6-8</a>                                           |
|                 | P2MAP7      | 25      | L3  | I/O                     | Default mapping: no secondary function<br>Mapping Options: See <a href="#">表 6-8</a>                                           |
| Noise Reduction | NR          | 12      | E1  | I                       | Noise reduction. Connect pin to analog ground.                                                                                 |

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME          | PIN NO.  |                                                           | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                                                                 |
|----------|----------------------|----------|-----------------------------------------------------------|-------------------------|---------------------------------------------------------------------------------------------|
|          |                      | PZ       | ZQW                                                       |                         |                                                                                             |
| Op Amp   | OA1IN0               | 6        | C1                                                        | I                       | OA1 negative input internally connected to ADC negative analog differential input AD2-      |
|          | OA0IN0               | 2        | B2                                                        | I                       | OA0 negative input internally connected to ADC negative analog differential input AD0-      |
|          | OA0IP0               | 99       | A2                                                        | I                       | OA0 positive input internally connected to ADC analog input A2                              |
|          | OA0O                 | 1        | A1                                                        | O                       | OA0 output internally connected to ADC positive analog differential input AD0+              |
|          | OA1IP0               | 100      | D5                                                        | I                       | OA1 positive input internally connected to ADC analog input A3                              |
|          | OA1O                 | 5        | C2                                                        | O                       | OA1 output internally connected to ADC positive analog differential input AD2+              |
| Power    | AVSS1                | 13       | F2                                                        | P                       | Analog ground supply                                                                        |
|          | AVSS2                | 83       | A8                                                        | P                       | Analog ground supply                                                                        |
|          | DVCC                 | 16       | H1, G2                                                    | P                       | Digital power supply                                                                        |
|          | DVCC1                | 26       | L1                                                        | P                       | Digital power supply                                                                        |
|          | DVCC2                | 64       | F12                                                       | P                       | Digital power supply                                                                        |
|          | DVCC3                | 89       | A6                                                        | P                       | Digital power supply                                                                        |
|          | DVSS1                | 27       | M1                                                        | P                       | Digital ground supply                                                                       |
|          | DVSS2                | 63       | G12                                                       | P                       | Digital ground supply                                                                       |
|          | DVSS3                | 90       | A5                                                        | P                       | Digital ground supply                                                                       |
|          | LDO1                 | 80       | A10                                                       | I                       | LDO input (not available on FG662x devices)                                                 |
|          | LDOO                 | 81       | A9                                                        | O                       | LDO output (not available on FG662x devices)                                                |
|          | VCORE <sup>(2)</sup> | 28       | M2                                                        | O                       | Regulated core power supply (internal use only, no external current loading)                |
| REF      | VREFBG               | 9        | D1                                                        | O                       | Output of reference voltage to the ADC and DAC                                              |
| Reserved | NC                   | 78<br>82 | B10<br>B9                                                 | I/O                     | Not connected (not available on FG662x devices)                                             |
|          | Reserved             | –        | E5, E6,<br>E8, F4,<br>F5, F8,<br>G5, G8,<br>H5, H8,<br>H9 | –                       | Reserved. Internally connected to DVSS. TI recommends external connection to ground (DVSS). |
| SPI      | UCA1CLK              | 59       | J12                                                       | I/O                     | USCI_A1 clock input/output                                                                  |
|          | UCA1SIMO             | 60       | H11                                                       | I/O                     | USCI_A1 SPI slave in/master out                                                             |
|          | UCA1SOMI             | 61       | H12                                                       | I/O                     | USCI_A1 SPI slave out/master in                                                             |
|          | UCA1STE              | 62       | G11                                                       | I/O                     | USCI_A1 SPI slave transmit enable                                                           |
|          | UCB1CLK              | 62       | G11                                                       | I/O                     | USCI_B1 clock input/output                                                                  |
|          | UCB1SIMO             | 65       | F11                                                       | I/O                     | USCI_B1 SPI slave in/master out                                                             |
|          | UCB1SOMI             | 66       | G9                                                        | I/O                     | USCI_B1 SPI slave out/master in                                                             |
|          | UCB1STE              | 59       | J12                                                       | I/O                     | USCI_B1 SPI slave transmit enable                                                           |
| System   | NMI                  | 96       | A3                                                        | I                       | Nonmaskable interrupt input                                                                 |
|          | RST                  | 96       | A3                                                        | I/O                     | Reset input (active low) <sup>(3)</sup>                                                     |
|          | SVMOUT               | 57       | K12                                                       | O                       | SVM output                                                                                  |

(2) VCORE is for internal use only. No external current loading is possible. VCORE must be connected to the recommended capacitor value, C<sub>VCORE</sub>.

(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION             | SIGNAL NAME | PIN NO. |            | PIN TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                          |
|----------------------|-------------|---------|------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                      |             | PZ      | ZQW        |                         |                                                                                                                                                                                                                                                      |
| Timer_A              | TA0.0       | 35      | M5         | I/O                     | Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output                                                                                                                                                                                            |
|                      | TA0.1       | 36      | J6         | I/O                     | Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output                                                                                                                                                                                            |
|                      |             | 40      | J7         | I/O                     | Timer TA0 CCR1 capture: CCI1B input, compare: Out1 output                                                                                                                                                                                            |
|                      | TA0.2       | 37      | H6         | I/O                     | Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output                                                                                                                                                                                            |
|                      |             | 41      | M7         | I/O                     | Timer TA0 CCR2 capture: CCI2B input, compare: Out2 output                                                                                                                                                                                            |
|                      | TA0.3       | 38      | M6         | I/O                     | Timer TA0 CCR3 capture: CCI3A input compare: Out3 output                                                                                                                                                                                             |
|                      | TA0.4       | 39      | L6         | I/O                     | Timer TA0 CCR4 capture: CCI4A input, compare: Out4 output                                                                                                                                                                                            |
|                      | TA0CLK      | 34      | L5         | I                       | Timer TA0 clock signal TACLK input                                                                                                                                                                                                                   |
|                      | TA1.0       | 43      | H7         | I/O                     | Timer TA1 capture CCR0: CCI0A input, compare: Out0 output                                                                                                                                                                                            |
|                      | TA1.1       | 44      | M8         | I/O                     | Timer TA1 capture CCR1: CCI1A input, compare: Out1 output                                                                                                                                                                                            |
|                      | TA1.2       | 45      | L8         | I/O                     | Timer TA1 capture CCR2: CCI2A input, compare: Out2 output                                                                                                                                                                                            |
|                      | TA1CLK      | 42      | L7         | I                       | Timer TA1 clock input                                                                                                                                                                                                                                |
|                      | TA2.0       | 47      | M9         | I/O                     | Timer TA2 capture CCR0: CCI0A input, compare: Out0 output                                                                                                                                                                                            |
|                      | TA2.1       | 48      | L9         | I/O                     | Timer TA2 capture CCR1: CCI1A input, compare: Out1 output                                                                                                                                                                                            |
|                      | TA2.2       | 49      | M10        | I/O                     | Timer TA2 capture CCR2: CCI2A input, compare: Out2 output                                                                                                                                                                                            |
|                      | TA2CLK      | 46      | J8         | I                       | Timer TA2 clock input                                                                                                                                                                                                                                |
| Timer_B              | TB0.0       | 50      | J9         | I/O                     | Timer TB0 capture CCR0: CCI0A input, compare: Out0 output                                                                                                                                                                                            |
|                      | TB0.1       | 51      | M11        | I/O                     | Timer TB0 capture CCR1: CCI1A input, compare: Out1 output                                                                                                                                                                                            |
|                      | TB0.2       | 52      | L10        | I/O                     | Timer TB0 capture CCR2: CCI2A input, compare: Out2 output                                                                                                                                                                                            |
|                      | TB0.3       | 53      | M12        | I/O                     | Timer TB0 capture CCR3: CCI3A input, compare: Out3 output                                                                                                                                                                                            |
|                      | TB0.4       | 54      | L12        | I/O                     | Timer TB0 capture CCR4: CCI4A input, compare: Out4 output                                                                                                                                                                                            |
|                      | TB0.5       | 55      | L11        | I/O                     | Timer TB0 capture CCR5: CCI5A input, compare: Out5 output                                                                                                                                                                                            |
|                      | TB0.6       | 56      | K11        | I/O                     | Timer TB0 capture CCR6: CCI6A input, compare: Out6 output                                                                                                                                                                                            |
|                      | TB0CLK      | 58      | J11        | I                       | Timer TB0 clock input                                                                                                                                                                                                                                |
|                      | TB0OUTH     | 57      | K12        | I                       | Timer TB0: Switch all PWM outputs high impedance                                                                                                                                                                                                     |
| UART                 | UCA1CLK     | 59      | J12        | I/O                     | USCI_A1 clock input/output                                                                                                                                                                                                                           |
|                      | UCA1RXD     | 61      | H12        | I                       | USCI_A1 UART receive data                                                                                                                                                                                                                            |
|                      | UCA1TXD     | 60      | H11        | O                       | USCI_A1 UART transmit data                                                                                                                                                                                                                           |
| USB<br>(FG662x only) | DM          | 79      | A11        | I/O                     | USB data terminal DM (not available on FG6426 and FG6425 devices)                                                                                                                                                                                    |
|                      | DP          | 77      | A12        | I/O                     | USB data terminal DP (not available on FG6426 and FG6425 devices)                                                                                                                                                                                    |
|                      | PUR         | 78      | B10        | I/O                     | USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL.<br>Recommended 1-MΩ resistor to ground. See <a href="#">节 6.6</a> for more information.<br>Not available on FG6426 and FG6425 devices. |
|                      | V18         | 82      | B9         | O                       | USB regulated power (internal use only, no external current loading) (not available on FG6426 and FG6425 devices)                                                                                                                                    |
|                      | VBUS        | 80      | A10        | I                       | USB LDO input (connect to USB power source) (not available on FG6426 and FG6425 devices)                                                                                                                                                             |
|                      | VSSU        | 76      | B11<br>B12 | P                       | USB PHY ground supply                                                                                                                                                                                                                                |
|                      | VUSB        | 81      | A9         | O                       | USB LDO output (not available on FG6426 and FG6425 devices)                                                                                                                                                                                          |

## 4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [§ 6.13](#).

## 4.5 Buffer Type

[Table 4-3](#) describes the buffer types that are referenced in [Table 4-1](#).

**Table 4-3. Buffer Type**

| BUFFER TYPE (STANDARD)               | NOMINAL VOLTAGE | HYSTERESIS       | PU OR PD     | NOMINAL PU OR PD STRENGTH ( $\mu$ A)              | OUTPUT DRIVE STRENGTH (mA)                                       | OTHER CHARACTERISTICS                                                       |
|--------------------------------------|-----------------|------------------|--------------|---------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------------|
| Analog <sup>(1)</sup>                | 3.0 V           | N                | N/A          | N/A                                               | N/A                                                              | See analog modules in <a href="#">Section 5, Specifications</a> for details |
| HVCMOS                               | 5.0 V           | Y                | N/A          | N/A                                               | See <a href="#">§ 5.8.5.1, Typical Characteristics – Outputs</a> |                                                                             |
| LVC MOS                              | 3.0 V           | Y <sup>(2)</sup> | Programmable | See <a href="#">§ 5.8.5, General-Purpose I/Os</a> | See <a href="#">§ 5.8.5.1, Typical Characteristics – Outputs</a> |                                                                             |
| Power (DVCC) <sup>(3)</sup>          | 3.0 V           | N                | N/A          | N/A                                               | N/A                                                              | SVS enables hysteresis on DVCC                                              |
| Power (AVCC) <sup>(3)</sup>          | 3.0 V           | N                | N/A          | N/A                                               | N/A                                                              |                                                                             |
| Power (DVSS and AVSS) <sup>(3)</sup> | 0 V             | N                | N/A          | N/A                                               | N/A                                                              |                                                                             |

(1) This is a switch, not a buffer.

(2) Only for input pins

(3) This is supply input, not a buffer.

## 4.6 Connection of Unused Pins

Table 4-4 lists the correct termination of all unused pins.

**Table 4-4. Connection of Unused Pins<sup>(1)</sup>**

| PIN                                          | POTENTIAL                           | COMMENT                                                                                                                                                                                                             |
|----------------------------------------------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AVCC                                         | DV <sub>CC</sub>                    |                                                                                                                                                                                                                     |
| AVSS                                         | DV <sub>SS</sub>                    |                                                                                                                                                                                                                     |
| CPCAP                                        | Open                                | For devices where the charge pump is not used (no rail-to-rail OA and no rail-to-rail CTSD16).                                                                                                                      |
| LCDCAP                                       | DV <sub>SS</sub>                    |                                                                                                                                                                                                                     |
| LDO1                                         | DV <sub>SS</sub>                    | For devices with LDO-PWR module when not being used in the application.                                                                                                                                             |
| LDO0                                         | Open                                | For devices with LDO-PWR module when not being used in the application.                                                                                                                                             |
| NC                                           | Open                                |                                                                                                                                                                                                                     |
| PJ.0/TDO<br>PJ.1/TDI<br>PJ.2/TMS<br>PJ.3/TCK | Open                                | The JTAG pins are shared with general-purpose I/O function (PJ.x). If not being used, these must be switched to port function, output direction (PJDIR.n = 1). When used as JTAG pins, these pins must remain open. |
| PU.0/DP<br>PU.1/DM                           | Open                                | For USB devices only when USB module is not being used in the application                                                                                                                                           |
| PUR <sup>(2)</sup>                           | DV <sub>SS</sub>                    | For USB devices only when USB module is not being used in the application                                                                                                                                           |
| Px.y                                         | Open                                | Switched to port function, output direction (PxDIR.n = 1). Px.y represents port x and bit y of port x (for example, P1.0, P1.1, P2.2, PJ.0, PJ.1)                                                                   |
| RST/NMI                                      | DV <sub>CC</sub> or V <sub>CC</sub> | 47-kΩ pullup or internal pullup selected with 10-nF (2.2 nF) pulldown <sup>(3)</sup>                                                                                                                                |
| Reserved                                     | DV <sub>SS</sub>                    |                                                                                                                                                                                                                     |
| TEST                                         | Open                                | This pin always has an internal pulldown enabled.                                                                                                                                                                   |
| V18                                          | Open                                | For USB devices only when USB module is not being used in the application                                                                                                                                           |
| VBAK                                         | Open                                | For devices where no separate battery backup supply is used in the system. Set bit BAKDIS = 1.                                                                                                                      |
| VBAT                                         | DV <sub>CC</sub>                    | For devices where no separate battery backup supply is used in the system. Set bit BAKDIS = 1.                                                                                                                      |
| VBUS, VSSU                                   | DV <sub>SS</sub>                    | For USB devices only when USB module is not being used in the application                                                                                                                                           |
| VUSB                                         | Open                                | For USB devices only when USB module is not being used in the application                                                                                                                                           |
| XIN                                          | DV <sub>SS</sub>                    | For dedicated XIN pins only. XIN pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.                                                                                        |
| XOUT                                         | Open                                | For dedicated XOUT pins only. XOUT pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.                                                                                      |
| XT2IN                                        | DV <sub>SS</sub>                    | For dedicated XT2IN pins only. XT2IN pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.                                                                                    |
| XT2OUT                                       | Open                                | For dedicated XT2OUT pins only. XT2OUT pins with shared GPIO functions must be programmed to GPIO and follow Px.y recommendations.                                                                                  |

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.y unused pin connection guidelines.
- (2) The default USB BSL evaluates the state of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends a 1-MΩ resistor to ground.
- (3) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools such as FET interfaces or GANG programmers.

## 5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

### 5.1 Absolute Maximum Ratings <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                                                                                     | MIN  | MAX            | UNIT |
|---------------------------------------------------------------------------------------------------------------------|------|----------------|------|
| Voltage applied at $V_{CC}$ to $V_{SS}$                                                                             | −0.3 | 4.1            | V    |
| Voltage applied to any pin (excluding V <sub>CORE</sub> , V <sub>BUS</sub> , V <sub>18</sub> , LDO1) <sup>(2)</sup> | −0.3 | $V_{CC} + 0.3$ | V    |
| Diode current at any device pin                                                                                     |      | ±2             | mA   |
| Storage temperature, $T_{stg}$ <sup>(3)</sup>                                                                       | −55  | 150            | °C   |
| Maximum junction temperature, $T_J$                                                                                 |      | 95             | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ . V<sub>CORE</sub> is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 5.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

### 5.3 Recommended Operating Conditions

Typical values are specified at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

|                             |                                                                                                                                                        | MIN                                             | NOM  | MAX | UNIT |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|------|-----|------|
| $V_{CC}$                    | Supply voltage during program execution and flash programming ( $AV_{CC} = DV_{CC1} = DV_{CC2} = DV_{CC3} = DV_{CC} = V_{CC}$ ) <sup>(1) (2) (3)</sup> | PMMCOREV = 0                                    | 1.8  | 3.6 | V    |
|                             |                                                                                                                                                        | PMMCOREV = 0, 1                                 | 2.0  | 3.6 |      |
|                             |                                                                                                                                                        | PMMCOREV = 0, 1, 2                              | 2.2  | 3.6 |      |
|                             |                                                                                                                                                        | PMMCOREV = 0, 1, 2, 3                           | 2.4  | 3.6 |      |
| $V_{CC,USB}$ <sup>(2)</sup> | Supply voltage during USB operation, USB PLL disabled ( $USB\_EN = 1$ , $UPLLEN = 0$ )                                                                 | PMMCOREV = 0                                    | 1.8  | 3.6 | V    |
|                             |                                                                                                                                                        | PMMCOREV = 0, 1                                 | 2.0  | 3.6 |      |
|                             |                                                                                                                                                        | PMMCOREV = 0, 1, 2                              | 2.2  | 3.6 |      |
|                             |                                                                                                                                                        | PMMCOREV = 0, 1, 2, 3                           | 2.4  | 3.6 |      |
|                             | Supply voltage during USB operation, USB PLL enabled <sup>(4)</sup> ( $USB\_EN = 1$ , $UPLLEN = 1$ )                                                   | PMMCOREV = 2                                    | 2.2  | 3.6 |      |
|                             |                                                                                                                                                        | PMMCOREV = 2, 3                                 | 2.4  | 3.6 |      |
| $V_{SS}$                    | Supply voltage ( $AV_{SS1} = AV_{SS2} = AV_{SS3} = DV_{SS1} = DV_{SS2} = DV_{SS3} = V_{SS}$ )                                                          |                                                 | 0    |     | V    |
| $V_{BAT,RTC}$               | Backup-supply voltage with RTC operational                                                                                                             | $T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$   | 1.55 | 3.6 | V    |
|                             |                                                                                                                                                        | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | 1.70 | 3.6 |      |
| $V_{BAT,MEM}$               | Backup-supply voltage with backup memory retained.                                                                                                     | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ | 1.20 | 3.6 | V    |
| $T_A$                       | Operating free-air temperature                                                                                                                         | I version                                       | −40  | 85  | °C   |
| $T_J$                       | Operating junction temperature                                                                                                                         | I version                                       | −40  | 85  | °C   |

- (1) TI recommends powering  $AV_{CC}$  and  $DV_{CC}$  from the same source. A maximum difference of 0.3 V between  $AV_{CC}$  and  $DV_{CC}$  can be tolerated during power up and operation.
- (2) Some modules may have reduced recommended ranges of operation.
- (3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the threshold parameters in [Table 5-16](#) for the exact values and further details.
- (4) USB operation with USB PLL enabled requires  $PMMCOREV \geq 2$  for proper operation.

## Recommended Operating Conditions (continued)

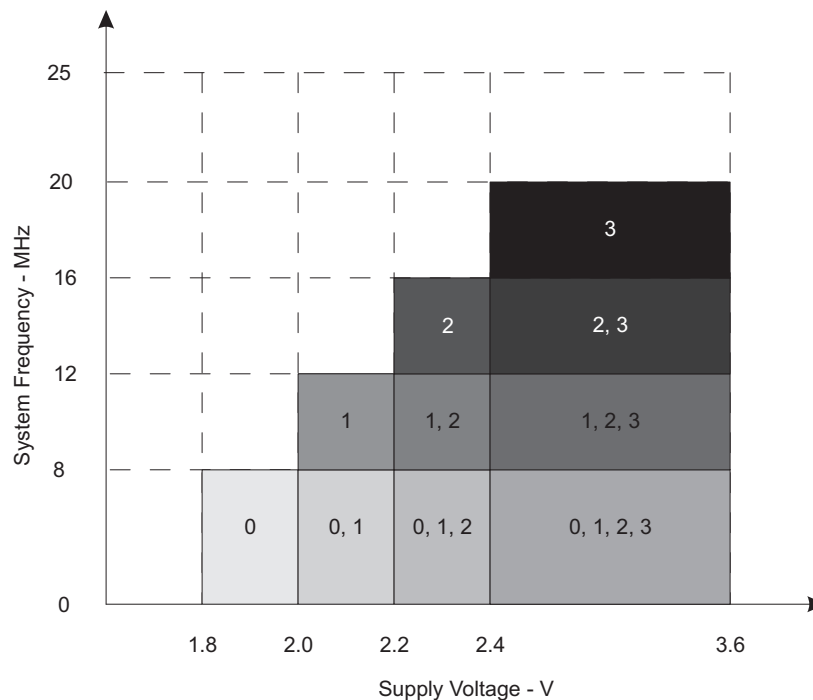
Typical values are specified at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

|                                           |                                                                                                                 | MIN                                                                     | NOM | MAX | UNIT |        |
|-------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-----|-----|------|--------|
| C <sub>BAK</sub>                          | Capacitance at pin VBAK                                                                                         | 1                                                                       | 4.7 | 10  | nF   |        |
| C <sub>VCORE</sub>                        | Capacitor at VCORE <sup>(5)</sup>                                                                               | 470                                                                     |     |     | nF   |        |
| C <sub>DVCC</sub> /<br>C <sub>VCORE</sub> | Capacitor ratio of DVCC to VCORE                                                                                | 10                                                                      |     |     |      |        |
| f <sub>SYSTEM</sub>                       | Processor frequency (maximum MCLK frequency) <sup>(6)</sup> <sup>(7)</sup><br>(see <a href="#">Figure 5-1</a> ) | PMMCOREV = 0,<br>1.8 V ≤ V <sub>CC</sub> ≤ 3.6 V<br>(default condition) |     | 0   | 8.0  | MHz    |
|                                           |                                                                                                                 | PMMCOREV = 1,<br>2 V ≤ V <sub>CC</sub> ≤ 3.6 V                          |     | 0   | 12.0 |        |
|                                           |                                                                                                                 | PMMCOREV = 2,<br>2.2 V ≤ V <sub>CC</sub> ≤ 3.6 V                        |     | 0   | 16.0 |        |
|                                           |                                                                                                                 | PMMCOREV = 3,<br>2.4 V ≤ V <sub>CC</sub> ≤ 3.6 V                        |     | 0   | 20.0 |        |
| f <sub>SYSTEM_USB</sub>                   | Minimum processor frequency for USB operation                                                                   | 1.5                                                                     |     |     |      | MHz    |
| USB_wait                                  | Wait state cycles during USB operation                                                                          | 16                                                                      |     |     |      | cycles |

(5) A capacitor tolerance of  $\pm 20\%$  is required.

(6) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.

(7) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

**Figure 5-1. Frequency vs Supply Voltage**

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

| PARAMETER              | EXECUTION MEMORY | V <sub>CC</sub> | PMMCOREV | FREQUENCY (f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> ) |      |       |     |        |     |        |     | UNIT |
|------------------------|------------------|-----------------|----------|------------------------------------------------------------------------|------|-------|-----|--------|-----|--------|-----|------|
|                        |                  |                 |          | 1 MHz                                                                  |      | 8 MHz |     | 12 MHz |     | 20 MHz |     |      |
|                        |                  |                 |          | TYP                                                                    | MAX  | TYP   | MAX | TYP    | MAX | TYP    | MAX |      |
| I <sub>AM, Flash</sub> | Flash            | 3 V             | 0        | 0.31                                                                   | 0.36 | 2.0   | 2.4 |        |     |        |     | mA   |
|                        |                  |                 | 1        | 0.35                                                                   |      | 2.3   |     | 3.4    | 4.0 |        |     |      |
|                        |                  |                 | 2        | 0.37                                                                   |      | 2.5   |     | 3.8    |     |        |     |      |
|                        |                  |                 | 3        | 0.4                                                                    |      | 2.7   |     | 4.0    |     | 6.6    |     |      |
| I <sub>AM, RAM</sub>   | RAM              | 3 V             | 0        | 0.2                                                                    | 0.23 | 1.1   | 1.2 |        |     |        |     | mA   |
|                        |                  |                 | 1        | 0.22                                                                   |      | 1.3   |     | 1.9    | 2.1 |        |     |      |
|                        |                  |                 | 2        | 0.24                                                                   |      | 1.5   |     | 2.2    |     |        |     |      |
|                        |                  |                 | 3        | 0.26                                                                   |      | 1.6   |     | 2.4    |     | 3.9    |     |      |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Characterized with program executing typical data processing. FG6626 and FG6625 USB disabled ( $V_{USBEN} = 0$ ,  $SLDOEN = 0$ ). FG6426 and FG6425 LDO disabled ( $LDOEN = 0$ ).

$f_{ACLK} = 32786 \text{ Hz}$ ,  $f_{DCO} = f_{MCLK} = f_{SMCLK}$  at specified frequency.

$XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$ .

## 5.5 Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                                                                                                                 | V <sub>CC</sub> | PMMCOREV | TEMPERATURE (T <sub>A</sub> ) |     |      |     |      |     |      |      | UNIT |
|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------|-------------------------------|-----|------|-----|------|-----|------|------|------|
|                                                                                                                                           |                 |          | −40°C                         |     | 25°C |     | 60°C |     | 85°C |      |      |
|                                                                                                                                           |                 |          | TYP                           | MAX | TYP  | MAX | TYP  | MAX | TYP  | MAX  |      |
| I <sub>LPM0,1MHz</sub> Low-power mode 0 <sup>(3) (4)</sup>                                                                                | 2.2 V           | 0        | 72                            |     | 77   | 87  | 81   |     | 87   | 98   | μA   |
|                                                                                                                                           | 3 V             | 3        | 86                            |     | 92   | 105 | 97   |     | 104  | 117  |      |
| I <sub>LPM2</sub> Low-power mode 2 <sup>(5) (4)</sup>                                                                                     | 2.2 V           | 0        | 6.9                           |     | 7.5  | 9.9 | 8.5  |     | 12   | 17   | μA   |
|                                                                                                                                           | 3 V             | 3        | 7.9                           |     | 8.5  | 11  | 9.7  |     | 14   | 20   |      |
| I <sub>LPM3,XT1LF</sub> Low-power mode 3, crystal mode <sup>(6) (4)</sup>                                                                 | 2.2 V           | 0        | 2.8                           |     | 3.2  | 3.7 | 4.2  |     | 7.6  | 13.5 | μA   |
|                                                                                                                                           |                 | 1        | 3.1                           |     | 3.6  |     | 4.6  |     | 8.2  |      |      |
|                                                                                                                                           |                 | 2        | 3.5                           |     | 4.0  |     | 5.1  |     | 8.8  |      |      |
|                                                                                                                                           | 3 V             | 0        | 3.0                           |     | 3.4  | 4.0 | 4.4  |     | 7.9  | 14   |      |
|                                                                                                                                           |                 | 1        | 3.3                           |     | 3.8  |     | 4.9  |     | 8.5  |      |      |
|                                                                                                                                           |                 | 2        | 3.7                           |     | 4.2  |     | 5.3  |     | 9.0  |      |      |
|                                                                                                                                           |                 | 3        | 3.7                           |     | 4.2  | 4.8 | 5.3  |     | 9.1  | 16   |      |
| I <sub>LPM3, VLO, WDT</sub> Low-power mode 3, VLO mode, Watchdog enabled <sup>(7) (4)</sup>                                               | 3 V             | 0        | 1.2                           |     | 1.5  | 2.1 | 2.4  |     | 5.8  | 12.5 | μA   |
|                                                                                                                                           |                 | 1        | 1.4                           |     | 1.6  |     | 2.6  |     | 6.1  |      |      |
|                                                                                                                                           |                 | 2        | 1.6                           |     | 1.8  |     | 2.8  |     | 6.5  |      |      |
|                                                                                                                                           |                 | 3        | 1.6                           |     | 1.8  | 2.6 | 2.9  |     | 6.5  | 14   |      |
| I <sub>LPM4</sub> Low-power mode 4 <sup>(8) (4)</sup>                                                                                     | 3 V             | 0        | 0.6                           |     | 0.9  | 1.8 | 1.9  |     | 5.4  | 11.5 | μA   |
|                                                                                                                                           |                 | 1        | 0.7                           |     | 1.0  |     | 2.0  |     | 5.6  |      |      |
|                                                                                                                                           |                 | 2        | 0.8                           |     | 1.1  |     | 2.2  |     | 5.9  |      |      |
|                                                                                                                                           |                 | 3        | 0.8                           |     | 1.1  | 2.1 | 2.2  |     | 6.0  | 13   |      |
| I <sub>LPM3.5, RTC, VCC</sub> Low-power mode 3.5 (LPM3.5) current with active RTC into primary supply pin DV <sub>CC</sub> <sup>(9)</sup> | 3 V             |          |                               |     | 0.2  |     |      |     | 0.7  | 1.7  | μA   |
| I <sub>LPM3.5, RTC, VBAT</sub> Low-power mode 3.5 (LPM3.5) current with active RTC into backup supply pin VBAT <sup>(10)</sup>            | 3 V             |          |                               |     | 0.7  |     |      |     | 0.9  | 1.2  | μA   |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE<sub>ex</sub> = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0),  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  = 0 MHz,  $f_{SMCLK}$  =  $f_{DCO}$  = 1 MHz FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(4) Current for brownout included. Low-side supervisor and monitors disabled (SVS<sub>L</sub>, SVM<sub>L</sub>). High-side supervisor and monitor disabled (SVS<sub>H</sub>, SVM<sub>H</sub>). RAM retention enabled.

(5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE<sub>ex</sub> = 0).

CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2),  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  = 0 MHz,  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.

FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(6) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE<sub>ex</sub> = 0).

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3),  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz

FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(7) Current for watchdog timer clocked by VLO included.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3),  $f_{ACLK}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz

FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4),  $f_{DCO}$  =  $f_{ACLK}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz FG6626 and FG6625 USB disabled (VUSBEN = 0, SLDOEN = 0). FG6426 and FG6425 LDO disabled (LDOEN = 0).

(9)  $V_{VBAT}$  =  $V_{CC}$  – 0.2 V,  $f_{DCO}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz,  $f_{ACLK}$  = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active

(10)  $V_{VBAT}$  =  $V_{CC}$  – 0.2 V,  $f_{DCO}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz,  $f_{ACLK}$  = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

## Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                    |                                                                           | V <sub>CC</sub> | PMMCOREV | TEMPERATURE (T <sub>A</sub> ) |     |      |     |      |     |      |     | UNIT |
|------------------------------|---------------------------------------------------------------------------|-----------------|----------|-------------------------------|-----|------|-----|------|-----|------|-----|------|
|                              |                                                                           |                 |          | −40°C                         |     | 25°C |     | 60°C |     | 85°C |     |      |
|                              |                                                                           |                 |          | TYP                           | MAX | TYP  | MAX | TYP  | MAX | TYP  | MAX |      |
| I <sub>LPM3.5, RTC,TOT</sub> | Total low-power mode 3.5 (LPM3.5) current with active RTC <sup>(11)</sup> | 3 V             |          | 0.8                           |     | 0.9  |     | 1.0  |     | 1.6  | 2.9 | μA   |
| I <sub>LPM4.5</sub>          | Low-power mode 4.5 (LPM4.5) <sup>(12)</sup>                               | 3 V             |          | 0.12                          |     | 0.2  | 0.6 | 0.32 |     | 0.8  | 1.9 | μA   |

(11)  $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$  MHz,  $f_{ACLK} = 32768$  Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

(12) Internal regulator disabled. No data retention.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5),  $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$  MHz

## 5.6 Low-Power Mode With LCD Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                |                                                                                                            | V <sub>CC</sub> | PMMCOREV | TEMPERATURE (T <sub>A</sub> ) |      |      |     |      |     |      |      | UNIT |
|------------------------------------------|------------------------------------------------------------------------------------------------------------|-----------------|----------|-------------------------------|------|------|-----|------|-----|------|------|------|
|                                          |                                                                                                            |                 |          | −40°C                         |      | 25°C |     | 60°C |     | 85°C |      |      |
|                                          |                                                                                                            |                 |          | TYP                           | MAX  | TYP  | MAX | TYP  | MAX | TYP  | MAX  |      |
| I <sub>LPM3</sub> ,<br>LCD,<br>ext. bias | Low-power mode 3 (LPM3) current, LCD 4-mux mode, external biasing <sup>(3) (4)</sup>                       | 3 V             | 0        | 3.7                           |      | 4.3  | 4.9 | 5.5  |     | 9.0  | 15.0 | μA   |
|                                          |                                                                                                            |                 | 1        | 4.1                           |      | 4.7  |     | 5.9  |     | 9.6  |      |      |
|                                          |                                                                                                            |                 | 2        | 4.5                           |      | 5.1  |     | 6.3  |     | 10.2 |      |      |
|                                          |                                                                                                            |                 | 3        | 4.5                           |      | 5.2  | 5.8 | 6.5  |     | 10.4 | 18.0 |      |
| I <sub>LPM3</sub> ,<br>LCD,<br>int. bias | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled <sup>(3) (5)</sup> | 3 V             | 0        | 4.2                           |      | 4.8  | 5.4 | 6.0  |     | 9.6  | 17.0 | μA   |
|                                          |                                                                                                            |                 | 1        | 4.7                           |      | 5.4  |     | 6.6  |     | 10.4 |      |      |
|                                          |                                                                                                            |                 | 2        | 5.1                           |      | 5.8  |     | 7.1  |     | 11.0 |      |      |
|                                          |                                                                                                            |                 | 3        | 5.0                           |      | 5.7  | 6.4 | 7.0  |     | 11.0 | 19.0 |      |
| I <sub>LPM3</sub><br>LCD,CP              | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled <sup>(3) (6)</sup>  | 2.2 V           | 0        |                               |      | 6.4  |     |      |     |      |      | μA   |
|                                          |                                                                                                            |                 | 1        |                               |      | 6.77 |     |      |     |      |      |      |
|                                          |                                                                                                            |                 | 2        |                               |      | 7.13 |     |      |     |      |      |      |
|                                          | 3 V                                                                                                        | 0               |          |                               | 6.53 |      |     |      |     |      |      | μA   |
|                                          |                                                                                                            | 1               |          |                               | 7.0  |      |     |      |     |      |      |      |
|                                          |                                                                                                            | 2               |          |                               | 7.43 |      |     |      |     |      |      |      |
|                                          |                                                                                                            | 3               |          |                               | 7.6  |      |     |      |     |      |      |      |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

(3) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEX = 0).

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3),  $f_{ACLK} = 32768$  Hz,  $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$  MHz  
Current for brownout included. Low-side supervisor (SVSL) and low-side monitor (SVM<sub>L</sub>) disabled. High-side supervisor (SVSH) and high-side monitor (SVM<sub>H</sub>) disabled. RAM retention enabled.

(4) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ( $f_{LCD} = 32768$  Hz / 32 / 4 = 256 Hz)  
Current through external resistors not included (voltage levels are supplied by test equipment).

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ( $f_{LCD} = 32768$  Hz / 32 / 4 = 256 Hz)

Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

(6) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ( $V_{LCD} = 3$  V, typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ( $f_{LCD} = 32768$  Hz / 32 / 4 = 256 Hz)  
Even segments S0, S2,... = 0, odd segments S1, S3,... = 1. No LCD panel load.

## 5.7 Thermal Resistance Characteristics

| PARAMETER                                                                      |           | VALUE | UNIT |
|--------------------------------------------------------------------------------|-----------|-------|------|
| $\theta_{JA}$ Junction-to-ambient thermal resistance, still air <sup>(1)</sup> | QFP (PZ)  | 122   | °C/W |
|                                                                                | BGA (ZQW) | 108   |      |
| $\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance <sup>(2)</sup>    | QFP (PZ)  | 83    | °C/W |
|                                                                                | BGA (ZQW) | 72    |      |
| $\theta_{JB}$ Junction-to-board thermal resistance <sup>(3)</sup>              | QFP (PZ)  | 98    | °C/W |
|                                                                                | BGA (ZQW) | 76    |      |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

## 5.8 Timing and Switching Characteristics

### 5.8.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

[表 5-1](#) lists the device reset requirements.

**表 5-1. Brownout and Device Reset Power Ramp Requirements**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                          | TEST CONDITIONS                 | MIN  | TYP  | MAX  | UNIT |
|------------------------------------------------------------------------------------|---------------------------------|------|------|------|------|
| $V_{(DVCC\_BOR\_IT-)}$ BOR <sub>H</sub> on voltage, DV <sub>CC</sub> falling level | $ dDV_{CC}/dt  < 3 \text{ V/s}$ |      |      | 1.47 | V    |
| $V_{(DVCC\_BOR\_IT+)}$ BOR <sub>H</sub> off voltage, DV <sub>CC</sub> rising level | $ dDV_{CC}/dt  < 3 \text{ V/s}$ | 0.80 | 1.30 | 1.55 | V    |
| $V_{(DVCC\_BOR\_hys)}$ BOR <sub>H</sub> hysteresis                                 |                                 | 60   |      | 250  | mV   |

### 5.8.2 Reset Timing

[表 5-2](#) lists the reset input timing.

**表 5-2. Reset Input**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                         | TYP | UNIT |
|-----------------------------------------------------------------------------------|-----|------|
| $t_{RESET}$ Pulse duration required at $\overline{RST}/NMI$ pin to accept a reset | 2   | μs   |

### 5.8.3 Clock Specifications

表 5-3 lists the characteristics of XT1 in low-frequency mode.

**表 5-3. Crystal Oscillator, XT1, Low-Frequency Mode<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                                                            | TEST CONDITIONS                                                                                 | V <sub>CC</sub> | MIN   | TYP    | MAX   | UNIT       |
|----------------------|--------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-----------------|-------|--------|-------|------------|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 1                         | 3 V             | 0.075 |        |       | $\mu$ A    |
|                      |                                                                                            | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 2                         |                 | 0.170 |        |       |            |
|                      |                                                                                            | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 3                         |                 | 0.290 |        |       |            |
| $f_{XT1,LF0}$        | XT1 oscillator crystal frequency, LF mode                                                  | XTS = 0, XT1BYPASS = 0                                                                          |                 | 32768 |        |       | Hz         |
| $f_{XT1,LF,SW}$      | XT1 oscillator logic-level square-wave input frequency, LF mode                            | XTS = 0, XT1BYPASS = 1 <sup>(2)</sup> <sup>(3)</sup>                                            |                 | 10    | 32.768 | 50    | kHz        |
| $OA_{LF}$            | Oscillation allowance for LF crystals <sup>(4)</sup>                                       | XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF  |                 | 210   |        |       | k $\Omega$ |
|                      |                                                                                            | XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF |                 | 300   |        |       |            |
| $C_{L,eff}$          | Integrated effective load capacitance, LF mode <sup>(5)</sup>                              | XTS = 0, XCAP <sub>x</sub> = 0 <sup>(6)</sup>                                                   |                 | 1     |        |       | pF         |
|                      |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 1                                                                  |                 | 5.5   |        |       |            |
|                      |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 2                                                                  |                 | 8.5   |        |       |            |
|                      |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 3                                                                  |                 | 12.0  |        |       |            |
|                      | Duty cycle, LF mode                                                                        | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz                                              |                 | 30%   |        | 70%   |            |
| $f_{Fault,LF}$       | Oscillator fault frequency, LF mode <sup>(7)</sup>                                         | XTS = 0 <sup>(8)</sup>                                                                          |                 | 10    |        | 10000 | Hz         |
| $t_{START,LF}$       | Start-up time, LF mode                                                                     | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 0, $C_{L,eff}$ = 6 pF     | 3 V             | 1000  |        |       | ms         |
|                      |                                                                                            | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 3, $C_{L,eff}$ = 12 pF    |                 | 500   |        |       |            |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE<sub>x</sub> settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  - For XT1DRIVE<sub>x</sub> = 0,  $C_{L,eff} \leq 6$  pF.
  - For XT1DRIVE<sub>x</sub> = 1,  $6 \text{ pF} \leq C_{L,eff} \leq 9$  pF.
  - For XT1DRIVE<sub>x</sub> = 2,  $6 \text{ pF} \leq C_{L,eff} \leq 10$  pF.
  - For XT1DRIVE<sub>x</sub> = 3,  $C_{L,eff} \geq 6$  pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

表 5-4 lists the characteristics of XT2.

**表 5-4. Crystal Oscillator, XT2**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                                                            | TEST CONDITIONS                                                                                                          | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| I <sub>DVCC,XT2</sub> XT2 oscillator crystal current consumption                     | f <sub>OSC</sub> = 4 MHz, XT2OFF = 0, T <sub>A</sub> = 25°C, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 0                    | 3 V             |     | 200 |     | μA   |
|                                                                                      | f <sub>OSC</sub> = 12 MHz, XT2OFF = 0, T <sub>A</sub> = 25°C, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 1                   |                 |     | 260 |     |      |
|                                                                                      | f <sub>OSC</sub> = 20 MHz, XT2OFF = 0, T <sub>A</sub> = 25°C, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 2                   |                 |     | 325 |     |      |
|                                                                                      | f <sub>OSC</sub> = 32 MHz, XT2OFF = 0, T <sub>A</sub> = 25°C, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 3                   |                 |     | 450 |     |      |
| f <sub>XT2,HF0</sub> XT2 oscillator crystal frequency, mode 0                        | XT2DRIVE <sub>x</sub> = 0, XT2BYPASS = 0 <sup>(3)</sup>                                                                  |                 | 4   |     | 8   | MHz  |
| f <sub>XT2,HF1</sub> XT2 oscillator crystal frequency, mode 1                        | XT2DRIVE <sub>x</sub> = 1, XT2BYPASS = 0 <sup>(3)</sup>                                                                  |                 | 8   |     | 16  | MHz  |
| f <sub>XT2,HF2</sub> XT2 oscillator crystal frequency, mode 2                        | XT2DRIVE <sub>x</sub> = 2, XT2BYPASS = 0 <sup>(3)</sup>                                                                  |                 | 16  |     | 24  | MHz  |
| f <sub>XT2,HF3</sub> XT2 oscillator crystal frequency, mode 3                        | XT2DRIVE <sub>x</sub> = 3, XT2BYPASS = 0 <sup>(3)</sup>                                                                  |                 | 24  |     | 32  | MHz  |
| f <sub>XT2,HF,SW</sub> XT2 oscillator logic-level square-wave input frequency        | XT2BYPASS = 1 <sup>(4) (3)</sup>                                                                                         |                 | 0.7 |     | 32  | MHz  |
| O <sub>AHF</sub> Oscillation allowance for HF crystals <sup>(5)</sup>                | XT2DRIVE <sub>x</sub> = 0, XT2BYPASS = 0, f <sub>XT2,HF0</sub> = 6 MHz, C <sub>L,eff</sub> = 15 pF                       |                 |     | 450 |     | Ω    |
|                                                                                      | XT2DRIVE <sub>x</sub> = 1, XT2BYPASS = 0, f <sub>XT2,HF1</sub> = 12 MHz, C <sub>L,eff</sub> = 15 pF                      |                 |     | 320 |     |      |
|                                                                                      | XT2DRIVE <sub>x</sub> = 2, XT2BYPASS = 0, f <sub>XT2,HF2</sub> = 20 MHz, C <sub>L,eff</sub> = 15 pF                      |                 |     | 200 |     |      |
|                                                                                      | XT2DRIVE <sub>x</sub> = 3, XT2BYPASS = 0, f <sub>XT2,HF3</sub> = 32 MHz, C <sub>L,eff</sub> = 15 pF                      |                 |     | 200 |     |      |
| t <sub>START,HF</sub> Start-up time                                                  | f <sub>OSC</sub> = 6 MHz<br>XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 0, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 15 pF  | 3 V             |     | 0.5 |     | ms   |
|                                                                                      | f <sub>OSC</sub> = 20 MHz<br>XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 3, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 15 pF |                 |     | 0.3 |     |      |
| C <sub>L,eff</sub> Integrated effective load capacitance, HF mode <sup>(6) (1)</sup> |                                                                                                                          |                 |     | 1   |     | pF   |
| Duty cycle                                                                           | Measured at ACLK, f <sub>XT2,HF2</sub> = 20 MHz                                                                          |                 | 40% | 50% | 60% |      |
| f <sub>Fault,HF</sub> Oscillator fault frequency <sup>(7)</sup>                      | XT2BYPASS = 1 <sup>(8)</sup>                                                                                             |                 | 30  |     | 300 | kHz  |

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

表 5-5 lists the characteristics of the VLO.

**表 5-5. Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub>                    | VLO frequency                      | Measured at ACLK                | 1.8 V to 3.6 V  | 6   | 9.4 | 14  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | Measured at ACLK <sup>(1)</sup> | 1.8 V to 3.6 V  |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 4   |     | %/V  |
| Duty cycle                          |                                    | Measured at ACLK                | 1.8 V to 3.6 V  | 40% | 50% | 60% |      |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

表 5-6 lists the characteristics of the REFO.

**表 5-6. Internal Reference, Low-Frequency Oscillator (REFO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                            |                                     | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP   | MAX   | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|-------|------|
| I <sub>REFO</sub>                    | REFO oscillator current consumption | T <sub>A</sub> = 25°C           | 1.8 V to 3.6 V  |     | 3     |       | μA   |
| f <sub>REFO</sub>                    | REFO frequency calibrated           | Measured at ACLK                | 1.8 V to 3.6 V  |     | 32768 |       | Hz   |
|                                      | REFO absolute tolerance calibrated  | Full temperature range          | 1.8 V to 3.6 V  |     |       | ±3.5% |      |
|                                      |                                     | T <sub>A</sub> = 25°C           | 3 V             |     |       | ±1.5% |      |
| df <sub>REFO</sub> /dT               | REFO frequency temperature drift    | Measured at ACLK <sup>(1)</sup> | 1.8 V to 3.6 V  |     | 0.01  |       | %/°C |
| df <sub>REFO</sub> /dV <sub>CC</sub> | REFO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 1.0   |       | %/V  |
| Duty cycle                           |                                     | Measured at ACLK                | 1.8 V to 3.6 V  | 40% | 50%   | 60%   |      |
| t <sub>START</sub>                   | REFO start-up time                  | 40%/60% duty cycle              | 1.8 V to 3.6 V  |     | 25    |       | μs   |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

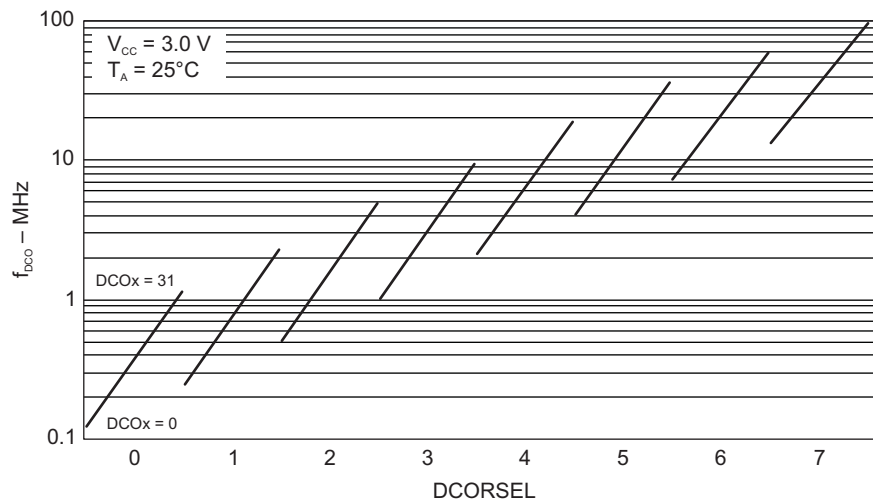
表 5-7 lists the characteristics of the DCO frequency.

**表 5-7. DCO Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                        | TEST CONDITIONS                                      | MIN                                                                                                           | TYP  | MAX  | UNIT  |
|----------------------------------|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|------|------|-------|
| $f_{\text{DCO}(0,0)}$            | DCO frequency (0, 0) <sup>(1)</sup>                  | DCORSELx = 0, DCOx = 0, MODx = 0                                                                              | 0.07 | 0.20 | MHz   |
| $f_{\text{DCO}(0,31)}$           | DCO frequency (0, 31) <sup>(1)</sup>                 | DCORSELx = 0, DCOx = 31, MODx = 0                                                                             | 0.70 | 1.70 | MHz   |
| $f_{\text{DCO}(1,0)}$            | DCO frequency (1, 0) <sup>(1)</sup>                  | DCORSELx = 1, DCOx = 0, MODx = 0                                                                              | 0.15 | 0.36 | MHz   |
| $f_{\text{DCO}(1,31)}$           | DCO frequency (1, 31) <sup>(1)</sup>                 | DCORSELx = 1, DCOx = 31, MODx = 0                                                                             | 1.47 | 3.45 | MHz   |
| $f_{\text{DCO}(2,0)}$            | DCO frequency (2, 0) <sup>(1)</sup>                  | DCORSELx = 2, DCOx = 0, MODx = 0                                                                              | 0.32 | 0.75 | MHz   |
| $f_{\text{DCO}(2,31)}$           | DCO frequency (2, 31) <sup>(1)</sup>                 | DCORSELx = 2, DCOx = 31, MODx = 0                                                                             | 3.17 | 7.38 | MHz   |
| $f_{\text{DCO}(3,0)}$            | DCO frequency (3, 0) <sup>(1)</sup>                  | DCORSELx = 3, DCOx = 0, MODx = 0                                                                              | 0.64 | 1.51 | MHz   |
| $f_{\text{DCO}(3,31)}$           | DCO frequency (3, 31) <sup>(1)</sup>                 | DCORSELx = 3, DCOx = 31, MODx = 0                                                                             | 6.07 | 14.0 | MHz   |
| $f_{\text{DCO}(4,0)}$            | DCO frequency (4, 0) <sup>(1)</sup>                  | DCORSELx = 4, DCOx = 0, MODx = 0                                                                              | 1.3  | 3.2  | MHz   |
| $f_{\text{DCO}(4,31)}$           | DCO frequency (4, 31) <sup>(1)</sup>                 | DCORSELx = 4, DCOx = 31, MODx = 0                                                                             | 12.3 | 28.2 | MHz   |
| $f_{\text{DCO}(5,0)}$            | DCO frequency (5, 0) <sup>(1)</sup>                  | DCORSELx = 5, DCOx = 0, MODx = 0                                                                              | 2.5  | 6.0  | MHz   |
| $f_{\text{DCO}(5,31)}$           | DCO frequency (5, 31) <sup>(1)</sup>                 | DCORSELx = 5, DCOx = 31, MODx = 0                                                                             | 23.7 | 54.1 | MHz   |
| $f_{\text{DCO}(6,0)}$            | DCO frequency (6, 0) <sup>(1)</sup>                  | DCORSELx = 6, DCOx = 0, MODx = 0                                                                              | 4.6  | 10.7 | MHz   |
| $f_{\text{DCO}(6,31)}$           | DCO frequency (6, 31) <sup>(1)</sup>                 | DCORSELx = 6, DCOx = 31, MODx = 0                                                                             | 39.0 | 88.0 | MHz   |
| $f_{\text{DCO}(7,0)}$            | DCO frequency (7, 0) <sup>(1)</sup>                  | DCORSELx = 7, DCOx = 0, MODx = 0                                                                              | 8.5  | 19.6 | MHz   |
| $f_{\text{DCO}(7,31)}$           | DCO frequency (7, 31) <sup>(1)</sup>                 | DCORSELx = 7, DCOx = 31, MODx = 0                                                                             | 60   | 135  | MHz   |
| $S_{\text{DCORSEL}}$             | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{\text{RSEL}} = f_{\text{DCO}(\text{DCORSEL}+1, \text{DCO})} / f_{\text{DCO}(\text{DCORSEL}, \text{DCO})}$ | 1.2  | 2.3  | ratio |
| $S_{\text{DCO}}$                 | Frequency step between tap DCO and DCO + 1           | $S_{\text{DCO}} = f_{\text{DCO}(\text{DCORSEL}, \text{DCO}+1)} / f_{\text{DCO}(\text{DCORSEL}, \text{DCO})}$  | 1.02 | 1.12 | ratio |
|                                  | Duty cycle                                           | Measured at SMCLK                                                                                             | 40%  | 50%  | 60%   |
| $df_{\text{DCO}}/dT$             | DCO frequency temperature drift                      | $f_{\text{DCO}} = 1 \text{ MHz}$                                                                              | 0.1  |      | %/°C  |
| $df_{\text{DCO}}/dV_{\text{CC}}$ | DCO frequency voltage drift                          | $f_{\text{DCO}} = 1 \text{ MHz}$                                                                              | 1.9  |      | %/V   |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency,  $f_{\text{DCO}}$ , should be set to reside within the range of  $f_{\text{DCO}(n, 0), \text{MAX}} \leq f_{\text{DCO}} \leq f_{\text{DCO}(n, 31), \text{MIN}}$ , where  $f_{\text{DCO}(n, 0), \text{MAX}}$  represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and  $f_{\text{DCO}(n, 31), \text{MIN}}$  represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual  $f_{\text{DCO}}$  frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.



**图 5-2. Typical DCO Frequency**

## 5.8.4 Wake-up Characteristics

表 5-8 lists the characteristics of the wake-up times.

**表 5-8. Wake-up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                  |                                                                                      | TEST CONDITIONS                                                     | MIN                                               | TYP | MAX | UNIT          |
|----------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------------------------------|-----|-----|---------------|
| $t_{\text{WAKE-UP-FAST}}$  | Wake-up time from LPM2, LPM3, or LPM4 to active mode <sup>(1)</sup>                  | PMMCOREV = SVSMLRRL = n<br>(where n = 0, 1, 2, or 3),<br>SVSLFP = 1 | $f_{\text{MCLK}} \geq 4 \text{ MHz}$              | 3   | 6.5 | $\mu\text{s}$ |
|                            |                                                                                      |                                                                     | $1 \text{ MHz} < f_{\text{MCLK}} < 4 \text{ MHz}$ | 4   | 8.0 |               |
| $t_{\text{WAKE-UP-SLOW}}$  | Wake-up time from LPM2, LPM3, or LPM4 to active mode <sup>(2)(3)</sup>               | PMMCOREV = SVSMLRRL = n<br>(where n = 0, 1, 2, or 3),<br>SVSLFP = 0 |                                                   | 150 | 165 | $\mu\text{s}$ |
| $t_{\text{WAKE-UP-LPM5}}$  | Wake-up time from LPM3.5 or LPM4.5 to active mode <sup>(4)</sup>                     |                                                                     |                                                   | 2   | 3   | ms            |
| $t_{\text{WAKE-UP-RESET}}$ | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode <sup>(4)</sup> |                                                                     |                                                   | 2   | 3   | ms            |

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS<sub>L</sub>) and low-side monitor (SVM<sub>L</sub>).  $t_{\text{WAKE-UP-FAST}}$  is possible with SVS<sub>L</sub> and SVM<sub>L</sub> in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS<sub>L</sub>) and low-side monitor (SVM<sub>L</sub>).  $t_{\text{WAKE-UP-SLOW}}$  is set with SVS<sub>L</sub> and SVM<sub>L</sub> in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

## 5.8.5 General-Purpose I/Os

Table 5-9 lists the characteristics of the Schmitt-trigger inputs.

**Table 5-9. Schmitt-Trigger Inputs – General-Purpose I/O<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                                                                                  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          |                                                                                                  | 1.8 V           | 0.80 |     | 1.40 | V    |
|                                                                                  |                                                                                                  | 3 V             | 1.50 |     | 2.10 |      |
| V <sub>IT–</sub> Negative-going input threshold voltage                          |                                                                                                  | 1.8 V           | 0.45 |     | 1.00 | V    |
|                                                                                  |                                                                                                  | 3 V             | 0.75 |     | 1.65 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                                                                                  | 1.8 V           | 0.3  |     | 0.8  | V    |
|                                                                                  |                                                                                                  | 3 V             | 0.4  |     | 1.0  |      |
| R <sub>Pull</sub> Pullup or pulldown resistor                                    | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I</sub> Input capacitance                                                 | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                             |                 |      | 5   |      | pF   |

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

Table 5-10 lists the characteristics of P1, P2, P3, and P4 .

**Table 5-10. Inputs – Ports P1, P2, P3, and P4<sup>(1)</sup>**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                   | TEST CONDITIONS                                                                             | V <sub>CC</sub> | MIN | MAX | UNIT |
|-------------------------------------------------------------|---------------------------------------------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>(int)</sub> External interrupt timing <sup>(2)</sup> | Port P1, P2, P3, P4: P1.x to P4.x,<br>External trigger pulse duration to set interrupt flag | 2.2 V, 3 V      | 20  |     | ns   |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.

Table 5-11 lists the leakage current of the GPIOs.

**Table 5-11. Leakage Current – General-Purpose I/O**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                             | TEST CONDITIONS                   | V <sub>CC</sub> | MIN | MAX | UNIT |
|-------------------------------------------------------|-----------------------------------|-----------------|-----|-----|------|
| I <sub>lkg(Px.x)</sub> High-impedance leakage current | See <sup>(1)</sup> <sup>(2)</sup> | 1.8 V, 3 V      |     | ±50 | nA   |

(1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Table 5-12 lists the output characteristics of the GPIOs.

**Table 5-12. Outputs – General-Purpose I/O (Full Drive Strength)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                              | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-------------------------------------------|----------------------------------------------|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = –3 mA <sup>(1)</sup>  | 1.8 V           | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        | V    |
|                                           | I <sub>(OHmax)</sub> = –10 mA <sup>(2)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –5 mA <sup>(1)</sup>  | 3 V             | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –15 mA <sup>(2)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 3 mA <sup>(1)</sup>   | 1.8 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                                           | I <sub>(OLmax)</sub> = 10 mA <sup>(2)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |
|                                           | I <sub>(OLmax)</sub> = 5 mA <sup>(1)</sup>   | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                                           | I <sub>(OLmax)</sub> = 15 mA <sup>(2)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |

(1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Table 5-13 lists the output characteristics of the GPIOs.

**Table 5-13. Outputs – General-Purpose I/O (Reduced Drive Strength)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                 | TEST CONDITIONS                             | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-------------------------------------------|---------------------------------------------|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = –1 mA <sup>(2)</sup> | 1.8 V           | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        | V    |
|                                           | I <sub>(OHmax)</sub> = –3 mA <sup>(3)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –2 mA <sup>(2)</sup> | 3 V             | V <sub>CC</sub> – 0.25 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = –6 mA <sup>(3)</sup> |                 | V <sub>CC</sub> – 0.60 | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 1 mA <sup>(2)</sup>  | 1.8 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                                           | I <sub>(OLmax)</sub> = 3 mA <sup>(3)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |
|                                           | I <sub>(OLmax)</sub> = 2 mA <sup>(2)</sup>  | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                                           | I <sub>(OLmax)</sub> = 6 mA <sup>(3)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Table 5-14 lists the frequency characteristics of the GPIOs.

**Table 5-14. Output Frequency – Ports P1, P2 and P3**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                           | TEST CONDITIONS                                                                                                           |                                          | MIN | MAX | UNIT |
|-----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|------------------------------------------|-----|-----|------|
| f <sub>Px,y</sub> Port output frequency (with load) | P3.4/TA2CLK/SMCLK/S27<br>C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ <sup>(1)</sup> or 3.2 kΩ <sup>(2)</sup> (3)        | V <sub>CC</sub> = 1.8 V<br>PMMCOREVx = 0 |     | 8   | MHz  |
|                                                     |                                                                                                                           | V <sub>CC</sub> = 3 V<br>PMMCOREVx = 3   |     | 20  |      |
| f <sub>Port_CLK</sub> Clock output frequency        | P1.0/TA0CLK/ACLK/S39<br>P3.4/TA2CLK/SMCLK/S27<br>P2.0/P2MAP0 (P2MAP0 = PM_MCLK )<br>C <sub>L</sub> = 20 pF <sup>(3)</sup> | V <sub>CC</sub> = 1.8 V<br>PMMCOREVx = 0 |     | 8   | MHz  |
|                                                     |                                                                                                                           | V <sub>CC</sub> = 3 V<br>PMMCOREVx = 3   |     | 20  |      |

(1) Full drive strength of port: A resistive divider with 2 × 0.5 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.

(2) Reduced drive strength of port: A resistive divider with 2 × 1.6 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.

(3) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

### 5.8.5.1 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

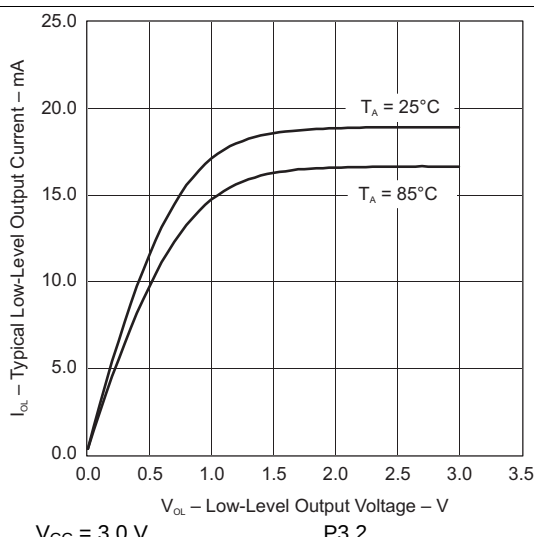


图 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

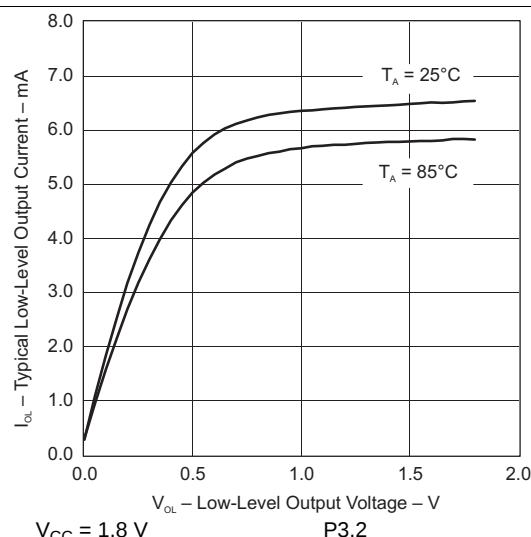


图 5-4. Typical Low-Level Output Current vs Low-Level Output Voltage

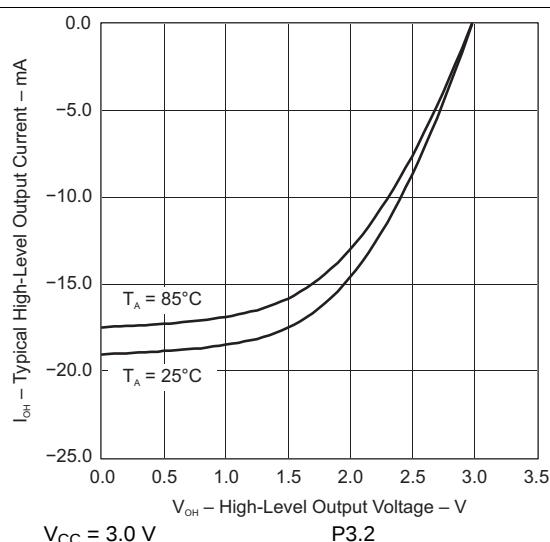


图 5-5. Typical High-Level Output Current Vs High-Level Output Voltage

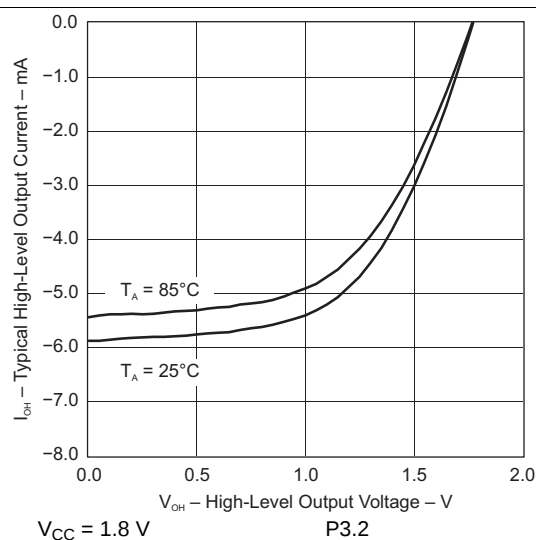


图 5-6. Typical High-Level Output Current Vs High-Level Output Voltage

### 5.8.5.2 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

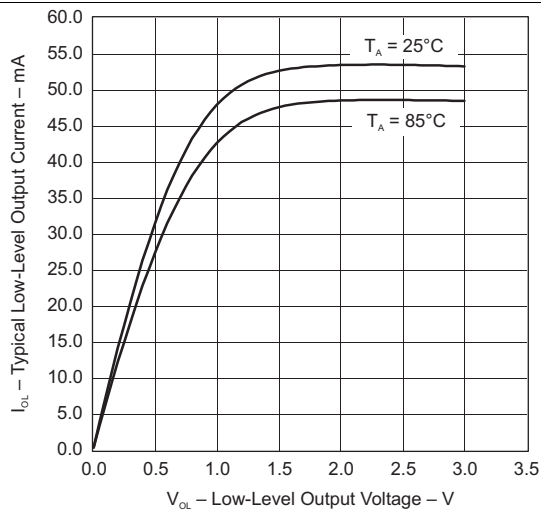


图 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

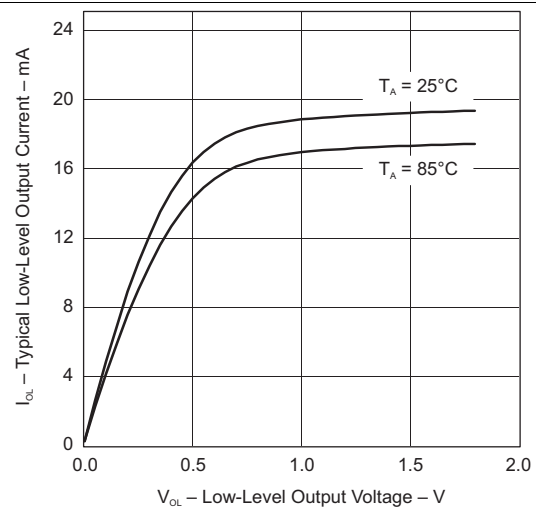


图 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

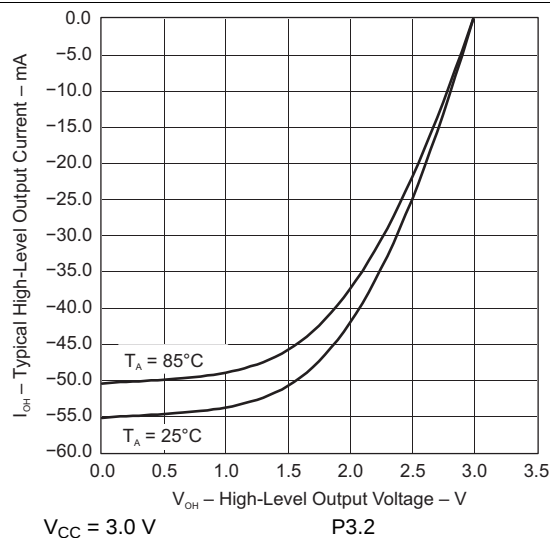


图 5-9. Typical High-Level Output Current vs High-level Output Voltage

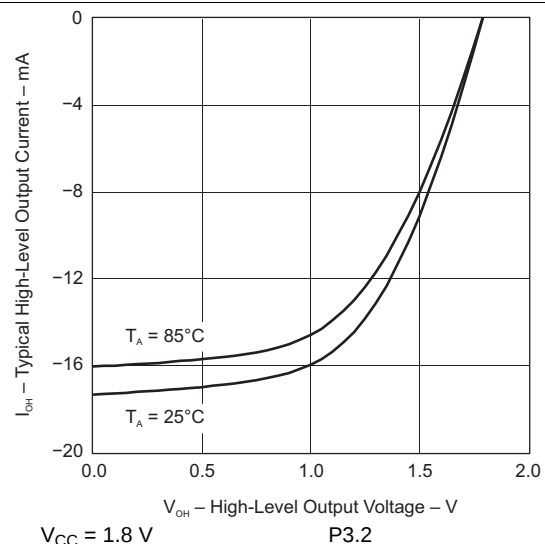


图 5-10. Typical High-Level Output Current vs High-level Output Voltage

## 5.8.6 PMM

Table 5-15 lists the characteristics of the PMM core voltage.

**Table 5-15. PMM, Core Voltage**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                |                                              | TEST CONDITIONS                                                        | MIN | TYP  | MAX | UNIT |
|--------------------------|----------------------------------------------|------------------------------------------------------------------------|-----|------|-----|------|
| V <sub>CORE3</sub> (AM)  | Core voltage, active mode, PMMCOREV = 3      | 2.4 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 mA ≤ I(V <sub>CORE</sub> ) ≤ 21 mA |     | 1.90 |     | V    |
| V <sub>CORE2</sub> (AM)  | Core voltage, active mode, PMMCOREV = 2      | 2.2 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 mA ≤ I(V <sub>CORE</sub> ) ≤ 21 mA |     | 1.80 |     | V    |
| V <sub>CORE1</sub> (AM)  | Core voltage, active mode, PMMCOREV = 1      | 2 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 mA ≤ I(V <sub>CORE</sub> ) ≤ 17 mA   |     | 1.60 |     | V    |
| V <sub>CORE0</sub> (AM)  | Core voltage, active mode, PMMCOREV = 0      | 1.8 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 mA ≤ I(V <sub>CORE</sub> ) ≤ 13 mA |     | 1.40 |     | V    |
| V <sub>CORE3</sub> (LPM) | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 μA ≤ I(V <sub>CORE</sub> ) ≤ 30 μA |     | 1.94 |     | V    |
| V <sub>CORE2</sub> (LPM) | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 μA ≤ I(V <sub>CORE</sub> ) ≤ 30 μA |     | 1.84 |     | V    |
| V <sub>CORE1</sub> (LPM) | Core voltage, low-current mode, PMMCOREV = 1 | 2 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 μA ≤ I(V <sub>CORE</sub> ) ≤ 30 μA   |     | 1.64 |     | V    |
| V <sub>CORE0</sub> (LPM) | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ DV <sub>CC</sub> ≤ 3.6 V, 0 μA ≤ I(V <sub>CORE</sub> ) ≤ 30 μA |     | 1.44 |     | V    |

Table 5-16 lists the characteristics of the SVS high side.

**Table 5-16. PMM, SVS High Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               |                                                   | TEST CONDITIONS                                          | MIN  | TYP  | MAX  | UNIT |
|-------------------------|---------------------------------------------------|----------------------------------------------------------|------|------|------|------|
| I <sub>(SVSH)</sub>     | SVS current consumption                           | SVSHE = 0, DV <sub>CC</sub> = 3.6 V                      |      | 0    |      | nA   |
|                         |                                                   | SVSHE = 1, DV <sub>CC</sub> = 3.6 V, SVSHFP = 0          |      | 200  |      |      |
|                         |                                                   | SVSHE = 1, DV <sub>CC</sub> = 3.6 V, SVSHFP = 1          |      | 2.0  |      | μA   |
| V <sub>(SVSH_IT-)</sub> | SVS <sub>H</sub> on voltage level <sup>(1)</sup>  | SVSHE = 1, SVSHRVL = 0                                   | 1.59 | 1.64 | 1.69 | V    |
|                         |                                                   | SVSHE = 1, SVSHRVL = 1                                   | 1.79 | 1.84 | 1.91 |      |
|                         |                                                   | SVSHE = 1, SVSHRVL = 2                                   | 1.98 | 2.04 | 2.11 |      |
|                         |                                                   | SVSHE = 1, SVSHRVL = 3                                   | 2.10 | 2.16 | 2.23 |      |
| V <sub>(SVSH_IT+)</sub> | SVS <sub>H</sub> off voltage level <sup>(1)</sup> | SVSHE = 1, SVSMHRRRL = 0                                 | 1.62 | 1.74 | 1.81 | V    |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 1                                 | 1.88 | 1.94 | 2.01 |      |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 2                                 | 2.07 | 2.14 | 2.21 |      |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 3                                 | 2.20 | 2.26 | 2.33 |      |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 4                                 | 2.32 | 2.40 | 2.48 |      |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 5                                 | 2.56 | 2.70 | 2.84 |      |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 6                                 | 2.85 | 3.00 | 3.15 |      |
|                         |                                                   | SVSHE = 1, SVSMHRRRL = 7                                 | 2.85 | 3.00 | 3.15 |      |
| t <sub>pd</sub> (SVSH)  | SVS <sub>H</sub> propagation delay                | SVSHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVSHFP = 1 |      | 2.5  |      | μs   |
|                         |                                                   | SVSHE = 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVSHFP = 0  |      | 20   |      |      |
| t <sub>(SVSH)</sub>     | SVS <sub>H</sub> on or off delay time             | SVSHE = 0→1, SVSHFP = 1                                  |      | 12.5 |      | μs   |
|                         |                                                   | SVSHE = 0→1, SVSHFP = 0                                  |      | 100  |      |      |
| dV <sub>DVCC</sub> /dt  | DV <sub>CC</sub> rise time                        |                                                          | 0    |      | 1000 | V/s  |

(1) The SVS<sub>H</sub> settings available depend on the VCORE (PMMCOREV) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430x5xx and MSP430x6xx Family User's Guide](#) on recommended settings and use.

Table 5-17 lists the characteristics of the SVM high side.

**Table 5-17. PMM, SVM High Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                            | TEST CONDITIONS                                          | MIN  | TYP  | MAX  | UNIT |
|----------------------------------------------------------------------|----------------------------------------------------------|------|------|------|------|
| $I_{(SVMH)}$ SVM <sub>H</sub> current consumption                    | SVMHE = 0, DV <sub>CC</sub> = 3.6 V                      |      | 0    |      | nA   |
|                                                                      | SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 0          |      | 200  |      |      |
|                                                                      | SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 1          |      | 2.0  |      | μA   |
| $V_{(SVMH)}$ SVM <sub>H</sub> on or off voltage level <sup>(1)</sup> | SVMHE = 1, SVSMHRRRL = 0                                 | 1.65 | 1.74 | 1.86 | V    |
|                                                                      | SVMHE = 1, SVSMHRRRL = 1                                 | 1.85 | 1.94 | 2.02 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 2                                 | 2.02 | 2.14 | 2.22 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 3                                 | 2.18 | 2.26 | 2.35 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 4                                 | 2.32 | 2.40 | 2.48 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 5                                 | 2.56 | 2.70 | 2.84 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 6                                 | 2.85 | 3.00 | 3.15 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 7                                 | 2.85 | 3.00 | 3.15 |      |
| $t_{pd(SVMH)}$ SVM <sub>H</sub> propagation delay                    | SVMHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVMHFP = 1 |      | 2.5  |      | μs   |
|                                                                      | SVMHE = 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVMHFP = 0  |      | 20   |      |      |
| $t_{(SVMH)}$ SVM <sub>H</sub> on or off delay time                   | SVMHE = 0→1, SVSMF = 1                                   |      | 12.5 |      | μs   |
|                                                                      | SVMHE = 0→1, SVMHFP = 0                                  |      | 100  |      |      |

(1) The SVM<sub>H</sub> settings available depend on the VCORE (PMMCOREV) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430x5xx and MSP430x6xx Family User's Guide](#) on recommended settings and use.

Table 5-18 lists the characteristics of the SVS low side.

**Table 5-18. PMM, SVS Low Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                          | TEST CONDITIONS                                          | MIN | TYP  | MAX | UNIT |
|----------------------------------------------------|----------------------------------------------------------|-----|------|-----|------|
| $I_{(SVSL)}$ SVS <sub>L</sub> current consumption  | SVSLE = 0, PMMCOREV = 2                                  |     | 0    |     | nA   |
|                                                    | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0                      |     | 200  |     |      |
|                                                    | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1                      |     | 2.0  |     | μA   |
| $t_{pd(SVSL)}$ SVS <sub>L</sub> propagation delay  | SVSLE = 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVSLFP = 1 |     | 2.5  |     | μs   |
|                                                    | SVSLE = 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVSLFP = 0  |     | 20   |     |      |
| $t_{(SVSL)}$ SVS <sub>L</sub> on or off delay time | SVSLE = 0→1, SVSLFP = 1                                  |     | 12.5 |     | μs   |
|                                                    | SVSLE = 0→1, SVSLFP = 0                                  |     | 100  |     |      |

Table 5-19 lists the characteristics of the SVM low side.

**Table 5-19. PMM, SVM Low Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                          | TEST CONDITIONS                                          | MIN | TYP  | MAX | UNIT |
|----------------------------------------------------|----------------------------------------------------------|-----|------|-----|------|
| $I_{(SVML)}$ SVM <sub>L</sub> current consumption  | SVMLE = 0, PMMCOREV = 2                                  |     | 0    |     | nA   |
|                                                    | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0                      |     | 200  |     |      |
|                                                    | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1                      |     | 2.0  |     | μA   |
| $t_{pd(SVML)}$ SVM <sub>L</sub> propagation delay  | SVMLE = 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVMLFP = 1 |     | 2.5  |     | μs   |
|                                                    | SVMLE = 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVMLFP = 0  |     | 20   |     |      |
| $t_{(SVML)}$ SVM <sub>L</sub> on or off delay time | SVMLE = 0→1, SVMLFP = 1                                  |     | 12.5 |     | μs   |
|                                                    | SVMLE = 0→1, SVMLFP = 0                                  |     | 100  |     |      |

### 5.8.7 Timers

Table 5-20 lists the characteristics of Timer\_A.

**Table 5-20. Timer\_A, Timers TA0, TA1, and TA2**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS                                                       | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------------------------------|-----------------------------------------------------------------------|-----------------|-----|-----|------|
| f <sub>TA</sub> Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% ±10% | 1.8 V, 3 V      |     | 20  | MHz  |
| t <sub>TA,cap</sub> Timer_A capture timing    | All capture inputs, minimum pulse<br>duration required for capture    | 1.8 V, 3 V      | 20  |     | ns   |

Table 5-21 lists the characteristics of Timer\_B.

**Table 5-21. Timer\_B, Timer TB0**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS                                                       | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------------------------------|-----------------------------------------------------------------------|-----------------|-----|-----|------|
| f <sub>TB</sub> Timer_B input clock frequency | Internal: SMCLK or ACLK,<br>External: TBCLK,<br>Duty cycle = 50% ±10% | 1.8 V, 3 V      |     | 20  | MHz  |
| t <sub>TB,cap</sub> Timer_B capture timing    | All capture inputs, minimum pulse<br>duration required for capture    | 1.8 V, 3 V      | 20  |     | ns   |

### 5.8.8 Battery Backup

Table 5-22 lists the characteristics of the battery backup.

**Table 5-22. Battery Backup**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                                                                      | TEST CONDITIONS                                     |                        | V <sub>CC</sub> | MIN                   | TYP  | MAX | UNIT |
|----------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------|------------------------|-----------------|-----------------------|------|-----|------|
| I <sub>VBAT</sub>    | Current into VBAT terminal in case no primary battery is connected.                  | VBAT = 1.7 V,<br>DVCC not connected,<br>RTC running | T <sub>A</sub> = −40°C |                 | 0.43                  |      | μA  |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 25°C  |                 | 0.52                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 60°C  |                 | 0.58                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 85°C  |                 | 0.66                  |      |     |      |
|                      |                                                                                      | VBAT = 2.2 V,<br>DVCC not connected,<br>RTC running | T <sub>A</sub> = −40°C |                 | 0.50                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 25°C  |                 | 0.59                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 60°C  |                 | 0.64                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 85°C  |                 | 0.72                  |      |     |      |
|                      |                                                                                      | VBAT = 3 V,<br>DVCC not connected,<br>RTC running   | T <sub>A</sub> = −40°C |                 | 0.68                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 25°C  |                 | 0.75                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 60°C  |                 | 0.79                  |      |     |      |
|                      |                                                                                      |                                                     | T <sub>A</sub> = 85°C  |                 | 0.86                  |      |     |      |
| V <sub>SWITCH</sub>  | Switch-over level (V <sub>CC</sub> to VBAT)                                          | C <sub>VCC</sub> = 4.7 μF                           | General                |                 | V <sub>SVSH_IT-</sub> |      | V   |      |
|                      |                                                                                      |                                                     | SVSHRL = 0             |                 | 1.59                  | 1.69 |     |      |
|                      |                                                                                      |                                                     | SVSHRL = 1             |                 | 1.79                  | 1.91 |     |      |
|                      |                                                                                      |                                                     | SVSHRL = 2             |                 | 1.98                  | 2.11 |     |      |
|                      |                                                                                      |                                                     | SVSHRL = 3             |                 | 2.10                  | 2.23 |     |      |
|                      |                                                                                      |                                                     |                        |                 |                       |      |     |      |
| R <sub>ON_VBAT</sub> | ON-resistance of switch between VBAT and VBAK                                        | V <sub>BAT</sub> = 1.8 V                            |                        | 0 V             | 0.35                  | 1    | kΩ  |      |
| V <sub>BAT3</sub>    | VBAT to ADC:<br>V <sub>BAT</sub> divided,<br>V <sub>BAT3</sub> = V <sub>BAT</sub> /3 |                                                     |                        | 1.8 V           | 0.6                   | ±5%  | V   |      |
|                      |                                                                                      |                                                     |                        | 3 V             | 1.0                   | ±5%  |     |      |
|                      |                                                                                      |                                                     |                        | 3.6 V           | 1.2                   | ±5%  |     |      |
| V <sub>CHVx</sub>    | Charger end voltage                                                                  | CHVx = 2                                            |                        |                 | 2.65                  | 2.7  | 2.9 | V    |
| R <sub>CHARGE</sub>  | Charge limiting resistor                                                             |                                                     | CHCx = 1               |                 | 5.2                   |      | kΩ  |      |
|                      |                                                                                      |                                                     | CHCx = 2               |                 | 10.2                  |      |     |      |
|                      |                                                                                      |                                                     | CHCx = 3               |                 | 20                    |      |     |      |

## 5.8.9 USCI

Table 5-23 lists the characteristics of the USCI in UART mode.

**Table 5-23. USCI (UART Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                              | TEST CONDITIONS                                                      | V <sub>CC</sub> | MIN                 | MAX | UNIT |
|------------------------------------------------------------------------|----------------------------------------------------------------------|-----------------|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                           | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% |                 | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency (equals baud rate in MBaud) |                                                                      |                 |                     | 1   | MHz  |
| t <sub>t</sub> UART receive deglitch time <sup>(1)</sup>               |                                                                      | 2.2 V           | 50                  | 600 | ns   |
|                                                                        |                                                                      | 3 V             | 50                  | 600 |      |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

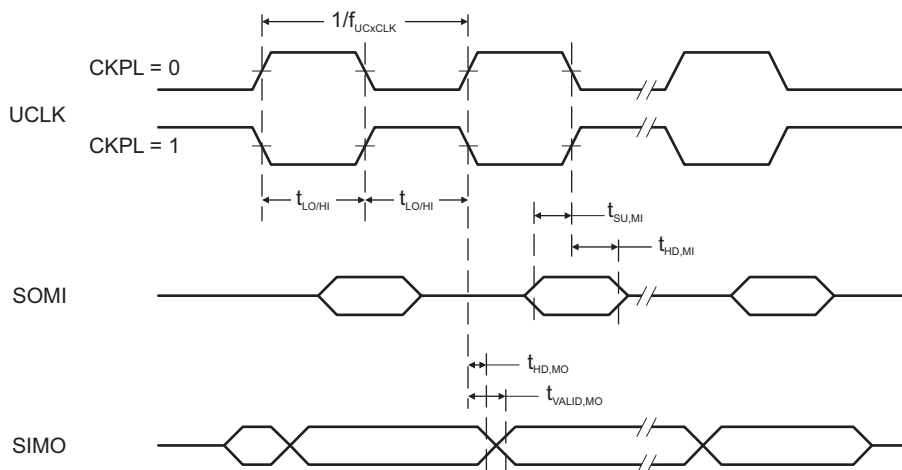
Table 5-24 lists the characteristics of the USCI in SPI master mode.

**Table 5-24. USCI (SPI Master Mode)**

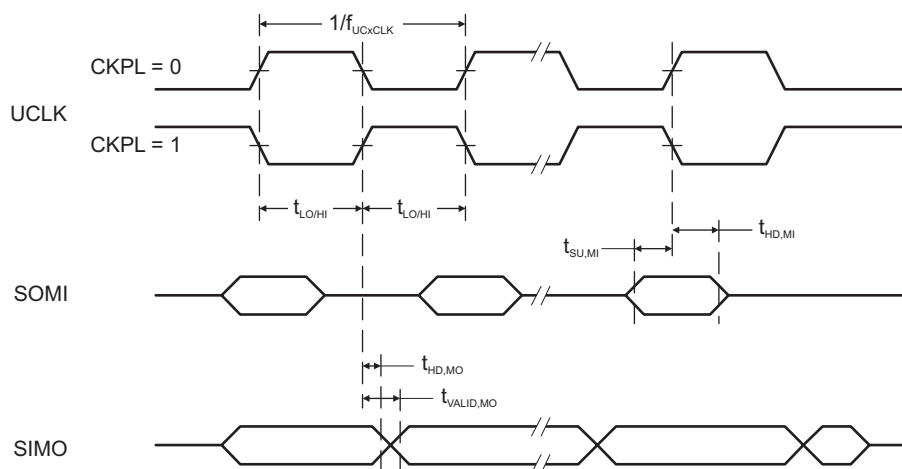
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>  
(see Figure 5-11 and Figure 5-12)

| PARAMETER                                                        | TEST CONDITIONS                                                  | V <sub>CC</sub> | MIN                 | MAX | UNIT |
|------------------------------------------------------------------|------------------------------------------------------------------|-----------------|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                     | SMCLK, ACLK, duty cycle = 50% ±10%                               |                 | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>SU,MI</sub> SOMI input data setup time                    | PMMCOREV = 0                                                     | 1.8 V           | 55                  |     | ns   |
|                                                                  |                                                                  | 3 V             | 38                  |     |      |
|                                                                  | PMMCOREV = 3                                                     | 2.4 V           | 30                  |     |      |
|                                                                  |                                                                  | 3 V             | 25                  |     |      |
| t <sub>HD,MI</sub> SOMI input data hold time                     | PMMCOREV = 0                                                     | 1.8 V           | 0                   |     | ns   |
|                                                                  |                                                                  | 3 V             | 0                   |     |      |
|                                                                  | PMMCOREV = 3                                                     | 2.4 V           | 0                   |     |      |
|                                                                  |                                                                  | 3 V             | 0                   |     |      |
| t <sub>VALID,MO</sub> SIMO output data valid time <sup>(2)</sup> | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF, PMMCOREV = 0 | 1.8 V           |                     | 20  | ns   |
|                                                                  |                                                                  | 3 V             |                     | 18  |      |
|                                                                  | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF, PMMCOREV = 3 | 2.4 V           |                     | 16  |      |
|                                                                  |                                                                  | 3 V             |                     | 15  |      |
| t <sub>HD,MO</sub> SIMO output data hold time <sup>(3)</sup>     | C <sub>L</sub> = 20 pF, PMMCOREV = 0                             | 1.8 V           | –10                 |     | ns   |
|                                                                  |                                                                  | 3 V             | –8                  |     |      |
|                                                                  | C <sub>L</sub> = 20 pF, PMMCOREV = 3                             | 2.4 V           | –10                 |     |      |
|                                                                  |                                                                  | 3 V             | –8                  |     |      |

- (1)  $f_{UCLK} = 1/2t_{LO/Hi}$  with  $t_{LO/Hi} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$   
For the slave parameters  $t_{SU,SI}(Slave)$  and  $t_{VALID,SO}(Slave)$ , see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-11 and Figure 5-12.



**Figure 5-11. SPI Master Mode, CKPH = 0**



**Figure 5-12. SPI Master Mode, CKPH = 1**

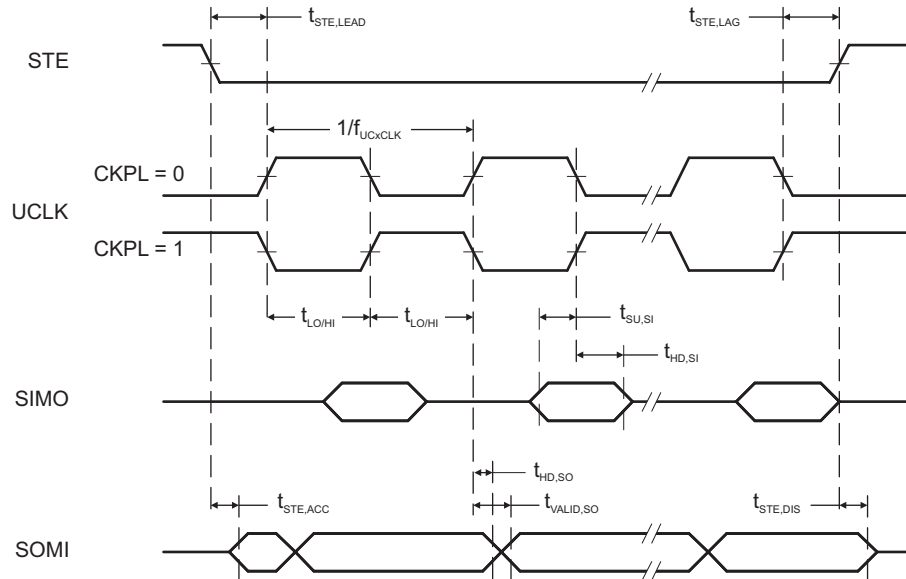
Table 5-25 lists the characteristics of the USCI in SPI slave mode.

**Table 5-25. USCI (SPI Slave Mode)**

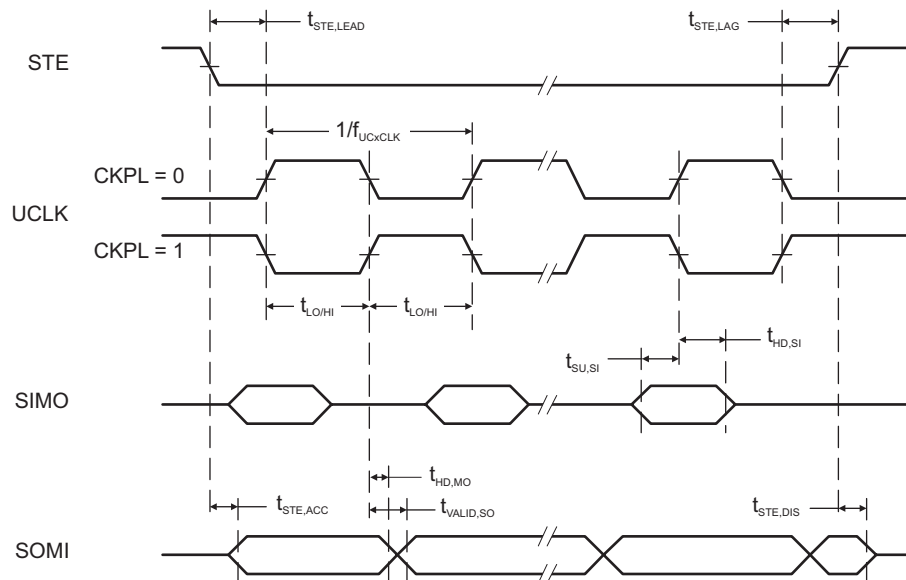
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>  
(see Figure 5-13 and Figure 5-14)

| PARAMETER                                                              | TEST CONDITIONS                                               | V <sub>CC</sub> | MIN | MAX | UNIT |
|------------------------------------------------------------------------|---------------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>STE,LEAD</sub> STE lead time, STE low to clock                  | PMMCOREV = 0                                                  | 1.8 V           | 11  |     | ns   |
|                                                                        |                                                               | 3 V             | 8   |     |      |
|                                                                        | PMMCOREV = 3                                                  | 2.4 V           | 7   |     |      |
|                                                                        |                                                               | 3 V             | 6   |     |      |
| t <sub>STE,LAG</sub> STE lag time, Last clock to STE high              | PMMCOREV = 0                                                  | 1.8 V           | 3   |     | ns   |
|                                                                        |                                                               | 3 V             | 3   |     |      |
|                                                                        | PMMCOREV = 3                                                  | 2.4 V           | 3   |     |      |
|                                                                        |                                                               | 3 V             | 3   |     |      |
| t <sub>STE,ACC</sub> STE access time, STE low to SOMI data out         | PMMCOREV = 0                                                  | 1.8 V           |     | 66  | ns   |
|                                                                        |                                                               | 3 V             |     | 50  |      |
|                                                                        | PMMCOREV = 3                                                  | 2.4 V           |     | 36  |      |
|                                                                        |                                                               | 3 V             |     | 30  |      |
| t <sub>STE,DIS</sub> STE disable time, STE high to SOMI high impedance | PMMCOREV = 0                                                  | 1.8 V           |     | 30  | ns   |
|                                                                        |                                                               | 3 V             |     | 30  |      |
|                                                                        | PMMCOREV = 3                                                  | 2.4 V           |     | 30  |      |
|                                                                        |                                                               | 3 V             |     | 30  |      |
| t <sub>SU,SI</sub> SIMO input data setup time                          | PMMCOREV = 0                                                  | 1.8 V           | 5   |     | ns   |
|                                                                        |                                                               | 3 V             | 5   |     |      |
|                                                                        | PMMCOREV = 3                                                  | 2.4 V           | 2   |     |      |
|                                                                        |                                                               | 3 V             | 2   |     |      |
| t <sub>HD,SI</sub> SIMO input data hold time                           | PMMCOREV = 0                                                  | 1.8 V           | 5   |     | ns   |
|                                                                        |                                                               | 3 V             | 5   |     |      |
|                                                                        | PMMCOREV = 3                                                  | 2.4 V           | 5   |     |      |
|                                                                        |                                                               | 3 V             | 5   |     |      |
| t <sub>VALID,SO</sub> SOMI output data valid time <sup>(2)</sup>       | UCLK edge to SOMI valid, C <sub>L</sub> = 20 pF, PMMCOREV = 0 | 1.8 V           |     | 76  | ns   |
|                                                                        |                                                               | 3 V             |     | 60  |      |
|                                                                        | UCLK edge to SOMI valid, C <sub>L</sub> = 20 pF, PMMCOREV = 3 | 2.4 V           |     | 44  |      |
|                                                                        |                                                               | 3 V             |     | 40  |      |
| t <sub>HD,SO</sub> SOMI output data hold time <sup>(3)</sup>           | C <sub>L</sub> = 20 pF, PMMCOREV = 0                          | 1.8 V           | 12  |     | ns   |
|                                                                        |                                                               | 3 V             | 12  |     |      |
|                                                                        | C <sub>L</sub> = 20 pF, PMMCOREV = 3                          | 2.4 V           | 12  |     |      |
|                                                                        |                                                               | 3 V             | 12  |     |      |

- (1)  $f_{UCXCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$   
For the master parameters  $t_{SU,MI(Master)}$  and  $t_{VALID,MO(Master)}$ , see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.



**Figure 5-13. SPI Slave Mode, CKPH = 0**



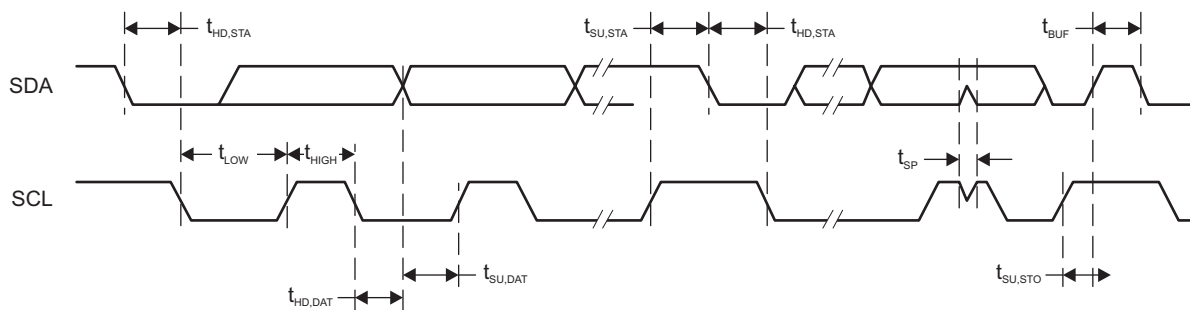
**Figure 5-14. SPI Slave Mode, CKPH = 1**

Table 5-26 lists the characteristics of the USCI in I<sup>2</sup>C mode.

**Table 5-26. USCI (I<sup>2</sup>C Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-15)

| PARAMETER           |                                                     | TEST CONDITIONS                                                      | V <sub>CC</sub> | MIN                 | MAX | UNIT |
|---------------------|-----------------------------------------------------|----------------------------------------------------------------------|-----------------|---------------------|-----|------|
| f <sub>USCI</sub>   | USCI input clock frequency                          | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% |                 | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>SCL</sub>    | SCL clock frequency                                 |                                                                      | 2.2 V, 3 V      | 0                   | 400 | kHz  |
| t <sub>HD,STA</sub> | Hold time (repeated) START                          | f <sub>SCL</sub> ≤ 100 kHz                                           | 2.2 V, 3 V      | 4.0                 |     | μs   |
|                     |                                                     | f <sub>SCL</sub> > 100 kHz                                           |                 | 0.6                 |     |      |
| t <sub>SU,STA</sub> | Setup time for a repeated START                     | f <sub>SCL</sub> ≤ 100 kHz                                           | 2.2 V, 3 V      | 4.7                 |     | μs   |
|                     |                                                     | f <sub>SCL</sub> > 100 kHz                                           |                 | 0.6                 |     |      |
| t <sub>HD,DAT</sub> | Data hold time                                      |                                                                      | 2.2 V, 3 V      | 0                   |     | ns   |
| t <sub>SU,DAT</sub> | Data setup time                                     |                                                                      | 2.2 V, 3 V      | 250                 |     | ns   |
| t <sub>SU,STO</sub> | Setup time for STOP                                 | f <sub>SCL</sub> ≤ 100 kHz                                           | 2.2 V, 3 V      | 4.0                 |     | μs   |
|                     |                                                     | f <sub>SCL</sub> > 100 kHz                                           |                 | 0.6                 |     |      |
| t <sub>SP</sub>     | Pulse duration of spikes suppressed by input filter |                                                                      | 2.2 V           | 50                  | 600 | ns   |
|                     |                                                     |                                                                      | 3 V             | 50                  | 600 |      |



**Figure 5-15. I<sup>2</sup>C Mode Timing**

### 5.8.10 LCD Controller

Table 5-27 lists the operating conditions of the LCD controller.

**Table 5-27. LCD\_B Operating Conditions**

| PARAMETER                      | CONDITIONS                                                                                     | MIN                                                                                 | NOM | MAX | UNIT |
|--------------------------------|------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|-----|------|
| $V_{CC,LCD\_B}$ ,<br>CP en,3,6 | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6$ V                                | LCDPEN = 1, $0000 < VLCDx \leq 1111$<br>(charge pump enabled, $V_{LCD} \leq 3.6$ V) |     |     | V    |
| $V_{CC,LCD\_B}$ ,<br>CP en,3,3 | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.3$ V                                | LCDPEN = 1, $0000 < VLCDx \leq 1100$<br>(charge pump enabled, $V_{LCD} \leq 3.3$ V) |     |     | V    |
| $V_{CC,LCD\_B}$ ,<br>int. bias | Supply voltage range, internal biasing, charge pump disabled                                   | LCDPEN = 0, VLCDx = 0                                                               |     |     | V    |
| $V_{CC,LCD\_B}$ ,<br>ext. bias | Supply voltage range, external biasing, charge pump disabled                                   | LCDPEN = 0, VLCDx = 0                                                               |     |     | V    |
| $V_{CC,LCD\_B}$ ,<br>VLCDx     | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDPEN = 0, VLCDx = 1                                                               |     |     | V    |
| $V_{LDCAP/R33}$                | External LCD voltage at LDCAP/R33, internal or external biasing, charge pump disabled          | LCDPEN = 0, VLCDx = 1                                                               |     |     | V    |
| $C_{LDCAP}$                    | Capacitor on LDCAP when charge pump enabled                                                    | LCDPEN = 1, VLCDx > 0000<br>(charge pump enabled)                                   |     |     | μF   |
| $f_{Frame}$                    | LCD frame frequency range                                                                      | $f_{LCD} = 2 \times \text{MUX} \times f_{FRAME}$<br>(mux = 1 (static), 2, 3, 4)     |     |     | Hz   |
| $f_{ACLK,in}$                  | ACLK input frequency range                                                                     |                                                                                     |     |     | kHz  |
| $C_{Panel}$                    | Panel capacitance                                                                              | 100-Hz frame frequency                                                              |     |     | pF   |
| $V_{R33}$                      | Analog input voltage at R33                                                                    | LCDPEN = 0, VLCDx = 1                                                               |     |     | V    |
| $V_{R23,1/3bias}$              | Analog input voltage at R23                                                                    | LCDREXT = 1, LCDEXTBIAS = 1,<br>LCD2B = 0                                           |     |     | V    |
| $V_{R13,1/3bias}$              | Analog input voltage at R13 with 1/3 biasing                                                   | LCDREXT = 1, LCDEXTBIAS = 1,<br>LCD2B = 0                                           |     |     | V    |
| $V_{R13,1/2bias}$              | Analog input voltage at R13 with 1/2 biasing                                                   | LCDREXT = 1, LCDEXTBIAS = 1,<br>LCD2B = 1                                           |     |     | V    |
| $V_{R03}$                      | Analog input voltage at R03                                                                    | R0EXT = 1                                                                           |     |     | V    |
| $V_{LCD}-V_{R03}$              | Voltage difference between $V_{LCD}$ and R03                                                   | LCDPEN = 0, R0EXT = 1                                                               |     |     | V    |
| $V_{LCDREF/R13}$               | External LCD reference voltage applied at LCDREF/R13                                           | VLCDREFx = 01                                                                       |     |     | V    |

Table 5-28 lists the characteristics of the LCD controller.

**Table 5-28. LCD\_B, Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                  | TEST CONDITIONS                                              | V <sub>CC</sub> | MIN | TYP             | MAX | UNIT |
|----------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|-----|-----------------|-----|------|
| V <sub>LCD</sub> LCD voltage                                               | VLCDx = 0000, VLCDxEXT = 0                                   | 2.4 V to 3.6 V  |     | V <sub>CC</sub> |     | V    |
|                                                                            | LCDCPEN = 1, VLCDx = 0001                                    | 2 V to 3.6 V    |     | 2.60            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 0010                                    | 2 V to 3.6 V    |     | 2.66            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 0011                                    | 2 V to 3.6 V    |     | 2.72            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 0100                                    | 2 V to 3.6 V    |     | 2.79            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 0101                                    | 2 V to 3.6 V    |     | 2.85            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 0110                                    | 2 V to 3.6 V    |     | 2.92            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 0111                                    | 2 V to 3.6 V    |     | 2.98            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1000                                    | 2 V to 3.6 V    |     | 3.05            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1001                                    | 2 V to 3.6 V    |     | 3.10            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1010                                    | 2 V to 3.6 V    |     | 3.17            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1011                                    | 2 V to 3.6 V    |     | 3.24            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1100                                    | 2 V to 3.6 V    |     | 3.30            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1101                                    | 2.2 V to 3.6 V  |     | 3.36            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1110                                    | 2.2 V to 3.6 V  |     | 3.42            |     |      |
|                                                                            | LCDCPEN = 1, VLCDx = 1111                                    | 2.2 V to 3.6 V  |     | 3.48            | 3.6 |      |
| I <sub>CC,Peak,CP</sub> Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111                                    | 2.2 V           |     | 400             |     | μA   |
| t <sub>LCD,CP,on</sub> Time to charge C <sub>LCD</sub> when discharged     | C <sub>LCD</sub> = 4.7 μF,<br>LCDCPEN = 0→1,<br>VLCDx = 1111 | 2.2 V           |     | 100             | 500 | ms   |
| I <sub>CP,Load</sub> Maximum charge pump load current                      | LCDCPEN = 1, VLCDx = 1111                                    | 2.2 V           | 50  |                 |     | μA   |
| R <sub>LCD,Seg</sub> LCD driver output impedance, segment lines            | LCDCPEN = 1, VLCDx = 1000,<br>I <sub>LOAD</sub> = ±10 μA     | 2.2 V           |     |                 | 10  | kΩ   |
| R <sub>LCD,COM</sub> LCD driver output impedance, common lines             | LCDCPEN = 1, VLCDx = 1000,<br>I <sub>LOAD</sub> = ±10 μA     | 2.2 V           |     |                 | 10  | kΩ   |

### 5.8.11 CTSD16

#### NOTE

The delta-sigma analog-to-digital converter uses the CTSD16. The CTSD16 is preceded by a unity-gain buffer stage following the channel muxing as shown in [Figure 6-2](#). See [Table 5-43](#) for the electrical characteristics of the PGA buffer stages.

[Table 5-29](#) lists the operating conditions of the CTSD16.

**Table 5-29. CTSD16, Power Supply and Operating Conditions**

| PARAMETER              |                                                                                   | TEST CONDITIONS                                                                                                                                                                                                                                      |                      | V <sub>CC</sub> | MIN                | TYP | MAX                | UNIT |
|------------------------|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------------|--------------------|-----|--------------------|------|
| V <sub>CC</sub>        | Supply voltage range                                                              | AVSS = DVSS = 0 V                                                                                                                                                                                                                                    |                      |                 | 2.2                |     | 3.6                | V    |
| I <sub>CTSD16</sub>    | Analog plus digital supply current per converter (reference current not included) | CTSD16OSRx = 256, CTSD16RRI = 0                                                                                                                                                                                                                      | GAIN: 1, 2, 4, 8, 16 | 3 V             | 190 <sup>(1)</sup> |     | 300 <sup>(1)</sup> | μA   |
|                        |                                                                                   |                                                                                                                                                                                                                                                      | GAIN: 1, 16          | 3 V             |                    |     |                    |      |
| I <sub>CTSD16CLK</sub> | CTSD16 clock current consumption                                                  | This is requested when CTSD16 is converting, or CTSD16RRIBURST = 0, or when OA is in rail-to-rail input mode (OARRI = 1), or when OA charge pump is on. The current should only be counted once even if both OA and CTSD16 are requesting the clock. |                      | 3 V             |                    | 205 | 240                | μA   |

(1) See [Table 5-30](#) to calculate total current from CTSD16 for different use cases.

[Table 5-30](#) explains how to compute the total current, I<sub>TOTAL</sub>, when the CTSD, along with associated modules, are used. See [Table 5-44](#) for a similar table for the OA. A "yes" means it must be included in computing I<sub>TOTAL</sub>. Here is an example current calculation for CTSD16 in rail-to-rail input mode (CTSD16RRI = 1) using the internal reference (CTSD16REFS = 1) and OA0 and OA1 enabled in rail-to-rail input modes, OARRI = 1.

As an example, assume that the application uses the CTSD16 in rail-to-rail input mode (CTSD16RRI = 1) with the internal reference (CTSD16REFS = 1) and OA0 and OA1 are enabled in rail-to-rail input modes, OARRI = 1. The total current, I<sub>TOTAL</sub>, would be computed as follows:

$$I_{TOTAL} = I_{CTSD16} + I_{CTSD16CLK} + I_{CP} + I_{REFBG} + 2 \times I_{OA} \quad (1)$$

**Table 5-30. CTSD16, Current Calculation**

| USE CASE NAME              | USE CASE DETAILS | I <sub>CTSD16</sub> | I <sub>CTSD16CLK</sub> <sup>(1)</sup> | I <sub>CP</sub> <sup>(2)</sup> | I <sub>REFBG</sub> <sup>(3)</sup>             | I <sub>REF</sub> <sup>(4)</sup> |
|----------------------------|------------------|---------------------|---------------------------------------|--------------------------------|-----------------------------------------------|---------------------------------|
| CTSD16                     |                  | yes                 | yes                                   | no                             | yes if CTSD16REFS = 1<br>no if CTSD16REFS = 0 | yes                             |
| CTSD16 rail-to-rail inputs | CTSD16RRI = 1    | yes                 | yes                                   | yes                            | yes if CTSD16REFS = 1<br>no if CTSD16REFS = 0 | yes                             |

- (1) Count this only once no matter how many modules use it. OA can also use this when rail-to-rail input is selected.
- (2) Count this only once no matter how many modules use it. OA also uses this. This current is listed in [Table 5-43](#).
- (3) Count this only once no matter how many modules use it. DAC can use this as well as internal reference when it is available externally, REFOUT = 1. This current is listed in [Table 5-36](#).
- (4) Count this only once no matter how many modules use it. This current is listed in [Table 5-43](#). If I<sub>REFBG</sub> is used that includes I<sub>REF</sub> current.

Table 5-31 lists the characteristics of the CTSD16 external voltage reference.

**Table 5-31. CTSD16, External Voltage Reference**

| PARAMETER                               | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------------------------|-----------------|-----------------|-----|-----|-----|------|
| V <sub>VeREF+</sub> Input voltage range | CTSD16REFS = 0  | 3 V             | 1.0 | 1.2 | 1.5 | V    |
| I <sub>VeREF+</sub> Input current       | CTSD16REFS = 0  | 3 V             |     |     | 50  | nA   |

Table 5-32 lists the characteristics of the CTSD16 input range.

**Table 5-32. CTSD16, Input Range<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER           |                                                                           | TEST CONDITIONS                                                                                  |                  | V <sub>CC</sub> | MIN                                                 | TYP | MAX                                                 | UNIT |
|---------------------|---------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|------------------|-----------------|-----------------------------------------------------|-----|-----------------------------------------------------|------|
| V <sub>ID,FSR</sub> | Differential full-scale input voltage range                               | V <sub>ID</sub> = V <sub>I,A+</sub> – V <sub>I,A–</sub>                                          |                  |                 | –V <sub>R</sub> /Gain                               |     | +V <sub>R</sub> /Gain                               | V    |
| V <sub>I,FSR</sub>  | Single-ended full-scale input voltage range                               | V <sub>ID</sub> = V <sub>I,A+</sub> – V <sub>R</sub><br>negative input is tied to V <sub>R</sub> |                  |                 | V <sub>R</sub> –<br>V <sub>R</sub> /Gain            |     | V <sub>R</sub> +<br>V <sub>R</sub> /Gain            | V    |
| V <sub>ID</sub>     | Differential input voltage range for specified performance <sup>(2)</sup> | CTSD16REFS = 1                                                                                   | CTSD16GAINx = 1  |                 | ±928                                                |     | mV                                                  |      |
|                     |                                                                           |                                                                                                  | CTSD16GAINx = 2  |                 | ±464                                                |     |                                                     |      |
|                     |                                                                           |                                                                                                  | CTSD16GAINx = 4  |                 | ±232                                                |     |                                                     |      |
|                     |                                                                           |                                                                                                  | CTSD16GAINx = 8  |                 | ±116                                                |     |                                                     |      |
|                     |                                                                           |                                                                                                  | CTSD16GAINx = 16 |                 | ±58                                                 |     |                                                     |      |
| V <sub>I</sub>      | Single-ended input voltage range for specified performance                |                                                                                                  |                  |                 | V <sub>R</sub> –<br>(0.8 ×<br>V <sub>R</sub> /Gain) |     | V <sub>R</sub> +<br>(0.8 ×<br>V <sub>R</sub> /Gain) | V    |
| Z <sub>I</sub>      | Input impedance (pin Ax or ADx+ or ADx- to AVSS)                          | CTSD16GAINx = 1, 16                                                                              |                  | 3 V             | 20                                                  |     |                                                     | MΩ   |
| Z <sub>ID</sub>     | Differential input impedance (pin ADx+ to pin ADx-)                       | CTSD16GAINx = 1, 16                                                                              |                  | 3 V             | 35                                                  |     |                                                     | MΩ   |
| V <sub>I</sub>      | Absolute input voltage range                                              |                                                                                                  |                  |                 | AVSS                                                |     | V <sub>CC</sub>                                     | V    |
| V <sub>IC</sub>     | Common-mode input voltage range                                           |                                                                                                  |                  |                 | AVSS                                                |     | V <sub>CC</sub>                                     | V    |

(1) All parameters pertain to each CTSD16 input.

(2) The full-scale range is defined by V<sub>FSR+</sub> = +V<sub>R</sub>/GAIN and V<sub>FSR–</sub> = –V<sub>R</sub>/GAIN; FSR = V<sub>FSR+</sub> – V<sub>FSR–</sub> = 2xV<sub>R</sub>/GAIN. If V<sub>R</sub> is sourced externally, the analog input range should not exceed 80% of V<sub>FSR+</sub> or V<sub>FSR–</sub>; that is, V<sub>ID</sub> = 0.8 V<sub>FSR–</sub> to 0.8 V<sub>FSR+</sub>. If V<sub>R</sub> is sourced internally, the given V<sub>ID</sub> ranges apply.

Table 5-33 lists the performance characteristics of the CTSD16.

**Table 5-33. CTSD16, Performance**

CTSD16OSRx = 256, CTSD164REFS = 1 (see Figure 5-16, Figure 5-17, and Figure 5-18)

| PARAMETER                         |                                                            | TEST CONDITIONS                                                    |                                        | V <sub>CC</sub> | MIN          | TYP | MAX | UNIT       |
|-----------------------------------|------------------------------------------------------------|--------------------------------------------------------------------|----------------------------------------|-----------------|--------------|-----|-----|------------|
| f <sub>M</sub>                    | Modulator clock                                            |                                                                    |                                        |                 | 1.024        |     |     | MHz        |
| SINAD                             | Signal-to-noise + distortion ratio for differential inputs | CTSD16GAINx = 1, input ADx+ and ADx- (differential)                | f <sub>IN</sub> = 50 Hz <sup>(1)</sup> | 3 V             | 84           | 87  |     | dB         |
|                                   |                                                            | CTSD16GAINx = 2, input ADx+ and ADx- (differential)                |                                        |                 | 86           |     |     |            |
|                                   |                                                            | CTSD16GAINx = 4, input ADx+ and ADx- (differential)                |                                        |                 | 85           |     |     |            |
|                                   |                                                            | CTSD16GAINx = 8, input ADx+ and ADx- (differential)                |                                        |                 | 82           |     |     |            |
|                                   |                                                            | CTSD16GAINx = 16, input ADx+ and ADx- (differential)               |                                        |                 | 77           |     |     |            |
| SINAD                             | Signal-to-noise + distortion ratio for single-ended input  | CTSD16GAINx = 1, input Ax (single-ended)                           | f <sub>IN</sub> = 50 Hz <sup>(1)</sup> | 3 V             | 83           |     |     | dB         |
|                                   |                                                            | CTSD16GAINx = 2, input Ax (single-ended)                           |                                        |                 | 82           |     |     |            |
|                                   |                                                            | CTSD16GAINx = 4, input Ax (single-ended)                           |                                        |                 | 78           |     |     |            |
|                                   |                                                            | CTSD16GAINx = 8, input Ax (single-ended)                           |                                        |                 | 72           |     |     |            |
|                                   |                                                            | CTSD16GAINx = 16, input Ax (single-ended)                          |                                        |                 | 66           |     |     |            |
| G                                 | Nominal gain                                               | CTSD16GAINx = 1                                                    |                                        | 3 V             | 1            |     |     |            |
|                                   |                                                            | CTSD16GAINx = 2                                                    |                                        |                 | 2            |     |     |            |
|                                   |                                                            | CTSD16GAINx = 4                                                    |                                        |                 | 4            |     |     |            |
|                                   |                                                            | CTSD16GAINx = 8                                                    |                                        |                 | 8            |     |     |            |
|                                   |                                                            | CTSD16GAINx = 16                                                   |                                        |                 | 16           |     |     |            |
| E <sub>G</sub>                    | Gain error                                                 | CTSD16GAINx: 1, 8, or 16 with external reference (1.2 V)           |                                        | 3 V             | –1%      +1% |     |     |            |
| ΔE <sub>G</sub> /ΔT               | Gain error temperature coefficient, internal reference     | CTSD16GAINx: 1, 8, or 16                                           |                                        | 3 V             | 3      50    |     |     | ppm/°C     |
| ΔE <sub>G</sub> /ΔT               | Gain error temperature coefficient, external reference     | CTSD16GAIN: 1, 8, or 16 with external reference (1.2 V)            |                                        | 3 V             | 4      15    |     |     | ppm/°C     |
| ΔE <sub>G</sub> /ΔV <sub>CC</sub> | Gain error vs VCC                                          | CTSD16GAINx: 1, 8, or 16                                           |                                        |                 | 0.02         |     |     | %/V        |
| E <sub>OS</sub>                   | Offset error                                               | CTSD16GAINx = 1                                                    |                                        | 3 V             | ±4.1         |     |     | mV         |
|                                   |                                                            | CTSD16GAINx = 16                                                   |                                        |                 | ±3.4         |     |     |            |
| ΔEOS/ΔT                           | Offset error temperature coefficient                       | CTSD16GAINx = 1, 16                                                |                                        | 3 V             | ±1      ±10  |     |     | ppm FSR/°C |
| ΔEOS/ΔV <sub>CC</sub>             | Offset error vs VCC                                        | CTSD16GAINx = 1, 16                                                |                                        | 3 V             | 11           |     |     | μV/V       |
| CMRR, 50Hz                        | Common-mode rejection ratio at 50 Hz                       | CTSD16GAINx = 1, V <sub>ID</sub> = 928 mV, f <sub>IN</sub> = 50 Hz |                                        | 3 V             | 78           |     |     | dB         |
|                                   |                                                            | CTSD16GAINx = 16, V <sub>ID</sub> = 58 mV, f <sub>IN</sub> = 50 Hz |                                        |                 | 80           |     |     |            |

(1) The following voltages were applied to the CTSD16 inputs:

$$V_{I,A+}(t) = 0 \text{ V} + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$$

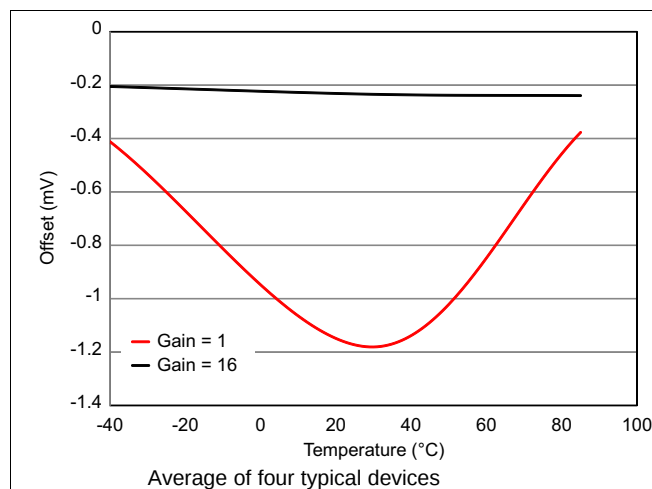
$$V_{I,A-}(t) = 0 \text{ V} - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$$

resulting in a differential voltage of V<sub>ID</sub> = V<sub>IN,A+</sub>(t) – V<sub>IN,A-</sub>(t) = V<sub>PP</sub> × sin(2π × f<sub>IN</sub> × t) with V<sub>PP</sub> being selected as the maximum value allowed for a given range (according to CTSD16 input range).

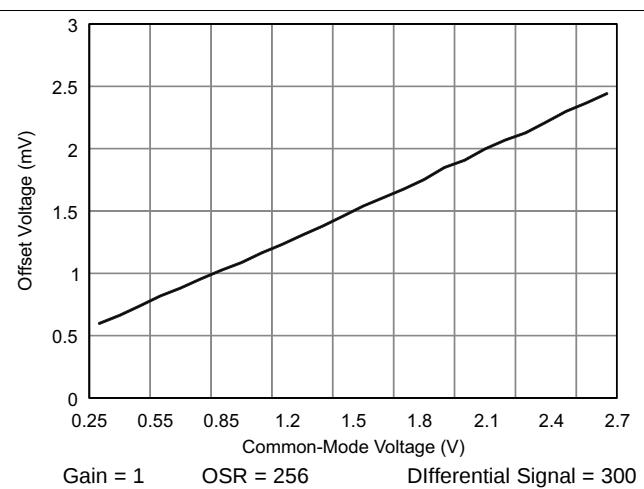
**Table 5-33. CTSD16, Performance (continued)**

CTSD16OSRx = 256, CTSD16REFS = 1 (see [Figure 5-16](#), [Figure 5-17](#), and [Figure 5-18](#))

| PARAMETER                                    | TEST CONDITIONS                                                                                                                                                                                   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| AC PSRR      AC power supply rejection ratio | CTSD16GAINx: 1, V <sub>CC</sub> = 3 V ±50 mV × sin(2π × f <sub>VCC</sub> × t), f <sub>VCC</sub> = 50 Hz, Inputs grounded (no analog signal applied)                                               |                 |     | 95  |     | dB   |
|                                              | CTSD16GAINx: 8, V <sub>CC</sub> = 3 V ±50 mV × sin(2π × f <sub>VCC</sub> × t), f <sub>VCC</sub> = 50 Hz, Inputs grounded (no analog signal applied)                                               |                 |     | 105 |     |      |
|                                              | CTSD16GAINx: 16, V <sub>CC</sub> = 3 V ±50 mV × sin(2π × f <sub>VCC</sub> × t), f <sub>VCC</sub> = 50 Hz, Inputs grounded (no analog signal applied)                                              |                 |     | 105 |     |      |
| DC PSRR      DC power supply rejection ratio | CTSD16GAINx: (1, 8, 16), V <sub>CC</sub> = 2.2 V to 3.6 V, (PSRR [dB] = -20 log(dVout/dVcc) with dVout observed as change in the digital conversion result; assumed to be dominated by reference) |                 |     | 90  |     | dB   |



**Figure 5-16. CTSD16 Offset Voltage vs Temperature**



**Figure 5-17. CTSD16 Typical Offset Voltage vs Common-Mode Voltage**



**Figure 5-18. SINAD Performance vs OSR**

Table 5-34 lists the characteristics of the built-in  $V_{CC}$  sense.

**Table 5-34. Built-in  $V_{CC}$  Sense**

| PARAMETER                        | TEST CONDITIONS                 | MIN                         | TYP           | MAX                         | UNIT |
|----------------------------------|---------------------------------|-----------------------------|---------------|-----------------------------|------|
| $V_{CC,sense}$ $AV_{CC}$ divider | CTSD16ON = 1, CTSD16INCH = 0111 | $0.95 \times (AV_{CC} / 2)$ | $AV_{CC} / 2$ | $1.05 \times (AV_{CC} / 2)$ | V    |

Table 5-35 lists the characteristics of the temperature sensor.

**Table 5-35. Temperature Sensor**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                         | TEST CONDITIONS                                                          | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------------|--------------------------------------------------------------------------|-----|-----|-----|------|
| $V_{sensor}$ Temperature sensor output voltage <sup>(1) (2)</sup> | CTSD16ON = 1, CTSD16INCH = 110, $V_{CC} = 3$ V, $T_A = 30^\circ\text{C}$ |     | 800 |     | mV   |
| $I_{sensor}$ Temperature sensor quiescent current consumption     | CTSD16ON = 1, CTSD16INCH = 110, $T_A = 85^\circ\text{C}$                 |     | 2   |     | uA   |

- (1) The temperature sensor offset can be as much as  $\pm 30^\circ\text{C}$ . TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for  $30^\circ\text{C} \pm 3^\circ\text{C}$  and  $85^\circ\text{C} \pm 3^\circ\text{C}$  for each of the available reference voltage levels. The sensor voltage can be computed as  $V_{SENSE} = TC_{SENSOR} * (\text{Temperature}, ^\circ\text{C}) + V_{SENSOR}$ , where  $TC_{SENSOR}$  and  $V_{SENSOR}$  can be computed from the calibration values for higher accuracy.

## 5.8.12 REF

Table 5-36 lists the characteristics of the REF and REFBG built-in reference.

**Table 5-36. REF and REFBG, Built-In Reference**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                      | TEST CONDITIONS                                                                                             | MIN   | TYP  | MAX   | UNIT   |
|------------------------|----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------|------|-------|--------|
| I <sub>REFBG</sub>     | Operating supply current into AVCC terminal <sup>(1)</sup>           | V <sub>CC</sub> = 3.0 V, REFON = 1 and REFOUT = 1                                                           |       | 110  | 130   | μA     |
| V <sub>REFBG</sub>     | Bandgap output voltage calibrated                                    | V <sub>CC</sub> = 3.0 V,<br>V <sub>eREF+</sub> ≤ 1.5 V if used                                              | 1.146 | 1.16 | 1.174 | V      |
| I <sub>REF</sub>       | Operating supply current into AVCC terminal <sup>(1)</sup>           | V <sub>CC</sub> = 3.0 V, REFON = 1                                                                          |       | 15   | 20    | μA     |
| V <sub>REF</sub>       | Positive built-in reference voltage output                           | REFVSEL = {2} for 2.5 V, REFON = 1                                                                          |       | 2.5  | ±1%   | V      |
|                        |                                                                      | REFVSEL = {1} for 2.0 V, REFON = 1                                                                          |       | 2.0  | ±1%   |        |
|                        |                                                                      | REFVSEL = {0} for 1.5 V, REFON = 1                                                                          |       | 1.5  | ±1%   |        |
| AV <sub>CC(min)</sub>  | AVCC minimum voltage, Positive built-in reference active             | DAC12SREFx = 0, REFVSEL = {0} for 1.5 V                                                                     | 2.2   |      |       | V      |
|                        |                                                                      | DAC12SREFx = 0, REFVSEL = {1} for 2 V                                                                       | 2.3   |      |       |        |
|                        |                                                                      | DAC12SREFx = 0, REFVSEL = {2} for 2.5 V                                                                     | 2.8   |      |       |        |
| PSRR_DC                | Power supply rejection ratio (DC)                                    | V <sub>CC</sub> = 2.2 V to 3.6 V, T <sub>A</sub> = 25°C                                                     |       | 50   |       | μV/V   |
| PSRR_AC                | Power supply rejection ratio (AC)                                    | V <sub>CC</sub> = 2.2 V to 3.6 V, T <sub>A</sub> = 25°C,<br>f = 1 kHz, ΔV <sub>pp</sub> = 100 mV            |       | 1.5  |       | mV/V   |
| TC <sub>REF+</sub>     | Bandgap reference temperature coefficient <sup>(2)</sup>             | I <sub>VREF+</sub> = 0 A                                                                                    |       | 15   | 50    | ppm/°C |
| t <sub>SETTLE</sub>    | Settling time of V <sub>REFBG</sub> reference voltage <sup>(3)</sup> | AV <sub>CC</sub> = AV <sub>CC (min)</sub> through AV <sub>CC(max)</sub> ,<br>REFON = 0 → 1                  |       |      | 120   | μs     |
| C <sub>VREFBG</sub>    | Capacitance at VREFBG terminal                                       | See <sup>(4)</sup>                                                                                          |       |      | 1     | nF     |
| I <sub>LOAD</sub>      | VREFBG maximum load current                                          | REFOUT = REFON = 1                                                                                          |       |      | 1     | mA     |
| I <sub>L(VREFBG)</sub> | Load-current regulation, VREFBG terminal <sup>(5)</sup>              | I <sub>(VREF+)</sub> = +1 mA or −1 mA,<br>AV <sub>CC</sub> = AV <sub>CC (min)</sub> ,<br>REFON = REFOUT = 1 |       |      | 3.5   | mV/mA  |

(1) The internal reference current is supplied from terminal AVCC. Consumption is independent of the CTSD16ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

(2) Calculated using the box method:  $(\text{MAX}(-40^\circ\text{C to } 85^\circ\text{C}) - \text{MIN}(-40^\circ\text{C to } 85^\circ\text{C})) / \text{MIN}(-40^\circ\text{C to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$ .

(3) The condition is that the error in a conversion started after  $t_{REFON}$  is less than  $\pm 0.5\text{ LSB}$ .

(4) There is no capacitance required on VREFBG if the reference voltage is not used externally. However, TI recommends a capacitance close to the maximum value to reduce any reference voltage noise.

(5) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB traces or other external factors.

### 5.8.13 DAC

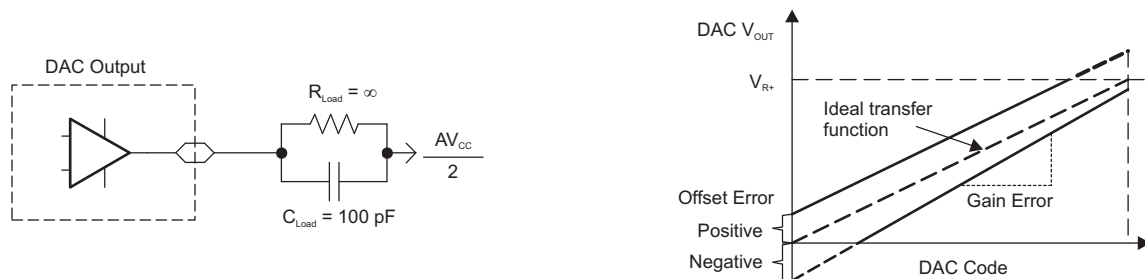
Table 5-37 lists the supply specifications of the DAC.

**Table 5-37. 12-Bit DAC, Supply Specifications**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                             | TEST CONDITIONS                                                                                | V <sub>CC</sub>   | MIN | TYP | MAX  | UNIT |
|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------|-------------------|-----|-----|------|------|
| AV <sub>CC</sub> Analog supply voltage                                | AV <sub>CC</sub> = DV <sub>CC</sub> , AV <sub>SS</sub> = DV <sub>SS</sub> = 0 V                |                   | 2.2 |     | 3.6  | V    |
| I <sub>DD</sub> Supply current, single DAC channel <sup>(1) (2)</sup> | DAC12AMPx = 2, DAC12IR = 0,<br>DAC12OG = 1,<br>DAC12_xDAT = 0800h,<br>VeREF+ = VREFBG = 1.16 V | 3 V               |     | 65  | 110  | μA   |
|                                                                       | DAC12AMPx = 2, DAC12IR = 1,<br>DAC12_xDAT = 0800h,<br>VeREF+ = AV <sub>CC</sub>                | 2.2 V to<br>3.6 V |     | 125 | 165  |      |
|                                                                       | DAC12AMPx = 5, DAC12IR = 1,<br>DAC12_xDAT = 0800h,<br>VeREF+ = AV <sub>CC</sub>                |                   |     | 250 | 350  |      |
|                                                                       | DAC12AMPx = 7, DAC12IR = 1,<br>DAC12_xDAT = 0800h,<br>VeREF+ = AV <sub>CC</sub>                |                   |     | 750 | 1100 |      |
| PSRR Power supply rejection ratio <sup>(3) (4)</sup>                  | DAC12_xDAT = 800h,<br>VeREF+ = 1.16 V or 1.5 V,<br>ΔAV <sub>CC</sub> = 100 mV                  | 2.2 V to<br>3.6 V |     | 70  |      | dB   |
|                                                                       | DAC12_xDAT = 800h,<br>VeREF+ = 1.16 V or 2.5 V<br>ΔAV <sub>CC</sub> = 100 mV                   | 3 V               |     | 70  |      |      |

- (1) No load at the output pin, DAC12\_0 or DAC12\_1, assuming that the control bits for the shared pins are set properly.  
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications Table 5-40.  
(3) PSRR = 20 log (ΔAV<sub>CC</sub> / ΔV<sub>DAC12\_xOUT</sub>)  
(4) The internal reference is not used.



**Figure 5-19. Linearity Test Load Conditions, Gain and Offset Definition**

Table 5-38 lists the linearity specifications of the DAC.

**Table 5-38. 12-Bit DAC, Linearity Specifications**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-19)

| PARAMETER                         |                                                     | TEST CONDITIONS                                         |                                                               | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT          |
|-----------------------------------|-----------------------------------------------------|---------------------------------------------------------|---------------------------------------------------------------|-----------------|------|-----|-----|---------------|
| Resolution                        |                                                     | 12-bit monotonic                                        |                                                               |                 | 12   |     |     | bits          |
| INL                               | Integral nonlinearity <sup>(1)</sup>                | V <sub>eREF+</sub> = 1.16 V, DAC12AMPx = 7, DAC12IR = 1 |                                                               | 2.2 V, 3 V      | ±2   |     |     | LSB           |
|                                   |                                                     | V <sub>eREF+</sub> = 2.5 V, DAC12AMPx = 7, DAC12IR = 1  |                                                               | 2.2 V, 3 V      | ±2   |     |     |               |
| DNL                               | Differential nonlinearity <sup>(1)</sup>            | V <sub>eREF+</sub> = 1.16 V, DAC12AMPx = 7, DAC12IR = 1 |                                                               | 2.2 V, 3 V      | ±0.4 |     |     | LSB           |
|                                   |                                                     | V <sub>eREF+</sub> = 2.5 V, DAC12AMPx = 7, DAC12IR = 1  |                                                               | 2.2 V, 3 V      | ±0.4 |     |     |               |
| E <sub>O</sub>                    | Offset voltage                                      | Without calibration <sup>(1) (2)</sup>                  | V <sub>eREF+</sub> = 1.16 V,<br>DAC12AMPx = 7,<br>DAC12IR = 1 | 2.2 V, 3 V      | ±21  |     |     | mV            |
|                                   |                                                     |                                                         | V <sub>eREF+</sub> = 2.5 V,<br>DAC12AMPx = 7,<br>DAC12IR = 1  | 2.2 V, 3 V      | ±21  |     |     |               |
|                                   |                                                     | With calibration <sup>(1) (2)</sup>                     | V <sub>eREF+</sub> = 1.16 V,<br>DAC12AMPx = 7,<br>DAC12IR = 1 | 2.2 V, 3 V      | ±1.5 |     |     |               |
|                                   |                                                     |                                                         | V <sub>eREF+</sub> = 2.5 V,<br>DAC12AMPx = 7,<br>DAC12IR = 1  | 2.2 V, 3 V      | ±1.5 |     |     |               |
| d <sub>E(O)</sub> /d <sub>T</sub> | Offset error temperature coefficient <sup>(1)</sup> | With calibration                                        |                                                               | 2.2 V, 3 V      | ±10  |     |     | μV/°C         |
| E <sub>G</sub>                    | Gain error                                          | V <sub>eREF+</sub> = 1.16 V                             |                                                               | 2.2 V, 3 V      | ±2.5 |     |     | %FSR          |
|                                   |                                                     | V <sub>eREF+</sub> = 2.5 V                              |                                                               | 2.2 V, 3 V      | ±2.5 |     |     |               |
| d <sub>E(G)</sub> /d <sub>T</sub> | Gain temperature coefficient <sup>(1)</sup>         |                                                         |                                                               | 2.2 V, 3 V      | 10   |     |     | ppm of FSR/°C |
| t <sub>Offset_Cal</sub>           | Time for offset calibration <sup>(3)</sup>          | DAC12AMPx = 2                                           |                                                               | 2.2 V, 3 V      | 165  |     |     | ms            |
|                                   |                                                     | DAC12AMPx = 3, 5                                        |                                                               |                 | 66   |     |     |               |
|                                   |                                                     | DAC12AMPx = 4, 6, 7                                     |                                                               |                 | 16.5 |     |     |               |

- (1) Parameters calculated from the best-fit curve from 0x0F to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation:  $y = a + bx$ .  $V_{DAC12\_XOUT} = E_O + (1 + E_G) \times (V_{REF+}/4095) \times DAC12\_xDAT$ , DAC12IR = 1.
- (2) The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
- (3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends configuring the DAC12 module before initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

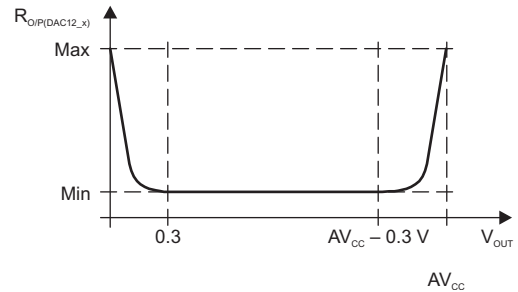
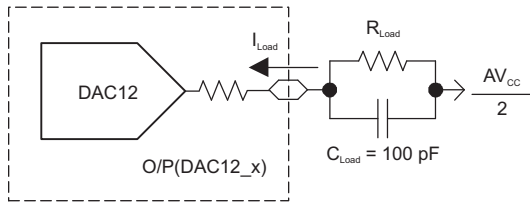
Table 5-39 lists the output specifications of the DAC.

**Table 5-39. 12-Bit DAC, Output Specifications**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                   | TEST CONDITIONS                                                                                                        | V <sub>CC</sub> | MIN                     | TYP | MAX              | UNIT |
|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------|-------------------------|-----|------------------|------|
| V <sub>O</sub><br><br>Output voltage range <sup>(1)</sup> (see Figure 5-20) | No load, V <sub>eREF+</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0h, DAC12IR = 1,<br>DAC12AMPx = 7                     | 2.2 V, 3.6 V    | 0                       |     | 0.005            | V    |
|                                                                             | No load, V <sub>eREF+</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0FFFh, DAC12IR = 1,<br>DAC12AMPx = 7                  |                 | AV <sub>CC</sub> – 0.05 |     | AV <sub>CC</sub> |      |
|                                                                             | R <sub>Load</sub> = 3 kΩ, V <sub>eREF+</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0h, DAC12IR = 1,<br>DAC12AMPx = 7    |                 | 0                       |     | 0.1              |      |
|                                                                             | R <sub>Load</sub> = 3 kΩ, V <sub>eREF+</sub> = AV <sub>CC</sub> ,<br>DAC12_xDAT = 0FFFh, DAC12IR = 1,<br>DAC12AMPx = 7 |                 | AV <sub>CC</sub> – 0.13 |     | AV <sub>CC</sub> |      |
| C <sub>L(DAC12)</sub>                                                       | Maximum DAC12 load capacitance                                                                                         | 2.2 V, 3.6 V    |                         |     | 100              | pF   |
| I <sub>L(DAC12)</sub>                                                       | DAC12AMPx = 2, DAC12_xDAT = 0FFFh,<br>V <sub>O/P(DAC12)</sub> > AV <sub>CC</sub> – 0.3                                 | 2.2 V, 3.6 V    | –1                      |     |                  | mA   |
|                                                                             | DAC12AMPx = 2, DAC12_xDAT = 0h,<br>V <sub>O/P(DAC12)</sub> < 0.3 V                                                     |                 |                         |     | 1                |      |
| R <sub>O/P(DAC12)</sub>                                                     | R <sub>Load</sub> = 3 kΩ, V <sub>O/P(DAC12)</sub> < 0.3 V,<br>DAC12AMPx = 2, DAC12_xDAT = 0h                           | 2.2 V, 3.6 V    |                         | 150 | 250              | Ω    |
|                                                                             | R <sub>Load</sub> = 3 kΩ, V <sub>O/P(DAC12)</sub> > AV <sub>CC</sub> – 0.3 V,<br>DAC12_xDAT = 0FFFh                    |                 |                         | 150 | 250              |      |
|                                                                             | R <sub>Load</sub> = 3 kΩ,<br>0.3 V ≤ V <sub>O/P(DAC12)</sub> ≤ AV <sub>CC</sub> – 0.3 V                                |                 |                         |     | 6                |      |

(1) Data is valid after the offset calibration of the output amplifier.



**Figure 5-20. DAC12\_x Output Resistance Tests**

Table 5-40 lists the reference input specifications of the DAC.

**Table 5-40. 12-Bit DAC, Reference Input Specifications**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                   | TEST CONDITIONS                                                                                        | V <sub>CC</sub> | MIN                  | TYP | MAX                    | UNIT |
|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|-----------------|----------------------|-----|------------------------|------|
| V <sub>REF+</sub> Reference input voltage range                             | DAC12IR = 0 <sup>(1)</sup> <sup>(2)</sup>                                                              | 2.2 V to 3.6 V  | AV <sub>CC</sub> / 3 |     | AV <sub>CC</sub> + 0.2 | V    |
|                                                                             | DAC12IR = 1 <sup>(3)</sup> <sup>(4)</sup>                                                              |                 | AV <sub>CC</sub>     |     | AV <sub>CC</sub> + 0.2 |      |
| R <sub>i(VREFB)</sub> ,<br>R <sub>i(VREF+)</sub> Reference input resistance | DAC12_0 DAC12IR =<br>DAC12_1 DAC12IR = 0                                                               | 2.2 V, 3 V      | 20                   |     |                        | MΩ   |
|                                                                             | DAC12_0 DAC12IR = 1,<br>DAC12_1 DAC12IR = 0                                                            |                 | 52                   |     |                        | kΩ   |
|                                                                             | DAC12_0 DAC12IR = 0,<br>DAC12_1 DAC12IR = 1                                                            |                 | 52                   |     |                        |      |
|                                                                             | DAC12_0 DAC12IR =<br>DAC12_1 DAC12IR = 1,<br>DAC12_0 DAC12SREFx =<br>DAC12_1 DAC12SREFx <sup>(5)</sup> |                 | 26                   |     |                        |      |

- (1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV<sub>CC</sub>).  
(2) The maximum voltage applied at reference input voltage terminal V<sub>REF+</sub> = [AV<sub>CC</sub> – V<sub>E(O)</sub>] / [3 × (1 + E<sub>G</sub>)].  
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV<sub>CC</sub>).  
(4) The maximum voltage applied at reference input voltage terminal V<sub>REF+</sub> = [AV<sub>CC</sub> – V<sub>E(O)</sub>] / (1 + E<sub>G</sub>).  
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel and reduce the reference input resistance.

Table 5-41 and Table 5-42 list the dynamic specifications of the DAC.

**Table 5-41. 12-Bit DAC, Dynamic Specifications**

V<sub>REF</sub> = V<sub>CC</sub>, DAC12IR = 1 (see Figure 5-21 and Figure 5-22), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                       | TEST CONDITIONS                                                                            | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|-------------------------------------------------|--------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|
| t <sub>ON</sub> DAC12 on time                   | DAC12_xDAT = 800h,<br>Error <sub>V(O)</sub> < ±0.5 LSB <sup>(1)</sup><br>(see Figure 5-21) | 2.2 V, 3 V      | 60   |     | 120  | μs   |
|                                                 |                                                                                            |                 | 15   |     | 30   |      |
|                                                 |                                                                                            |                 | 6    |     | 12   |      |
| t <sub>S(FS)</sub> Settling time, full scale    | DAC12_xDAT =<br>80h → F7Fh → 80h                                                           | 2.2 V, 3 V      | 100  |     | 200  | μs   |
|                                                 |                                                                                            |                 | 40   |     | 80   |      |
|                                                 |                                                                                            |                 | 15   |     | 30   |      |
| t <sub>S(C-C)</sub> Settling time, code to code | DAC12_xDAT =<br>3F8h → 408h → 3F8h,<br>BF8h → C08h → BF8h                                  | 2.2 V, 3 V      | 5    |     |      | μs   |
|                                                 |                                                                                            |                 | 2    |     |      |      |
|                                                 |                                                                                            |                 | 1    |     |      |      |
| SR Slew rate                                    | DAC12_xDAT =<br>80h → F7Fh → 80h <sup>(2)</sup>                                            | 2.2 V, 3 V      | 0.05 |     | 0.35 | V/μs |
|                                                 |                                                                                            |                 | 0.35 |     | 1.10 |      |
|                                                 |                                                                                            |                 | 1.50 |     | 5.20 |      |
| Glitch energy                                   | DAC12_xDAT =<br>800h → 7FFh → 800h                                                         | 2.2 V, 3 V      | 35   |     |      | nV-s |

- (1) R<sub>Load</sub> and C<sub>Load</sub> connected to AV<sub>SS</sub> (not AV<sub>CC</sub>/2) in Figure 5-21.  
(2) Slew rate applies to output voltage steps ≥ 200 mV.

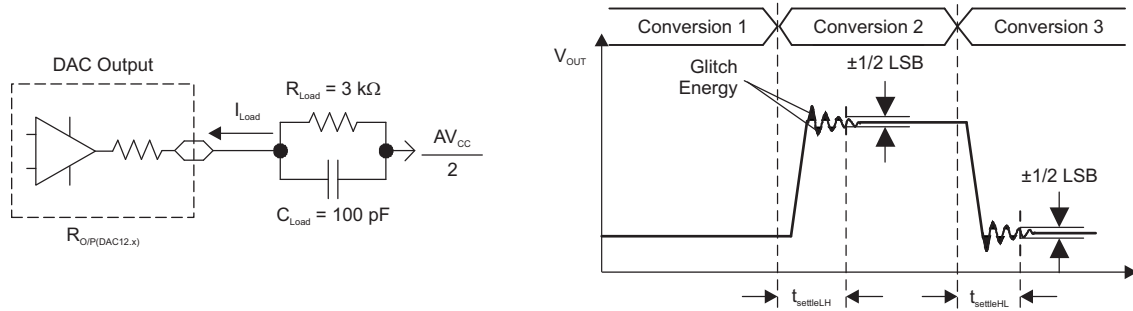


Figure 5-21. Settling Time and Glitch Energy Testing

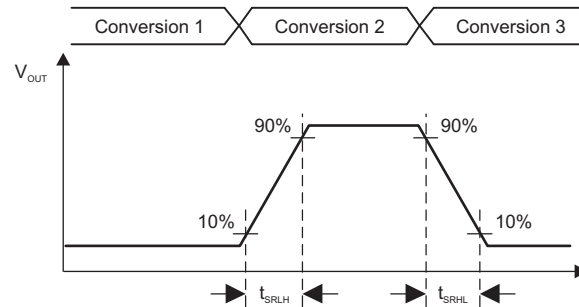


Figure 5-22. Slew Rate Testing

Table 5-42. 12-Bit DAC, Dynamic Specifications (Continued)

over recommended ranges of supply voltage and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                                                                        | TEST CONDITIONS                                                                                                                                  | $V_{CC}$   | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|-----|-----|------|
| $BW_{-3dB}$<br>3-dB bandwidth,<br>$V_{DC} = 1.5\text{ V}$ ,<br>$V_{AC} = 0.1\text{ V}_{PP}$<br>(see Figure 5-23) | DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2,<br>DAC12IR = 1, DAC12_xDAT = 800h                                                                         | 2.2 V, 3 V | 40  |     |     | kHz  |
|                                                                                                                  | DAC12AMPx = {5, 6}, DAC12SREFx = 2,<br>DAC12IR = 1, DAC12_xDAT = 800h                                                                            |            | 180 |     |     |      |
|                                                                                                                  | DAC12AMPx = 7, DAC12SREFx = 2,<br>DAC12IR = 1, DAC12_xDAT = 800h                                                                                 |            | 550 |     |     |      |
| Channel-to-channel crosstalk <sup>(1)</sup><br>(see Figure 5-24)                                                 | DAC12_0DAT = 800h, No load,<br>DAC12_1DAT = 80h ↔ F7Fh, $R_{Load} = 3\text{ k}\Omega$ ,<br>$f_{DAC12\_1OUT} = 10\text{ kHz}$ at 50/50 duty cycle | 2.2 V, 3 V |     | –80 |     | dB   |
|                                                                                                                  | DAC12_0DAT = 80h ↔ F7Fh, $R_{Load} = 3\text{ k}\Omega$ ,<br>DAC12_1DAT = 800h, No load,<br>$f_{DAC12\_0OUT} = 10\text{ kHz}$ at 50/50 duty cycle |            |     | –80 |     |      |

(1)  $R_{Load} = 3\text{ k}\Omega$ ,  $C_{Load} = 100\text{ pF}$

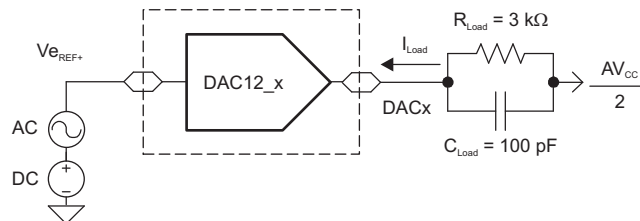
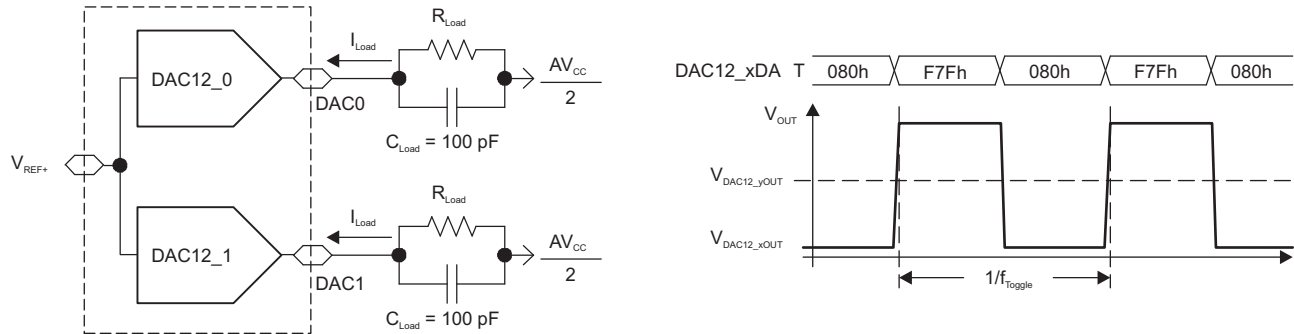


Figure 5-23. Test Conditions for 3-dB Bandwidth Specification


**Figure 5-24. Crosstalk Test Conditions**

### 5.8.14 Operational Amplifier

Table 5-43 lists the characteristics of the OA.

**Table 5-43. Operational Amplifier, OA0, OA1, PGA Buffers**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                      | V <sub>CC</sub>                                                                                                                                            | MIN   | TYP                   | MAX                | UNIT   |
|-------------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----------------------|--------------------|--------|
| V <sub>CC</sub>         | Analog supply voltage                                | AV <sub>CC</sub> = DV <sub>CC</sub> , AV <sub>SS</sub> = DV <sub>SS</sub> = 0 V                                                                            | 2.2   |                       | 3.6                | V      |
| C <sub>CPCAP</sub>      | External charge pump capacitor to AV <sub>SS</sub> . | Required when charge pump is enabled                                                                                                                       | 20    | 22                    | 24                 | nF     |
| I <sub>CP_PEAK</sub>    | Charge pump peak current                             | OARRI = 0h to 1h, I <sub>CP_LOAD</sub> = 0 μA                                                                                                              |       | 1.6                   |                    | mA     |
| I <sub>CP</sub>         | Charge pump average current                          | OARRI = 1h, I <sub>CP_LOAD</sub> = 100 μA                                                                                                                  |       | 570 <sup>(1)</sup>    | 710 <sup>(1)</sup> | μA     |
| t <sub>CP_EN_fast</sub> | Charge pump enable time fast                         | OARRI = 0h to 1h, I <sub>CP_LOAD</sub> = 0 μA, AFE biases previously enabled and settled which can be done with REFON=1 or other modules requesting REFON. |       | 50                    |                    | μs     |
| t <sub>CP_EN_slow</sub> | Charge pump enable time slow                         | OARRI = 0h to 1h, I <sub>CP_LOAD</sub> = 0 μA, Includes AFE bias settling                                                                                  |       | 75                    |                    | μs     |
| I <sub>OA</sub>         | Supply current, per opamp                            | I <sub>O</sub> = 0 mA, OARRI = 0h (charge pump disabled)                                                                                                   |       | 105 <sup>(1)</sup>    | 130 <sup>(1)</sup> | μA     |
| V <sub>OS</sub>         | Input offset voltage                                 | Noninverting, unity gain                                                                                                                                   |       | ±2                    |                    | mV     |
| dV <sub>OS</sub> /dT    | Input offset voltage temperature drift               | Noninverting, unity gain                                                                                                                                   |       | ±1                    |                    | μV/°C  |
| dV <sub>OS</sub> /dV    | Input offset voltage voltage drift                   | Noninverting, unity gain                                                                                                                                   |       | ±3                    |                    | μV/V   |
| C <sub>in</sub>         | Input capacitance                                    | Differential                                                                                                                                               |       | 4                     |                    | pF     |
|                         |                                                      | Common mode                                                                                                                                                |       | 6                     |                    | pF     |
| PSRR <sub>DC</sub>      | Power supply rejection ratio, DC                     | Noninverting, unity gain, V <sub>INP</sub> = positive input of OA = 1 V                                                                                    |       | 50                    |                    | μV/V   |
| V <sub>CM</sub>         | Common mode voltage range <sup>(2)</sup>             | OARRI = 0h, Noninverting, unity gain                                                                                                                       | 0.1   | V <sub>CC</sub> - 1.0 |                    | V      |
|                         |                                                      | OARRI = 1h, Noninverting, unity gain                                                                                                                       | 0.1   | V <sub>CC</sub> - 0.1 |                    | V      |
| CMRR <sub>DC</sub>      | Common mode rejection ratio, DC                      | Over common-mode voltage range                                                                                                                             |       | 110                   |                    | dB     |
| e <sub>n</sub>          | Input voltage noise density                          | f = 100 Hz, OARRI = 0h or 1h                                                                                                                               | 3.0 V | 90                    |                    | nV/√Hz |
|                         |                                                      | f = 50 kHz, OARRI = 0h or 1h                                                                                                                               | 3.0 V | 25                    |                    |        |

(1) See Table 5-44 to calculate total current from OA for different use cases.

(2) The common-mode input range is measured with the OA in a unity-gain source-follower configuration. The input signal is swept from 0 V to V<sub>CC</sub>, and the output of the OA is monitored. The minimum and maximum values represent when the input and output differ more than 10 mV, not including the offset, V<sub>OS</sub>.

**Table 5-43. Operational Amplifier, OA0, OA1, PGA Buffers (continued)**

over operating free-air temperature range (unless otherwise noted)

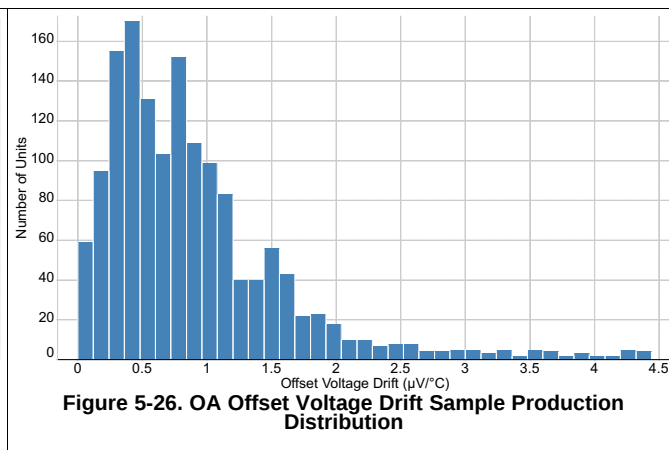
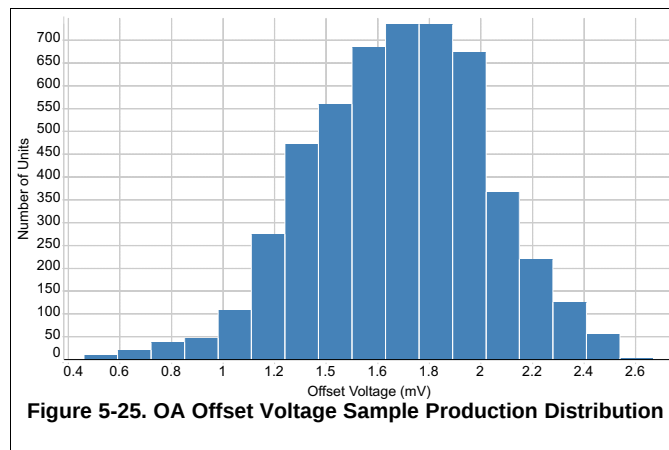
| PARAMETER            |                                | TEST CONDITIONS                                                                                                                                                                  | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|----------------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| A <sub>OL</sub>      | Open-loop voltage gain, DC     |                                                                                                                                                                                  |                 |     | 95  |     | dB   |
| GBW                  | Gain-bandwidth product         | C <sub>L</sub> = 100 pF, OAM = 1h                                                                                                                                                |                 |     | 800 |     | kHz  |
| SR                   | Slew rate                      | Noninverting, unity gain, C <sub>L</sub> = 100 pF, OAM = 1h                                                                                                                      |                 |     | 0.4 |     | V/μs |
| t <sub>SETTLE</sub>  | Settling time                  | Noninverting, unity gain, 2.0-V step, 0.1%, OAM = 1h                                                                                                                             | 3.0 V           |     | 5.3 |     | μs   |
| V <sub>O</sub>       | Voltage output swing from rail | –250 μA ≤ I <sub>O</sub> ≤ 250 μA, Noninverting, unity gain (OAM = 1h)                                                                                                           |                 |     | 5   | 55  | mV   |
| t <sub>EN_FAST</sub> | Enable time fast               | Noninverting, unity gain, OAM = 0h transition to 1h, AFE biases previously enabled and settled which can be done with REFON = 1 or other modules requesting REFON <sup>(3)</sup> |                 |     | 3   | 7   | μs   |
| t <sub>EN_SLOW</sub> | Enable time slow               | Noninverting, unity gain, OARRI = 0h transition to 1h, OAM = 0h transition to 1h, Includes AFE bias and charge pump settling <sup>(3)</sup>                                      |                 |     | 190 | 225 | μs   |
| t <sub>DIS</sub>     | Disable time                   |                                                                                                                                                                                  |                 |     | 0.4 |     | μs   |

(3) The AFE bias is used by several modules including the OA charge pump, OA, and CTSD16. Any of these modules will request the AFE bias when enabled. The AFE bias is generated by the REF module, so enabling the REF module also enables the AFE bias.

Table 5-44 explains how to compute the total current, I<sub>TOTAL</sub>, when the OA and associated modules are used. See Table 5-30 for a similar table for the CTSD16. A "yes" means it must be included in computing I<sub>TOTAL</sub>.

As an example, assume that the application uses the CTSD16D in rail-to-rail input mode (CTSD16RRI = 1) with the internal reference (CTSD16REFS = 1) and OA0 and OA1 are enabled in rail-to-rail input modes, OARRI = 1. The total current, I<sub>TOTAL</sub>, would be computed as follows:

$$I_{TOTAL} = I_{CTSD16} + I_{CTSD16CLK} + I_{CP} + I_{REFBG} + 2 \times I_{OA}$$



**Table 5-44. OA, Current Calculation**

| USE CASE NAME                     | USE CASE DETAILS                                                                                                    | I <sub>OA</sub> | I <sub>CTSD16CLK</sub> <sup>(1)</sup> | I <sub>CP</sub> <sup>(2)</sup> | I <sub>REF</sub> <sup>(3)</sup> |
|-----------------------------------|---------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------------------|--------------------------------|---------------------------------|
| OA                                | OARRI = 0                                                                                                           | yes             | no                                    | no                             | yes                             |
| OA with rail-to-rail input        | OARRI = 1                                                                                                           | yes             | yes                                   | yes                            | yes                             |
| Rail-to-rail input up, module off | (CTSD16SC = 0) AND<br>(CTSD16RRI = 1) AND<br>(CTSD16RRIBURST = 0) OR<br>((OARRI = 1 (for any OA))<br>AND (OAM = 0)) | no              | yes                                   | yes                            | yes                             |

- (1) Count this current only once no matter how many modules use it. CTSD16 and the charge pump also use this. This current is listed in [Table 5-29](#).
- (2) Count this current only once no matter how many modules use it. CTSD16 also uses this when rail-to-rail inputs are selected.
- (3) Count this current only once no matter how many modules use it. This current is listed in [Table 5-43](#). If I<sub>REFBG</sub> is used, that includes the I<sub>REF</sub> current.

### 5.8.15 Switches

[Table 5-45](#) lists the characteristics of the ground switches.

**Table 5-45. Ground Switches (GSW0A, GSW0B, GSW1A, GSW1B)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER           |                                         | TEST CONDITIONS                                                    | MIN | TYP   | MAX  | UNIT |
|---------------------|-----------------------------------------|--------------------------------------------------------------------|-----|-------|------|------|
| V <sub>CC</sub>     | Supply voltage                          |                                                                    | 2.2 |       | 3.6  | V    |
| I <sub>LKG</sub>    | Input leakage <sup>(1)</sup>            | T <sub>A</sub> = 0°C to 60°C                                       |     | ±0.25 |      | nA   |
|                     |                                         | T <sub>A</sub> = −40°C to 85°C                                     |     |       | ±50  |      |
| I <sub>IN</sub>     | Input current switch to AVSS            |                                                                    | 0   |       | 100  | μA   |
| R <sub>ON</sub>     | Switch ON resistance with switch closed | I <sub>IN</sub> = 100 μA,<br>T <sub>A</sub> = −40°C to 85°C        |     | 9.5   | 18.5 | Ω    |
| R <sub>OFF</sub>    | Switch OFF resistance with switch open  | T <sub>A</sub> = −40°C to 85°C,<br>Input signal frequency < 100 Hz | 100 |       |      | MΩ   |
| t <sub>ON/OFF</sub> | Enable or disable time                  | T <sub>A</sub> = −40°C to 85°C                                     |     | 0.25  |      | μs   |

- (1) Ground switches are shared with general-purpose I/Os. This leakage includes all leakage seen at the device pin, not only leakage caused by the switch itself.

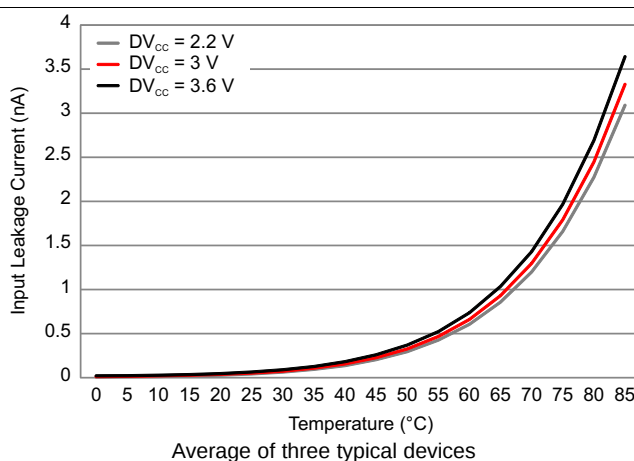
**Figure 5-27. Ground Switch Input Leakage Current vs Temperature**

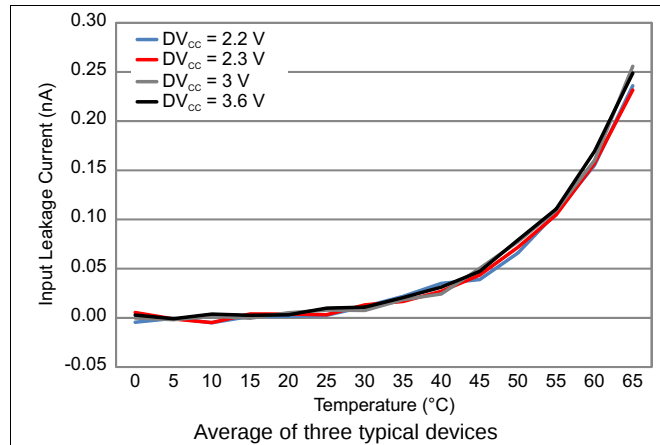
Table 5-46 lists the characteristics of the OA switches.

**Table 5-46. Operational Amplifier Switches**

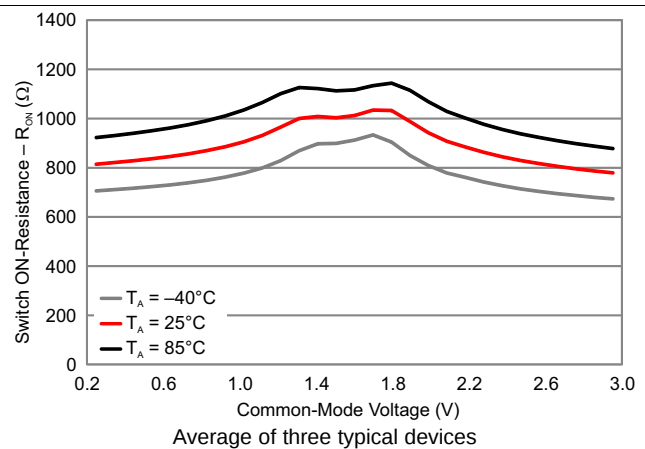
over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                              | TEST CONDITIONS                                                    | MIN | TYP   | MAX | UNIT |
|------------------------------------------------------------------------|--------------------------------------------------------------------|-----|-------|-----|------|
| V <sub>CC</sub> Supply voltage                                         |                                                                    | 2.2 |       | 3.6 | V    |
| I <sub>LKG</sub> Input leakage <sup>(1)</sup>                          | T <sub>A</sub> = 0°C to 60°C                                       |     | ±0.25 |     | nA   |
|                                                                        | T <sub>A</sub> = -40°C to 85°C                                     |     |       | ±50 |      |
| I <sub>IN</sub> Input current through switch                           |                                                                    | 0   |       | 100 | μA   |
| R <sub>ON</sub> Switch ON resistance with switch closed <sup>(2)</sup> | I <sub>IN</sub> = 100 μA,<br>T <sub>A</sub> = -40°C to 85°C        |     | 1     |     | kΩ   |
| R <sub>OFF</sub> Switch OFF resistance with switch open                | T <sub>A</sub> = -40°C to 85°C,<br>Input signal frequency < 100 Hz | 100 |       |     | MΩ   |
| t <sub>ON/OFF</sub> Enable or disable time                             | T <sub>A</sub> = -40°C to 85°C                                     |     | 0.45  |     | μs   |

- (1) This leakage includes all leakage seen at the device pin, not only leakage caused by the switch itself. It assumes a total of five switches present and a shared digital I/O.
- (2) The resistance varies with input voltage range. This resistance represents the peak resistance at the worst case input range (see Figure 5-29).



**Figure 5-28. OA Switch Input Leakage Current vs Temperature**



**Figure 5-29. OA Switch R<sub>ON</sub> vs Common-Mode Voltage**

## 5.8.16 Comparator

Table 5-47 lists the characteristics of the comparator.

**Table 5-47. Comparator\_B**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              | TEST CONDITIONS                                                                   | V <sub>CC</sub>                                               | MIN                                  | TYP                                | MAX                                  | UNIT   |
|------------------------|-----------------------------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------|------------------------------------|--------------------------------------|--------|
| V <sub>CC</sub>        | Supply voltage                                                                    |                                                               | 1.8                                  |                                    | 3.6                                  | V      |
| I <sub>AVCC_COMP</sub> | Comparator operating supply current into AVCC, Excludes reference resistor ladder | 1.8 V                                                         |                                      |                                    | 40                                   | μA     |
|                        |                                                                                   | 2.2 V                                                         |                                      | 30                                 | 50                                   |        |
|                        |                                                                                   | 3 V                                                           |                                      | 40                                 | 65                                   |        |
|                        |                                                                                   | 2.2 V, 3 V                                                    |                                      | 10                                 | 30                                   |        |
|                        |                                                                                   | 2.2 V, 3 V                                                    |                                      | 0.5                                | 1.3                                  |        |
| I <sub>AVCC_REF</sub>  | Quiescent current of resistor ladder into AVCC, Includes REF module current       | 2.2 V, 3 V                                                    |                                      | 10                                 | 22                                   | μA     |
| V <sub>IC</sub>        | Common mode input range                                                           |                                                               | 0                                    |                                    | V <sub>CC</sub> – 1                  | V      |
| V <sub>OFFSET</sub>    | Input offset voltage                                                              | CBPWRMD = 00                                                  |                                      | –20                                | 20                                   | mV     |
|                        |                                                                                   | CBPWRMD = 01 or 10                                            |                                      | –10                                | 10                                   |        |
| C <sub>IN</sub>        | Input capacitance                                                                 |                                                               |                                      | 5                                  |                                      | pF     |
| R <sub>SIN</sub>       | Series input resistance                                                           | On (switch closed)                                            |                                      | 3                                  | 4                                    | kΩ     |
|                        |                                                                                   | Off (switch open)                                             |                                      | 50                                 |                                      | MΩ     |
| t <sub>PD</sub>        | Propagation delay, response time                                                  | CBPWRMD = 00, CBF = 0                                         |                                      |                                    | 450                                  | ns     |
|                        |                                                                                   | CBPWRMD = 01, CBF = 0                                         |                                      |                                    | 600                                  |        |
|                        |                                                                                   | CBPWRMD = 10, CBF = 0                                         |                                      |                                    | 50                                   | μs     |
| t <sub>PD,filter</sub> | Propagation delay with filter active                                              | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 00      | 0.35                                 | 0.6                                | 1.5                                  | μs     |
|                        |                                                                                   | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 01      | 0.6                                  | 1.0                                | 1.8                                  |        |
|                        |                                                                                   | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 10      | 1.0                                  | 1.8                                | 3.4                                  |        |
|                        |                                                                                   | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 11      | 1.8                                  | 3.4                                | 6.5                                  |        |
| t <sub>EN_CMP</sub>    | Comparator enable time                                                            | CBON = 0 → 1, CBPWRMD = 00 or 01                              |                                      | 1                                  | 2                                    | μs     |
|                        |                                                                                   | CBON = 0 → 1, CBPWRMD = 10                                    |                                      |                                    | 100                                  |        |
| t <sub>EN_REF</sub>    | Resistor reference enable time                                                    | CBON = 0 → 1                                                  |                                      | 1.0                                | 1.5                                  | μs     |
| TC <sub>CB_REF</sub>   | Temperature coefficient of V <sub>CB_REF</sub>                                    |                                                               |                                      |                                    | 50                                   | ppm/°C |
| V <sub>CB_REF</sub>    | Reference voltage for a given tap                                                 | V <sub>IN</sub> = reference into resistor ladder, n = 0 to 31 | $\frac{V_{IN} \times (n + 0.5)}{32}$ | $\frac{V_{IN} \times (n + 1)}{32}$ | $\frac{V_{IN} \times (n + 1.5)}{32}$ | V      |

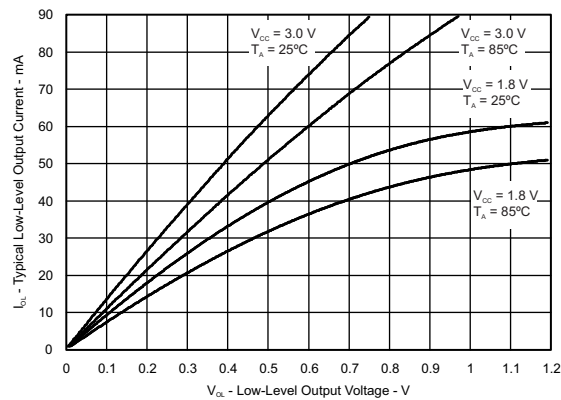
## 5.8.17 USB

Table 5-48 lists the characteristics of PU.0 and PU.1.

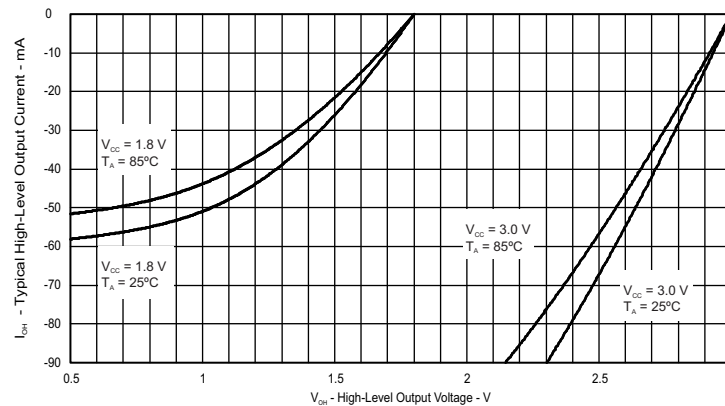
**Table 5-48. Ports PU.0 and PU.1**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

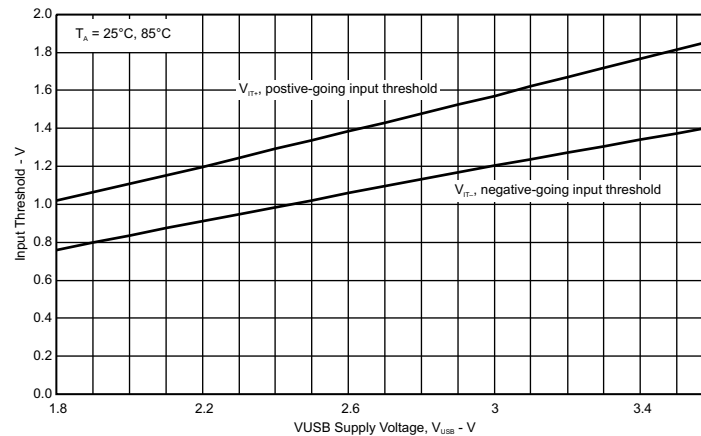
| PARAMETER                                            | TEST CONDITIONS                                              | MIN | MAX | UNIT |
|------------------------------------------------------|--------------------------------------------------------------|-----|-----|------|
| $V_{OH}$ High-level output voltage (see Figure 5-31) | $V_{USB} = 3.3\text{ V} \pm 10\%$ , $I_{OH} = -25\text{ mA}$ | 2.4 |     | V    |
| $V_{OL}$ Low-level output voltage (see Figure 5-30)  | $V_{USB} = 3.3\text{ V} \pm 10\%$ , $I_{OL} = 25\text{ mA}$  |     | 0.4 | V    |
| $V_{IH}$ High-level input voltage (see Figure 5-32)  | $V_{USB} = 3.3\text{ V} \pm 10\%$                            | 2.0 |     | V    |
| $V_{IL}$ Low-level input voltage (see Figure 5-32)   | $V_{USB} = 3.3\text{ V} \pm 10\%$                            |     | 0.8 | V    |



**Figure 5-30. Ports PU.0, PU.1 Typical Low-Level Output Characteristics**



**Figure 5-31. Ports PU.0, PU.1 Typical High-Level Output Characteristics**



**Figure 5-32. Ports PU.0, PU.1 Typical Input Threshold Characteristics**

Table 5-49 and Table 5-50 list the characteristics of the DP and DM ports.

**Table 5-49. USB Output Ports DP and DM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS                                             | MIN | MAX | UNIT     |
|------------------------------|-------------------------------------------------------------|-----|-----|----------|
| $V_{OH}$ D+, D– single ended | USB 2.0 load conditions                                     | 2.8 | 3.6 | V        |
| $V_{OL}$ D+, D– single ended | USB 2.0 load conditions                                     | 0   | 0.3 | V        |
| $Z_{(DRV)}$ D+, D– impedance | Including external series resistor of 27 $\Omega$           | 28  | 44  | $\Omega$ |
| $t_{RISE}$ Rise time         | Full speed, differential, $C_L = 50$ pF, 10%/90%, Rpu on D+ | 4   | 20  | ns       |
| $t_{FALL}$ Fall time         | Full speed, differential, $C_L = 50$ pF, 10%/90%, Rpu on D+ | 4   | 20  | ns       |

**Table 5-50. USB Input Ports DP and DM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                       | MIN | MAX | UNIT       |
|-------------------------------------------------|-----|-----|------------|
| $V_{(CM)}$ Differential input common mode range | 0.8 | 2.5 | V          |
| $Z_{(IN)}$ Input impedance                      | 300 |     | k $\Omega$ |
| $V_{CRS}$ Crossover voltage                     | 1.3 | 2.0 | V          |
| $V_{IL}$ Static SE input logic low level        | 0.8 |     | V          |
| $V_{IH}$ Static SE input logic high level       |     | 2.0 | V          |
| $V_{DI}$ Differential input voltage             |     | 0.2 | V          |

Table 5-51 lists the characteristics of the USB power system.

**Table 5-51. USB-PWR (USB Power System)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                                        | TEST CONDITIONS                     | MIN  | TYP | MAX  | UNIT |
|----------------------|------------------------------------------------------------------------|-------------------------------------|------|-----|------|------|
| V <sub>LAUNCH</sub>  | V <sub>BUS</sub> detection threshold                                   |                                     |      |     | 3.75 | V    |
| V <sub>BUS</sub>     | USB bus voltage                                                        | Normal operation                    | 3.76 |     | 5.5  | V    |
| V <sub>USB</sub>     | USB LDO output voltage                                                 |                                     |      | 3.3 | ±9%  | V    |
| V <sub>18</sub>      | Internal USB voltage <sup>(1)</sup>                                    |                                     |      | 1.8 |      | V    |
| I <sub>USB_EXT</sub> | Maximum external current from V <sub>USB</sub> terminal <sup>(2)</sup> | USB LDO is on                       |      |     | 12   | mA   |
| I <sub>DET</sub>     | USB LDO current overload detection <sup>(3)</sup>                      |                                     | 60   |     | 100  | mA   |
| I <sub>SUSPEND</sub> | Operating supply current into V <sub>BUS</sub> terminal <sup>(4)</sup> | USB LDO is on, USB PLL disabled     |      |     | 250  | µA   |
| C <sub>BUS</sub>     | V <sub>BUS</sub> terminal recommended capacitance                      |                                     |      | 4.7 |      | µF   |
| C <sub>USB</sub>     | V <sub>USB</sub> terminal recommended capacitance                      |                                     |      | 220 |      | nF   |
| C <sub>18</sub>      | V <sub>18</sub> terminal recommended capacitance                       |                                     |      | 220 |      | nF   |
| t <sub>ENABLE</sub>  | Settling time V <sub>USB</sub> and V <sub>18</sub>                     | Within 2%, recommended capacitances |      |     | 2    | ms   |
| RPUR                 | Pullup resistance of PUR terminal                                      |                                     | 70   | 110 | 150  | Ω    |

(1) This voltage is for internal use only. No external DC loading should be applied.

(2) This represents additional current that can be supplied to the application from the V<sub>USB</sub> terminal beyond the needs of the USB operation.

(3) A current overload is detected when the total current supplied from the USB LDO, including I<sub>USB\_EXT</sub>, exceeds this value.

(4) Does not include current contribution of R<sub>pu</sub> and R<sub>pd</sub> as outlined in the USB specification.

Table 5-52 lists the characteristics of the USB PLL.

**Table 5-52. USB-PLL (USB Phase-Locked Loop)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                          | MIN | TYP  | MAX | UNIT |
|---------------------|--------------------------|-----|------|-----|------|
| I <sub>PLL</sub>    | Operating supply current |     |      | 7   | mA   |
| f <sub>PLL</sub>    | PLL frequency            |     | 48   |     | MHz  |
| f <sub>UPD</sub>    | PLL reference frequency  | 1.5 |      | 3   | MHz  |
| t <sub>LOCK</sub>   | PLL lock time            |     |      | 2   | ms   |
| t <sub>Jitter</sub> | PLL jitter               |     | 1000 |     | ps   |

## 5.8.18 LDO-PWR (LDO Power System)

Table 5-53 lists the characteristics of the LDO power system.

**Table 5-53. LDO-PWR (LDO Power System)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                               | TEST CONDITIONS                     | MIN  | TYP | MAX  | UNIT |
|----------------------|-----------------------------------------------|-------------------------------------|------|-----|------|------|
| V <sub>LAUNCH</sub>  | LDO input detection threshold                 |                                     |      |     | 3.75 | V    |
| V <sub>LDO</sub>     | LDO input voltage                             |                                     | 3.76 |     | 5.5  | V    |
| V <sub>LDO</sub>     | LDO output voltage                            |                                     |      | 3.3 | ±9%  | V    |
| V <sub>LDO_EXT</sub> | LDOO terminal input voltage with LDO disabled | LDO disabled                        | 1.8  |     | 3.6  | V    |
| I <sub>LDOO</sub>    | Maximum external current from LDOO terminal   | LDO is on                           |      |     | 20   | mA   |
| I <sub>DET</sub>     | LDO current overload detection <sup>(1)</sup> |                                     | 60   |     | 100  | mA   |
| C <sub>LDO</sub>     | LDO terminal recommended capacitance          |                                     |      | 4.7 |      | µF   |
| C <sub>LDOO</sub>    | LDOO terminal recommended capacitance         |                                     |      | 220 |      | nF   |
| t <sub>ENABLE</sub>  | Settling time V <sub>LDO</sub>                | Within 2%, recommended capacitances |      |     | 2    | ms   |

(1) A current overload will be detected when the total current supplied from the LDO exceeds this value.

### 5.8.19 Flash

Table 5-54 lists the characteristics of the flash memory.

**Table 5-54. Flash Memory**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                                                    | T <sub>J</sub> | MIN             | TYP             | MAX | UNIT   |
|------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----------------|-----|--------|
| DV <sub>CC(PGM/ERASE)</sub> Program and erase supply voltage                                                                 |                | 1.8             |                 | 3.6 | V      |
| I <sub>PGM</sub> Average supply current from DV <sub>CC</sub> during program                                                 |                |                 | 3               | 5   | mA     |
| I <sub>ERASE</sub> Average supply current from DV <sub>CC</sub> during erase                                                 |                |                 | 6               | 11  | mA     |
| I <sub>MERASE</sub> , I <sub>BANK</sub> Average supply current from DV <sub>CC</sub> during mass erase or bank erase         |                |                 | 6               | 11  | mA     |
| t <sub>CPT</sub> Cumulative program time <sup>(1)</sup>                                                                      |                |                 |                 | 16  | ms     |
| Program and erase endurance                                                                                                  |                | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles |
| t <sub>Retention</sub> Data retention duration                                                                               | 25°C           | 100             |                 |     | years  |
| t <sub>Word</sub> Word or byte program time <sup>(2)</sup>                                                                   |                | 64              |                 | 85  | μs     |
| t <sub>Block, 0</sub> Block program time for first byte or word <sup>(2)</sup>                                               |                | 49              |                 | 65  | μs     |
| t <sub>Block, 1–(N–1)</sub> Block program time for each additional byte or word, except for last byte or word <sup>(2)</sup> |                | 37              |                 | 49  | μs     |
| t <sub>Block, N</sub> Block program time for last byte or word <sup>(2)</sup>                                                |                | 55              |                 | 73  | μs     |
| t <sub>Seg Erase</sub> Erase time for segment, mass erase, and bank erase when available <sup>(2)</sup>                      |                | 23              |                 | 32  | ms     |
| f <sub>MCLK,MGR</sub> MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)                                |                | 0               |                 | 1   | MHz    |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the state machine of the flash controller.

### 5.8.20 Debug and Emulation

Table 5-55 lists the characteristics of the JTAG and SBW interface.

**Table 5-55. JTAG and Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                                | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------------------------------|-----------------|-------|-----|-----|------|
| f <sub>SBW</sub> Spy-Bi-Wire input frequency                                                             | 2.2 V, 3 V      | 0     |     | 20  | MHz  |
| t <sub>SBW,Low</sub> Spy-Bi-Wire low clock pulse duration                                                | 2.2 V, 3 V      | 0.025 |     | 15  | μs   |
| t <sub>SBW,En</sub> Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) <sup>(1)</sup> | 2.2 V, 3 V      |       |     | 1   | μs   |
| t <sub>SBW,Rst</sub> Spy-Bi-Wire return to normal operation time                                         |                 | 15    |     | 100 | μs   |
| f <sub>TCK</sub> TCK input frequency (4-wire JTAG) <sup>(2)</sup>                                        | 2.2 V           | 0     |     | 5   | MHz  |
|                                                                                                          | 3 V             | 0     |     | 10  | MHz  |
| R <sub>internal</sub> Internal pulldown resistance on TEST                                               | 2.2 V, 3 V      | 45    | 60  | 80  | kΩ   |

(1) Tools that access the Spy-Bi-Wire interface must wait for the t<sub>SBW,En</sub> time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

## 6 Detailed Description

### 6.1 Overview

The MSP430FG6626 and MSP430FG6625 are microcontroller configurations with a high-performance 16-bit ADC, dual 12-bit DACs, dual low-power operational amplifiers, a comparator (COMPB), two USCIs, USB 2.0, a hardware multiplier (MPY32), DMA, four 16-bit timers, an RTC module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

The MSP430FG6426 and MSP430FG6425 are microcontroller configurations with a high-performance 16-bit ADC, dual 12-bit DACs, dual low-power operational amplifiers, a comparator (COMPB), two USCIs, a 3.3-V LDO, a hardware multiplier (MPY32), DMA, four 16-bit timers, an RTC module with alarm capabilities, an LCD driver, and up to 73 I/O pins.

### 6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [图 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**图 6-1. Integrated CPU Registers**

### 6.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. 表 6-1 lists examples of the three types of instruction formats, and 表 6-2 lists the address modes.

**表 6-1. Instruction Word Formats**

| INSTRUCTION WORD FORMAT                     | EXAMPLE   | OPERATION                                 |
|---------------------------------------------|-----------|-------------------------------------------|
| Dual operands, source and destination       | ADD R4,R5 | $R4 + R5 \rightarrow R5$                  |
| Single operands, destination only           | CALL R8   | $PC \rightarrow (TOS), R8 \rightarrow PC$ |
| Relative jump, unconditional or conditional | JNE       | Jump-on-equal bit = 0                     |

**表 6-2. Address Mode Descriptions**

| ADDRESS MODE            | S <sup>(1)</sup> | D <sup>(1)</sup> | SYNTAX           | EXAMPLE          | OPERATION                                             |
|-------------------------|------------------|------------------|------------------|------------------|-------------------------------------------------------|
| Register                | ✓                | ✓                | MOV Rs,Rd        | MOV R10,R11      | $R10 \rightarrow R11$                                 |
| Indexed                 | ✓                | ✓                | MOV X(Rn),Y(Rm)  | MOV 2(R5),6(R6)  | $M(2+R5) \rightarrow M(6+R6)$                         |
| Symbolic (PC relative)  | ✓                | ✓                | MOV EDE,TONI     |                  | $M(EDE) \rightarrow M(TONI)$                          |
| Absolute                | ✓                | ✓                | MOV &MEM, &TCDAT |                  | $M(MEM) \rightarrow M(TCDAT)$                         |
| Indirect                | ✓                |                  | MOV @Rn,Y(Rm)    | MOV @R10,Tab(R6) | $M(R10) \rightarrow M(Tab+R6)$                        |
| Indirect auto-increment | ✓                |                  | MOV @Rn+,Rm      | MOV @R10+,R11    | $M(R10) \rightarrow R11$<br>$R10 + 2 \rightarrow R10$ |
| Immediate               | ✓                |                  | MOV #X,TONI      | MOV #45,TONI     | $\#45 \rightarrow M(TONI)$                            |

(1) S = source, D = destination

## 6.4 Operating Modes

The devices have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No data retention
  - RTC enabled and clocked by low-frequency oscillator
  - Wake-up input from  $\overline{\text{RST}}$ /NMI, RTC\_B, P1, P2, P3, and P4
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up input from  $\overline{\text{RST}}$ /NMI, P1, P2, P3, and P4

## 6.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [表 6-3](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**表 6-3. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE                                                                                                  | INTERRUPT FLAG                                                                                                  | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY    |
|-------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|------------------|--------------|-------------|
| <b>System Reset</b><br>Power-up, External reset<br>Watchdog time-out, key violation<br>Flash memory key violation | WDTIFG, KEYV (SYSRSTIV) <sup>(1)(2)</sup>                                                                       | Reset            | 0FFFEh       | 63, highest |
| <b>System NMI</b><br>PMM<br>Vacant memory access<br>JTAG mailbox                                                  | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG,<br>VLRHIFG, VLRHIFG, VMAIFG, JMBNIFG,<br>JMBOUTIFG (SYSSNIV) <sup>(1)</sup> | (Non)maskable    | 0FFFCCh      | 62          |
| <b>User NMI</b><br>NMI<br>Oscillator fault<br>Flash memory access violation                                       | NMIIFG, OFIFG, ACCVIFG, BUSIFG<br>(SYSUNIV) <sup>(1)(2)</sup>                                                   | (Non)maskable    | 0FFFAh       | 61          |
| Comp_B                                                                                                            | Comparator B interrupt flags (CBIV) <sup>(1)(3)</sup>                                                           | Maskable         | 0FFF8h       | 60          |
| Timer TB0                                                                                                         | TB0CCR0 CCIFG0 <sup>(3)</sup>                                                                                   | Maskable         | 0FFF6h       | 59          |
| Timer TB0                                                                                                         | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6,<br>TB0IFG (TBIV) <sup>(1)(3)</sup>                                            | Maskable         | 0FFF4h       | 58          |
| Watchdog interval timer mode                                                                                      | WDTIFG                                                                                                          | Maskable         | 0FFF2h       | 57          |
| USCI_A0 receive or transmit                                                                                       | UCA0RXIFG, UCA0TXIFG (UCA0IV) <sup>(1)(3)</sup>                                                                 | Maskable         | 0FFF0h       | 56          |
| USCI_B0 receive or transmit                                                                                       | UCB0RXIFG, UCB0TXIFG (UCB0IV) <sup>(1)(3)</sup>                                                                 | Maskable         | 0FFEEh       | 55          |
| CTSD16                                                                                                            | CTSD16IFG0, CTSD16OVIFG0 <sup>(1)(3)</sup>                                                                      | Maskable         | 0FFECCh      | 54          |
| Timer TA0                                                                                                         | TA0CCR0 CCIFG0 <sup>(3)</sup>                                                                                   | Maskable         | 0FFEAh       | 53          |
| Timer TA0                                                                                                         | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4,<br>TA0IFG (TA0IV) <sup>(1)(3)</sup>                                           | Maskable         | 0FFE8h       | 52          |
| USB_UBM <sup>(4)</sup>                                                                                            | USB interrupts (USBIV) <sup>(1)(3)</sup>                                                                        | Maskable         | 0FFE6h       | 51          |
| LDO-PWR <sup>(5)</sup>                                                                                            | LDOOFFIFG, LDOONIFG, LDOOVLIFG                                                                                  |                  |              |             |
| DMA                                                                                                               | DMA0IFG, DMA1IFG, DMA2IFG, DMA3IFG,<br>DMA4IFG, DMA5IFG (DMAIV) <sup>(1)(3)</sup>                               | Maskable         | 0FFE4h       | 50          |
| Timer TA1                                                                                                         | TA1CCR0 CCIFG0 <sup>(3)</sup>                                                                                   | Maskable         | 0FFE2h       | 49          |
| Timer TA1                                                                                                         | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2,<br>TA1IFG (TA1IV) <sup>(1)(3)</sup>                                           | Maskable         | 0FFE0h       | 48          |
| I/O Port P1                                                                                                       | P1IFG.0 to P1IFG.7 (P1IV) <sup>(1)(3)</sup>                                                                     | Maskable         | 0FFDEh       | 47          |
| USCI_A1 receive or transmit                                                                                       | UCA1RXIFG, UCA1TXIFG (UCA1IV) <sup>(1)(3)</sup>                                                                 | Maskable         | 0FFDCh       | 46          |
| USCI_B1 receive or transmit                                                                                       | UCB1RXIFG, UCB1TXIFG (UCB1IV) <sup>(1)(3)</sup>                                                                 | Maskable         | 0FFDAh       | 45          |
| I/O port P2                                                                                                       | P2IFG.0 to P2IFG.7 (P2IV) <sup>(1)(3)</sup>                                                                     | Maskable         | 0FFD8h       | 44          |
| LCD_B                                                                                                             | LCD_B Interrupt Flags (LCDBIV) <sup>(1)</sup>                                                                   | Maskable         | 0FFD6h       | 43          |
| RTC_B                                                                                                             | RTCRDYIFG, RTCTEVIFG, RTCAIFG,<br>RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) <sup>(1)(3)</sup>                        | Maskable         | 0FFD4h       | 42          |
| DAC12_A                                                                                                           | DAC12_0IFG, DAC12_1IFG <sup>(1)(3)</sup>                                                                        | Maskable         | 0FFD2h       | 41          |
| Timer TA2                                                                                                         | TA2CCR0 CCIFG0 <sup>(3)</sup>                                                                                   | Maskable         | 0FFD0h       | 40          |
| Timer TA2                                                                                                         | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2,<br>TA2IFG (TA2IV) <sup>(1)(3)</sup>                                           | Maskable         | 0FFCEh       | 39          |
| I/O port P3                                                                                                       | P3IFG.0 to P3IFG.7 (P3IV) <sup>(1)(3)</sup>                                                                     | Maskable         | 0FFCCh       | 38          |
| I/O port P4                                                                                                       | P4IFG.0 to P4IFG.7 (P4IV) <sup>(1)(3)</sup>                                                                     | Maskable         | 0FFCAh       | 37          |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.

(3) Interrupt flags are in the module.

(4) Only on devices with peripheral module USB (MSP430FG6626 and MSP430FG6625)

(5) Only on devices with peripheral module LDO-PWR (MSP430FG6426 and MSP430FG6425)

**表 6-3. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG          | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY  |
|------------------|-------------------------|------------------|--------------|-----------|
| Reserved         | Reserved <sup>(6)</sup> |                  | 0FFC8h       | 36        |
|                  |                         |                  | ⋮            | ⋮         |
|                  |                         |                  | 0FF80h       | 0, lowest |

(6) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

## 6.6 USB BSL

The devices MSP430FG6626 and MSP430FG6625 are preprogrammed with the USB BSL. Use of the USB BSL requires external access to six pins (see 表 6-4). In addition to these pins, the application must support external components necessary for normal USB operation; for example, the proper crystal on XT2IN and XT2OUT, proper decoupling, and so on.

**表 6-4. USB BSL Pin Requirements and Functions**

| DEVICE SIGNAL                                     | BSL FUNCTION                 |
|---------------------------------------------------|------------------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal        |
| PU.0/DP                                           | USB data terminal DP         |
| PU.1/DM                                           | USB data terminal DM         |
| PUR                                               | USB pullup resistor terminal |
| VBUS                                              | USB bus power supply         |
| VSSU                                              | USB ground supply            |

### 注

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless the application is invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends applying a 1-M $\Omega$  resistor to ground.

## 6.7 UART BSL

Devices without a USB module (MSP430FG642x) come preprogrammed with the UART BSL. A UART BSL is also available for devices with the USB module (MSP430FG662x), and it can be programmed by the user into the BSL memory by replacing the preprogrammed factory-supplied USB BSL. Use of the UART BSL requires external access to six pins (see 表 6-5).

**表 6-5. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL                                     | BSL FUNCTION          |
|---------------------------------------------------|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| TEST/SBWTK                                        | Entry sequence signal |
| P1.1                                              | Data transmit         |
| P1.2                                              | Data receive          |
| VCC                                               | Power supply          |
| VSS                                               | Ground supply         |

## 6.8 JTAG Operation

### 6.8.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the  $\overline{\text{RST}}$ /NMI/SBWDIO is required to interface with MSP430 development tools and device programmers. 表 6-6 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

表 6-6. JTAG Pin Requirements and Functions

| DEVICE SIGNAL                       | DIRECTION | FUNCTION                    |
|-------------------------------------|-----------|-----------------------------|
| PJ.3/TCK                            | IN        | JTAG clock input            |
| PJ.2/TMS                            | IN        | JTAG state control          |
| PJ.1/TDI/TCLK                       | IN        | JTAG data input, TCLK input |
| PJ.0/TDO                            | OUT       | JTAG data output            |
| TEST/SBWTCK                         | IN        | Enable JTAG pins            |
| $\overline{\text{RST}}$ /NMI/SBWDIO | IN        | External reset              |
| VCC                                 |           | Power supply                |
| VSS                                 |           | Ground supply               |

### 6.8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-7 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

表 6-7. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL                       | DIRECTION | FUNCTION                      |
|-------------------------------------|-----------|-------------------------------|
| TEST/SBWTCK                         | IN        | Spy-Bi-Wire clock input       |
| $\overline{\text{RST}}$ /NMI/SBWDIO | IN, OUT   | Spy-Bi-Wire data input/output |
| VCC                                 |           | Power supply                  |
| VSS                                 |           | Ground supply                 |

## 6.9 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

## 6.10 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in [节 6.15](#).
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

## 6.11 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5 and during operation from a backup supply if the Battery Backup System module is implemented.

There are 8 bytes of backup RAM. It can be word-wise accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

## 6.12 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

### 6.12.1 Digital I/O

Up to nine 8-bit I/O ports are implemented: P1 through P9 are complete except P5.2, and port PJ contains four individual I/O ports.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise (P1 through P8) in pairs (PA through PD).

### 6.12.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P2 (see 表 6-8).

**表 6-8. Port Mapping Mnemonics and Functions**

| VALUE                    | PxMAPy MNEMONIC | INPUT PIN FUNCTION                                                                                                         | OUTPUT PIN FUNCTION                  |
|--------------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| 0                        | PM_NONE         | None                                                                                                                       | DVSS                                 |
| 1                        | PM_CBOUT        | –                                                                                                                          | Comparator_B output                  |
|                          | PM_TB0CLK       | Timer TB0 clock input                                                                                                      | –                                    |
| 2                        | Reserved        | –                                                                                                                          | Reserved                             |
|                          | PM_DMAE0        | DMAE0 Input                                                                                                                | –                                    |
| 3                        | PM_SVMOUT       | –                                                                                                                          | SVM output                           |
|                          | PM_TB0OUTH      | Timer TB0 high impedance input TB0OUTH                                                                                     | –                                    |
| 4                        | PM_TB0CCR0B     | Timer TB0 CCR0 capture input CCI0B                                                                                         | Timer TB0: TB0.0 compare output Out0 |
| 5                        | PM_TB0CCR1B     | Timer TB0 CCR1 capture input CCI1B                                                                                         | Timer TB0: TB0.1 compare output Out1 |
| 6                        | PM_TB0CCR2B     | Timer TB0 CCR2 capture input CCI2B                                                                                         | Timer TB0: TB0.2 compare output Out2 |
| 7                        | PM_TB0CCR3B     | Timer TB0 CCR3 capture input CCI3B                                                                                         | Timer TB0: TB0.3 compare output Out3 |
| 8                        | PM_TB0CCR4B     | Timer TB0 CCR4 capture input CCI4B                                                                                         | Timer TB0: TB0.4 compare output Out4 |
| 9                        | PM_TB0CCR5B     | Timer TB0 CCR5 capture input CCI5B                                                                                         | Timer TB0: TB0.5 compare output Out5 |
| 10                       | PM_TB0CCR6B     | Timer TB0 CCR6 capture input CCI6B                                                                                         | Timer TB0: TB0.6 compare output Out6 |
| 11                       | PM_UCA0RXD      | USCI_A0 UART RXD (Direction controlled by USCI – input)                                                                    |                                      |
|                          | PM_UCA0SOMI     | USCI_A0 SPI slave out master in (direction controlled by USCI)                                                             |                                      |
| 12                       | PM_UCA0TXD      | USCI_A0 UART TXD (Direction controlled by USCI – output)                                                                   |                                      |
|                          | PM_UCA0SIMO     | USCI_A0 SPI slave in master out (direction controlled by USCI)                                                             |                                      |
| 13                       | PM_UCA0CLK      | USCI_A0 clock input/output (direction controlled by USCI)                                                                  |                                      |
|                          | PM_UCB0STE      | USCI_B0 SPI slave transmit enable (direction controlled by USCI – input)                                                   |                                      |
| 14                       | PM_UCB0SOMI     | USCI_B0 SPI slave out master in (direction controlled by USCI)                                                             |                                      |
|                          | PM_UCB0SCL      | USCI_B0 I <sup>2</sup> C clock (open drain and direction controlled by USCI)                                               |                                      |
| 15                       | PM_UCB0SIMO     | USCI_B0 SPI slave in master out (direction controlled by USCI)                                                             |                                      |
|                          | PM_UCB0SDA      | USCI_B0 I <sup>2</sup> C data (open drain and direction controlled by USCI)                                                |                                      |
| 16                       | PM_UCB0CLK      | USCI_B0 clock input/output (direction controlled by USCI)                                                                  |                                      |
|                          | PM_UCA0STE      | USCI_A0 SPI slave transmit enable (direction controlled by USCI – input)                                                   |                                      |
| 17                       | PM_MCLK         | –                                                                                                                          | MCLK                                 |
| 18-30                    | Reserved        | None                                                                                                                       | DVSS                                 |
| 31 (0FFh) <sup>(1)</sup> | PM_ANALOG       | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. |                                      |

(1) The value of the PM\_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read out value of 31.

表 6-9 lists the default settings for all pins that support port mapping.

**表 6-9. Default Mapping**

| PIN                    | PxMAPy<br>MNEMONIC         | INPUT PIN FUNCTION                                                                                                                              | OUTPUT PIN FUNCTION |
|------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| P2.0/P2MAP0            | PM_UCB0STE,<br>PM_UCA0CLK  | USCI_B0 SPI slave transmit enable (direction controlled by USCI – input),<br>USCI_A0 clock input/output (direction controlled by USCI)          |                     |
| P2.1/P2MAP1            | PM_UCB0SIMO,<br>PM_UCB0SDA | USCI_B0 SPI slave in master out (direction controlled by USCI),<br>USCI_B0 I <sup>2</sup> C data (open drain and direction controlled by USCI)  |                     |
| P2.2/P2MAP2            | PM_UCB0SOMI,<br>PM_UCB0SCL | USCI_B0 SPI slave out master in (direction controlled by USCI),<br>USCI_B0 I <sup>2</sup> C clock (open drain and direction controlled by USCI) |                     |
| P2.3/P2MAP3            | PM_UCB0CLK,<br>PM_UCA0STE  | USCI_B0 clock input/output (direction controlled by USCI),<br>USCI_A0 SPI slave transmit enable (direction controlled by USCI – input)          |                     |
| P2.4/P2MAP4            | PM_UCA0TXD,<br>PM_UCA0SIMO | USCI_A0 UART TXD (direction controlled by USCI – output),<br>USCI_A0 SPI slave in master out (direction controlled by USCI)                     |                     |
| P2.5/P2MAP5/R23        | PM_UCA0RXD,<br>PM_UCA0SOMI | USCI_A0 UART RXD (direction controlled by USCI – input),<br>USCI_A0 SPI slave out master in (direction controlled by USCI)                      |                     |
| P2.6/P2MAP6/R03        | PM_NONE                    | -                                                                                                                                               | DVSS                |
| P2.7/P2MAP7/LCDREF/R13 | PM_NONE                    | -                                                                                                                                               | DVSS                |

### 6.12.3 Oscillator and System Clock

The clock system in the MSP430FG662x and MSP430FG642x devices are supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (in XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3  $\mu$ s (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

### 6.12.4 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detect if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and the core supply.

### 6.12.5 Hardware Multiplier (MPY32)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 6.12.6 Real-Time Clock (RTC\_B)

The RTC\_B module can be configured for real-time clock (RTC) or calendar mode providing seconds, minutes, hours, day of week, day of month, month, and year. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC\_B also supports flexible alarm functions and offset-calibration hardware. The implementation on this device supports operation in LPM3.5 mode and operation from a backup supply.

### 6.12.7 Watchdog Timer (WDT\_A)

The primary function of the WDT\_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### 6.12.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. 表 6-10 lists the SYS module interrupt vector registers.

**表 6-10. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT                    | WORD ADDRESS | OFFSET     | PRIORITY |
|---------------------------|------------------------------------|--------------|------------|----------|
| SYSRSTIV, System Reset    | No interrupt pending               | 019Eh        | 00h        |          |
|                           | Brownout (BOR)                     |              | 02h        | Highest  |
|                           | $\overline{\text{RST}}$ /NMI (BOR) |              | 04h        |          |
|                           | PMMSWBOR (BOR)                     |              | 06h        |          |
|                           | LPM3.5 or LPM4.5 wake up (BOR)     |              | 08h        |          |
|                           | Security violation (BOR)           |              | 0Ah        |          |
|                           | SVSL (POR)                         |              | 0Ch        |          |
|                           | SVSH (POR)                         |              | 0Eh        |          |
|                           | SVML_OVP (POR)                     |              | 10h        |          |
|                           | SVMH_OVP (POR)                     |              | 12h        |          |
|                           | PMMSWPOR (POR)                     |              | 14h        |          |
|                           | WDT time-out (PUC)                 |              | 16h        |          |
|                           | WDT key violation (PUC)            |              | 18h        |          |
|                           | KEYV flash key violation (PUC)     |              | 1Ah        |          |
|                           | Reserved                           |              | 1Ch        |          |
|                           | Peripheral area fetch (PUC)        |              | 1Eh        |          |
|                           | PMM key violation (PUC)            |              | 20h        |          |
|                           | Reserved                           |              | 22h to 3Eh | Lowest   |

**表 6-10. System Module Interrupt Vector Registers (continued)**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT         | WORD ADDRESS | OFFSET     | PRIORITY |
|---------------------------|-------------------------|--------------|------------|----------|
| SYSSNIV, System NMI       | No interrupt pending    | 019Ch        | 00h        | Highest  |
|                           | SVMLIFG                 |              | 02h        |          |
|                           | SVMHIFG                 |              | 04h        |          |
|                           | DLYLIFG                 |              | 06h        |          |
|                           | DLYHIFG                 |              | 08h        |          |
|                           | VMAIFG                  |              | 0Ah        |          |
|                           | JMBINIFG                |              | 0Ch        |          |
|                           | JMBOUTIFG               |              | 0Eh        |          |
|                           | SVMLVLRIFG              |              | 10h        |          |
|                           | SVMHVLRIFG              |              | 12h        |          |
|                           | Reserved                |              | 14h to 1Eh | Lowest   |
| SYSUNIV, User NMI         | No interrupt pending    | 019Ah        | 00h        | Highest  |
|                           | NMIFG                   |              | 02h        |          |
|                           | OFIFG                   |              | 04h        |          |
|                           | ACCVIFG                 |              | 06h        |          |
|                           | BUSIFG                  |              | 08h        |          |
|                           | Reserved                |              | 0Ah to 1Eh | Lowest   |
| SYSBERRIV, Bus Error      | No interrupt pending    | 0198h        | 00h        |          |
|                           | USB wait state time-out |              | 02h        | Highest  |
|                           | Reserved                |              | 04h to 1Eh | Lowest   |

### 6.12.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also uses the channel 0, 1, and 2 DMA trigger assignments (see [表 6-11](#)). The USB timestamp generator is available only on devices with the USB module (MSP430FG662x).

**表 6-11. DMA Trigger Assignments<sup>(1)</sup>**

| TRIGGER | CHANNEL                  |         |         |         |         |         |
|---------|--------------------------|---------|---------|---------|---------|---------|
|         | 0                        | 1       | 2       | 3       | 4       | 5       |
| 0       | DMAREQ                   |         |         |         |         |         |
| 1       | TA0CCR0 CCIFG            |         |         |         |         |         |
| 2       | TA0CCR2 CCIFG            |         |         |         |         |         |
| 3       | TA1CCR0 CCIFG            |         |         |         |         |         |
| 4       | TA1CCR2 CCIFG            |         |         |         |         |         |
| 5       | TA2CCR0 CCIFG            |         |         |         |         |         |
| 6       | TA2CCR2 CCIFG            |         |         |         |         |         |
| 7       | TBCCR0 CCIFG             |         |         |         |         |         |
| 8       | TBCCR2 CCIFG             |         |         |         |         |         |
| 9       | Reserved                 |         |         |         |         |         |
| 10      | Reserved                 |         |         |         |         |         |
| 11      | Reserved                 |         |         |         |         |         |
| 12      | Reserved                 |         |         |         |         |         |
| 13      | Reserved                 |         |         |         |         |         |
| 14      | Reserved                 |         |         |         |         |         |
| 15      | Reserved                 |         |         |         |         |         |
| 16      | UCA0RXIFG                |         |         |         |         |         |
| 17      | UCA0TXIFG                |         |         |         |         |         |
| 18      | UCB0RXIFG                |         |         |         |         |         |
| 19      | UCB0TXIFG                |         |         |         |         |         |
| 20      | UCA1RXIFG                |         |         |         |         |         |
| 21      | UCA1TXIFG                |         |         |         |         |         |
| 22      | UCB1RXIFG                |         |         |         |         |         |
| 23      | UCB1TXIFG                |         |         |         |         |         |
| 24      | CTSD16IFG0               |         |         |         |         |         |
| 25      | DAC12_0IFG               |         |         |         |         |         |
| 26      | DAC12_1IFG               |         |         |         |         |         |
| 27      | USB FNRXD <sup>(2)</sup> |         |         |         |         |         |
| 28      | USB ready <sup>(2)</sup> |         |         |         |         |         |
| 29      | MPY ready                |         |         |         |         |         |
| 30      | DMA5IFG                  | DMA0IFG | DMA1IFG | DMA2IFG | DMA3IFG | DMA4IFG |
| 31      | DMAE0                    |         |         |         |         |         |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

(2) Only on devices with peripheral module USB (MSP430FG662x), otherwise reserved (MSP430FG642x).

### 6.12.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I<sup>2</sup>C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI\_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI\_Bn module provides support for SPI (3- or 4-pin) or I<sup>2</sup>C.

The MSP430FG662x and MSP430FG642x include two complete USCI modules (n = 0 to 1).

### 6.12.11 Timer TA0

Timer TA0 is a 16-bit timer/counter (Timer\_A type) with five capture/compare registers. TA0 supports multiple capture/compares, PWM outputs, and interval timing (see 表 6-12). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-12. Timer TA0 Signal Connections**

| INPUT PIN NUMBER |         | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER |         |
|------------------|---------|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|-------------------|---------|
| PZ               | ZQW     |                           |                           |                 |                            |                            | PZ                | ZQW     |
| 34-P1.0          | L5-P1.0 | TA0CLK                    | TACLK                     | Timer           | NA                         | NA                         |                   |         |
|                  |         | ACLK                      | ACLK                      |                 |                            |                            |                   |         |
|                  |         | SMCLK                     | SMCLK                     |                 |                            |                            |                   |         |
| 34-P1.0          | L5-P1.0 | TA0CLK                    | TACLK                     | CCR0            | TA0                        | TA0.0                      |                   |         |
| 35-P1.1          | M5-P1.1 | TA0.0                     | CCI0A                     |                 |                            |                            | 35-P1.1           | M5-P1.1 |
|                  |         | DV <sub>SS</sub>          | CCI0B                     |                 |                            |                            |                   |         |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR1            | TA1                        | TA0.1                      |                   |         |
| 36-P1.2          | J6-P1.2 | TA0.1                     | CCI1A                     |                 |                            |                            | 36-P1.2           | J6-P1.2 |
| 40-P1.6          | J7-P1.6 | TA0.1                     | CCI1B                     |                 |                            |                            | 40-P1.6           | J7-P1.6 |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR2            | TA2                        | TA0.2                      |                   |         |
| 37-P1.3          | H6-P1.3 | TA0.2                     | CCI2A                     |                 |                            |                            | 37-P1.3           | H6-P1.3 |
| 41-P1.7          | M7-P1.7 | TA0.2                     | CCI2B                     |                 |                            |                            | 41-P1.7           | M7-P1.7 |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR3            | TA3                        | TA0.3                      |                   |         |
| 38-P1.4          | M6-P1.4 | TA0.3                     | CCI3A                     |                 |                            |                            | 38-P1.4           | M6-P1.4 |
|                  |         | DV <sub>SS</sub>          | CCI3B                     |                 |                            |                            |                   |         |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR4            | TA4                        | TA0.4                      |                   |         |
| 39-P1.5          | L6-P1.5 | TA0.4                     | CCI4A                     |                 |                            |                            | 39-P1.5           | L6-P1.5 |
|                  |         | DV <sub>SS</sub>          | CCI4B                     |                 |                            |                            |                   |         |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           |                 |                            |                            |                   |         |

### 6.12.12 Timer TA1

Timer TA1 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. TA1 supports multiple capture/compares, PWM outputs, and interval timing (see [表 6-13](#)). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-13. Timer TA1 Signal Connections**

| INPUT PIN NUMBER |         | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER                         |         |
|------------------|---------|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|-------------------------------------------|---------|
| PZ               | ZQW     |                           |                           |                 |                            |                            | PZ                                        | ZQW     |
| 42-P3.0          | L7-P3.0 | TA1CLK                    | TACLK                     | Timer           | NA                         | NA                         |                                           |         |
|                  |         | ACLK                      | ACLK                      |                 |                            |                            |                                           |         |
|                  |         | SMCLK                     | SMCLK                     |                 |                            |                            |                                           |         |
| 42-P3.0          | L7-P3.0 | TA1CLK                    | $\overline{\text{TACLK}}$ | CCR0            | TA0                        | TA1.0                      | 43-P3.1                                   | H7-P3.1 |
| 43-P3.1          | H7-P3.1 | TA1.0                     | CCI0A                     |                 |                            |                            |                                           |         |
|                  |         | DV <sub>SS</sub>          | CCI0B                     |                 |                            |                            |                                           |         |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                                           |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR1            | TA1                        | TA1.1                      | 44-P3.2                                   | M8-P3.2 |
| 44-P3.2          | M8-P3.2 | TA1.1                     | CCI1A                     |                 |                            |                            | DAC12_A<br>DAC12_0, DAC12_1<br>(internal) |         |
|                  |         | CBOUT<br>(internal)       | CCI1B                     |                 |                            |                            |                                           |         |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                                           |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR2            | TA2                        | TA1.2                      | 45-P3.3                                   | L8-P3.3 |
| 45-P3.3          | L8-P3.3 | TA1.2                     | CCI2A                     |                 |                            |                            |                                           |         |
|                  |         | ACLK<br>(internal)        | CCI2B                     |                 |                            |                            |                                           |         |
|                  |         | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                                           |         |
|                  |         | DV <sub>CC</sub>          | V <sub>CC</sub>           |                 |                            |                            |                                           |         |

### 6.12.13 Timer TA2

Timer TA2 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. TA2 supports multiple capture/compares, PWM outputs, and interval timing (see [表 6-14](#)). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-14. Timer TA2 Signal Connections**

| INPUT PIN NUMBER |          | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER |          |
|------------------|----------|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|-------------------|----------|
| PZ               | ZQW      |                           |                           |                 |                            |                            | PZ                | ZQW      |
| 46-P3.4          | J8-P3.4  | TA2CLK                    | TACLK                     | Timer           | NA                         | NA                         |                   |          |
|                  |          | ACLK                      | ACLK                      |                 |                            |                            |                   |          |
|                  |          | SMCLK                     | SMCLK                     |                 |                            |                            |                   |          |
| 46-P3.4          | J8-P3.4  | TA2CLK                    | $\overline{\text{TACLK}}$ | CCR0            | TA0                        | TA2.0                      | 47-P3.5           | M9-P3.5  |
| 47-P3.5          | M9-P3.5  | TA2.0                     | CCI0A                     |                 |                            |                            |                   |          |
|                  |          | DV <sub>SS</sub>          | CCI0B                     |                 |                            |                            |                   |          |
|                  |          | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |          |
|                  |          | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR1            | TA1                        | TA2.1                      | 48-P3.6           | L9-P3.6  |
| 48-P3.6          | L9-P3.6  | TA2.1                     | CCI1A                     |                 |                            |                            |                   |          |
|                  |          | CBOU<br>(internal)        | CCI1B                     |                 |                            |                            |                   |          |
|                  |          | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |          |
|                  |          | DV <sub>CC</sub>          | V <sub>CC</sub>           | CCR2            | TA2                        | TA2.2                      | 49-P3.7           | M10-P3.7 |
| 49-P3.7          | M10-P3.7 | TA2.2                     | CCI2A                     |                 |                            |                            |                   |          |
|                  |          | ACLK<br>(internal)        | CCI2B                     |                 |                            |                            |                   |          |
|                  |          | DV <sub>SS</sub>          | GND                       |                 |                            |                            |                   |          |
|                  |          | DV <sub>CC</sub>          | V <sub>CC</sub>           |                 |                            |                            |                   |          |

### 6.12.14 Timer TB0

Timer TB0 is a 16-bit timer/counter (Timer\_B type) with seven capture/compare registers. TB0 supports multiple capture/compares, PWM outputs, and interval timing (see 表 6-15). It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-15. Timer TB0 Signal Connections

| INPUT PIN NUMBER                             |                                               | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL  | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER                            |                                               |
|----------------------------------------------|-----------------------------------------------|---------------------------|----------------------------|-----------------|----------------------------|----------------------------|----------------------------------------------|-----------------------------------------------|
| PZ                                           | ZQW                                           |                           |                            |                 |                            |                            | PZ                                           | ZQW                                           |
| 58-P8.0<br>P2MAP <sub>x</sub> <sup>(1)</sup> | J11-P8.0<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0CLK                    | TB0CLK                     | Timer           | NA                         | NA                         |                                              |                                               |
|                                              |                                               | ACLK                      | ACLK                       |                 |                            |                            |                                              |                                               |
|                                              |                                               | SMCLK                     | SMCLK                      |                 |                            |                            |                                              |                                               |
| 58-P8.0<br>P2MAP <sub>x</sub> <sup>(1)</sup> | J11-P8.0<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0CLK                    | $\overline{\text{TB0CLK}}$ |                 |                            |                            |                                              |                                               |
| 50-P4.0<br>P2MAP <sub>x</sub> <sup>(1)</sup> | J9-P4.0<br>P2MAP <sub>x</sub> <sup>(1)</sup>  | TB0.0                     | CCI0A                      | CCR0            | TB0                        | TB0.0                      | 50-P4.0<br>P2MAP <sub>x</sub> <sup>(1)</sup> | J9-P4.0<br>P2MAP <sub>x</sub> <sup>(1)</sup>  |
|                                              |                                               | TB0.0                     | CCI0B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |
| 51-P4.1<br>P2MAP <sub>x</sub> <sup>(1)</sup> | M11-P4.1<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0.1                     | CCI1A                      | CCR1            | TB1                        | TB0.1                      | 51-P4.1<br>P2MAP <sub>x</sub> <sup>(1)</sup> | M11-P4.1<br>P2MAP <sub>x</sub> <sup>(1)</sup> |
|                                              |                                               | TB0.1                     | CCI1B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |
| 52-P4.2<br>P2MAP <sub>x</sub> <sup>(1)</sup> | L10-P4.2<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0.2                     | CCI2A                      | CCR2            | TB2                        | TB0.2                      | 52-P4.2<br>P2MAP <sub>x</sub> <sup>(1)</sup> | L10-P4.2<br>P2MAP <sub>x</sub> <sup>(1)</sup> |
|                                              |                                               | TB0.2                     | CCI2B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            | DAC12_A<br>DAC12_0, DAC12_1<br>(internal)    |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |
| 53-P4.3<br>P2MAP <sub>x</sub> <sup>(1)</sup> | M12-P4.3<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0.3                     | CCI3A                      | CCR3            | TB3                        | TB0.3                      | 53-P4.3<br>P2MAP <sub>x</sub> <sup>(1)</sup> | M12-P4.3<br>P2MAP <sub>x</sub> <sup>(1)</sup> |
|                                              |                                               | TB0.3                     | CCI3B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |
| 54-P4.4<br>P2MAP <sub>x</sub> <sup>(1)</sup> | L12-P4.4<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0.4                     | CCI4A                      | CCR4            | TB4                        | TB0.4                      | 54-P4.4<br>P2MAP <sub>x</sub> <sup>(1)</sup> | L12-P4.4<br>P2MAP <sub>x</sub> <sup>(1)</sup> |
|                                              |                                               | TB0.4                     | CCI4B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |
| 55-P4.5<br>P2MAP <sub>x</sub> <sup>(1)</sup> | L11-P4.5<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0.5                     | CCI5A                      | CCR5            | TB5                        | TB0.5                      | 55-P4.5<br>P2MAP <sub>x</sub> <sup>(1)</sup> | L11-P4.5<br>P2MAP <sub>x</sub> <sup>(1)</sup> |
|                                              |                                               | TB0.5                     | CCI5B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |
| 56-P4.6<br>P2MAP <sub>x</sub> <sup>(1)</sup> | K11-P4.6<br>P2MAP <sub>x</sub> <sup>(1)</sup> | TB0.6                     | CCI6A                      | CCR6            | TB6                        | TB0.6                      | 56-P4.6<br>P2MAP <sub>x</sub> <sup>(1)</sup> | K11-P4.6<br>P2MAP <sub>x</sub> <sup>(1)</sup> |
|                                              |                                               | TB0.6                     | CCI6B                      |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>SS</sub>          | GND                        |                 |                            |                            |                                              |                                               |
|                                              |                                               | DV <sub>CC</sub>          | V <sub>CC</sub>            |                 |                            |                            |                                              |                                               |

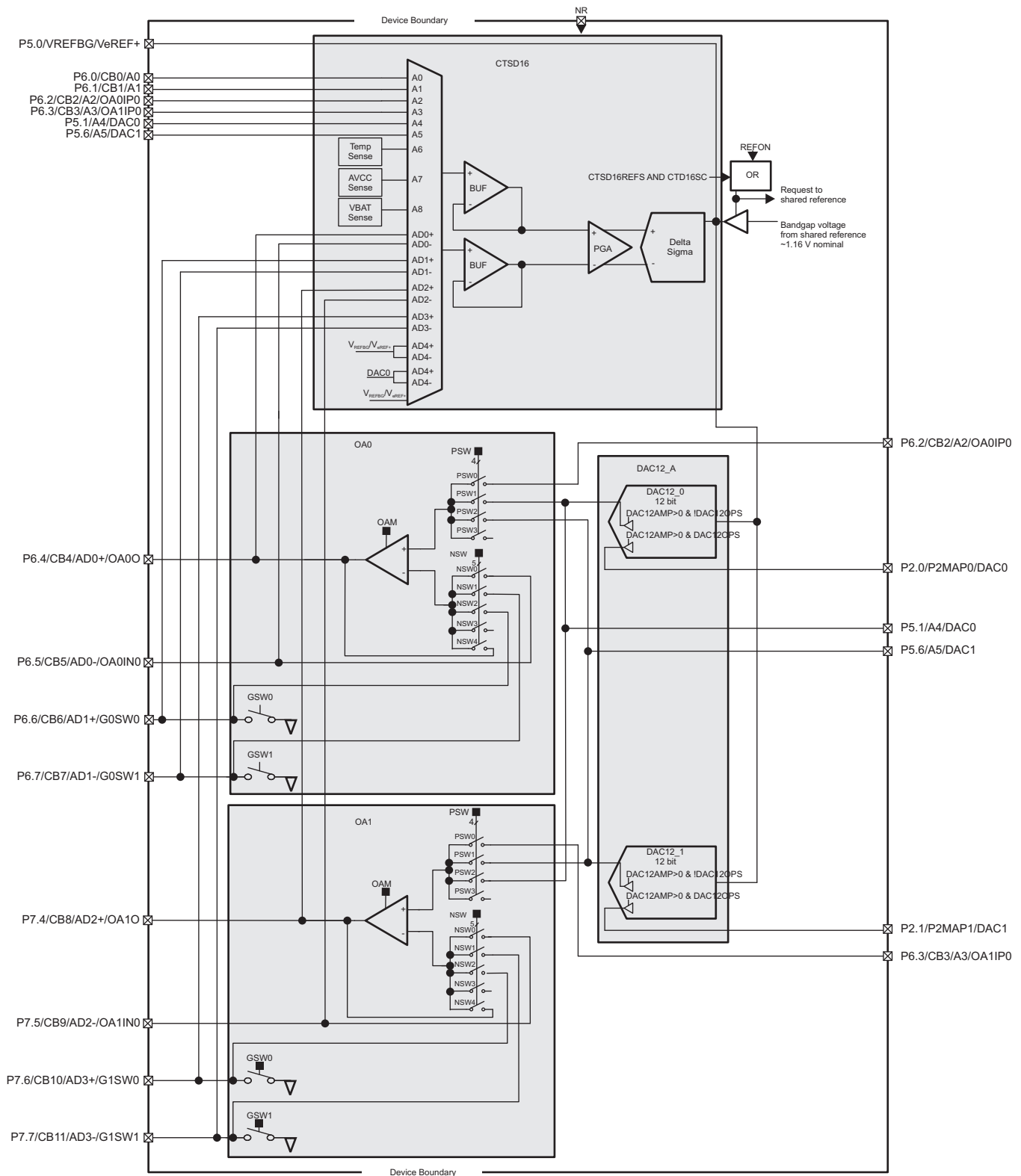
(1) Timer functions are selectable by the port mapping controller.

### 6.12.15 Comparator\_B

The primary function of the Comparator\_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### 6.12.16 Signal Chain

All devices include all the building blocks to construct a complete signal chain. These blocks include two digital-to-analog converter (DAC) channels, two integrated operational amplifiers (OAs), a sigma-delta analog-to-digital converter (CTSD16), and low-ohmic switches (GSW). 图 6-2 shows the various signal chain blocks and their interconnections in the overall system.



NOTE: See the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for additional module details.

图 6-2. Signal Chain

#### 6.12.16.1 CTSD16

The CTSD16 module integrates a single sigma-delta ADC with ten external inputs and four internal inputs. The converter is designed with a fully differential analog input pair and a programmable gain amplifier input stage. The converter is based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb type filters with selectable oversampling ratios of up to 256.

The CTSD16 is preceded by an analog multiplexer which is used for channel selection, followed by a unity gain buffer stage useful when sampling high impedance sensors.

The CTSD16 can use as its reference the internal bandgap voltage from the REF module or an external reference at the V<sub>REF+</sub> pin.

#### 6.12.16.2 DAC12\_A

The DAC12\_A module is a 12-bit R-ladder voltage-output DAC. The DAC12\_A can be used in 8-bit or 12-bit mode, and can be used in conjunction with the DMA controller. When multiple DAC12\_A modules are present, they may be grouped together for synchronous operation. Two complete channels are available, DAC12\_0 and DAC12\_1.

#### 6.12.16.3 Operational Amplifiers (OA)

The device integrates two low-power operational amplifiers. The operational amplifiers can perform signal conditioning of low-level analog signals before conversion by the ADC. Each operational amplifier can be individually controlled by software.

#### 6.12.16.4 Ground Switches (GSW)

The device integrates four low-ohmic switches to ground that are individually controllable in software. These can switch in and out various components in the measurement system.

#### 6.12.17 REF Voltage Reference

The reference module (REF) generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

#### 6.12.18 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

#### 6.12.19 LCD\_B

The LCD\_B driver generates the segment and common signals that are required to drive a liquid crystal display (LCD). The LCD\_B controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage, and thus contrast, by software. The module also provides an automatic blinking capability for individual segments.

#### 6.12.20 USB Universal Serial Bus

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

The USB module is only available on the MSP430FG662x devices.

### 6.12.21 LDO and PU Port

The integrated 3.3-V power system incorporates an integrated 3.3-V LDO regulator that allows the entire MSP430 microcontroller to be powered from nominal 5-V LDO1 when it is made available for the system. Alternatively, the power system can supply power only to other components within the system, or it can be unused altogether.

The Port U pins (PU.0 and PU.1) function as general-purpose high-current I/O pins. These pins must be configured together as either both inputs or both outputs. Port U is supplied by the LDO0 rail. If the 3.3-V LDO is not used in the system (disabled), the LDO0 pin can be supplied externally.

The LDO-PWR module (LDO and PU port) is available only on the MSP430FG6426 and MSP430FG6425 devices.

### 6.12.22 Embedded Emulation Module (EEM) (L Version)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access.
- Two hardware triggers or breakpoints on CPU register write access.
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints.
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

## 6.13 Input/Output Diagrams

### 6.13.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

图 6-3 shows the port diagram. 表 6-16 summarizes the selection of the port function.

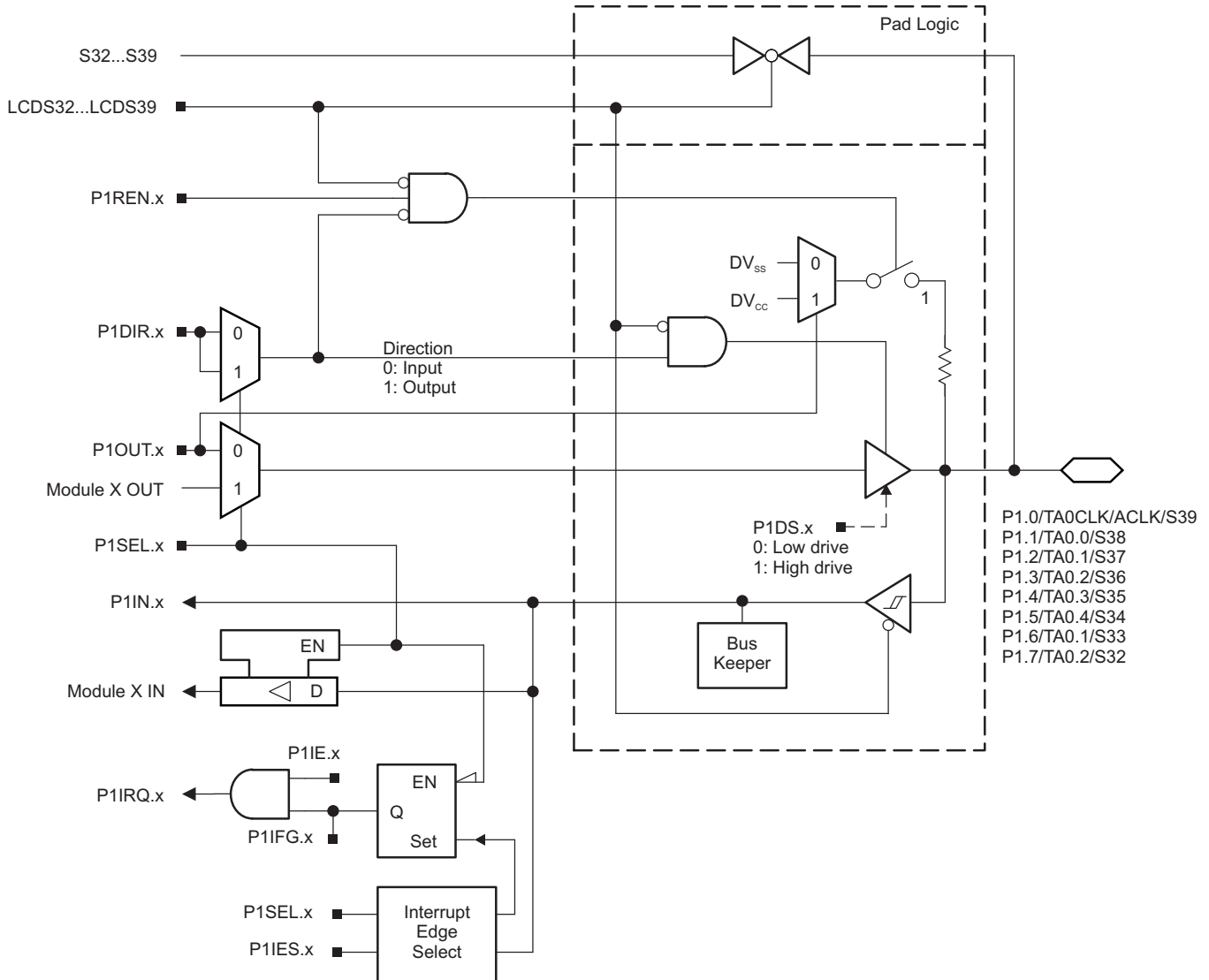


图 6-3. Port P1 (P1.0 to P1.7) Diagram

**表 6-16. Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x)      | x | FUNCTION                      | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |                  |
|----------------------|---|-------------------------------|----------------------------------------|---------|------------------|
|                      |   |                               | P1DIR.x                                | P1SEL.x | LCDS32 to LCDS39 |
| P1.0/TA0CLK/ACLK/S39 | 0 | P1.0 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.TA0CLK              | 0                                      | 1       | 0                |
|                      |   | ACLK                          | 1                                      | 1       | 0                |
|                      |   | S39                           | X                                      | X       | 1                |
| P1.1/TA0.0/S38       | 1 | P1.1 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI0A capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.0 output            | 1                                      | 1       | 0                |
|                      |   | S38                           | X                                      | X       | 1                |
| P1.2/TA0.1/S37       | 2 | P1.2 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI1A capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.1 output            | 1                                      | 1       | 0                |
|                      |   | S37                           | X                                      | X       | 1                |
| P1.3/TA0.2/S36       | 3 | P1.3 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI2A capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.2 output            | 1                                      | 1       | 0                |
|                      |   | S36                           | X                                      | X       | 1                |
| P1.4/TA0.3/S35       | 4 | P1.4 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI3A capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.3 output            | 1                                      | 1       | 0                |
|                      |   | S35                           | X                                      | X       | 1                |
| P1.5/TA0.4/S34       | 5 | P1.5 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI4A capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.4 output            | 1                                      | 1       | 0                |
|                      |   | S34                           | X                                      | X       | 1                |
| P1.6/TA0.1/S33       | 6 | P1.6 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI1B capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.1 output            | 1                                      | 1       | 0                |
|                      |   | S33                           | X                                      | X       | 1                |
| P1.7/TA0.2/S32       | 7 | P1.7 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                      |   | Timer TA0.CCI2B capture input | 0                                      | 1       | 0                |
|                      |   | Timer TA0.2 output            | 1                                      | 1       | 0                |
|                      |   | S32                           | X                                      | X       | 1                |

(1) X = Don't care

### 6.13.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

图 6-4 shows the port diagram. 表 6-17 summarizes the selection of the port function.

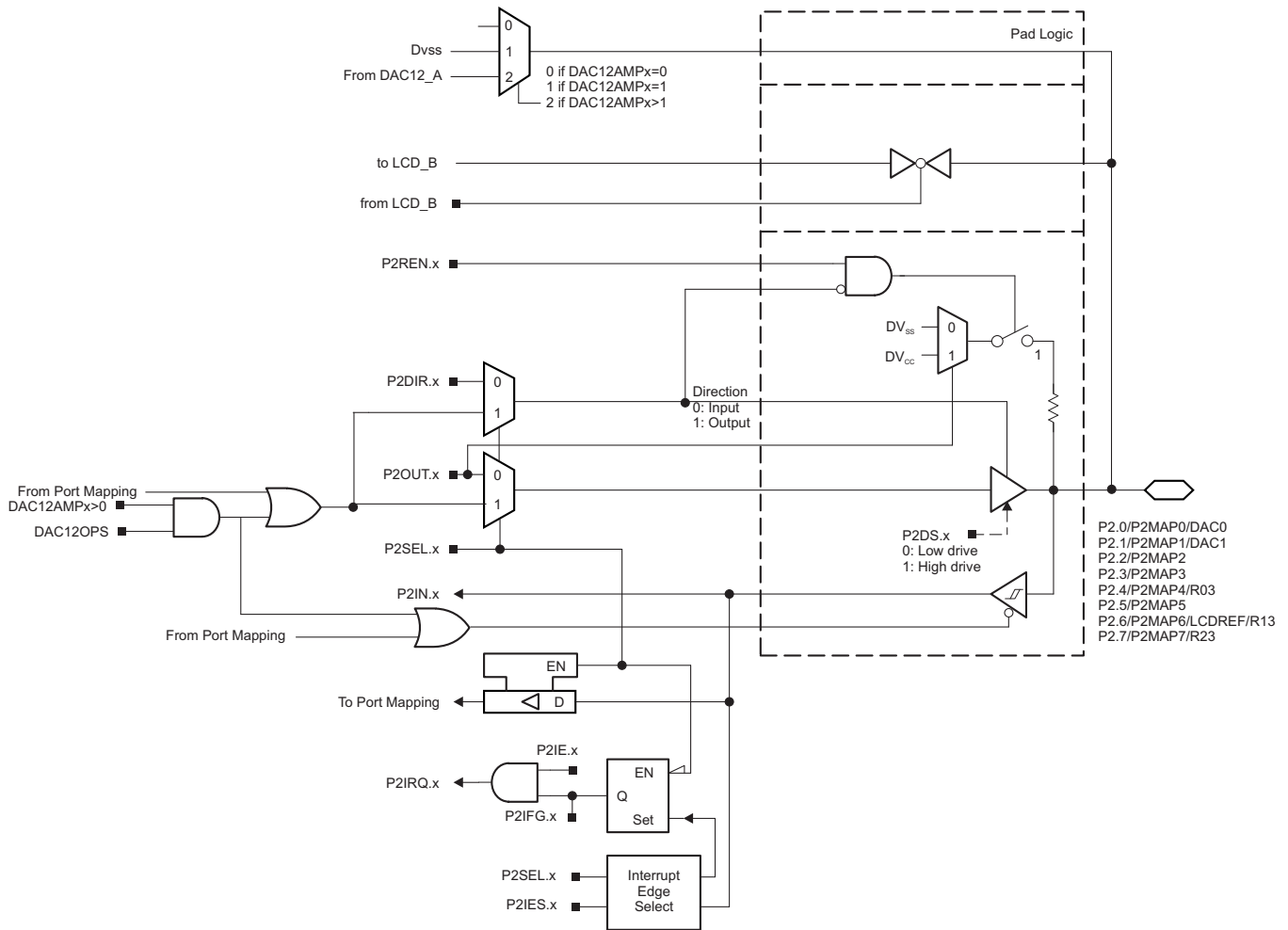


图 6-4. Port P2 (P2.0 to P2.7) Diagram

**表 6-17. Port P2 (P2.0 to P2.7) Pin Functions**

| PIN NAME (P2.x)        | x | FUNCTION                          | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |        |          |           |
|------------------------|---|-----------------------------------|----------------------------------------|---------|--------|----------|-----------|
|                        |   |                                   | P2DIR.x                                | P2SEL.x | P2MAPx | DAC12OPS | DAC12AMPx |
| P2.0/P2MAP0/DAC0       | 0 | P2.0 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
|                        |   | DAC0                              | X                                      | X       | = 31   | 1        | >1        |
| P2.1/P2MAP1/DAC1       | 1 | P2.1 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
|                        |   | DAC1                              | X                                      | X       | = 31   | 1        | >1        |
| P2.2/P2MAP2            | 2 | P2.2 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
| P2.3/P2MAP3            | 3 | P2.3 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
| P2.4/P2MAP4/R03        | 4 | P2.4 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
|                        |   | R03                               | X                                      | 1       | = 31   | X        | 0         |
| P2.5/P2MAP5            | 5 | P2.5 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
| P2.6/P2MAP6/LCDREF/R13 | 6 | P2.6 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
|                        |   | LCDREF/R13                        | X                                      | 1       | = 31   | X        | 0         |
| P2.7/P2MAP7/R23        | 7 | P2.7 (I/O)                        | I: 0; O: 1                             | 0       |        | X        | 0         |
|                        |   | Mapped secondary digital function | X                                      | 1       | ≤ 19   | X        | 0         |
|                        |   | R23                               | X                                      | 1       | = 31   | X        | 0         |

(1) X = Don't care

### 6.13.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

图 6-5 shows the port diagram. 表 6-18 summarizes the selection of the port function.

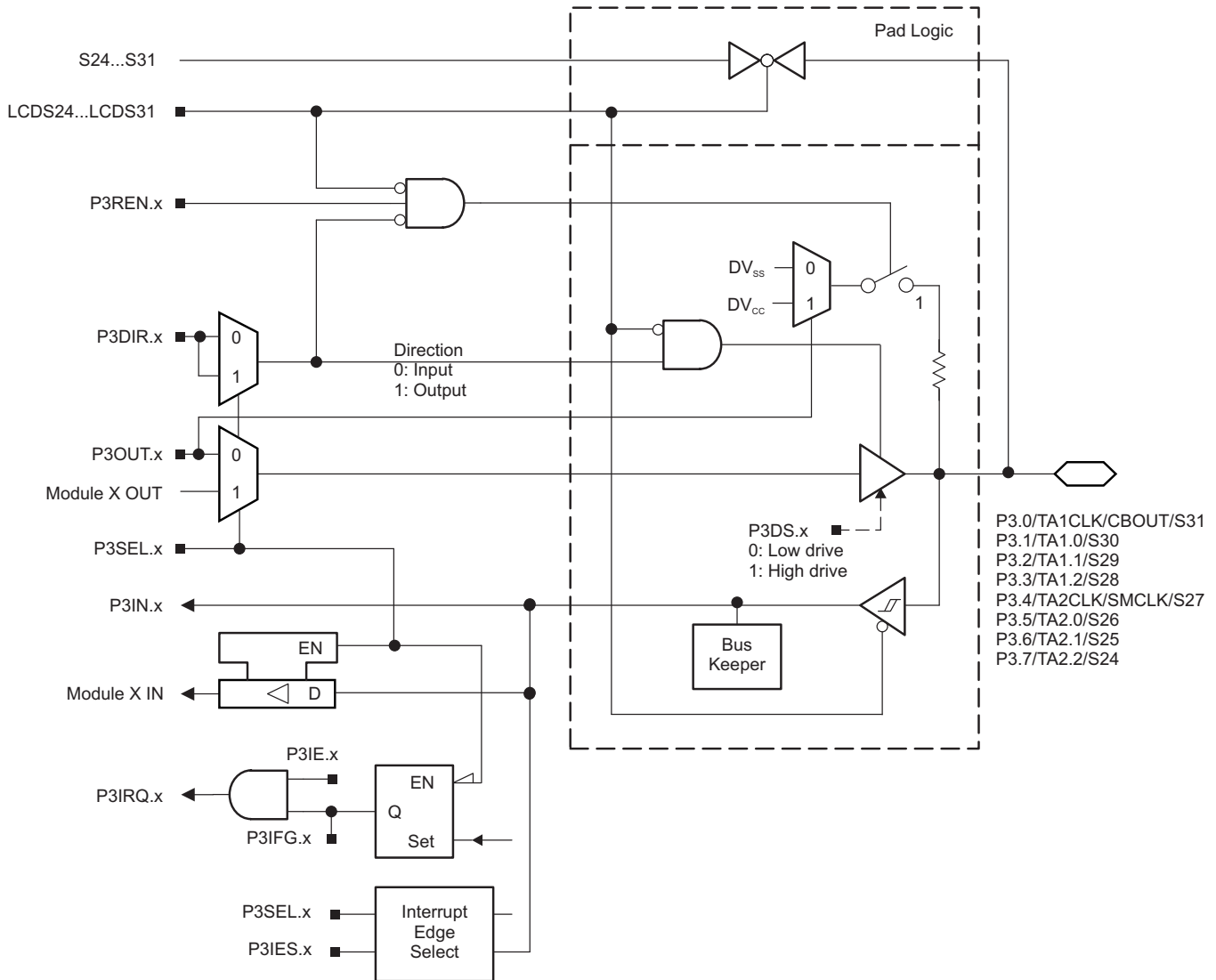


图 6-5. Port P3 (P3.0 to P3.7) Diagram

**表 6-18. Port P3 (P3.0 to P3.7) Pin Functions**

| PIN NAME (P3.x)       | x | FUNCTION                      | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |                  |
|-----------------------|---|-------------------------------|----------------------------------------|---------|------------------|
|                       |   |                               | P3DIR.x                                | P3SEL.x | LCDS24 to LCDS31 |
| P3.0/TA1CLK/CBOUT/S31 | 0 | P3.0 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA1.TA1CLK              | 0                                      | 1       | 0                |
|                       |   | CBOUT                         | 1                                      | 1       | 0                |
|                       |   | S31                           | X                                      | X       | 1                |
| P3.1/TA1.0/S30        | 1 | P3.1 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA1.CCI0A capture input | 0                                      | 1       | 0                |
|                       |   | Timer TA1.0 output            | 1                                      | 1       | 0                |
|                       |   | S30                           | X                                      | X       | 1                |
| P3.2/TA1.1/S29        | 2 | P3.2 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA1.CCI1A capture input | 0                                      | 1       | 0                |
|                       |   | Timer TA1.1 output            | 1                                      | 1       | 0                |
|                       |   | S29                           | X                                      | X       | 1                |
| P3.3/TA1.2/S28        | 3 | P3.3 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA1.CCI2A capture input | 0                                      | 1       | 0                |
|                       |   | Timer TA1.2 output            | 1                                      | 1       | 0                |
|                       |   | S28                           | X                                      | X       | 1                |
| P3.4/TA2CLK/SMCLK/S27 | 4 | P3.4 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA2.TA2CLK              | 0                                      | 1       | 0                |
|                       |   | SMCLK                         | 1                                      | 1       | 0                |
|                       |   | S27                           | X                                      | X       | 1                |
| P3.5/TA2.0/S26        | 5 | P3.5 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA2.CCI0A capture input | 0                                      | 1       | 0                |
|                       |   | Timer TA2.0 output            | 1                                      | 1       | 0                |
|                       |   | S26                           | X                                      | X       | 1                |
| P3.6/TA2.1/S25        | 6 | P3.6 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA2.CCI1A capture input | 0                                      | 1       | 0                |
|                       |   | Timer TA2.1 output            | 1                                      | 1       | 1                |
|                       |   | S25                           | X                                      | X       | 1                |
| P3.7/TA2.2/S24        | 7 | P3.7 (I/O)                    | I: 0; O: 1                             | 0       | 0                |
|                       |   | Timer TA2.CCI2A capture input | 0                                      | 1       | 0                |
|                       |   | Timer TA2.2 output            | 1                                      | 1       | 0                |
|                       |   | S24                           | X                                      | X       | 1                |

(1) X = Don't care

### 6.13.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

图 6-6 shows the port diagram. 表 6-19 summarizes the selection of the port function.

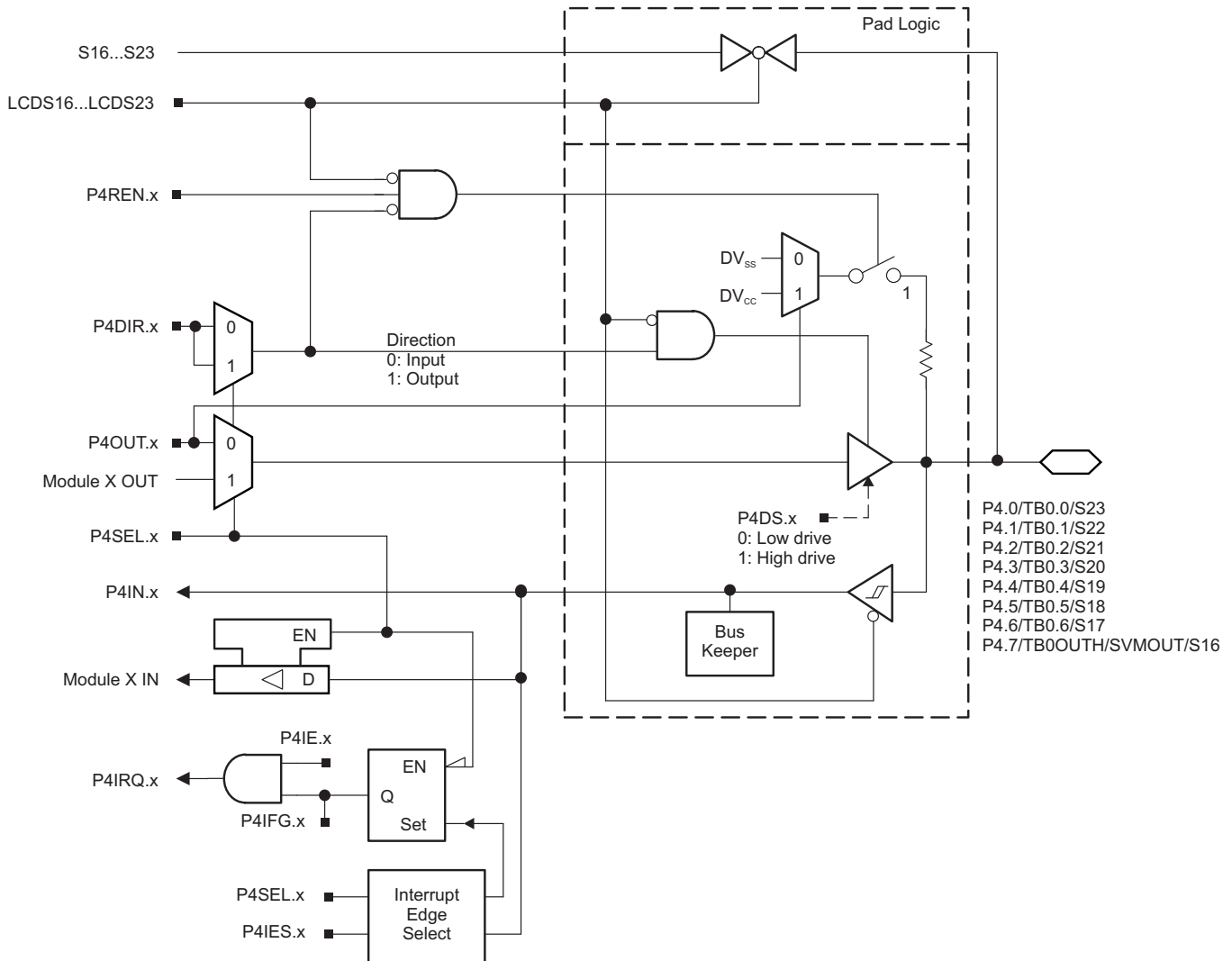


图 6-6. Port P4 (P4.0 to P4.7) Diagram

**表 6-19. Port P4 (P4.0 to P4.7) Pin Functions**

| PIN NAME (P4.x)          | x | FUNCTION                          | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |                  |
|--------------------------|---|-----------------------------------|----------------------------------------|---------|------------------|
|                          |   |                                   | P4DIR.x                                | P4SEL.x | LCDS16 to LCDS23 |
| P4.0/TB0.0/S23           | 0 | P4.0 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI0A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.0 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S23                               | X                                      | X       | 1                |
| P4.1/TB0.1/S22           | 1 | P4.1 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI1A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.1 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S22                               | X                                      | X       | 1                |
| P4.2/TB0.2/S21           | 2 | P4.2 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI2A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.2 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S21                               | X                                      | X       | 1                |
| P4.3/TB0.3/S20           | 3 | P4.3 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI3A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.3 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S20                               | X                                      | X       | 1                |
| P4.4/TB0.4/S19           | 4 | P4.4 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI4A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.4 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S19                               | X                                      | X       | 1                |
| P4.5/TB0.5/S18           | 5 | P4.5 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI5A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.5 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S18                               | X                                      | X       | 1                |
| P4.6/TB0.6/S17           | 6 | P4.6 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.CCI6A capture input     | 0                                      | 1       | 0                |
|                          |   | Timer TB0.6 output <sup>(2)</sup> | 1                                      | 1       | 0                |
|                          |   | S17                               | X                                      | X       | 1                |
| P4.7/TB0OUTH/ SVMOUT/S16 | 7 | P4.7 (I/O)                        | I: 0; O: 1                             | 0       | 0                |
|                          |   | Timer TB0.TB0OUTH                 | 0                                      | 1       | 0                |
|                          |   | SVMOUT                            | 1                                      | 1       | 0                |
|                          |   | S16                               | X                                      | X       | 1                |

(1) X = Don't care

(2) Setting TB0OUTH causes all Timer\_B configured outputs to be set to high impedance.

### 6.13.5 Port P5 (P5.0) Input/Output With Schmitt Trigger

图 6-7 shows the port diagram. 表 6-20 summarizes the selection of the port function.

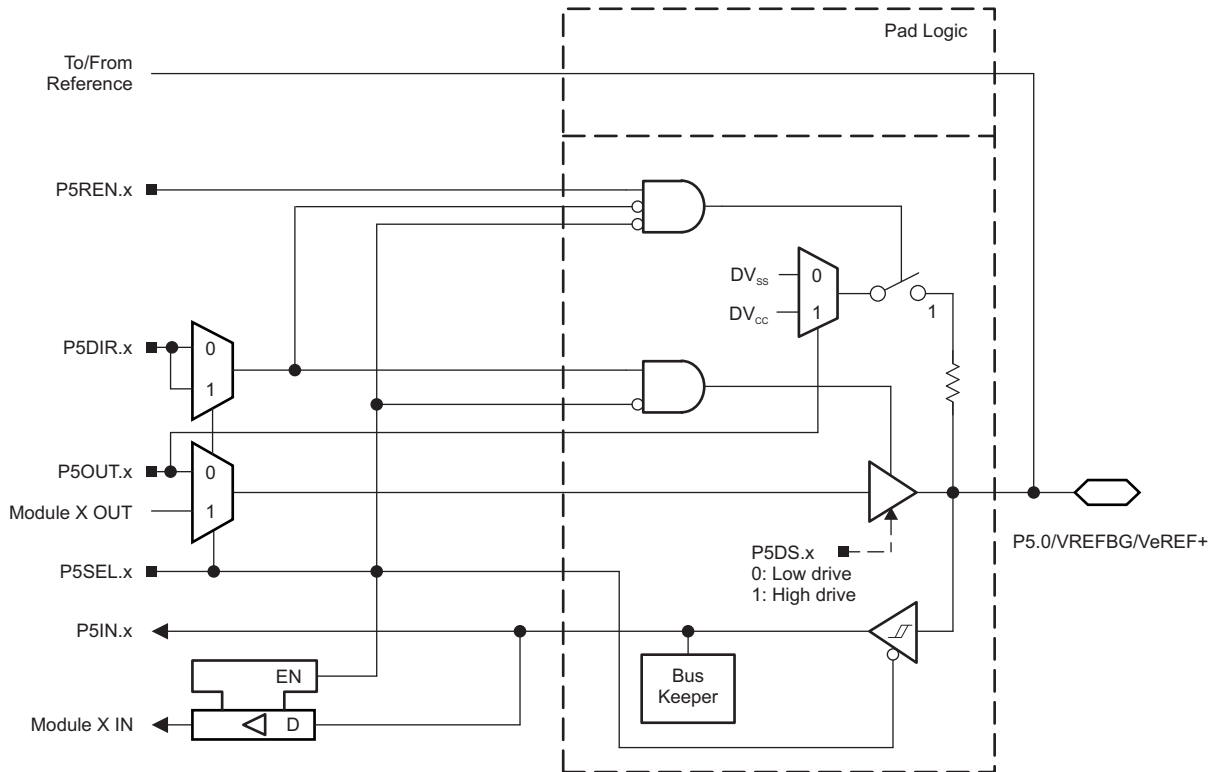


图 6-7. Port P5 (P5.0) Diagram

表 6-20. Port P5 (P5.0) Pin Functions

| PIN NAME (P5.x)    | x | FUNCTION                  | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |        |                      |                           |
|--------------------|---|---------------------------|----------------------------------------|---------|--------|----------------------|---------------------------|
|                    |   |                           | P5DIR.x                                | P5SEL.x | REFOUT | REFON <sup>(2)</sup> | CTSD16REFS <sup>(3)</sup> |
| P5.0/VREFBG/VeREF+ | 0 | P5.0 (I/O) <sup>(4)</sup> | I: 0; O: 1                             | 0       | X      | X                    | X                         |
|                    |   | VeREF+ <sup>(5)</sup>     | X                                      | 1       | 0      | X                    | 0                         |
|                    |   | VREFBG <sup>(6)</sup>     | X                                      | 1       | 1      | 1                    | 1                         |

(1) X = Don't care

(2) If a module is requesting a reference then REFON need not be set to 1 for VREFBG to be selected on P5.0.

(3) If CTSD16 is active, this bit must be set as shown in the table. Otherwise if set to 1, it will force VREFBG to be selected regardless of REFOUT setting and if P5SEL.x is set to 0 it will cause possible contention on the I/O.

(4) Default condition

(5) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the CTSD16 or DAC.

(6) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The internal reference voltage signal, VREFBG, is available at the pin.

### 6.13.6 Port P5 (P5.1 and P5.6) Input/Output With Schmitt Trigger

图 6-8 shows the port diagram. 表 6-21 summarizes the selection of the port function.

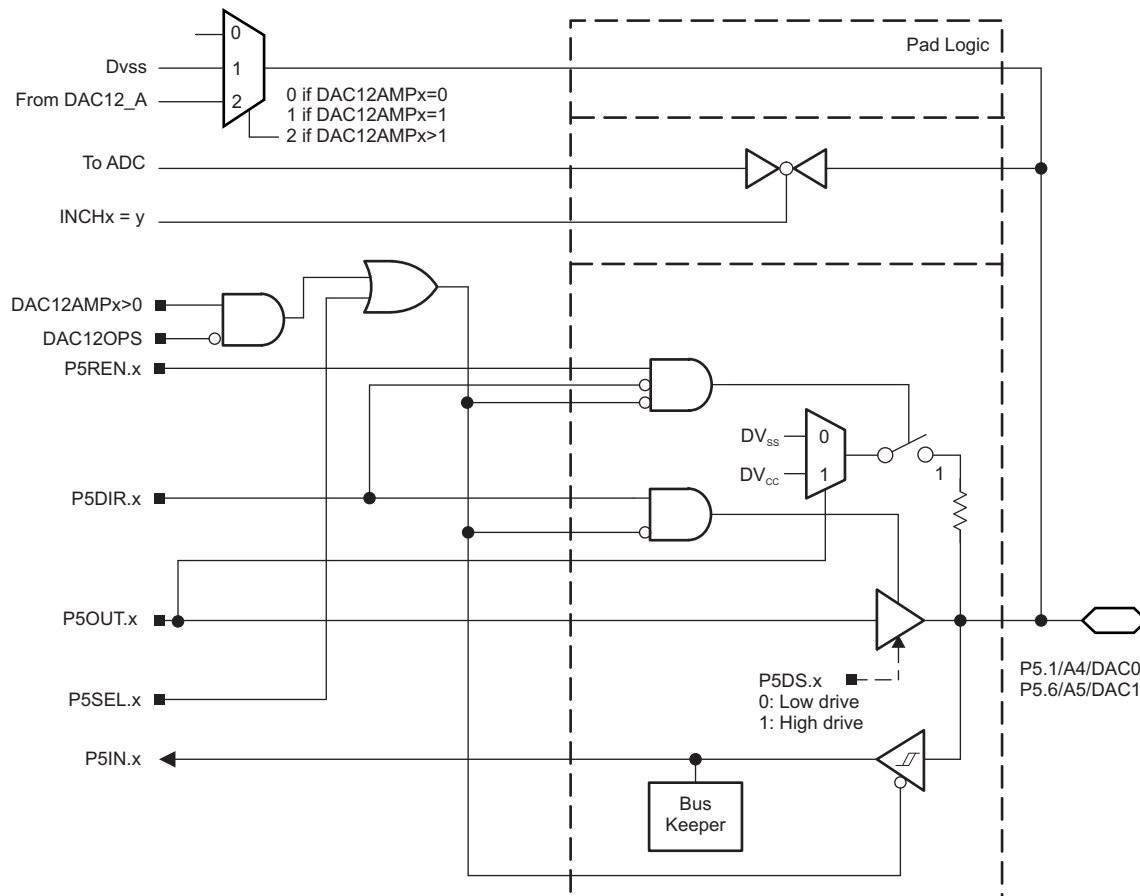


图 6-8. Port P5 (P5.1 and P5.6) Diagram

**表 6-21. Port P5 (P5.1 and P5.6) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION              | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |          |           |
|-----------------|---|-----------------------|----------------------------------------|---------|----------|-----------|
|                 |   |                       | P5DIR.x                                | P5SEL.x | DAC12OPS | DAC12AMPx |
| P5.1/A4/DAC0    | 1 | P5.1(I/O)             | I: 0; O: 1                             | 0       | X        | 0         |
|                 |   | A4 <sup>(2)</sup> (3) | X                                      | 1       | X        | 0         |
|                 |   | DAC0                  | X                                      | X       | 0        | >1        |
| P5.6/A5/DAC1    | 1 | P5.6(I/O)             | I: 0; O: 1                             | 0       | X        | 0         |
|                 |   | A5 <sup>(2)</sup> (3) | X                                      | 1       | X        | 0         |
|                 |   | DAC1                  | X                                      | X       | 0        | >1        |

(1) X = Don't care

(2) Setting the P5SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

### 6.13.7 Port P5 (P5.3 to P5.5, P5.7) Input/Output With Schmitt Trigger

图 6-9 shows the port diagram. 表 6-22 summarizes the selection of the port function.

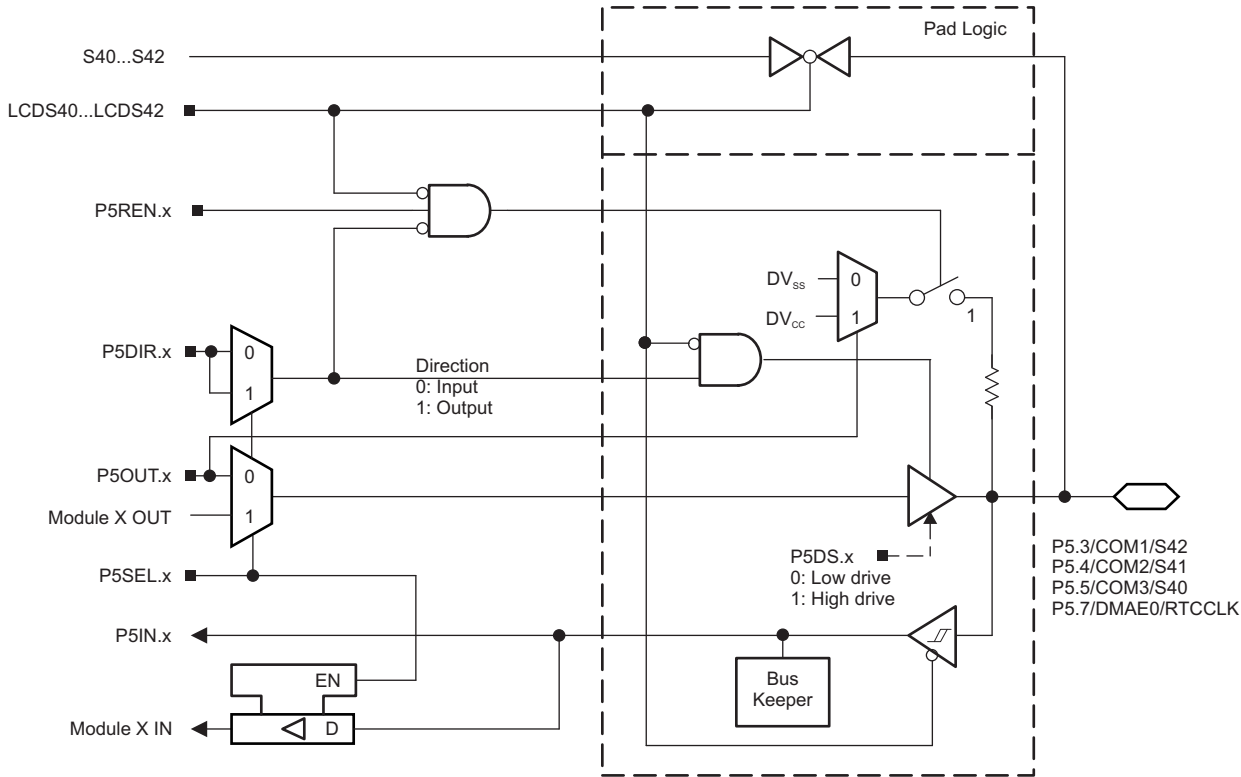


图 6-9. Port P5 (P5.3 to P5.5 and P5.7) Diagram

表 6-22. Port P5 (P5.3 to P5.5, P5.7) Pin Functions

| PIN NAME (P5.x)   | x | FUNCTION   | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |                  |
|-------------------|---|------------|----------------------------------------|---------|------------------|
|                   |   |            | P5DIR.x                                | P5SEL.x | LCDS40 to LCDS42 |
| P5.3/COM1/S42     | 3 | P5.3 (I/O) | I: 0; O: 1                             | 0       | 0                |
|                   |   | COM1       | X                                      | 1       | X                |
|                   |   | S42        | X                                      | 0       | 1                |
| P5.4/COM2/S41     | 4 | P5.4 (I/O) | I: 0; O: 1                             | 0       | 0                |
|                   |   | COM2       | X                                      | 1       | X                |
|                   |   | S41        | X                                      | 0       | 1                |
| P5.5/COM3/S40     | 5 | P5.5 (I/O) | I: 0; O: 1                             | 0       | 0                |
|                   |   | COM3       | X                                      | 1       | X                |
|                   |   | S40        | X                                      | 0       | 1                |
| P5.7/DMAE0/RTCCLK | 7 | P5.7 (I/O) | I: 0; O: 1                             | 0       | na               |
|                   |   | DMAE0      | 0                                      | 1       | na               |
|                   |   | RTCCLK     | 1                                      | 1       | na               |

(1) X = Don't care

### 6.13.8 Port P6 (P6.0 to P6.1) Input/Output With Schmitt Trigger

图 6-10 shows the port diagram. 表 6-23 summarizes the selection of the port function.

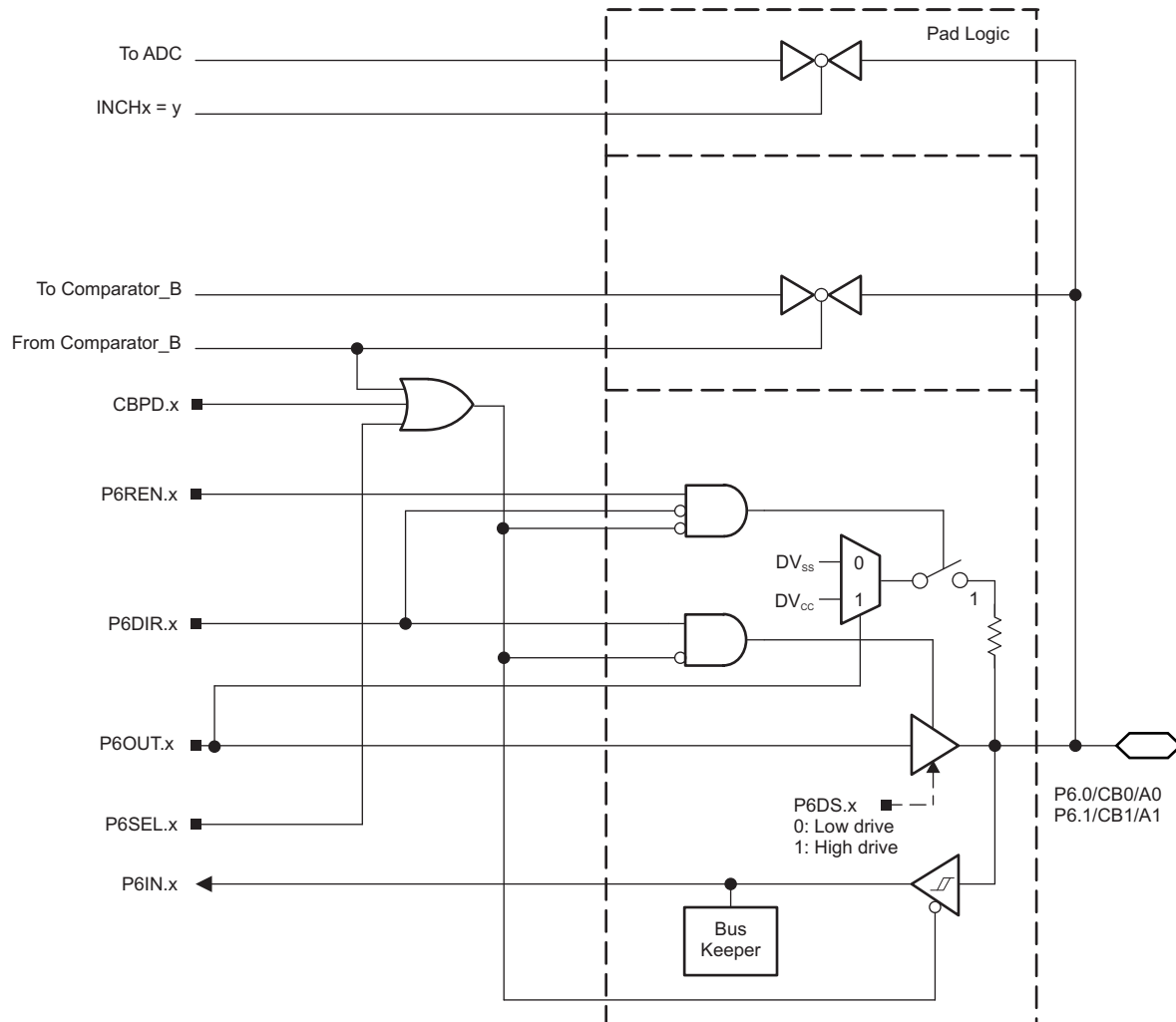


图 6-10. Port P6 (P6.0 to P6.1) Diagram

表 6-23. Port P6 (P6.0 to P6.1) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION              | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |        |
|-----------------|---|-----------------------|----------------------------------------|---------|--------|
|                 |   |                       | P6DIR.x                                | P6SEL.x | CBPD.x |
| P6.0/CB0/A0     | 0 | P6.0 (I/O)            | I: 0; O: 1                             | 0       | 0      |
|                 |   | CB0                   | X                                      | X       | 1      |
|                 |   | A0 <sup>(2) (3)</sup> | X                                      | 1       | X      |
| P6.1/CB1/A1     | 1 | P6.1 (I/O)            | I: 0; O: 1                             | 0       | 0      |
|                 |   | CB1                   | X                                      | X       | 1      |
|                 |   | A1 <sup>(2) (3)</sup> | X                                      | 1       | X      |

(1) X = Don't care

(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

### 6.13.9 Port P6 (P6.2 and P6.3) Input/Output With Schmitt Trigger

图 6-11 shows the port diagram. 表 6-24 summarizes the selection of the port function.

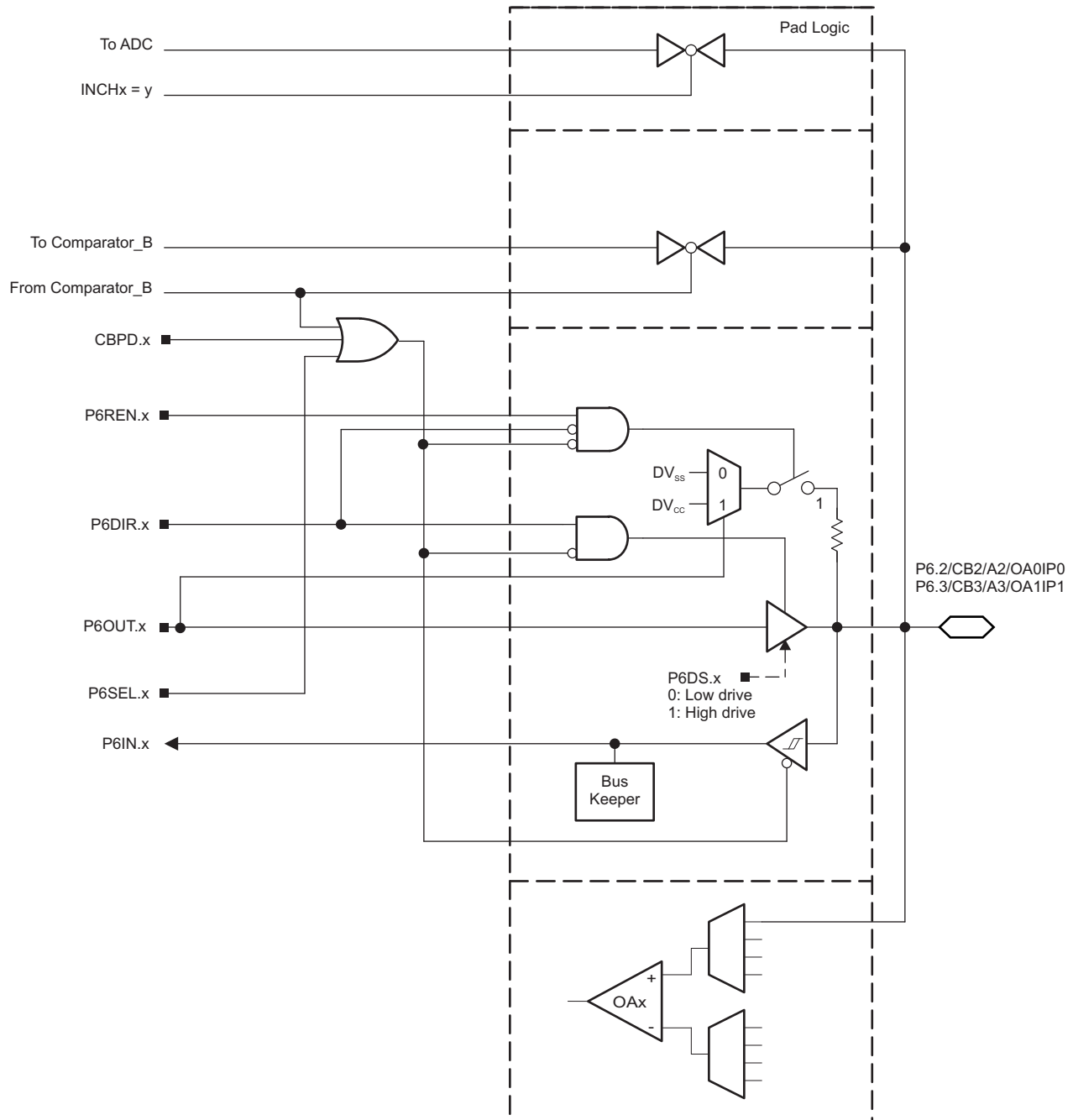


图 6-11. Port P6 (P6.2 and P6.3) Diagram

表 6-24. Port P6 (P6.2 and P6.3) Pin Functions

| PIN NAME (P6.x)    | x | FUNCTION              | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |
|--------------------|---|-----------------------|----------------------------------------|------------------------|-----------------------|
|                    |   |                       | P6DIR.x                                | P6SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> |
| P6.2/CB2/A2/OA0IP0 | 2 | P6.2 (I/O)            | I: 0; O: 1                             | 0                      | 0                     |
|                    |   | CB2                   | X                                      | X                      | 1                     |
|                    |   | A2 <sup>(3)</sup>     | X                                      | 1                      | X                     |
|                    |   | OA0IP0 <sup>(2)</sup> | X                                      | 1                      | X                     |
| P6.3/CB3/A3/OA1IP0 | 3 | P6.2 (I/O)            | I: 0; O: 1                             | 0                      | 0                     |
|                    |   | CB3                   | X                                      | X                      | 1                     |
|                    |   | A3 <sup>(4)</sup>     | X                                      | 1                      | X                     |
|                    |   | OA1IP0 <sup>(2)</sup> | X                                      | 1                      | X                     |

(1) X = Don't care

(2) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

(4) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

### 6.13.10 Port P6 (P6.4) Input/Output With Schmitt Trigger

图 6-12 shows the port diagram. 表 6-25 summarizes the selection of the port function.

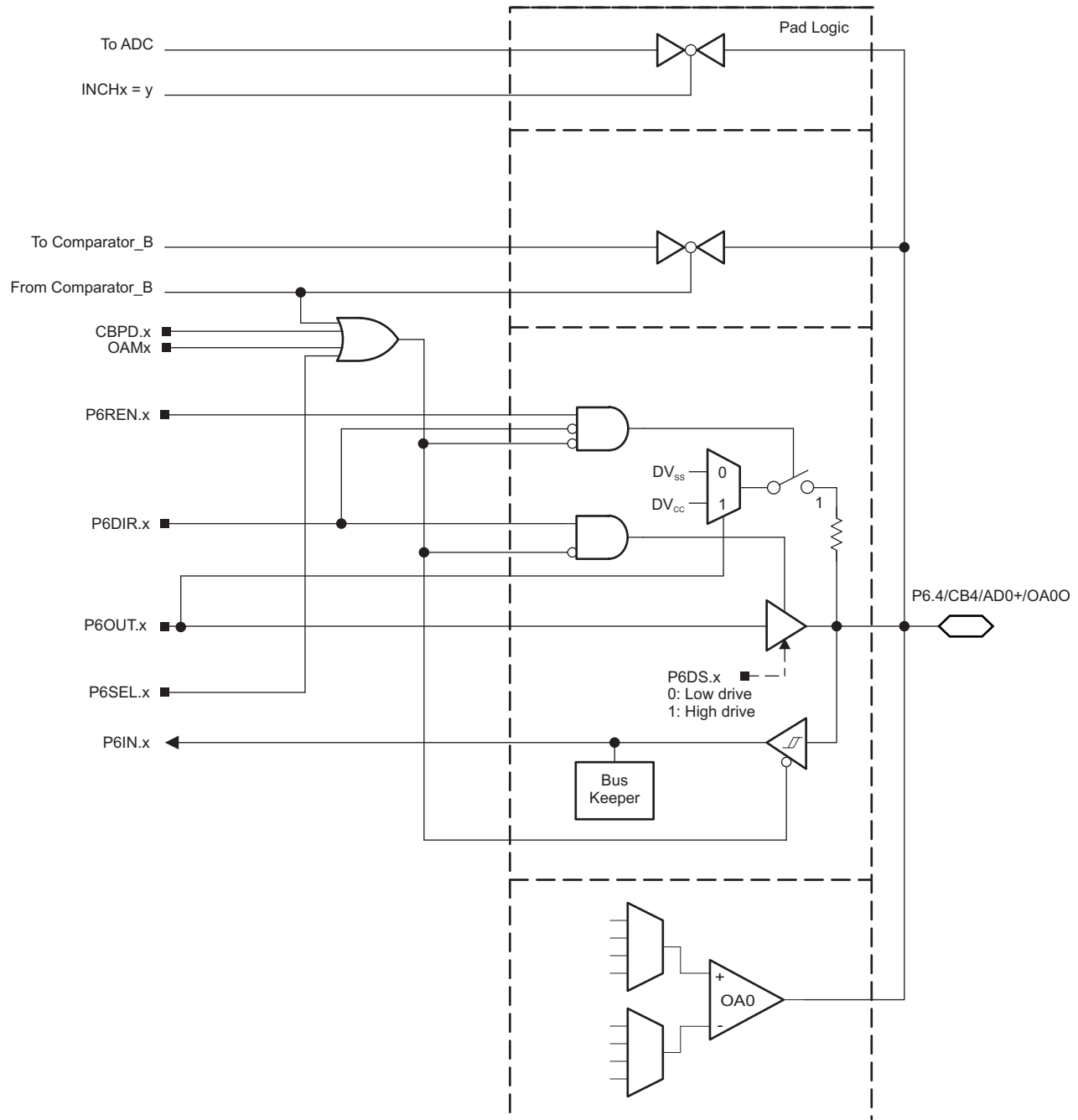


图 6-12. Port P6 (P6.4) Diagram

表 6-25. Port P6 (P6.4) Pin Functions

| PIN NAME (P6.x)    | x | FUNCTION            | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |                    |
|--------------------|---|---------------------|----------------------------------------|------------------------|-----------------------|--------------------|
|                    |   |                     | P6DIR.x                                | P6SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> | OAMx               |
| P6.4/CB4/AD0+/OA00 | 4 | P6.4 (I/O)          | I: 0; O: 1                             | 0                      | 0                     | 0 <sup>(3)</sup>   |
|                    |   | CB4                 | X                                      | X                      | 1                     | 0 <sup>(3)</sup>   |
|                    |   | AD0+ <sup>(4)</sup> | X                                      | 1                      | X                     | 0 <sup>(3)</sup>   |
|                    |   | OA00                | X                                      | X                      | X                     | = 1 <sup>(3)</sup> |

- (1) X = Don't care
- (2) Setting the P6SEL.x bit, the CBPD.x bit, or the OAMx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) Setting OAMx = 0 disables the operational amplifier and its output is high impedance. Setting OAMx = 1 enables the operational amplifier output. Because the operational amplifier output is shared with the ADC channel, selection of the respective ADC channel allows for direct measurement of the output voltage of the amplifier.
- (4) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

### 6.13.11 Port P6 (P6.5) Input/Output With Schmitt Trigger

图 6-13 shows the port diagram. 表 6-26 summarizes the selection of the port function.

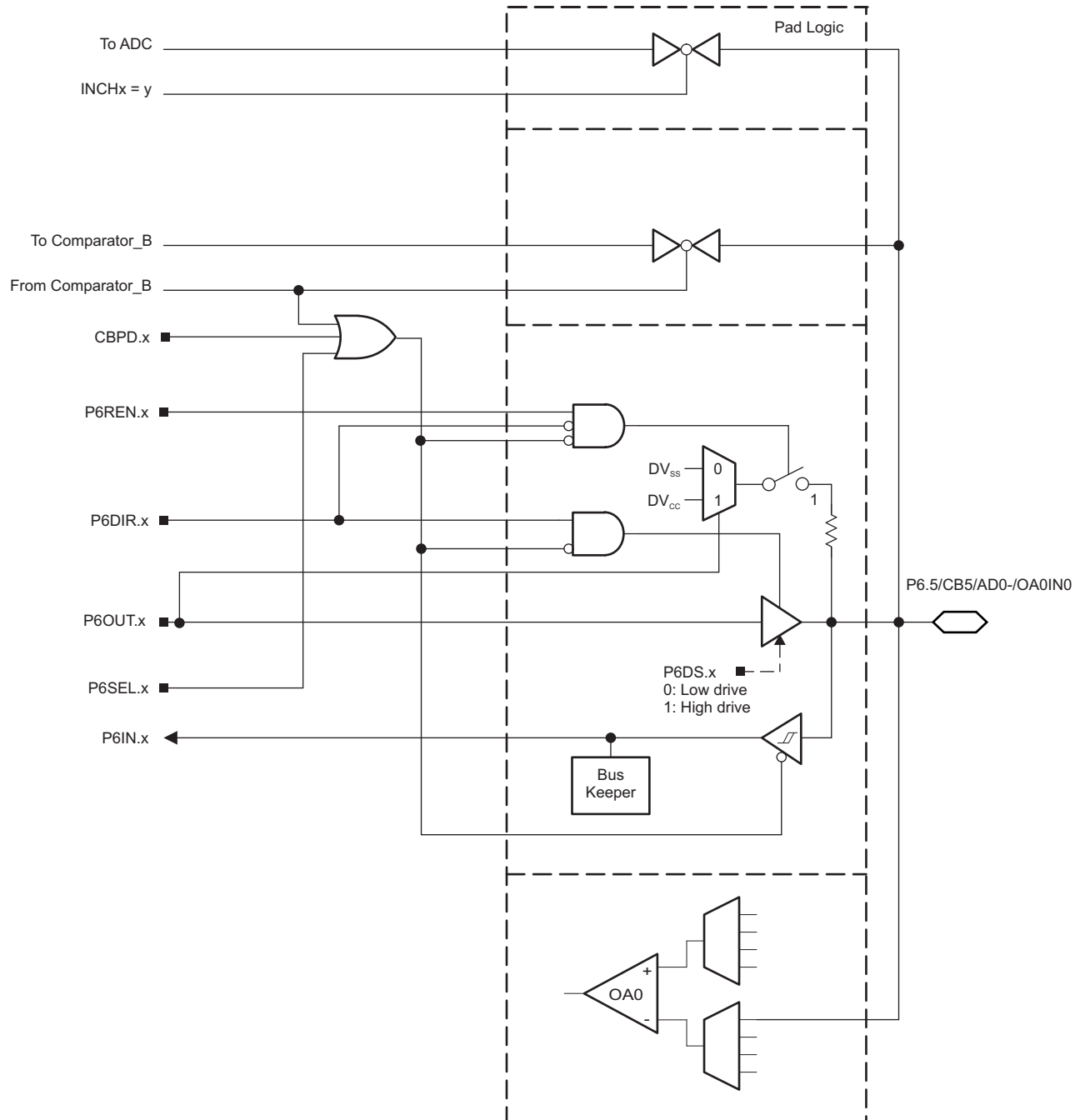


图 6-13. Port P6 (P6.5) Diagram

表 6-26. Port P6 (P6.5) Pin Functions

| PIN NAME (P6.x)      | x | FUNCTION              | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |
|----------------------|---|-----------------------|----------------------------------------|------------------------|-----------------------|
|                      |   |                       | P6DIR.x                                | P6SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> |
| P6.5/CB5/AD0-/OA0IN0 | 5 | P6.5 (I/O)            | I: 0; O: 1                             | 0                      | 0                     |
|                      |   | CB5                   | X                                      | X                      | 1                     |
|                      |   | AD0- <sup>(3)</sup>   | X                                      | 1                      | X                     |
|                      |   | OA0IN0 <sup>(4)</sup> | X                                      | 1                      | X                     |

- (1) X = Don't care  
 (2) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.  
 (3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.  
 (4) Setting the P6SEL.x bit or CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

### 6.13.12 Port P6 (P6.6) Input/Output With Schmitt Trigger

图 6-14 shows the port diagram. 表 6-27 summarizes the selection of the port function.

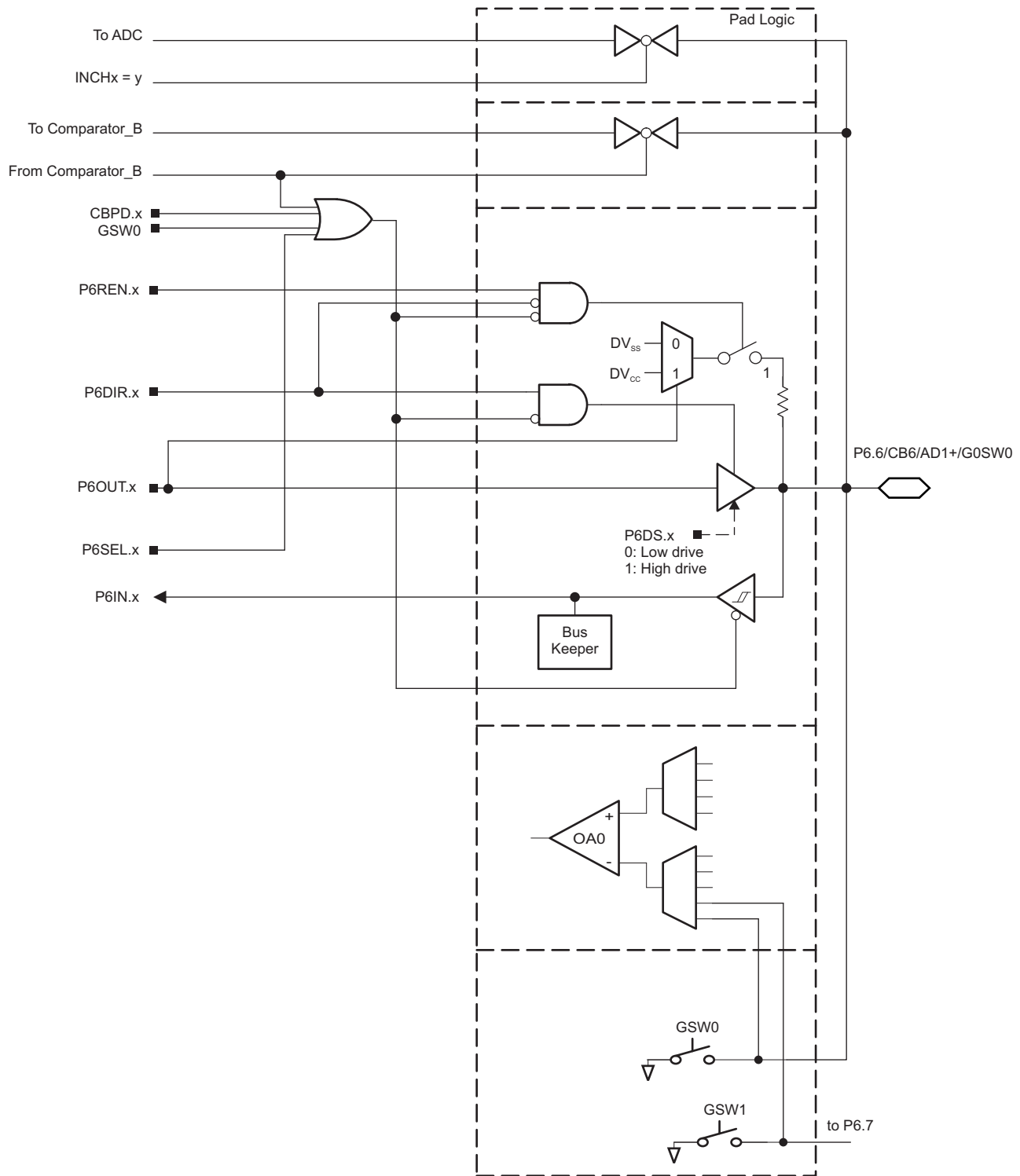


图 6-14. Port P6 (P6.6) Diagram

表 6-27. Port P6 (P6.6) Pin Functions

| PIN NAME (P6.x)     | x | FUNCTION             | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |                     |
|---------------------|---|----------------------|----------------------------------------|------------------------|-----------------------|---------------------|
|                     |   |                      | P6DIR.x                                | P6SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> | GSW0 <sup>(2)</sup> |
| P6.6/CB6/AD1+/G0SW0 | 6 | P6.6 (I/O)           | I: 0; O: 1                             | 0                      | 0                     | 0                   |
|                     |   | CB6                  | X                                      | X                      | 1                     | 0                   |
|                     |   | AD1+ <sup>(3)</sup>  | X                                      | 1                      | X                     | 0                   |
|                     |   | G0SW0 <sup>(4)</sup> | X                                      | X                      | X                     | 1                   |

(1) X = Don't care

(2) Setting the P6SEL.x bit, the CBPD.x bit, or the GSW0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

(4) Setting GSW0 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

### 6.13.13 Port P6 (P6.7) Input/Output With Schmitt Trigger

图 6-15 shows the port diagram. 表 6-28 summarizes the selection of the port function.

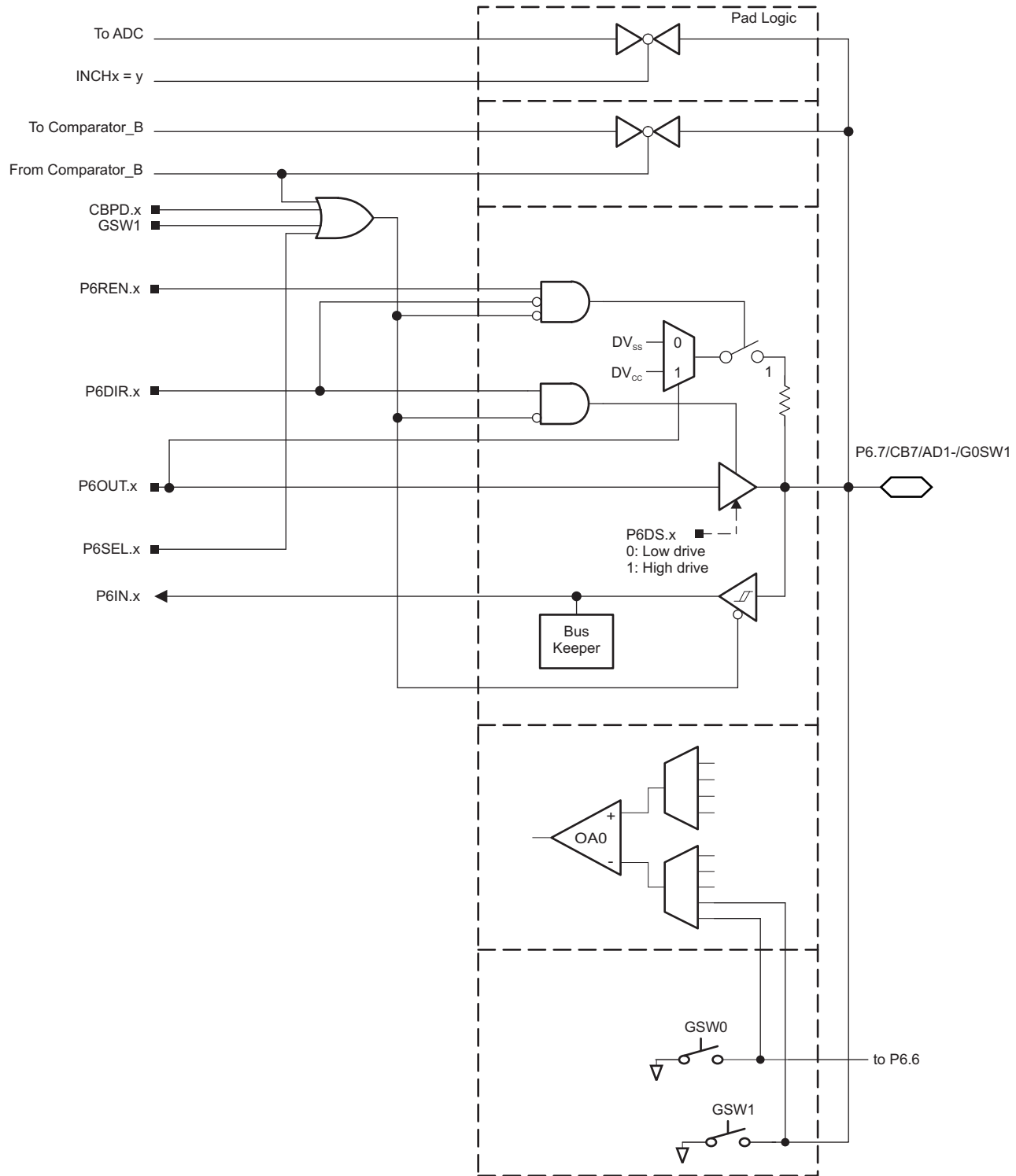


图 6-15. Port P6 (P6.7) Diagram

表 6-28. Port P6 (P6.7) Pin Functions

| PIN NAME (P6.x)     | x | FUNCTION             | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |                     |
|---------------------|---|----------------------|----------------------------------------|------------------------|-----------------------|---------------------|
|                     |   |                      | P6DIR.x                                | P6SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> | GSW1 <sup>(2)</sup> |
| P6.7/CB7/AD1-/G0SW1 | 7 | P6.7 (I/O)           | I: 0; O: 1                             | 0                      | 0                     | 0                   |
|                     |   | CB7                  | X                                      | X                      | 1                     | 0                   |
|                     |   | AD1- <sup>(3)</sup>  | X                                      | 1                      | X                     | 0                   |
|                     |   | G0SW1 <sup>(4)</sup> | X                                      | X                      | X                     | 1                   |

(1) X = Don't care

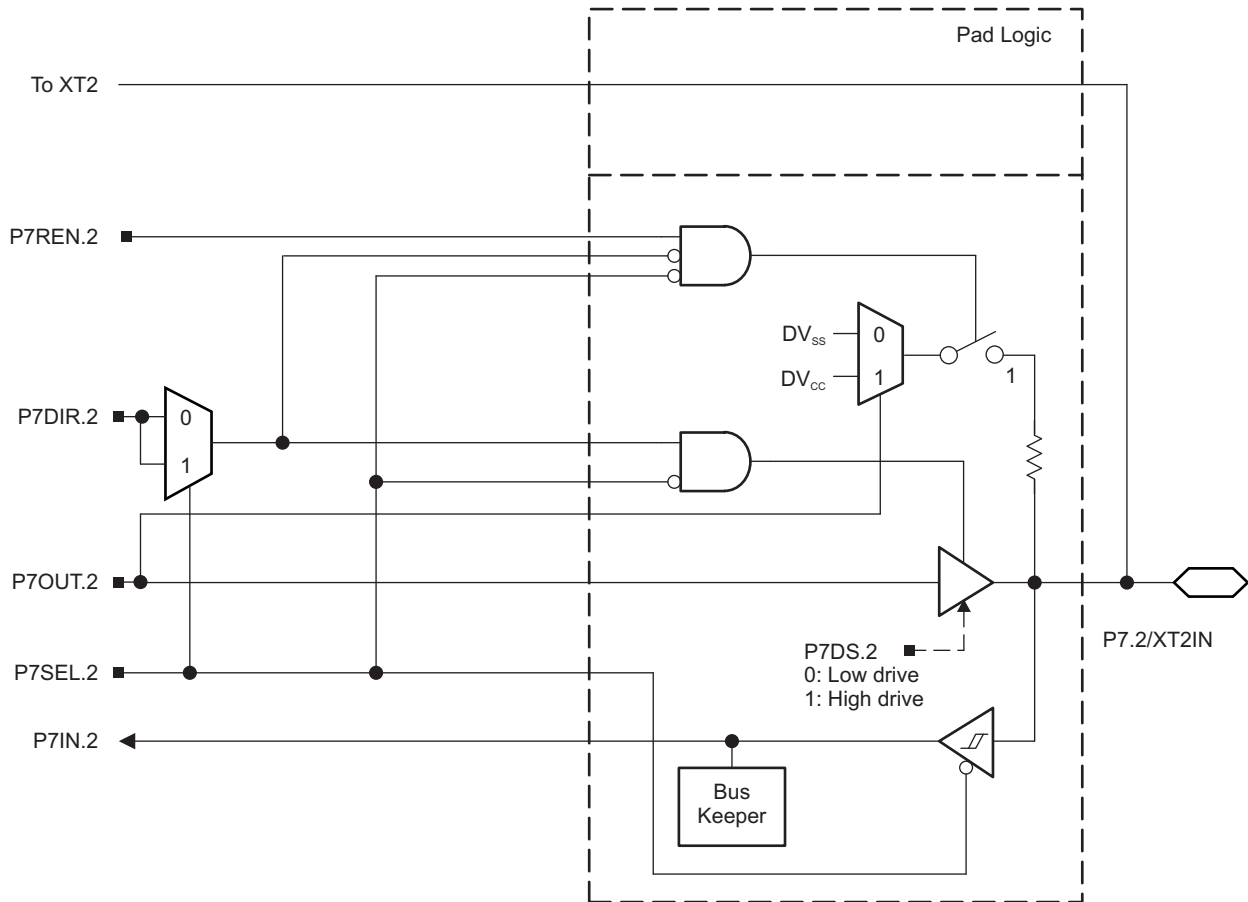
(2) Setting the P6SEL.x bit, the CBPD.x bit, or the GSW0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

(4) Setting GSW1 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

#### 6.13.14 Port P7 (P7.2 and P7.3) Input/Output With Schmitt Trigger

图 6-16 and 图 6-17 show the port diagrams. 表 6-29 summarizes the selection of the port function.



**图 6-16. Port P7 (P7.2) Diagram**

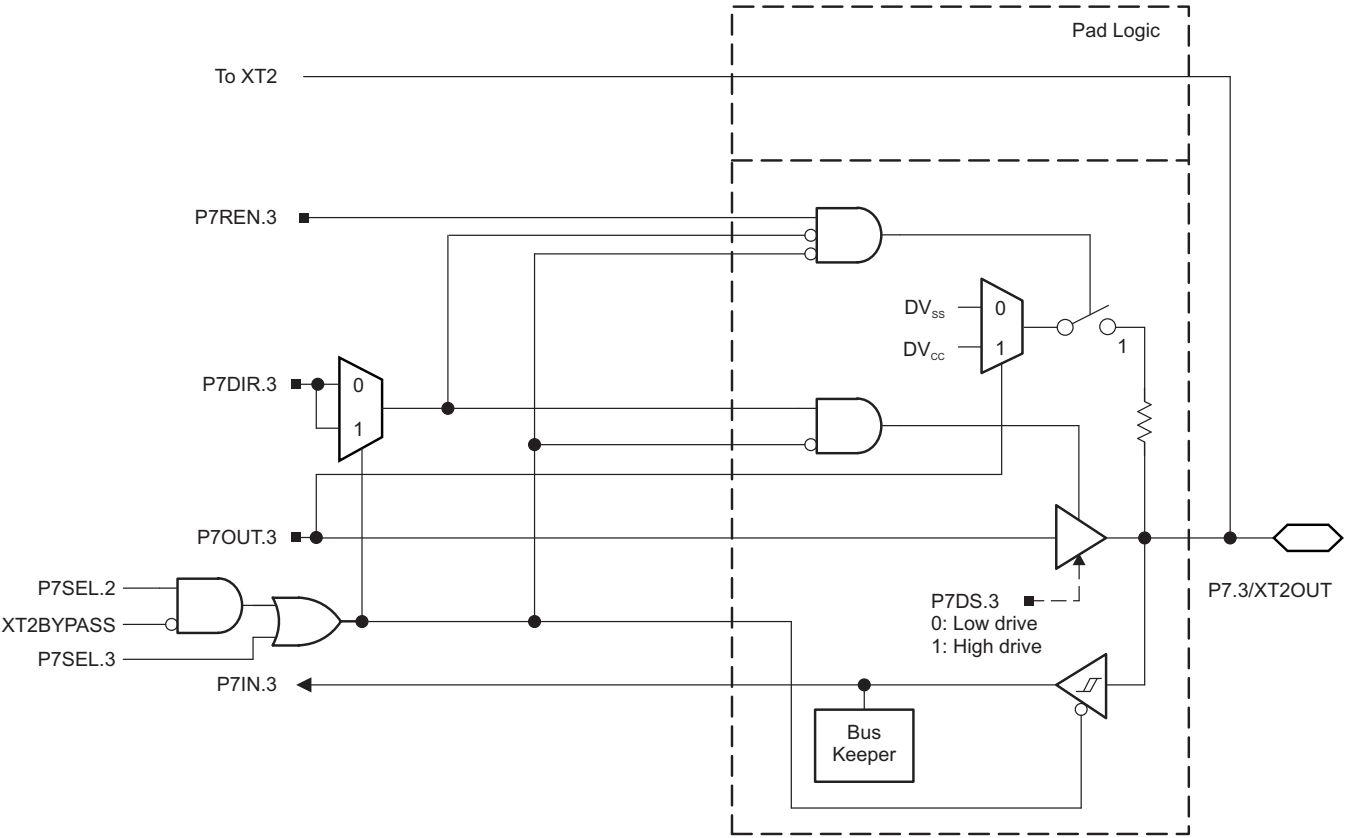


图 6-17. Port P7 (P7.3) Diagram

表 6-29. Port P7 (P7.2 and P7.3) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION                           | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |         |           |
|-----------------|---|------------------------------------|----------------------------------------|---------|---------|-----------|
|                 |   |                                    | P7DIR.x                                | P7SEL.2 | P7SEL.3 | XT2BYPASS |
| P7.2/XT2IN      | 2 | P7.2 (I/O)                         | I: 0; O: 1                             | 0       | X       | X         |
|                 |   | XT2IN crystal mode <sup>(2)</sup>  | X                                      | 1       | X       | 0         |
|                 |   | XT2IN bypass mode <sup>(2)</sup>   | X                                      | 1       | X       | 1         |
| P7.3/XT2OUT     | 3 | P7.3 (I/O)                         | I: 0; O: 1                             | 0       | X       | X         |
|                 |   | XT2OUT crystal mode <sup>(3)</sup> | X                                      | 1       | X       | 0         |
|                 |   | P7.3 (I/O) <sup>(3)</sup>          | X                                      | 1       | X       | 1         |

(1) X = Don't care  
(2) Setting P7SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P7.2 is configured for crystal mode or bypass mode.  
(3) Setting P7SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.3 can be used as general-purpose I/O.

### 6.13.15 Port P7 (P7.4) Input/Output With Schmitt Trigger

图 6-18 shows the port diagram. 表 6-30 summarizes the selection of the port function.

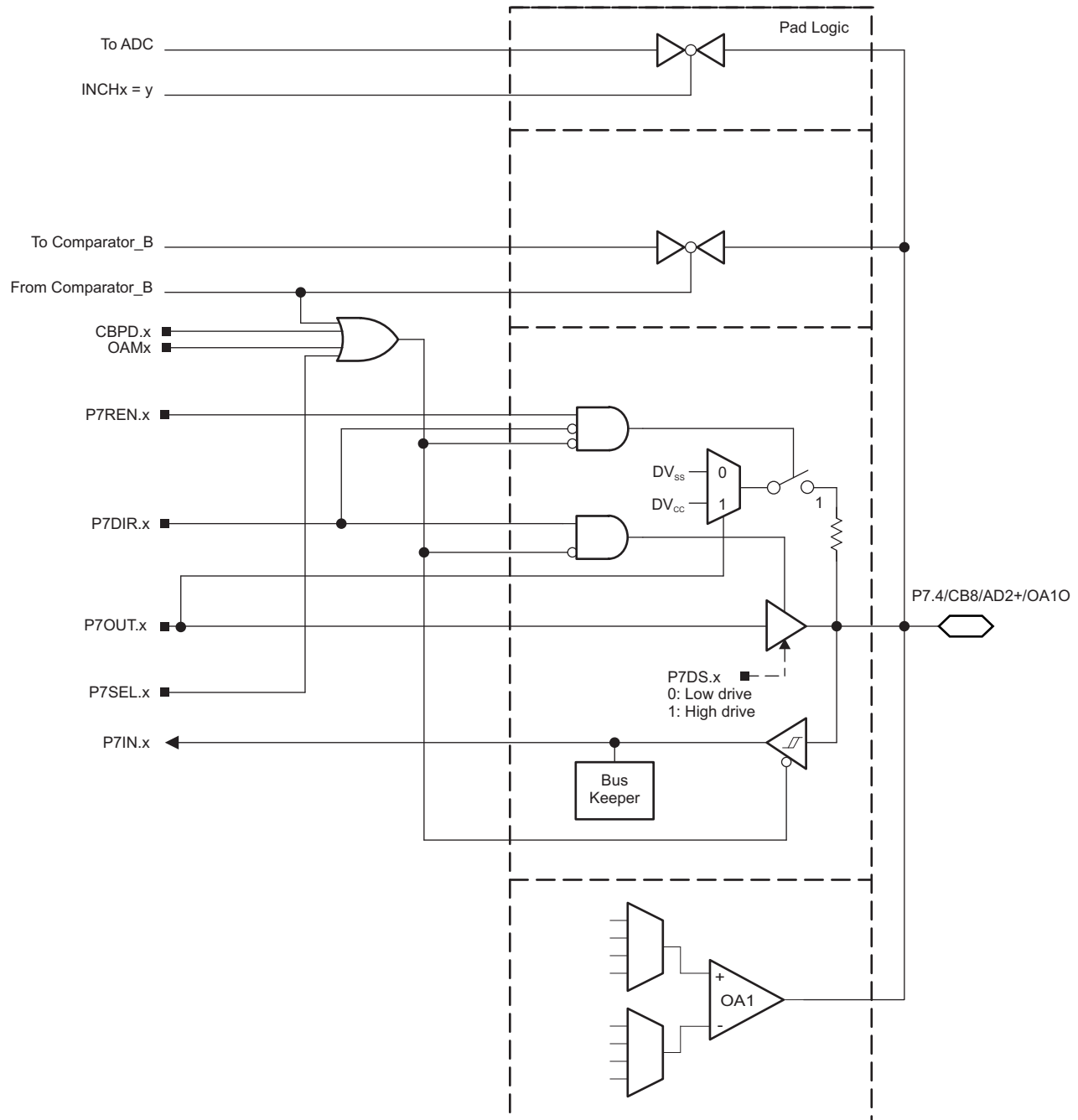


图 6-18. Port P7 (P7.4) Diagram

表 6-30. Port P7 (P7.4) Pin Functions

| PIN NAME (P6.x)    | x | FUNCTION            | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |                     |
|--------------------|---|---------------------|----------------------------------------|------------------------|-----------------------|---------------------|
|                    |   |                     | P6DIR.x                                | P7SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> | OAMx <sup>(2)</sup> |
| P7.4/CB8/AD2+/OA1O | 4 | P7.4 (I/O)          | I: 0; O: 1                             | 0                      | 0                     | 0 <sup>(3)</sup>    |
|                    |   | CB8                 | X                                      | X                      | 1                     | 0 <sup>(3)</sup>    |
|                    |   | AD2+ <sup>(4)</sup> | X                                      | 1                      | X                     | 0 <sup>(3)</sup>    |
|                    |   | OA1O                | X                                      | X                      | X                     | 1 <sup>(3)</sup>    |

(1) X = Don't care

(2) Setting the P6SEL.x bit, the CBPD.x bit, or the OAMx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Setting OAMx = 0 disables the operational amplifier and its output is high impedance. Setting OAMx = 1 enables the operational amplifier output. Because the operational amplifier output is shared with the ADC channel, selection of the respective ADC channel allows for direct measurement of the output voltage of the amplifier.

(4) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

### 6.13.16 Port P7 (P7.5) Input/Output With Schmitt Trigger

图 6-19 shows the port diagram. 表 6-31 summarizes the selection of the port function.

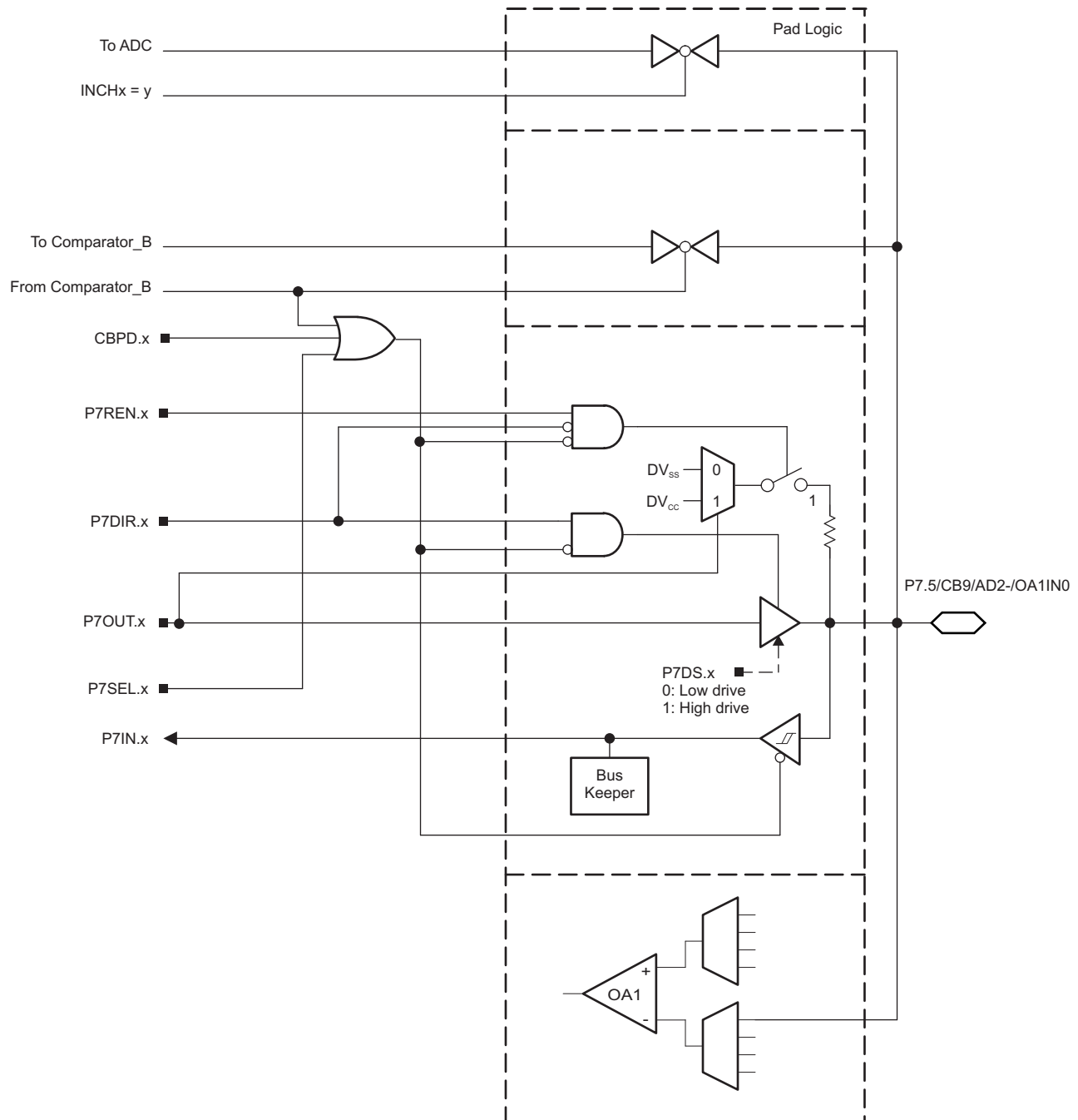


图 6-19. Port P7 (P7.5) Diagram

表 6-31. Port P7 (P7.5) Pin Functions

| PIN NAME (P7.x)     | x | FUNCTION             | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |
|---------------------|---|----------------------|----------------------------------------|------------------------|-----------------------|
|                     |   |                      | P7DIR.x                                | P7SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> |
| P7.5/CB9/AD2-/OAIN0 | 5 | P7.5 (I/O)           | I: 0; O: 1                             | 0                      | 0                     |
|                     |   | CB9                  | X                                      | X                      | 1                     |
|                     |   | AD2- <sup>(3)</sup>  | X                                      | 1                      | X                     |
|                     |   | OAIN0 <sup>(2)</sup> | X                                      | 1                      | X                     |

(1) X = Don't care

(2) Setting the P7SEL.x bit or the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

### 6.13.17 Port P7 (P7.6) Input/Output With Schmitt Trigger

图 6-20 shows the port diagram. 表 6-32 summarizes the selection of the port function.

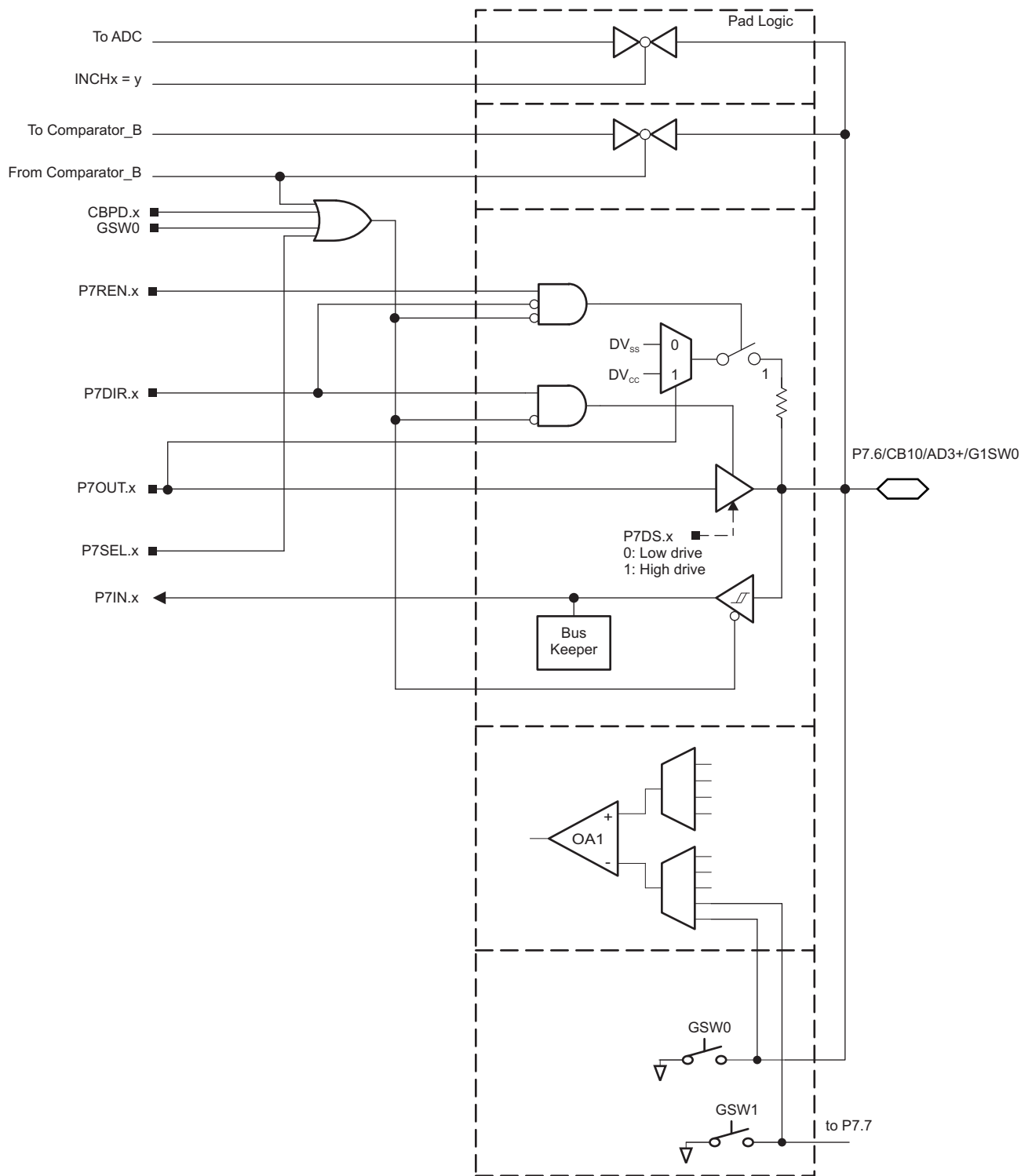


图 6-20. Port P7 (P7.6) Diagram

表 6-32. Port P7 (P7.6) Pin Functions

| PIN NAME (P7.x)      | x | FUNCTION             | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |                     |
|----------------------|---|----------------------|----------------------------------------|------------------------|-----------------------|---------------------|
|                      |   |                      | P6DIR.x                                | P7SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> | GSW0 <sup>(2)</sup> |
| P7.6/CB10/AD3+/G1SW0 | 6 | P7.6 (I/O)           | I: 0; O: 1                             | 0                      | 0                     | 0                   |
|                      |   | CB10                 | X                                      | X                      | 1                     | 0                   |
|                      |   | AD3+ <sup>(3)</sup>  | X                                      | 1                      | X                     | 0                   |
|                      |   | G1SW0 <sup>(4)</sup> | X                                      | X                      | X                     | 1                   |

(1) X = Don't care

(2) Setting the P7SEL.x bit, the CBPD.x bit, or the GSW0 disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

(4) Setting GSW0 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

### 6.13.18 Port P7 (P7.7) Input/Output With Schmitt Trigger

图 6-21 shows the port diagram. 表 6-33 summarizes the selection of the port function.

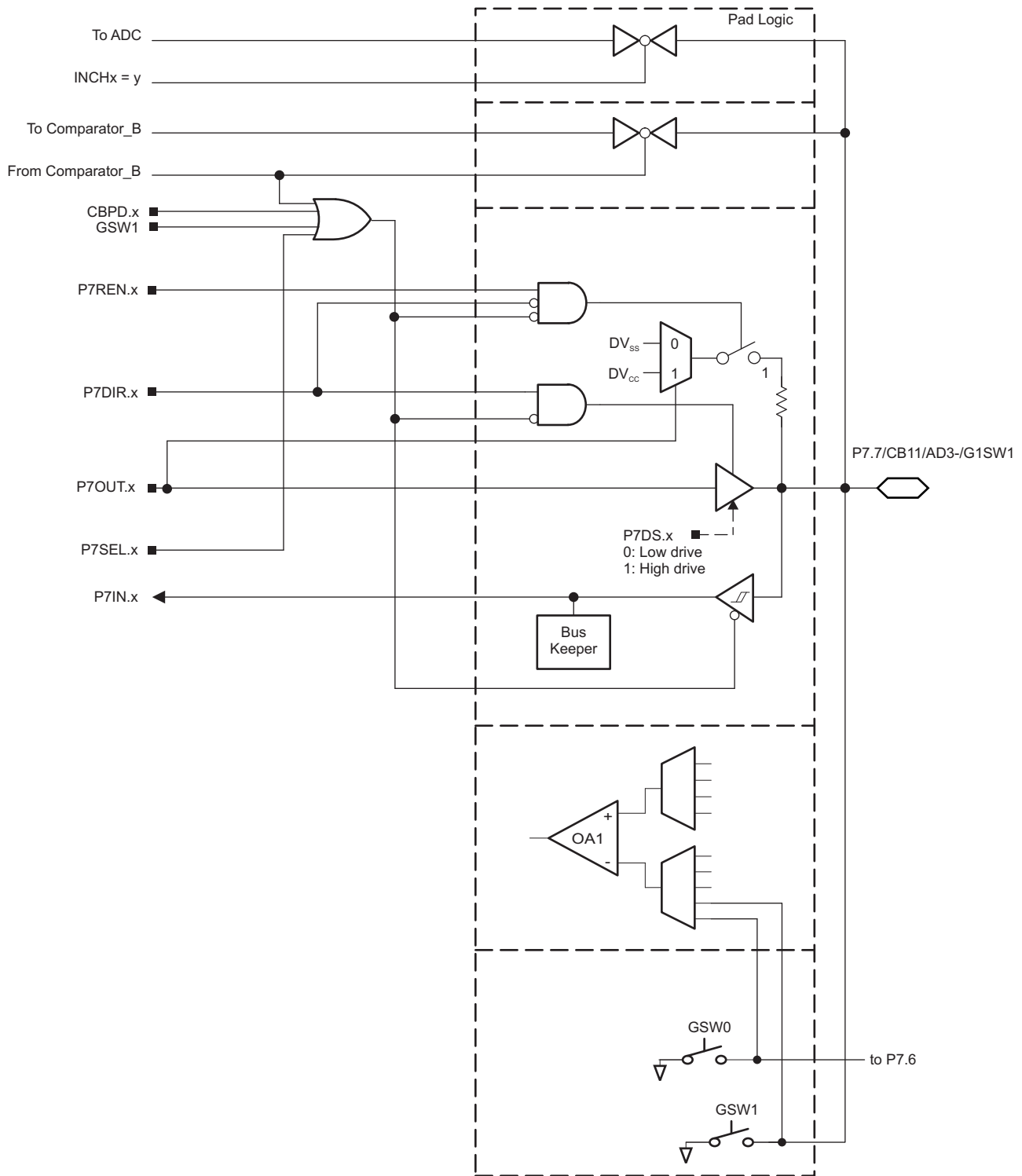


图 6-21. Port P7 (P7.7) Diagram

表 6-33. Port P7 (P7.7) Pin Functions

| PIN NAME (P7.x)      | x | FUNCTION             | CONTROL BITS OR SIGNALS <sup>(1)</sup> |                        |                       |                     |
|----------------------|---|----------------------|----------------------------------------|------------------------|-----------------------|---------------------|
|                      |   |                      | P6DIR.x                                | P7SEL.x <sup>(2)</sup> | CBPD.x <sup>(2)</sup> | GSW1 <sup>(2)</sup> |
| P7.7/CB11/AD3-/G1SW1 | 7 | P7.7 (I/O)           | I: 0; O: 1                             | 0                      | 0                     | 0                   |
|                      |   | CB11                 | X                                      | X                      | 1                     | 0                   |
|                      |   | AD3- <sup>(3)</sup>  | X                                      | 1                      | X                     | 0                   |
|                      |   | G1SW1 <sup>(4)</sup> | X                                      | X                      | X                     | 1                   |

(1) X = Don't care

(2) Setting the P7SEL.x bit, the CBPD.x bit, or the GSW1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) The ADC channel Ax is connected internally to AV<sub>SS</sub> if not selected by the respective INCHx bits.

(4) Setting GSW1 = 1 closes the switch and forces the pin to be switched to ground. All switches are independent of each other, so different settings can impose different voltages on the pin. Application must ensure there are no conflicts.

### 6.13.19 Port P8 (P8.0 to P8.7) Input/Output With Schmitt Trigger

图 6-22 shows the port diagram. 表 6-34 summarizes the selection of the port function.

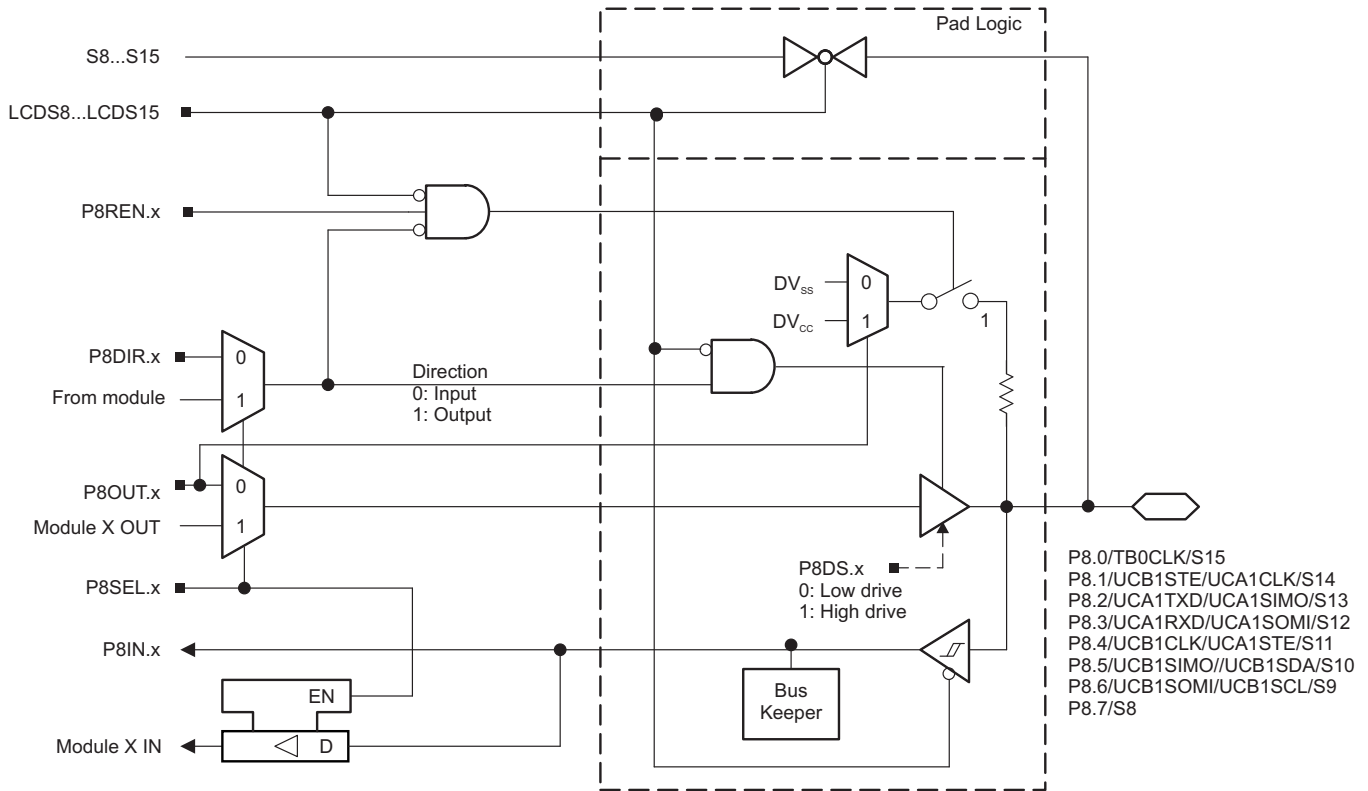


图 6-22. Port P8 (P8.0 to P8.7) Diagram

**表 6-34. Port P8 (P8.0 to P8.7) Pin Functions**

| PIN NAME (P9.x)           | x | FUNCTION                     | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |             |
|---------------------------|---|------------------------------|----------------------------------------|---------|-------------|
|                           |   |                              | P8DIR.x                                | P8SEL.x | LCDS8 to 16 |
| P8.0/TB0CLK/S15           | 0 | P8.0 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | Timer TB0.TB0CLK clock input | 0                                      | 1       | 0           |
|                           |   | S15                          | X                                      | X       | 1           |
| P8.1/UCB1STE/UCA1CLK/S14  | 1 | P8.1 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | UCB1STE/UCA1CLK              | X                                      | 1       | 0           |
|                           |   | S14                          | X                                      | X       | 1           |
| P8.2/UCA1TXD/UCA1SIMO/S13 | 2 | P8.2 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | UCA1TXD/UCA1SIMO             | X                                      | 1       | 0           |
|                           |   | S13                          | X                                      | X       | 1           |
| P8.3/UCA1RXD/UCA1SOMI/S12 | 3 | P8.3 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | UCA1RXD/UCA1SOMI             | X                                      | 1       | 0           |
|                           |   | S12                          | X                                      | X       | 1           |
| P8.4/UCB1CLK/UCA1STE/S11  | 4 | P8.4 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | UCB1CLK/UCA1STE              | X                                      | 1       | 0           |
|                           |   | S11                          | X                                      | X       | 1           |
| P8.5/UCB1SIMO/UCB1SDA/S10 | 5 | P8.5 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | UCB1SIMO/UCB1SDA             | X                                      | 1       | 0           |
|                           |   | S10                          | X                                      | X       | 1           |
| P8.6/UCB1SOMI/UCB1SCL/S9  | 6 | P8.6 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | UCB1SOMI/UCB1SCL             | X                                      | 1       | 0           |
|                           |   | S9                           | X                                      | X       | 1           |
| P8.7/S8                   | 7 | P8.7 (I/O)                   | I: 0; O: 1                             | 0       | 0           |
|                           |   | S8                           | X                                      | X       | 1           |

(1) X = Don't care

### 6.13.20 Port P9 (P9.0 to P9.7) Input/Output With Schmitt Trigger

图 6-23 shows the port diagram. 表 6-35 summarizes the selection of the port function.

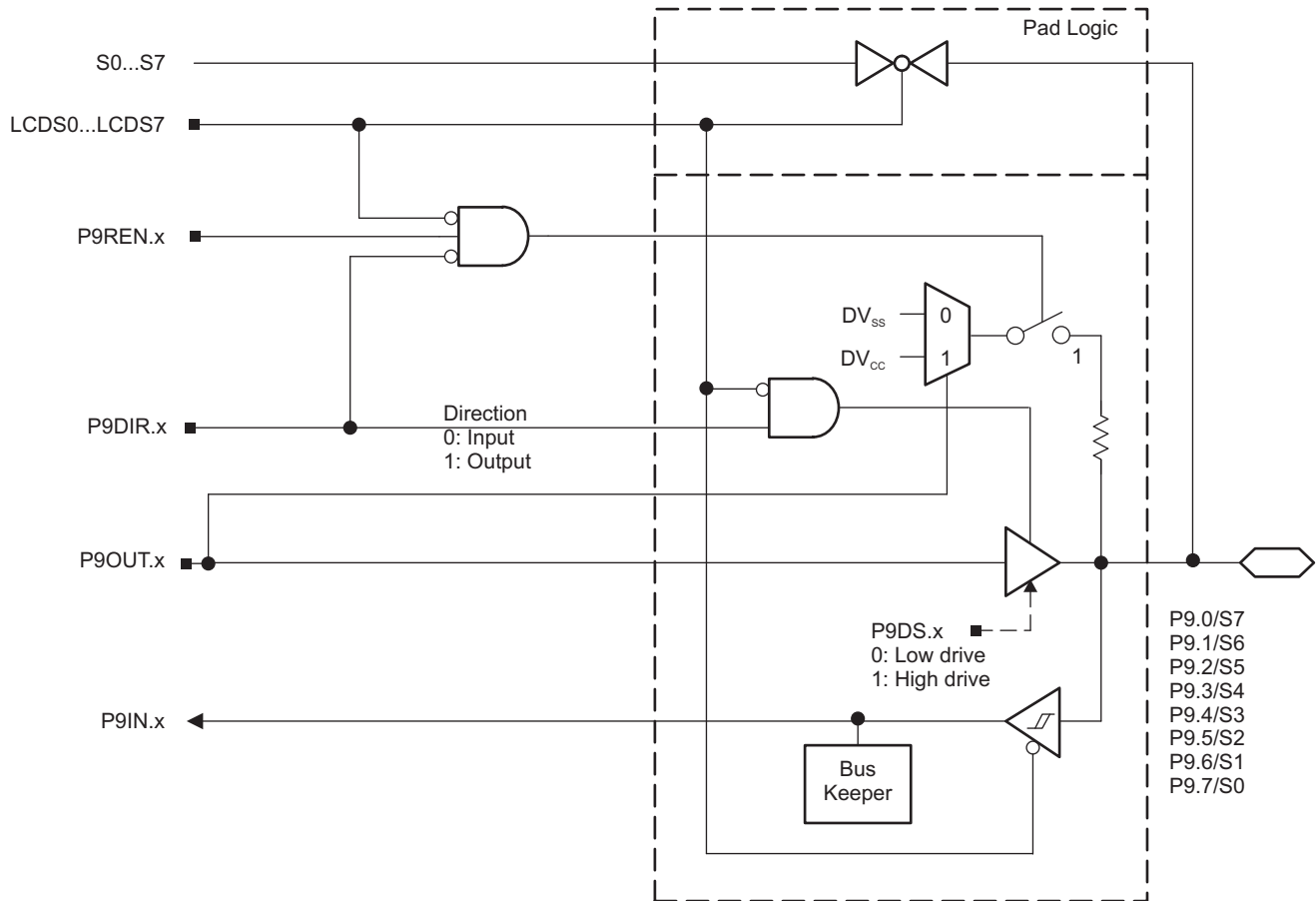


图 6-23. Port P9 (P9.0 to P9.7) Diagram

**表 6-35. Port P9 (P9.0 to P9.7) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION   | CONTROL BITS OR SIGNALS <sup>(1)</sup> |         |                |
|-----------------|---|------------|----------------------------------------|---------|----------------|
|                 |   |            | P9DIR.x                                | P9SEL.x | LCDS0 to LCDS7 |
| P9.0/S7         | 0 | P9.0 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S7         | X                                      | X       | 1              |
| P9.1/S6         | 1 | P9.1 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S6         | X                                      | X       | 1              |
| P9.2/S5         | 2 | P9.2 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S5         | X                                      | X       | 1              |
| P9.3/S4         | 3 | P9.3 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S4         | X                                      | X       | 1              |
| P9.4/S3         | 4 | P9.4 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S3         | X                                      | X       | 1              |
| P9.5/S2         | 5 | P9.5 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S2         | X                                      | X       | 1              |
| P9.6/S1         | 6 | P9.6 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S1         | X                                      | X       | 1              |
| P9.7/S0         | 7 | P9.7 (I/O) | I: 0; O: 1                             | 0       | 0              |
|                 |   | S0         | X                                      | X       | 1              |

(1) X = Don't care

### 6.13.21 Port U (PU.0/DP, PU.1/DM, PUR) USB Ports for MSP430FG662x

图 6-24 shows the port diagram. 表 6-36 and 表 6-37 summarize the port function selection.

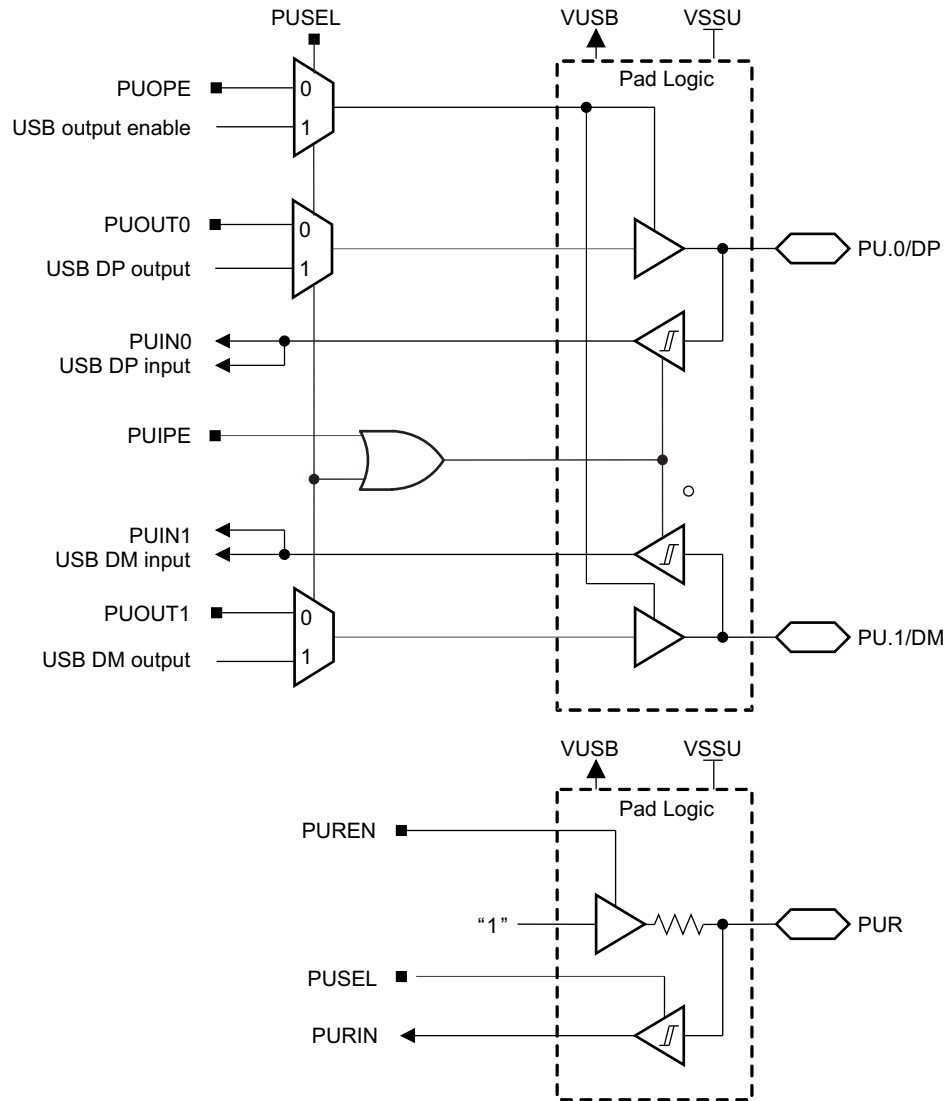


图 6-24. Port U (PU.0 and PU.1) Diagram

表 6-36. Port U (PU.0/DP, PU.1/DM) Output Functions for MSP430FG662x

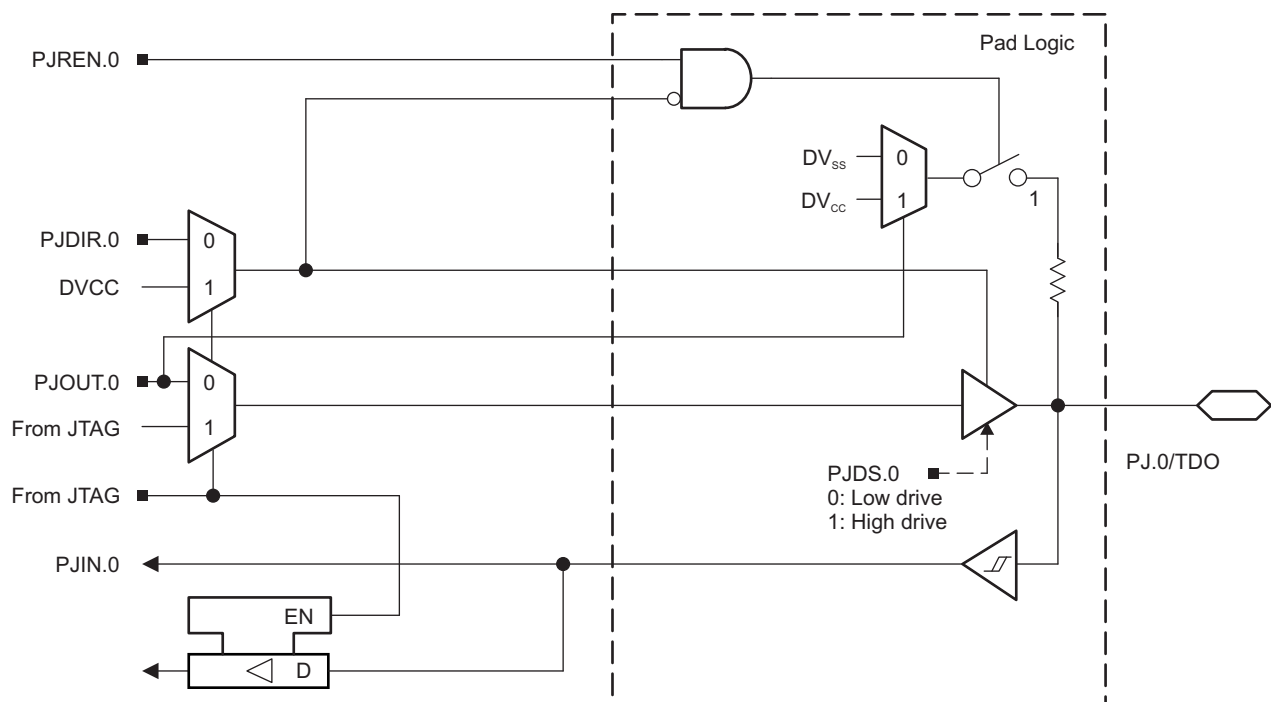
| CONTROL BITS |       |        |        | PIN NAME |         | FUNCTION                    |
|--------------|-------|--------|--------|----------|---------|-----------------------------|
| PUSEL        | PUDIR | PUOUT1 | PUOUT0 | PU.1/DM  | PU.0/DP |                             |
| 0            | 0     | X      | X      | Hi-Z     | Hi-Z    | Outputs off                 |
| 0            | 1     | 0      | 0      | 0        | 0       | Outputs enabled             |
| 0            | 1     | 0      | 1      | 0        | 1       | Outputs enabled             |
| 0            | 1     | 1      | 0      | 1        | 0       | Outputs enabled             |
| 0            | 1     | 1      | 1      | 1        | 1       | Outputs enabled             |
| 1            | X     | X      | X      | DM       | DP      | Direction set by USB module |

**表 6-37. Port U (PUR) Input Functions**

| CONTROL BITS |       | FUNCTION                          |
|--------------|-------|-----------------------------------|
| PUSEL        | PUREN |                                   |
| 0            | 0     | Input disabled<br>Pullup disabled |
| 0            | 1     | Input disabled<br>Pullup enabled  |
| 1            | 0     | Input enabled<br>Pullup disabled  |
| 1            | 1     | Input enabled<br>Pullup enabled   |

### 6.13.22 Port J (J.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

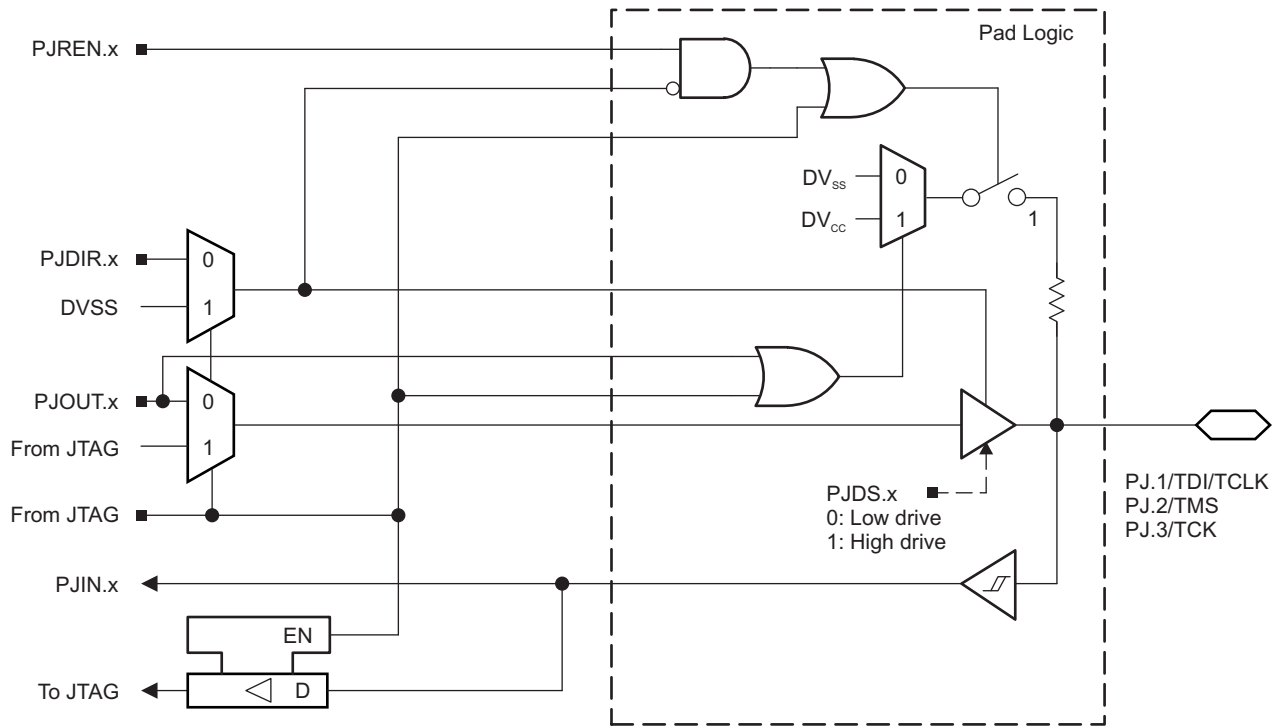
图 6-25 shows the port diagram. 表 6-38 summarizes the selection of the port function.



**图 6-25. Port PJ (PJ.0) Diagram**

### 6.13.23 Port J (J.1 to J.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

图 6-26 shows the port diagram. 表 6-38 summarizes the selection of the port function.



**图 6-26. Port PJ (PJ.1 to PJ.3) Diagram**

**表 6-38. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (P.J.x) | x | FUNCTION                    | CONTROL BITS OR SIGNALS <sup>(1)</sup> |
|------------------|---|-----------------------------|----------------------------------------|
|                  |   |                             | PJDIR.x                                |
| PJ.0/TDO         | 0 | PJ.0 (I/O) <sup>(2)</sup>   | I: 0; O: 1                             |
|                  |   | TDO <sup>(3)</sup>          | X                                      |
| PJ.1/TDI/TCLK    | 1 | PJ.1 (I/O) <sup>(2)</sup>   | I: 0; O: 1                             |
|                  |   | TDI/TCLK <sup>(3) (4)</sup> | X                                      |
| PJ.2/TMS         | 2 | PJ.2 (I/O) <sup>(2)</sup>   | I: 0; O: 1                             |
|                  |   | TMS <sup>(3) (4)</sup>      | X                                      |
| PJ.3/TCK         | 3 | PJ.3 (I/O) <sup>(2)</sup>   | I: 0; O: 1                             |
|                  |   | TCK <sup>(3) (4)</sup>      | X                                      |

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

## 6.14 Device Descriptors

表 6-39 summarizes the contents of the device descriptor tag-length-value (TLV) structure.

**表 6-39. Device Descriptor Table**

| DESCRIPTION        |                                                   | ADDRESS | SIZE<br>(bytes) | VALUE    |          |          |          |
|--------------------|---------------------------------------------------|---------|-----------------|----------|----------|----------|----------|
|                    |                                                   |         |                 | FG6626   | FG6625   | FG6426   | FG6425   |
| Info Block         | Info length                                       | 01A00h  | 1               | 06h      | 06h      | 06h      | 06h      |
|                    | CRC length                                        | 01A01h  | 1               | 06h      | 06h      | 06h      | 06h      |
|                    | CRC value                                         | 01A02h  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | Device ID                                         | 01A04h  | 2               | 8234h    | 8235h    | 8236h    | 8237h    |
|                    | Hardware revision                                 | 01A06h  | 1               | Per unit | Per unit | Per unit | Per unit |
|                    | Firmware revision                                 | 01A07h  | 1               | Per unit | Per unit | Per unit | Per unit |
| Die Record         | Die record tag                                    | 01A08h  | 1               | 08h      | 08h      | 08h      | 08h      |
|                    | Die record length                                 | 01A09h  | 1               | 0Ah      | 0Ah      | 0Ah      | 0Ah      |
|                    | Lot/wafer ID                                      | 01A0Ah  | 4               | Per unit | Per unit | Per unit | Per unit |
|                    | Die X position                                    | 01A0Eh  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | Die Y position                                    | 01A10h  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | Test results                                      | 01A12h  | 2               | Per unit | Per unit | Per unit | Per unit |
| CTSD16 Calibration | CTSD16 calibration tag                            | 01A14h  | 1               | 1Dh      | 1Dh      | 1Dh      | 1Dh      |
|                    | CTSD16 calibration length                         | 01A15h  | 1               | 0Ch      | 0Ch      | 0Ch      | 0Ch      |
|                    | CTSD16 gain factor gain = 1                       | 01A16h  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | CTSD16 gain factor gain = 16                      | 01A18h  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | CTSD16 offset gain = 1                            | 01A1Ah  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | CTSD16 offset gain = 16                           | 01A1Ch  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | CTSD16 internal reference temperature sensor 30°C | 01A1Eh  | 2               | Per unit | Per unit | Per unit | Per unit |
|                    | CTSD16 internal reference temperature sensor 85°C | 01A20h  | 2               | Per unit | Per unit | Per unit | Per unit |

## 6.15 Memory

表 6-40 summarizes the memory organization for all devices.

**表 6-40. Memory Organization<sup>(1)(2)</sup>**

|                                          |            | <b>MSP430FG6626</b>      | <b>MSP430FG6625</b>      | <b>MSP430FG6426</b>      | <b>MSP430FG6425</b>      |
|------------------------------------------|------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Memory (flash)<br>Main: interrupt vector | Total Size | 128KB<br>00FFFFh–00FF80h | 64KB<br>00FFFFh–00FF80h  | 128KB<br>00FFFFh–00FF80h | 64KB<br>00FFFFh–00FF80h  |
| Main: code memory                        | Bank 3     | 32KB<br>0243FFh–01C400h  | NA                       | 32KB<br>0243FFh–01C400h  | NA                       |
|                                          | Bank 2     | 32KB<br>01C3FFh–014400h  | NA                       | 32KB<br>01C3FFh–014400h  | NA                       |
|                                          | Bank 1     | 32KB<br>0143FFh–00C400h  | 32KB<br>0143FFh–00C400h  | 32KB<br>0143FFh–00C400h  | 32KB<br>0143FFh–00C400h  |
|                                          | Bank 0     | 32KB<br>00C3FFh–004400h  | 32KB<br>00C3FFh–004400h  | 32KB<br>00C3FFh–004400h  | 32KB<br>00C3FFh–004400h  |
| RAM                                      | Sector 3   | 2KB<br>0043FFh–003C00h   | 2KB<br>0043FFh–003C00h   | 2KB<br>0043FFh–003C00h   | 2KB<br>0043FFh–003C00h   |
|                                          | Sector 2   | 2KB<br>003BFFh–003400h   | 2KB<br>003BFFh–003400h   | 2KB<br>003BFFh–003400h   | 2KB<br>003BFFh–003400h   |
|                                          | Sector 1   | 2KB<br>0033FFh–002C00h   | 2KB<br>0033FFh–002C00h   | 2KB<br>0033FFh–002C00h   | 2KB<br>0033FFh–002C00h   |
|                                          | Sector 0   | 2KB<br>002BFFh–002400h   | 2KB<br>002BFFh–002400h   | 2KB<br>002BFFh–002400h   | 2KB<br>002BFFh–002400h   |
| RAM <sup>(3)</sup>                       | Sector 7   | NA                       | NA                       | 2 KB<br>0023FFh–001C00h  | 2KB<br>0023FFh–001C00h   |
| USB RAM <sup>(4)</sup>                   | Sector 7   | 2KB<br>0023FFh–001C00h   | 2KB<br>0023FFh–001C00h   | NA                       | NA                       |
| TI factory memory<br>(ROM)               | A          | 128 B<br>001BFFh–001B80h | 128 B<br>001BFFh–001B80h | 128 B<br>001BFFh–001B80h | 128 B<br>001BFFh–001B80h |
|                                          | B          | 128 B<br>001B7Fh–001B00h | 128 B<br>001B7Fh–001B00h | 128 B<br>001B7Fh–001B00h | 128 B<br>001B7Fh–001B00h |
|                                          | C          | 128 B<br>001AFFh–001A80h | 128 B<br>001AFFh–001A80h | 128 B<br>001AFFh–001A80h | 128 B<br>001AFFh–001A80h |
|                                          | D          | 128 B<br>001A7Fh–001A00h | 128 B<br>001A7Fh–001A00h | 128 B<br>001A7Fh–001A00h | 128 B<br>001A7Fh–001A00h |
| Information memory<br>(flash)            | Info A     | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h |
|                                          | Info B     | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h |
|                                          | Info C     | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h |
|                                          | Info D     | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h |
| Bootloader (BSL)<br>memory (flash)       | BSL 3      | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h |
|                                          | BSL 2      | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h |
|                                          | BSL 1      | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h |
|                                          | BSL 0      | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h |
| Peripherals                              | Size       | 4 KB<br>000FFFh–000000h  | 4KB<br>000FFFh–000000h   | 4KB<br>000FFFh–000000h   | 4KB<br>000FFFh–000000h   |

(1) N/A = Not available.

(2) Backup RAM is accessed through the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

(3) Only available on FG642x.

(4) Only available on FG662x. USB RAM can be used as general-purpose RAM when not used for USB operation.

### 6.15.1 Peripheral File Map

表 6-41 lists all of the the available peripherals and their base addresses. 表 6-42 through 表 6-78 list the registers and their offset addresses for each peripheral.

**表 6-41. Peripherals**

| MODULE NAME                                                       | BASE ADDRESS | OFFSET ADDRESS RANGE <sup>(1)</sup> |
|-------------------------------------------------------------------|--------------|-------------------------------------|
| Special Functions (see 表 6-42)                                    | 0100h        | 000h-01Fh                           |
| PMM (see 表 6-43)                                                  | 0120h        | 000h-010h                           |
| Flash Control (see 表 6-44)                                        | 0140h        | 000h-00Fh                           |
| CRC16 (see 表 6-45)                                                | 0150h        | 000h-007h                           |
| RAM Control (see 表 6-46)                                          | 0158h        | 000h-001h                           |
| Watchdog (see 表 6-47)                                             | 015Ch        | 000h-001h                           |
| UCS (see 表 6-48)                                                  | 0160h        | 000h-01Fh                           |
| SYS (see 表 6-49)                                                  | 0180h        | 000h-01Fh                           |
| Shared Reference (see 表 6-50)                                     | 01B0h        | 000h-001h                           |
| Port Mapping Control (see 表 6-51)                                 | 01C0h        | 000h-003h                           |
| Port Mapping Port P2 (see 表 6-51)                                 | 01D0h        | 000h-007h                           |
| Port P1, P2 (see 表 6-52)                                          | 0200h        | 000h-01Fh                           |
| Port P3, P4 (see 表 6-53)                                          | 0220h        | 000h-01Fh                           |
| Port P5, P6 (see 表 6-54)                                          | 0240h        | 000h-00Bh                           |
| Port P7, P8 (see 表 6-55)                                          | 0260h        | 000h-00Bh                           |
| Port P9 (see 表 6-56)                                              | 0280h        | 000h-00Bh                           |
| Port PJ (see 表 6-57)                                              | 0320h        | 000h-01Fh                           |
| Timer TA0 (see 表 6-58)                                            | 0340h        | 000h-02Eh                           |
| Timer TA1 (see 表 6-59)                                            | 0380h        | 000h-02Eh                           |
| Timer TB0 (see 表 6-60)                                            | 03C0h        | 000h-02Eh                           |
| Timer TA2 (see 表 6-61)                                            | 0400h        | 000h-02Eh                           |
| Battery Backup (see 表 6-62)                                       | 0480h        | 000h-01Fh                           |
| RTC_B (see 表 6-63)                                                | 04A0h        | 000h-01Fh                           |
| 32-Bit Hardware Multiplier (see 表 6-64)                           | 04C0h        | 000h-02Fh                           |
| DMA General Control (see 表 6-65)                                  | 0500h        | 000h-00Fh                           |
| DMA Channel 0 (see 表 6-65)                                        | 0510h        | 000h-00Ah                           |
| DMA Channel 1 (see 表 6-65)                                        | 0520h        | 000h-00Ah                           |
| DMA Channel 2 (see 表 6-65)                                        | 0530h        | 000h-00Ah                           |
| DMA Channel 3 (see 表 6-65)                                        | 0540h        | 000h-00Ah                           |
| DMA Channel 4 (see 表 6-65)                                        | 0550h        | 000h-00Ah                           |
| DMA Channel 5 (see 表 6-65)                                        | 0560h        | 000h-00Ah                           |
| USCI_A0 (see 表 6-66)                                              | 05C0h        | 000h-01Fh                           |
| USCI_B0 (see 表 6-67)                                              | 05E0h        | 000h-01Fh                           |
| USCI_A1 (see 表 6-68)                                              | 0600h        | 000h-01Fh                           |
| USCI_B1 (see 表 6-69)                                              | 0620h        | 000h-01Fh                           |
| DAC12_A (see 表 6-70)                                              | 0780h        | 000h-01Fh                           |
| Comparator_B (see 表 6-71)                                         | 08C0h        | 000h-00Fh                           |
| USB configuration (see 表 6-72) <sup>(2)</sup>                     | 0900h        | 000h-014h                           |
| USB control (see 表 6-73) <sup>(2)</sup>                           | 0920h        | 000h-01Fh                           |
| LDO-PWR; LDO and Port U configuration (see 表 6-74) <sup>(3)</sup> | 0900h        | 000h-014h                           |

(1) For a detailed description of the individual control register offset addresses, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

(2) Only on devices with peripheral module USB.

(3) Only on devices with peripheral module LDO-PWR.

**表 6-41. Peripherals (continued)**

| MODULE NAME                | BASE ADDRESS | OFFSET ADDRESS RANGE <sup>(1)</sup> |
|----------------------------|--------------|-------------------------------------|
| LCD_B control (see 表 6-75) | 0A00h        | 000h-05Fh                           |
| CTSD16 (see 表 6-76)        | 0A80h        | 000h-05Fh                           |
| OA0 and GSW0 (see 表 6-77)  | 0AE0h        | 000h-00Fh                           |
| OA1 and GSW1 (see 表 6-78)  | 0AF0h        | 000h-00Fh                           |

**表 6-42. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable  | SFRIE1   | 00h    |
| SFR interrupt flag    | SFRIFG1  | 02h    |
| SFR reset pin control | SFRRPCR  | 04h    |

**表 6-43. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM control 0            | PMMCTL0  | 00h    |
| PMM control 1            | PMMCTL1  | 02h    |
| SVS high-side control    | SVSMHCTL | 04h    |
| SVS low-side control     | SVSMLCTL | 06h    |
| PMM interrupt flags      | PMMIFG   | 0Ch    |
| PMM interrupt enable     | PMMIE    | 0Eh    |
| PMM power mode 5 control | PM5CTL0  | 10h    |

**表 6-44. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1      | FCTL1    | 00h    |
| Flash control 3      | FCTL3    | 04h    |
| Flash control 4      | FCTL4    | 06h    |

**表 6-45. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER  | OFFSET |
|----------------------|-----------|--------|
| CRC data input       | CRC16DI   | 00h    |
| CRC result           | CRC16NIRS | 04h    |

**表 6-46. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0        | RCCTL0   | 00h    |

**表 6-47. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION   | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL   | 00h    |

表 6-48. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0        | UCSCTL0  | 00h    |
| UCS control 1        | UCSCTL1  | 02h    |
| UCS control 2        | UCSCTL2  | 04h    |
| UCS control 3        | UCSCTL3  | 06h    |
| UCS control 4        | UCSCTL4  | 08h    |
| UCS control 5        | UCSCTL5  | 0Ah    |
| UCS control 6        | UCSCTL6  | 0Ch    |
| UCS control 7        | UCSCTL7  | 0Eh    |
| UCS control 8        | UCSCTL8  | 10h    |

表 6-49. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| System control                | SYSCTL    | 00h    |
| Bootloader configuration area | SYSBSLC   | 02h    |
| JTAG mailbox control          | SYSJMBC   | 06h    |
| JTAG mailbox input 0          | SYSJMBI0  | 08h    |
| JTAG mailbox input 1          | SYSJMBI1  | 0Ah    |
| JTAG mailbox output 0         | SYSJMBO0  | 0Ch    |
| JTAG mailbox output 1         | SYSJMBO1  | 0Eh    |
| Bus error vector generator    | SYSBERRIV | 18h    |
| User NMI vector generator     | SYSUNIV   | 1Ah    |
| System NMI vector generator   | SYSSNIV   | 1Ch    |
| Reset vector generator        | SYSRSTIV  | 1Eh    |

表 6-50. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL   | 00h    |

表 6-51. Port Mapping Registers  
(Base Address of Port Mapping Control: 01C0h, Port P2: 01D0h)

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| Port mapping password | PMAPPWD  | 00h    |
| Port mapping control  | PMAPCTL  | 02h    |
| Port P2.0 mapping     | P2MAP0   | 00h    |
| Port P2.1 mapping     | P2MAP1   | 01h    |
| Port P2.2 mapping     | P2MAP2   | 02h    |
| Port P2.3 mapping     | P2MAP3   | 03h    |
| Port P2.4 mapping     | P2MAP4   | 04h    |
| Port P2.5 mapping     | P2MAP5   | 05h    |
| Port P2.6 mapping     | P2MAP6   | 06h    |
| Port P2.7 mapping     | P2MAP7   | 07h    |

**表 6-52. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P1 input                 | P1IN     | 00h    |
| Port P1 output                | P1OUT    | 02h    |
| Port P1 direction             | P1DIR    | 04h    |
| Port P1 resistor enable       | P1REN    | 06h    |
| Port P1 drive strength        | P1DS     | 08h    |
| Port P1 selection             | P1SEL    | 0Ah    |
| Port P1 interrupt vector word | P1IV     | 0Eh    |
| Port P1 interrupt edge select | P1IES    | 18h    |
| Port P1 interrupt enable      | P1IE     | 1Ah    |
| Port P1 interrupt flag        | P1IFG    | 1Ch    |
| Port P2 input                 | P2IN     | 01h    |
| Port P2 output                | P2OUT    | 03h    |
| Port P2 direction             | P2DIR    | 05h    |
| Port P2 resistor enable       | P2REN    | 07h    |
| Port P2 drive strength        | P2DS     | 09h    |
| Port P2 selection             | P2SEL    | 0Bh    |
| Port P2 interrupt vector word | P2IV     | 1Eh    |
| Port P2 interrupt edge select | P2IES    | 19h    |
| Port P2 interrupt enable      | P2IE     | 1Bh    |
| Port P2 interrupt flag        | P2IFG    | 1Dh    |

**表 6-53. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P3 input                 | P3IN     | 00h    |
| Port P3 output                | P3OUT    | 02h    |
| Port P3 direction             | P3DIR    | 04h    |
| Port P3 resistor enable       | P3REN    | 06h    |
| Port P3 drive strength        | P3DS     | 08h    |
| Port P3 selection             | P3SEL    | 0Ah    |
| Port P3 interrupt vector word | P3IV     | 0Eh    |
| Port P3 interrupt edge select | P3IES    | 18h    |
| Port P3 interrupt enable      | P3IE     | 1Ah    |
| Port P3 interrupt flag        | P3IFG    | 1Ch    |
| Port P4 input                 | P4IN     | 01h    |
| Port P4 output                | P4OUT    | 03h    |
| Port P4 direction             | P4DIR    | 05h    |
| Port P4 resistor enable       | P4REN    | 07h    |
| Port P4 drive strength        | P4DS     | 09h    |
| Port P4 selection             | P4SEL    | 0Bh    |
| Port P4 interrupt vector word | P4IV     | 1Eh    |
| Port P4 interrupt edge select | P4IES    | 19h    |
| Port P4 interrupt enable      | P4IE     | 1Bh    |
| Port P4 interrupt flag        | P4IFG    | 1Dh    |

表 6-54. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P5 input           | P5IN     | 00h    |
| Port P5 output          | P5OUT    | 02h    |
| Port P5 direction       | P5DIR    | 04h    |
| Port P5 resistor enable | P5REN    | 06h    |
| Port P5 drive strength  | P5DS     | 08h    |
| Port P5 selection       | P5SEL    | 0Ah    |
| Port P6 input           | P6IN     | 01h    |
| Port P6 output          | P6OUT    | 03h    |
| Port P6 direction       | P6DIR    | 05h    |
| Port P6 resistor enable | P6REN    | 07h    |
| Port P6 drive strength  | P6DS     | 09h    |
| Port P6 selection       | P6SEL    | 0Bh    |

表 6-55. Port P7, P8 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P7 input           | P7IN     | 00h    |
| Port P7 output          | P7OUT    | 02h    |
| Port P7 direction       | P7DIR    | 04h    |
| Port P7 resistor enable | P7REN    | 06h    |
| Port P7 drive strength  | P7DS     | 08h    |
| Port P7 selection       | P7SEL    | 0Ah    |
| Port P8 input           | P8IN     | 01h    |
| Port P8 output          | P8OUT    | 03h    |
| Port P8 direction       | P8DIR    | 05h    |
| Port P8 resistor enable | P8REN    | 07h    |
| Port P8 drive strength  | P8DS     | 09h    |
| Port P8 selection       | P8SEL    | 0Bh    |

表 6-56. Port P9 Register (Base Address: 0280h)

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P9 input           | P9IN     | 00h    |
| Port P9 output          | P9OUT    | 02h    |
| Port P9 direction       | P9DIR    | 04h    |
| Port P9 resistor enable | P9REN    | 06h    |
| Port P9 drive strength  | P9DS     | 08h    |
| Port P9 selection       | P9SEL    | 0Ah    |

表 6-57. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port PJ input           | PJIN     | 00h    |
| Port PJ output          | PJOUT    | 02h    |
| Port PJ direction       | PJDIR    | 04h    |
| Port PJ resistor enable | PJREN    | 06h    |
| Port PJ drive strength  | PJDS     | 08h    |

**表 6-58. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control               | TA0CTL   | 00h    |
| Capture/compare control 0 | TA0CCTL0 | 02h    |
| Capture/compare control 1 | TA0CCTL1 | 04h    |
| Capture/compare control 2 | TA0CCTL2 | 06h    |
| Capture/compare control 3 | TA0CCTL3 | 08h    |
| Capture/compare control 4 | TA0CCTL4 | 0Ah    |
| TA0 counter               | TA0R     | 10h    |
| Capture/compare 0         | TA0CCR0  | 12h    |
| Capture/compare 1         | TA0CCR1  | 14h    |
| Capture/compare 2         | TA0CCR2  | 16h    |
| Capture/compare 3         | TA0CCR3  | 18h    |
| Capture/compare 4         | TA0CCR4  | 1Ah    |
| TA0 expansion 0           | TA0EX0   | 20h    |
| TA0 interrupt vector      | TA0IV    | 2Eh    |

**表 6-59. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control               | TA1CTL   | 00h    |
| Capture/compare control 0 | TA1CCTL0 | 02h    |
| Capture/compare control 1 | TA1CCTL1 | 04h    |
| Capture/compare control 2 | TA1CCTL2 | 06h    |
| TA1 counter               | TA1R     | 10h    |
| Capture/compare 0         | TA1CCR0  | 12h    |
| Capture/compare 1         | TA1CCR1  | 14h    |
| Capture/compare 2         | TA1CCR2  | 16h    |
| TA1 expansion 0           | TA1EX0   | 20h    |
| TA1 interrupt vector      | TA1IV    | 2Eh    |

表 6-60. TB0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control               | TB0CTL   | 00h    |
| Capture/compare control 0 | TB0CCTL0 | 02h    |
| Capture/compare control 1 | TB0CCTL1 | 04h    |
| Capture/compare control 2 | TB0CCTL2 | 06h    |
| Capture/compare control 3 | TB0CCTL3 | 08h    |
| Capture/compare control 4 | TB0CCTL4 | 0Ah    |
| Capture/compare control 5 | TB0CCTL5 | 0Ch    |
| Capture/compare control 6 | TB0CCTL6 | 0Eh    |
| TB0 counter               | TB0R     | 10h    |
| Capture/compare 0         | TB0CCR0  | 12h    |
| Capture/compare 1         | TB0CCR1  | 14h    |
| Capture/compare 2         | TB0CCR2  | 16h    |
| Capture/compare 3         | TB0CCR3  | 18h    |
| Capture/compare 4         | TB0CCR4  | 1Ah    |
| Capture/compare 5         | TB0CCR5  | 1Ch    |
| Capture/compare 6         | TB0CCR6  | 1Eh    |
| TB0 expansion 0           | TB0EX0   | 20h    |
| TB0 interrupt vector      | TB0IV    | 2Eh    |

表 6-61. TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA2 control               | TA2CTL   | 00h    |
| Capture/compare control 0 | TA2CCTL0 | 02h    |
| Capture/compare control 1 | TA2CCTL1 | 04h    |
| Capture/compare control 2 | TA2CCTL2 | 06h    |
| TA2 counter               | TA2R     | 10h    |
| Capture/compare 0         | TA2CCR0  | 12h    |
| Capture/compare 1         | TA2CCR1  | 14h    |
| Capture/compare 2         | TA2CCR2  | 16h    |
| TA2 expansion 0           | TA2EX0   | 20h    |
| TA2 interrupt vector      | TA2IV    | 2Eh    |

表 6-62. Battery Backup Registers (Base Address: 0480h)

| REGISTER DESCRIPTION    | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Battery backup memory 0 | BAKMEM0  | 00h    |
| Battery backup memory 1 | BAKMEM1  | 02h    |
| Battery backup memory 2 | BAKMEM2  | 04h    |
| Battery backup memory 3 | BAKMEM3  | 06h    |
| Battery backup control  | BAKCTL   | 1Ch    |
| Battery charger control | BAKCHCTL | 1Eh    |

**表 6-63. Real-Time Clock Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION      | REGISTER    | OFFSET |
|---------------------------|-------------|--------|
| RTC control 0             | RTCCTL0     | 00h    |
| RTC control 1             | RTCCTL1     | 01h    |
| RTC control 2             | RTCCTL2     | 02h    |
| RTC control 3             | RTCCTL3     | 03h    |
| RTC prescaler 0 control   | RTCPSEL0CTL | 08h    |
| RTC prescaler 1 control   | RTCPSEL1CTL | 0Ah    |
| RTC prescaler 0           | RTCPSEL0    | 0Ch    |
| RTC prescaler 1           | RTCPSEL1    | 0Dh    |
| RTC interrupt vector word | RTCIV       | 0Eh    |
| RTC seconds               | RTCSEC      | 10h    |
| RTC minutes               | RTCMIN      | 11h    |
| RTC hours                 | RTCHOUR     | 12h    |
| RTC day of week           | RTCDOW      | 13h    |
| RTC days                  | RTCDAY      | 14h    |
| RTC month                 | RTCMON      | 15h    |
| RTC year low              | RTCYEARL    | 16h    |
| RTC year high             | RTCYEARH    | 17h    |
| RTC alarm minutes         | RTCAMIN     | 18h    |
| RTC alarm hours           | RTCAHOUR    | 19h    |
| RTC alarm day of week     | RTCADOW     | 1Ah    |
| RTC alarm days            | RTCADAY     | 1Bh    |
| Binary-to-BCD conversion  | BIN2BCD     | 1Ch    |
| BCD-to-binary conversion  | BCD2BIN     | 1Eh    |

**表 6-64. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION                                    | REGISTER  | OFFSET |
|---------------------------------------------------------|-----------|--------|
| 16-bit operand 1 – multiply                             | MPY       | 00h    |
| 16-bit operand 1 – signed multiply                      | MPYS      | 02h    |
| 16-bit operand 1 – multiply accumulate                  | MAC       | 04h    |
| 16-bit operand 1 – signed multiply accumulate           | MACS      | 06h    |
| 16-bit operand 2                                        | OP2       | 08h    |
| 16 × 16 result low word                                 | RESLO     | 0Ah    |
| 16 × 16 result high word                                | RESHI     | 0Ch    |
| 16 × 16 sum extension register                          | SUMEXT    | 0Eh    |
| 32-bit operand 1 – multiply low word                    | MPY32L    | 10h    |
| 32-bit operand 1 – multiply high word                   | MPY32H    | 12h    |
| 32-bit operand 1 – signed multiply low word             | MPYS32L   | 14h    |
| 32-bit operand 1 – signed multiply high word            | MPYS32H   | 16h    |
| 32-bit operand 1 – multiply accumulate low word         | MAC32L    | 18h    |
| 32-bit operand 1 – multiply accumulate high word        | MAC32H    | 1Ah    |
| 32-bit operand 1 – signed multiply accumulate low word  | MACS32L   | 1Ch    |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H   | 1Eh    |
| 32-bit operand 2 – low word                             | OP2L      | 20h    |
| 32-bit operand 2 – high word                            | OP2H      | 22h    |
| 32 × 32 result 0 – least significant word               | RES0      | 24h    |
| 32 × 32 result 1                                        | RES1      | 26h    |
| 32 × 32 result 2                                        | RES2      | 28h    |
| 32 × 32 result 3 – most significant word                | RES3      | 2Ah    |
| MPY32 control 0                                         | MPY32CTL0 | 2Ch    |

**表 6-65. DMA Registers (Base Address DMA General Control: 0500h,  
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA  
Channel 4: 0550h, DMA Channel 5: 0560h)**

| REGISTER DESCRIPTION                      | REGISTER | OFFSET |
|-------------------------------------------|----------|--------|
| DMA general control: DMA module control 0 | DMACTL0  | 00h    |
| DMA general control: DMA module control 1 | DMACTL1  | 02h    |
| DMA general control: DMA module control 2 | DMACTL2  | 04h    |
| DMA general control: DMA module control 3 | DMACTL3  | 06h    |
| DMA general control: DMA module control 4 | DMACTL4  | 08h    |
| DMA general control: DMA interrupt vector | DMAIV    | 0Ah    |
| DMA channel 0 control                     | DMA0CTL  | 00h    |
| DMA channel 0 source address low          | DMA0SAL  | 02h    |
| DMA channel 0 source address high         | DMA0SAH  | 04h    |
| DMA channel 0 destination address low     | DMA0DAL  | 06h    |
| DMA channel 0 destination address high    | DMA0DAH  | 08h    |
| DMA channel 0 transfer size               | DMA0SZ   | 0Ah    |
| DMA channel 1 control                     | DMA1CTL  | 00h    |
| DMA channel 1 source address low          | DMA1SAL  | 02h    |
| DMA channel 1 source address high         | DMA1SAH  | 04h    |
| DMA channel 1 destination address low     | DMA1DAL  | 06h    |
| DMA channel 1 destination address high    | DMA1DAH  | 08h    |
| DMA channel 1 transfer size               | DMA1SZ   | 0Ah    |
| DMA channel 2 control                     | DMA2CTL  | 00h    |
| DMA channel 2 source address low          | DMA2SAL  | 02h    |
| DMA channel 2 source address high         | DMA2SAH  | 04h    |
| DMA channel 2 destination address low     | DMA2DAL  | 06h    |
| DMA channel 2 destination address high    | DMA2DAH  | 08h    |
| DMA channel 2 transfer size               | DMA2SZ   | 0Ah    |
| DMA channel 3 control                     | DMA3CTL  | 00h    |
| DMA channel 3 source address low          | DMA3SAL  | 02h    |
| DMA channel 3 source address high         | DMA3SAH  | 04h    |
| DMA channel 3 destination address low     | DMA3DAL  | 06h    |
| DMA channel 3 destination address high    | DMA3DAH  | 08h    |
| DMA channel 3 transfer size               | DMA3SZ   | 0Ah    |
| DMA channel 4 control                     | DMA4CTL  | 00h    |
| DMA channel 4 source address low          | DMA4SAL  | 02h    |
| DMA channel 4 source address high         | DMA4SAH  | 04h    |
| DMA channel 4 destination address low     | DMA4DAL  | 06h    |
| DMA channel 4 destination address high    | DMA4DAH  | 08h    |
| DMA channel 4 transfer size               | DMA4SZ   | 0Ah    |
| DMA channel 5 control                     | DMA5CTL  | 00h    |
| DMA channel 5 source address low          | DMA5SAL  | 02h    |
| DMA channel 5 source address high         | DMA5SAH  | 04h    |
| DMA channel 5 destination address low     | DMA5DAL  | 06h    |
| DMA channel 5 destination address high    | DMA5DAH  | 08h    |
| DMA channel 5 transfer size               | DMA5SZ   | 0Ah    |

**表 6-66. USCI\_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION       | REGISTER   | OFFSET |
|----------------------------|------------|--------|
| USCI control 0             | UCA0CTL0   | 00h    |
| USCI control 1             | UCA0CTL1   | 01h    |
| USCI baud rate 0           | UCA0BR0    | 06h    |
| USCI baud rate 1           | UCA0BR1    | 07h    |
| USCI modulation control    | UCA0MCTL   | 08h    |
| USCI status                | UCA0STAT   | 0Ah    |
| USCI receive buffer        | UCA0RXBUF  | 0Ch    |
| USCI transmit buffer       | UCA0TXBUF  | 0Eh    |
| USCI LIN control           | UCA0ABCTL  | 10h    |
| USCI IrDA transmit control | UCA0IRTCTL | 12h    |
| USCI IrDA receive control  | UCA0IRRCTL | 13h    |
| USCI interrupt enable      | UCA0IE     | 1Ch    |
| USCI interrupt flags       | UCA0IFG    | 1Dh    |
| USCI interrupt vector word | UCA0IV     | 1Eh    |

**表 6-67. USCI\_B0 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION             | REGISTER  | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 0       | UCB0CTL0  | 00h    |
| USCI synchronous control 1       | UCB0CTL1  | 01h    |
| USCI synchronous bit rate 0      | UCB0BR0   | 06h    |
| USCI synchronous bit rate 1      | UCB0BR1   | 07h    |
| USCI synchronous status          | UCB0STAT  | 0Ah    |
| USCI synchronous receive buffer  | UCB0RXBUF | 0Ch    |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh    |
| USCI I2C own address             | UCB0I2COA | 10h    |
| USCI I2C slave address           | UCB0I2CSA | 12h    |
| USCI interrupt enable            | UCB0IE    | 1Ch    |
| USCI interrupt flags             | UCB0IFG   | 1Dh    |
| USCI interrupt vector word       | UCB0IV    | 1Eh    |

**表 6-68. USCI\_A1 Registers (Base Address: 0600h)**

| REGISTER DESCRIPTION       | REGISTER   | OFFSET |
|----------------------------|------------|--------|
| USCI control 0             | UCA1CTL0   | 00h    |
| USCI control 1             | UCA1CTL1   | 01h    |
| USCI baud rate 0           | UCA1BR0    | 06h    |
| USCI baud rate 1           | UCA1BR1    | 07h    |
| USCI modulation control    | UCA1MCTL   | 08h    |
| USCI status                | UCA1STAT   | 0Ah    |
| USCI receive buffer        | UCA1RXBUF  | 0Ch    |
| USCI transmit buffer       | UCA1TXBUF  | 0Eh    |
| USCI LIN control           | UCA1ABCTL  | 10h    |
| USCI IrDA transmit control | UCA1IRTCTL | 12h    |
| USCI IrDA receive control  | UCA1IRRCTL | 13h    |
| USCI interrupt enable      | UCA1IE     | 1Ch    |
| USCI interrupt flags       | UCA1IFG    | 1Dh    |
| USCI interrupt vector word | UCA1IV     | 1Eh    |

**表 6-69. USCI\_B1 Registers (Base Address: 0620h)**

| REGISTER DESCRIPTION             | REGISTER  | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 0       | UCB1CTL0  | 00h    |
| USCI synchronous control 1       | UCB1CTL1  | 01h    |
| USCI synchronous bit rate 0      | UCB1BR0   | 06h    |
| USCI synchronous bit rate 1      | UCB1BR1   | 07h    |
| USCI synchronous status          | UCB1STAT  | 0Ah    |
| USCI synchronous receive buffer  | UCB1RXBUF | 0Ch    |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh    |
| USCI I2C own address             | UCB1I2COA | 10h    |
| USCI I2C slave address           | UCB1I2CSA | 12h    |
| USCI interrupt enable            | UCB1IE    | 1Ch    |
| USCI interrupt flags             | UCB1IFG   | 1Dh    |
| USCI interrupt vector word       | UCB1IV    | 1Eh    |

**表 6-70. DAC12\_A Registers (Base Address: 0780h)**

| REGISTER DESCRIPTION                  | REGISTER      | OFFSET |
|---------------------------------------|---------------|--------|
| DAC12_A channel 0 control 0           | DAC12_0CTL0   | 00h    |
| DAC12_A channel 0 control 1           | DAC12_0CTL1   | 02h    |
| DAC12_A channel 0 data                | DAC12_0DAT    | 04h    |
| DAC12_A channel 0 calibration control | DAC12_0CALCTL | 06h    |
| DAC12_A channel 0 calibration data    | DAC12_0CALDAT | 08h    |
| DAC12_A channel 1 control 0           | DAC12_1CTL0   | 10h    |
| DAC12_A channel 1 control 1           | DAC12_1CTL1   | 12h    |
| DAC12_A channel 1 data                | DAC12_1DAT    | 14h    |
| DAC12_A channel 1 calibration control | DAC12_1CALCTL | 16h    |
| DAC12_A channel 1 calibration data    | DAC12_1CALDAT | 18h    |
| DAC12_A interrupt vector word         | DAC12IV       | 1Eh    |

**表 6-71. Comparator\_B Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control 0             | CBCTL0   | 00h    |
| Comp_B control 1             | CBCTL1   | 02h    |
| Comp_B control 2             | CBCTL2   | 04h    |
| Comp_B control 3             | CBCTL3   | 06h    |
| Comp_B interrupt             | CBINT    | 0Ch    |
| Comp_B interrupt vector word | CBIV     | 0Eh    |

表 6-72. USB Configuration Registers (Base Address: 0900h)

| REGISTER DESCRIPTION      | REGISTER  | OFFSET |
|---------------------------|-----------|--------|
| USB key/ID                | USBKEYID  | 00h    |
| USB module configuration  | USBCNF    | 02h    |
| USB PHY control           | USBPHYCTL | 04h    |
| USB power control         | USBPWRCTL | 08h    |
| USB power voltage setting | USBPWRVSR | 0Ah    |
| USB PLL control           | USBPLLCTL | 10h    |
| USB PLL divider           | USBPLLDIV | 12h    |
| USB PLL interrupts        | USBPLLIR  | 14h    |

表 6-73. USB Control Registers (Base Address: 0920h)

| REGISTER DESCRIPTION              | REGISTER     | OFFSET |
|-----------------------------------|--------------|--------|
| Input endpoint_0 configuration    | USBIEPCNF_0  | 00h    |
| Input endpoint_0 byte count       | USBIEPBCNT_0 | 01h    |
| Output endpoint_0 configuration   | USBOEPCNFG_0 | 02h    |
| Output endpoint_0 byte count      | USBOEPBCNT_0 | 03h    |
| Input endpoint interrupt enables  | USBIEPIE     | 0Eh    |
| Output endpoint interrupt enables | USBOEPIE     | 0Fh    |
| Input endpoint interrupt flags    | USBIEPIFG    | 10h    |
| Output endpoint interrupt flags   | USBOEPIFG    | 11h    |
| USB interrupt vector              | USBIV        | 12h    |
| USB maintenance                   | USBMAINT     | 16h    |
| Time stamp                        | USBTSREG     | 18h    |
| USB frame number                  | USBFN        | 1Ah    |
| USB control                       | USBCTL       | 1Ch    |
| USB interrupt enables             | USBIE        | 1Dh    |
| USB interrupt flags               | USBIFG       | 1Eh    |
| Function address                  | USBFUNADR    | 1Fh    |

表 6-74. LDO and Port U Configuration Registers (Base Address: 0900h)

| REGISTER DESCRIPTION | REGISTER  | OFFSET |
|----------------------|-----------|--------|
| LDO key and ID       | LDOKEYPID | 00h    |
| PU port control      | PUCTL     | 04h    |
| LDO power control    | LDPWRCTL  | 08h    |

**表 6-75. LCD\_B Registers (Base Address: 0A00h)**

| REGISTER DESCRIPTION        | REGISTER   | OFFSET |
|-----------------------------|------------|--------|
| LCD_B control 0             | LCDBCTL0   | 000h   |
| LCD_B control 1             | LCDBCTL1   | 002h   |
| LCD_B blinking control      | LCDBBLKCTL | 004h   |
| LCD_B memory control        | LCDBMEMCTL | 006h   |
| LCD_B voltage control       | LCDBVCTL   | 008h   |
| LCD_B port control 0        | LCDBPCTL0  | 00Ah   |
| LCD_B port control 1        | LCDBPCTL1  | 00Ch   |
| LCD_B port control 2        | LCDBPCTL2  | 00Eh   |
| LCD_B charge pump control   | LCDBCTL0   | 012h   |
| LCD_B interrupt vector word | LCDBIV     | 01Eh   |
| LCD_B memory 1              | LCDM1      | 020h   |
| LCD_B memory 2              | LCDM2      | 021h   |
| ⋮                           | ⋮          | ⋮      |
| LCD_B memory 22             | LCDM22     | 035h   |
| LCD_B blinking memory 1     | LCDBM1     | 040h   |
| LCD_B blinking memory 2     | LCDBM2     | 041h   |
| ⋮                           | ⋮          | ⋮      |
| LCD_B blinking memory 22    | LCDBM22    | 055h   |

**表 6-76. CTSD16 Registers (Base Address: 0A80h)**

| REGISTER DESCRIPTION               | REGISTER     | OFFSET |
|------------------------------------|--------------|--------|
| CTSD16 control                     | CTSD16CTL    | 00h    |
| CTSD16 channel 0 control           | CTSD16CCTL0  | 02h    |
| CTSD16 channel 0 input control     | CTSD16INCTL0 | 04h    |
| CTSD16 channel 0 preload           | CTSD16PRE0   | 06h    |
| CTSD16 interrupt flag              | CTSD16IFG    | 2Ch    |
| CTSD16 interrupt enable            | CTSD16IE     | 2Eh    |
| CTSD16 interrupt vector            | CTSD16IV     | 30h    |
| CTSD16 channel 0 conversion memory | CTSD16MEM0   | 32h    |

**表 6-77. OA0 Registers (Base Address: 0AE0h)**

| REGISTER DESCRIPTION                 | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| OA0 control 0                        | OA0CTL0  | 00h    |
| OA0 positive input terminal switches | OA0PSW   | 02h    |
| OA0 negative input terminal switches | OA0NSW   | 04h    |
| OA0 ground switches                  | OA0GSW   | 0Eh    |

**表 6-78. OA1 Registers (Base Address: 0AF0h)**

| REGISTER DESCRIPTION                 | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| OA1 control 0                        | OA1CTL0  | 00h    |
| OA1 positive input terminal switches | OA1PSW   | 02h    |
| OA1 negative input terminal switches | OA1NSW   | 04h    |
| OA1 ground switches                  | OA1GSW   | 0Eh    |

## 6.16 Identification

### 6.16.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see .

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [节 6.14](#).

### 6.16.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see .

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [节 6.14](#).

### 6.16.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the [MSP430 Programming With the JTAG Interface User's Guide](#).

## 7 Applications, Implementation, and Layout

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

#### 7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 1- $\mu$ F plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommended for better noise isolation from digital to analog circuits on the board and are especially recommended to achieve high analog accuracy.

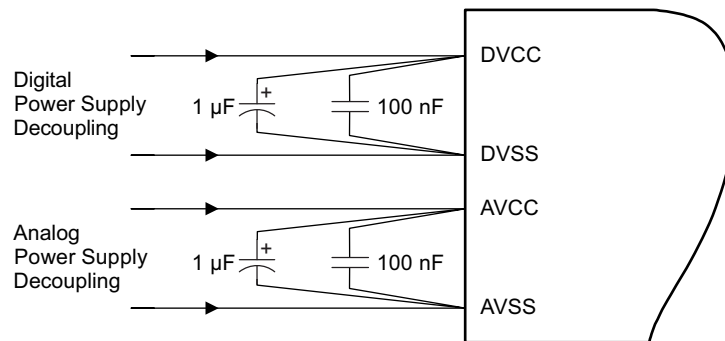


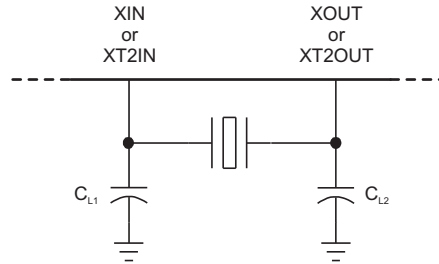
图 7-1. Power Supply Decoupling

#### 7.1.2 External Oscillator

Depending on the device variant (see [Section 3](#)), the device can support a low-frequency crystal (32 kHz) on the XT1 pins, a high-frequency crystal on the XT2 pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN and XT2IN input pins that meet the specifications of the respective oscillator if the appropriate XT1BYPASS or XT2BYPASS mode is selected. In this case, the associated XOUT and XT2OUT pins can be used for other purposes. If they are left unused, they must be terminated according to [Table 4-4](#).

图 7-2 shows a typical connection diagram.

**图 7-2. Typical Crystal Connection**

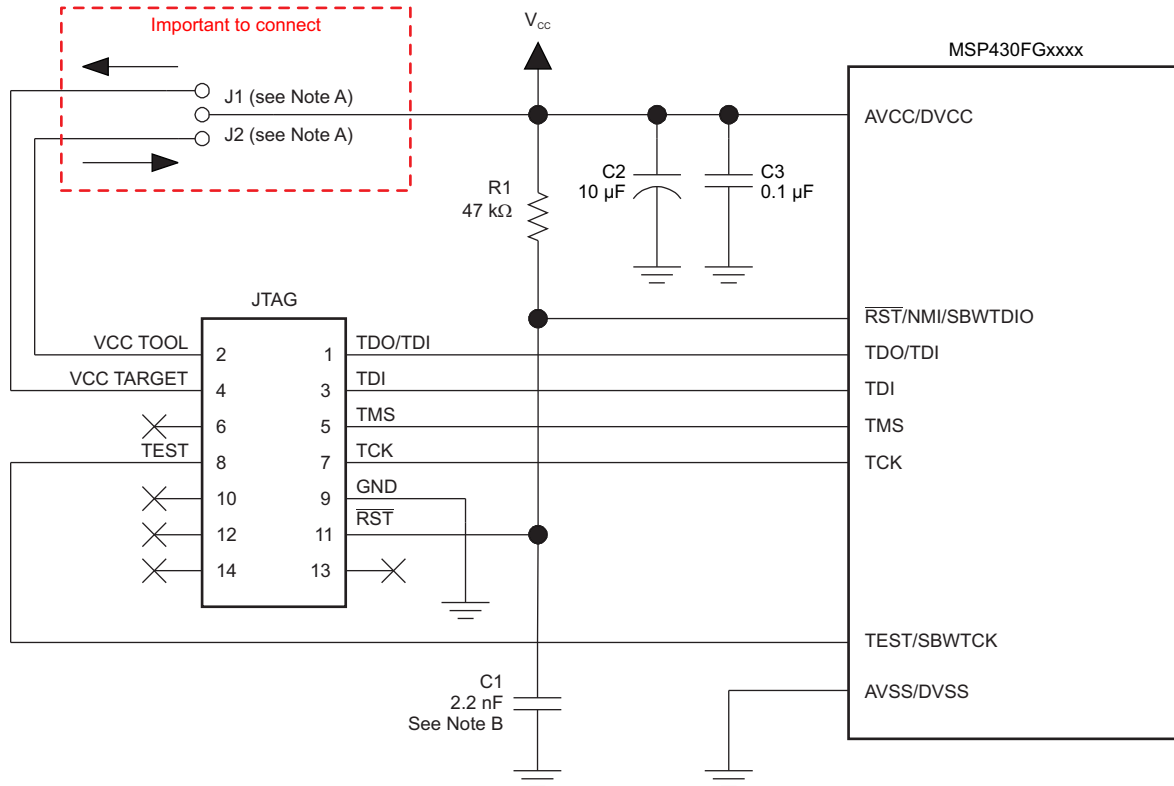
See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. [图 7-3](#) shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. [图 7-4](#) shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

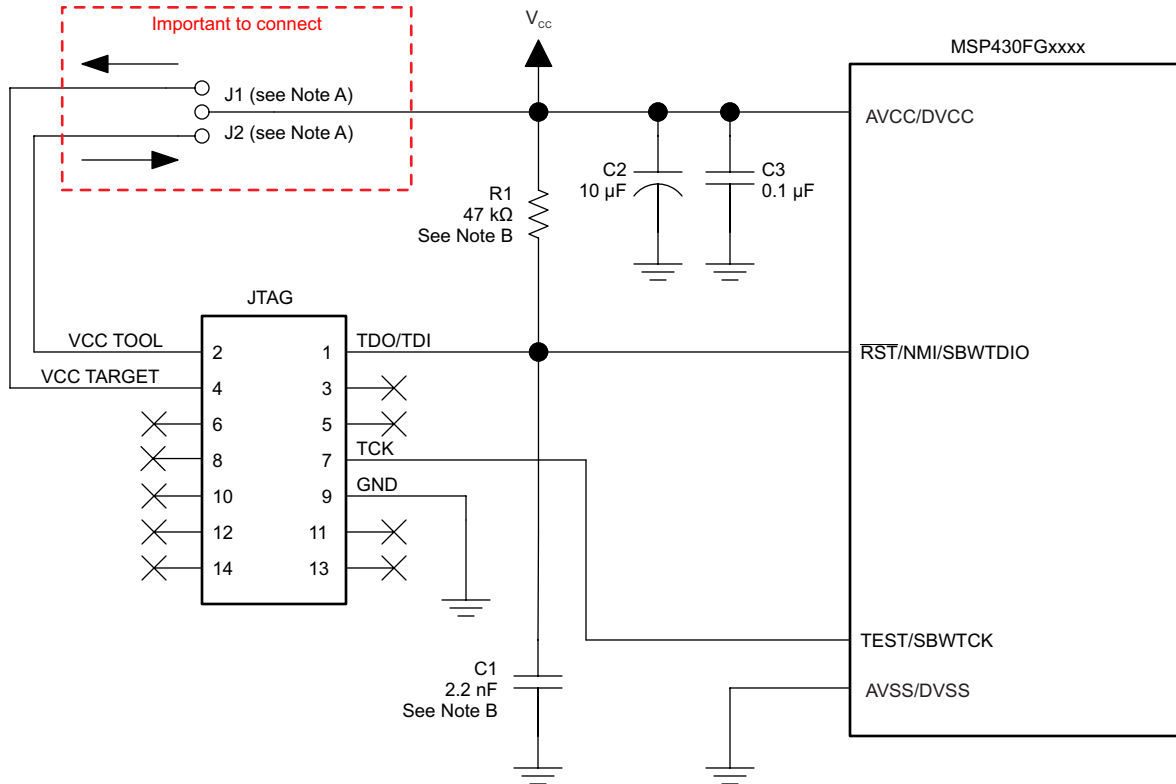
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. [图 7-3](#) and [图 7-4](#) show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



- If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- The upper limit for C1 is 2.2 nF when using current TI tools.

图 7-3. Signal Connections for 4-Wire JTAG Communication



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device  $\overline{\text{RST}}/\text{NMI}/\text{SBWTIO}$  pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

图 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR),  $\text{SFR}_{\text{RPCR}}$ .

In reset mode, the  $\overline{\text{RST}}/\text{NMI}$  pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting  $\text{SYSNMI}$  causes the  $\overline{\text{RST}}/\text{NMI}$  pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by  $\text{SYSNMIIES}$ . Setting the  $\text{NMIIE}$  enables the interrupt of the external NMI. When an external NMI event occurs, the  $\text{NMIIFG}$  is set.

The  $\overline{\text{RST}}/\text{NMI}$  pin can have either a pullup or pulldown that is enabled or not.  $\text{SYSRSTUP}$  selects either pullup or pulldown, and  $\text{SYSRSTRE}$  causes the pullup (default) or pulldown to be enabled (default) or not. If the  $\overline{\text{RST}}/\text{NMI}$  pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the  $\overline{\text{RST}}/\text{NMI}$  pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for more information on the referenced control registers and bits.

### 7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.6](#).

### 7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

### 7.1.7 Do's and Don'ts

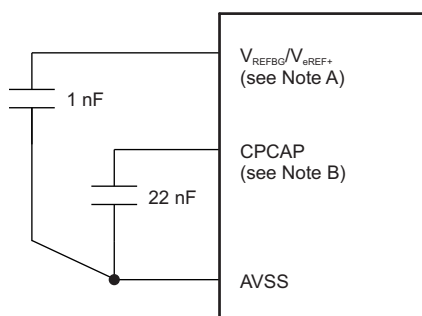
TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 CTSD16 Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see [节 6.12.16](#). When internal connections are available, they should be chosen over external connections to reduce noise and save pins.

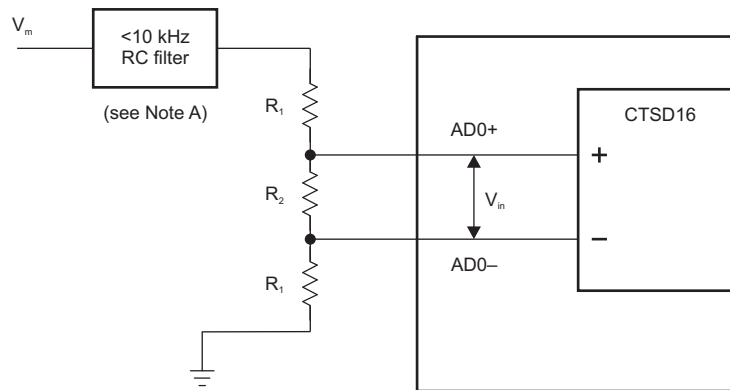
Solid decoupling on both the digital and analog supplies is also required (best with two capacitors, one 1  $\mu$ F and one 100 nF [see [节 7.1.1](#)]).



- The capacitor reduces noise when using internal  $V_{REFBG}$  setting. This pin is also used for the external reference input for the CTSD16 or DAC, and when doing so the capacitor is not needed. Because of the shared signal path and pin, the internal and external references ( $V_{REFBG}$  and  $V_{eREF+}$ , respectively) cannot be used at the same time.
- The capacitor on CPCAP is required when the charge pump is enabled. The charge pump can be enabled by rail-to-rail operation of the CTSD16 or by the OA module. See the register settings for each module in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for enabling this operation.

**图 7-5. CTSD16 Partial Schematic**

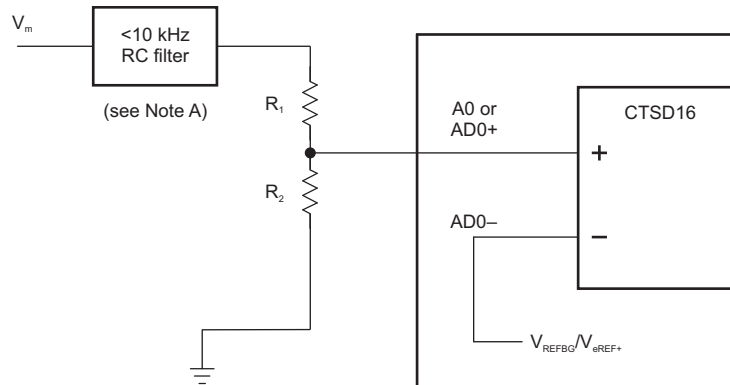
### 7.2.1.1 Example Measurement Schematic – Differential Input



- A. TI recommends an external RC antialiasing low-pass filter for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements. It is up to the user to determine the configuration and type of low-pass filter used.

图 7-6. CTSD16 Measurement Schematic – Differential Input

### 7.2.1.2 Example Measurement Schematic – Single-Ended Input



- A. TI recommends an external RC antialiasing low-pass filter for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements. It is up to the user to determine the configuration and type of low-pass filter used.

图 7-7. CTSD16 Measurement Schematic – Single-Ended Input

### 7.2.1.3 Design Requirements

As with any high-resolution ADC, appropriate printed circuit board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. Therefore, solid decoupling on both the digital and analog supplies is required (best with two capacitors, one 1  $\mu$ F and one 100 nF [see 节 7.1.1]).

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

If the internal reference is used, the reference voltage should be buffered externally by connecting a small (approximately 1 nF) capacitor to the VREFBG pin to reduce the noise on the reference.

The CTSD16 has a fixed 1.024-MHz clock ( $f_M$ ). Fault flags for this oscillator are described in the CTSD16 and UCS section of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

Rail-to-rail operation mode is available when the OA module is used to buffer the CTSD16 inputs. For more information, see the CTSD16 and the OA modules in the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

## 7.2.1.4 Detailed Design Procedure

### 7.2.1.4.1 OSR and Sampling Frequency

A simple equation guides the relationship between effective sampling frequency and oversampling ratio (OSR) for CTSD16.

$$f_s = \frac{f_m}{\text{OSR}} \quad (2)$$

Where

- $f_s$  = effective sampling frequency
- $f_m$  = modulation frequency

For the CTSD16, the modulation frequency is set to 1.024 MHz. Using [公式 2](#) with an example OSR of 256, the effective sampling frequency would be 4 kHz. The OSR value also affects the number of bits in the digital filter output. See the CTSD16 chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for additional information and available OSR values.

### 7.2.1.4.2 Differential Input Range Explanation

The following equations can give guidance on the input range for the CTSD16 while using an external reference. Keep in mind the absolute bounds of an external reference as mentioned in the specifications section of this module. The external and internal references cannot be used at the same time, because they share the same signal path and pin. For internal reference ranges, see [Section 5.8.11](#).

$$V_{\text{FSR}+} = \frac{+V_R}{\text{GAIN}} \quad (3)$$

$$V_{\text{FSR}-} = \frac{-V_R}{\text{GAIN}} \quad (4)$$

$$\text{Full-Scale Range} = V_{\text{FSR}+} - V_{\text{FSR}-} = 2 \times \frac{V_R}{\text{GAIN}} \quad (5)$$

$$V_{\text{ID}} = 0.8 V_{\text{FSR}-} \text{ to } 0.8 V_{\text{FSR}+}, \text{ with externally sourced } V_R \quad (6)$$

Where

- $V_{\text{FSR}}$  is the full-scale range voltage
- $V_{\text{ID}}$  is the differential input voltage
- $V_R$  is the reference voltage

The differential input voltage range with internal voltage reference at different GAIN settings is given in [Section 5.8.11](#). Using [公式 3](#) through [公式 6](#), determine the absolute maximum differential input ranges for the CTSD16 with a given external voltage reference. [公式 7](#) corresponds to the example circuit in [图 7-6](#) and can be used after a range is chosen to limit differential input voltage to acceptable levels by solving for the external resistors R1 and R2.

$$V_{in} = V_m \times \frac{R_2}{R_2 + 2R_1} \times \frac{1}{1 + \frac{R_{eff}}{2R_{in}}} \quad (7)$$

Where

- $R_{eff} = (R_2 \times 2R_1) / (R_2 + 2R_1)$
- $V_{in}$  is the differential voltage input to CTSD16
- $V_m$  is the voltage to measure
- $R_{in}$  is the internal resistance of the CTSD16 (see [Section 5.8.11](#))

#### 7.2.1.4.3 Single-Ended Input Mode

The CTSD16 has six single-ended analog inputs and four differential inputs that can be placed in single-ended mode by the CTSDINCHx bits in the CTSD16INCTLx registers. These single-ended modes use the fully differential path of the CTSD16 by internally tying the negative input to the  $V_{REFBG}/V_{eREF+}$  signal. This means for the differential inputs in single-ended mode, the external pin normally tied to the negative input can be used for its alternate functions. [公式 8](#) through [公式 11](#) apply for full-scale range while in single-ended mode.

$$V_{FSR+} = V_R + \frac{V_R}{GAIN} \quad (8)$$

$$V_{FSR-} = V_R - \frac{V_R}{GAIN} \quad (9)$$

$$\text{Full-Scale Range} = V_{FSR+} - V_{FSR-} = \left( V_R + \frac{V_R}{GAIN} \right) - \left( V_R - \frac{V_R}{GAIN} \right) = 2 \times \frac{V_R}{GAIN} \quad (10)$$

$$V_I = V_R - 0.8 \times \left( \frac{V_R}{GAIN} \right) \text{ to } V_R + 0.8 \times \left( \frac{V_R}{GAIN} \right) \quad (11)$$

Where

- $V_{FSR}$  is the full-scale range voltage
- $V_I$  is the single-ended input voltage range for data-sheet specified performance
- $V_R$  is the reference voltage

To ensure the measured voltage is within the single-ended voltage range, a simple voltage divider circuit can be used to condition the desired input signal. In single-ended mode, additional error may be introduced by noise when compared to a fully differential measurement. [公式 12](#) corresponds to the example circuit in [图 7-7](#) and can be used after a range is chosen to limit differential input voltage to acceptable levels by solving for the external resistors R1 and R2.

$$V_{in} = V_m \times \frac{R_2}{R_1 + R_2} \quad (12)$$

Where

- $V_{in}$  is the single-ended voltage input to CTSD16
- $V_m$  is the voltage to measure

#### 7.2.1.4.4 Offset Calibration

In some applications, it is necessary to calibrate the module for offset error. This module allows an easy way to do this by providing internal connections from input to VREF or DAC0. To short AD4+ and AD4- to VREF or DAC0, change the CTSD16INCHx setting for each channel to 0x11 for VREF and 0x12 for DAC0. This allows calibration of the CTSD16 input stage by what is measured from the ideal value. The total signal chain offset depends on the impedance of the external circuitry; thus, the actual offset seen at any of the analog inputs may be different.

### 7.2.1.5 Layout Guidelines

Components that are shown in the partial schematic (see 图 7-5) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

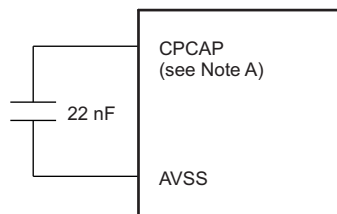
The analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

## 7.2.2 Operational Amplifier With Ground Switches Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see 节 6.12.16. When internal connections are available, they should be chosen over external connections to reduce noise and save pins.

Solid decoupling on both the digital and analog supplies is also required (best with two capacitors, one 1  $\mu$ F and one 100 nF [see 节 7.1.1]).

### 7.2.2.1 Reference Schematic



- A. The capacitor on CPCAP is required when the charge pump is enabled. The charge pump can be enabled by rail-to-rail operation of the PGA buffers of the CTSD16 or by the OA module. See the register settings for each module in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for enabling this operation.

图 7-8. Op Amp Partial Schematic

### 7.2.2.2 Design Requirements

As with any analog signals, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the signal. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy. For more information about noise and its effects on op amps, see [Noise Analysis in Operational Amplifiers](#).

Rail-to-rail operation mode is available with the OA module at the cost of increased current. This should be used when OA input is near the AVCC rail. See the  $V_{CM}$  specification (see [Section 5.8.14](#)) to see if rail-to-rail operation is required for your application. For more information, see the OA chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

Ground switches are also available for use. See 节 6.12.16 for connections. These ground switches provide a low-ohmic connection to ground to both internal connections and to the external pin. When a ground switch is active, the Digital I/O logic for the corresponding pin is ignored.

### 7.2.2.3 Detailed Design Procedure

Operational amplifiers are a diverse and useful tool in many applications. Some common configurations that might prove to be useful to the user are transimpedance amplifiers to convert currents to voltage, voltage-gain amplifiers, and buffering configurations. For more information about how to design these circuits along with other common configurations, see the following documents.

- *Op Amps for Everyone* (ISBN: 978-0128116487)
- [Handbook of Operational Amplifier Applications](#)
- [Understanding Basic Analog – Ideal Op Amps](#)
- [An Applications Guide for Op Amps](#)

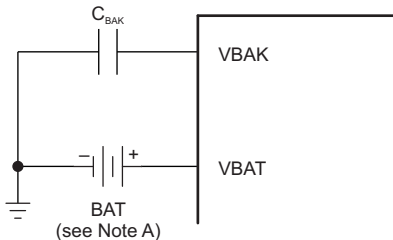
### 7.2.2.4 Layout Guidelines

Components that are shown in the partial schematic (see [图 7-8](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal. Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal. When possible, use internal connections to other modules to limit the potential of error introduction.

## 7.2.3 RTC\_B With Battery Backup System

If not using a separate battery backup supply in the system, see [Section 4.6](#) for VBAT and VBAK connections.

### 7.2.3.1 Partial Schematic



A. BAT can be a battery or super-capacitor. See [Section 5.8.8](#) for specifications.

图 7-9. RTC\_B With Battery Backup Partial Schematic

### 7.2.3.2 Retaining an Accurate Real-Time Clock (RTC) Through Main Supply Interruptions

The RTC\_B module with Battery Backup System is designed to keep an accurate RTC during main supply interruptions and during low-power modes. For more details on when the Backup Battery System engages, see the Battery Backup System chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#). See [Using the MSP430 RTC\\_B Module With Battery Backup Supply](#) for more information and example code on how to keep an accurate RTC through power loss.

### 7.2.3.3 Charging Super-Capacitors With Built-In Resistive Charger

In applications that use a super-capacitor instead of a battery for secondary supply, the charging circuit functionality of the Battery Backup System can be used to charge the super-capacitor. The resistive charger circuit connects VBAT to DVCC with selectable resistor values found in [Section 5.8.8](#). This means that if DVCC is not present, you cannot use this feature to charge a super-capacitor connected to VBAT. The CTSD16 module can be used to sense the voltage level on VBAT divided by a factor of three. Typical values during VBAT sensing are listed in [Section 5.8.8](#). Channel A8 of the CTSD16 is routed internally for this. See the CTSD16 chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#) for more information. The BAKADC bit in the BAKCTL register must also be enabled for this feature to operate.

Additionally, RTC interrupts can be used to wake up from LPMx.5 states to charge the super-capacitor. While in an LPMx.5 state, the super-capacitor on VBAT drains. This means that the "wake up to charge" interrupt interval must be designed so that charging starts before the leftover charge in the super-capacitor is too small to accommodate the worst-case backup time if the system were to suddenly lose power. To estimate this time, use [公式 13](#) for capacitor discharge in an RC circuit.

$$V(t) = V_O e^{-\frac{t}{RC}} \quad (13)$$

Where

- $V_O$  = initial voltage of capacitor
- $t$  = time
- $R$  = circuit resistance
- $C$  = capacitance

Because the operational current is given for when RTC is operating within the specifications section,  $R$  can be replaced with  $V_O/I_{LPM3.5}$  by Ohm's law. By setting  $V(t)$  to the minimum voltage for RTC operation while in backup supply,  $V_O$  as voltage of capacitor when fully charged, and  $C$  as the super-capacitor capacitance, the estimated RTC operation time can be calculated. If periodic wakeups from LPM3.5 are not desirable for a given application, external means of charging the super-capacitor must be implemented by the user.

For a detailed list of when the secondary supply VBAT powers the backup-supplied subsystem, see the Battery Backup System chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

## 7.2.4 LCD\_B Peripheral

### 7.2.4.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, there is flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU which (assuming that the correct choices are made) can be advantageous for the PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However for an example of a schematic using the LCD\_B module with an MSP430F6638, see the [Ultra Low Power Blood Pressure And Heart Rate Monitor Reference Design](#).

### 7.2.4.2 Design Requirements

Due to the flexibility of the LCD\_B peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. There can be well-defined requirements in terms of how many individually addressable LCD segments need to be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use and which are required by other application functions, and what the power budget is, to name just a few. TI strongly recommends reviewing the LCD\_B peripheral module chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) during the initial design requirements and decision process. The following table provides a brief overview over different choices that can be made and their impact.

| OPTION OR FEATURE        | IMPACT OR USE CASE                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Multiplexed LCD          | <ul style="list-style-type: none"> <li>• Enable displays with more segments</li> <li>• Use fewer device pins</li> <li>• LCD contrast decreases as mux level increases</li> <li>• Power consumption increases with mux level</li> <li>• Requires multiple intermediate bias voltages</li> </ul>                                                                                                                    |
| Static LCD               | <ul style="list-style-type: none"> <li>• Limited number of segments that can be addressed</li> <li>• Use a relatively large number of device pins</li> <li>• Use the least amount of power</li> <li>• Use only <math>V_{CC}</math> and GND to drive LCD signals</li> </ul>                                                                                                                                        |
| Internal Bias Generation | <ul style="list-style-type: none"> <li>• Simpler solution – no external circuitry</li> <li>• Independent of <math>V_{LCD}</math> source</li> <li>• Somewhat higher power consumption</li> </ul>                                                                                                                                                                                                                   |
| External Bias Generation | <ul style="list-style-type: none"> <li>• Requires external resistor ladder divider</li> <li>• Resistor size depends on display</li> <li>• Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load)</li> <li>• External resistor ladder divider can be stabilized through capacitors to reduce ripple</li> </ul>                    |
| Internal Charge Pump     | <ul style="list-style-type: none"> <li>• Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications)</li> <li>• Programmable voltage levels allow software-driven contrast control</li> <li>• Requires an external capacitor on the LCD CAP pin</li> <li>• Higher current consumption than simply using <math>V_{CC}</math> for the LCD driver</li> </ul> |

### 7.2.4.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD\_B peripheral module and the display itself. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is necessary:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, the segment  $S_x$  and common  $COM_x$  signals are connected to respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the  $S_x$  and  $COM_x$  signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD\_B module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD\_B module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit through a single byte-wide access to an LCDMx register. And consecutive segments are mapped to consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing the most convenient memory layout must be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, refer to the LCD\_B controller chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

For additional design information, see [Designing With MSP430 and Segment LCD](#).

#### 7.2.4.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP pin should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace and also have a solid connection to the ground plane that is supplying the V<sub>SS</sub> pins of the MCU.

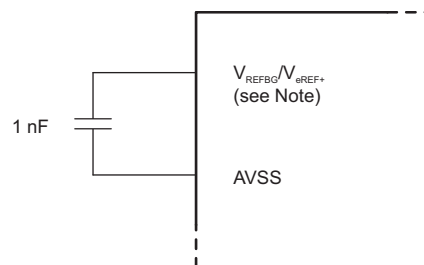
For an example layout of the LCD\_B module with an MSP430F6638, see the [Ultra Low Power Blood Pressure And Heart Rate Monitor Reference Design](#).

#### 7.2.5 DAC12 Peripheral

For internal connections between signal chain modules such as CTSD16, OA, and DAC12, see [节 6.12.16](#). When available, internal connections should be chosen over external ones to reduce noise and save pins.

Solid decoupling on both the digital and analog supplies is required (best with two capacitors per supply, one 1 µF and one 100 nF [see [节 7.1.1](#)]).

##### 7.2.5.1 Partial Schematic



NOTE: The capacitor is used to reduce noise when using internal VREFBG setting. This pin is also used for the external reference input for the CTSD16 or DAC. When using the external reference, the capacitor is not needed. Because of the shared signal path and pin, the internal and external references (VREFBG and VREF+, respectively) cannot be used at the same time.

图 7-10. DAC12 Partial Schematic

##### 7.2.5.2 Design Requirements

As with any analog signals, appropriate printed-circuit-board layout and grounding techniques must be followed to eliminate ground loops, unwanted parasitic effects, and noise.

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the signal. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

### 7.2.5.3 Detailed Design Procedure

Digital-to-analog converters (DACs) can be used in a variety of applications and configurations. This section provides some resources for the user to help get started in a design. For details on example DAC applications, see [Bridging the Divide: A DAC Applications Tutorial \(Precision Signal Path\)](#).

Some DAC applications may need an output buffer to reduce the affect of a load on the DAC output. This buffer can be an external op amp or, on some MSP430 devices, the integrated op amp can be used. For more information on how to configure an op amp for this function, see [节 7.2.2](#).

For more information about DAC applications, see the following application notes:

[High Speed, Digital to Analog Converters Basics](#)

[Design for a Wideband, Differential Transimpedance DAC Output](#)

### 7.2.5.4 Layout Guidelines

Application circuits attached to the DAC output should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal. Avoid routing analog signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal. When possible, use internal connections to other modules to limit the potential of error introduction.

### 7.2.6 USB Module

See the following resources for help with USB design. The application notes contain hardware, software, and application guides and implementations.

[Starting a USB Design Using MSP430 MCUs](#)

[USB Field Firmware Updates on MSP430 MCUs](#)

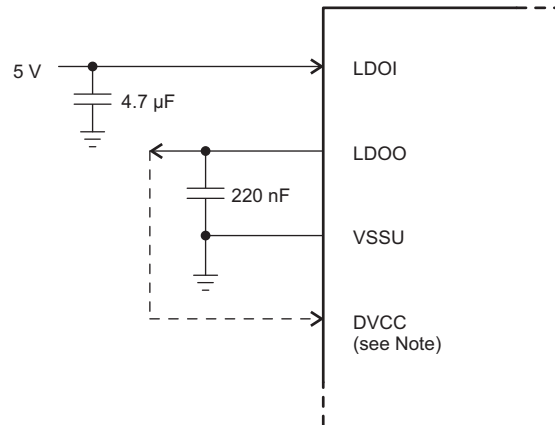
[MSP430 USB Developers Package](#)

## 7.2.7 LDO Module

Solid decoupling on both the digital and analog supplies is required (best with two capacitors per supply, one 1  $\mu$ F and one 100 nF [see 节 7.1.1]).

The LDO module is in its own power domain on chip (separate from DVCC). To use the Port U pins (PU.0 and PU.1) this domain must be powered. If use of the Port U pins is needed and no voltage is supplied to LDOI, then a 3.3-V supply to LDOO is needed. LDOO can act as an input only when the 3.3-V LDO is not enabled. When the 3.3-V LDO is not needed in applications, keep LDOI tied low to make sure that the LDO module does not draw excessive current when disabled.

### 7.2.7.1 Partial Schematic



- A. Connection between LDOO and DVCC is optional. If connected, the LDO powers the device. LDOO can also supply other subsystems in the application if the maximum output current for the LDO is not exceeded (see the LDO power system specifications in Table 5-53).

图 7-11. LDO Partial Schematic

## 8 器件和文档支持

### 8.1 使用入门

有关 MSP430™ 系列器件以及开发协助工具和库的更多信息，请访问 [MSP430 超低功耗传感和测量 MCU 概述](#)。

### 8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [图 8-1](#) provides a legend for reading the complete device name.

|                                      |                                                                                                                                |                                                                                                                                                                                             |
|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>MSP 430 F 5 438 A I ZQW T -EP</b> |                                                                                                                                |                                                                                                                                                                                             |
| Processor Family                     | MCU Platform                                                                                                                   | Optional: Additional Features                                                                                                                                                               |
| Device Type                          | Series                                                                                                                         | Optional: Tape and Reel                                                                                                                                                                     |
| Feature Set                          | Optional: Temperature Range                                                                                                    | Packaging                                                                                                                                                                                   |
| Optional: A = Revision               |                                                                                                                                |                                                                                                                                                                                             |
| <b>Processor Family</b>              | CC = Embedded RF Radio<br>MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon<br>PMS = Prototype Device                 |                                                                                                                                                                                             |
| <b>MCU Platform</b>                  | 430 = MSP430 low-power microcontroller platform                                                                                |                                                                                                                                                                                             |
| <b>Device Type</b>                   | <b>Memory Type</b><br>C = ROM<br>F = Flash<br>FR = FRAM<br>G = Flash or FRAM (Value Line)<br>L = No Nonvolatile Memory         | <b>Specialized Application</b><br>AFE = Analog Front End<br>BQ = Contactless Power<br>CG = ROM Medical<br>FE = Flash Energy Meter<br>FG = Flash Medical<br>FW = Flash Electronic Flow Meter |
| <b>Series</b>                        | 1 = Up to 8 MHz<br>2 = Up to 16 MHz<br>3 = Legacy<br>4 = Up to 16 MHz with LCD                                                 | 5 = Up to 25 MHz<br>6 = Up to 25 MHz with LCD<br>0 = Low-Voltage Series                                                                                                                     |
| <b>Feature Set</b>                   | Various levels of integration within a series                                                                                  |                                                                                                                                                                                             |
| <b>Optional: A = Revision</b>        | N/A                                                                                                                            |                                                                                                                                                                                             |
| <b>Optional: Temperature Range</b>   | S = 0°C to 50°C<br>C = 0°C to 70°C<br>I = -40°C to 85°C<br>T = -40°C to 105°C                                                  |                                                                                                                                                                                             |
| <b>Packaging</b>                     | <a href="http://www.ti.com/packaging">http://www.ti.com/packaging</a>                                                          |                                                                                                                                                                                             |
| <b>Optional: Tape and Reel</b>       | T = Small reel<br>R = Large reel<br>No markings = Tube or tray                                                                 |                                                                                                                                                                                             |
| <b>Optional: Additional Features</b> | -EP = Enhanced Product (-40°C to 105°C)<br>-HT = Extreme Temperature Parts (-55°C to 150°C)<br>-Q1 = Automotive Q100 Qualified |                                                                                                                                                                                             |

图 8-1. Device Nomenclature

## 8.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。请参阅 [MSP430 超低功耗 MCU – 工具与软件](#)，了解所有工具。

表 8-1 列出了 MSP430FG662x 和 MSP430FG642x MCU 的调试功能。请参阅《适用于 MSP430 的 Code Composer Studio IDE 用户指南》，以了解可用功能的详细信息。

表 8-1. 硬件调试特性

| MSP430 架构 | 四线制 JTAG | 两线制 JTAG | 断点 (N) | 范围断点 | 时钟控制 | 状态序列发生器 | 跟踪缓冲器 | LPMx.5 调试支持 | EnergyTrace++™ 技术 |
|-----------|----------|----------|--------|------|------|---------|-------|-------------|-------------------|
| MSP430Xv2 | 有        | 是        | 8      | 是    | 是    | 是       | 是     | 否           | 否                 |

### 设计套件与评估模块

**MSP-TS430PZ100AUSB - 适用于 MSP430FG6x MCU 的 100 引脚目标开发板** MSP-TS430PZ100AUSB 是一款独立的 100 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy-Bi-Wire（两线制 JTAG）协议在系统内对 MSP430 MCU 进行编程和调试。

**教育版 BoosterPack MKII** 教育版 BoosterPack MKII 为开发者提供高度集成方案以快速获得完整解决方案的原型设计。各种模拟和数字输入/输出供您使用，包括模拟游戏手柄、环境和运动传感器、RGB LED、麦克风、蜂鸣器、彩色 LCD 显示屏等。

### 软件

**MSP430Ware™ 软件** MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件可作为 Code Composer Studio™IDE 的一部分提供，也可以以独立软件包的形式提供。

**MSP430FG662x、MSP430FG642x 代码示例** 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

**MSP 驱动程序库** MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可使用驱动程序库函数以尽可能低的费用编写全部项目。

**电容式触摸软件库** 可在 MSP430 MCU 启用电容触控功能的免费 C 代码库。MSP430 MCU 库版本采用多种电容触控实现方法，包括 RO 和 RC 方法。

**MSP EnergyTrace™ 技术** 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

**ULP（超低功耗）Advisor** ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器独特功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

**IEC60730 软件包** IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 MCU 中运行的客户应用，从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

**适用于 MSP 的定点数学运算库** MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时应用，而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

**适用于 MSP430 的浮点数学运算库** TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。此标量函数的浮点数学运算库，能够充分利用器件的智能外设，使速度最高达到标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

## 开发工具

**适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境** Code Composer Studio 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。Code Composer Studio IDE 包含一整套用于开发和调试嵌入式应用的嵌入式软件实用工具。Code Composer Studio IDE 包含用于优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、性能评测工具以及多种其他功能。

**MSPWare 软件** MSPWare 软件集合了所有 MSP 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有设计资源的完整集合外，MSPWare 软件还包含名为 MSP 驱动程序库的高级 API。该库可简化针对 MSP 硬件的编程操作。MSPWare 软件以 Code Composer Studio IDE 组件或独立软件包两种形式提供。

**命令行编程器** MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件 (.txt 或 .hex 文件) 直接下载到 MSP 微控制器，而无需使用 IDE。

**MSP MCU 编程器和调试器** MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

**MSP-GANG 生产编程器** MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

## 8.4 文档支持

以下文档对 MSP430FG662x 和 MSP430FG642x MCU 进行了介绍。[www.ti.com.cn](http://www.ti.com.cn) 网站上提供了这些文档的副本。

### 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 [ti.com.cn](http://ti.com.cn) 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

### 勘误

《MSP430FG6626 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430FG6625 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430FG6426 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430FG6425 器件勘误表》 介绍功能规格的已知例外情况。

### 用户指南

《MSP430F5xx 和 MSP430F6xx 系列用户指南》 详细介绍了该器件系列提供的模块和外设。

《MSP430 闪存器件引导加载程序 (BSL) 用户指南》 MSP430 引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器（RAM）可根据相关要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导装载程序混为一谈。

《通过 JTAG 接口对 MSP430 进行编程》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

《MSP430 硬件工具用户指南》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

### 应用报告

《使用 MSP430 和段式 LCD 进行设计》 从智能电表，到电子货架标签 (ESL)，再到医疗设备，各式各样的应用 都需要使用段式液晶显示屏 (LCD) 为用户 提供相关信息。部分 MSP430™ 微控制器系列内置低功耗 LCD 驱动电路，MSP430 MCU 借此能够直接控制段式 LCD 玻璃。本应用手册可帮助您理解段式 LCD 的工作原理、MSP430 MCU 系列各种 LCD 模块的不同特性， 并提供了 LCD 硬件布线技巧、编写高效易用的 LCD 驱动软件的相关指导以及 具有不同 LCD 特性的 MSP430 器件的 产品组合概述， 旨在协助您进行器件选型。

《**MSP430 32kHz 晶体振荡器**》 对于稳定的晶体振荡器，选择合适的晶振、正确的负载电路和适当的电路板布局布线至关重要。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《**MSP430 系统级 ESD 注意事项**》 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

《**使用具有电池备用电源的 MSP430 RTC\_B 模块**》 有些应用需要在发生电池更换、断电和其他事件期间保持精确的实时时钟 (RTC)。对于此类应用，包含具有电池备用系统的 RTC\_B 实时时钟模块的 MSP430™ 器件非常适用。该应用手册展示了如何使用具有电池备用电源功能的 RTC\_B 在失去主电源期间保持时间并保持 RTC 计数，以及在主电源恢复时正确处理重新初始化。

## 8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 8-2. 相关链接

| 器件           | 产品文件夹                 | 立即订购                  | 技术文档                  | 工具与软件                 | 支持和社区                 |
|--------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| MSP430FG6626 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| MSP430FG6625 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| MSP430FG6426 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| MSP430FG6425 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |

## 8.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的《使用条款》。

### TI E2E™ 社区

TI 的工程师交流 (E2E) 社区。此社区的创建目的是为了促进工程师之间协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

### TI 嵌入式处理器维基网页

德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

## 8.7 商标

MSP430, MSP430Ware, Code Composer Studio, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 8.8 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 8.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 机械、封装和可订购信息

### 9.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FG6425IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FG6425                  | <a href="#">Samples</a> |
| MSP430FG6426IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FG6426                  | <a href="#">Samples</a> |
| MSP430FG6625IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FG6625                  | <a href="#">Samples</a> |
| MSP430FG6626IPZ   | ACTIVE        | LQFP         | PZ                 | 100  | 90             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FG6626                  | <a href="#">Samples</a> |
| MSP430FG6626IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FG6626                  | <a href="#">Samples</a> |
| MSP430FG6626IZCAR | ACTIVE        | NFBGA        | ZCA                | 113  | 2500           | RoHS & Green    | Call TI                              | Call TI              | -40 to 85    | FG6626                  | <a href="#">Samples</a> |
| MSP430FG6626IZCAT | ACTIVE        | NFBGA        | ZCA                | 113  | 250            | RoHS & Green    | Call TI                              | Call TI              | -40 to 85    | FG6626                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

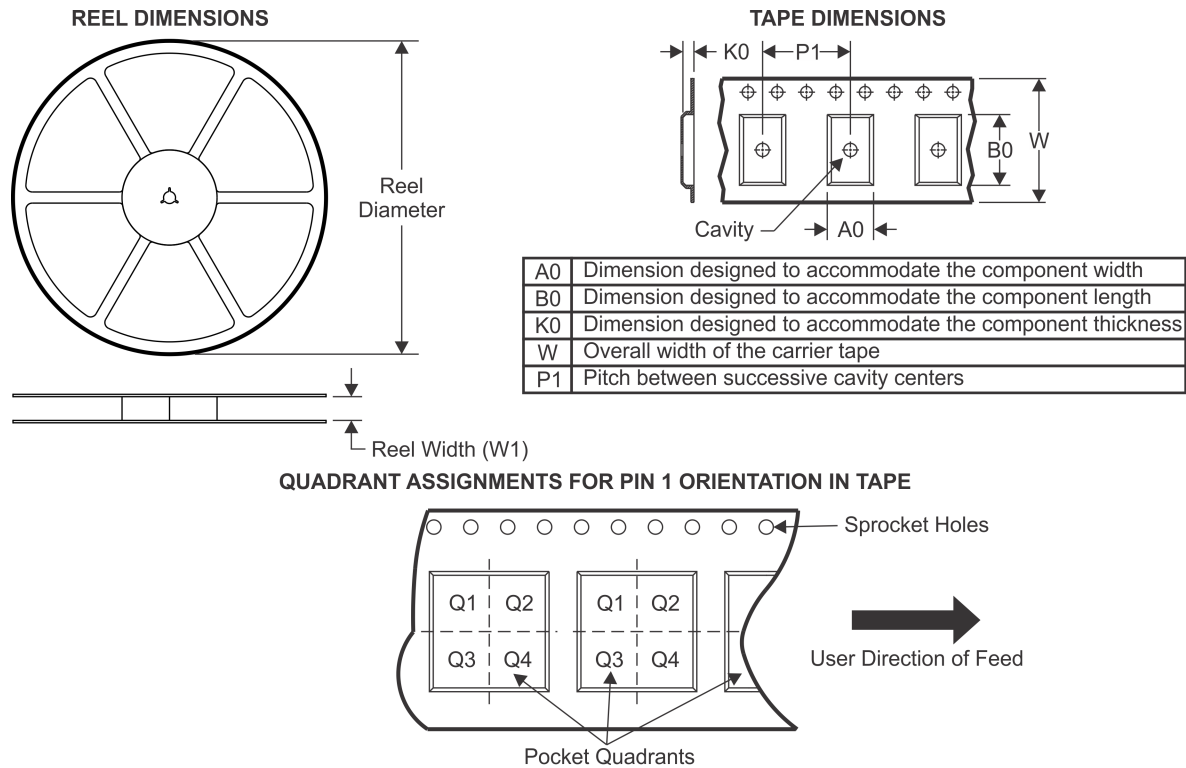
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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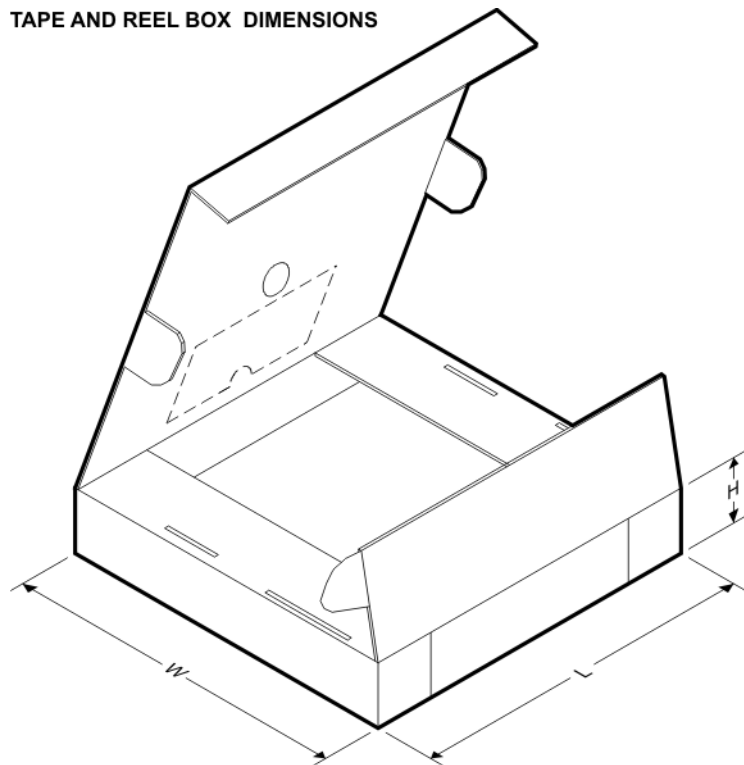
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FG6425IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430FG6426IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430FG6625IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430FG6626IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430FG6626IZCAR | NFBGA        | ZCA             | 113  | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q1            |
| MSP430FG6626IZCAT | NFBGA        | ZCA             | 113  | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

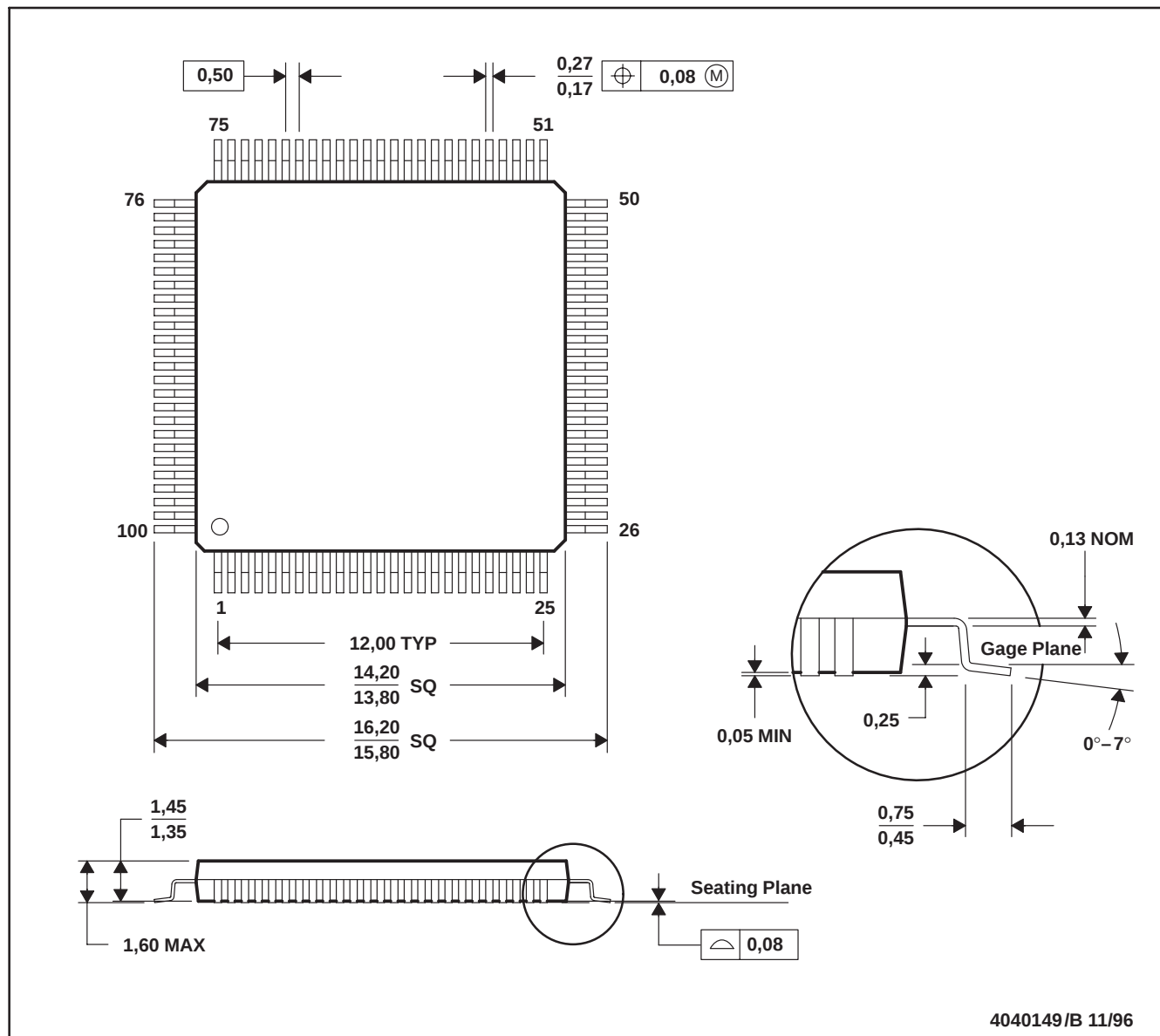


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FG6425IPZR  | LQFP         | PZ              | 100  | 1000 | 350.0       | 350.0      | 43.0        |
| MSP430FG6426IPZR  | LQFP         | PZ              | 100  | 1000 | 350.0       | 350.0      | 43.0        |
| MSP430FG6625IPZR  | LQFP         | PZ              | 100  | 1000 | 350.0       | 350.0      | 43.0        |
| MSP430FG6626IPZR  | LQFP         | PZ              | 100  | 1000 | 350.0       | 350.0      | 43.0        |
| MSP430FG6626IZCAR | NFBGA        | ZCA             | 113  | 2500 | 350.0       | 350.0      | 43.0        |
| MSP430FG6626IZCAT | NFBGA        | ZCA             | 113  | 250  | 213.0       | 191.0      | 55.0        |

## PZ (S-PQFP-G100)

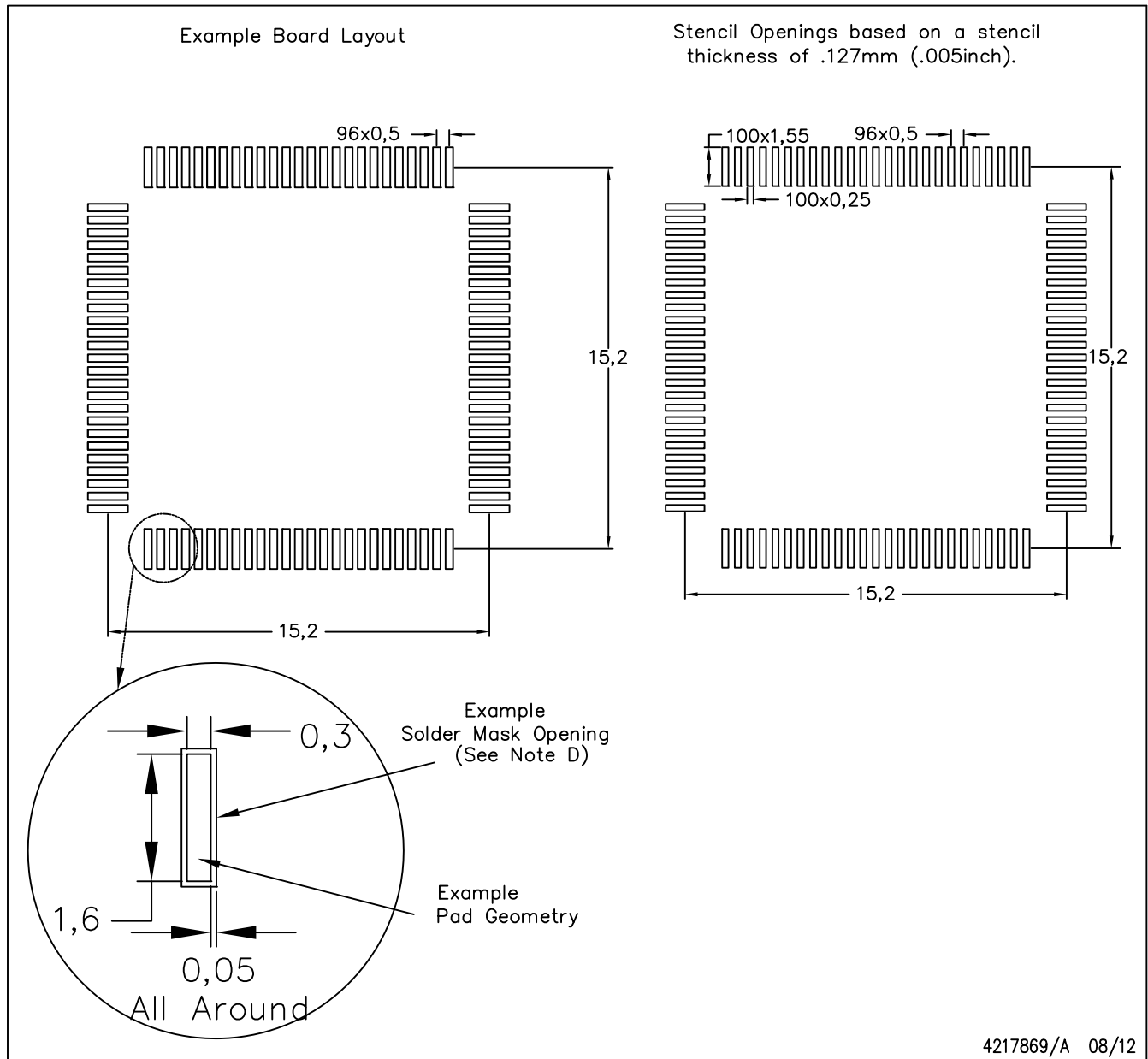
## PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026

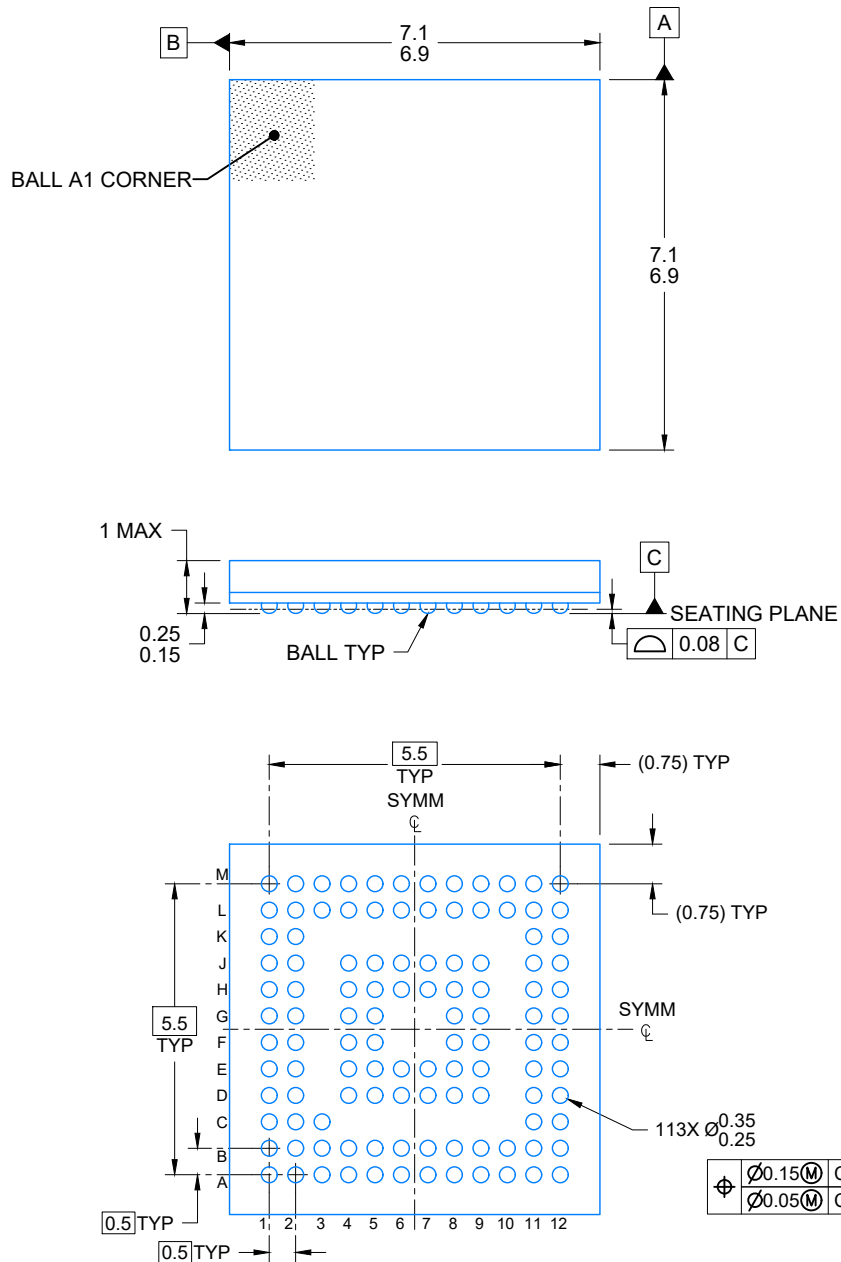
PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

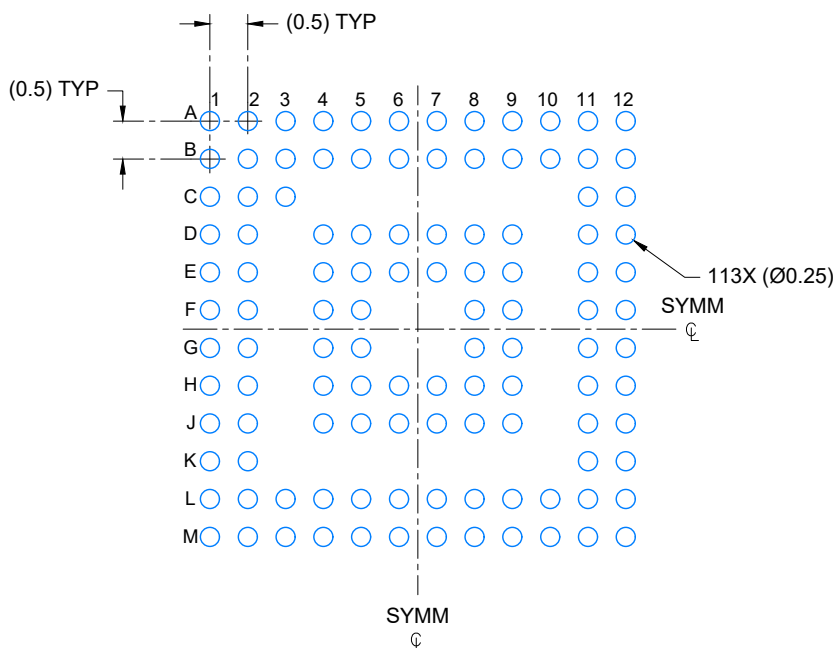


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## NOTES:

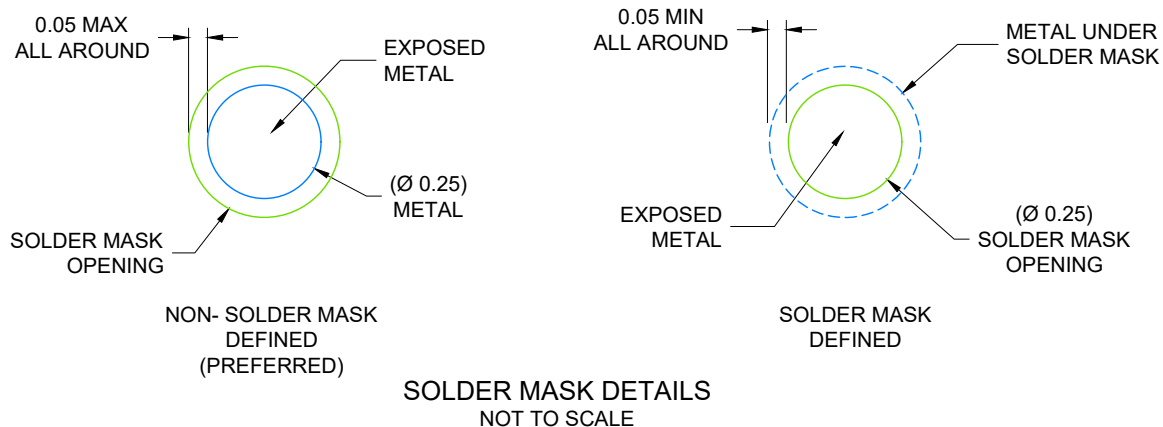
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

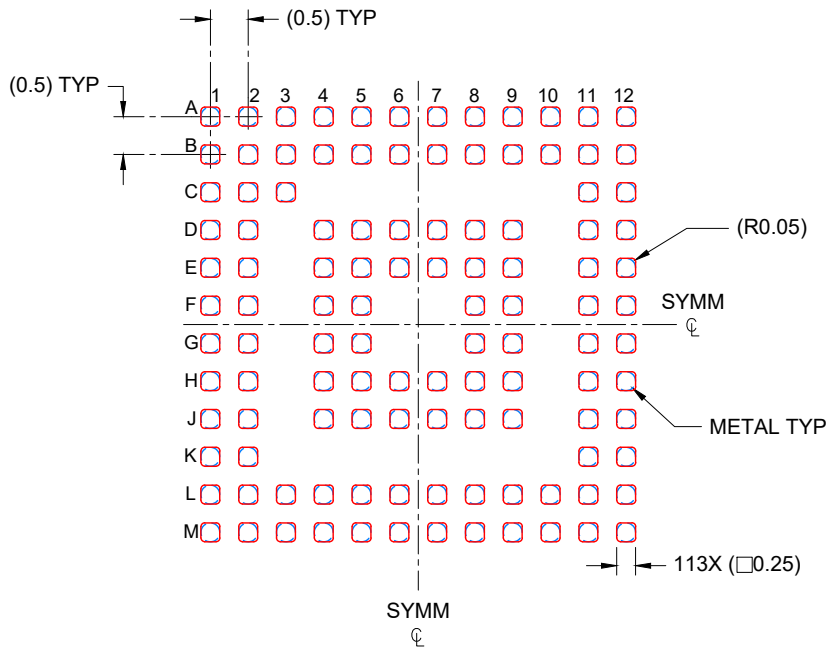
SCALE: 10X



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NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



SOLDER PASTE EXAMPLE  
BASED ON 0.100 mm THICK STENCIL  
SCALE: 10X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## 重要声明和免责声明

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