MSP430F14x、MSP430F14x1、MSP430F13x 混合信号微控制器

1 器件概述

1.1 特性

- 低电源电压范围：1.8V 至 3.6V
- 超低功耗：
  - 激活模式：280μA（在 1MHz 频率和 2.2V 电压条件下）
  - 待机模式：1.6μA
  - 关闭模式（RAM 保持）：0.1μA
- 5 种省电模式
- 可在不到 6μs 的时间内从待机模式唤醒
- 16 位精简指令集 (RISC) 架构，125ns 指令周期时间
- 具有内部基准、采样保持和自动扫描功能的 12 位模数转换器 (ADC)
- 具有 7 个捕捉/比较及影子寄存器的 16 位 Timer_B
- 具有 3 个捕捉/比较寄存器的 16 位 Timer_A
- 片载比较器
- 串行板上编程、无需外部编程电压、通过安全保险丝实现的可编程代码保护
- 串行通信接口 (USART)，作为异步 UART 或同步 SPI 接口
  - MSP430F14x 和 MSP430F14x1 器件上有两个 USART（USART0、USART1）
  - MSP430F13x 器件上有一个 USART (USART0)
- 系列成员（另请参阅 器件比较）
  - MSP430F133
    - 8KB + 256B 闪存，256B RAM
  - MSP430F135
    - 16KB + 256B 闪存，512B RAM
  - MSP430F147、MSP430F1471
    - 32KB + 256B 闪存，1KB RAM
  - MSP430F148、MSP430F1481
    - 48KB + 256B 闪存，2KB RAM
  - MSP430F149、MSP430F1491
    - 60KB + 256B 闪存，2KB RAM

1.2 应用

- 传感器系统
- 工业控制
- 手持仪表

1.3 说明

德州仪器 (TI) MSP430™系列的超低功耗微控制器 (MCU) 包含多款器件，这些器件配备了不同的外设集以满足各类 应用的需求。该架构可与五种低功耗模式配合使用，专为在便携式测量应用中延长电池使用寿命而进行了 优化。该器件 具有 功能强大的 16 位 RISC CPU、16 位寄存器和有助于获得最大编码效率的常数发生器。数控振荡器 (DCO) 可在不到 6μs 的时间内完成从低功耗模式到激活模式的唤醒。

MSP430F13x、MSP430F14x 和 MSP430F14x1 MCU 支持两个内置 16 位计时器、快速 12 位 ADC（在 MSP430F13x 和 MSP430F14x 器件上）、一个 USART（在 MSP430F13x 器件上）或两个 USART（在 MSP430F14x 和 MSP430F14x1 器件上），以及 48 个 I/O 引脚。硬件乘法器可提高性能，并提供型号众多且具有代码和硬件兼容性的器件系列解决方案。

要获得完整的模块说明，请参见《MSP430x1xx 系列用户指南》。

器件信息(1)

部件号	封装	封装尺寸(2)
MSP430F149IPM	LQFP (64)	10mm × 10mm
MSP430F149IPAG	TQFP (64)	10mm × 10mm
MSP430F1491IRTD	VQFN (64)	9mm × 9mm

(1) 要获得最新的器件、封装和订购信息，请参见*封装选项附录*（节 8），或者访问 TI 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 8）。

1.4 功能框图

图 1-1 显示了 MSP430F13x MCU 的功能方框图。

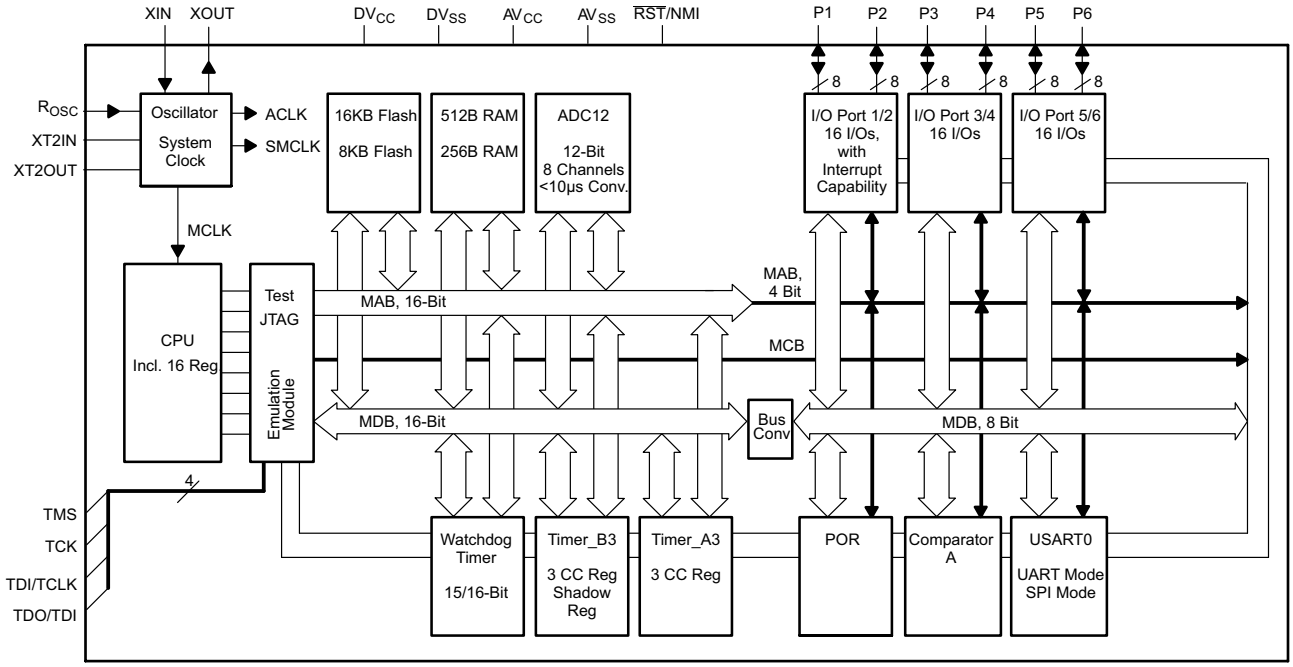


图 **1-1.** 功能方框图，**MSP430F13x**

图 1-2 显示了 MSP430F14x MCU 的功能方框图。

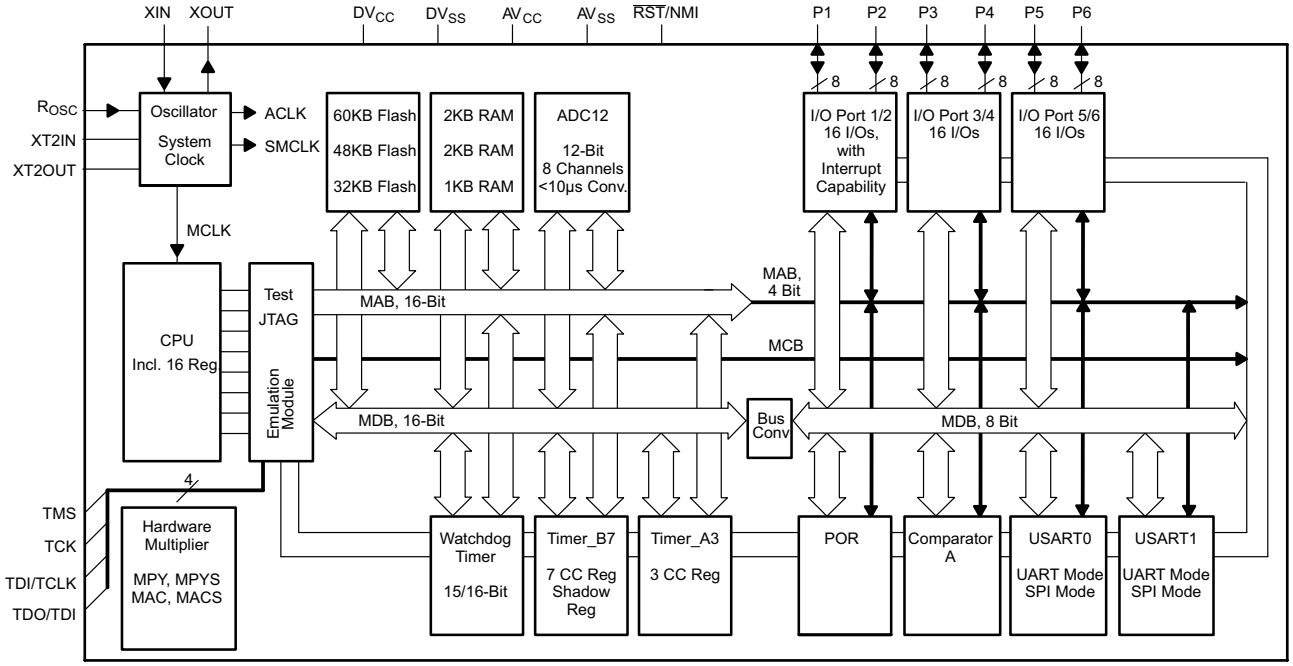


图 1-2. 功能方框图，MSP430F14x

图 1-3 显示了 MSP430F14x1 MCU 的功能方框图。

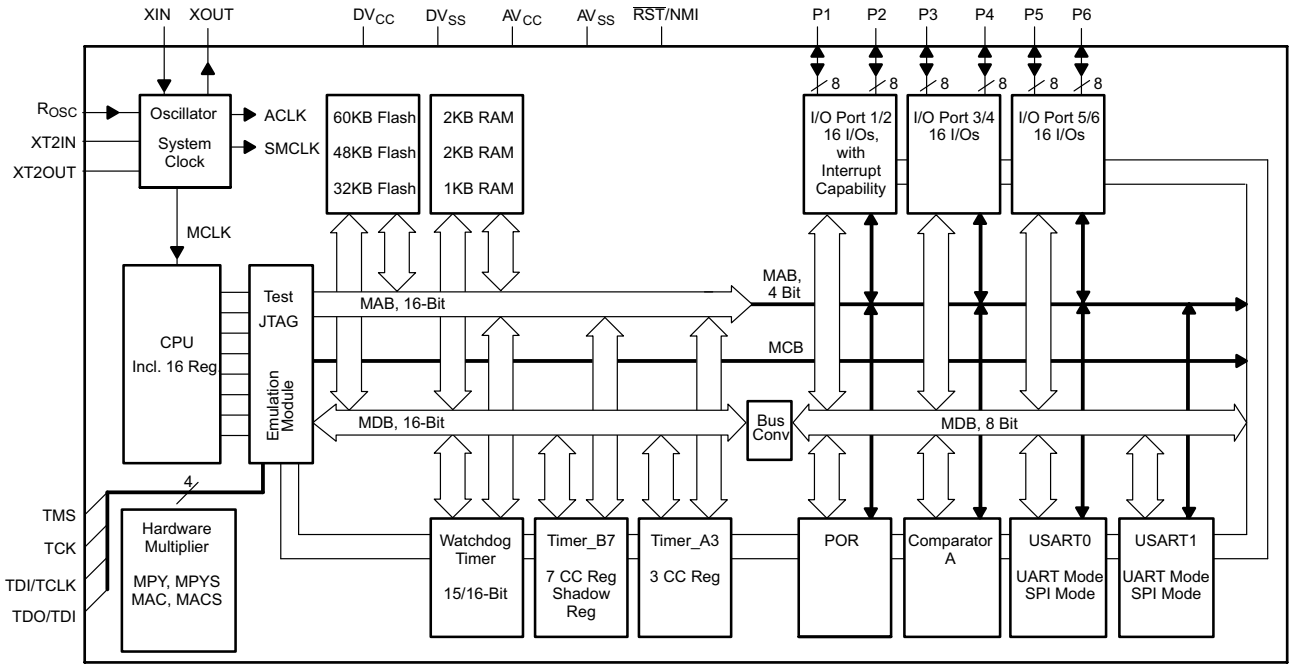


图 1-3. 功能方框图，MSP430F14x1

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from February 12, 2009 to May 23, 2018 **Page**

- 通篇更改了文档的格式和组织结构 1
- 添加了节 1.2*应用* 1
- Added Section 3, *Device Comparison* 6
- Added Section 5.2, *ESD Ratings* 16
- Removed note (2) with duplicate information from the f_{LFXT1} parameter in Section 5.3, *Recommended Operating Conditions* 16
- Removed duplicate conditions "XTS = 0, SELM = 0 or 1" from the second row of Test Conditions on the $I_{(AM)}$ parameter in Section 5.4, *Supply Current Into AV_{CC} and DV_{CC} Excluding External Current* 17
- Added Section 5.5, *Thermal Resistance Characteristics* 18
- Removed ADC12DIV from the equation in the TYP value of the $t_{CONVERT}$ parameter (because ADC12CLK is after division) in Section 5.26, *12-Bit ADC, Timing Parameters* 30
- Changed all instances of *bootstrap loader* to *bootloader* throughout document 35
- 添加了节 7*器件和文档支持* 59

3 Device Comparison

Table 3-1 summarizes the features of the device variants in this data sheet.

Table 3-1. Device Comparison(1)(2)

Device	Flash	SRAM	Timer_A(3)	Timer_B(4)	USART	COMP_A	ADC12 (Channels)	I/Os	Package
MSP430F149	60KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F1491	60KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin RTD
MSP430F148	48KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F1481	48KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin RTD
MSP430F147	32KB	1KB	3	7	2	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F1471	32KB	1KB	3	7	2	1	8	48	64-pin PM 64-pin RTD
MSP430F135	16KB	512 bytes	3	3	1	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F133	8KB	256 bytes	3	3	1	1	8	48	64-pin PM 64-pin PAG 64-pin RTD

(1) For the most current package and ordering information, see the *Package Option Addendum* in 节 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power microcontrollers One platform. One ecosystem. Endless possibilities.

Products for other MSP430 microcontrollers MCUs for metrology, monitoring, system control, and communications

Companion Products for MSP430F149 Review products that are frequently purchased or used with this product.

Reference Designs The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the MSP430F133 and MSP430F135 MCUs in the 64-pin PM, PAG, and RTD packages.

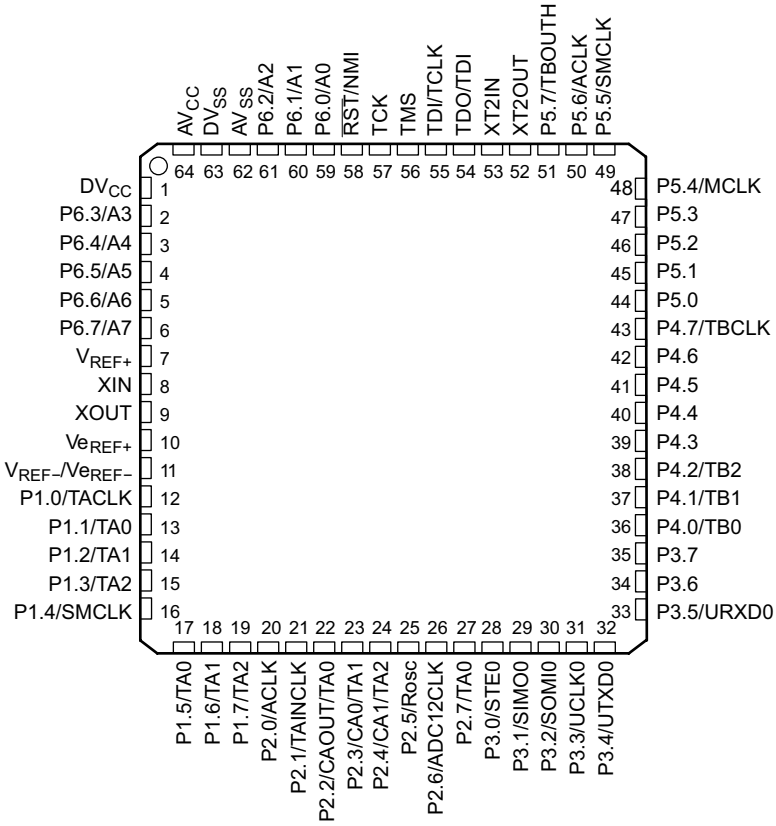


Figure 4-1. 64-Pin PM, PAG, or RTD Package (Top View) for MSP430F133 and MSP430F135

Figure 4-2 shows the pinout for the MSP430F147, MSP430F148, and MSP430F149 MCUs in the 64-pin PM, PAG, and RTD packages.

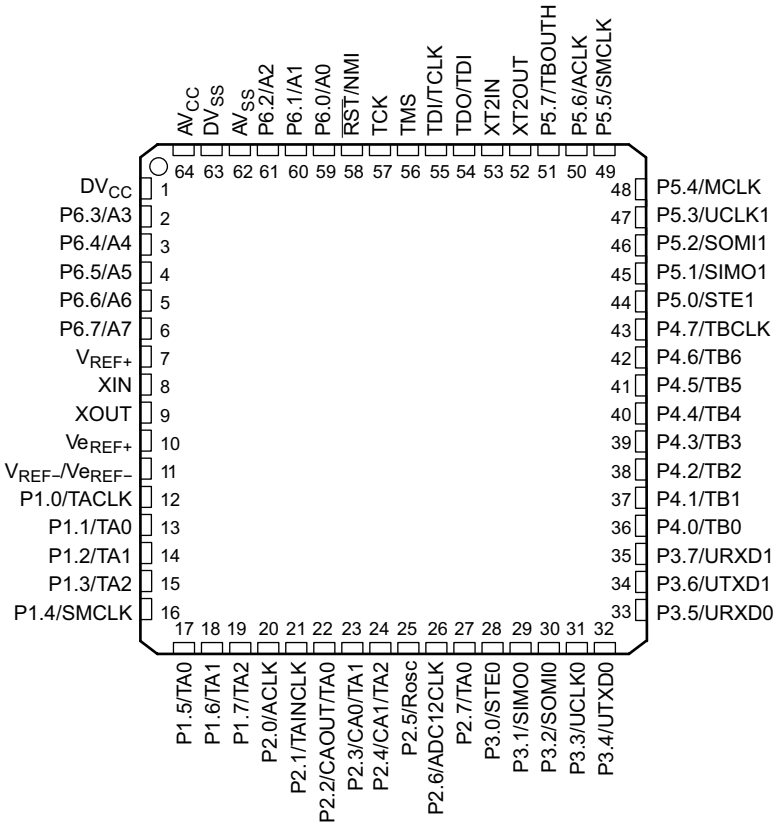


Figure 4-2. 64-Pin PM, PAG, or RTD Package (Top View) for MSP430F147, MSP430F148, and MSP430F149

Figure 4-3 shows the pinout for the MSP430F1471, MSP430F1481, and MSP430F1491 MCUs in the 64-pin PM and RTD packages.

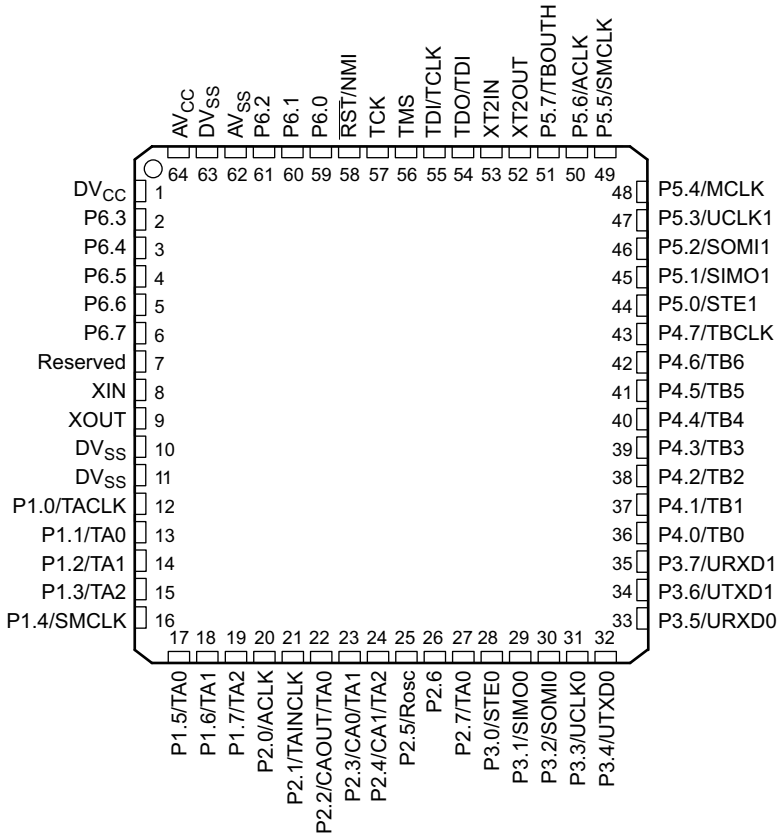


Figure 4-3. 64-Pin PM or RTD Package (Top View) for MSP430F1471, MSP430F1481, and MSP430F1491

4.2 Signal Descriptions

Table 4-1 describes the signals for the MSP430F13x and MSP430F14x MCUs. See Table 4-2 for the MSP430F14x1 signal descriptions.

Table 4-1. Signal Descriptions for MSP430F13x and MSP430F14x

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies the analog portion of the ADC.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies the analog portion of the ADC.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.3/TA2	15	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General-purpose digital I/O pin ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin Comparator_A output Timer_A, capture: CCI0B input BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input
P2.5/R_{OSC}	25	I/O	General-purpose digital I/O pin input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK	26	I/O	General-purpose digital I/O pin Conversion clock for ADC
P2.7/TA0	27	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin Slave transmit enable for USART0 in SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin Slave in/master out of USART0 in SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin Slave out/master in of USART0 in SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O USART0 clock: external input in UART or SPI mode, output in SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin Transmit data out for USART0 in UART mode

Table 4-1. Signal Descriptions for MSP430F13x and MSP430F14x (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
P3.5/URXD0	33	I/O	General-purpose digital I/O pin Receive data in for USART0 in UART mode
P3.6/UTXD1 (1)	34	I/O	General-purpose digital I/O pin Transmit data out for USART1 in UART mode
P3.7/URXD1 (1)	35	I/O	General-purpose digital I/O pin Receive data in for USART1 in UART mode
P4.0/TB0	.36	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A or CCI0B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A or CCI1B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A or CCI2B input, compare: Out2 output
P4.3/TB3 (1)	39	I/O	General-purpose digital I/O pin Timer_B, capture: CCI3A or CCI3B input, compare: Out3 output
P4.4/TB4 (1)	40	I/O	General-purpose digital I/O pin Timer_B, capture: CCI4A or CCI4B input, compare: Out4 output
P4.5/TB5 (1)	41	I/O	General-purpose digital I/O pin Timer_B, capture: CCI5A or CCI5B input, compare: Out5 output
P4.6/TB6 (1)	42	I/O	General-purpose digital I/O pin Timer_B, capture: CCI6A or CCI6B input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
P5.0/STE1 (1)	44	I/O	General-purpose digital I/O pin Slave transmit enable for USART1 in SPI mode
P5.1/SIMO1 (1)	45	I/O	General-purpose digital I/O pin Slave in/master out of USART1 in SPI mode
P5.2/SOMI1 (1)	46	I/O	General-purpose digital I/O pin Slave out/master in of USART1 in SPI mode
P5.3/UCLK1 (1)	47	I/O	General-purpose digital I/O pin USART1 clock: external input in UART or SPI mode, output in SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O pin Main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin Submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin Auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin Switch all PWM digital output ports to high impedance for Timer_B7 (TB0 to TB6)
P6.0/A0	59	I/O	General-purpose digital I/O pin Analog input A0 for ADC
P6.1/A1	60	I/O	General-purpose digital I/O pin Analog input A1 for ADC
P6.2/A2	61	I/O	General-purpose digital I/O pin Analog input A2 for ADC
P6.3/A3	2	I/O	General-purpose digital I/O pin Analog input A3 for ADC
P6.4/A4	3	I/O	General-purpose digital I/O pin Analog input A4 for ADC
P6.5/A5	4	I/O	General-purpose digital I/O pin Analog input A5 for ADC
P6.6/A6	5	I/O	General-purpose digital I/O pin Analog input A6 for ADC
P6.7/A7	6	I/O	General-purpose digital I/O pin Analog input A7 for ADC

(1) MSP430F14x devices only

Table 4-1. Signal Descriptions for MSP430F13x and MSP430F14x (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
$\overline{\text{RST}}$/NMI	58	I	Reset input Nonmaskable interrupt input port Bootloader start
TCK	57	I	Test clock, the clock input port for device programming test and bootloader start
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output or programming data input
TMS	56	I	Test mode select, used as an input port for device programming and test
VeREF+	10	I	Input for an external reference voltage to the ADC
VREF+	7	O	Output of positive terminal of the reference voltage in the ADC
VREF−/VeREF−	11	I	Negative terminal for the ADC reference voltage for both sources, the internal reference voltage or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1, standard or watch crystals can be connected
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2, only standard crystals can be connected
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad, connect to DV_{SS}

Table 4-2 describes the signals for the MSP430F14x1 MCUs. See Table 4-1 for the MSP430F13x and MSP430F14x signal descriptions.

Table 4-2. Signal Descriptions for MSP430F14x1

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage positive terminal
AV_{SS}	62		Analog supply voltage negative terminal
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output
P2.0/ACLK	20	I/O	General-purpose digital I/O pin ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input Comparator_A output BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input
$P2.5/R_{OSC}$	25	I/O	General-purpose digital I/O pin Input for external resistor defining the DCO nominal frequency
P2.6	26	I/O	General-purpose digital I/O pin
P2.7/TA0	27	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin Slave transmit enable for USART0 in SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin Slave in/master out of USART0 in SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin Slave out/master in of USART0 in SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O USART0 clock: external input in UART or SPI mode, output in SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin Transmit data out for USART0 in UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O pin Receive data in for USART0 in UART mode

Table 4-2. Signal Descriptions for MSP430F14x1 (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
P3.6/UTXD1	34	I/O	General-purpose digital I/O pin Transmit data out for USART1 in UART mode
P3.7/URXD1	35	I/O	General-purpose digital I/O pin Receive data in for USART1 in UART mode
P4.0/TB0	.36	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A or CCI0B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A or CCI1B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A or CCI2B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O pin Timer_B, capture: CCI3A or CCI3B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O pin Timer_B, capture: CCI4A or CCI4B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O pin Timer_B, capture: CCI5A or CCI5B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O pin Timer_B, capture: CCI6A or CCI6B input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
P5.0/STE1	44	I/O	General-purpose digital I/O pin Slave transmit enable for USART1 in SPI mode
P5.1/SIMO1	45	I/O	General-purpose digital I/O pin Slave in/master out of USART1 in SPI mode
P5.2/SOMI1	46	I/O	General-purpose digital I/O pin Slave out/master in of USART1 in SPI mode
P5.3/UCLK1	47	I/O	General-purpose digital I/O pin USART1 clock: external input in UART or SPI mode, output in SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O pin Main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin Submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin Auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin Switch all PWM digital output ports to high impedance for Timer_B7 (TB0 to TB6)
P6.0	59	I/O	General-purpose digital I/O pin
P6.1	60	I/O	General-purpose digital I/O pin
P6.2	61	I/O	General-purpose digital I/O pin
P6.3	2	I/O	General-purpose digital I/O pin
P6.4	3	I/O	General-purpose digital I/O pin
P6.5	4	I/O	General-purpose digital I/O pin
P6.6	5	I/O	General-purpose digital I/O pin
P6.7	6	I/O	General-purpose digital I/O pin
$\overline{\text{RST}}$/NMI	58	I	Reset input Nonmaskable interrupt input port Bootloader start
TCK	57	I	Test clock, the clock input port for device programming test and bootloader start
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output or programming data input
TMS	56	I	Test mode select, used as an input port for device programming and test
DV_{SS}	10	I	Connect to DV_{SS}
Reserved	7		Reserved, do not connect externally

Table 4-2. Signal Descriptions for MSP430F14x1 (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
DV_{SS}	11	I	Connect to DV_{SS}
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad, connect to DV_{SS}

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		−0.3	4.1	V
Voltage applied to any pin (2)		−0.3	V_{CC} + 0.3	V
Diode current at any device terminal			±2	mA
Storage temperature	Programmed device	−40	85	°C
	Unprogrammed device	–55	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge ratings	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (AV_{CC} = DV_{CC} = V_{CC})	During program execution	1.8		3.6	V
		During flash memory programming	2.7		3.6	
V_{SS}	Supply voltage (AV_{SS} = DV_{SS} = V_{SS})		0		0	V
T_A	Operating free-air temperature		–40		85	°C
f_{LFXT1}	LFXT1 crystal frequency(1)	LF selected, XTS = 0, watch crystal		32768		Hz
		XT1 selected, XTS = 1, ceramic resonator	450		8000	kHz
		XT1 selected, XTS = 1, crystal	1000		8000	
f_{XT2}	XT2 crystal frequency(1)	Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
f_{SYSTEM}	Processor frequency (signal MCLK)	V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

(1) In LF mode, the LFXT1 oscillator requires a watch crystal. TI recommends a 5.1-MΩ resistor from XOUT to V_{SS} when V_{CC} < 2.5 V.
In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15 MHz at V_{CC} ≥ 2.2 V.
In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8 MHz at V_{CC} ≥ 2.8 V.

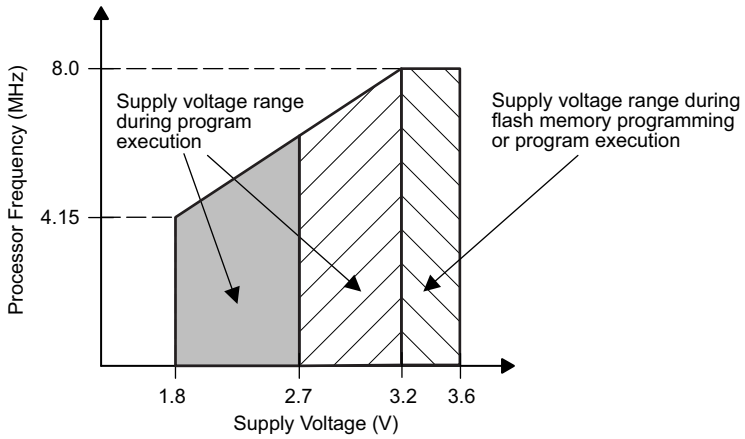


Figure 5-1. Frequency vs Supply Voltage

5.4 Supply Current Into AV_{CC} and DV_{CC} Excluding External Current

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode supply current(1)	$f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32768 Hz, XTS = 0, SELM = 0 or 1	–40°C to 85°C	2.2 V		280	360	µA
				3 V		420	560	
		$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz, XTS = 0, SELM = 3	–40°C to 85°C	2.2 V		2.5	7	
				3 V		9	20	
$I_{(LPM0)}$	Low-power mode 0 (LPM0) supply current(1)		–40°C to 85°C	2.2 V		32	45	µA
				3 V		55	70	
$I_{(LPM2)}$	Low-power mode 2 (LPM2) supply current	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 0	–40°C to 85°C	2.2 V		11	14	µA
				3 V		17	22	
$I_{(LPM3)}$	Low-power mode 3 (LPM3) supply current	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1(2)	–40°C	2.2 V		0.8	1.5	µA
			25°C			0.9	1.5	
			85°C			1.6	2.8	
			−40°C	3 V		1.8	2.2	
			25°C			1.6	1.9	
			85°C			2.3	3.9	
$I_{(LPM4)}$	Low-power mode 4 (LPM4) supply current	$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 0 MHz, SCG0 = 1	−40°C	2.2 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			0.8	2.5	
			−40°C	3 V		0.1	0.5	
			25°C			0.1	0.5	
			85°C			0.8	2.5	

(1) Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Timer_B is clocked by $f_{(ACLK)}$ = 32768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency

$I_{(AM)} = I_{(AM)}$ [1 MHz] × $f_{(System)}$ [MHz]

Current consumption of active mode versus supply voltage

$I_{(AM)} = I_{(AM)}$ [3 V] + 175 µA/V × (V_{CC} – 3 V)

5.5 Thermal Resistance Characteristics

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

THERMAL METRIC(1)		VALUE(2)			UNIT
		64-PIN PM	64-PIN PAG	64-PIN RTD	
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	52.0	52.7	25.0	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance	14.4	11.2	14.2	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance	23.0	23.4	9.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter	22.7	23.1	9.5	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter	0.6	0.3	0.2	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance	N/A(3)	N/A(3)	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = not applicable

5.6 Schmitt-Trigger Inputs – Ports P1, P2, P3, P4, P5, and P6

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	2.2 V	1.1	1.5	V
		3 V	1.5	1.9	
V_{IT-}	Negative-going input threshold voltage	2.2 V	0.4	0.9	V
		3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	2.2 V	0.3	1.1	V
		3 V	0.5	1	

5.7 Standard Inputs – $\overline{RST}$/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	2 2 V, 3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage		0.8 × V_{CC}	V_{CC}	V

5.8 Inputs – Px.y, TAx, TBx

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1.x and P2.x, External trigger pulse duration to set interrupt flag(1)	2.2 V, 3 V	1.5		cycle
			2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer A or Timer B capture timing	TA0, TA1, TA2, TB0, TB1, TB2, TB3, TB4, TB5, TB6(2)	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$, $f_{(TBext)}$	Timer_A or Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
			3 V		10	

(1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.
(2) Seven Timer_B capture/compare registers in MSP430F14x and MSP430F14x devices, and three Timer_B capture/compare registers in MSP430F13x devices.

Inputs – Px.y, TAx, TBx *(continued)*

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{(TAint)}$, $f_{(TBint)}$	Timer_A or Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

5.9 Leakage Current

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current[1]	Port P1	$V_{(P1.x)}$ [2]	2.2 V, 3 V		±50	nA
$I_{lkg(P2.x)}$		Port P2	$V_{(P2.3)}$, $V_{(P2.4)}$ [2]			±50	
$I_{lkg(P6.x)}$		Port P6	$V_{(P6.x)}$ [2]			±50	

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin, unless otherwise noted.
(2) The port pin must be set as input, and the optional pullup or pulldown resistor must be disabled.

5.10 Outputs – Ports P1, P2, P3, P4, P5, and P6

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA[1]	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –6 mA[2]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = 1 mA[1]	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA[2]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA[1]	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 6 mA[2]		V_{SS}	V_{SS} + 0.6	
		$I_{(OLmax)}$ = 1.5 mA[1]	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA[2]		V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, must not exceed ±6 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, must not exceed ±24 mA to hold the maximum voltage drop specified.

5.11 Output Frequency

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{TAx}	Timer_A or Timer_B output frequency	Internal clock source, SMCLK signal applied[1], TA0 to TA2, TB0 to TB6, C_L = 20 pF		DC		f_{SYSTEM}	MHz
f_{ACLK}	Clock output frequency	Measured at P5.6/ACLK	C_L = 20 pF			f_{SYSTEM}	MHz
f_{MCLK}		Measured at P5.4/MCLK				f_{SYSTEM}	
f_{SMCLK}		Measured at P5.5/SMCLK				f_{SYSTEM}	
t_{Xdc}	Duty cycle of output frequency	Measured at P2.0/ACLK, C_L = 20 pF, V_{CC} = 2.2 V or 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		Measured at P1 4/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V or 3 V	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$	35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$	50% – 15 ns	50%	50% + 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	50% – 15 ns	50%	50% + 15 ns	

(1) The limits of the system clock MCLK must be met; the MCLK frequency must not exceed the limits. MCLK and SMCLK frequencies can be different.

5.12 Typical Characteristics – Ports P1, P2, P3, P4, P5, and P6 Outputs

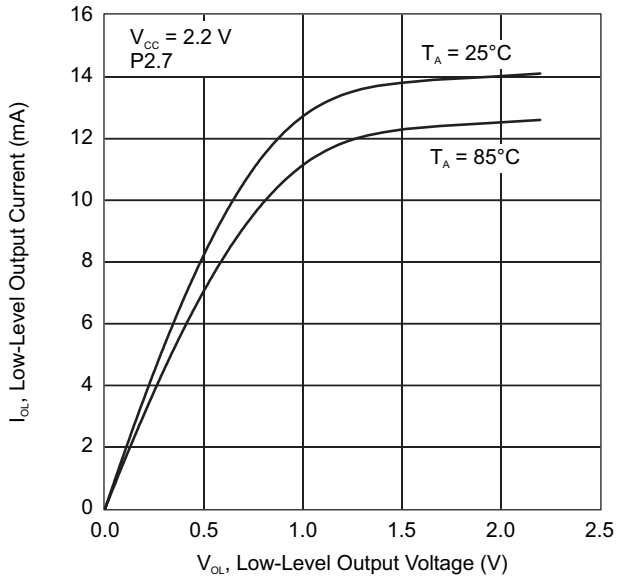


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

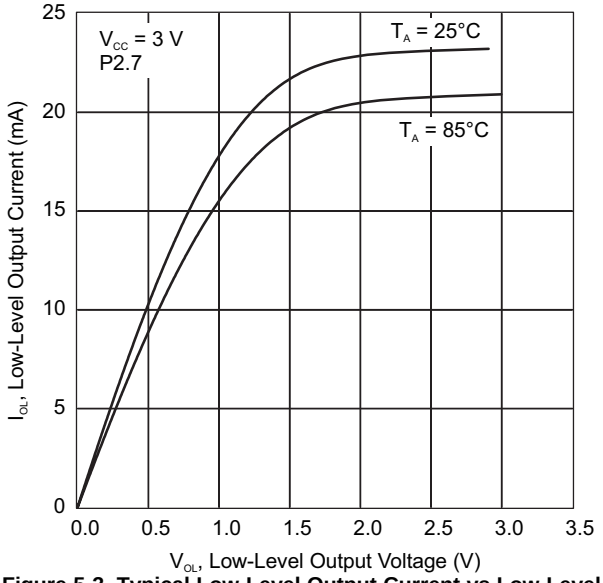


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

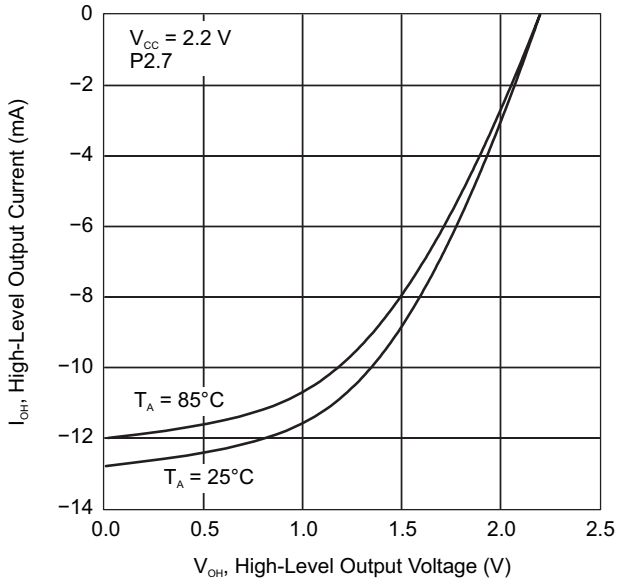


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

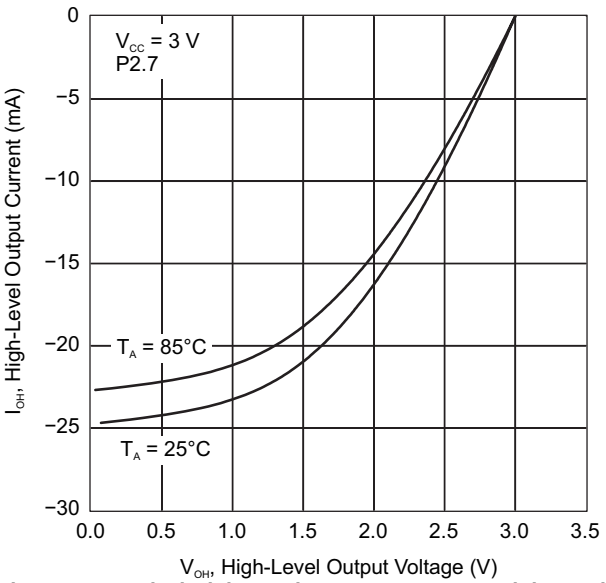


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.13 Wake-up Time From LPM3

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(LPM3)}$	Wake-up time from LPM3	f = 1 MHz	2.2 V, 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

5.14 RAM

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{RAMh}	Minimum supply voltage[1]	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.15 Comparator_A[1]

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$	Supply current	CAON = 1 CARSEL = 0 CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/Refdiode)}$	Reference ladder supply current	CAON = 1, CARSEL = 0, CAREF 1, 2, or 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON = 1	2.2 V, 3 V	0		V_{CC} – 1	V
$V_{(Ref025)}$	Ratio of (voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	Ratio of (voltage at 0.5 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	Reference voltage (see Figure 5-6 and Figure 5-7)	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage[2]		2.2 V, 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$	Low-to-high response time	T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$	High-to-low response time	T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	

(1) The leakage current for the Comparator_A terminals is identical to the $I_{lkgPx.x)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements.The two successive measurements are then summed together.

5.16 Typical Characteristics – Comparator_A

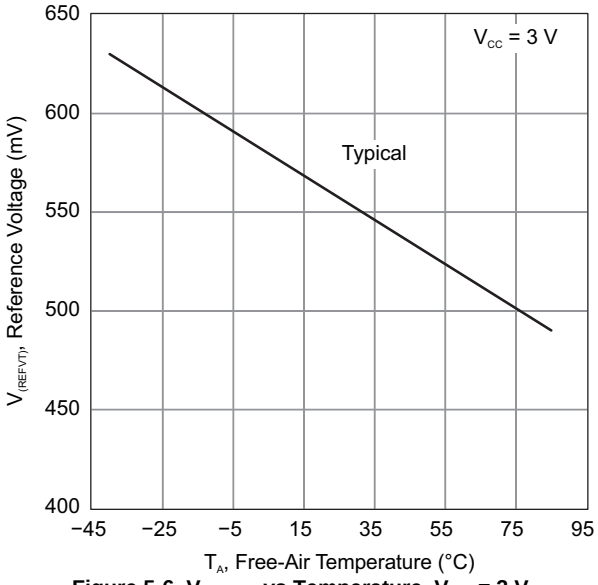


Figure 5-6. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

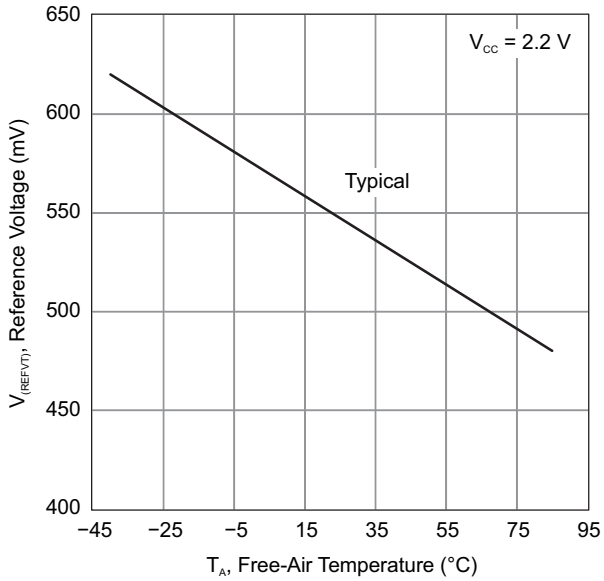


Figure 5-7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

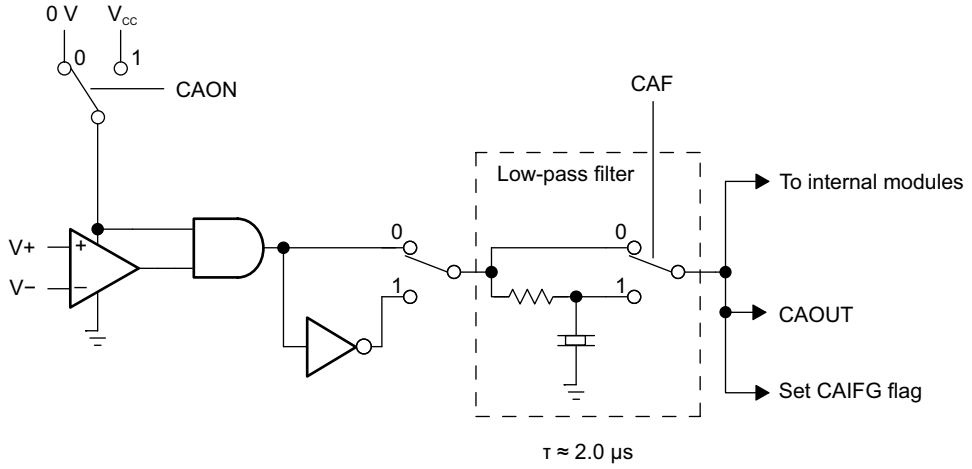


Figure 5-8. Block Diagram of Comparator_A Module

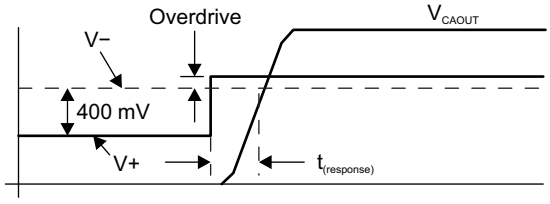


Figure 5-9. Overdrive Definition

5.17 PUC and POR

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(POR\_Delay)}$	Internal time delay to release POR		2.2 V, 3 V		150	250	µs
V_{POR}	V_{CC} threshold at which POR release delay time begins(1)	T_A = −40°C		1.4		1.8	V
		T_A = 25°C		1.1		1.5	
		T_A = 85°C		0.8		1.2	
$V_{(min)}$	V_{CC} threshold required to generate a POR(2)	V_{CC} |dV/dt| ≥ 1 V/ms	2.2 V, 3 V	0.2			V
$t_{(reset)}$	$\overline{RST}$/NMI low time for PUC or POR	Reset is accepted internally	2.2 V, 3 V	2			µs

(1) V_{CC} rise time dV/dt ≥ 1 V/ms
(2) When driving V_{CC} low to generate a POR condition, drive V_{CC} to 200 mV or lower with a dV/dt equal to or less than −1 V/ms. The corresponding rising V_{CC} must also meet the dV/dt requirement equal to or greater than +1 V/ms.

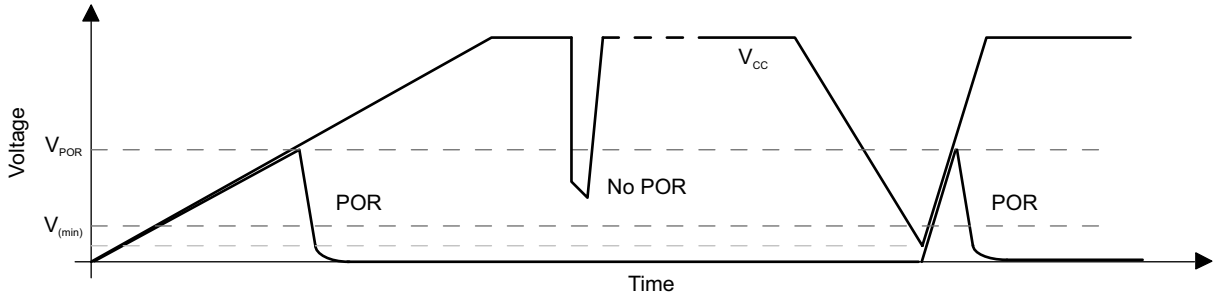


Figure 5-10. V_{POR} vs Supply Voltage

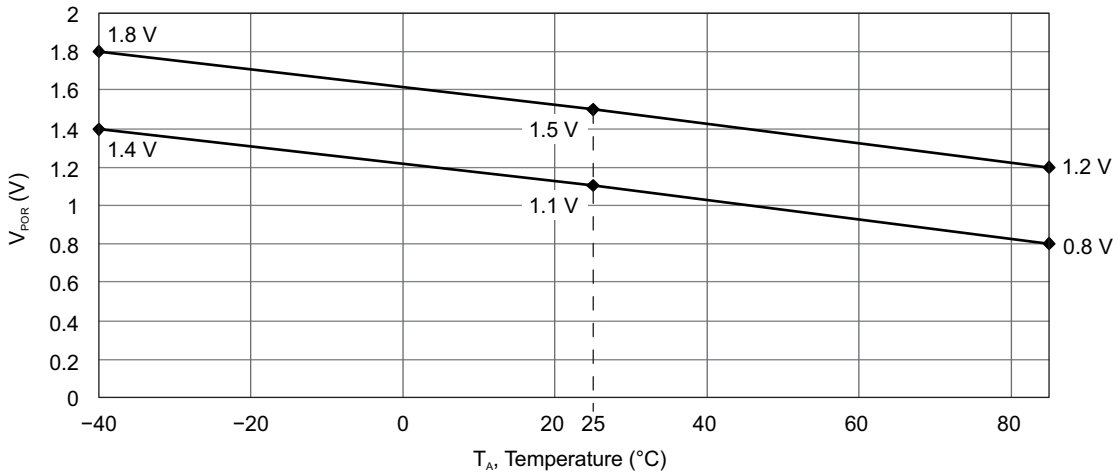


Figure 5-11. V_{POR} vs Temperature

5.18 DCO Frequency(1)

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO(03)}$	Rsel = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.08	0.12	0.15	MHz
			0.08	0.13	0.16	
$f_{DCO(13)}$	Rsel = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.14	0.19	0.23	MHz
			0.14	0.18	0.22	
$f_{DCO(23)}$	Rsel = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.22	0.30	0.36	MHz
			0.22	0.28	0.34	
$f_{DCO(33)}$	Rsel = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.37	0.49	0.59	MHz
			0.37	0.47	0.56	
$f_{DCO(43)}$	Rsel = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.61	0.77	0.93	MHz
			0.61	0.75	0.90	
$f_{DCO(53)}$	Rsel = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	1	1.2	1.5	MHz
			1	1.3	1.5	
$f_{DCO(63)}$	Rsel = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	1.6	1.9	2.2	MHz
			1.69	2.0	2.29	
$f_{DCO(73)}$	Rsel = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	2.4	2.9	3.4	MHz
			2.7	3.2	3.65	
$f_{DCO(47)}$	Rsel = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	f_{DCO40} × 1.7	f_{DCO40} × 2.1	f_{DCO40} × 2.5	MHz
$f_{DCO(77)}$	Rsel = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	4	4.5	4.9	MHz
			4.4	4.9	5.4	
S_{Rsel}	$S_{Rsel} = f_{Rsel+1} / f_{Rsel}$	2.2 V, 3 V	1.35	1.65	2	
S_{DCO}	$S_{DCO} = f_{DCO+1} / f_{DCO}$	2.2 V, 3 V	1.07	1.12	1.16	
D_t	Temperature drift(2), Rsel = 4, DCO = 3, MOD = 0	2.2 V, 3 V	–0.31	–0.36	–0.40	%/°C
			–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation(2), Rsel = 4, DCO = 3, MOD = 0	2.2 V, 3 V	0	5	10	%/V

(1) The DCO frequency may not exceed the maximum system frequency defined by the processor frequency parameter, f_{SYSTEM}.
(2) This parameter is not production tested.

DCO Characteristics (see Figure 5-12)

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{DCO(x0)}$ to $f_{DCO(x7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1); for example, Rsel0 overlaps with Rsel1, and Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to $f_{(DCO)} \times 2^{MOD/32}$.

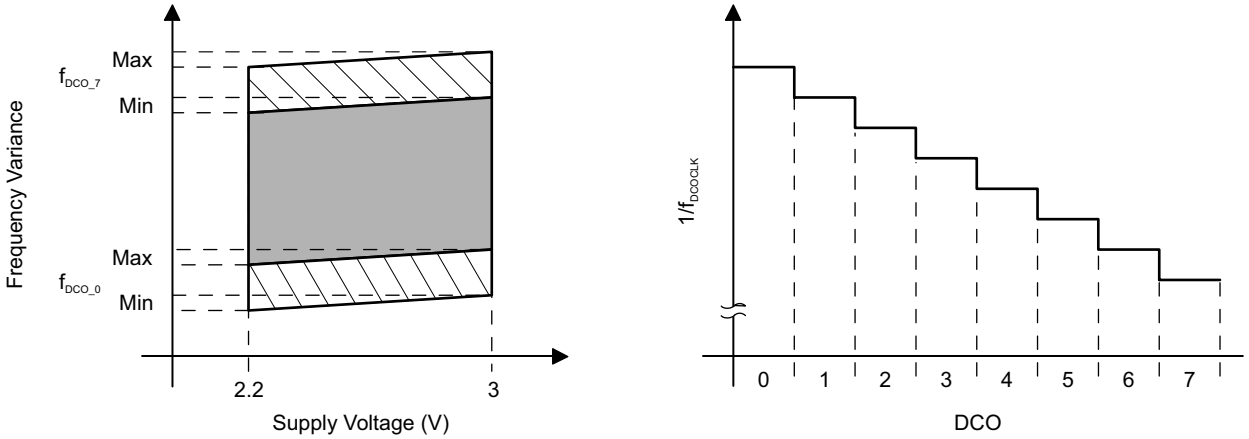


Figure 5-12. DCO Characteristics

5.19 DCO When Using R_{OSC}

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO}	DCO output frequency	Rsel = 4, DCO = 3, MOD = 0, DCOR = 1, T_A = 25°C	2.2 V		1.8 ±15%		MHz
			3 V		1.95 ±15%		
D_t	Temperature drift	Rsel = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V, 3 V		±0.1		%/°C
D_v	Drift with V_{CC} variation	Rsel = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V, 3 V		10		%/°V

(1) R_{OSC} = 100 kΩ, metal film resistor, type 0257, 0.6 W, 1% tolerance, T_K = ±50 ppm/°C

5.20 Crystal Oscillator, LFXT1

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance	XTS = 0, LF oscillator selected	2.2 V, 3 V		12		pF
		XTS = 1, XT1 oscillator selected			2		
C_{XOUT}	Integrated output capacitance	XTS = 0, LF oscillator selected	2.2 V, 3 V		12		pF
		XTS = 1, XT1 oscillator selected			2		
V_{IL}	Low-level input voltage at XIN(2)		2.2 V, 3 V	V_{SS}		0.2 × V_{CC}	V
V_{IH}	High-level input voltage at XIN(2)		2.2 V, 3 V	0.8 x V_{CC}		V_{CC}	V

(1) The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
(2) Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

5.21 Crystal Oscillator, XT2

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
C_{XT2IN}	Input capacitance	2.2 V, 3 V		2		pF
C_{XT2OUT}	Output capacitance	2.2 V, 3 V		2		pF
V_{IL}	Low-level input voltage at XT2IN(2)	2.2 V, 3 V	V_{SS}		0.2 × V_{CC}	V
V_{IH}	High-level input voltage at XT2IN(2)	2.2 V, 3 V	0.8 x V_{CC}		V_{CC}	V

(1) The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
(2) Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

5.22 USART0, USART1

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART0 or USART1 deglitch time(1)	2.2 V	200	430	800	ns
		3 V	150	280	500	

(1) The signal applied to the USART0 USART1 receive terminal (URXD0 or URXD1) must meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 or URXD1 line.

5.23 12-Bit ADC, Power Supply and Input Range Conditions

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage (2)	All P6.0/A0 to P6.7/A7 terminals, analog inputs selected in ADC12MCTLx register and P6Sel.x = 1, $0 \le x \le 7$, $V_{(AVSS)} \le V_{(P6.x/Ax)} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	ADC operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	REF operating supply current into AV_{CC} terminal(4)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.8	
			3 V		0.5	0.8	
C_I	Input capacitance(5)	Only one P6.x/Ax terminal can be selected at one time	2.2 V			40	pF
R_I	Input MUX ON resistance(5)	$0 V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

(1) The leakage current is defined in the leakage current table.
(2) The analog input voltage range must be within the selected reference voltage range V_R+ to V_R- for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter IADC12.
(4) The internal reference current is supplied through the AV_{CC} terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting a conversion.
(5) Not production tested, limits verified by design.

5.24 12-Bit ADC, External Reference

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{VeREF+}	Positive external reference input voltage	$V_{VeREF+} > V_{VREF-/VeREF-}$ (2)		1.4	V_{AVCC}	V
$V_{VREF-/VeREF-}$	Negative external reference input voltage	$V_{VeREF+} > V_{VREF-/VeREF-}$ (3)		0	1.2	V
$V_{VeREF+} - V_{VREF-/VeREF-}$	Differential external reference input voltage	$V_{VeREF+} > V_{VREF-/VeREF-}$ (4)		1.4	V_{AVCC}	V
I_{VeREF+}	Static input current, VeREF+	$0 V \le V_{VeREF+} \le V_{AVCC}$	2.2 V, 3 V		±1	µA
$I_{VREF-/VeREF-}$	Static input current, VeREF−	$0 V \le V_{VeREF-} \le V_{AVCC}$	2.2 V, 3 V		±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy requirements limit the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements
(3) The accuracy requirements limit the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy requirements limit the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

5.25 12-Bit ADC, Built-In Reference

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, $I_{VREF+} \le I_{VREF+}$(max)	3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V, $I_{VREF+} \le I_{VREF+}$(max)	2.2 V, 3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, $I_{VREF+} \le 1$ mA		2.2			V
		REF2_5V = 1, $I_{VREF+} \le 0.5$ mA		V_{REF+} + 0.15			
		REF2_5V = 1, $I_{VREF+} \le 1$ mA		V_{REF+} + 0.15			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal(1)	I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$	Load-current regulation, VREF+ terminal(2)	I_{VREF+} = 100 µA to 90 µA, C_{VREF+} = 5 µF, V_{Ax} ≈ 0 5 × V_{REF+}, Error of conversion result ≤ 1 LSB	3 V			20	ns
C_{VREF+}	Capacitance at VREF+ terminal(3)	R_{EFON} = 1, 0 mA ≤ $I_{VREF+} \le I_{VREF+}$(max)	2.2 V, 3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference(1)	I_{VREF+} is constant in the range of 0 mA ≤ $I_{VREF+} \le 1$ mA	2.2 V, 3 V			±100	ppm/°C
t_{REFON}	Settling time of reference voltage(4)(1) (see Figure 5-13)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{VREF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

(1) Not production tested, limits characterized
(2) Not production tested, limits verified by design
(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins VREF+ and AV_{SS} and VREF−/VeREF− and AV_{SS}: 10-µF tantalum and 100-nF ceramic.
(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

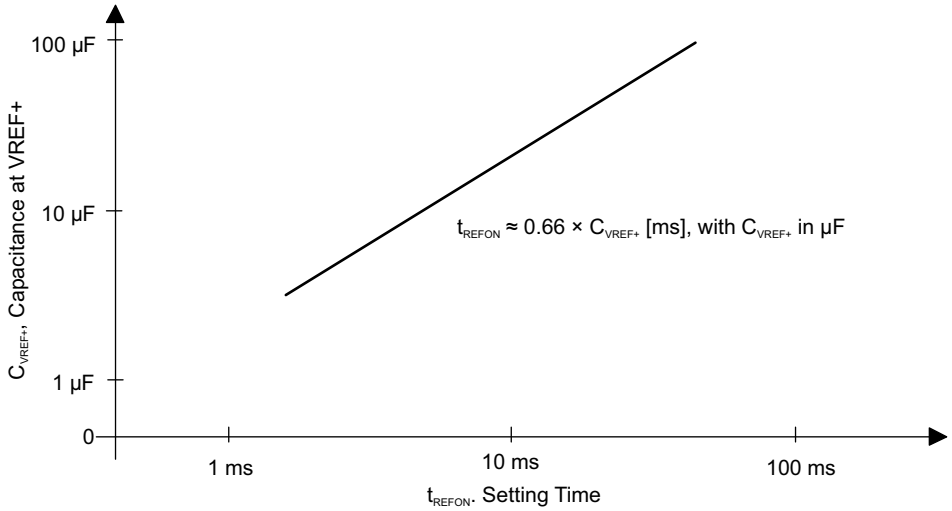


Figure 5-13. Typical Settling Time of Internal Reference (t_{REFON}) vs External Capacitor on VREF+

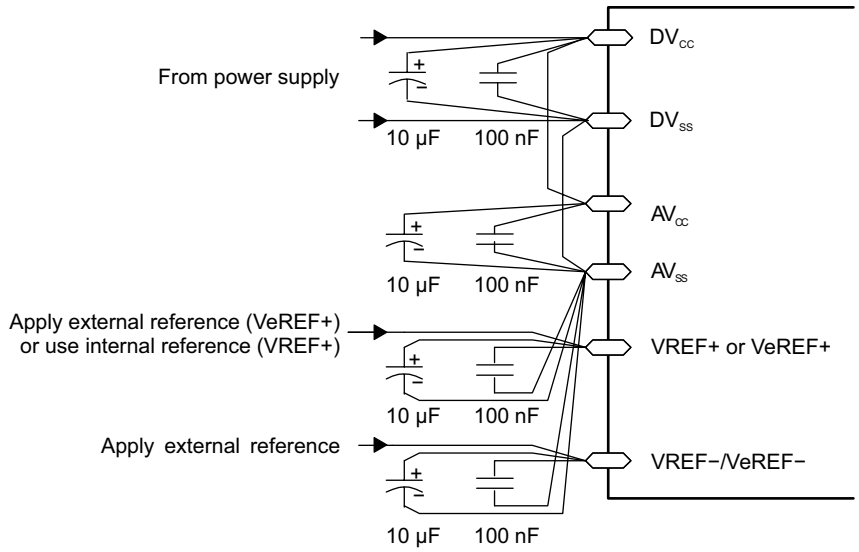


Figure 5-14. Supply Voltage and Reference Voltage Design, V_{REF-}/V_{eREF-} External Supply

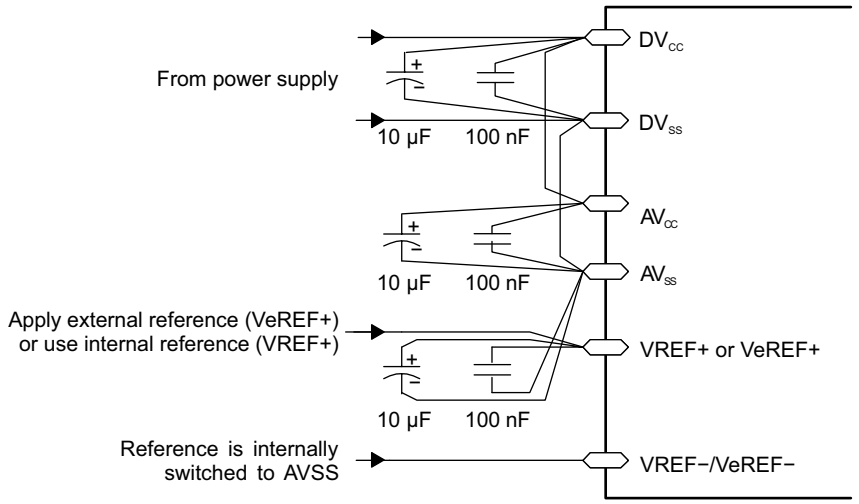


Figure 5-15. Supply Voltage and Reference Voltage Design, VREF-/VeREF- = AVSS, Internally Connected

5.26 12-Bit ADC, Timing Parameters

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC clock frequency	For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V, 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0			13 × $1/f_{ADC12CLK}$		
$t_{ADC12ON}$	Turn-on settling time of the ADC (1)	See (2)				100	ns
t_{Sample}	Sampling time (1)	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (3)	3 V	1220			ns
			2.2 V	1400			

(1) Not production tested, limits verified by design
(2) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

5.27 12-Bit ADC, Linearity Parameters

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ 1.6 V	2.2 V, 3 V			±2	LSB
		1.6 V < $(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ V_{AVCC}				±1.7	
E_D	Differential linearity error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V			±1	LSB
E_O	Offset error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±4	LSB
E_G	Gain error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±5	LSB

5.28 12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal(1)	REFON = 0, INCH = 0Ah, ADC12ON = N/A, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}	Sensor output voltage(2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986	986 ±5%	mV
			3 V		986	986 ±5%	
TC_{SENSOR}	Temperature coefficient of sensor output voltage(2)	ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55 ±3%	mV/°C
			3 V		3.55	3.55 ±3%	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(2)(3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (4)	ADC12ON = 1, INCH = 0Bh	2.2 V			N/A(5)	µA
			3 V			N/A	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V		1.1	1.1 ±0.04	V
			3 V		1.5	1.5 ±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(6)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). Therefore, it includes the constant current through the sensor and the reference.
(2) Not production tested, limits characterized
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor on-time, $t_{SENSOR(on)}$.
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) N/A = Not applicable
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

5.29 Flash Memory

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage		2.7		3.6	V
f_{FTG}	Flash timing generator frequency		257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program	V_{CC} = 2.7 V or 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase	V_{CC} = 2.7 V or 3.6 V		3	7	mA
t_{CPT}	Cumulative program time(1)	V_{CC} = 2.7 V or 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time(2)	V_{CC} = 2.7 V or 3.6 V	200			ms
	Program and erase endurance(3)		10^4	10^5		cycles
$t_{Retention}$	Data retention duration(3)	T_J = 25°C	100			years
t_{Word}	Word or byte program time(3)			35		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word(3)			30		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word(3)			21		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time(3)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time(3)			5297		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time(3)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297 × 1/f_{FTG}, maximum = 5297 × 1/476 kHz). To achieve the required cumulative mass erase time the flash controller mass erase operation can be repeated until this time is met. A worst case minimum of 19 cycles are required.
(3) These values are hardwired into the flash controller state machine (t_{FTG} = 1/f_{FTG}).

5.30 JTAG Interface

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency(1)	2.2 V	0		5	MHz
		3 V	0		10	
$R_{internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.31 JTAG Fuse (1)

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		T_A	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse blow	25°C	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse blow		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

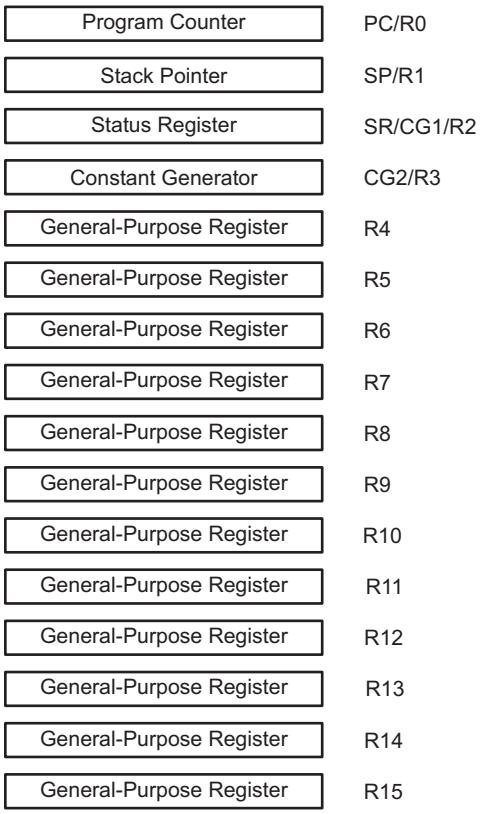


Figure 6-1. CPU Registers

6.2 Instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats, and Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4, R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	✓	✓	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+, Rm	MOV @R10+, R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

(1) S = source, D = destination

6.3 Operating Modes

The MSP430F13x, MSP430F14x, and MSP430F14x1 MCUs support one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the MCU from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - DC generator of the DCO is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash memory	WDTIFG KEYV(1)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(1)	(Non)maskable(2)	0FFFCh	14
Timer_B7(3)	TBCCR0 CCIFG(4)	Maskable	0FFFAh	13
Timer_B7(3)	TBCCR1 to 6 CCIFGs, TBIFG(1)(4)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF9h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12(5)	ADC12IFG(1)(4)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG(4)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG, TACCR2 CCIFG, TAIFG(1)(4)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(1)(4)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1	Maskable	0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(1)(4)	Maskable	0FFE2h	1
–	–	–	0FFE0h	0, lowest

(1) Multiple source flags
(2) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.
(3) Timer_B7 in the MSP430F14x(1) MCUs has 7 CCRs, and Timer_B3 in the MSP430F13x MCUs has 3 CCRs. In Timer_B3, there are only interrupt flags TBCCR0, TBCCR1, and TBCCR2 CCIFGs and the interrupt-enable bits TBCCTL0, TBCCTL1, and TBCCTL2 CCIEs.
(4) Interrupt flags are located in the module.
(5) ADC12 is not implemented on the MSP430F14x1 devices.

6.5 Bootloader (BSL)

The MSP430 BSL lets users program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory through the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the MSP430™ Flash Device Bootloader (BSL) User's Guide. Table 6-4 lists the pin requirements for the BSL.

Table 6-4. BSL Pin Requirements and Functions

BSL FUNCTION	PM, PAG, AND RTD PACKAGE PINS
Data transmit	13 - P1.1
Data receive	22 - P2.2

6.6 JTAG Fuse Check Mode

MSP430 MCUs that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current (I_{TF}) of 1 mA at 3 V or 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-2). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

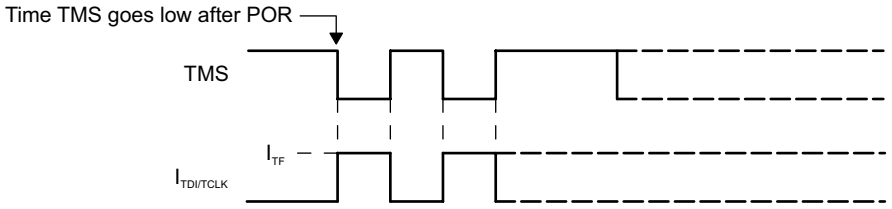


Figure 6-2. Fuse Check Mode Current

6.7 Memory

Table 6-5 summarizes the memory map of all device variants.

Table 6-5. Memory Organization

		MSP430F133	MSP430F135	MSP430F147 MSP430F1471	MSP430F148 MSP430F1481	MSP430F149 MSP430F149
Memory (flash)	Size	8KB	16KB	32KB	48KB	60KB
Main: interrupt vector	Flash	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h
Main: code memory	Flash	0FFFFh to 0E000h	0FFFFh to 0C000h	0FFFFh to 08000h	0FFFFh to 04000h	0FFFFh to 01100h
Information memory	Size	256 bytes	256 bytes	256 bytes	256 bytes	256 bytes
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
Boot memory	Size	1KB	1KB	1KB	1KB	1KB
	Flash	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h
RAM	Size	256 bytes	512 bytes	1KB	2KB	2KB
	RAM	02FFh to 0200h	03FFh to 0200h	05FFh to 0200h	09FFh to 0200h	09FFh to 0200h
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

6.7.1 Flash Memory

The flash memory can be programmed through the JTAG port, the bootloader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

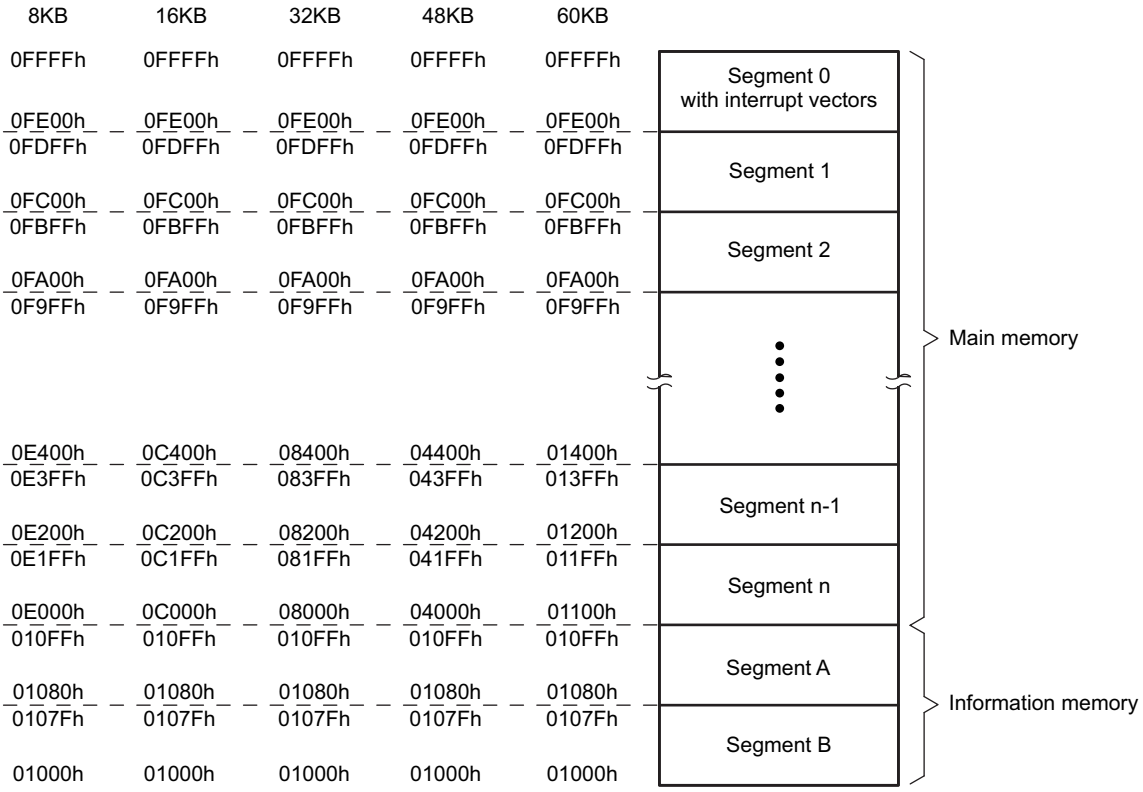


Figure 6-3. Flash Memory

6.7.2 Special Function Registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

Figure 6-4. Interrupt Enable 1 Bit Register

7	6	5	4	3	2	1	0
UTXIE0	URXIE0	ACCVIE	NMIIE	Reserved		OFIE	WDTIE
R/W-0	R/W-0	R/W-0	R/W-0	R-0		R/W-0	R/W-0

Table 6-6. Interrupt Enable 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXIE0	R/W	0	USART0: UART and SPI transmit interrupt enable
6	URXIE0	R/W	0	USART0: UART and SPI receive interrupt enable
5	ACCVIE	R/W	0	Flash access violation interrupt enable
4	NMIIE	R/W	0	Nonmaskable interrupt enable
3-2	Reserved	R	0	
1	OFIE	R/W	0	Oscillator-fault interrupt enable
0	WDTIE	R/W	0	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

Figure 6-5. Interrupt Enable 2 Bit Register

7	6	5	4	3	2	1	0
Reserved		UTXIE1	URXIE1	Reserved			
R-0		R/W-0	R/W-0	R-0			

Table 6-7. Interrupt Enable 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0	
5	UTXIE1	R/W	0	USART1: UART and SPI receive interrupt enable
4	URXIE1	R/W	0	USART1: UART and SPI transmit interrupt enable
3-0	Reserved	R/W	0	

Figure 6-6. Interrupt Flag 1 Bit Register

7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0	Reserved	NMIIFG	Reserved		OFIFG	WDTIFG
R/W-1	R/W-0	R-0	R/W-0	R-0		R/W-1	R/W-(0)

Table 6-8. Interrupt Flag 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXIFG0	R/W	1	USART0: UART and SPI transmit flag
6	URXIFG0	R/W	0	USART0: UART and SPI receive flag
5	Reserved	R	0	
4	NMIIFG	R/W	0	Set by $\overline{\text{RST}}$/NMI pin
3-2	Reserved	R	0	
1	OFIFG	R/W	1	Flag set on oscillator fault
0	WDTIFG	R/W	(0)	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power up or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode.

Figure 6-7. Interrupt Flag 2 Bit Register

7	6	5	4	3	2	1	0
Reserved		UTXIFG1	URXIFG1	Reserved			
R-0		R/W-1	R/W-0	R-0			

Table 6-9. Interrupt Flag 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0	
5	UTXIFG1	R/W	1	USART1: UART and SPI transmit flag
4	URXIFG1	R/W	0	USART1: UART and SPI receive flag
3-0	Reserved	R	0	

Figure 6-8. Module Enable 1 Bit Register

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0	Reserved					
R/W-0	R/W-0	R-0					

Table 6-10. Module Enable 1 Bit Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXE0	R/W	0	USART0: UART transmit enable
6	URXE0 USPIE0	R/W	0	USART0: UART receive enable USART0: SPI (synchronous peripheral interface) transmit and receive enable
5-0	Reserved	R	0	

Figure 6-9. Module Enable 2 Bit Register

7	6	5	4	3	2	1	0
Reserved		UTXE1	URXE1 USPIE1	Reserved			
R-0		R/W-0	R/W-0	R-0			

Table 6-11. Module Enable 2 Bit Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0	
5		R/W	0	USART1: UART transmit enable
4	URXE1 USPIE1	R/W	0	USART1: UART receive enable USART1: SPI (synchronous peripheral interface) transmit and receive enable
3-0	Reserved	R	0	

6.8 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the MSP430x1xx Family User's Guide.

6.8.1 Digital I/O

Six 8-bit I/O ports are implemented: ports P1 to P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.

6.8.2 Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules

6.8.3 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.8.4 Hardware Multiplier (MSP430F14x and MSP430F14x1 Only)

The multiplication operation is supported by a dedicated peripheral module. The module performs 16 × 16, 16 × 8, 8 × 16, and 8 × 8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

6.8.5 USART0

The hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

6.8.6 USART1 (MSP430F14x and MSP430F14x1 Only)

The MSP430F14x(1) has a second hardware universal synchronous/asynchronous receive transmit (USART1) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Operation of USART1 is identical to USART0.

6.8.7 Comparator_A

The primary function of the Comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

6.8.8 ADC12 (MSP430F14x and MSP430F13x Only)

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without CPU intervention.

6.8.9 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-12). Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. Timer_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	VCC			
14 - P1.2	TA1	CCI1A	CCR1	TA1	
	CAOUT (internal)	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
15 - P1.3	TA2	CCI2A	CCR2	TA2	
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

6.8.10 Timer_B3 (MSP430F13x Only)

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

6.8.11 Timer_B7 (MSP430F14x and MSP430F14x1 Only)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. Timer_B3 and Timer_B7 Signal Connections(1)

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	TBCLK	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	VCC			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

(1) Timer_B3 implements three capture/compare blocks (CCR0, CCR1 and CCR2).

6.8.12 Peripheral File Map

Table 6-14 lists the peripheral register that support word access. See Table 6-15 for the regsiters with byte access.

Table 6-14. Peripherals With Word Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B7, Timer_B3	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Timer_B capture/compare control 0	TBCCTL0	0182h
	Timer_B capture/compare control 1	TBCCTL1	0184h
	Timer_B capture/compare control 2	TBCCTL2	0186h
	Timer_B capture/compare control 3 (1)	TBCCTL3	0188h
	Timer_B capture/compare control 4 (1)	TBCCTL4	018Ah
	Timer_B capture/compare control 5 (1)	TBCCTL5	018Ch
	Timer_B capture/compare control 6 (1)	TBCCTL6	018Eh
	Timer_B counter	TBR	0190h
	Timer_B capture/compare 0	TBCCR0	0192h
	Timer_B capture/compare 1	TBCCR1	0194h
	Timer_B capture/compare 2	TBCCR2	0196h
	Timer_B capture/compare 3 (1)	TBCCR3	0198h
	Timer_B capture/compare 4 (1)	TBCCR4	019Ah
	Timer_B capture/compare 5 (1)	TBCCR5	019Ch
	Timer_B capture/compare 6 (1)	TBCCR6	019Eh
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Timer_A capture/compare control 0	TACCTL0	0162h
	Timer_A capture/compare control 1	TACCTL1	0164h
	Timer_A capture/compare control 2	TACCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A counter	TAR	0170h
	Timer_A capture/compare 0	TACCR0	0172h
	Timer_A capture/compare 1	TACCR1	0174h
	Timer_A capture/compare 2	TACCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh

(1) Timer_B7 only, reserved for Timer_B3

Table 6-14. Peripherals With Word Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Hardware multiplier (MSP430F14x and MSP430F14x1 only)	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Operand 2	OP2	0138h
	Multiply signed and accumulate operand 1	MACS	0136h
	Multiply and accumulate operand 1	MAC	0134h
	Multiply signed operand 1	MPYS	0132h
	Multiply unsigned operand 1	MPY	0130h
Flash	Flash control 3	FCTL1	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h

Table 6-14. Peripherals With Word Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
ADC12 (not in MSP430F14x1)	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt vector word	ADC12IV	01A8h
	Interrupt enable	ADC12IE	01A6h
	Interrupt flag	ADC12IFG	01A4h
	ADC control 1	ADC12CTL1	01A2h
	ADC control 0	ADC12CTL0	01A0h
	ADC memory control 15	ADC12MCTL15	08Fh
	ADC memory control 14	ADC12MCTL14	08Eh
	ADC memory control 13	ADC12MCTL13	08Dh
	ADC memory control 12	ADC12MCTL12	08Ch
	ADC memory control 11	ADC12MCTL11	08Bh
	ADC memory control 10	ADC12MCTL10	08Ah
	ADC memory control 9	ADC12MCTL9	089h
	ADC memory control 8	ADC12MCTL8	088h
	ADC memory control 7	ADC12MCTL7	087h
	ADC memory control 6	ADC12MCTL6	086h
	ADC memory control 5	ADC12MCTL5	085h
	ADC memory control 4	ADC12MCTL4	084h
	ADC memory control 3	ADC12MCTL3	083h
	ADC memory control 2	ADC12MCTL2	082h
	ADC memory control 1	ADC12MCTL1	081h
	ADC memory control 0	ADC12MCTL0	080h

Table 6-15 lists the peripheral register that support byte access. See Table 6-14 for the regsiters with word access.

Table 6-15. Peripherals With Byte Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
USART1 (MSP430F14x and MSP430F14x1 only)	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate 1	U1BR1	07Dh
	Baud rate 0	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate 1	U0BR1	075h
	Baud rate 0	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
Basic Clock	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h

Table 6-15. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

6.9 Input/Output Diagrams

6.9.1 Port P1, Input/Output With Schmitt Trigger

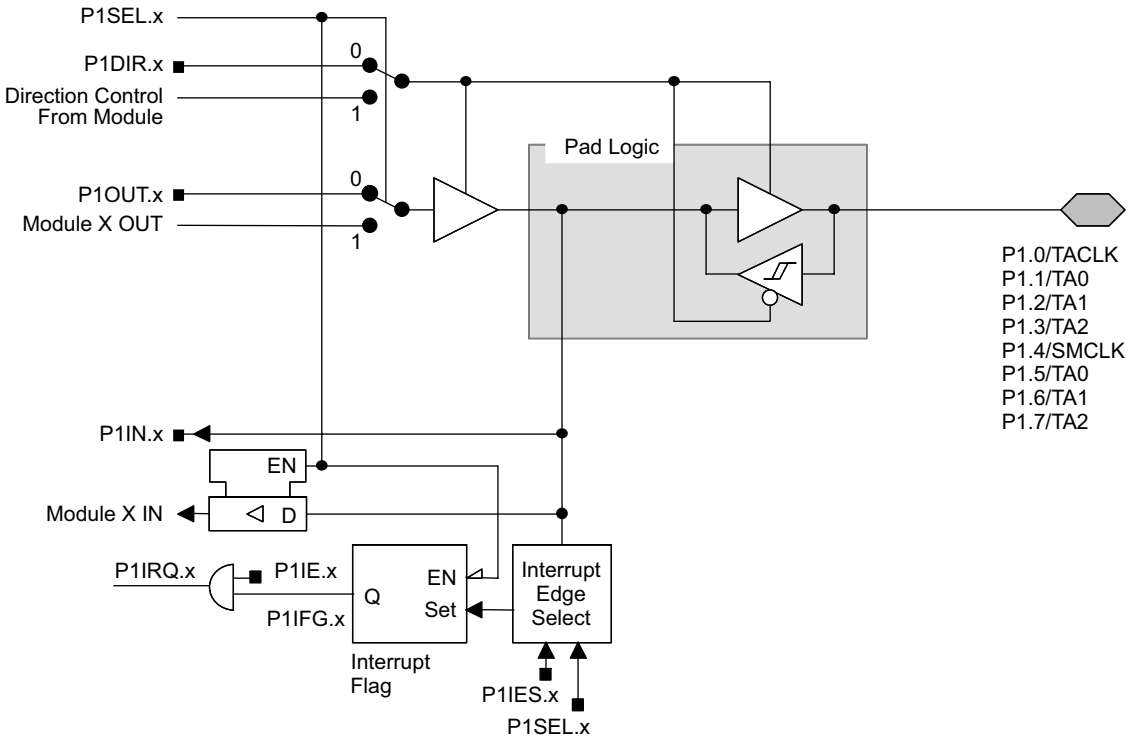


Figure 6-10. Port P1 (P1.0 to P1.7) Diagram

Table 6-16. Port P1 (P1.0 to P1.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK(1)	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal(1)	P1IN.1	CCI0A(1)	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal(1)	P1IN.2	CCI1A(1)	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal(1)	P1IN.3	CCI2A(1)	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal(1)	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal(1)	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal(1)	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

(1) Signal from or to Timer_A

6.9.2 Port P2, Input/Output With Schmitt Trigger

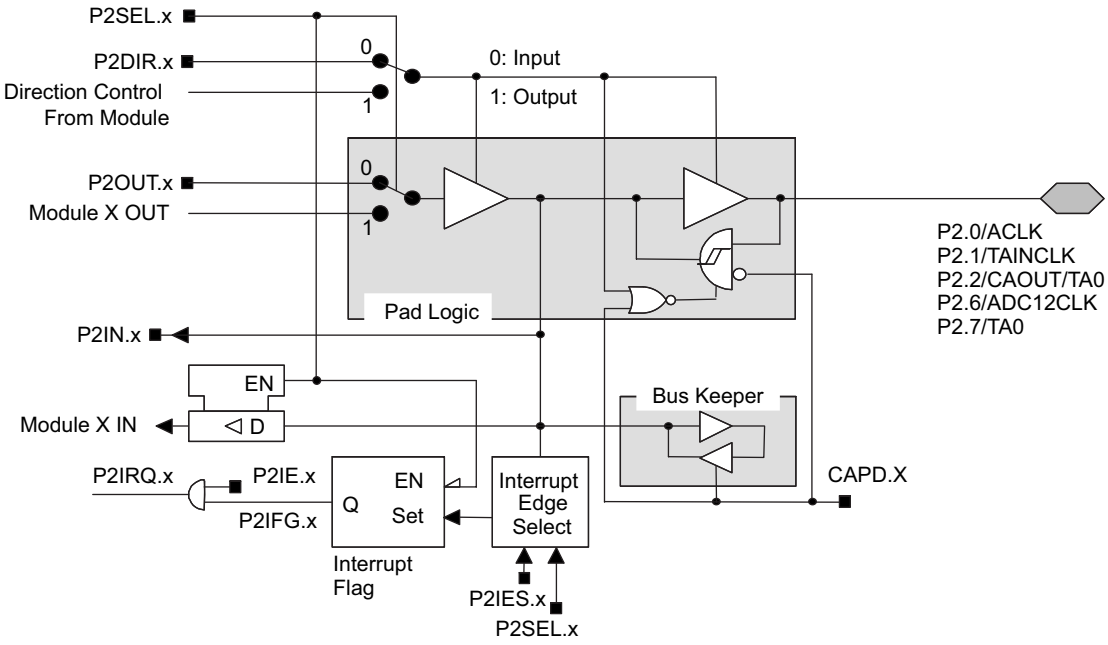


Figure 6-11. Port P2 (P2.0 to P2.2, P2.6, and P2.7) Diagram

Table 6-17. Port P2 (P2.0 to P2.2, P2.6, and P2.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK(1)	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT(2)	P2IN.2	CCI0B(1)	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	ADC12CLK(3)	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal(4)	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

(1) Signal to Timer_A
(2) Signal from Comparator_A
(3) ADC12CLK signal is output of the 12-bit ADC module
(4) Signal from Timer_A

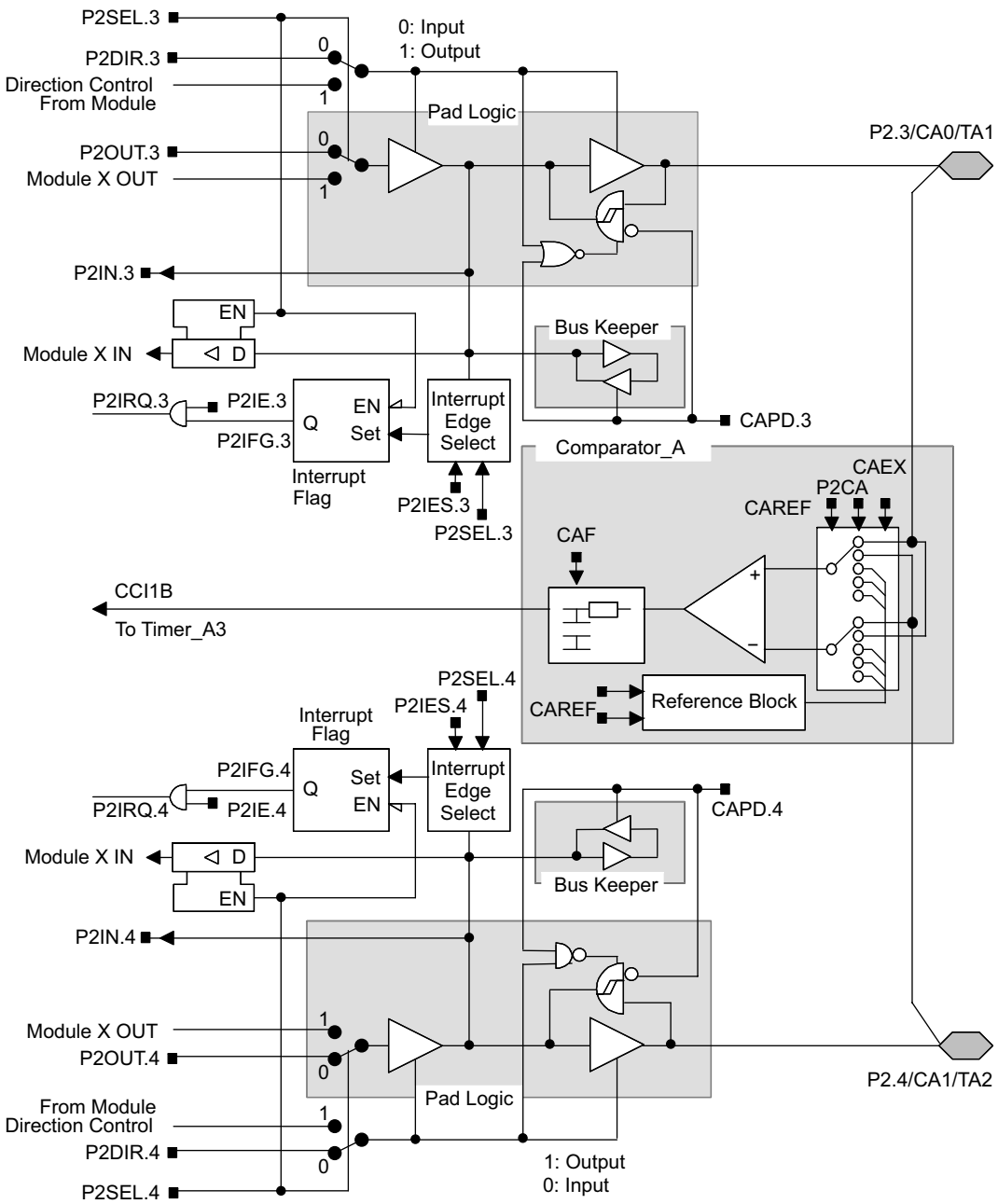
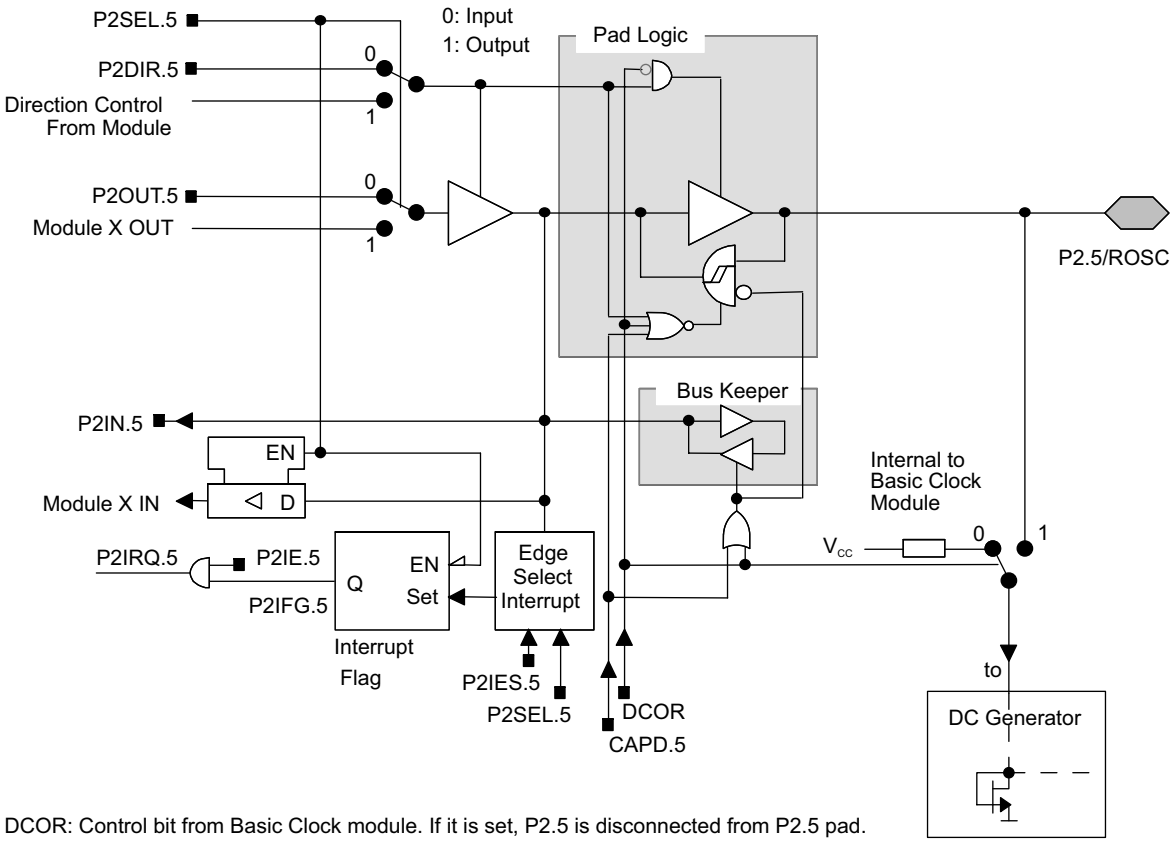


Figure 6-12. Port P2 (P2.3 and P2.4) Diagram

Table 6-18. Port P2 (P2.3 and P2.4) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal(1)	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal(1)	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

(1) Signal from Timer_A



DCOR: Control bit from Basic Clock module. If it is set, P2.5 is disconnected from P2.5 pad.

Figure 6-13. Port P2 (P2.5) Diagram

Table 6-19. Port P2 (P2.5) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

6.9.3 Port P3, Input/Output With Schmitt Trigger

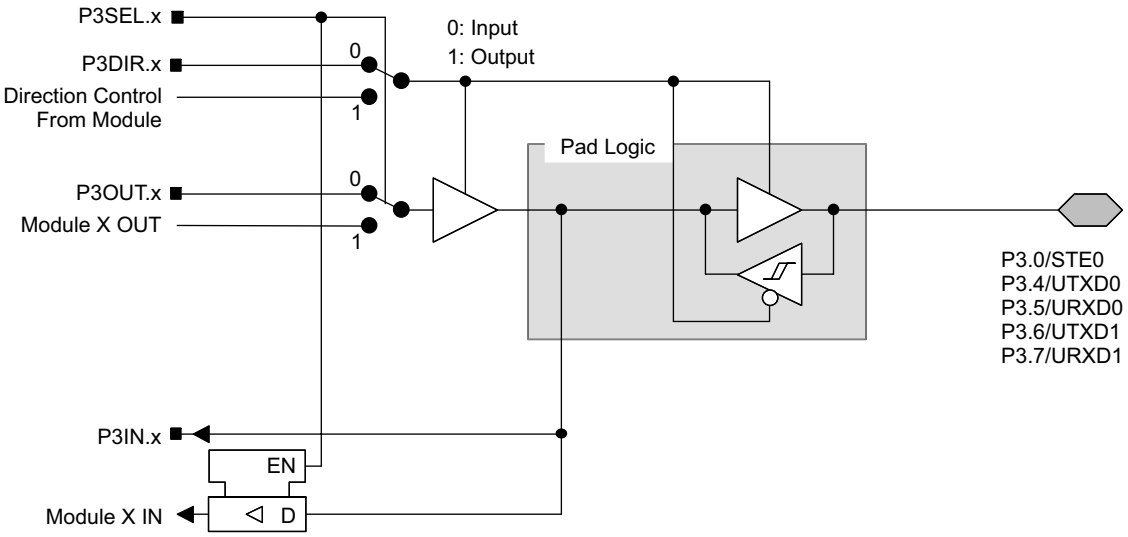


Figure 6-14. Port P3 (P3.0 and 3.4 to 3.7) Diagram

Table 6-20. Port P3 (P3.0 and 3.4 to 3.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0(1)	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0(2)
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	UTXD1(3)	P3IN.6	unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	URXD1(4)

(1) Output from USART0 module
(2) Input to USART0 module
(3) Output from USART1 module in MSP430F14x and MSP430F14x1 devices, DV_{SS} in MSP430F13x devices
(4) Input to USART1 module in MSP430F14x and MSP430F14x1 devices, unused in MSP430F13x devices

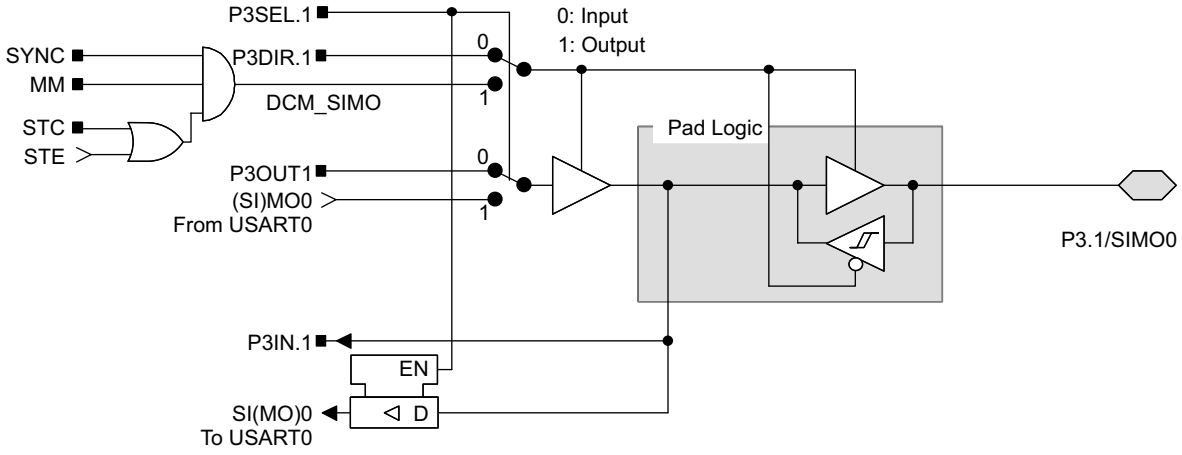


Figure 6-15. Port P3 (P3.1) Diagram

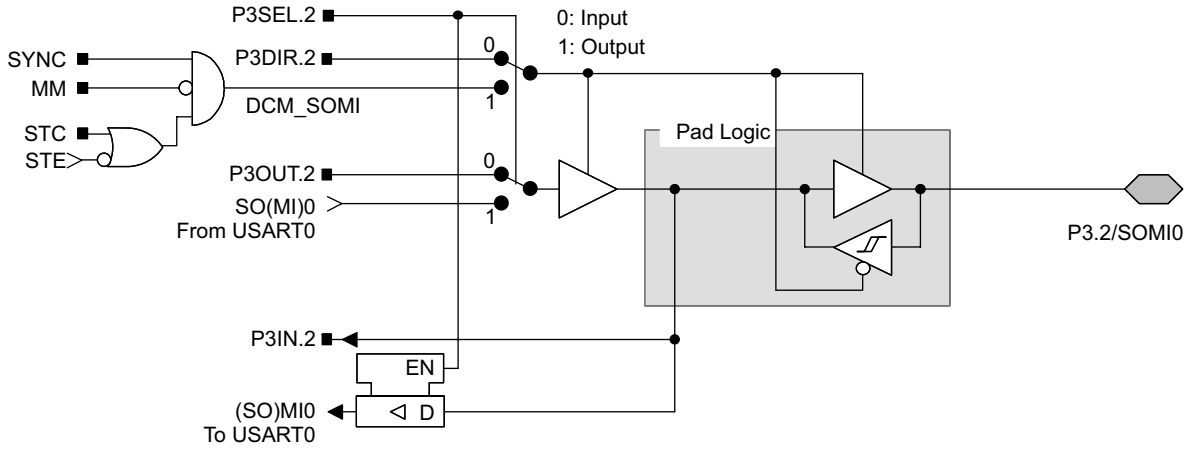
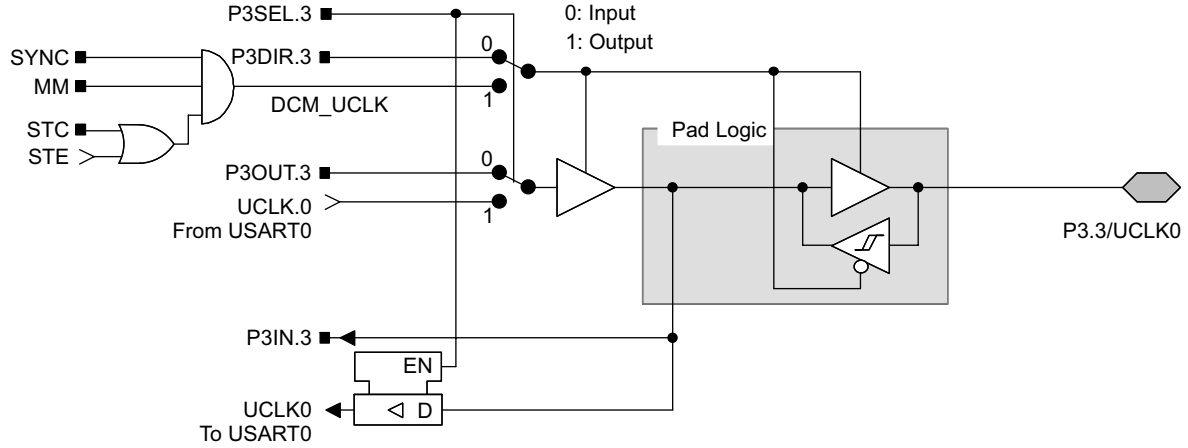


Figure 6-16. Port P3 (P3.2) Diagram



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, P3.3/UCLK0 is always an input.
SPI slave mode: The clock applied to UCLK0 is used to shift data in and out.
SPI master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

Figure 6-17. Port P3 (P3.3) Diagram

6.9.4 Port P4, Input/Output With Schmitt Trigger

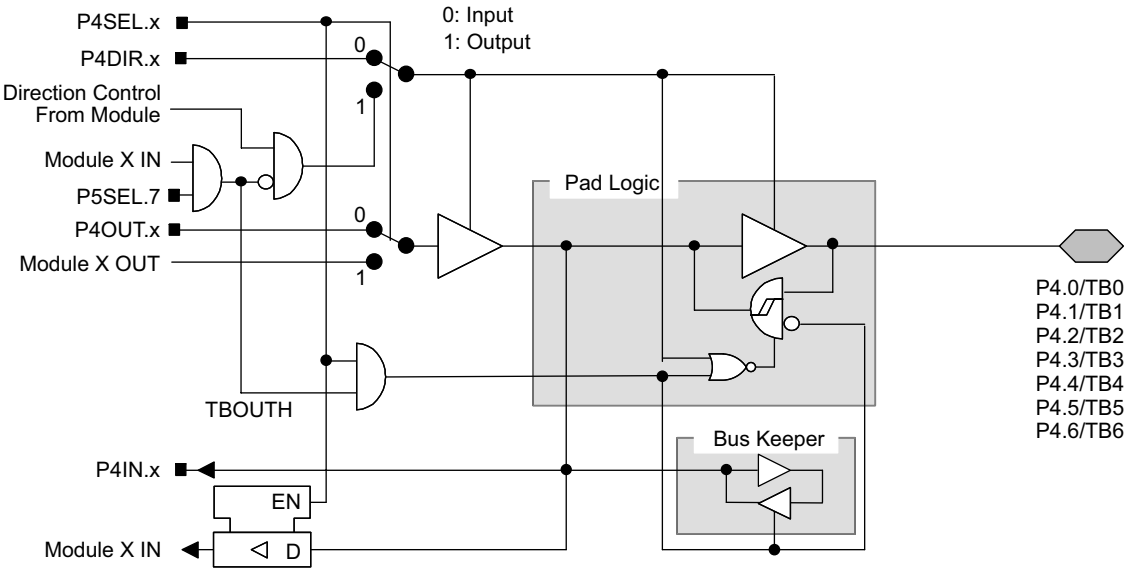


Figure 6-18. Port P4 (P4.0 to P4.6) Diagram

Table 6-21. Port P4 (P4.0 to P4.6) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal(1)	P4IN.0	CCI0A / CCI0B(2)
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal(1)	P4IN.1	CCI1A / CCI1B(2)
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal(1)	P4IN.2	CCI2A / CCI2B(2)
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	Out3 signal(1)	P4IN.3	CCI3A / CCI3B(2)
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	Out4 signal(1)	P4IN.4	CCI4A / CCI4B(2)
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	Out5 signal(1)	P4IN.5	CCI5A / CCI5B(2)
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	Out6 signal(1)	P4IN.6	CCI6A(2)

(1) Signal from Timer_B
(2) Signal to Timer_B

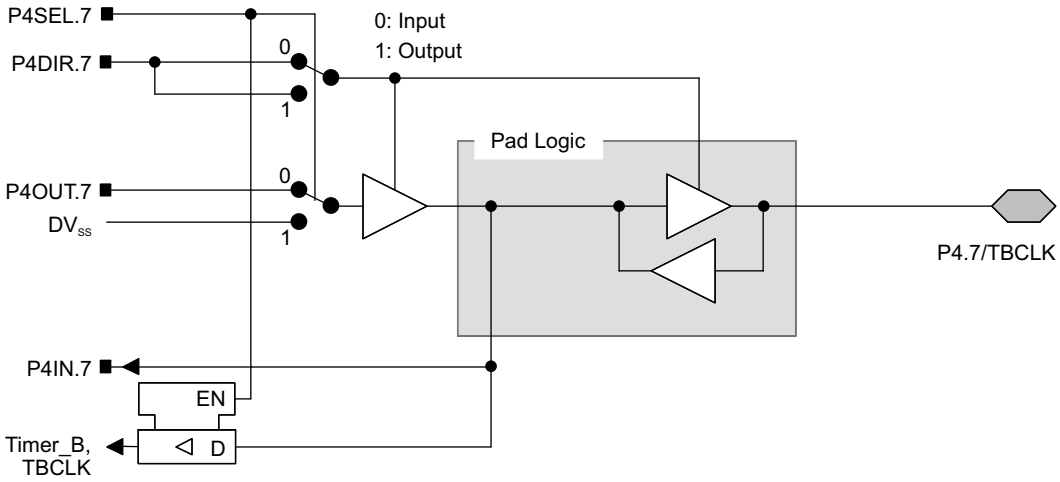


Figure 6-19. Port P4 (P4.7) Diagram

6.9.5 Port P5, Input/Output With Schmitt Trigger

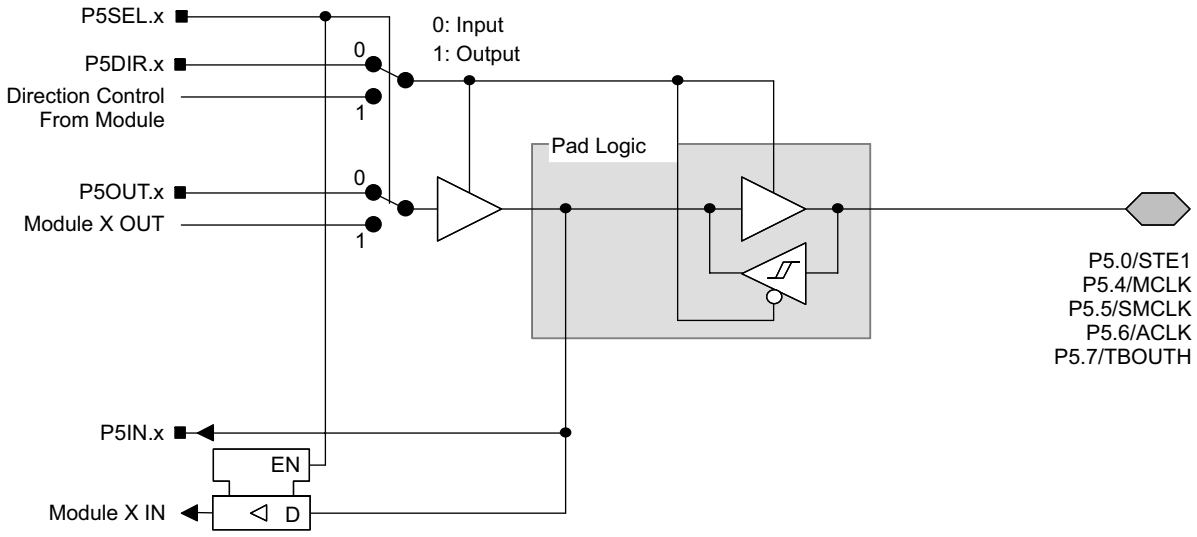


Figure 6-20. Port P5 (P5.0 and P5.4 to P5.7) Diagram

Table 6-22. Port P5 (P5.0 and P5.4 to P5.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	STE.1
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	DV_{SS}	P5IN.7	TBOUTH(1)

(1) The TBOUTH signal is used by port module P4, pins P4.0 to P4.6. The function of TBOUTH is most useful when used with Timer_B7.

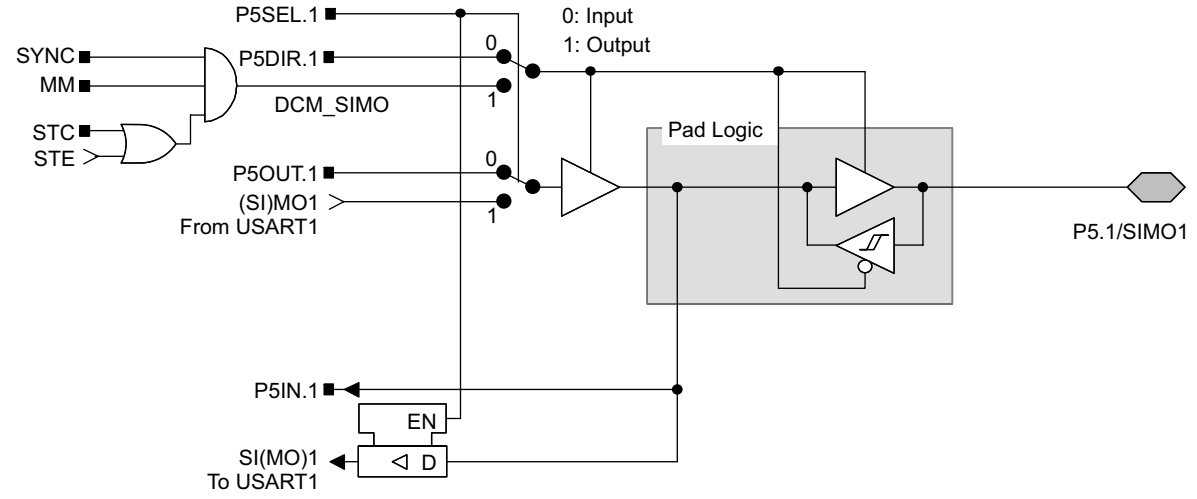


Figure 6-21. Port P5 (P5.1) Diagram

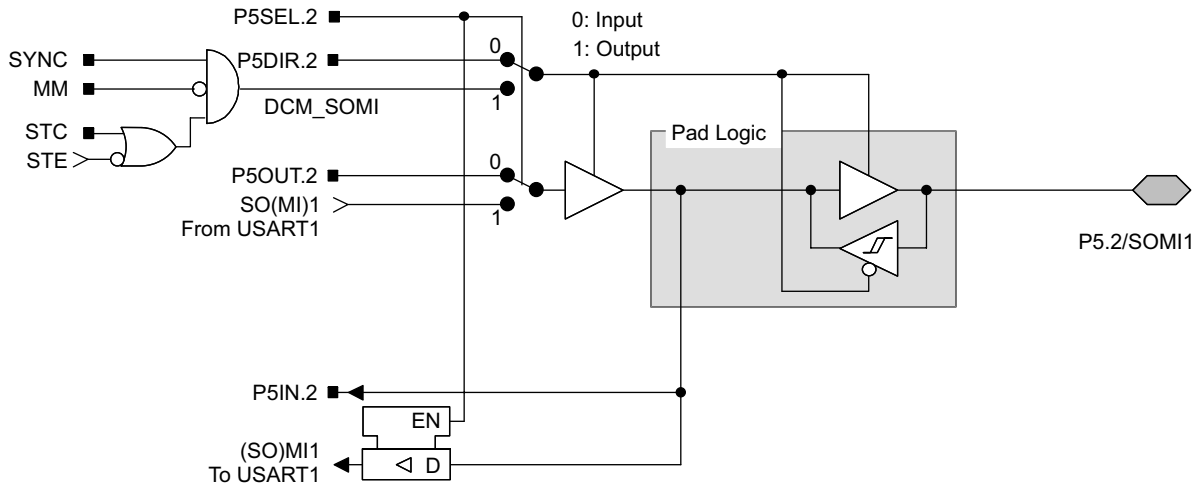
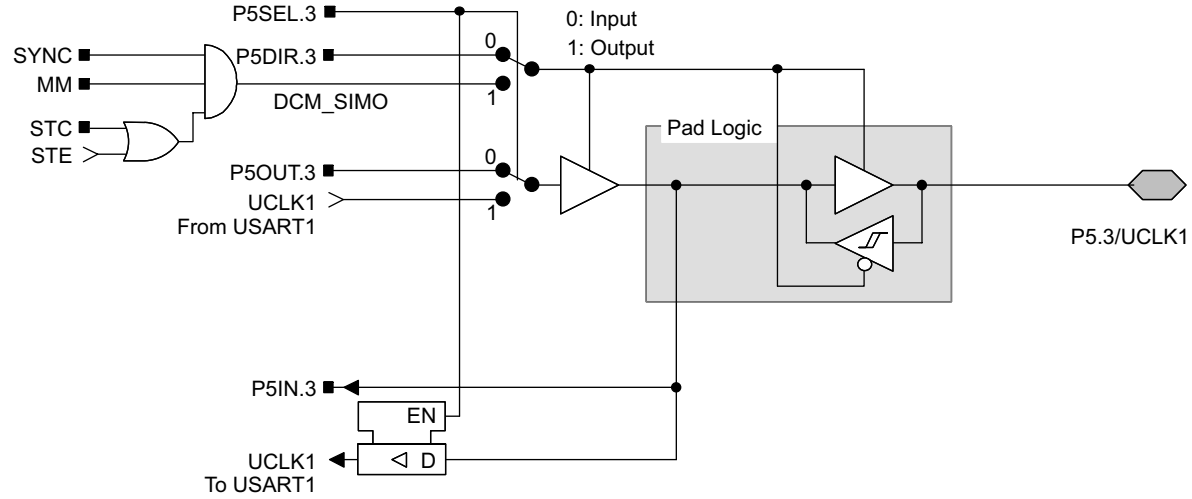


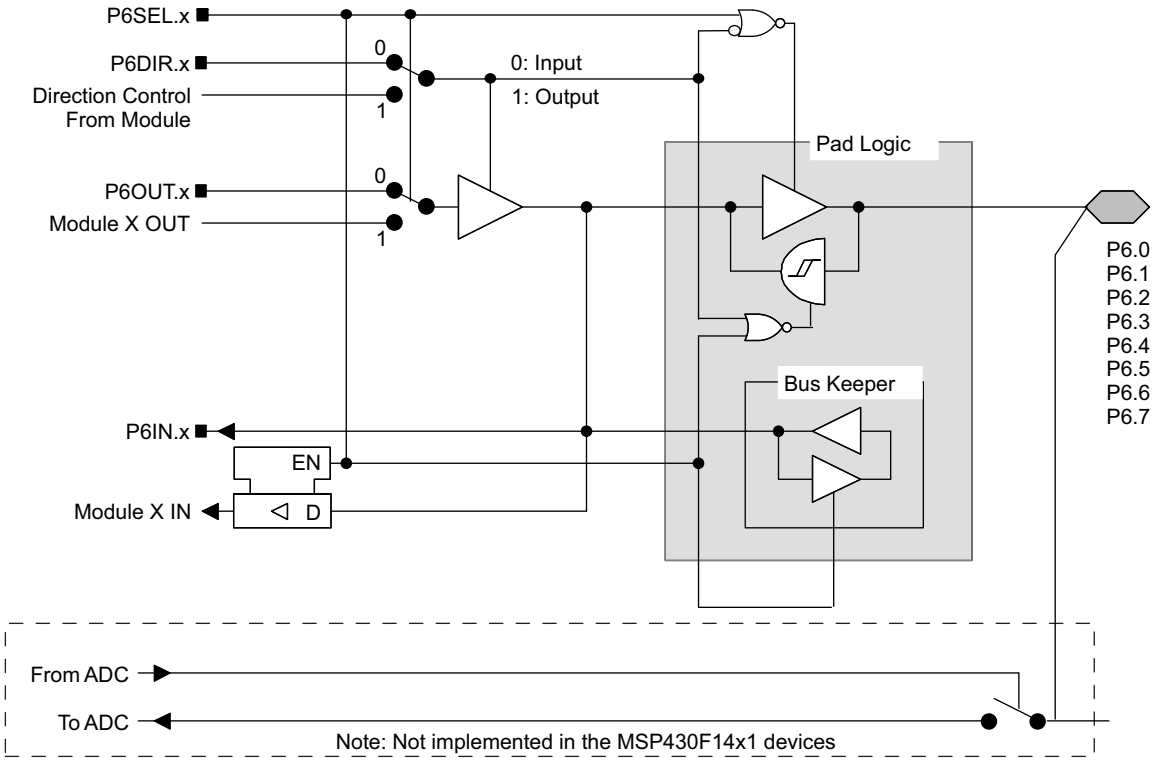
Figure 6-22. Port P5 (P5.2) Diagram



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, P5.3/UCLK1 is always an input.
SPI slave mode: The clock applied to UCLK1 is used to shift data in and out.
SPI master mode: The clock to shift data in and out is supplied to connected devices on pin P5.3/UCLK1 (in slave mode).

Figure 6-23. Port P5 (P5.3) Diagram

6.9.6 Port P6, Input/Output With Schmitt Trigger



NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430 MCUs, the current is approximately 100 µA. Use P6SEL.x = 1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

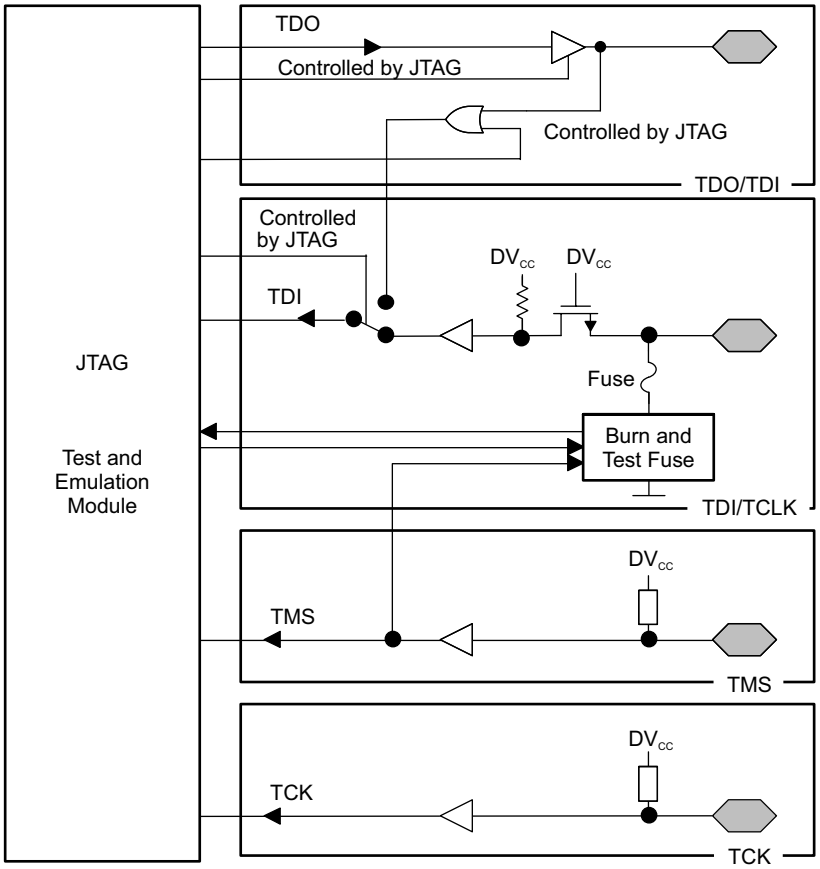
Figure 6-24. Port P6 (P6.0 to P6.7) Diagram

Table 6-23. Port P6 (P6.0 to P6.7) Pin Functions(1)

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

(1) The signal at pins P6.x/Ax is used by the 12-bit ADC module.

6.9.7 Port JTAG (TMS, TCK, TDI/TCLK, TDO/TDI), Input/Output With Schmitt Trigger



During programming activity and during blowing of the fuse, the TDO/TDI pin is used to apply the test input data for JTAG circuitry.

Figure 6-25. JTAG (TMS, TCK, TDI/TCLK, TDO/TDI) Diagram

7 器件和文档支持

7.1 入门和后续步骤

有关 MSP430 系列器件以及有助于开发的工具和库的更多信息，请访问入门页面。

7.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品开发的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

XMS - 实验器件，不一定代表最终器件的电气规格

MSP - 完全合格的生产器件

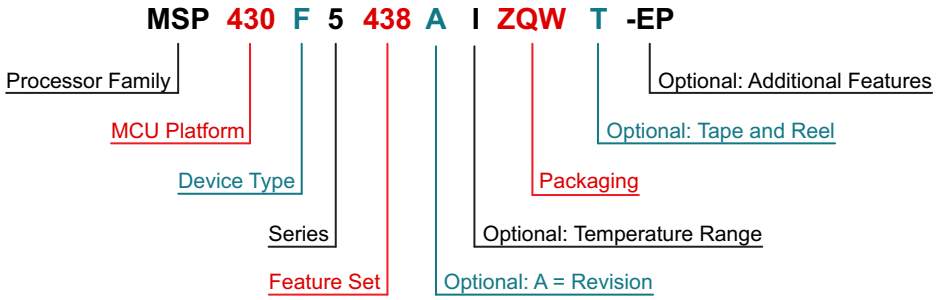
XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 7-1 提供了解读完整器件名称的图例。



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

NOTE: 该图不代表可用 特性 和选项的完整列表，也不表示所有这些 特性 和选项都可用于给定的器件或系列。

图 **7-1.** 器件命名规则 – 部件号解码器

7.3 工具和软件

表 7-1 列出 了 MSP430F14x、MSP430F14x1 和 MSP430F13x 微控制器支持的调试特性。关于可用特性的详细信息，请参见《适用于 MSP430 的 Code Composer Studio 用户指南 》。

表 7-1. 硬件 特性

MSP430 架构	四线制 JTAG	两线制 JTAG	断点	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMx.5 调试支持
MSP430	是	否	3	是	否	否	否	否

设计套件与评估模块

64 引脚目标开发板和 MSP-FET 编程器捆绑包 - MSP430F1x、MSP430F2x、MSP430F4x MCU MSP-FET430U64 是一款强大的闪存仿真工具，它包含在 MSP430 MCU 上快速开始应用开发所需的硬件和软件。它包含 ZIF 插座目标板 (MSP-TS430PM64) 和 USB 调试接口 (MSP-FET)，用于通过 JTAG 接口对 MSP430 系统内置器件进行编程和调试。只需使用几个按键即可在数秒钟内擦除闪存并对其进行编程。由于 MSP430 闪存的功耗极低，因此无需外部电源。

MSP-TS430PM64 - 适用于 MSP430F1x、MSP430F2x、MSP430F4x MCU 的 64 引脚目标开发板 MSP-TS430PM64 是一个独立的 ZIF 插座目标板，用于通过 JTAG 接口对 MSP430 MCU 系统内置器件进行编程和调试。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、产品说明书以及其他设计资源，打包提供给用户。除了提供已有 MSP430 MCU 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430F13x、MSP430F14x、MSP430F15x、MSP430F16x 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

适用于 MSP 低功耗微控制器的引导加载程序 (BSL) 引导加载程序 (BSL) 是内置到 MSP 低功耗微控制器中的应用程序。借助该应用程序，用户可以与器件通信，以便从其存储器中读取数据或向其中写入数据。该功能主要用于在原型设计、最终生产和服务期间对器件进行编程。可编程存储器（闪存）和数据存储器 (RAM) 可根据需要进行修改。

适用于 MSP 的定点数学库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式 应用的嵌入式软件实用程序。CCS 包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他众多 功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

7.4 文档支持

以下文档对 MSP430F14x、MSP430F14x1 和 MSP430F13x MCU 进行了介绍。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 7.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP430F149 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F1491 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F148 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F1481 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F147 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F1471 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F135 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430F133 器件勘误表》 介绍功能规格的已知例外情况。

用户指南

《MSP430x1xx 系列用户指南》 该器件系列提供的所有模块和外设的详细 说明 。

《MSP430 闪存器件引导加载程序 (BSL) 用户指南》 MSP430™ 引导加载程序 (BSL) 允许用户在原型设计、最终生产和服务阶段与 MSP430 微控制器 (MCU) 中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 可根据需要进行修改。

《通过 JTAG 接口对 MSP430 进行编程》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

《MSP430 硬件工具用户指南》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

《MSP430 32kHz 晶体振荡器》 选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《适用于 MSP430™ MCU 的软件编码技术》 该应用报告介绍了 MSP430 MCU 编程人员感兴趣的软件技术和相关主题。

《对 MSP ADC 进行一般过采样以获得更高分辨率》 多个 MSP430 超低功耗微控制器都可以提供用以将物理量转换成数字的 ADC，这是一种广泛用于大量 应用的函数。但是，有时客户设计要求的分辨率会高于所选 MSP 可提供的 ADC 分辨率。该应用报告介绍了如何通过加入过采样方式来提高 ADC 分辨率，使其超过当前可实现的位数。

《MSP430 系统级 ESD 注意事项》 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

7.5 相关链接

表 7-2 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 7-2. 相关链接

部件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
MSP430F149	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430F1491	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430F148	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430F1481	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430F147	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430F1471	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430F135	单击此处	单击此处	单击此处	单击此处	单击此处

7.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》 。

TI E2E™ 社区

TI 的工程师交流 (E2E) 社区. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页

德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.7 商标

MSP430, MSP430Ware, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.9 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

7.10 术语表

TI 术语表　　这份术语表列出并解释术语、缩写和定义。

8 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F133IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F133	Samples
MSP430F133IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F133	Samples
MSP430F133IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F133	Samples
MSP430F133IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F133	Samples
MSP430F135IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F135 REV #	Samples
MSP430F135IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F135 REV #	Samples
MSP430F135IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F135 REV #	Samples
MSP430F135IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F135	Samples
MSP430F135IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F135	Samples
MSP430F1471IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1471 REV #	Samples
MSP430F1471IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1471 REV #	Samples
MSP430F1471IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1471	Samples
MSP430F147IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPMR-KAM	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPMRG4	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F147	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F147IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F147	Samples
MSP430F1481IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1481	Samples
MSP430F1481IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1481	Samples
MSP430F1481IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1481	Samples
MSP430F148IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F148	Samples
MSP430F148IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F148 REV #	Samples
MSP430F148IPMG4	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F148 REV #	Samples
MSP430F148IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F148 REV #	Samples
MSP430F148IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F148	Samples
MSP430F148IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F148	Samples
MSP430F1491IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IPMG4	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F149IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPAGR	ACTIVE	TQFP	PAG	64	1500	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPMG4	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										REV #	
MSP430F149IPMRG4	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F149	Samples
MSP430F149IRTDRG4	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F149	Samples
MSP430F149IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F149	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

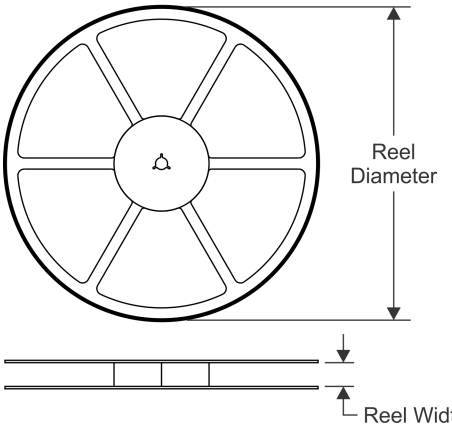
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

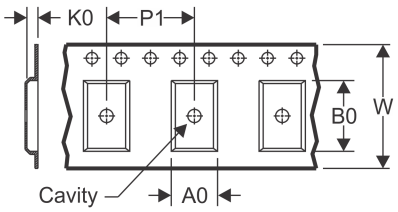
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

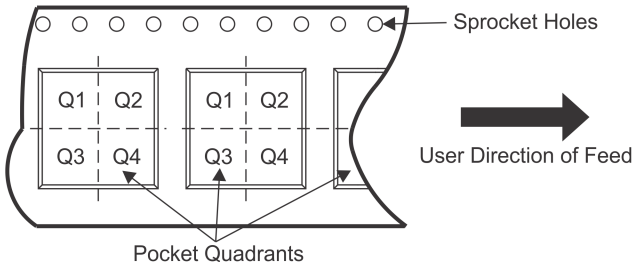


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

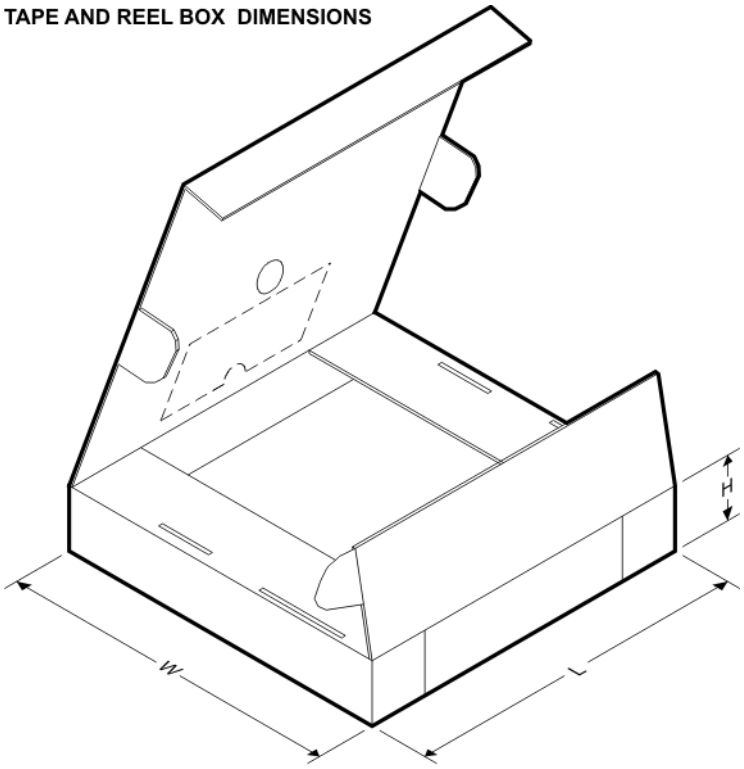


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F133IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F133IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F135IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F135IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F135IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1471IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F1471IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F147IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F147IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F147IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1481IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F1481IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F148IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F148IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F148IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1491IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F1491IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1491IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F149IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
MSP430F149IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F149IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F149IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F133IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F133IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F135IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F135IRTDR	VQFN	RTD	64	2500	853.0	449.0	35.0
MSP430F135IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F1471IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F1471IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F147IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F147IRTDR	VQFN	RTD	64	2500	853.0	449.0	35.0
MSP430F147IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F1481IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F1481IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F148IPMR	LQFP	PM	64	1000	336.6	336.6	41.3

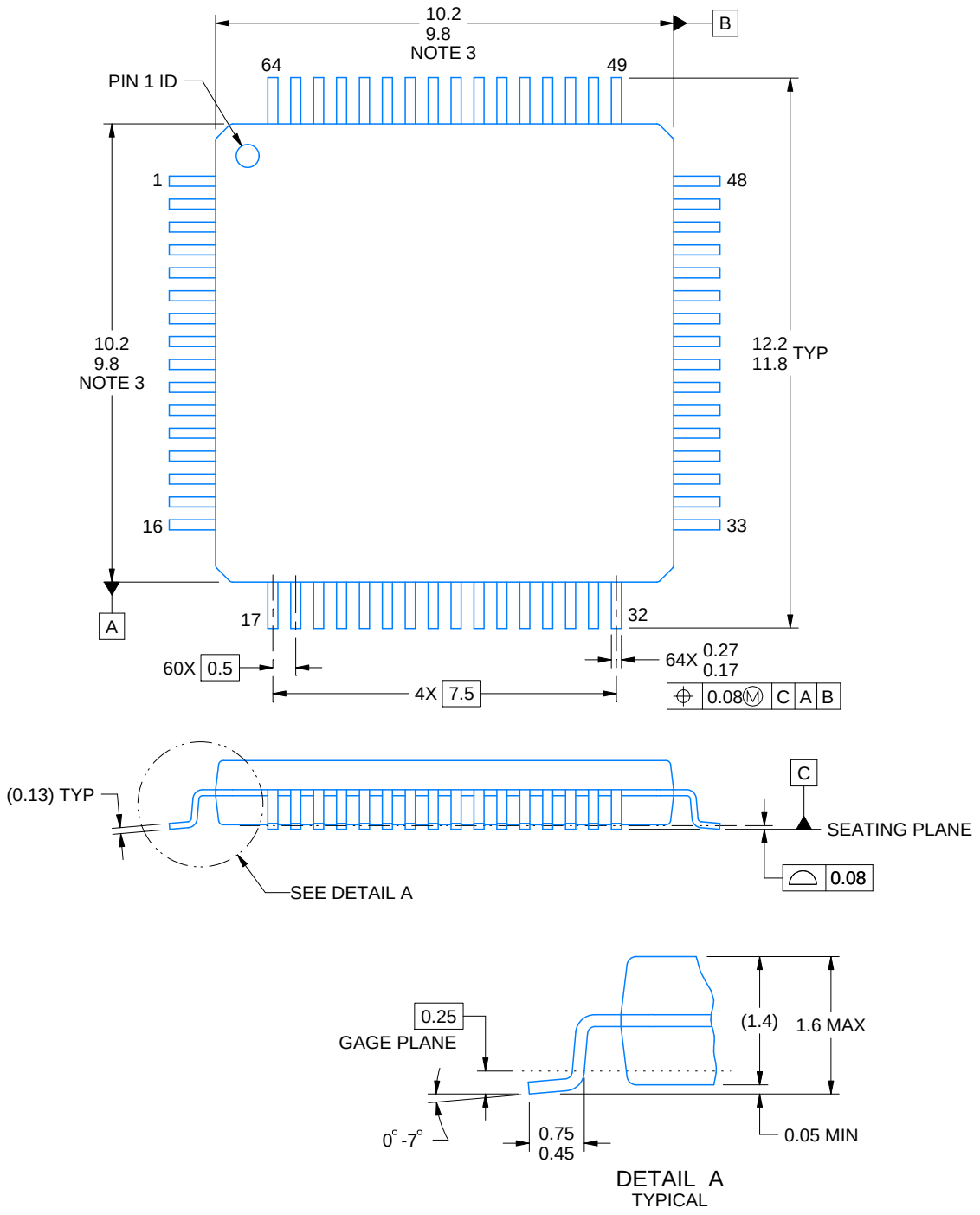
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F148IRTDR	VQFN	RTD	64	2500	853.0	449.0	35.0
MSP430F148IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F1491IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F1491IRTDR	VQFN	RTD	64	2500	853.0	449.0	35.0
MSP430F1491IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F149IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0
MSP430F149IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F149IRTDR	VQFN	RTD	64	2500	853.0	449.0	35.0
MSP430F149IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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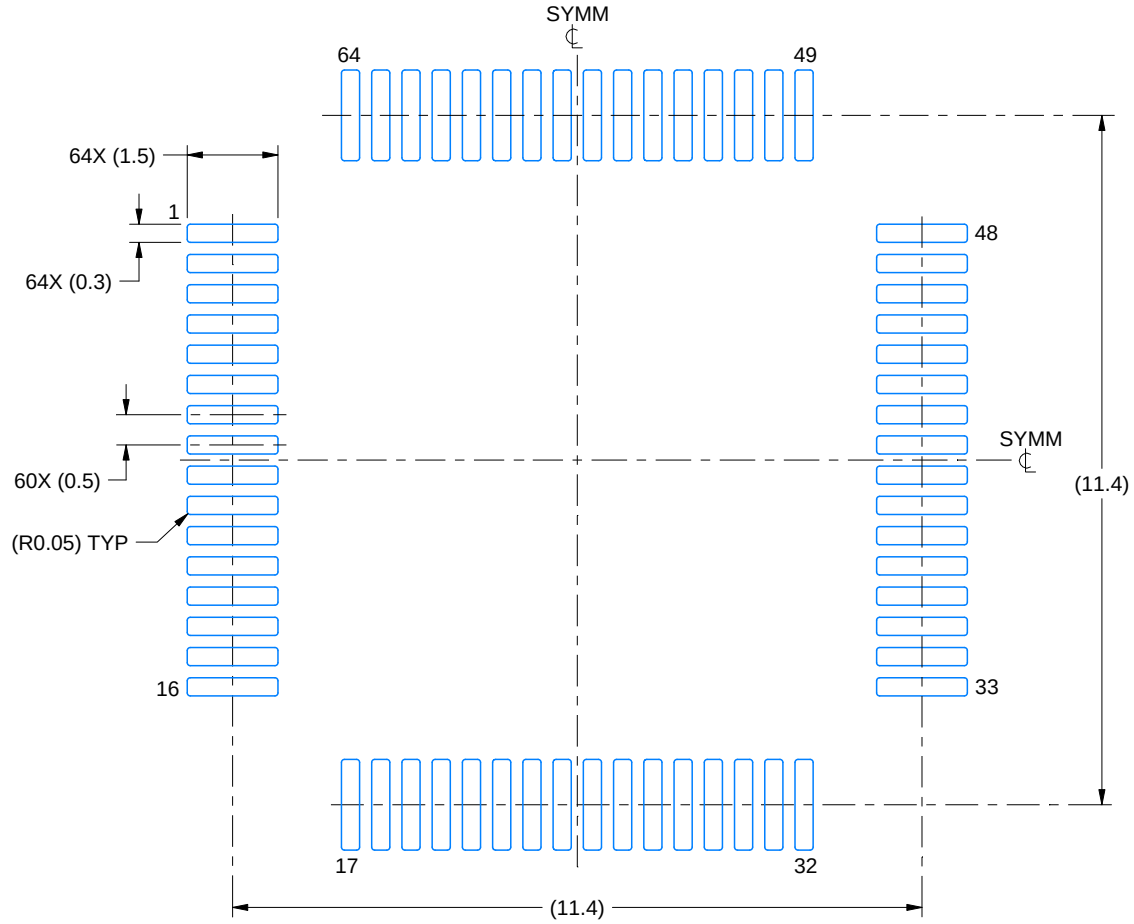
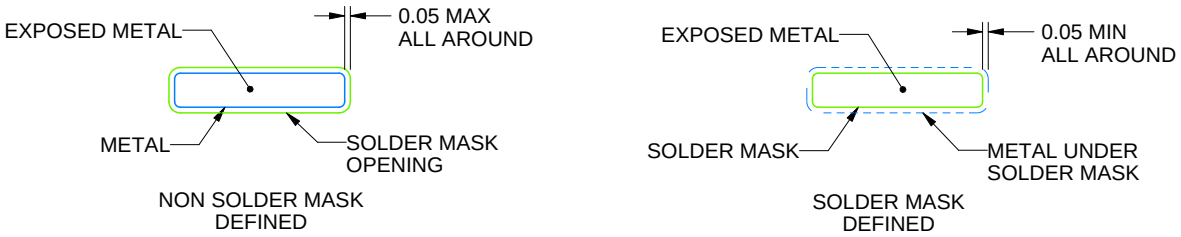
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

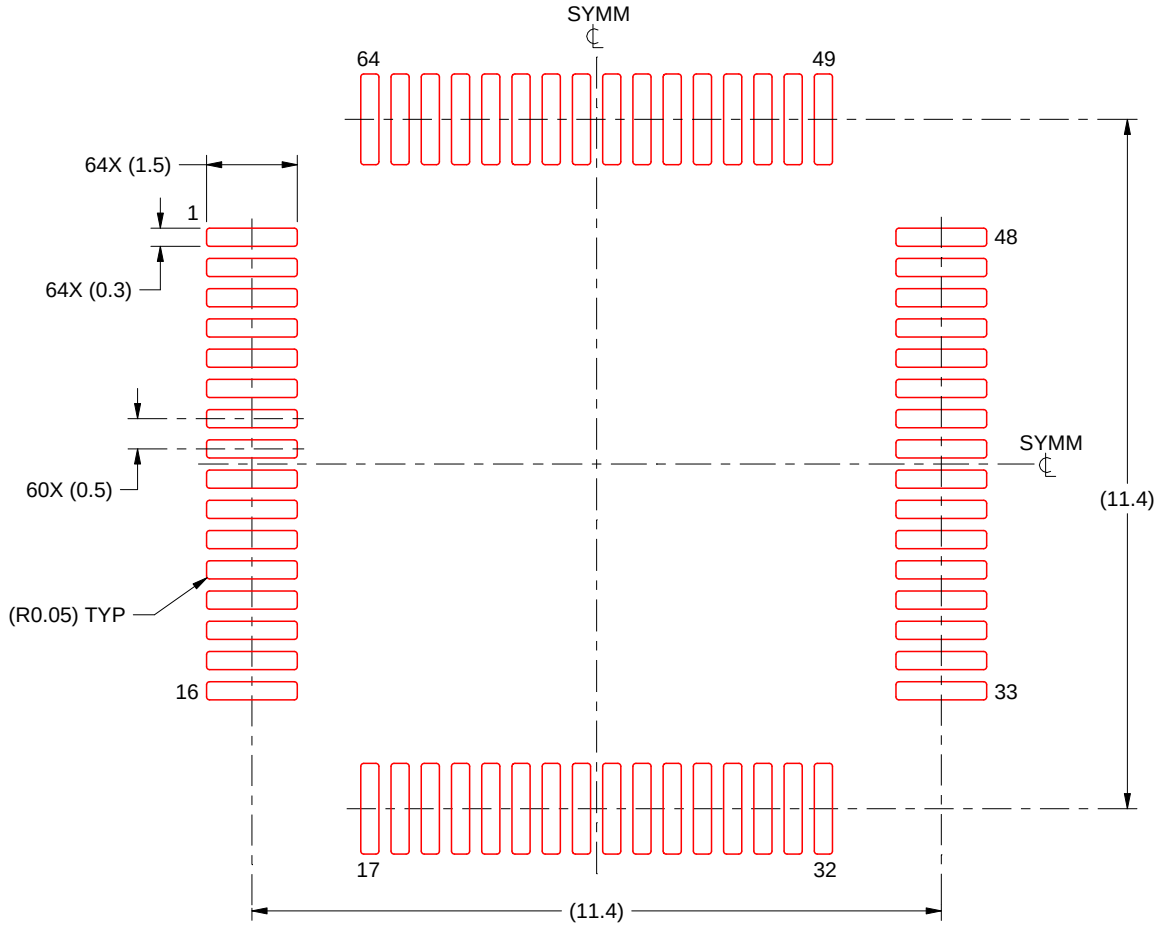


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

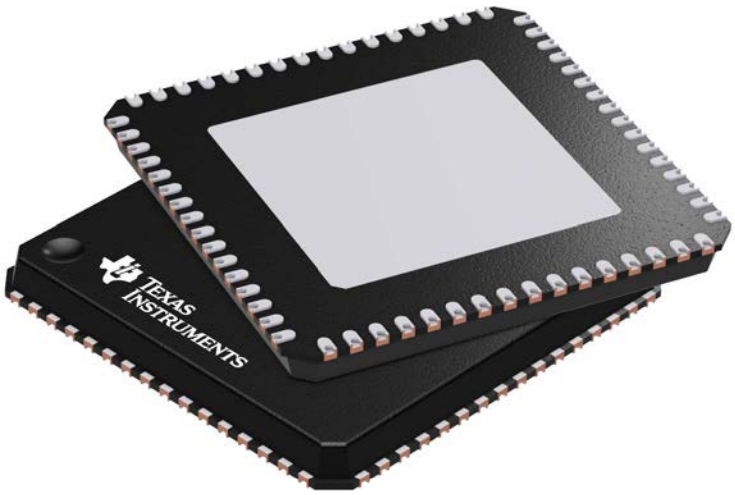
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

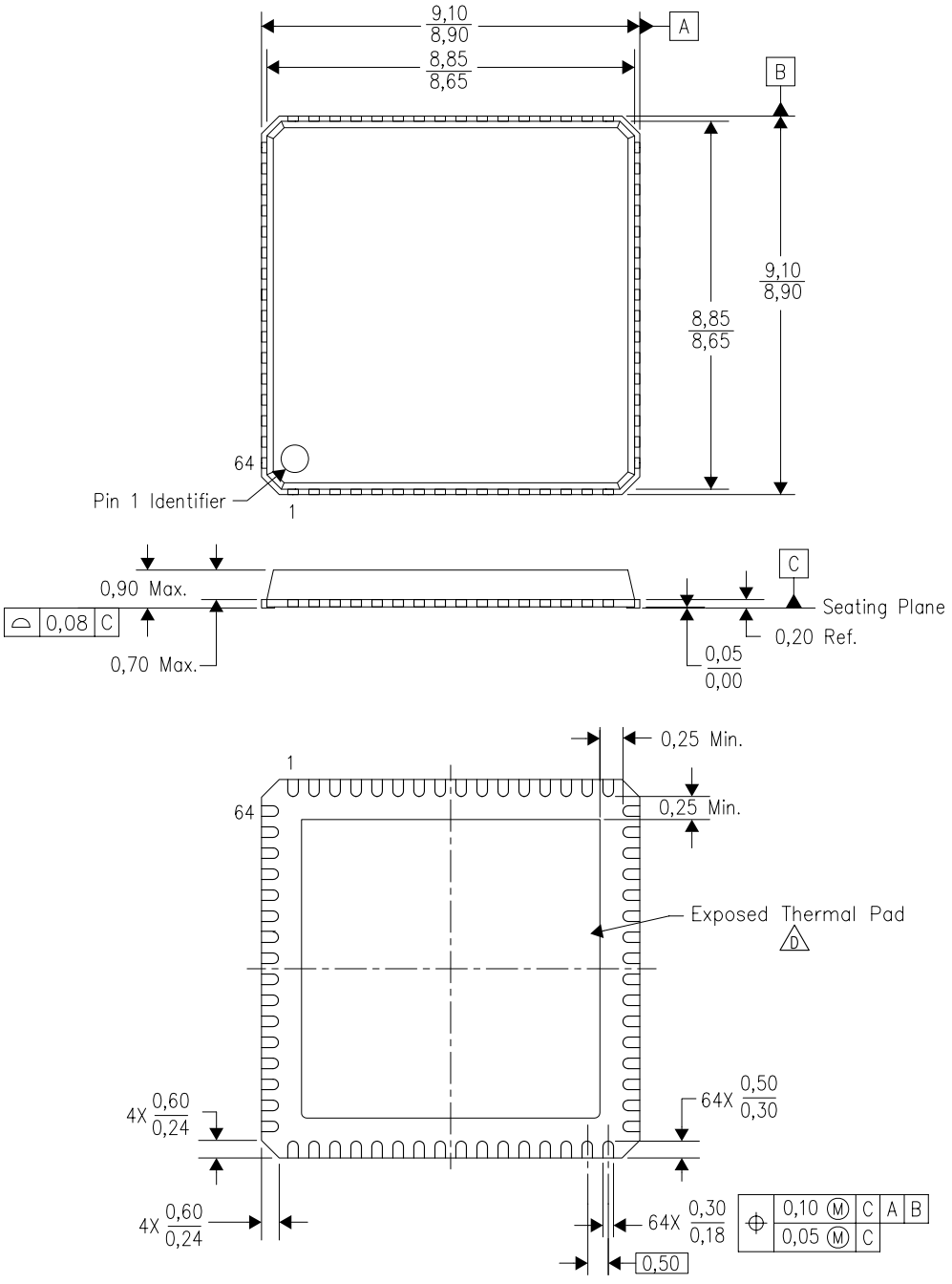
RTD 64 VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

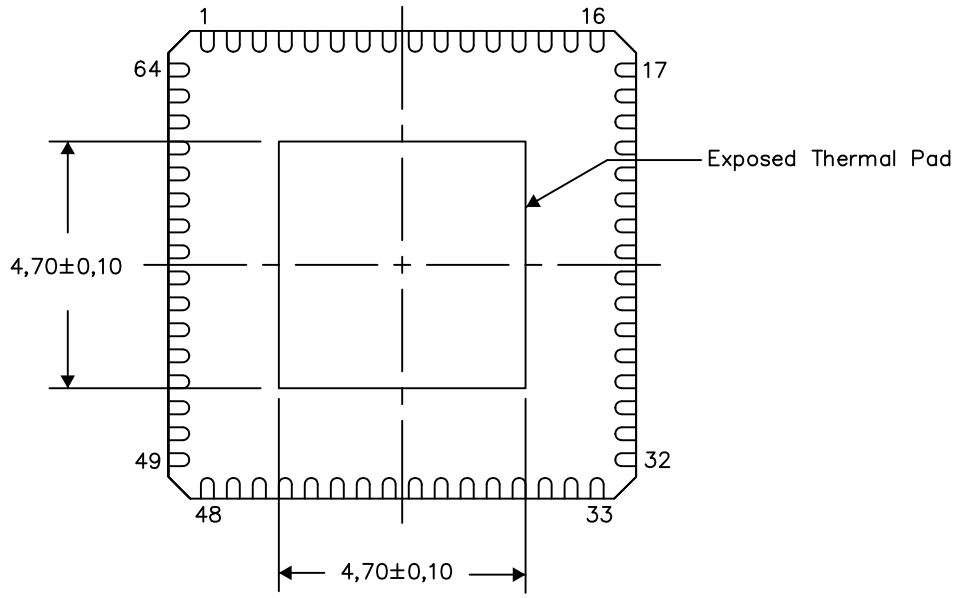
RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



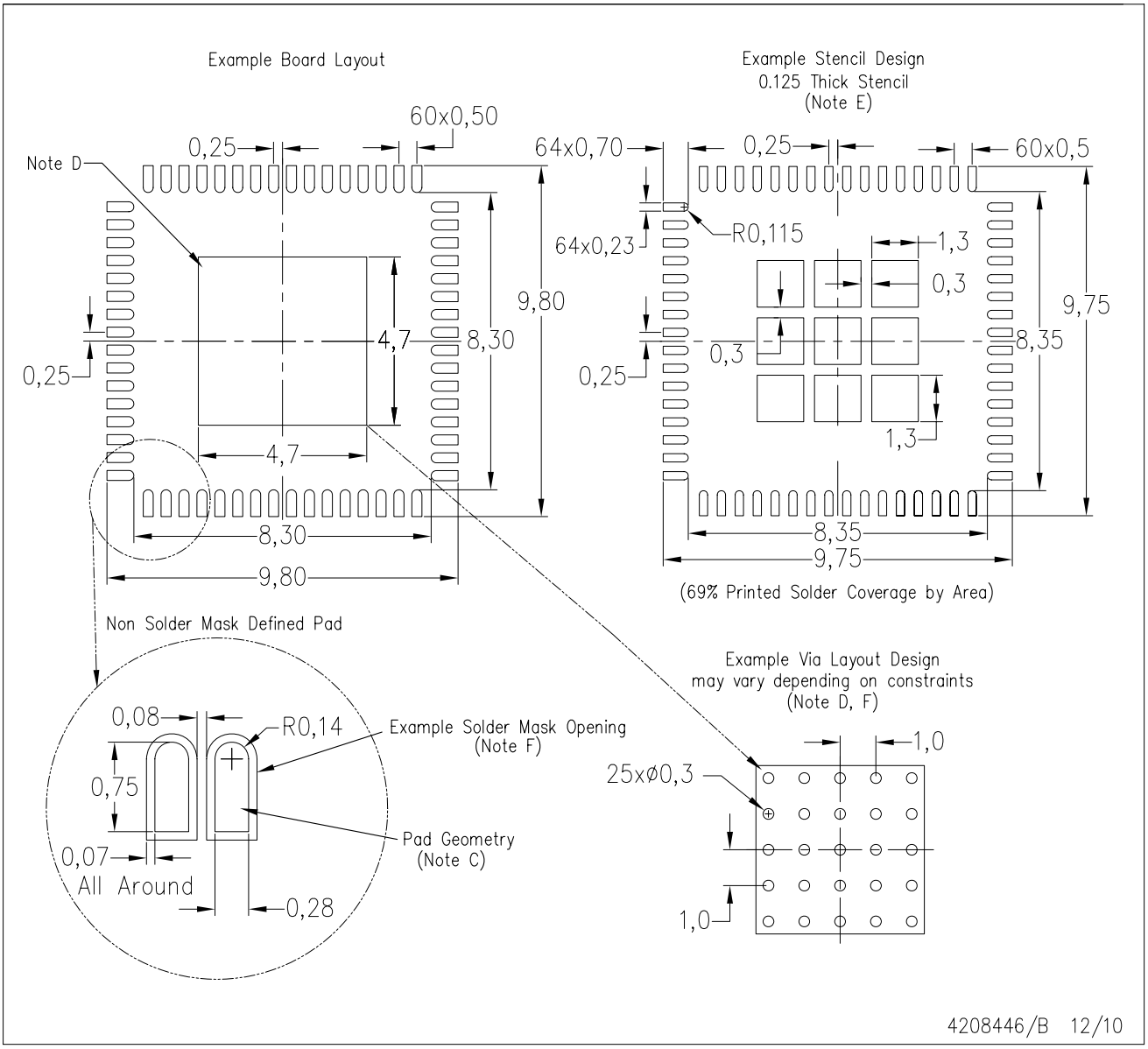
Bottom View

Exposed Thermal Pad Dimensions

4206338–3/F 09/14

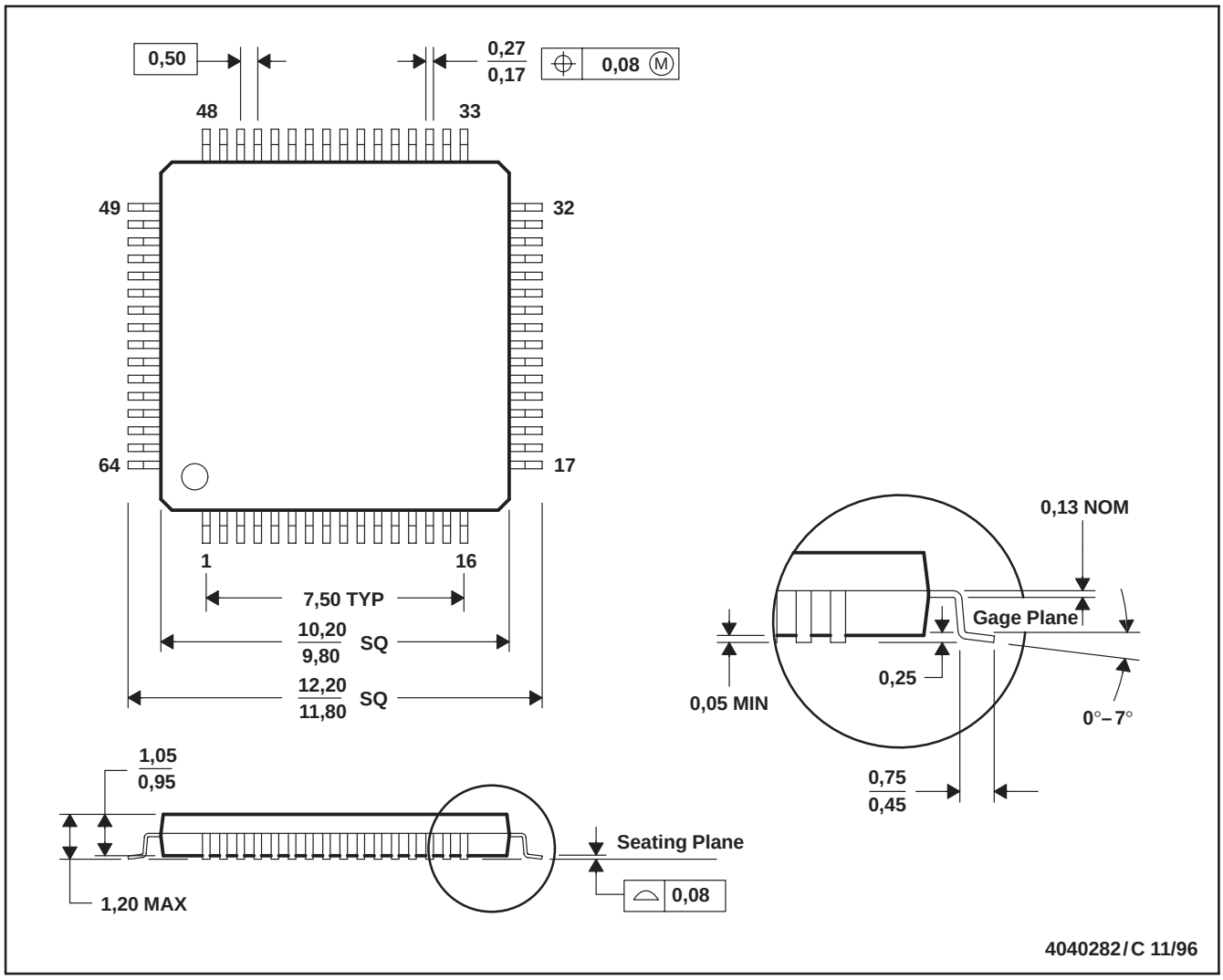
NOTE: A. All linear dimensions are in millimeters

RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Package, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed int the thermal pad.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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