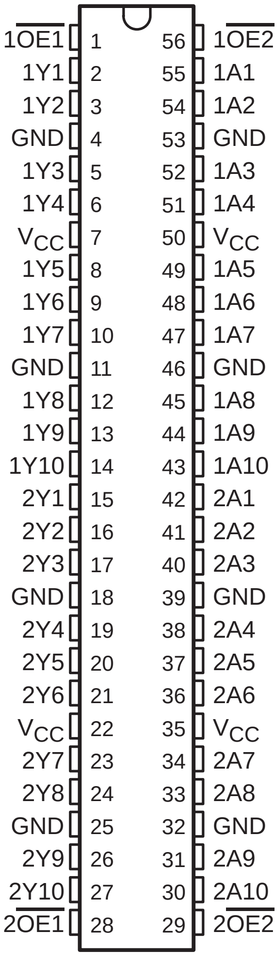
SN54ALVTH16827, SN74ALVTH16827
2.5-V/3.3-V 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES076E – JULY 1996 – REVISED DECEMBER 1998

- **State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **High Drive (–24/24 mA at 2.5-V and –32/64 mA at 3.3-V V_{CC})**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **High-Impedance State During Power Up and Power Down Prevents Driver Conflict**
- **Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Auto3-State Eliminates Bus Current Loading When Output Exceeds V_{CC} + 0.5 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH16827 . . . WD PACKAGE
SN74ALVTH16827 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The ’ALVTH16827 devices are 20-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices are composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1$\overline{\text{OE1}}$ and 1$\overline{\text{OE2}}$, or 2$\overline{\text{OE1}}$ and 2$\overline{\text{OE2}}$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

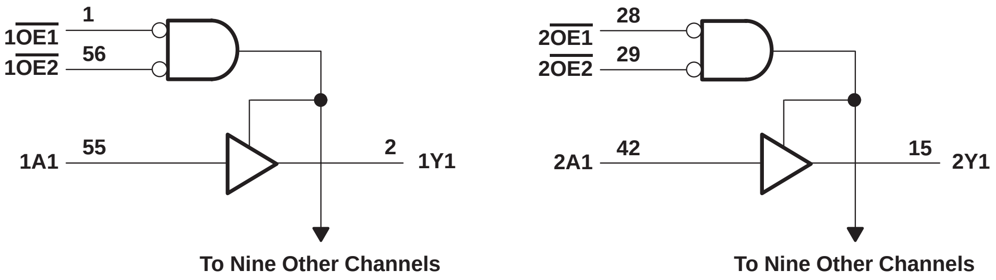
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH16827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH16827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to 7 V
Output current in the low state, I_O: SN54ALVTH16827	96 mA
SN74ALVTH16827	128 mA
Output current in the high state, I_O: SN54ALVTH16827	–48 mA
SN74ALVTH16827	–64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH16827			SN74ALVTH16827			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage		1.7			1.7			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				–6			–8	mA
I_{OL}	Low-level output current				6			8	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz				18			24	
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

			SN54ALVTH16827			SN74ALVTH16827			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3		3.6	3		3.6	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				–24			–32	mA
I_{OL}	Low-level output current				24			32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz				48			64	
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16827			SN74ALVTH16827			UNIT
				MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 2.3 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.3 V to 2.7 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 2.3 V	I_{OH} = –6 mA	1.8						
			I_{OH} = –8 mA				1.8			
V_{OL}		V_{CC} = 2.3 V to 2.7 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 2.3 V	I_{OL} = 6 mA			0.4			0.47	
			I_{OL} = 8 mA						0.4	
			I_{OL} = 18 mA			0.5				
			I_{OL} = 24 mA						0.5	
I_I	Control inputs	V_{CC} = 2.7 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 2.7 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 2.7 V	V_I = 5.5 V			10			10	
			V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}[‡]		V_{CC} = 2.3 V,	V_I = 0.7 V		115			115		µA
I_{BHH}[§]		V_{CC} = 2.3 V,	V_I = 1.7 V		–10			–10		µA
I_{BHLO}[¶]		V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	300			300			µA
I_{BHHO}[#]		V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	–300			–300			µA
I_{EX}[‖]		V_{CC} = 2.3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$[☆]		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 2.7 V	V_O = 2.3 V, V_I = 0.7 V or 1.7 V			5			5	µA
I_{OZL}		V_{CC} = 2.7 V	V_O = 0.5 V, V_I = 0.7 V or 1.7 V			–5			–5	µA
I_{CC}		V_{CC} = 2.7 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.04	0.1		0.04	0.1	mA
			Outputs low		2.3	5		2.3	5	
			Outputs disabled		0.04	0.1		0.04	0.1	
C_i		V_{CC} = 2.5 V,	V_I = 2.5 V or 0		3			3		pF
C_o		V_{CC} = 2.5 V,	V_O = 2.5 V or 0		6			6		pF

[†] All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
[‡] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
[§] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.
[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.
[‖] Current into an output in the high state when V_O > V_{CC}
[☆] High-impedance state during power up or power down

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16827			SN74ALVTH16827			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 3 V	I_{OL} = 16 mA						0.4	
			I_{OL} = 24 mA			0.5				
			I_{OL} = 32 mA						0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 3.6 V	V_I = 5.5 V			10			10	
			V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡		V_{CC} = 3 V,	V_I = 0.8 V	75			75			µA
I_{BHH}§		V_{CC} = 3 V,	V_I = 2 V	–75			–75			µA
I_{BHLO}¶		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	500			500			µA
I_{BHHO}#		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	–500			–500			µA
I_{EX}‖		V_{CC} = 3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$☆		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 3.6 V	V_O = 3 V, V_I = 0.8 V or 2 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V	V_O = 0.5 V, V_I = 0.8 V or 2 V			–5			–5	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.07	0.1		0.07	0.1	mA
			Outputs low		3.2	6		3.2	6	
			Outputs disabled		0.07	0.1		0.07	0.1	
ΔI_{CC}□		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.4			0.4	mA
C_i		V_{CC} = 3.3 V,	V_I = 3.3 V or 0		3			3		pF
C_o		V_{CC} = 3.3 V,	V_O = 3.3 V or 0		6			6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

‖ Current into an output in the high state when V_O > V_{CC}

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

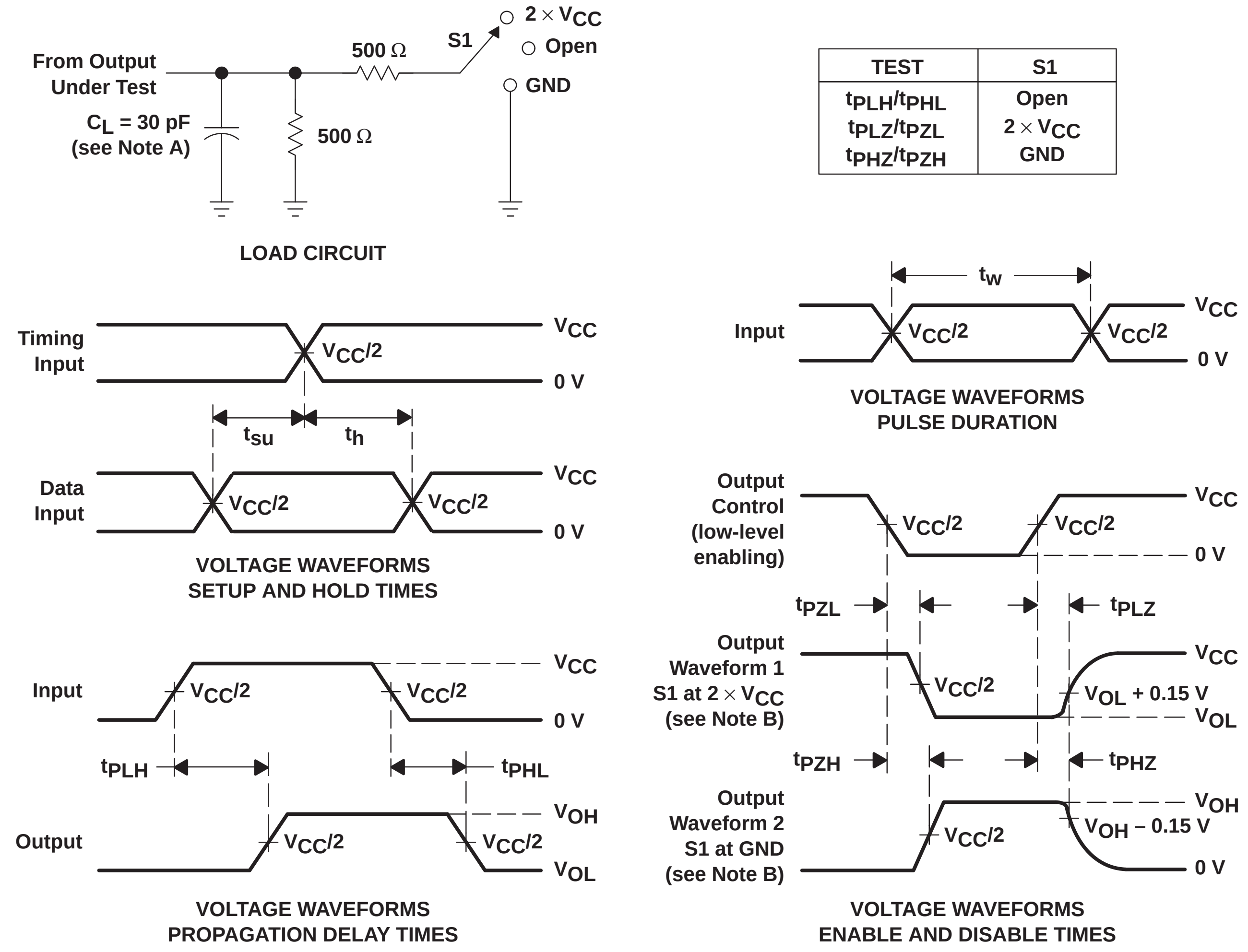
switching characteristics over recommended operating free-air temperature range, $C_L = 30$ pF, $V_{CC} = 2.5$ V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16827		SN74ALVTH16827		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	3.2	1.5	3.2	ns
t_{PHL}			1.7	3.7	1.7	3.7	
t_{PZH}	$\overline{OE}$	Y	1.9	4.3	1.9	4.3	ns
t_{PZL}			1.8	4	1.8	4	
t_{PHZ}	$\overline{OE}$	Y	2.5	5.6	2.5	5.6	ns
t_{PLZ}			1.7	4.6	1.7	4.6	

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF, $V_{CC} = 3.3$ V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16827		SN74ALVTH16827		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.8	3	1.8	3	ns
t_{PHL}			1.6	2.8	1.6	2.8	
t_{PZH}	$\overline{OE}$	Y	1.6	3.9	1.6	3.9	ns
t_{PZL}			1.5	3.4	1.5	3.4	
t_{PHZ}	$\overline{OE}$	Y	3.3	5.8	3.3	5.8	ns
t_{PLZ}			2.6	4.6	2.6	4.6	

PARAMETER MEASUREMENT INFORMATION
$V_{CC} = 2.5\ V \pm 0.2\ V$

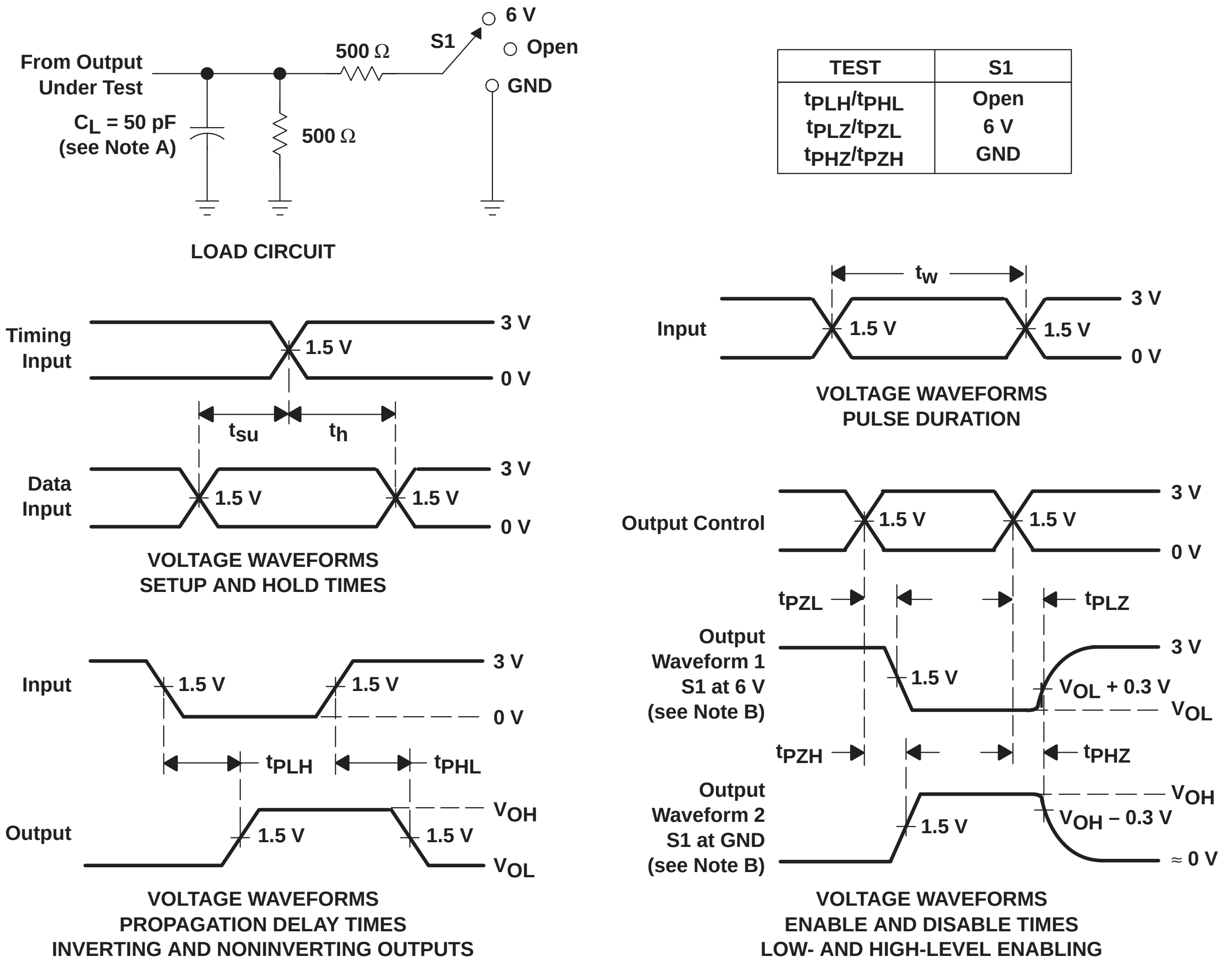


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform22 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVTH16827DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16827	Samples
SN74ALVTH16827DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16827	Samples
SN74ALVTH16827GR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVTH16827	Samples
SN74ALVTH16827VR	ACTIVE	TVSOP	DGV	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VT827	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

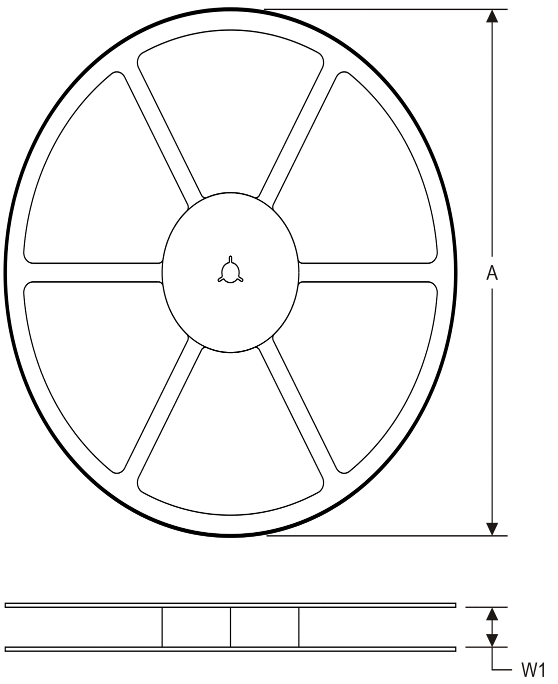
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

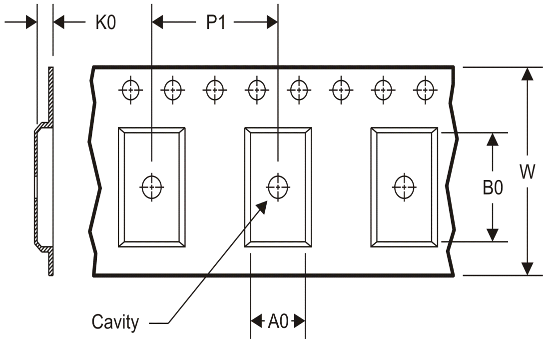
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



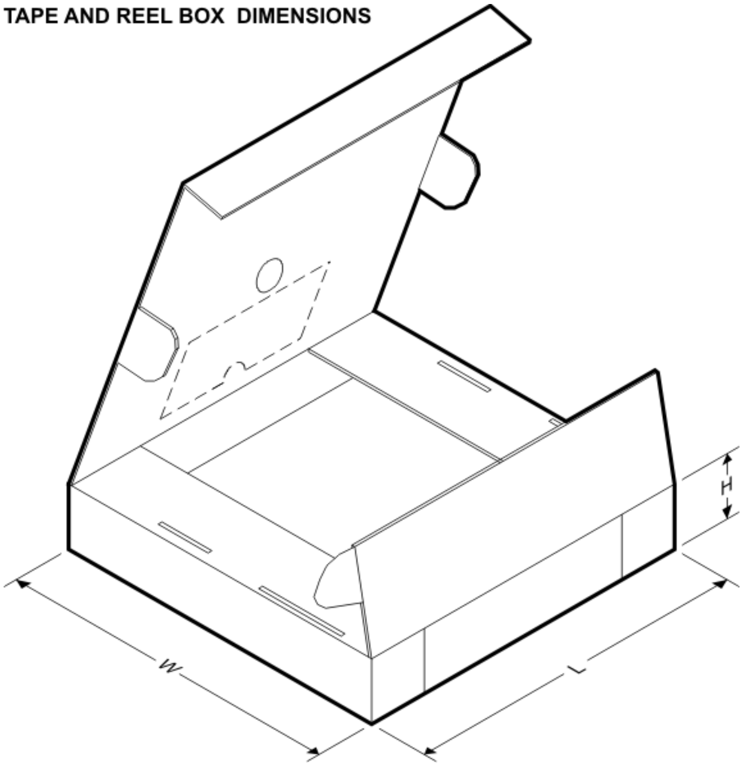
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVTH16827DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ALVTH16827GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVTH16827VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



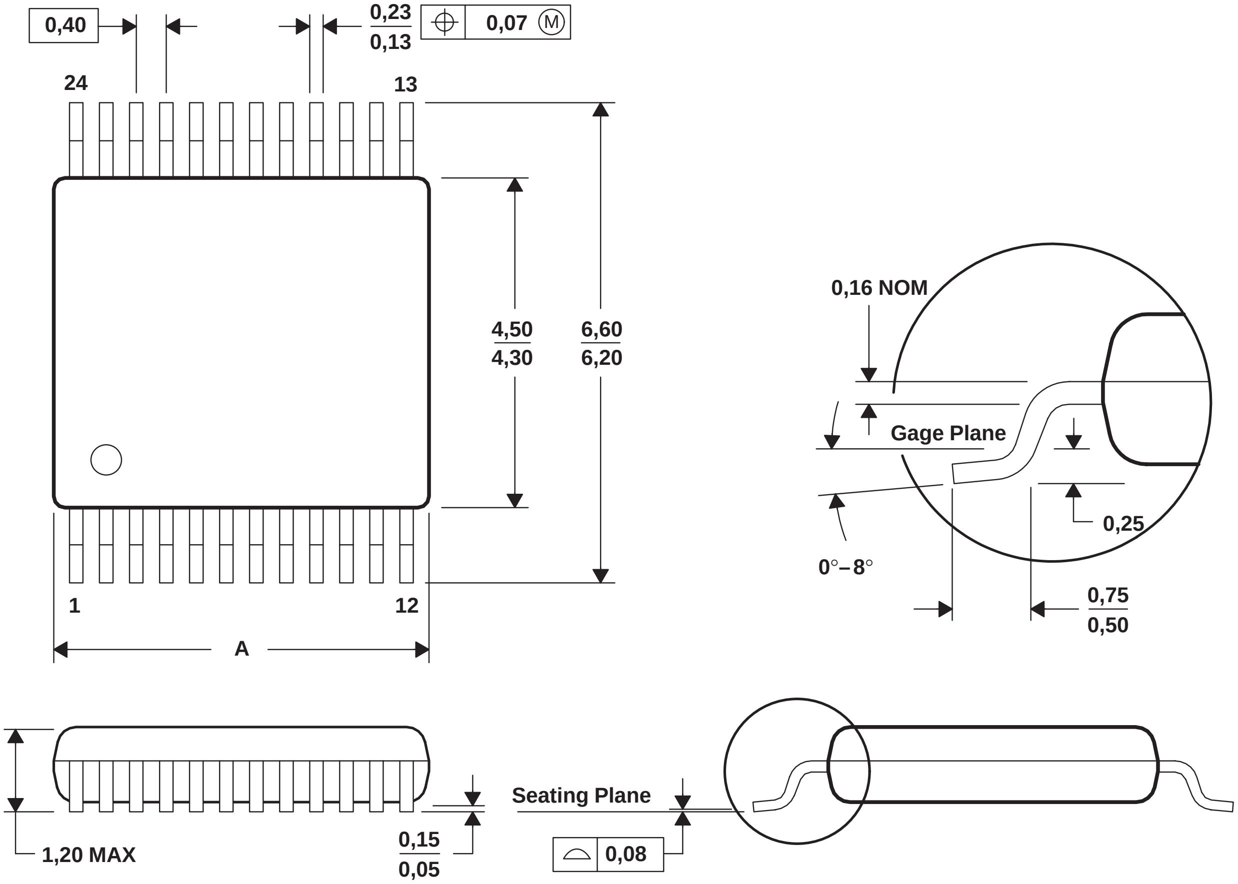
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVTH16827DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74ALVTH16827GR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ALVTH16827VR	TVSOP	DGV	56	2000	367.0	367.0	45.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

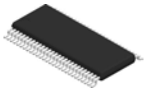


PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

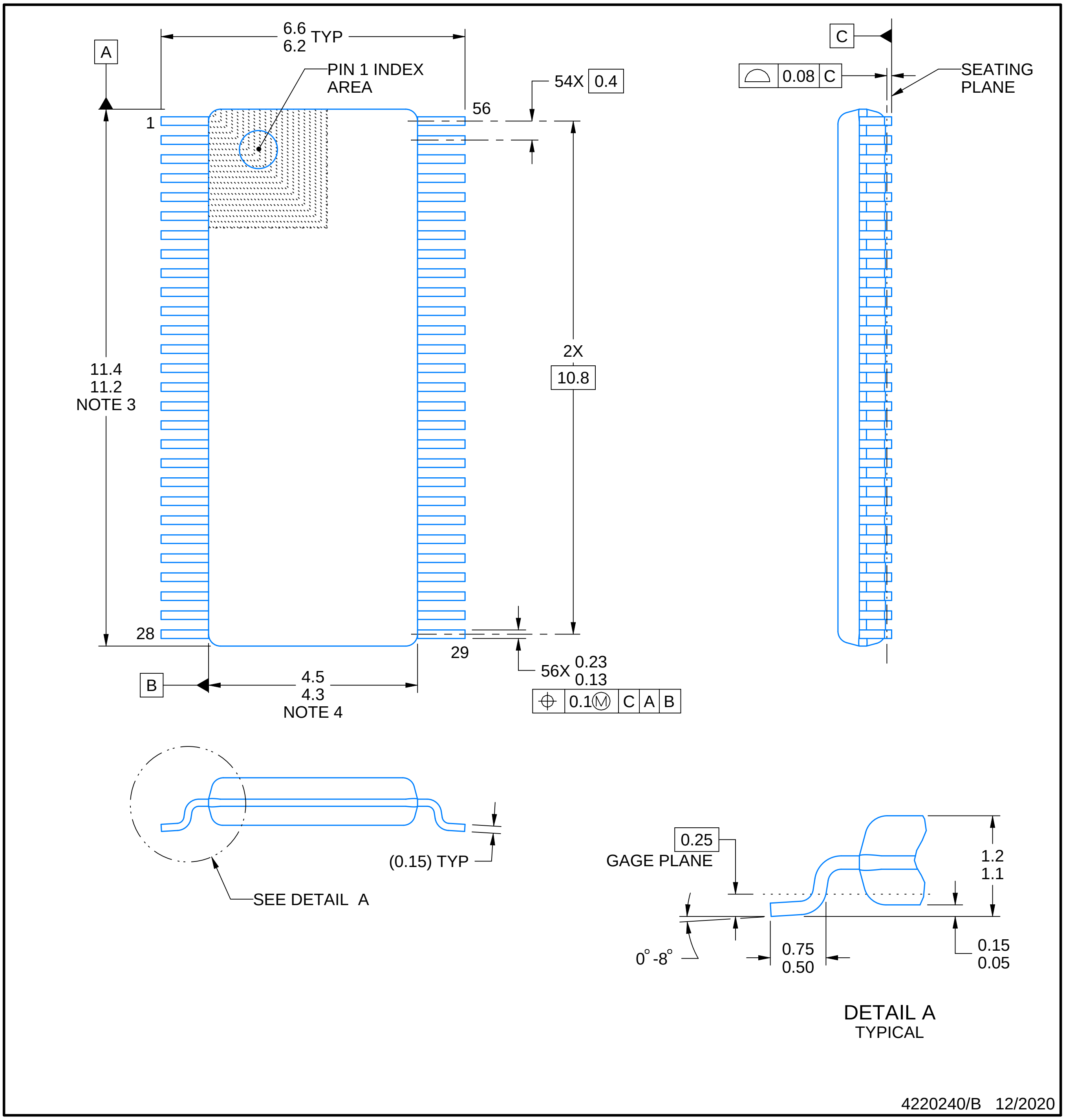
PACKAGE OUTLINE



DGV0056A

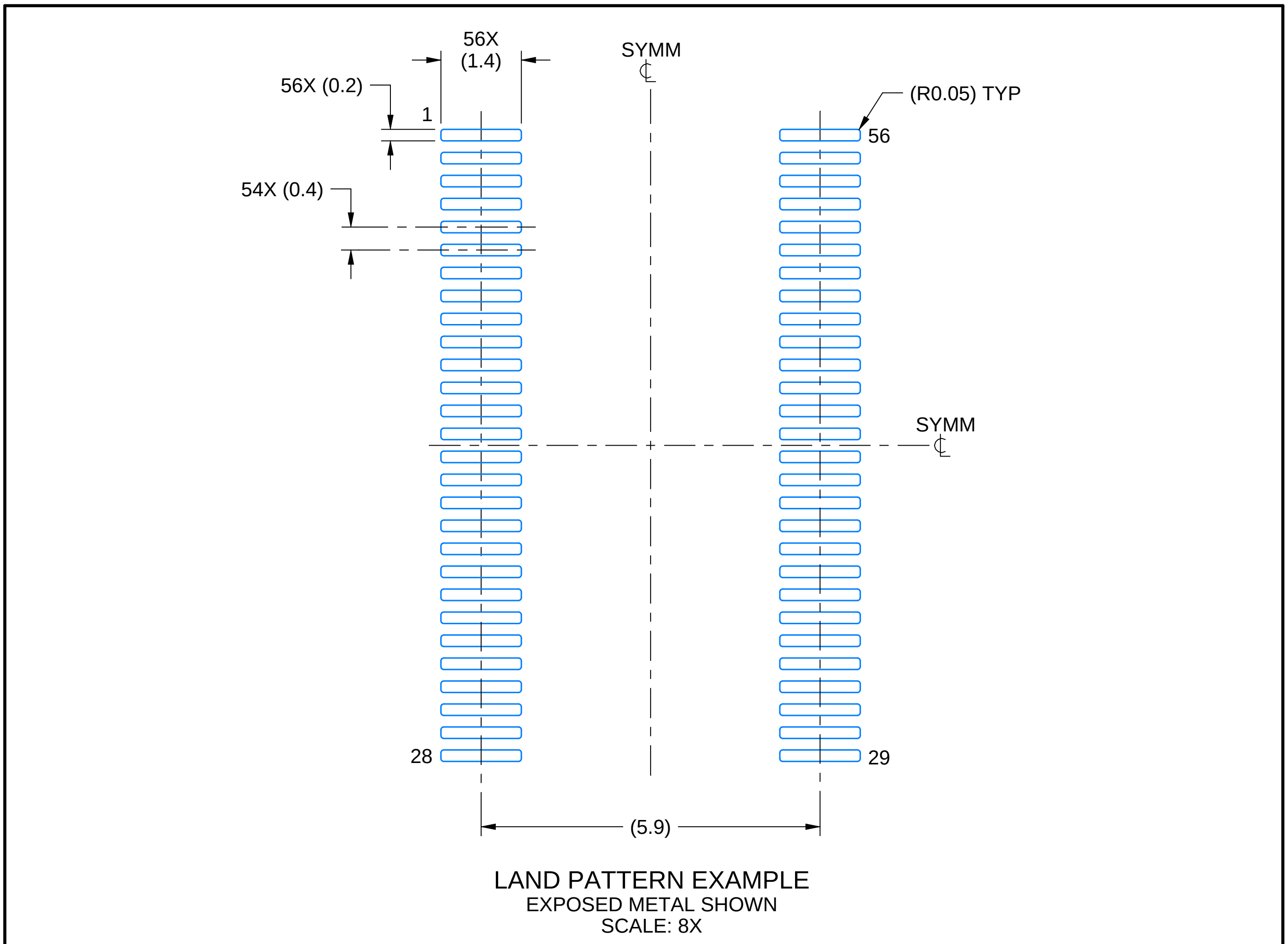
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

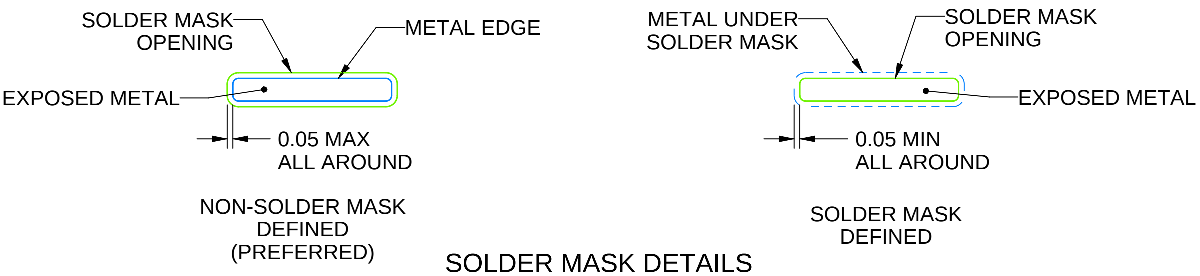


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

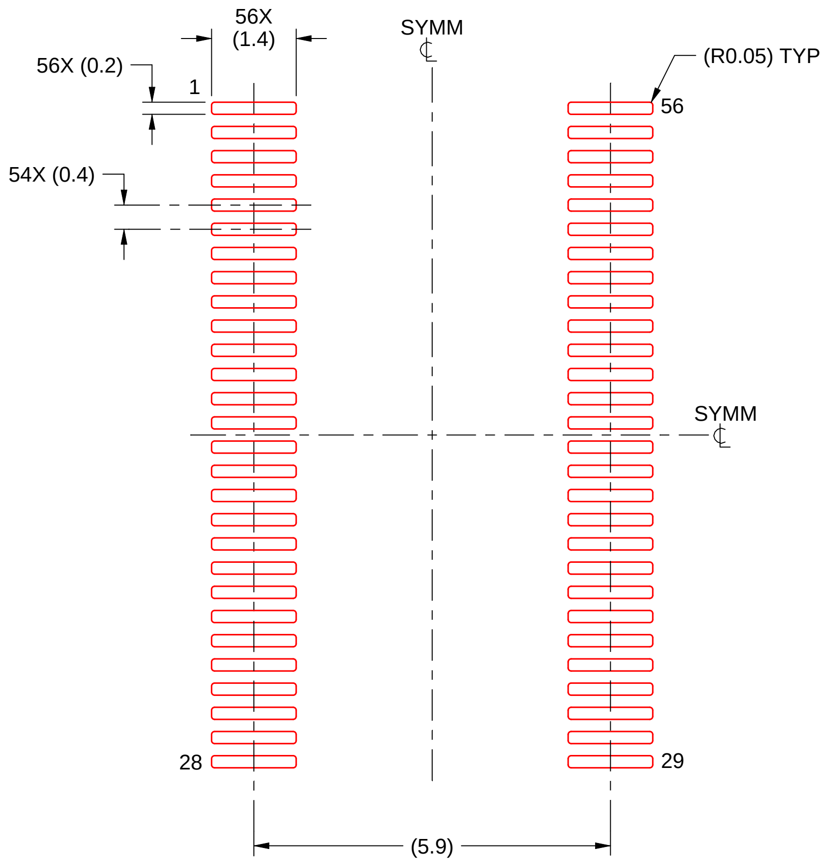


SOLDER MASK DETAILS

4220240/B 12/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

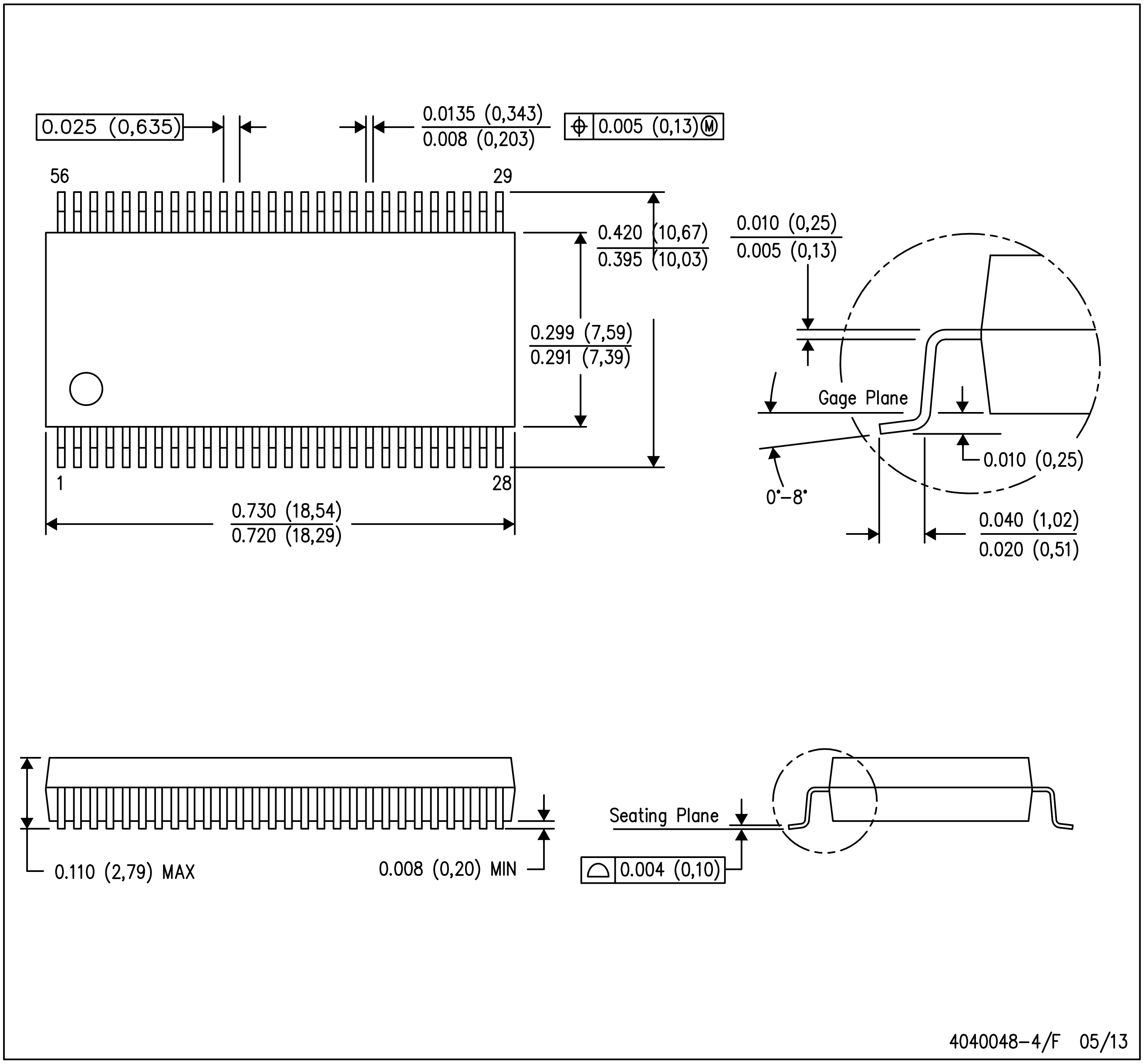


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

NOTES: (continued)

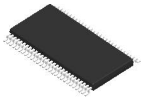
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

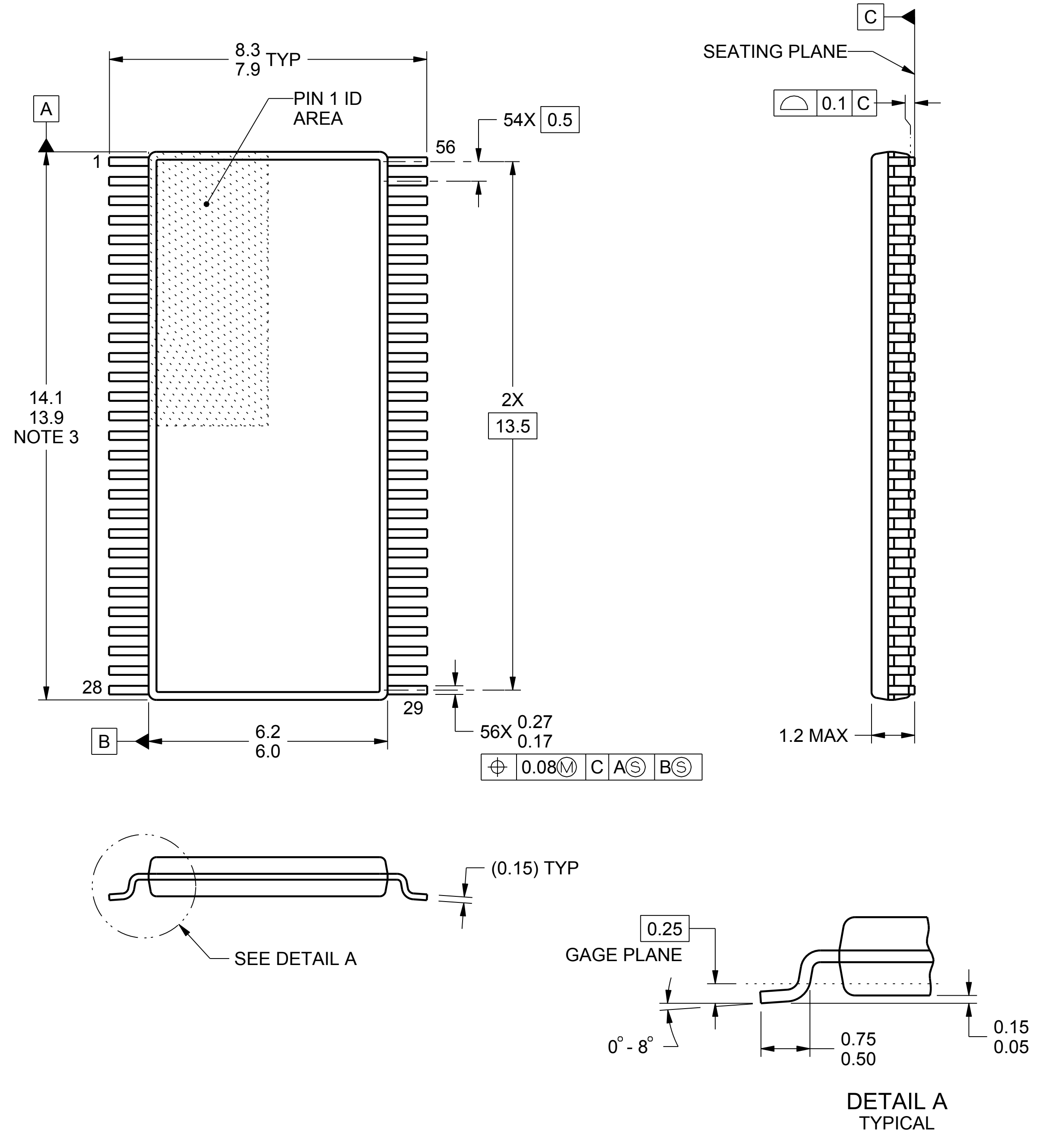


PACKAGE OUTLINE

DGG0056A

TSSOP - 1.2 mm max height

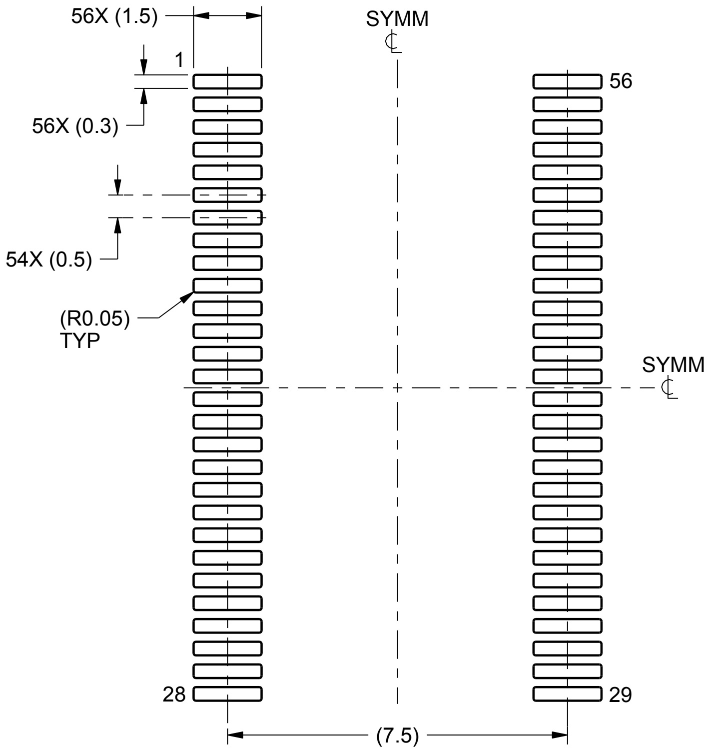
SMALL OUTLINE PACKAGE



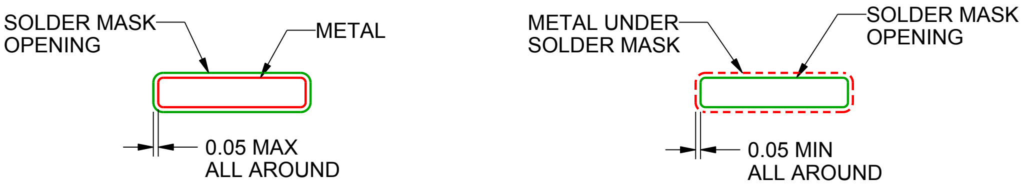
4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



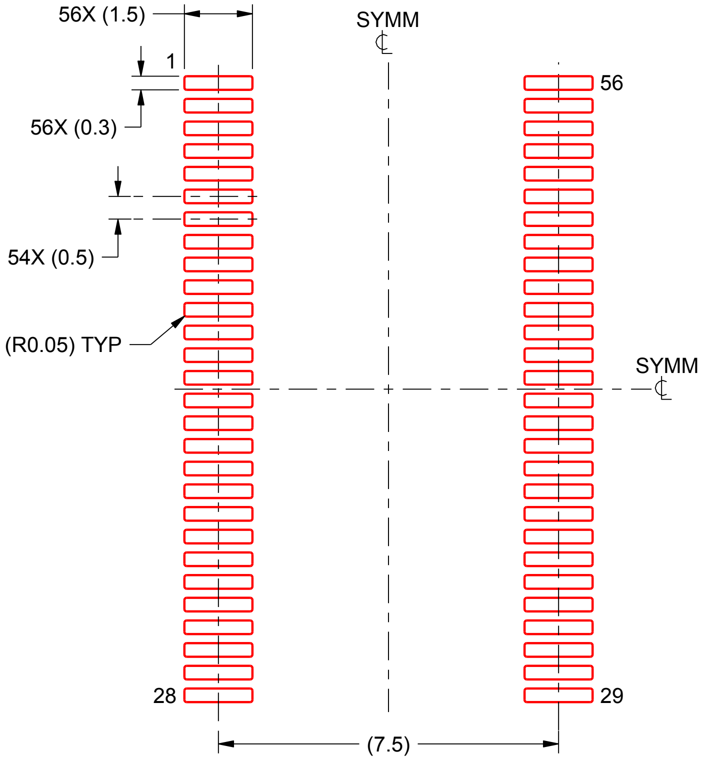
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated