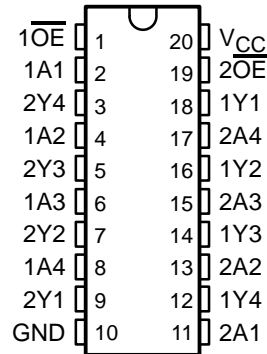


- **Q Devices Meet Automotive Performance Requirements**
- **Customer-Specific Configuration Control Can Be Supported Along with Major-Change Approval**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

**DW OR PW PACKAGE**  
**(TOP VIEW)**



## description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT244Q is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Tape and reel	SN74AHCT244QDWR	AHCT244Q
	TSSOP – PW	Tape and reel	SN74AHCT244QPWR	HB244Q

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**  
**(each 4-bit buffer/driver)**

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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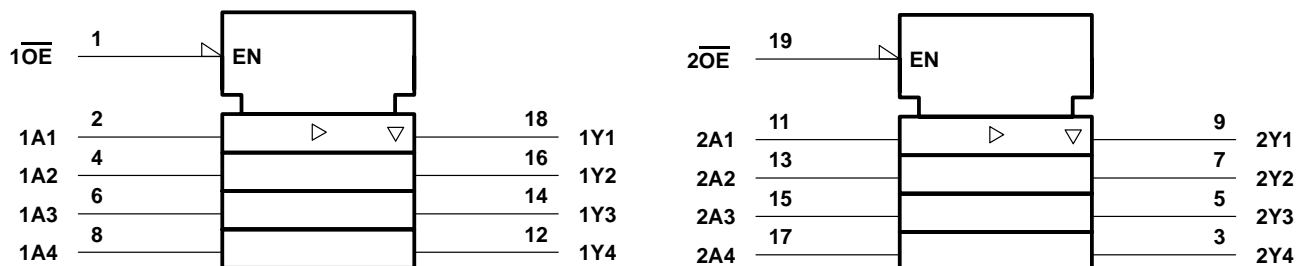
# SN74AHCT244Q

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

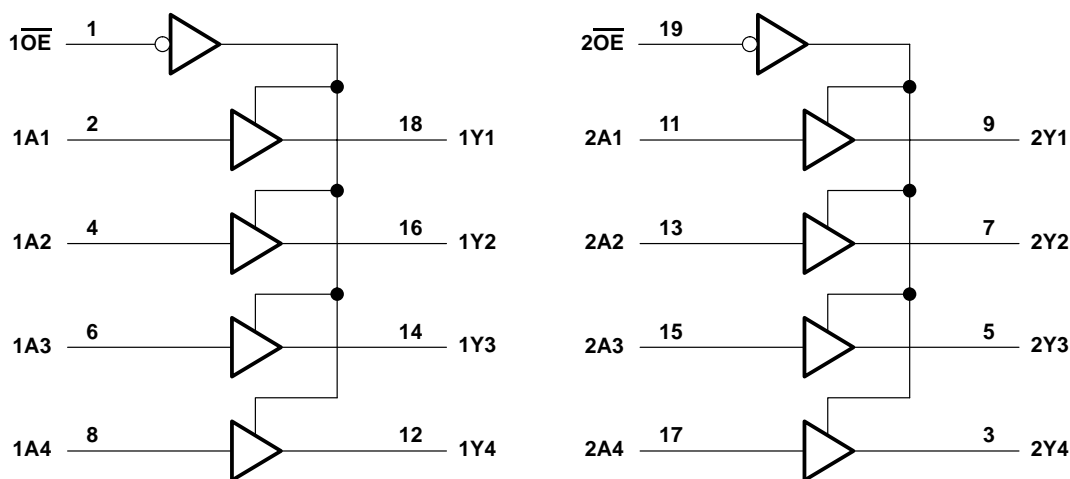
SGDS024 – FEBRUARY 2002

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	58°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–8	mA
I <sub>OL</sub>	Low-level output current		8	mA
T <sub>A</sub>	Operating free-air temperature	–40	125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = –50 µA	4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = –8 mA		3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.25		±2.5		µA
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40		µA
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		1.35		1.5		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		3				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		5.4	7.4	1	8.5	ns
t <sub>PHL</sub>					5.4	7.4	1	8.5	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Y	C <sub>L</sub> = 15 pF		7.7	10.4	1	12	ns
t <sub>PZL</sub>					7.7	10.4	1	12	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Y	C <sub>L</sub> = 15 pF		5	9.4	1	10	ns
t <sub>PLZ</sub>					5	9.4	1	10	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		5.9	8.4	1	9.5	ns
t <sub>PHL</sub>					5.9	8.4	1	9.5	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Y	C <sub>L</sub> = 50 pF		8.2	11.4	1	13	ns
t <sub>PZL</sub>					8.2	11.4	1	13	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Y	C <sub>L</sub> = 50 pF		8.8	11.4	1	13	ns
t <sub>PLZ</sub>					8.8	11.4	1	13	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1			ns

# SN74AHCT244Q

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OH}(V)$	Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH}(D)$	High-level dynamic input voltage	2			V
$V_{IL}(D)$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

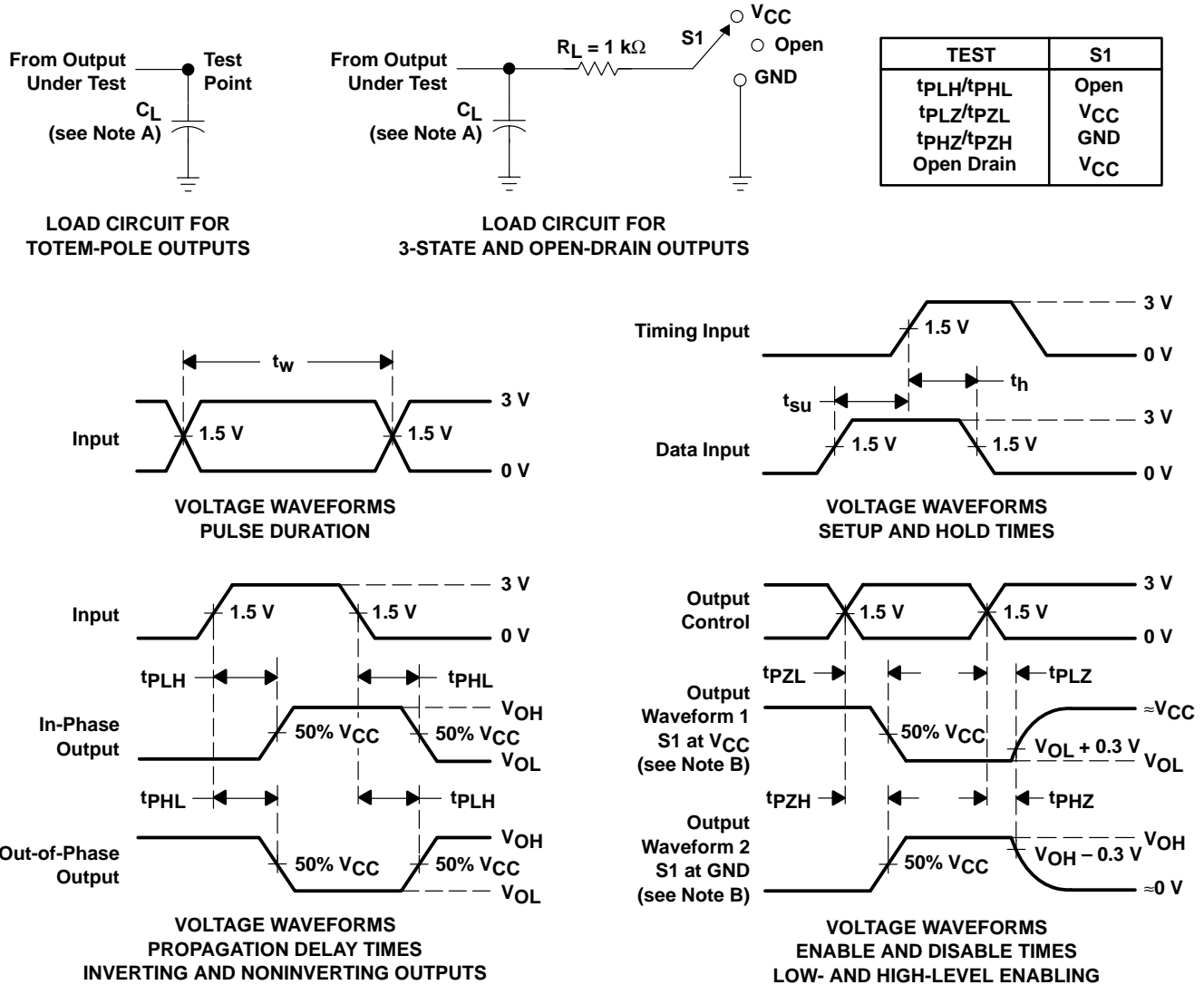
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	8.2	pF



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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT244QDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT244Q	<a href="#">Samples</a>
SN74AHCT244QDWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT244Q	<a href="#">Samples</a>
SN74AHCT244QPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB244Q	<a href="#">Samples</a>
SN74AHCT244QPWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		HB244Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT244QDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT244QDWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT244QPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT244QPWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT244QDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT244QDWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT244QPWR	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74AHCT244QPWRG4	TSSOP	PW	20	2000	853.0	449.0	35.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**DW0020A****PACKAGE OUTLINE****SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

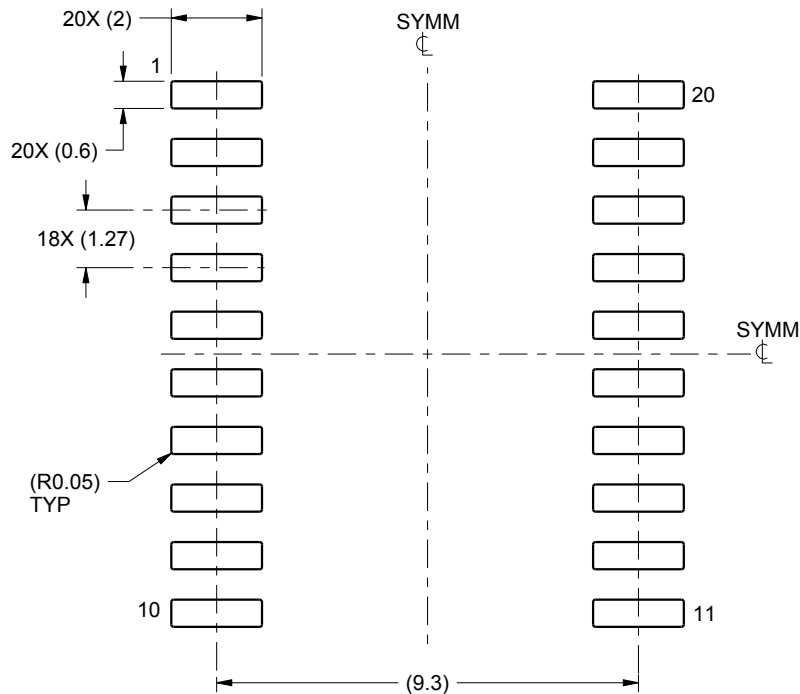
**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

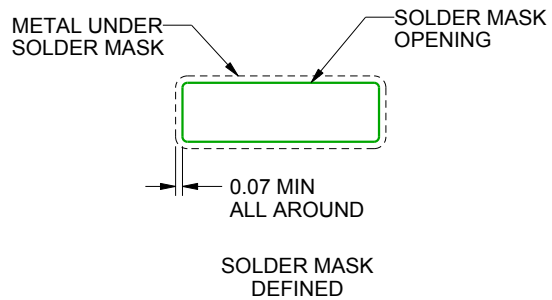
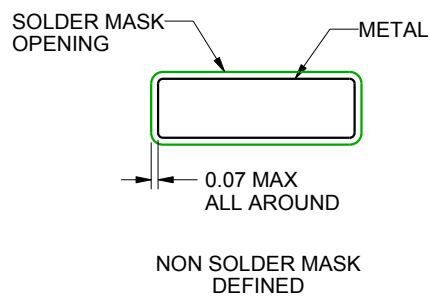
**DW0020A**

**SOIC - 2.65 mm max height**

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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