

SN54ABT5402A, SN74ABT5402A 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS660B – FEBRUARY 1996 – REVISED MAY 1997

- Output Ports Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*[™] BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OLV} (Output Undershoot) < 0.5 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW) Package and Ceramic Chip Carriers (FK) and DIPs (JT)

description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

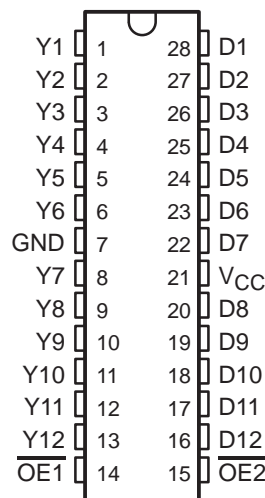
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all 12 outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25- Ω series resistors to reduce overshoot and undershoot.

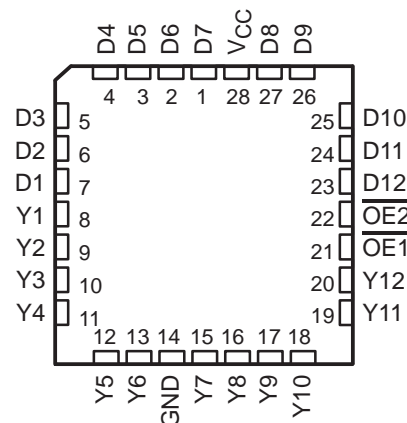
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5402A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT5402A is characterized for operation from -40°C to 85°C .

SN54ABT5402A . . . JT PACKAGE
SN74ABT5402A . . . DW PACKAGE
(TOP VIEW)



SN54ABT5402A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	D	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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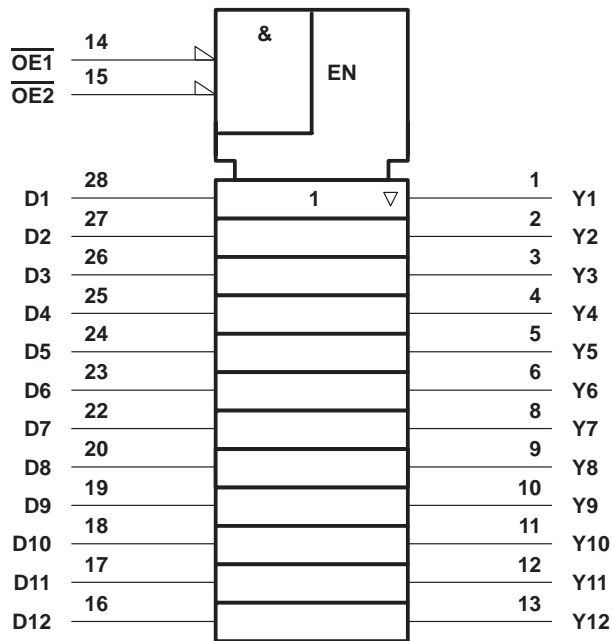
**TEXAS
INSTRUMENTS**

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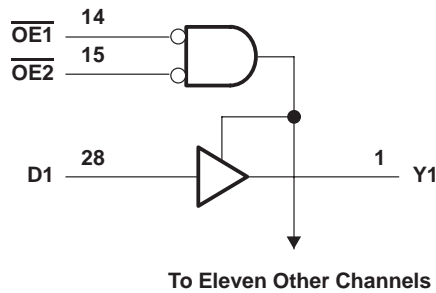
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 12-BIT LINE/MEMORY DRIVERS
 WITH 3-STATE OUTPUTS
 SCBS660B – FEBRUARY 1996 – REVISED MAY 1997

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	78°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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12-BIT LINE/MEMORY DRIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54ABT5402A		SN74ABT5402A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			–12		–12	mA
I _{OL}	Low-level output current			12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			SN54ABT5402A		SN74ABT5402A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –1 mA	3.35	3.7		3.3		3.35		V
		V _{CC} = 5 V, I _{OH} = –1 mA	3.85	4.2		3.8		3.85		
		V _{CC} = 4.5 V, I _{OH} = –3 mA				3		3.1		
		V _{CC} = 4.5 V, I _{OH} = –12 mA	2.6					2.6		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 8 mA				0.8		0.65		V
		V _{CC} = 4.5 V, I _{OL} = 12 mA						0.8		
V _{hys}				100						mV
I _I		V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V			10	10		10		μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.5 V			–10	–10		–10		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100			±100		μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50	50		50		μA
I _O		V _{CC} = 5.5 V, V _O = 2.5 V	–25	–45	–100	–25	–100	–25	–100	mA
I _{OS‡}		V _{CC} = 5.5 V, V _O = 0	–50		–200	–50	–200	–50	–200	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs high		5	50	50		50		μA
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs low		39	48	48		48		mA
		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs disabled		1	50	50		50		μA
ΔI _{CC} §	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND, Outputs enabled		1.5		1.5		1.5		mA
	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND, Outputs disabled		0.05		0.05		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5		1.5		1.5		
C _i		V _I = 2.5 V or 0.5 V		3						pF
C _o		V _O = 2.5 V or 0.5 V		8						pF

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54ABT5402A, SN74ABT5402A

12-BIT LINE/MEMORY DRIVERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

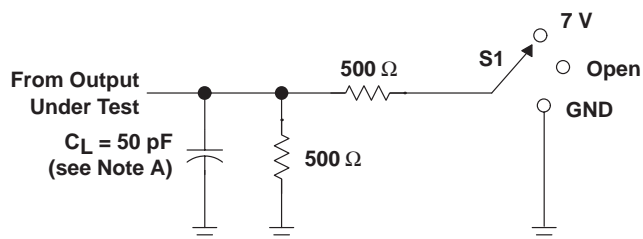
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT5402A		SN74ABT5402A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	2	4.5	5.2	2	6.3	2	6.2	ns
t_{PHL}			1.5	3.7	5	1.5	5.7	1.5	5.6	
t_{PZH}	\overline{OE}	Y	2.5	5.7	7.6	2.5	8.8	2.5	8.7	ns
t_{PZL}			2	4.4	6.3	2	7.6	2	7.5	
t_{PHZ}	\overline{OE}	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
t_{PLZ}			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

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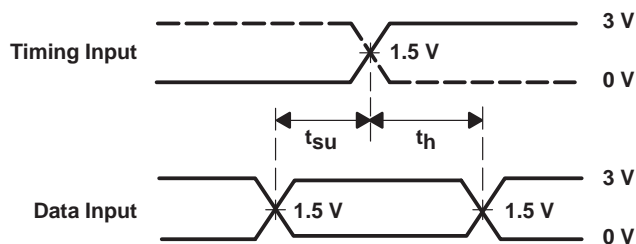
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PARAMETER MEASUREMENT INFORMATION

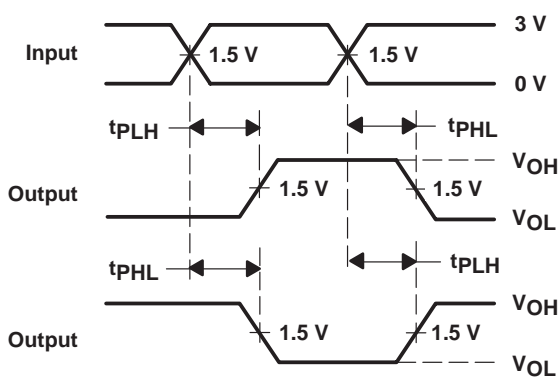


LOAD CIRCUIT

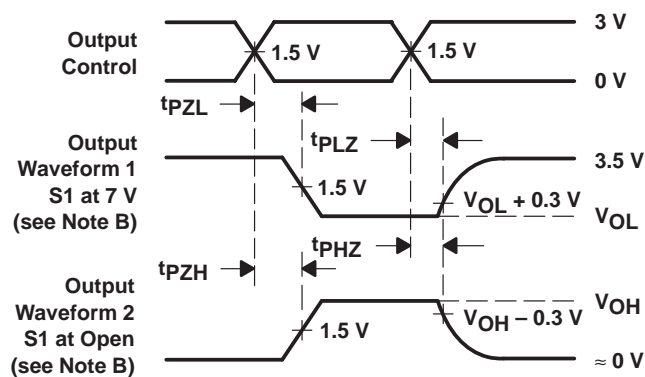
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT5402ADW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT5402A	Samples
SN74ABT5402ADWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT5402A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT5402ADWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

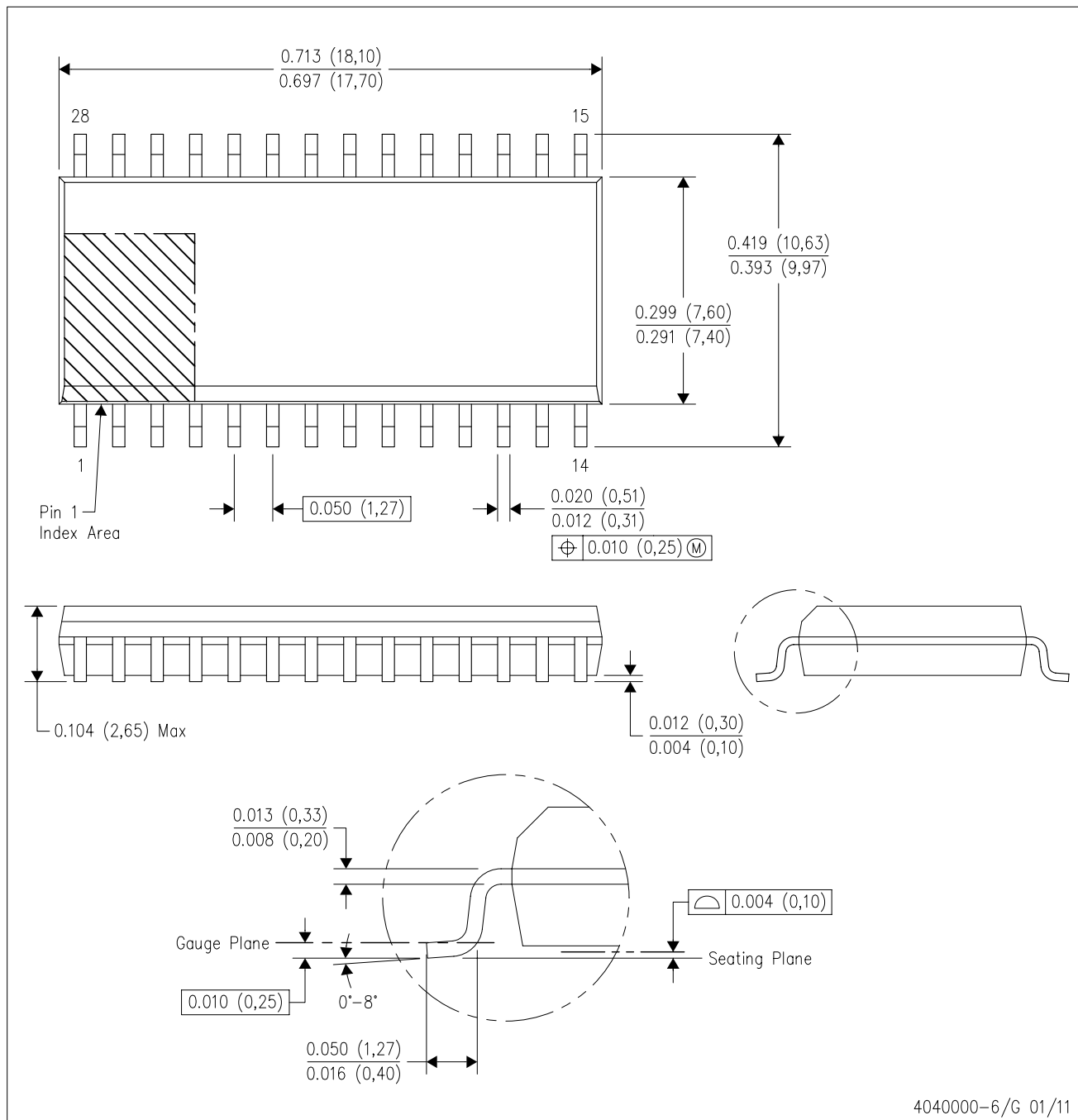


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT5402ADWR	SOIC	DW	28	1000	350.0	350.0	66.0

DW (R-PDSO-G28)

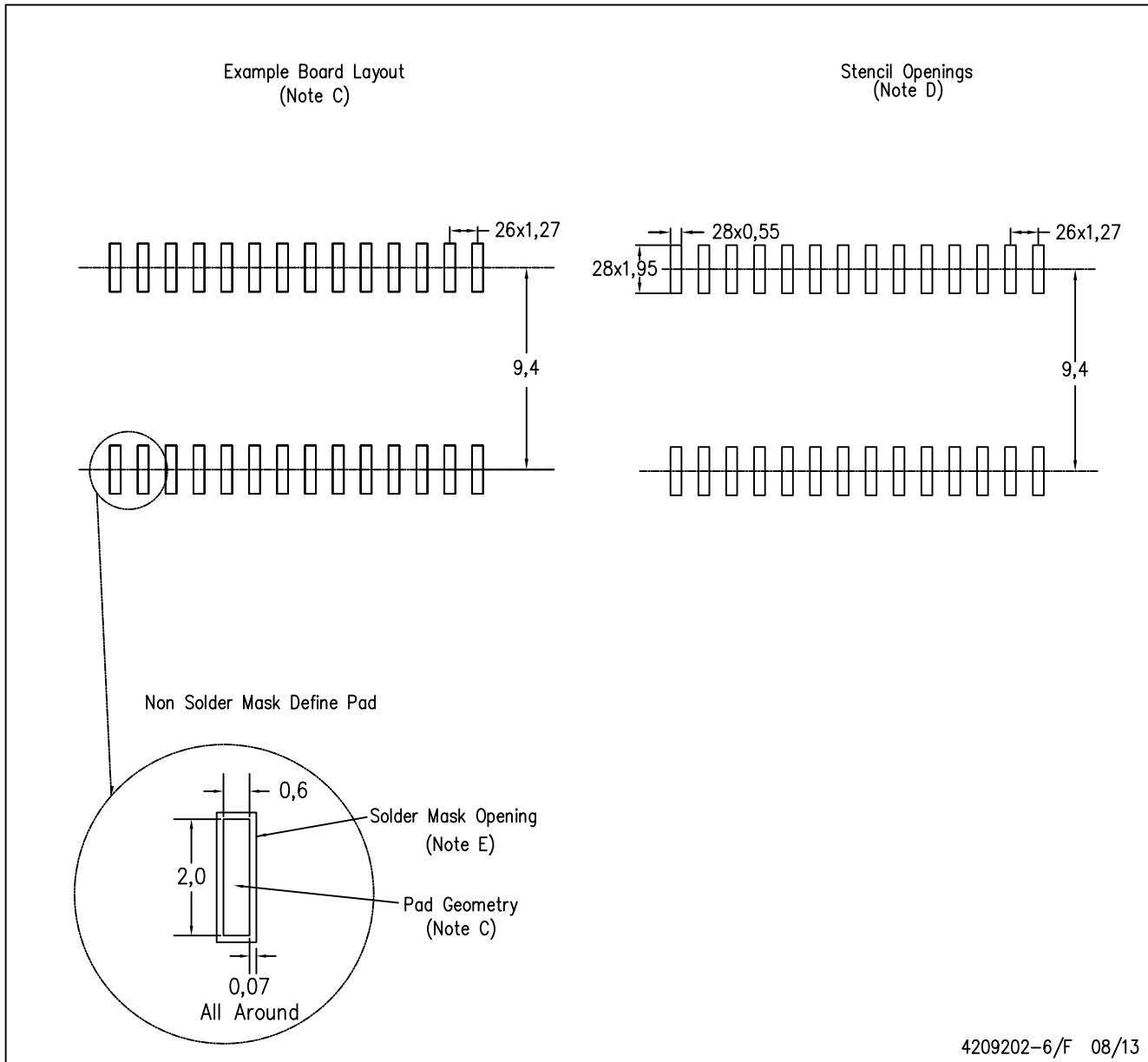
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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