20-W STEREO DIGITAL AUDIO POWER AMPLIFIER WITH EQ AND DRC

Check for Samples: TAS5705

FEATURES

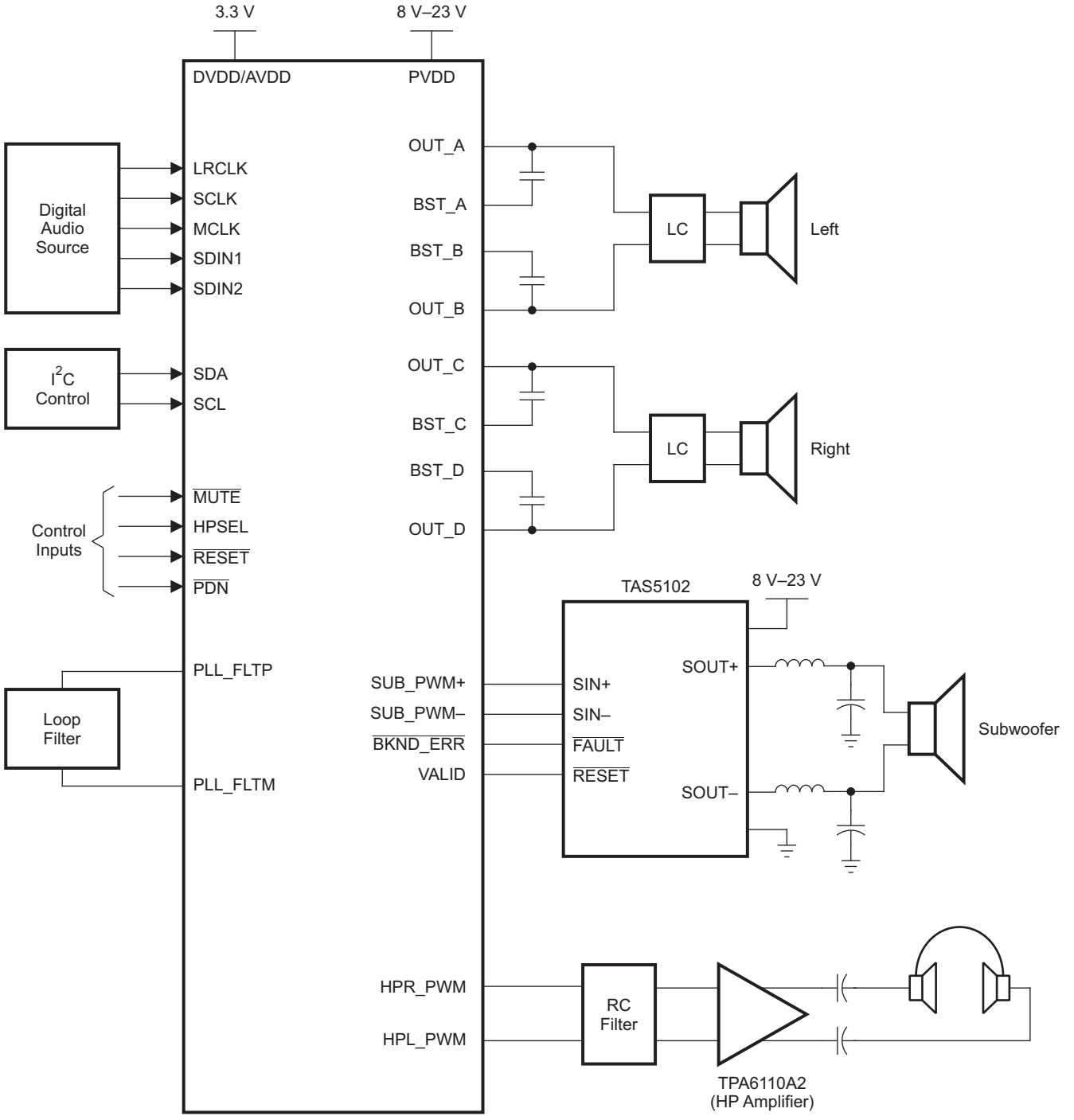
- **Audio Input/Output**
  - **20-W Into an 8-Ω Load From an 18-V Supply**
  - **Wide Power-Supply Range From (8 V to 23 V)**
  - **Efficient Class-D Operation Eliminates Need for Heat Sinks**
  - **Requires Only Two Power-Supply Rails**
  - **Two Serial Audio Inputs (Four Audio Channels)**
  - **Supports 32-kHz–192-kHz Sample Rates (LJ/RJ/I^2S)**
  - **Headphone PWM Outputs**
  - **Subwoofer PWM Outputs**
- **Audio/PWM Processing**
  - **Independent Channel Volume Controls With 24-dB to –100-dB Range**
  - **Soft Mute (50% Duty Cycle)**
  - **Programmable Dynamic Range Control**
  - **16 Adaptable Biquads for Speaker EQ**
    - **Seven Biquads for Left and Right Channels**
    - **Two Biquads for Subwoofer Channel**
  - **Adaptive Coefficients for DRC Filters**
  - **Programmable Input and Output Mixers**
  - **DC Blocking Filters**
  - **Loudness Compensation for Subwoofer**
  - **Automatic Sample Rate Detection and Coefficient Banking for DRC and EQ**
- **General Features**
  - **Serial Control Interface Operational Without MCLK**
  - **Factory-Trimmed Internal Oscillator Enables Automatic Detection of Incoming Sample Rates**
  - **Thermal and Short-Circuit Protection**
- **Benefits**
  - **EQ: Speaker Equalization Improves Audio Performance**
  - **DRC: Dynamic Range Compression. Enables Power Limiting, Speaker Protection, Easy Listening, Night-Mode Listening**
  - **Autobank Switching: Preload Coefficients for Different Sample Rates. No Need to Write Any Coefficients to the Part When Sample Rate Changes.**
  - **Autodetect: Automatically Detects Sample-Rate Changes. No Need for External Microprocessor Intervention**

DESCRIPTION

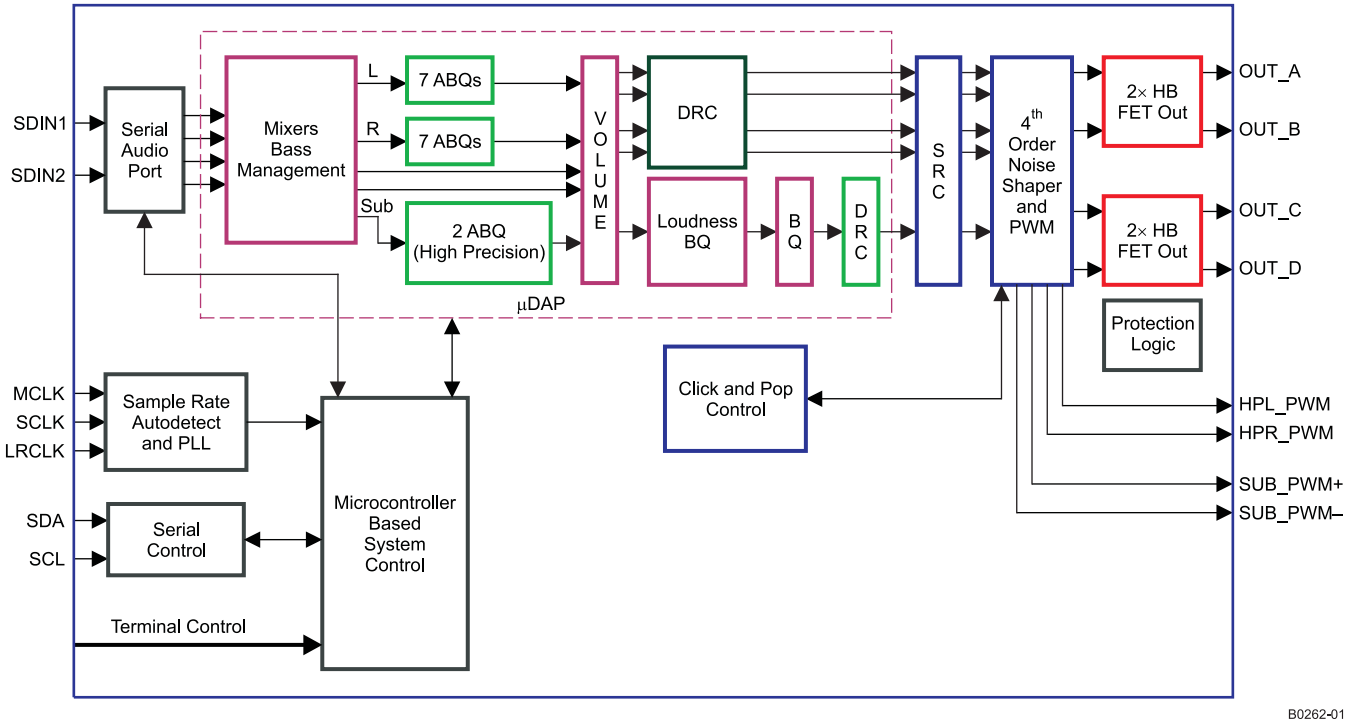
The TAS5705 is a 20-W, efficient, digital audio power amplifier for driving stereo bridge-tied speakers. Two serial data inputs allow processing of up to four discrete audio channels and seamless integration to most digital audio processors and MPEG decoders. The device accepts a wide range of input data and clock rates. A fully programmable data path allows these channels to be routed to the internal speaker drivers or output via the line-level subwoofer or headphone PWM outputs.

The TAS5705 is a slave-only device receiving clocks from external sources. The TAS5705 operates at a 384-kHz switching rate for 32-, 48-, 96-,and 192-kHz data and 352.8-kHz switching rate for 44.1-, 88.2- and 176.4-kHz data. The 8× oversampling combined with the fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

SIMPLIFIED APPLICATION DIAGRAM



FUNCTIONAL VIEW



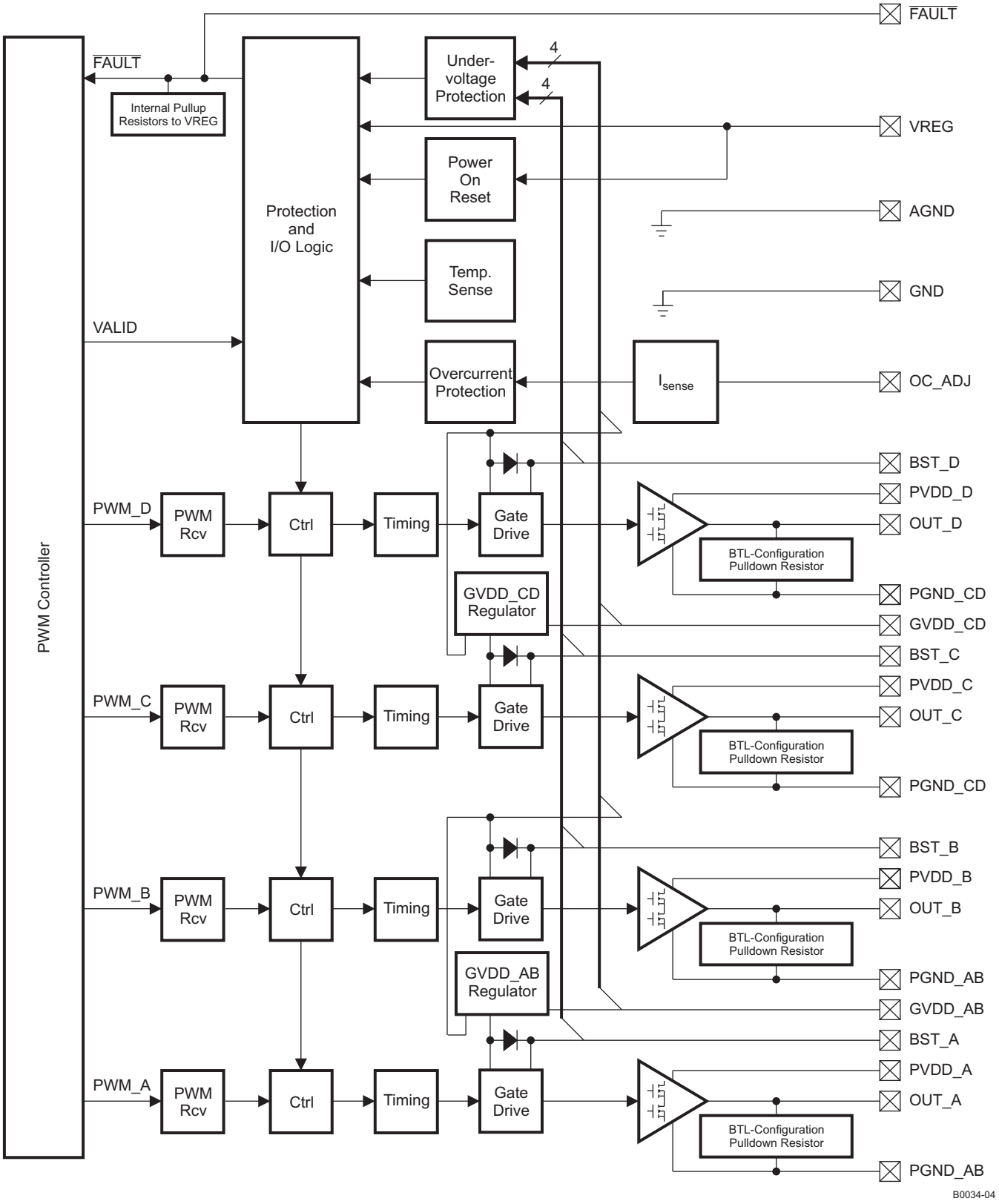
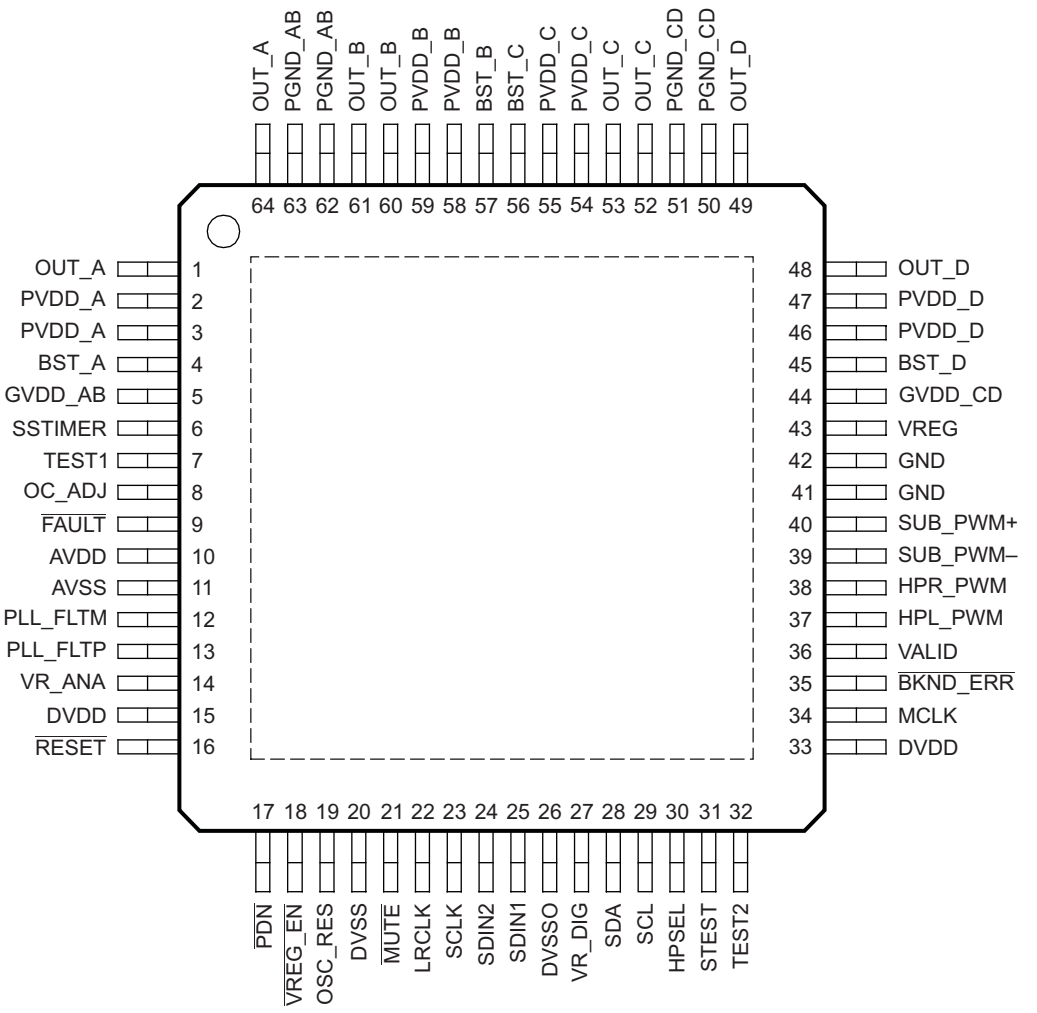


Figure 1. Power Stage Functional Block Diagram

64-PIN, HTQFP PACKAGE (TOP VIEW)

PAP Package
(Top View)



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TERMINAL FUNCTIONS

TERMINAL		TYPE (1)	5-V TOLERANT	TERMINATION (2)	DESCRIPTION
NAME	NO.				
AVDD	10	P			3.3-V analog power supply. Needs close decoupling capacitor.
AVSS	11	P			Analog 3.3-V supply ground
BKND_ERR	35	DI		Pullup	Active-low. A back-end error sequence is generated by applying logic LOW to this terminal. This pin is connected to an external power stage. If no external power stage is used, connect this pin directly to DVDD.
BST_A	4	P			High-side bootstrap supply for half-bridge A
BST_B	57	P			High-side bootstrap supply for half-bridge B
BST_C	56	P			High-side bootstrap supply for half-bridge C
BST_D	45	P			High-side bootstrap supply for half-bridge D

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2) All pullups are 20-µA *weak* pullups and all pulldowns are 20-µA *weak* pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input). Devices that drive inputs with pullups must be able to sink 50 µA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 50 µA while maintaining a logic-1 drive level.

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE (1)	5-V TOLERANT	TERMINATION (2)	DESCRIPTION
NAME	NO.				
DVDD	15, 33	P			3.3-V digital power supply
DVSS	20	P			Digital ground
DVSSO	26	P			Oscillator ground
$\overline{\text{FAULT}}$	9	DO		Pullup	Overtemperature, overcurrent, and undervoltage fault reporting. Active-low indicates fault. If high, normal operation.
GND	41, 42	P			Analog ground for power stage
GVDD_AB	5	P			Gate drive internal regulated output for AB channels
GVDD_CD	44	P			Gate drive internal regulated output for CD channels
HPL_PWM	37	DO			Headphone left-channel PWM output.
HPR_PWM	38	DO			Headphone right-channel PWM output.
HPSEL	30	DI	5-V		Headphone select, active-high. When a logic high is applied, device enters headphone mode and speakers are MUTED (HARD MUTE). When a logic LOW is applied, device is in speaker mode and headphone outputs become line outputs or are disabled. When in line out mode, this terminal functionality is disabled (see system control register 2.
LRCLK	22	DI	5-V		Input serial audio data left/right clock (sampling rate clock)
MCLK	34	DI	5-V		MCLK is the clock master input. The input frequency of this clock can range from 4.9 MHz to 49.2 MHz.
$\overline{\text{MUTE}}$	21	DI	5-V	Pullup	Performs a soft mute of outputs, active-low. A logic low on this pin sets the outputs equal to 50% duty cycle. A logic high on this pin allows normal operation. The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
OC_ADJ	8	AO			Analog overcurrent programming. Requires 22-kΩ resistor to ground.
OSC_RES	19	AO			Oscillator trim resistor. Connect an 18.2-kΩ, 1% tolerance resistor to DVSSO.
OUT_A	1, 64	O			Output, half-bridge A
OUT_B	60, 61	O			Output, half-bridge B
OUT_C	52, 53	O			Output, half-bridge C
OUT_D	48, 49	O			Output, half-bridge D
$\overline{\text{PDN}}$	17	DI	5-V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ powers down all logic, stops all clocks, and stops output switching whenever a logic low is applied. When $\overline{\text{PDN}}$ is released, the device powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration determined by register settings.
PGND_AB	62, 63	P			Power ground for half-bridges A and B
PGND_CD	50, 51	P			Power ground for half-bridges C and D
PLL_FLTM	12	AO			PLL negative loop filter terminal
PLL_FLTP	13	AI			PLL positive loop filter terminal
PVDD_A	2, 3	P			Power supply input for half-bridge output A (8 V–23 V)
PVDD_B	58, 59	P			Power supply input for half-bridge output B (8 V–23 V)
PVDD_C	54, 55	P			Power supply input for half-bridge output C (8 V–23 V)
PVDD_D	46, 47	P			Power supply input for half-bridge output D (8 V–23 V)
$\overline{\text{RESET}}$	16	DI	5-V	Pullup	Reset, active-low. A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the DAP to its default conditions, sets the VALID outputs low, and places the PWM in the hard-mute state (stops switching). Master volume is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4–5-ms device initialization and sets the volume at mute.
SCL	29	DI	5-V		I^2C serial control clock input

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE (1)	5-V TOLERANT	TERMINATION (2)	DESCRIPTION
NAME	NO.				
SCLK	23	DI	5-V		Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
SDA	28	DIO	5-V		I^2C serial control data interface input/output
SDIN1	25	DI	5-V		Serial audio data 1 input is one of the serial data input ports. SDIN1 supports three discrete (stereo) data formats.
SDIN2	24	DI	5-V		Serial audio data 2 input is one of the serial data input ports. SDIN2 supports three discrete (stereo) data formats.
SSTIMER	6	AI			Controls ramp time of OUT_X for pop-free operation. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time of PWM outputs from 0% to 50%. For 2.2 nF, start/stop time is ~10 ms.
STEST	31	DI			Test pin. Connect directly to GND.
SUB_PWM–	39	DO			Subwoofer negative PWM output
SUB_PWM+	40	DO			Subwoofer positive PWM output
TEST1	7	DI			Test pin. Connect directly to GND.
TEST2	32	DI			Test pin. Connect directly to DVDD.
VALID	36	DO			Output indicating validity of ALL PWM channels, active-high. This pin is connected to an external power stage. If no external power stage is used, leave this pin floating.
VR_ANA	14	P			Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices.
VR_DIG	27	P			Internally regulated 1.8V digital supply voltage.This terminal must not be used to power external devices.
VREG	43	P			3.3 Regulator output. Not to be used as s supply or connected to any other components other than decoupling caps. Add decoupling capacitors with pins 42 and 41.
$\overline{\text{VREG\_EN}}$	18	DI		Pulldown	Voltage regulator enable. Connect directly to GND.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage	DVDD, AVDD	–0.3 to 3.6	V
	PVDD_X	–0.3 to 30	V
Input voltage	OC_ADJ	–0.3 to 4.2	V
	3.3-V digital input	–0.5 to DVDD + 0.5	V
	5-V tolerant(2) digital input	–0.5 to DVDD + 2.5	V
OUT_x to PGND_X		32(3)	V
BST_x to PGND_X		43(3)	V
Input clamp current, I_{IK} (V_I < 0 or V_I > 1.8 V)		±20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > 1.8 V)		±20	mA
Operating free-air temperature		0 to 85	°C
Operating junction temperature range		0 to 150	°C
Storage temperature range, T_{stg}		–40 to 125	°C

(1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDA, SCL, and HPSEL.
(3) DC voltage + peak ac waveform measured at the pin should be below the allowed limit for all conditions.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
10-mm × 10-mm QFP	40 mW/°C	5 W	3.2 W	2.6 W

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
	Digital/analog supply voltage	DVDD, AVDD	3	3.3	3.6	V
	Half-bridge supply voltage	PVDD_X	8		23	V
V_{IH}	High-level input voltage	3.3-V TTL, 5-V tolerant	2		5.5	V
V_{IL}	Low-level input voltage	3.3-V TTL, 5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J	Operating junction temperature range		0		150	°C
R_L (BTL)	Load impedance	Output filter: L = 15 µH, C = 0.68 µF	6	8		Ω
R_L (SE)			3.2	4		
L_O (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition		10		µH
L_O (SE)				10		

PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MODE	VALUE	UNIT
Output sample rate 2×–1× oversampled	32–kHz data rate ±2%	12× sample rate	384	kHz
	44.1-, 88.2-, 176.4-kHz data rate ±2%	8×, 4×, and 2× sample rates	352.8	kHz
	48-, 96-, 192-kHz data rate ±2%	8×, 4×, and 2× sample rates	384	kHz

PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLKI}	Frequency, MCLK (1 / t_{cyc2})		4.9		49.2	MHz
	MCLK duty cycle		40%	50%	60%	
	MCLK minimum high time		8			ns
	MCLK minimum low time		8			ns
	LRCLK allowable drift before LRCLK reset				4	MCLKs
	External PLL filter capacitor C1	SMD 0603 Y5V		47		nF
	External PLL filter capacitor C2	SMD 0603 Y5V		4.7		nF
	External PLL filter resistor R	SMD 0603, metal film		470		Ω

ELECTRICAL CHARACTERISTICS

DC Characteristics

T_A = 25°, PVCC_X = 18 V, DVDD = AVDD = 3.3 V, R_L= 8 Ω, BTL mode (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL and 5-V tolerant (1)	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	3.3-V TTL and 5-V tolerant (1)	I_{OL} = 4 mA			0.5	V
I_{IL} (2)	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			±2	µA
		5-V tolerant (1)	V_I = 0 V, DVDD = 3 V			±2	
I_{IH} (2)	High-level input current	3.3-V TTL	$V_I = V_{IH}$			±2	µA
		5-V tolerant	V_I = 5.5 V, DVDD = 3 V			±20	
I_{DD}	Digital supply current	Digital supply voltage (DVDD, AVDD)	Normal Mode		65	83	mA
			Power down ($\overline{PDN}$ = low)		8	23	
			Reset ($\overline{RESET}$ = low)		23	38.5	
I_{PVDD}	Analog supply current	No load (all PVDD inputs)			30	60	mA
$I_{PVDD}(\overline{PDN})$	Power-down current	No load (all PVDD inputs)	Power down ($\overline{PDN}$ = low)		5	6.3	
$I_{PVDD}(\overline{RESET})$	Reset current	No load (all PVDD inputs)	Reset ($\overline{RESET}$ = low)		5	6.3	
$r_{DS(on)}$	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance			180		mΩ
	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance			180		
I/O Protection							
V_{uvp}	Undervoltage protection limit	PVDD falling			7.2		V
$V_{uvp,hyst}$	Undervoltage protection limit	PVDD rising			7.6		V
OTE (3)	Overtemperature error				150		°C
OTE_{HYST} (3)	Extra temperature drop required to recover from error				30		°C
OLPC	Overload protection counter	f_{PWM} = 384 kHz			0.63		ms
I_{OC}	Overcurrent limit protection	Resistor—programmable, max. current, R_{OCP} = 22 kΩ			4.5		A
I_{OCT}	Overcurrent response time				150		ns
R_{OCP}	OC programming resistor range	Resistor tolerance = 5% for typical value; the minimum resistance should not be less than 20 kΩ. This value is not adjustable. It must be fixed at 22 kΩ.		20	22		kΩ
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap capacitor charge.			3		kΩ

(1) 5-V tolerant inputs are $\overline{PDN}$, $\overline{RESET}$, $\overline{MUTE}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDA, SCL, and HPSEL.
(2) I_{IL} or I_{IH} for pins with internal pullup can go up to 50 µA.
(3) Specified by design

AC Characteristics (BTL)

PVDD_X = 18 V, BTL mode, R_L = 8 Ω, R_{OC} = 22 KΩ, C_{BST} = 33 nF, audio frequency = 1 kHz, AES17 filter, f_{PWM} = 384 kHz, T_A = 25°C (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 18 V,10% THD, 1-kHz input signal		20.0		W
		PVDD = 18 V, 7% THD, 1-kHz input signal		18.6		
		PVDD = 12 V, 10% THD, 1-kHz input signal		9		
		PVDD = 12 V, 7% THD, 1-kHz input signal		8.3		
		PVDD = 8 V, 10% THD, 1-kHz input signal		3.9		
		PVDD = 8 V, 7% THD, 1-kHz input signal		3.7		
THD+N	Total harmonic distortion + noise	PVDD = 18 V; P_O = 10 W (half-power)		0.12%		
		PVDD = 12 V; P_O = 4.5 W (half-power)		0.1%		
		PVDD = 8 V; P_O = 2 W (half-power)		0.24%		
V_n	Output integrated noise	A-weighted		50		µV
	Crosstalk	P_O = 1 W, f = 1kHz		–73		dB
SNR	Signal-to-noise ratio (1)	A-weighted, f = 1 kHz, maximum power at THD < 0.1%		105		dB
P_D	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0 W, 4 channels switching (2)		0.6		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AC Characteristics (Single-Ended Output)

PVDD_X = 18 V, SE mode, R_L = 4 Ω, R_{OC} = 22 kΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, f_{PWM} = 384 kHz, ambient temperature = 25°C (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 18 V, 10% THD		10		W
		PVDD = 18 V, 7% THD		9		
		PVDD = 12 V, 10% THD		4.5		
		PVDD = 12 V, 7% THD		4		
THD+N	Total harmonic distortion + noise	PVDD = 18V, Po =5 W (half-power)		0.2		%
		PVDD = 12V, Po =2.25 W (half-power)		0.2		
V_n	Output integrated noise	A-weighted		50		µV
SNR	Signal-to-noise ratio (1)	A-weighted		105		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5086 modulator		105		dB
P_D	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, 4 channels switching (2)		0.6		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

SERIAL AUDIO PORTS SLAVE MODE

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, SCLK 32 × f_S, 48 × f_S, 64 × f_S	C_L = 30 pF	1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		32		64	SCLK edges
$t_{(edge)}$	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period

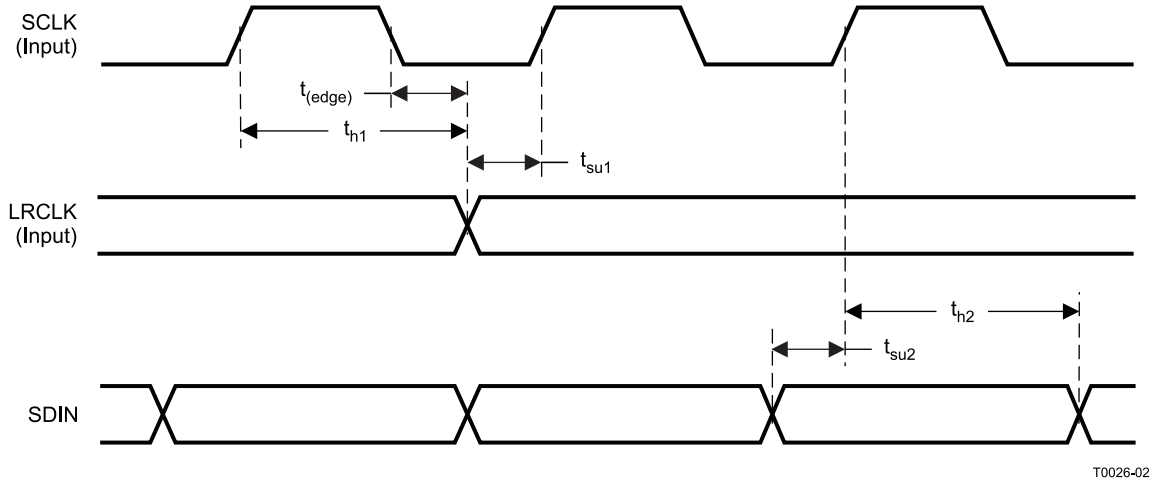


Figure 2. Slave Mode Serial Data Interface Timing

I²C SERIAL CONTROL PORT OPERATION

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states		400	kHz
$t_{w(H)}$	Pulse duration, SCL high		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low		1.3		µs
t_r	Rise time, SCL and SDA			300	ns
t_f	Fall time, SCL and SDA			300	ns
t_{su1}	Setup time, SDA to SCL		100		ns
t_{h1}	Hold time, SCL to SDA		0		ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3		µs
t_{su2}	Setup time, SCL to start condition		0.6		µs
t_{h2}	Hold time, start condition to SCL		0.6		µs
t_{su3}	Setup time, SCL to stop condition		0.6		µs
C_L	Load capacitance for each bus line			400	pF

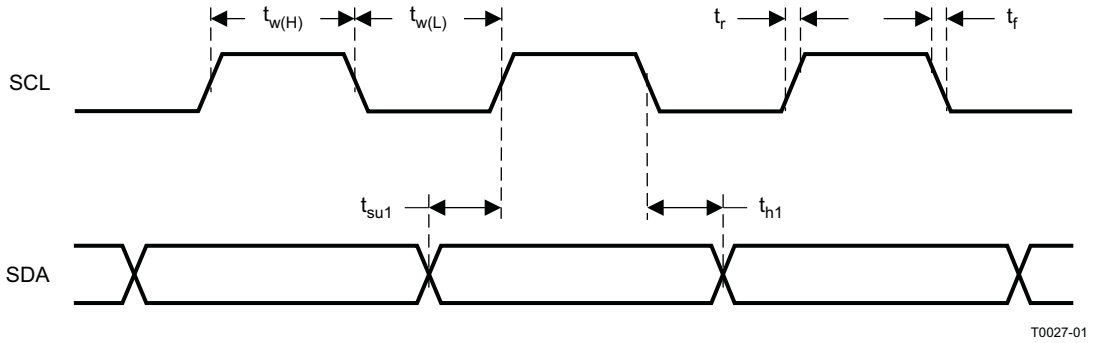


Figure 3. SCL and SDA Timing

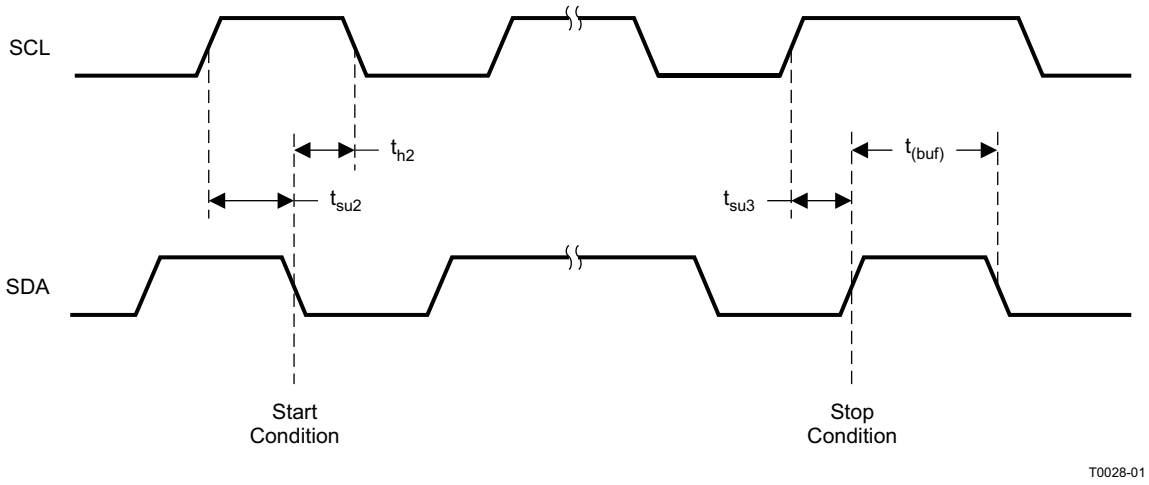
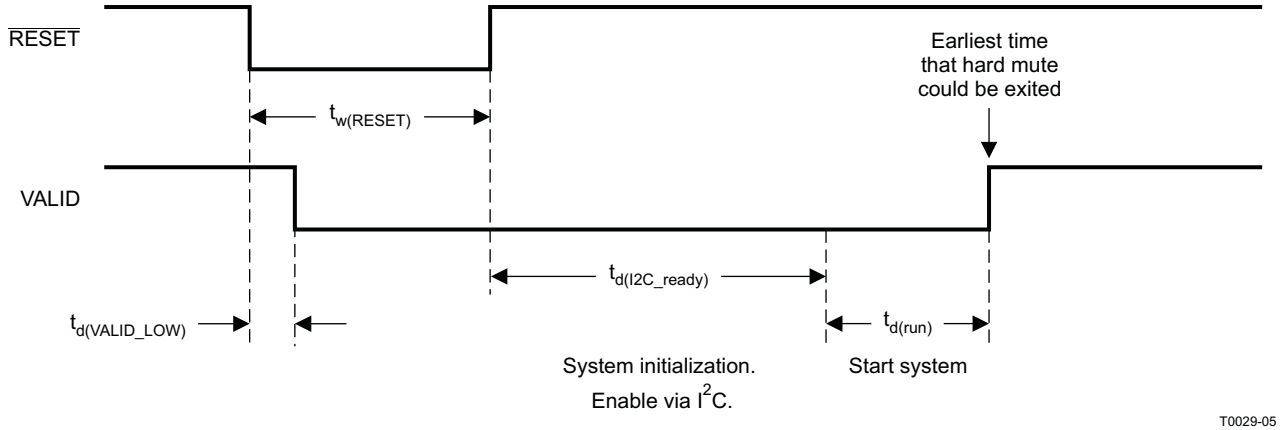


Figure 4. Start and Stop Conditions Timing

RESET TIMING ($\overline{\text{RESET}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VALID\_LOW)}$	Time to assert VALID (reset to power stage) low		100		ns
$t_{w(RESET)}$	Pulse duration, $\overline{\text{RESET}}$ active	100	200		ns
$t_{d(I2C\_ready)}$	Time to enable I^2C		3.5		ms
$t_{d(run)}$	Device start-up time (after start-up command via I^2C)	10			ms



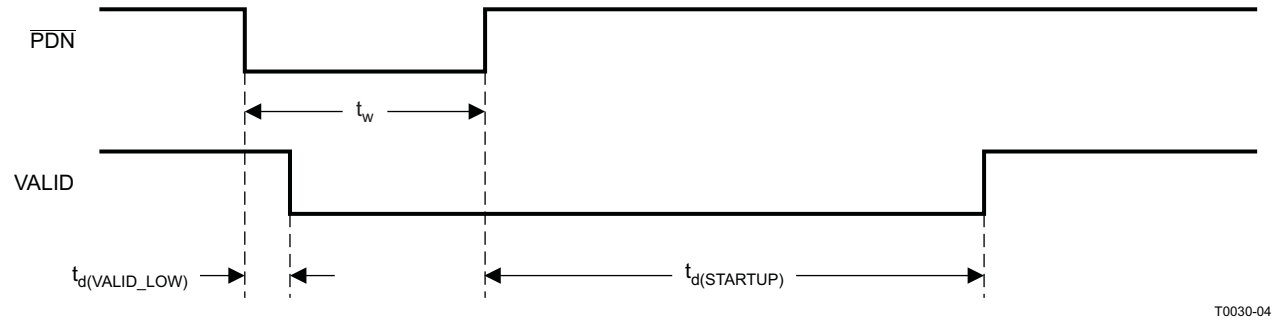
NOTE: On power up, it is recommended that the TAS5705 $\overline{\text{RESET}}$ be held LOW for at least 100 µs after DVDD has reached 3.0 V. RESET assertion is ignored if applied while part is powered down

Figure 5. Reset Timing

POWER-DOWN ($\overline{\text{PDN}}$) TIMING

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VALID\_LOW)}$	Time to assert VALID (reset to power stage) low		725		µs
$t_{d(STARTUP)}$	Device startup time			650	µs
t_w	Minimum pulse duration required	1			µs



NOTE: PDNZ assertion is ignored if applied when part is in RESET

Figure 6. Power-Down Timing

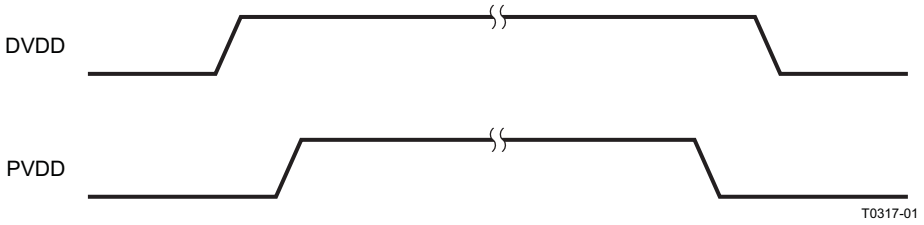
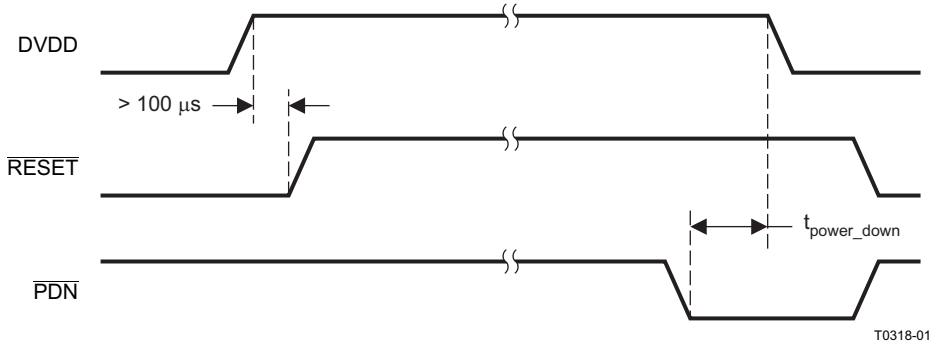


Figure 7. Power Up and Power Down of Power Supplies



NOTE: t_{power_down} = time to wait before powering down the supplies after $\overline{PDN}$ assertion = 725 µs + power-stage stop time defined by register 0x1A

Figure 8. Terminal Control and DVDD

BACK-END ERROR ($\overline{\text{BKND\_ERR}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(ER)}$	Minimum pulse duration, $\overline{\text{BKND\_ERR}}$ active (active-low)	350			ns
$t_{p(valid\_high)}$	Programmable. Time to stay in the VALID (reset to the power stage) low state. After $t_{p(valid\_high)}$, the TAS5705 attempts to bring the system out of the VALID low state if $\overline{\text{BKND\_ERR}}$ is high.		300		ms
$t_{p(valid\_low)}$	Time TAS5705 takes to bring VALID (reset to the power stage) low after $\overline{\text{BKND\_ERR}}$ assertion.		400		ns

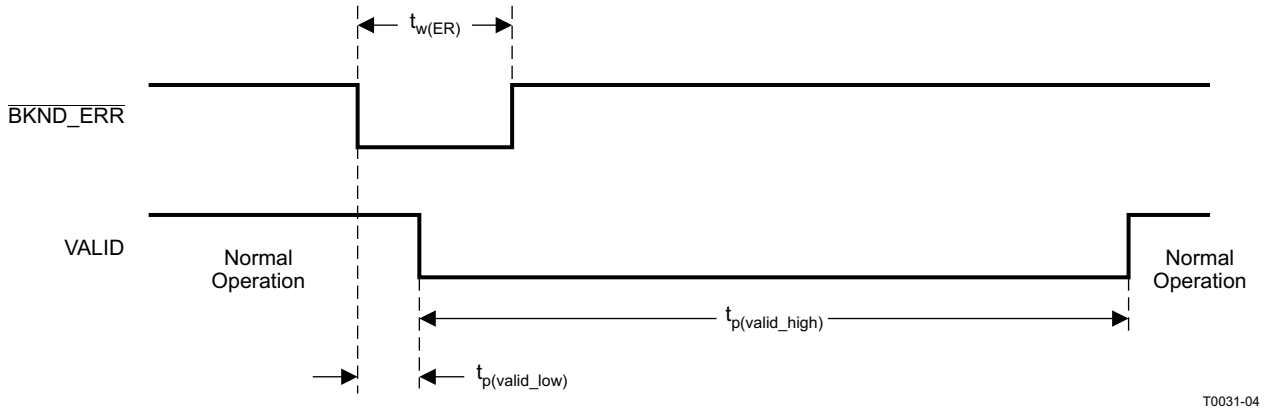


Figure 9. Error Recovery Timing

MUTE TIMING ($\overline{\text{MUTE}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VOL)}$	Volume ramp time (= number of steps × step size). Number of steps is defined by volume configuration register 0x0E (see *Volume Configuration Register*). Step size = 4 LRCLKs if $f_S \le 48$ kHz; else 8 LRCLKs if $f_S \le 96$ kHz ; else 16 LRCLKs		1024		steps

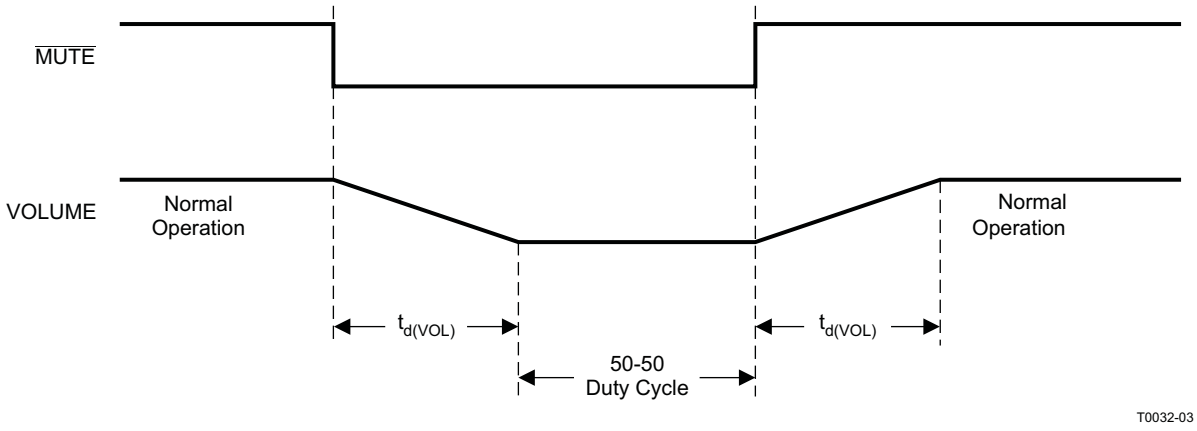


Figure 10. Mute Timing

HEADPHONE SELECT (HPSEL)

PARAMETER		MIN	MAX	UNIT
$t_{w(MUTE)}$	Pulse duration, HPSEL active	350		ns
$t_{d(VOL)}$	Soft volume update time	See (1)		ms
$t_{(SW)}$	Switch-over time (controlled by start/stop period register, 0x1A)	0.2		ms

(1) Defined by the volume slew rate setting (see the volume configuration register, 0x0E).

Figure 11 and Figure 12 show functionality when bit 4 in the HP configuration register is set to DISABLE (not in line-out mode). See register 0x05 for details. If bit 4 is not set, than the HP PWM outputs are not disabled when HPSEL is brought low.

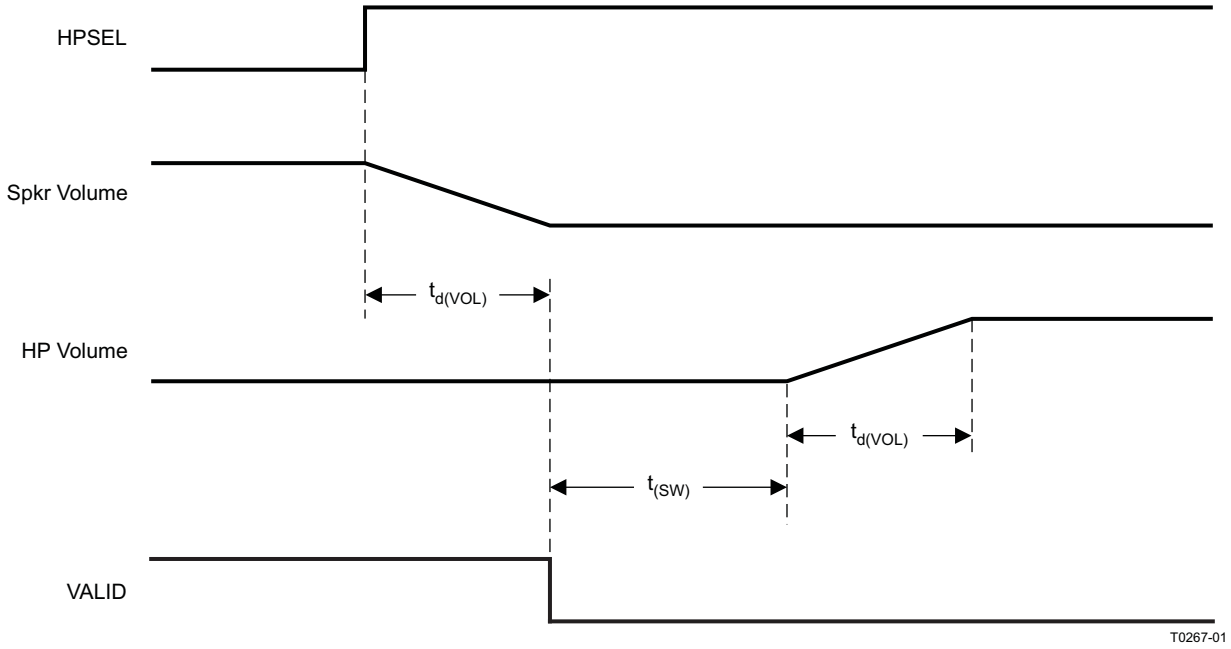


Figure 11. HPSEL Timing for Headphone Insertion

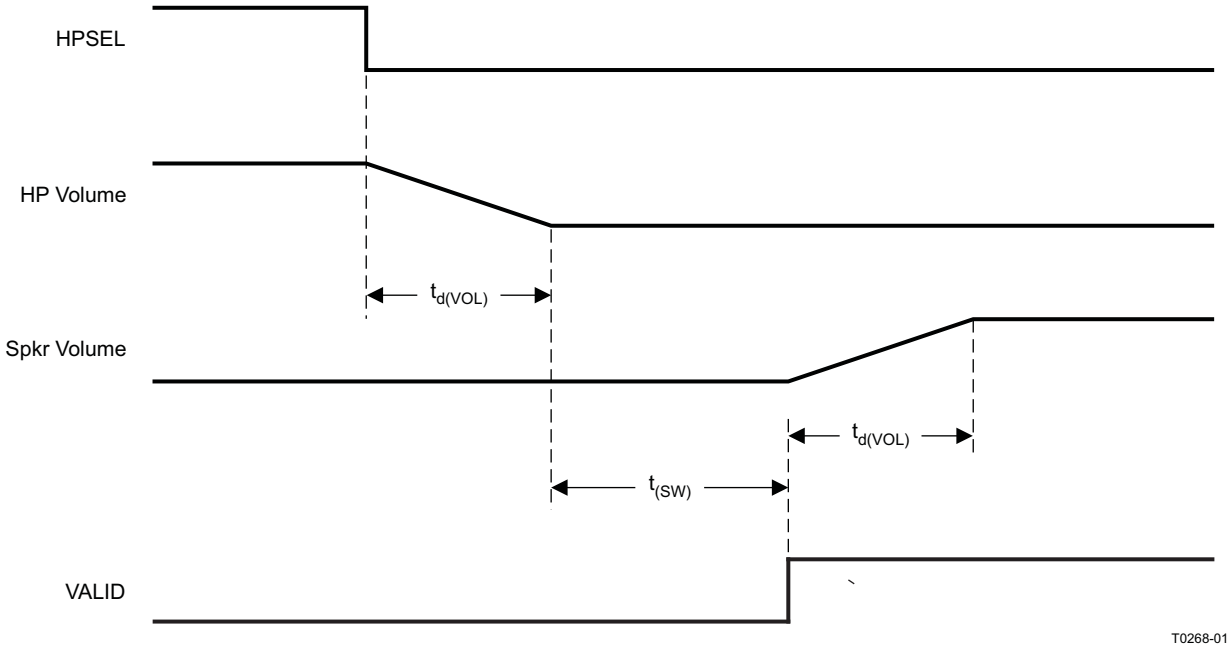


Figure 12. HPSEL Timing for Headphone Extraction

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

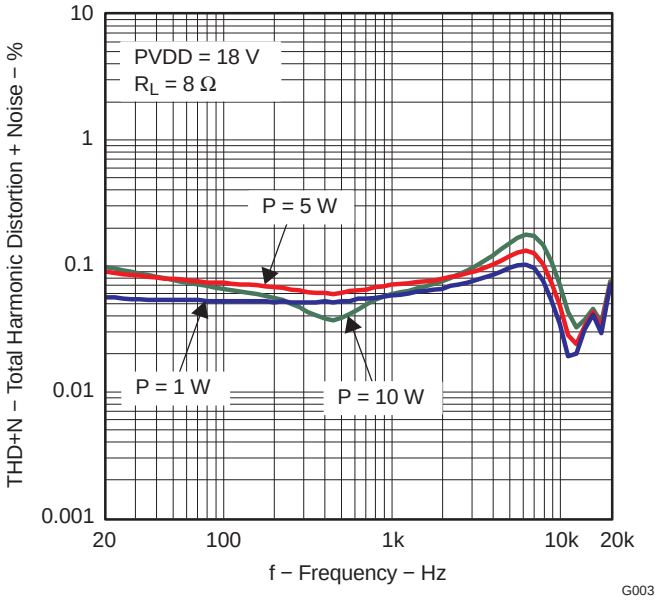


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

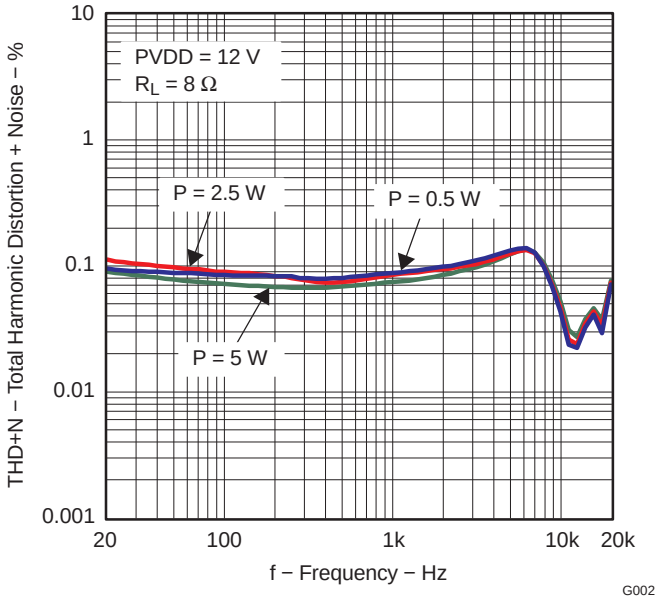


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

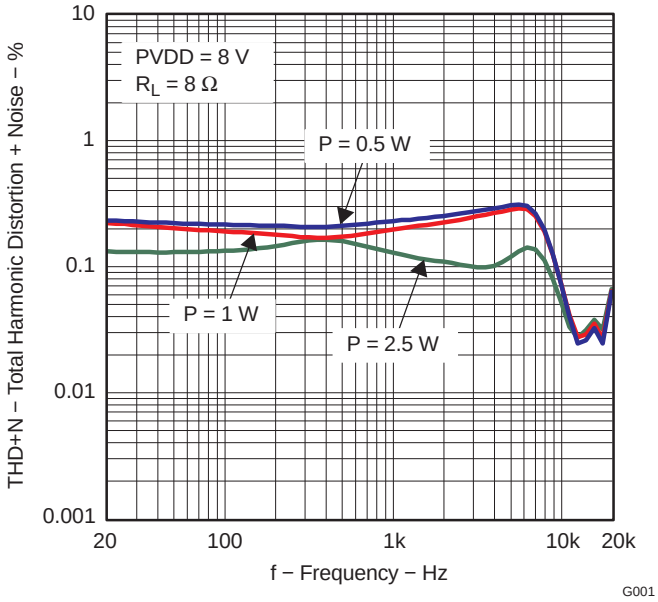


Figure 15.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

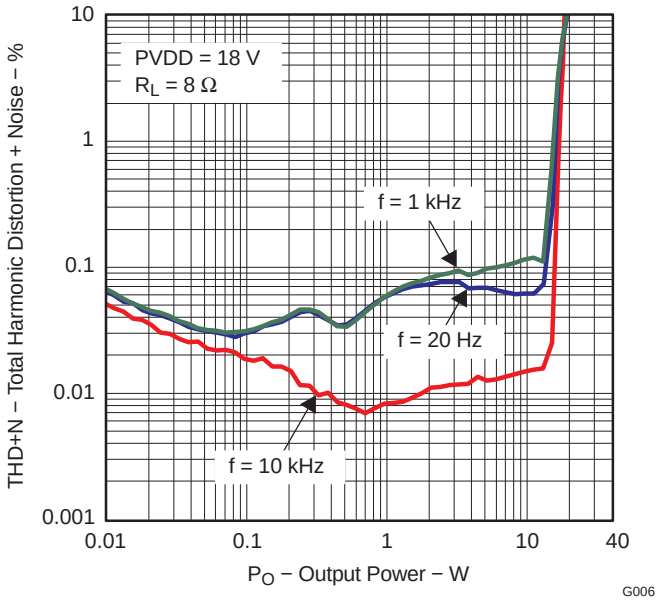


Figure 16.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

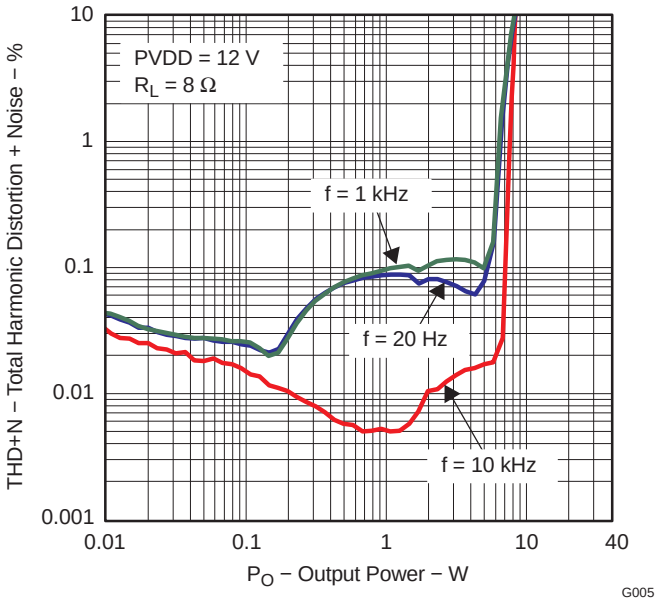


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

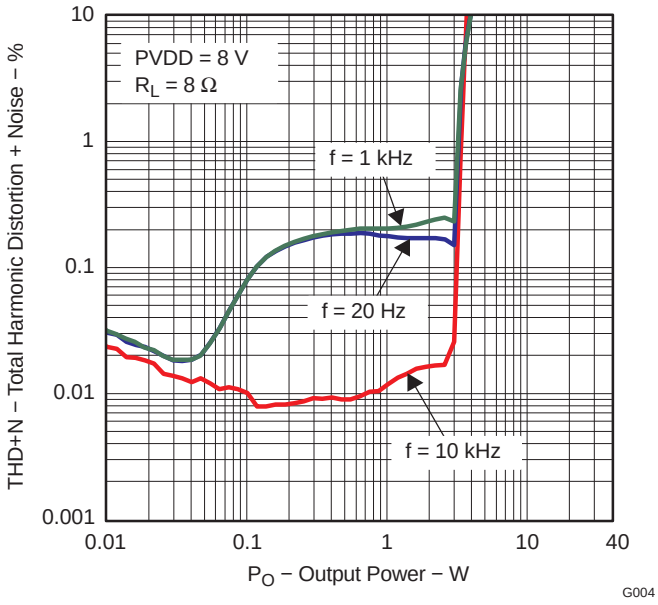


Figure 18.

EFFICIENCY vs OUTPUT POWER

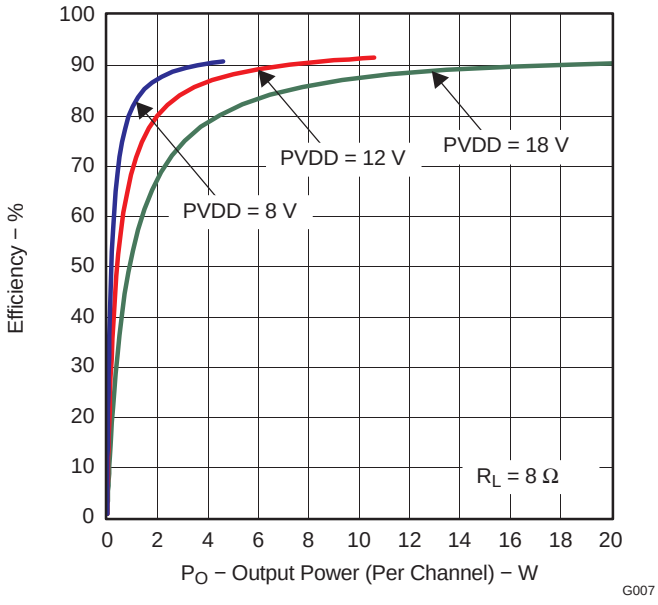


Figure 19.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

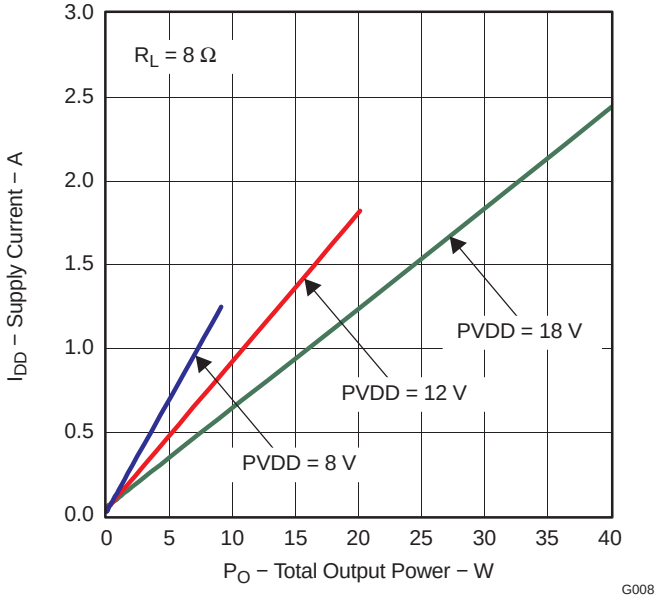


Figure 20.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

OUTPUT POWER vs SUPPLY VOLTAGE

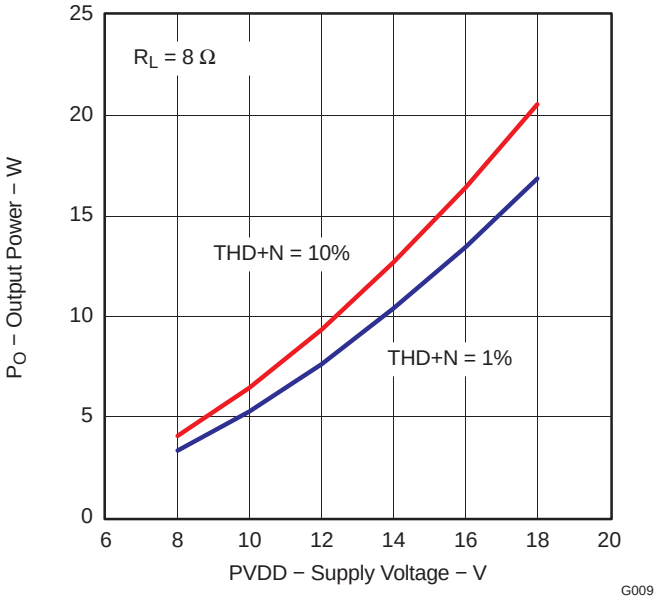


Figure 21.

CROSSTALK vs FREQUENCY

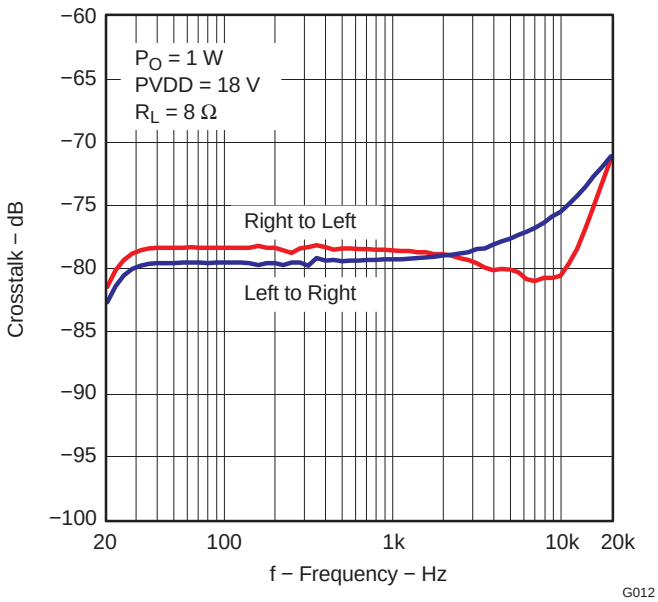


Figure 22.

TYPICAL CHARACTERISTICS, SE CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

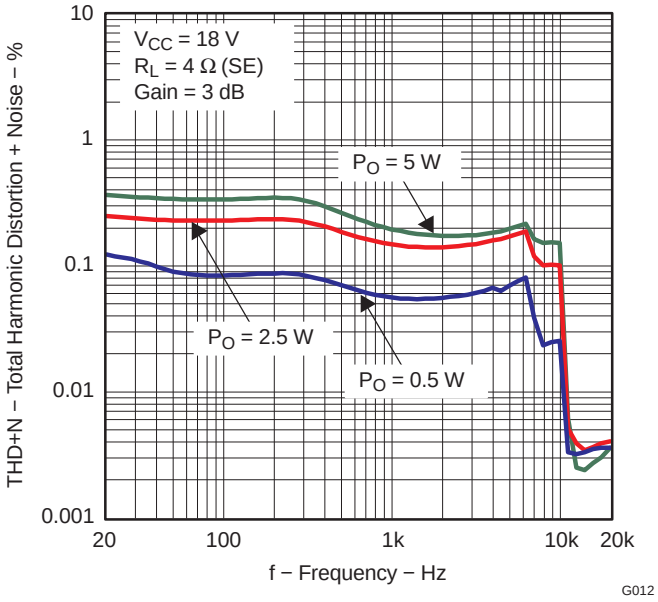


Figure 23.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

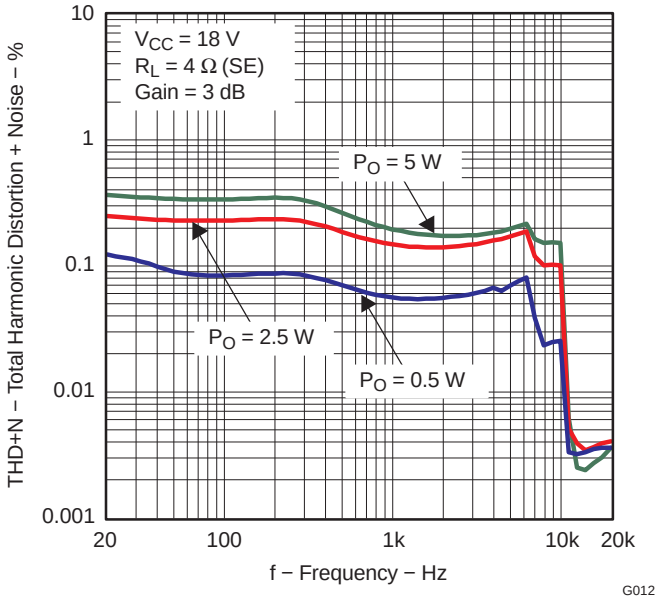


Figure 24.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

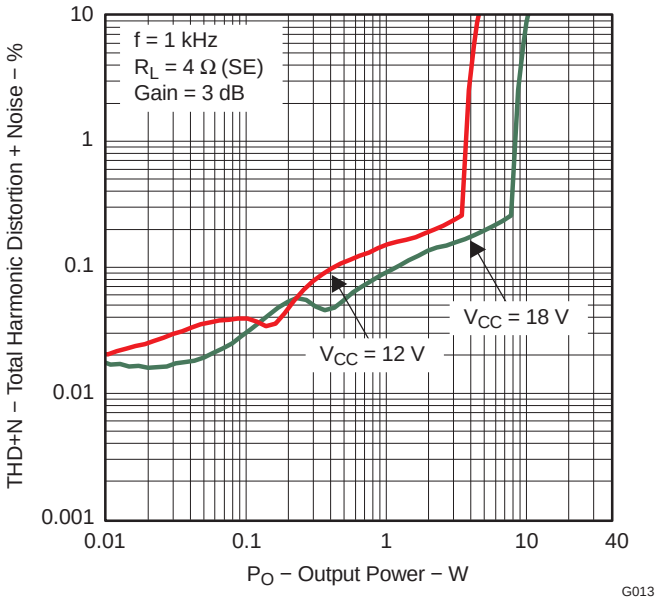


Figure 25.

OUTPUT POWER vs SUPPLY VOLTAGE

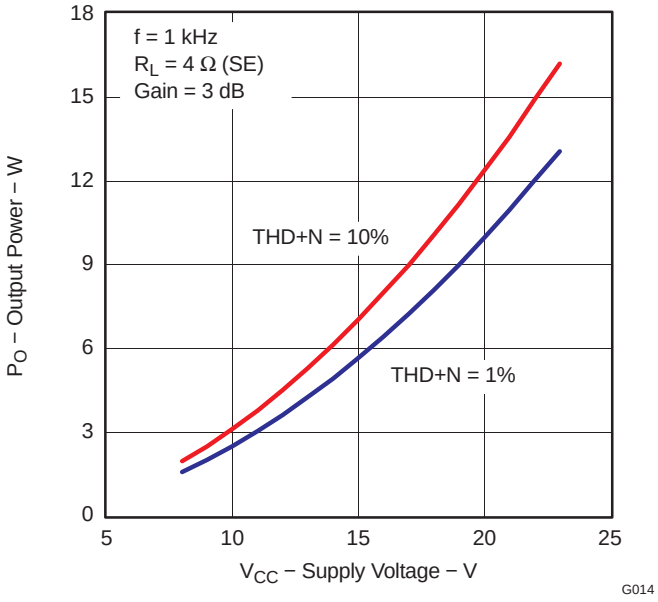


Figure 26.

DETAILED DESCRIPTION

POWER SUPPLY

To facilitate system design, the TAS5705 needs only a 3.3-V digital supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). The gate drive voltages (GVDD_AB and GVDD_CD) are derived from the PVDD voltage. Separate, internal voltage regulators reduce and regulate the PVDD voltage to a voltage appropriate for efficient gave drive operation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin.

The TAS5705 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The outputs of the H-bridges remain in a low-impedance state until the internal gate-drive supply voltage (GVDD_XY) and external VREG voltages are above the undervoltage protection (UVP) voltage threshold (see the *DC Characteristics* section of this data sheet). It is recommended to hold PVDD_X low until DVDD (3.3 V) is powered up while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output. The output impedance is approximately 3 kΩ. This means that the TAS5705 should be held in reset for at least 100 µs to ensure that the bootstrap capacitors are charged. This also assumes that the recommended 0.033-µF bootstrap capacitors are used. Changes to bootstrap capacitor values change the bootstrap capacitor charge time. See Figure 7 and Figure 8.

Powering Down

Apply $\overline{\text{PDN}}$ (assert low). Wait for the power stage to shut down. Power down PVDD. Then power down DVDD. Then de-assert $\overline{\text{PDN}}$. See Figure 8 for recommended timing.

ERROR REPORTING

The $\overline{\text{FAULT}}$ pin is an active-low, open-drain output. Its function is for protection-mode signaling to a system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low (see Table 1).

Table 1. $\overline{\text{FAULT}}$ Output States

$\overline{\text{FAULT}}$	DESCRIPTION
0	Overcurrent (OC) or undervoltage (UVP) warning or overtemperature error (OTE)
1	Junction temperature lower than 150°C and no faults (normal operation)

Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present.

To reduce external component count, an internal pullup resistor to 3.3 V is provided on the $\overline{\text{FAULT}}$ output. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5705 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overtemperature, and undervoltage. The TAS5705 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. The device automatically recovers when the fault condition has been removed.

Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current further increasing, i.e., it performs a cycle-by-cycle current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current condition situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device returns to normal operation once the fault condition (i.e., a short circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

The overcurrent protection threshold is set by a resistor to ground from the OC_ADJ pin. A value of 22 kΩ will result in an overcurrent threshold of 4.5 A. This resistor value should not be changed.

Overtemperature Protection

The TAS5705 has a two-level temperature-protection system that asserts an active-high warning signal (OTW) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5705 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_XY and VREG supply voltages reach 5.7 V (typical) and 2.7 V, respectively. Although GVDD_XY and VREG are independently monitored, a supply voltage drop below the UVP threshold on VREG or either GVDD_XY pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

One reset pin is provided for control of half-bridges A/B/C/D. When $\overline{\text{RESET}}$ is asserted low, all four power-stage FETs in half-bridges A, B, C, and D are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the weak pulldowns are not enabled, and it is therefore recommended to ensure bootstrap capacitor charging by providing a low pulse on the PWM inputs when reset is asserted high.

Asserting the reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, i.e., $\overline{\text{FAULT}}$ is forced high.

A rising-edge transition on the reset input allows the device to resume operation after an overcurrent fault.

SSTIMER FUNCTIONALITY

The SSTIMER pin uses a capacitor connected between this pin and ground to control the output duty cycle when a transition occurs on the $\overline{\text{RESET}}$ pin. The capacitor on the SSTIMER pin is slowly charged through an internal current source, and the charge time determines the rate at which the output transitions from a near zero duty cycle to the duty cycle that is present on the inputs. This allows for a smooth transition with no audible *pop* or *click* noises when the $\overline{\text{RESET}}$ pin transitions from high-to-low or low-to-high.

For a high-to-low transition of the $\overline{\text{RESET}}$ pin (shutdown case), it is important for the modulator to remain switching for a period of at least 10 ms (if using a 2.2 nF capacitor). Larger capacitors will increase the start-up/shutdown time, while capacitors smaller than 2.2 nF will decrease the start-up/shutdown time. The inputs MUST remain switching on the shutdown transition to allow the outputs to slowly ramp down the duty cycle to near zero before completely shutting off. The SSTIMER pin should be left floating for BD modulation and also for SE (single-ended) mode.

CLOCK, AUTODETECTION, AND PLL

The TAS5705 DAP is a slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the clock control register .

The TAS5705 checks to verify that SCLK is a specific value of 32 f_S, 48 f_S, or 64 f_S. The DAP only supports a 1 × f_S LRCLK. The timing relationship of these clocks to SDIN1/2 is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to produce the internal clock.

The DAP can autodetect and set the internal clock-control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz or 192 kHz). The automatic sample-rate detection can be disabled and the values set via I^2C in the clock control register.

The DAP also supports an AM interference-avoidance mode during which the clock rate is adjusted, in concert with the PWM sample rate converter, to produce a PWM output at 7 × f_S, 8 × f_S, or 6 × f_S.

The sample rate must be set manually during AM interference avoidance and when de-emphasis is enabled.

SERIAL DATA INTERFACE

Serial data is input on SDIN1/2. The PWM outputs are derived from SDIN1/2. The TAS5705 DAP accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 18-, 20-, or 24-bit data in left-justified, right-justified, and I^2S serial data formats.

PWM Section

The TAS5705 DAP device uses noise-shaping and sophisticated error-correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper that has >100-dB SNR performance from 20 Hz to 20 kHz. The PWM section accepts 24-bit PCM data from the DAP and outputs four PWM audio output channels. The TAS5705 PWM SECTION supports bridge-tied loads.

The PWM section has individual-channel dc-blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual-channel de-emphasis filters for 32-, 44.1-, and 48-kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

I²C-COMPATIBLE SERIAL CONTROL INTERFACE

The TAS5705 DAP has an I²C serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100-kHz) and high-speed (400-kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

The serial control interface supports both single-byte and multibyte read and write operations for status registers and the general control registers associated with the PWM.

The I²C interface supports a special mode which permits I²C write operations to be broken up into multiple data-write operations that are multiples of 4 data bytes. These are 6-, 10-, 14-, 18-, ... etc., -byte write operations that are composed of a device address, read/write bit, subaddress, and any multiple of 4 bytes of data. This permits the system to write large register values incrementally without blocking other I²C transactions.

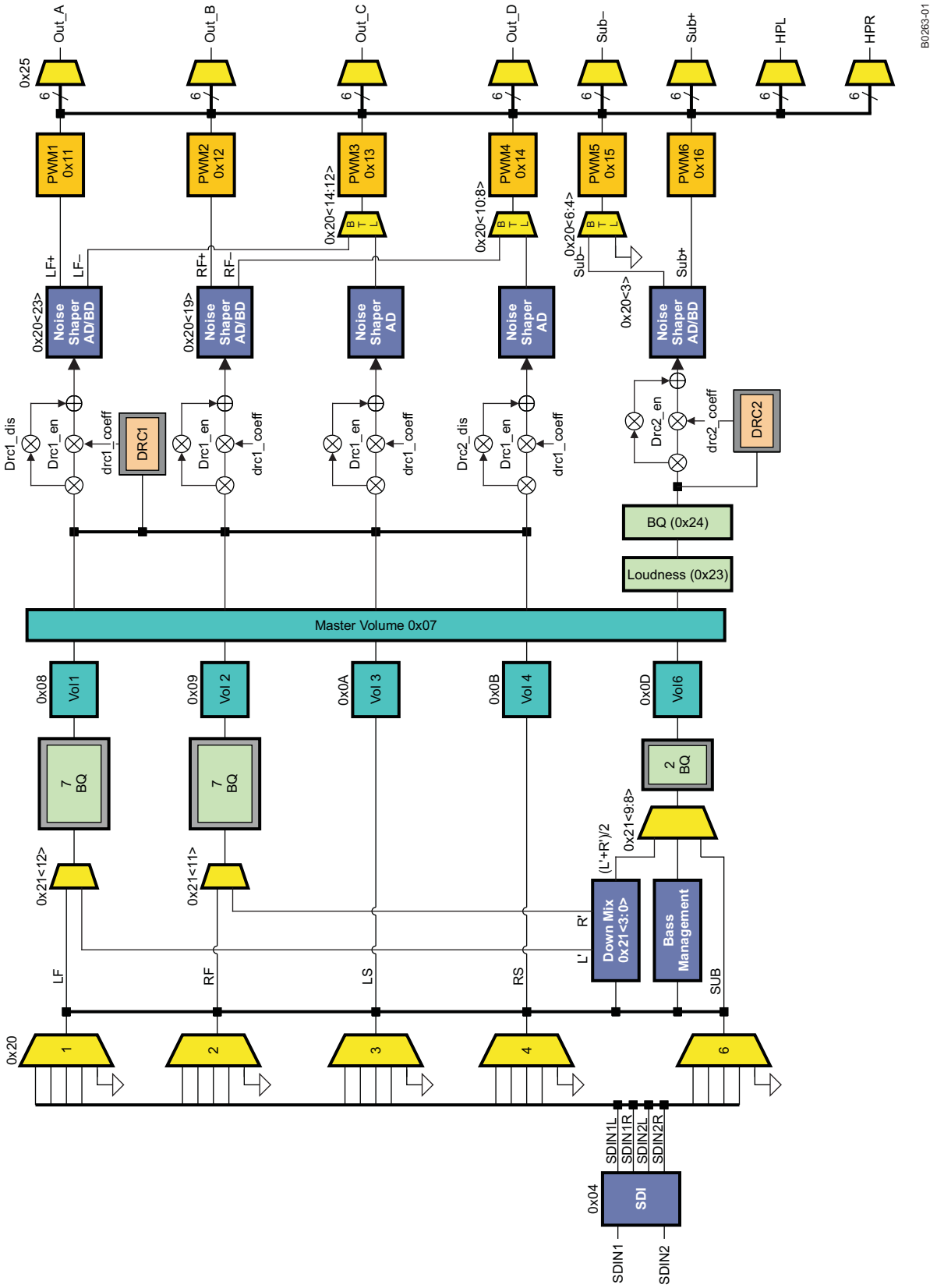


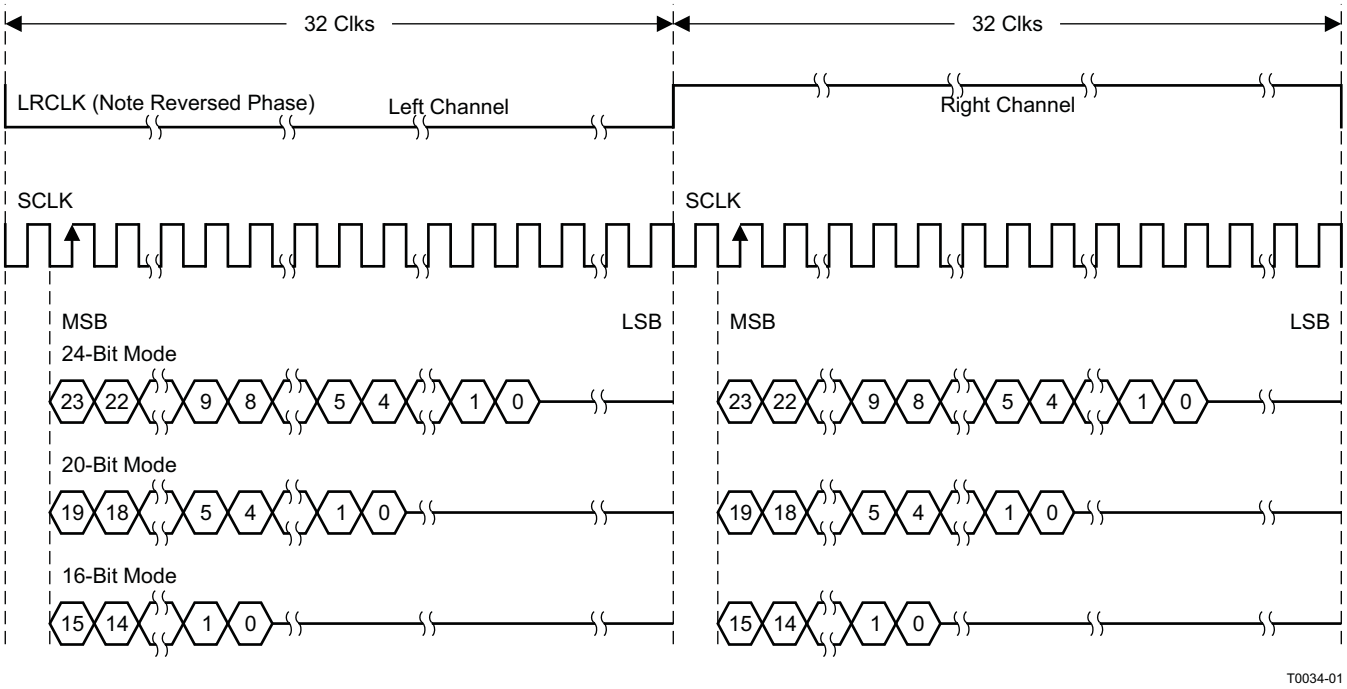
Figure 27. TAS5705 DAP Data Flow Diagram With I²C Registers

SERIAL INTERFACE CONTROL AND TIMING

I²S Timing

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data-bit positions.

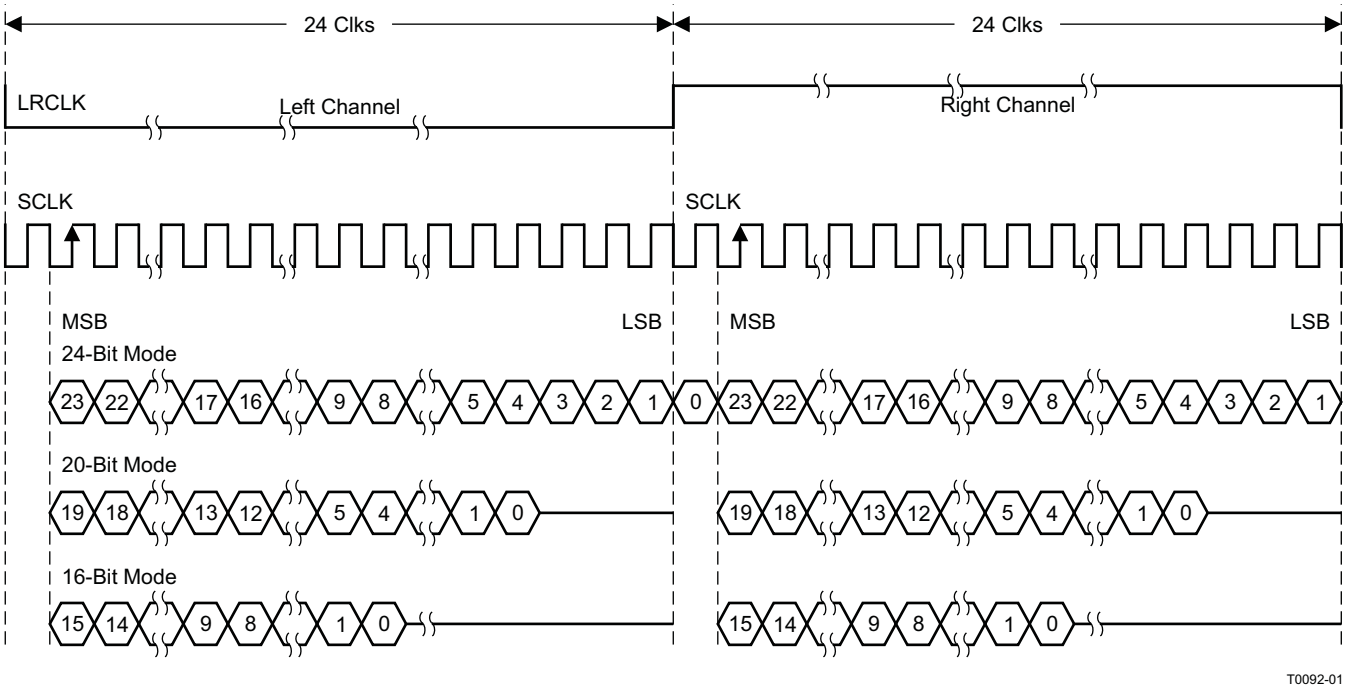
2-Channel I²S (Philips Format) Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 28. I²S 64-f_S Format

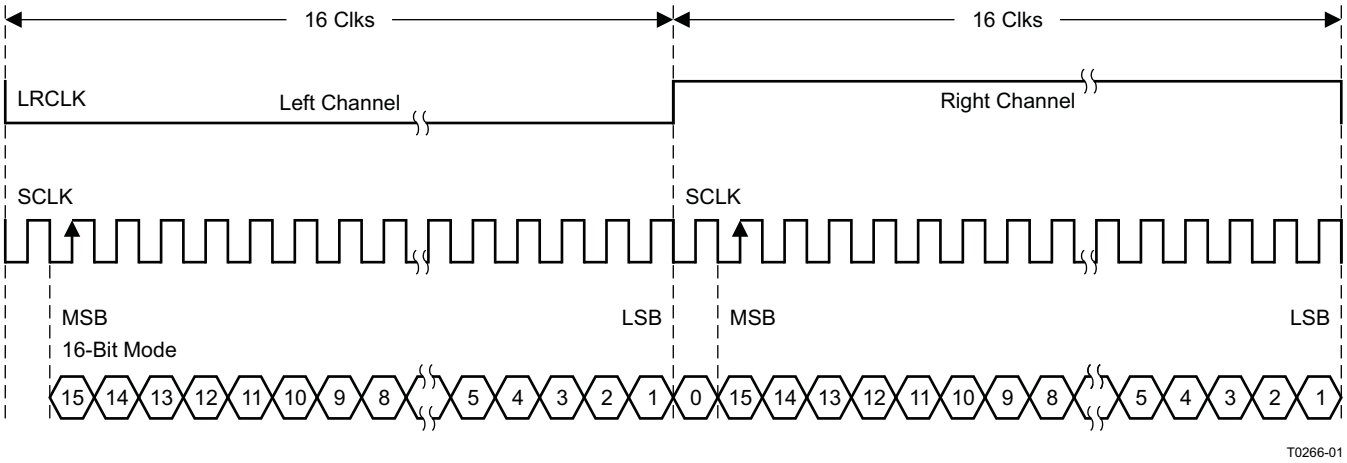
2-Channel I^2S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)



NOTE: All data presented in 2s-complement form with MSB first.

Figure 29. I^2S 48-f_S Format

2-Channel I^2S (Philips Format) Stereo Input

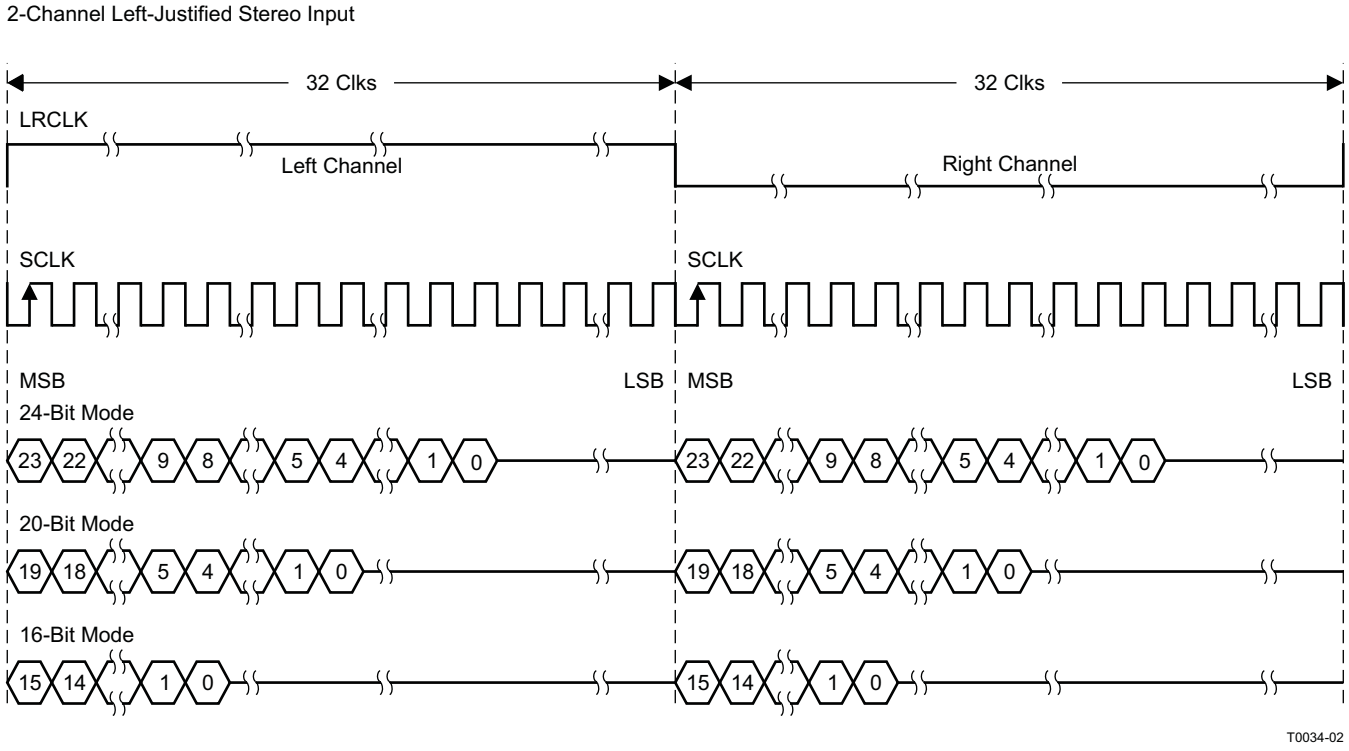


NOTE: All data presented in 2s-complement form with MSB first.

Figure 30. I^2S 32-f_S Format

Left-Justified

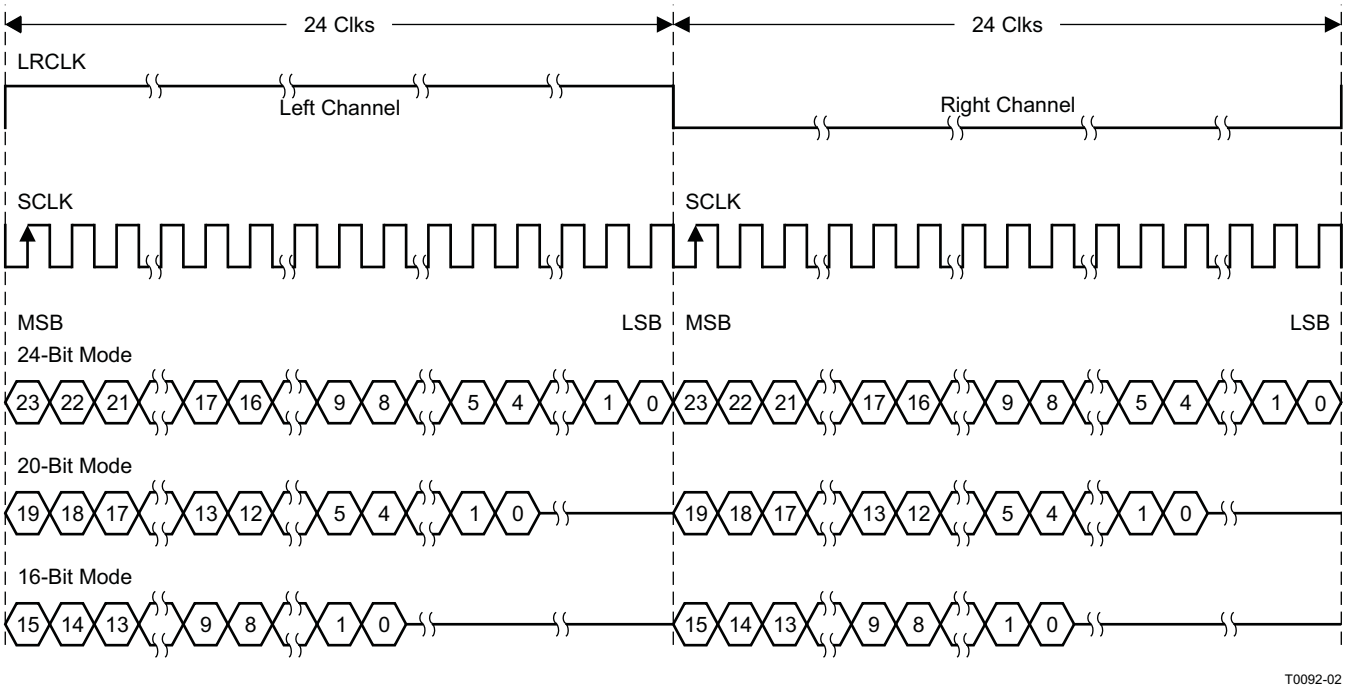
Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data-bit positions.



NOTE: All data presented in 2s-complement form with MSB first.

Figure 31. Left-Justified 64-f_S Format

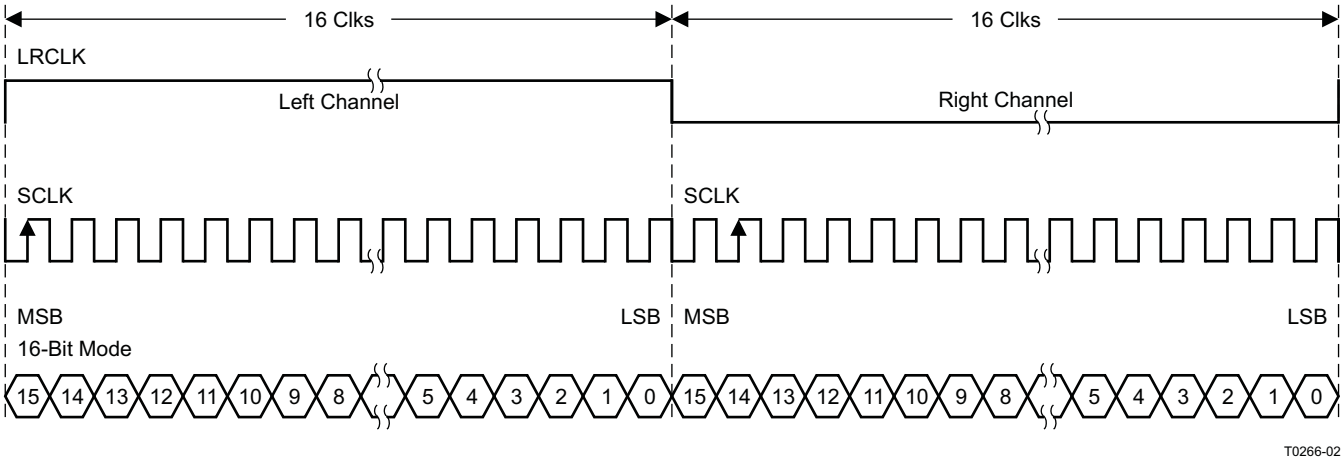
2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)



NOTE: All data presented in 2s-complement form with MSB first.

Figure 32. Left-Justified 48-f_S Format

2-Channel Left-Justified Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 33. Left-Justified 32-f_S Format

Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data line 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

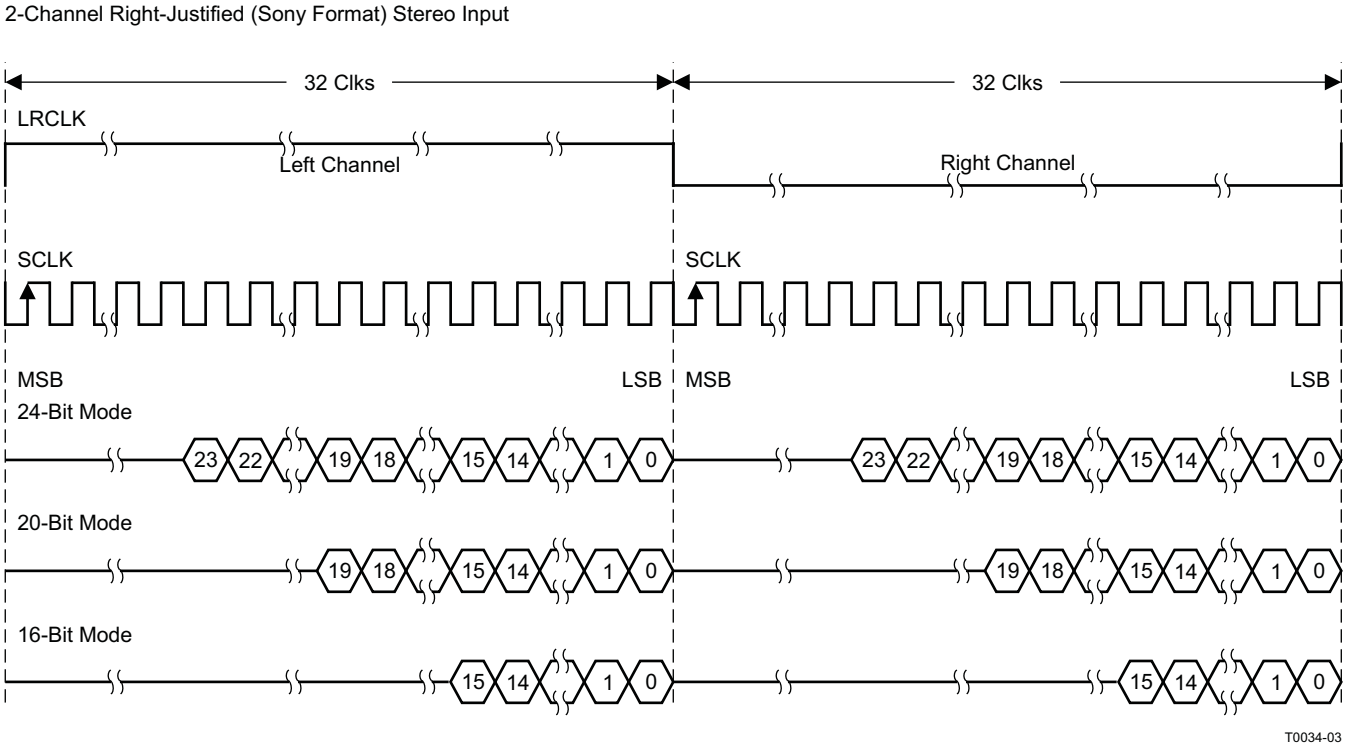


Figure 34. Right-Justified 64-f_S Format

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

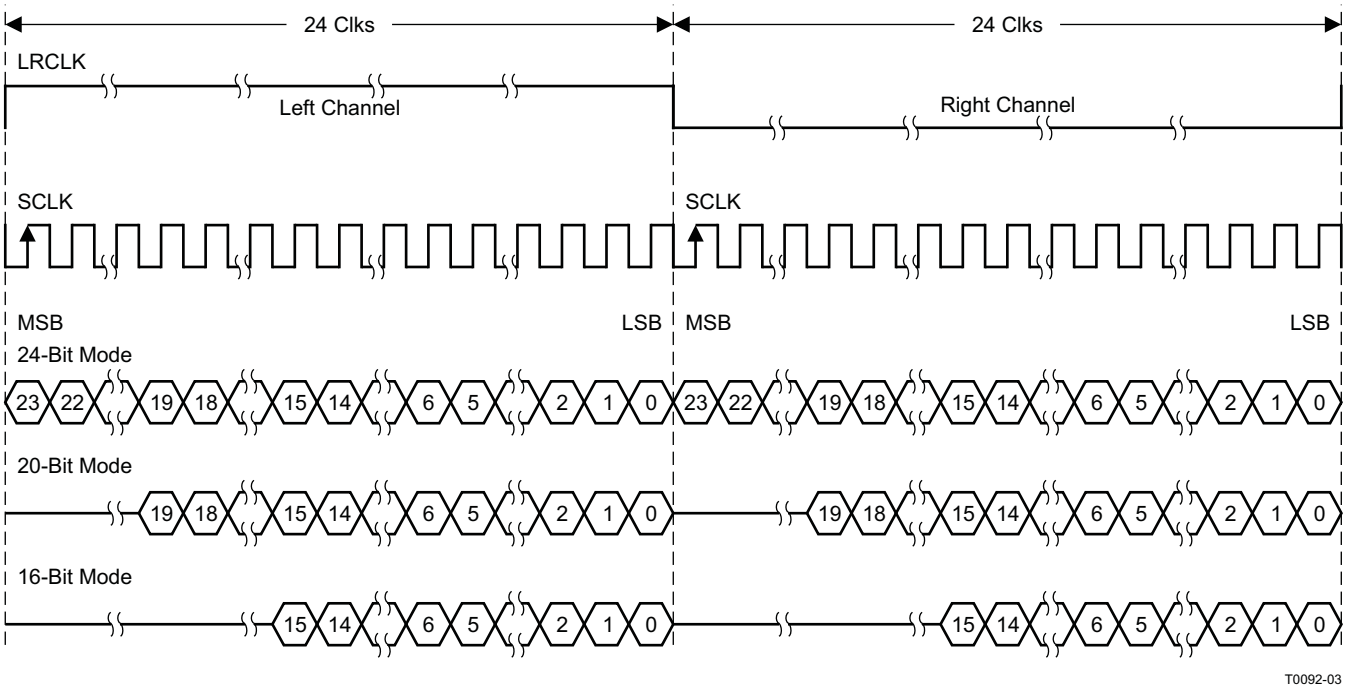


Figure 35. Right-Justified 48-f_S Format

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

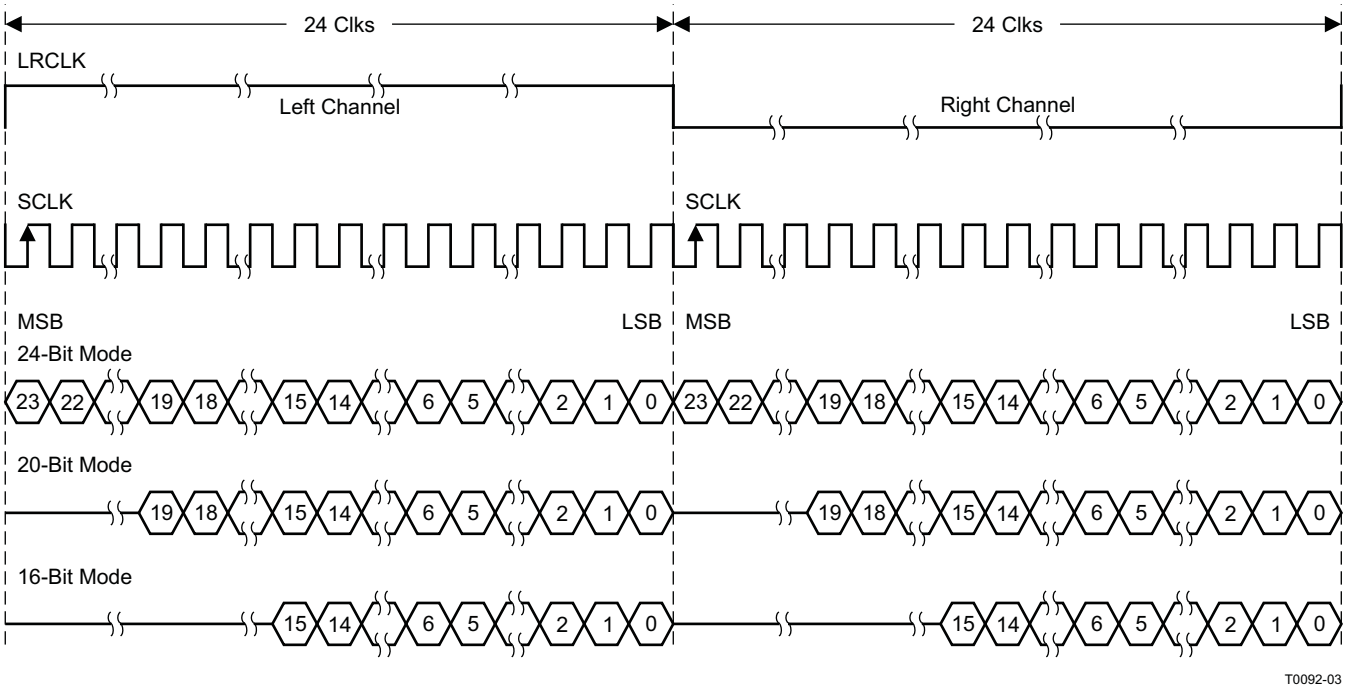


Figure 36. Right-Justified 32-f_S Format

I²C SERIAL CONTROL INTERFACE

The TAS5705 DAP has a bidirectional I²C interface that is compatible with the I²C (Inter IC) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports standard-mode I²C bus operation (100 kHz maximum) and fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 37. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5705 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. External pullup resistors must be used to set the high level for the SDA and SCL signals.

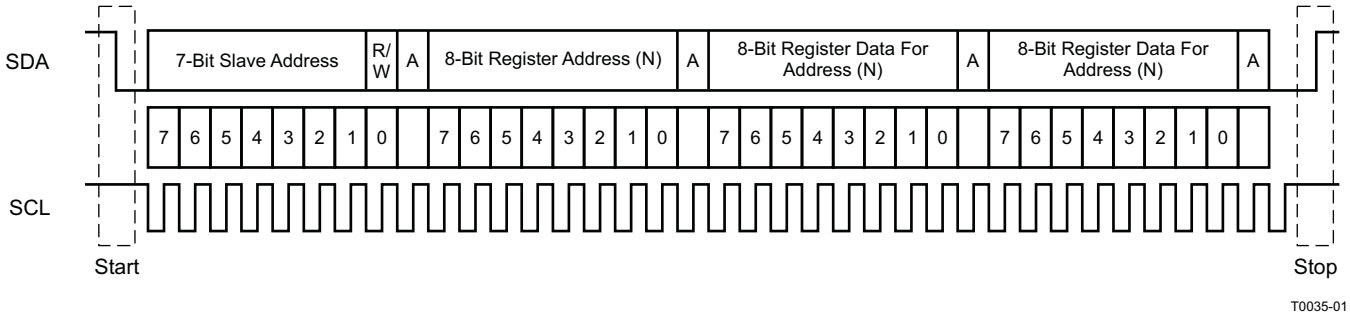


Figure 37. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 37.

The 7-bit address for TAS5705 is 0011 011 (0x36).

Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial control interface supports only multiple-byte (4-byte) read/write operations.

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. If a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded. Similarly, if a write command is received for a mixer coefficient, the DAP expects to receive one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random I^2C addressing. The TAS5705 also supports sequential I^2C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I^2C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5705. For sequential I^2C write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 38, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I^2C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5705 internal memory address being accessed. After receiving the address byte, the TAS5705 again responds with an acknowledge bit. Next, the master device transmits to the memory address being accessed the data byte to be written. After receiving the data byte, the TAS5705 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

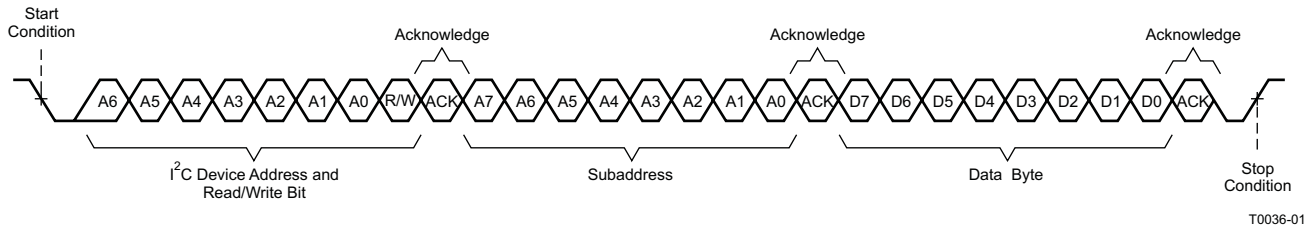


Figure 38. Single-Byte Write Transfer

Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 39. After receiving each data byte, the TAS5705 responds with an acknowledge bit.

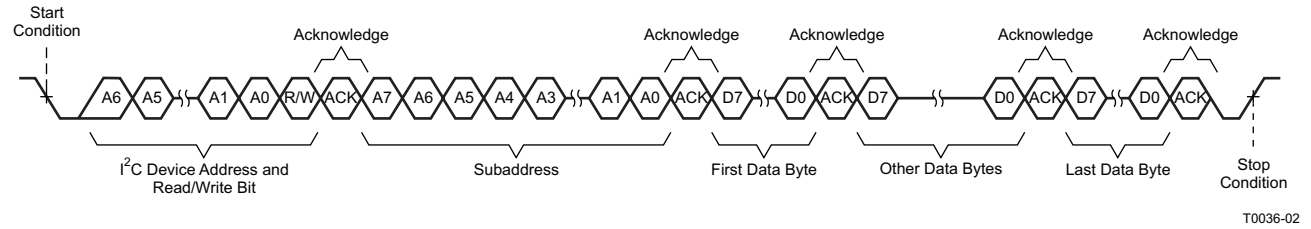


Figure 39. Multiple-Byte Write Transfer

Single-Byte Read

As shown in Figure 40, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5705 address and the read/write bit, TAS5705 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5705 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5705 again responds with an acknowledge bit. Next, the TAS5705 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

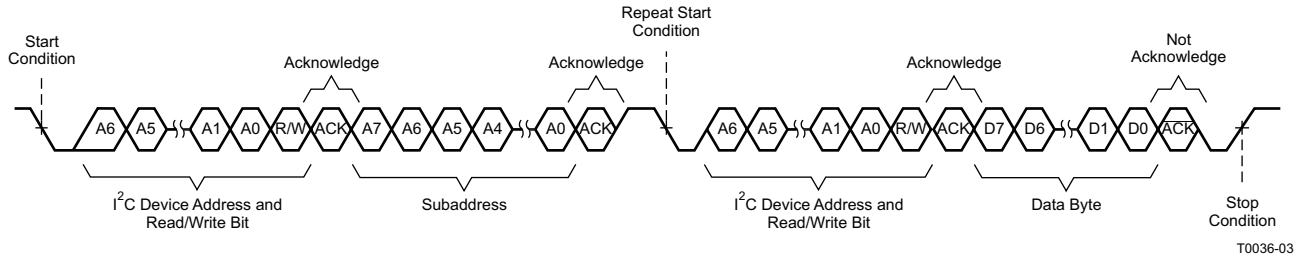


Figure 40. Single-Byte Read Transfer

Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5705 to the master device as shown in Figure 41. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

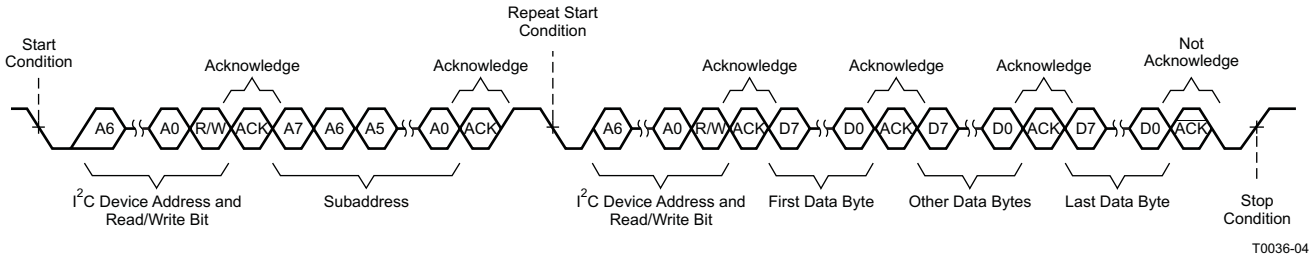


Figure 41. Multiple-Byte Read Transfer

Dynamic Range Control (DRC)

The DRC input/output diagram is shown in Figure 42.

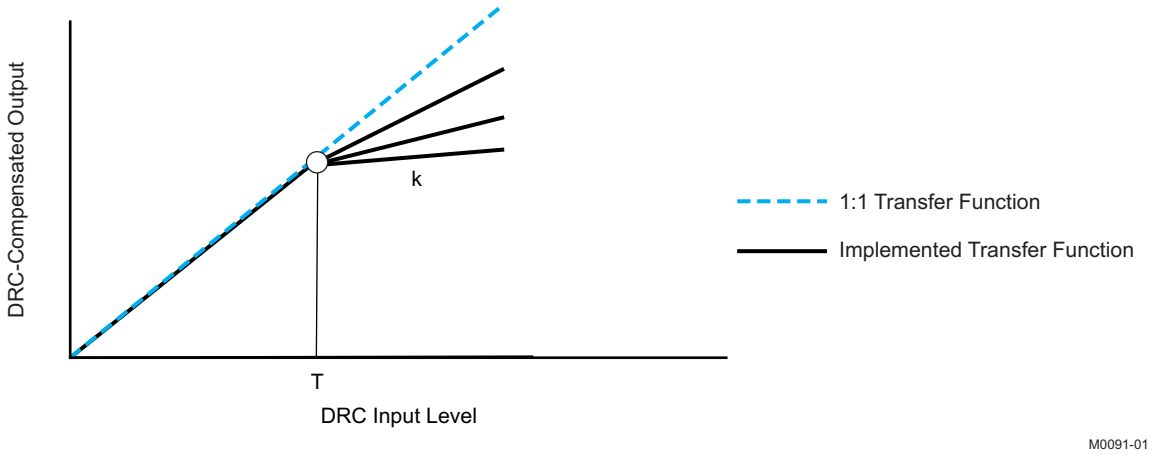


Figure 42. Dynamic Range Control

The TAS5705 has single-threshold dynamic range compressors (one for all satellites and one for the subwoofer). There are two distinct DRC blocks. DRC1 controls the satellite channels. DRC2 controls the subwoofer channel. The DRC provides compression capabilities above the threshold region of audio signal levels. A programmable threshold level sets the boundaries of the two regions. The offset (boost or cut) can be defined by a programmable offset coefficient. The DRC implements the composite transfer function by computing a 3.23-format gain coefficient from each sample output of an RMS estimator. This gain coefficient is then applied to a mixer element, whose other input is the audio data channel. The mixer output is the DRC-adjusted audio data.

The audio is the signal level following the volume control, as specified by the user. The estimates are then compared on a sample-by-sample basis, and the largest is used to compute the compression gain coefficient. The gain coefficient is then applied to the audio of the satellite group.

The control parameters for the dynamic range controls are programmable via the I^2C interface.

The DRC control for each channel is performed by two control bits. The encoding is shown in Table 2.

Table 2. DRC Control Inputs

0x46 Bit 1	0x46 Bit 0	Description
X	0	Disable DRC1
X	1	Enable DRC1
0	X	Disable DRC2
1	X	Enable DRC2

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/right channels and one DRC for the subwoofer channel.

- Thresholds T1 and T2 define the thresholds for DRC1 and DRC2, respectively.
- Offsets O1 and O2 define the gain coefficients for DRC1 and DRC2, respectively.
- The magnitudes of slopes k1 and k2 define the degree of compression to be performed above the threshold for DRC1 and DRC2, respectively.

The three sets of parameters are all defined in logarithmic space, and adhere to the following rules.

- The maximum input sample into the DRC is referenced at 0 dB. All values below this maximum value then have negative values in logarithmic (dB) space.
- Thresholds T1 and T2 define, in dB, the boundaries of the regions of the DRC, as referenced to the RMS value of the data into the DRC. 0-dB threshold settings reference the maximum-valued RMS input into the DRC, and negative-valued thresholds reference all other RMS input levels. Positive-valued thresholds have no physical meaning and are not allowed. In addition, zero-valued threshold settings are not allowed.

The threshold settings must be programmed as 32-bit (9.23 format) numbers.

Zero-valued and positive-valued threshold settings are not allowed, and cause unpredictable behavior if used.

- Offsets O1 and O2 define, in dB, the attenuation (cut) or gain (boost) applied by the DRC-derived gain coefficient at the threshold points T1 and T2, respectively. Positive offsets are defined as cuts, and thus boost or gain selections are negative numbers.
- Slopes k1 and k2 define the compression is to be performed within a given region, and the degree of compression to be applied. Slopes are programmed as 26-bit (3.23 format) numbers.

DRC Implementation

Figure 4.13.1-1 shows the three elements comprising the DRC: (1) an RMS estimator, (2) a compression coefficient computation engine, and (3) an attack/decay controller.

- RMS Estimator—This DRC element derives an estimate of the rms value of the audio data stream into the DRC. For the DRC block shared by Ch1 though Ch4 , the individual channel estimates are computed. The outputs of the estimators are then compared, sample-by-sample, and the largest-valued sample is forwarded to the compression/expansion coefficient-computation engine. Two programmable parameters, ae and (1 – ae), set the effective time window over which the RMS estimate is made. For the DRC block shared by Ch1 though Ch4, the programmable parameters apply to both RMS estimators. The time window over which the RMS estimation is computed can be determined by

$$t_{window} = \frac{1}{f_S \ln(1 - ae)}$$

- Compression Coefficient Computation—This DRC element converts the output of the rms estimator to a logarithmic number, determines the region where the input resides, and then computes and outputs the appropriate coefficient to the attack/decay element. The programmable parameters, T1, T2, O1, O2, K1, and K2, define the compression regions for both DRCs implemented by this element.
- Attack/Decay Control—This DRC element controls the transition time of changes in the coefficient computed in the compression/expansion coefficient computation element. Four programmable parameters define the operation of this element. Parameters ad and (1 – ad) set the decay or release time constant to be used for signal amplitude boost (expansion). Parameters aa and (1 – aa) set the attack time constant to be used for signal amplitude cuts. The transition-time constants can be determined by

$$t_a = \frac{1}{f_S \ln(1 - aa)}$$

$$t_a = \frac{1}{f_S \ln(1 - aa)}$$

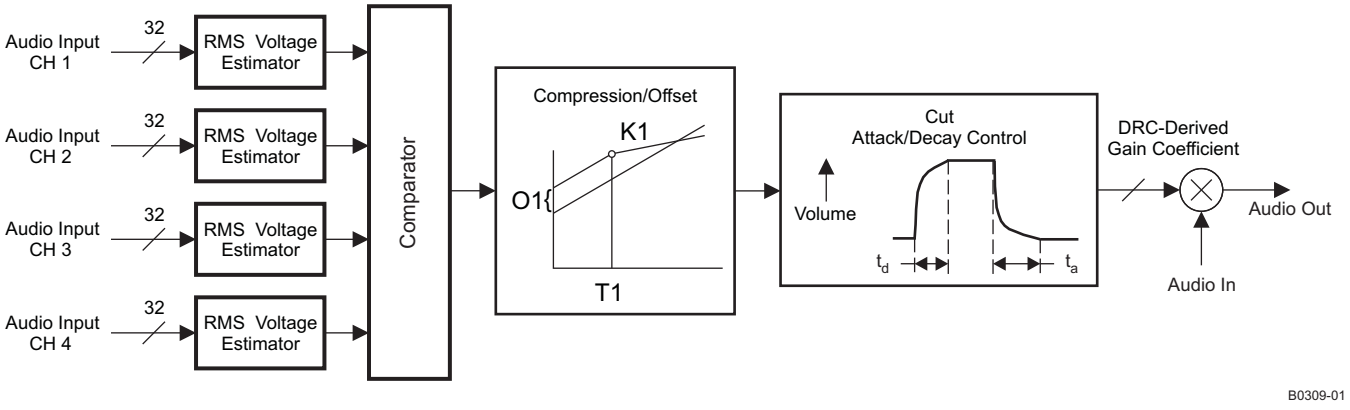


Figure 43. DRC Block Diagram

Threshold Parameter Computation

For thresholds,

$$T_{db} = -6.0206\,T_{INPUT} = -6.0206\,T_{SUB\_ADDRESS\_ENTRY}$$

If, for example, it is desired to set T1 = –64 dB, then the subaddress entry required to set T1 to –64 dB is

$$T1_{SUB\_ADDRESS\_ENTRY} = \frac{-64}{-6.0206} = 10.63$$

T1 is entered as a 32-bit number in 9.23 format. Therefore,

T1 = 10.63 = 0 1010.1010 0001 0100 0111 1010 111 = 0x0550 A3D7 in 9.23 format

Slope Parameter Computation

In developing the equations used to determine the subaddress input value required to realize a given compression or expansion within a given region of the DRC, the following convention has been adopted.

DRC Transfer = Input Increase : Output Increase

If the DRC realizes an output increase of n dB for every dB increase in the rms value of the audio into the DRC, a 1:n expansion is being performed. If the DRC realizes a 1-dB increase in output level for every n dB increase in the rms value of the audio into the DRC, an n:1 compression is being performed.

For a 1:n expansion, the slope k can be found by

$$k = n - 1$$

For an n:1 compression, the slope k can be found by

$$k = \frac{1}{n} - 1 \tag{1}$$

In compression (n:1), n is implied to be greater than 1. For compression, Equation 1 means –1 < k < 0 for n > 1. Thus k must always lie in the range k > –1.

$$\text{Compression equation: } k = -4 = \frac{1}{n} - 1 \rightarrow n = -\frac{1}{3} \rightarrow -0.3333{:}1 \text{ compression}$$

With k = –4 then, the output decreases 3 dB for every 1-dB increase in the rms value of the audio into the DRC. As the input increases in signal amplitude, the output decreases in signal amplitude.

DRC Offset Calculation

The DRC offset is calculated by

$$G_{offset} = \frac{10^{(g_d/20)}}{15.5}$$

where g_d = desired gain (in dB) and 15.5 is the the fixed antilog normalization factor. A value of g_d = 0 indicates no offset.

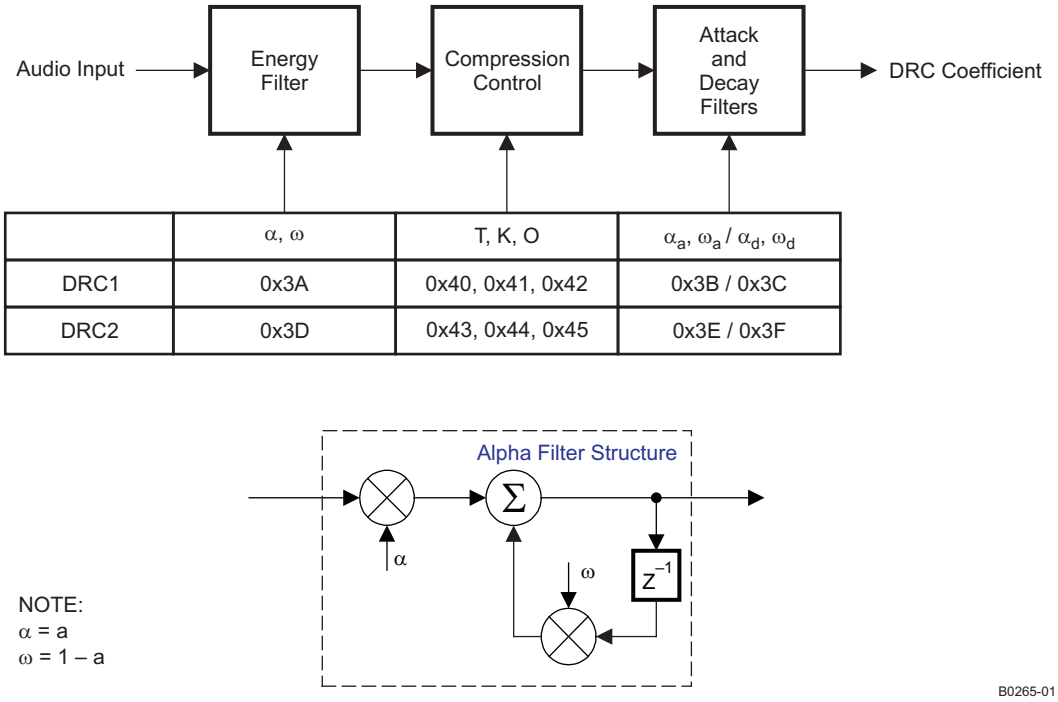


Figure 44. DRC Structure

AM Tuner Interference Management

Digital amplifiers produce AM interference by radio energy emissions near the digital amplifier switching rate and the harmonics of that switching rate. The digital amplifier emits an interference spectrum in the AM band that is centered on the second though sixth harmonics of the digital amplifier switching frequency. Because the digital amplifier switching rate is a multiple of the input data sample rate, the interference frequencies can be changed by changing the sample rate.

Anatomy of a Receiver

AM receivers are composed of six sections as shown in Figure

The radio-frequency (RF) section has a variable tuner that preselects the frequencies to be received. The RF section provides only enough filtering to significantly attenuate signals that are significantly above or below the desired tuned frequency. The RF-section gain is controlled by the AGC to compensate for variations in the signal strength.

The mixer, variable-frequency oscillator (VFO), and intermediate frequency (IF) sections perform the bulk of the receiver tuning. In home receivers, the variable oscillator is adjusted so that it is a constant 455 kHz higher than the desired tuned frequency. The output of the mixer consists of four frequencies, RF, VFO, RF + VFO and RF – VFO. These signals are then passed into the IF section, where sharp discriminating filters to accept only the constant 455-kHz (RF – VFO) signal. The resulting signal is amplified and then passed to the detector section, where it is transformed into an audio signal.

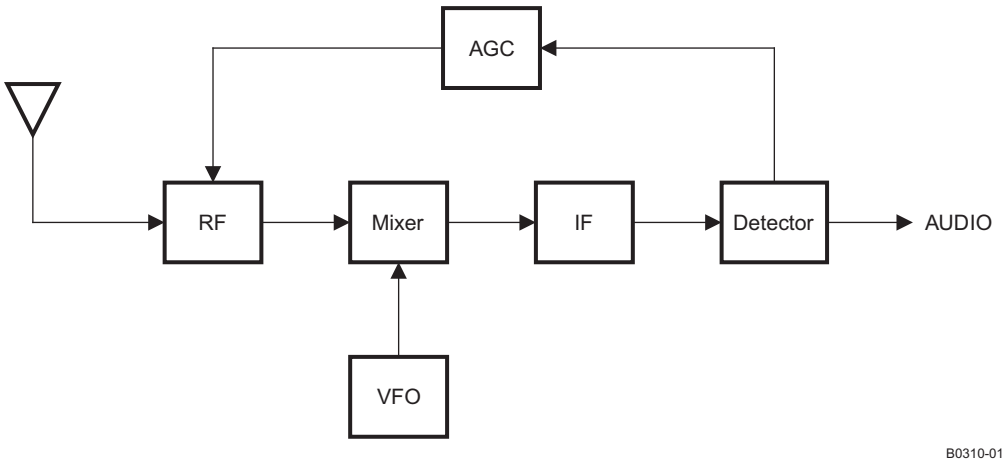


Figure 45. AM Receiver Architecture

Radio-frequency interference at either the tuned frequency or the 455-kHz IF frequency adversely affects the AM radio reception.

However, there is another frequency that this receiver architecture also receives. This is a signal at the VFO + tuned frequency (RF + 2 × IF).

For example, to tune a receiver at 540 kHz, an oscillator of 995 kHz is used to produce a difference frequency of 455 kHz. However, the receiver can also receive a frequency at the oscillator frequency 995 kHz plus the IF frequency of 455 kHz (= 1450 kHz). This frequency is called the IF image frequency. This is because the 1450 – 955 produces a difference frequency of 455 kHz. It is the role of the RF section to provide sufficient selectivity to attenuate frequencies that are several hundred kHz from the tuned frequency. However, this is often a weakness of low-cost receivers. Therefore, the AM interference avoidance approach includes this frequency in its interference avoidance algorithms.

AM Interference Avoidance

As a result, during AM interference avoidance, a the system select a switching rate such that the radiated emissions avoid

- The IF (455 kHz)
- The tuned frequency
- IF image frequency (tuned frequency + 2 × 455 kHz)

During AM interference avoidance, the TAS5705 receives the sample rate (38, 44.1, or 48 kHz) and the tuned frequency (typically 540 kHz to 1840 kHz) from the system controller. The TAS5705 uses these two values to determine what switching rate to use. The TAS5705 has a sample-rate converter (SRC) that permits the PWM switching rate to be increased or decreased by a fractional amount. The SRC produces a PWM switching rate that is 6, 7, or 8 times the data sample rate.

This is done by specifying the order in which the switching rates are tested. The TAS5705 provides four selectable sequences. The evaluation selects the first rate from the sequence and applies the three tests. If the switching rate is found to be GOOD in all three tests, then that rate is used. If that switching rate is found to be BAD in any of the tests, then the next rate in the sequence is taken for evaluation.

The sequences are as follows: (see Register 0x22, bits 19–18)

1. 8 × sample rate, 7 × sample rate, 6 × sample rate
2. 8 × sample rate, 6 × sample rate, 7 × sample rate
3. 7 × sample rate, 8 × sample rate, 6 × sample rate
4. 7 × sample rate, 6 × sample rate, 8 × sample rate

AM Controls

There are three controls for the AM section.

- AM Mode Enable—This control enables and disables sample rate conversion for 38, 44.1 and 48 kHz.
- AM Search Sequence—The sequence the device will search for switching frequency that avoids interference
- AM Tuned Frequency—The AM tuned frequency is encoded as four binary-encoded decimal digits, held in two registers, representing the tuned frequency in kHz. The range of valid values is from 1999 kHz to 0500 KHz.

When the TAS5705 receives a change to any of these inputs, it

1. Performs a fast (128-step) mute
2. Performs the requested AM interference avoidance operation
   (a) If requested, enables/disables the AM mode
   (b) If requested, selects the requested AM search sequence
   (c) Selects and sets the appropriate SRC rate
3. Performs a fast (128 step) unmute

Loudness Function

The TAS5705 provides a direct form I biquad for loudness on the subwoofer channel. The first biquad is contained in a gain-compensation circuit that maintains the overall system gain at 1 or less to prevent clipping at loud volume settings. This gain compensation is shown in Figure 46.

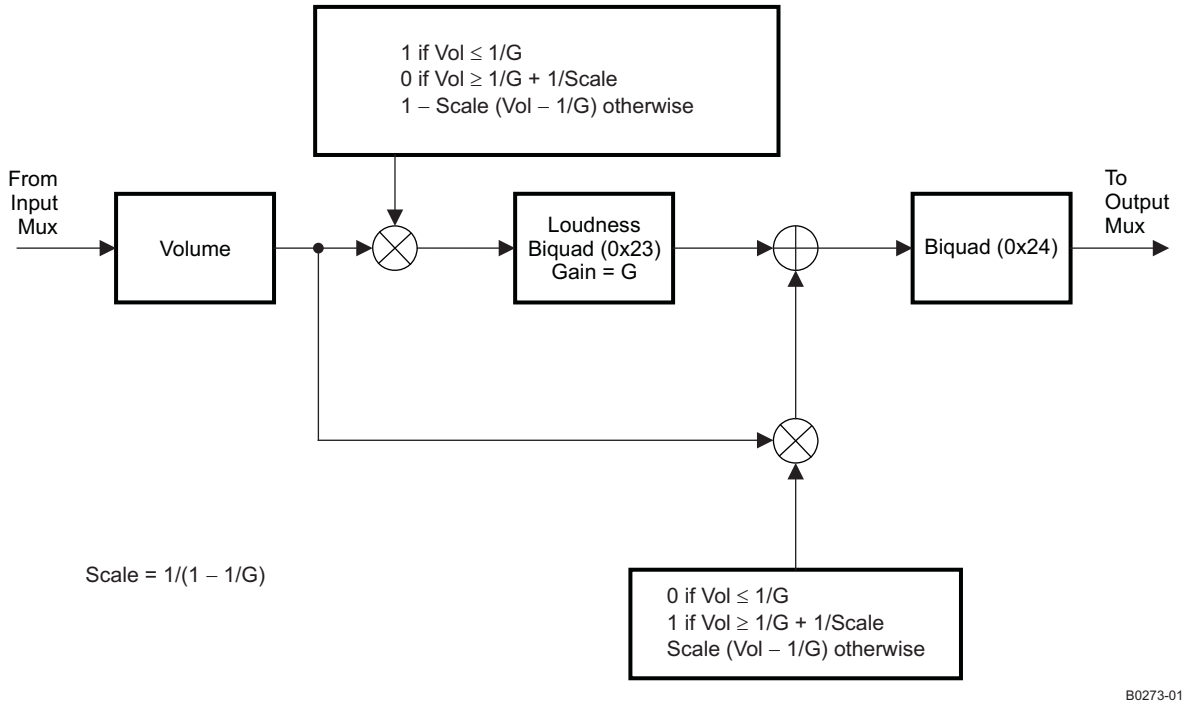


Figure 46. Biquad Gain Control Structure

Table 3. Loudness Table Example for Gain = 4, 1/G = 0.25, Scale = 1.33

Volume	0.125	0.25	0.375	0.5	0.625	0.75	0.875	1	1.125	1.25	1.375	1.5	1.625	1.75	1.875	2
Biquad path	1	1	0.833	0.666	0.5	0.333	0.166	0	0	0	0	0	0	0	0	0
Direct path	0	0	0.166	0.333	0.5	0.666	0.833	1	1	1	1	1	1	1	1	1
Total gain	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The biquads are implemented in a direct form-I architecture. The direct form-I structure provides a separate delay element and mixer (gain coefficient) for each node in the biquad filter.

The five 26-bit (3.23) coefficients for the biquad are programmable via the I^2C interface.

The following steps are invovled in using a loudness biquad with the volume comprensation feature:

1. Program the biquad with a loudness filter.
2. Program 0x26 (1/G) and 0x28 (scale).
3. Enable volume compensation in register 0x0E.

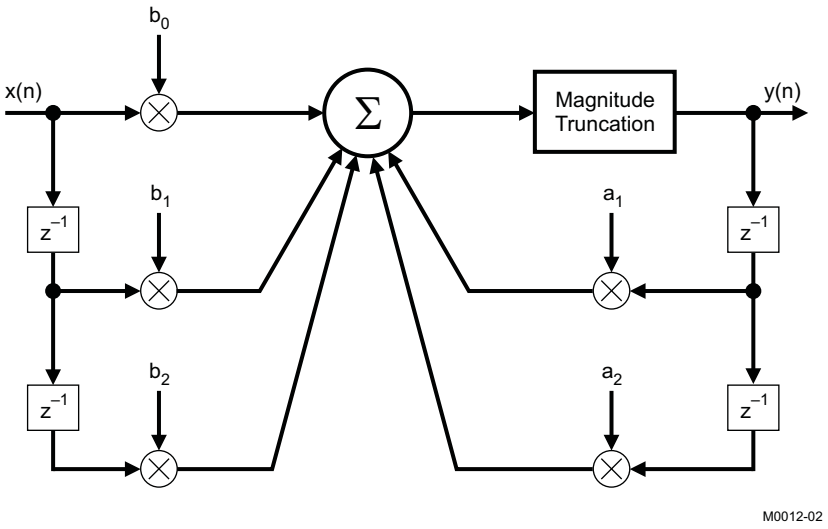


Figure 47. Biquad Filter

Subchannel Preprocessing

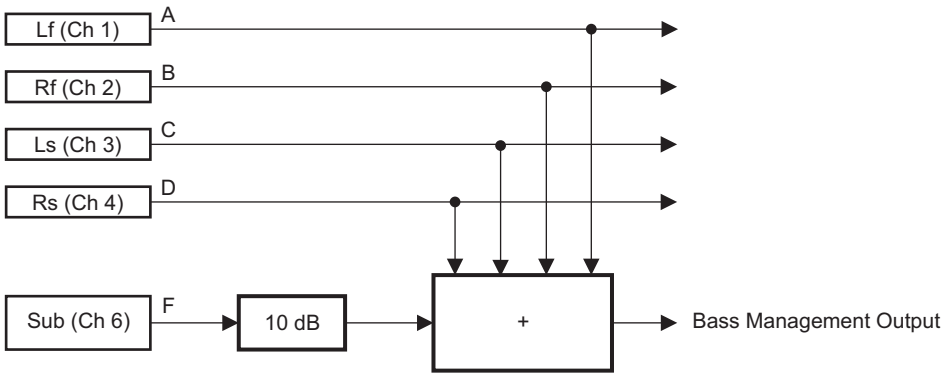
A subchannel has three input multiplexers that can select from the bass management output, the downmix output, or the channel-6 input multiplexer output.

Register 0x21, bits (9:8) determine the submultiplexer selection, defined in Table 4.

Table 4. Submultiplexer Selection

Bits	Submultiplexer
00	Pass through channel-6 input multiplexer output
01	Select bass management block output for submultiplexer
10	Select downmix ouput for submultiplexer

The Bass Management function is explained in Figure 48.



Bass Management Output = BS_Out (linear) = Ch 6 = F × 3.121 + (A + B + C + D)
BS_Out (log) = 20 × log (BS_Out)

B0291-01

NOTE: Selection of A, B, C, D, or F is determined by the input multiplexer selection register (0x20).

Figure 48. Bass Management Block Diagram

Downmix is defined by I^2C register 0x21, bits (3:0), as listed in Table 5.

Table 5. Downmix Definitions

Bits 3:0	Definition
X0X0	L' = (0.000 × Ls + 0.000 × L) / 1.000
X0X1	L' = (0.000 × Ls + 1.000 × L) / 1.000
X1X0	L' = (1.000 × Ls + 0.000 × L) / 1.000
X1X1	L' = (0.707 × Ls + 1.000 × L) / 1.707
0X0X	R' = (0.000 × Rs + 0.000 × R) / 1.000
0X1X	R' = (0.000 × Rs + 1.000 × R) / 1.000
1X0X	R' = (1.000 × Rs + 0.000 × R) / 1.000
1X1X	R' = (0.707 × Rs + 1.000 × R) / 1.707

BANK SWITCHING

The TAS5705 uses an approach called *bank switching* together with automatic sample-rate detection. All processing features that must be changed for different sample rates are stored internally in the TAS5705. The TAS5705 has three full banks storing information, one for 32 kHz, one for 44.1/48 kHz, and one for all other data rates. Combined with the clock-rate autodetection feature, bank switching allows the TAS5705 to detect automatically a change in the input sample rate and switch to the appropriate bank without any MCU intervention.

The TAS5705 supports three banks of coefficients to be updated during the initialization. One bank is for 32 kHz, a second bank is for 44.1/48 kHz, and a third bank is for all other sample rates. An external controller updates the three banks (see the I^2C register mapping table for bankable locations) during the initialization sequence.

If the autobank switch is enabled (register 0x50, bits 2:0) , then the TAS5705 automatically swaps the coefficients for subsequent sample rate changes, avoiding the need for any external controller intervention for a sample rate change.

By default, bits 2:0 have the value 000; that means the bank switch is disabled. In that state, any update to locations 0x29–0x3F go into the DAP. A write to register 0x50 with bits 2:0 being 001, 010, or 011 brings the system into the coefficient-bank-update state *update bank1*, *update bank2,* or *update bank3*, respectively. Any subsequent write to locations 0x29–0x3F updates the coefficient banks stored outside the DAP. After updating all the three banks, the system controller should issue a write to register 0x50 with bits 2:0 being 100; this changes the system state to automatic bank update. In automatic bank update, the TAS5705 automatically swaps banks based on the sample rate.

In the headphone mode, speaker equalization and DRC are disabled, and they are restored on returning to the speaker mode.

Command sequences for initialization can be summarized as follows:

1. **Enable factory trim for internal oscillator:** Write to register 0x1B with a value 0x00.
2. **Update coefficients:** Coefficients can be loaded into DAP RAM using the manual bank mode.

   OR

   Use automatic bank mode.
   (a) Enable bank-1 mode: Write to register 0x50 with 0x01. Load the 32-kHz coefficients. TI ALE can generate coefficients.
   (b) Enable bank-2 mode: Write to register 0x50 with 0x02. Load the 48-kHz coefficients.
   (c) Enable bank-3 mode: Write to register 0x50 with 0x03. Load the other coefficients.
   (d) Enable automatic bank switching by writing to register 0x50 with 0x04.
3. **Bring the system out of all-channel shutdown:** Write 0 to bit 6 of register 0x05.
4. **Issue master volume:** Write to register 0x07 with the volume value (0 db = 0x30).

Interchannel Delay (ICD) Settings

Table 6. Recommended ICD Settings

Mode	Description	ICD1	ICD2	ICD3	ICD4	ICD5	ICD6
BD	2 BTL channels, internal power stage only, BD mode	A(L+) = –18 (0xB8)	C(R+) = 24 = (0x60)	B(L–) = –24 = (0xA0)	D(R–) = 18 = (0x48)	SM(S–) = –3 = (0xF4)	SP(S+) = 3 = (0x0C)
AD	2 internal BTL channels, 1 external BTL channel using PBTL TAS5102, AD mode	A(L+) = –21 = (0xAC)	C(R+) = 21 (0x54)	B(L–) = –21 = (0xAC)	D(R–) = 21 = (0x54)	SM(S–) = 0 = (0x00)	SP(S+) = 0 = (0x00)

I²C SERIAL CONTROL COMMAND CHARACTERISTICS

The DAP has two groups of I²C commands. One set is commands that are designed specifically to be operated while audio is streaming and that have built-in mechanisms to prevent noise, clicks, and pops. The other set does not have this built-in protection.

Commands that are designed to be adjusted while audio is streaming:

- Master volume
- Master mute
- Individual channel volume
- Individual channel mute

Commands that are normally issued as part of initialization:

- Serial data interface format
- De-emphasis
- Sample-rate conversion
- Input multiplexer
- Output multiplexer
- Biquads
- Down mix
- Channel delay
- Enable/disable dc blocking
- Hard/soft unmute from clock error
- Enable/disable headphone outputs

Start-up sequence for correct device operation

This sequence must be followed to ensure proper operation.

1. Hold ALL logic inputs low. Power up AVDD/DVDD and wait for the inputs to settle in the allowed range.
2. Drive $\overline{\text{PDN}}$ = 1, $\overline{\text{MUTE}}$ = 1, and drive other logic inputs to the desired state.
3. Provide a stable MCLK, LRCLK, and SCLK (clock errors must be avoided during the initialization sequence) .
4. After completing step 3, wait 100 µs, then drive $\overline{\text{RESET}}$ = 1, and wait 13.5 ms after $\overline{\text{RESET}}$ goes high.
5. Trim the internal oscillator (write 0x00 to register 0x1B).
6. Wait 50 ms while the part acquires lock.
7. Configure the DAP via I²C, e.g.:
   - Downmix control (0x21)
   - Biquads (0x23–0x24 and 0x29–0x38)
   - DRC parameters and controls (0x3A–0x46)
   - Bank select (0x50)

   NOTE: User may not issue any I²C reads or writes to the above registers after this step is complete.
8. Configure remaining I²C registers, e.g.:
   - Shutdown group
   - De-emphasis
   - Input multiplexers
   - Output multiplexers
   - Channel delays
   - DC blocking
   - Hard/soft unmute from clock error
   - Serial data interface format
   - Clock register (manual clock mode only)

   NOTE: The BKND_ERR register (0x1C) can only be written once with a value that is not reserved (00 and 01 are reserved values).
9. Exit all-channel shutdown (write 0 to bit 6 of register 0x05).

10. This completes the initialization sequence. From this step on, no further constraints are imposed on $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, and clocks.
11. During normal operation the user may do the following:
    (a) Write to the master or individual-channel volume registers.
    (b) Write to the soft-mute register.
    (c) Write to the clock and serial data interface format registers (in manual clock mode only).
    (d) Write to bit 6 of register 0x05 to enter/exit all-channel shutdown. No other bits of register 0x05 may be altered. After issuing the all-channel shutdown command, no further I^2C transactions that address this device are allowed for a period of at least: 1 ms + 1.3 × (period specified in start/stop register 0x1A) .
    (e) $\overline{\text{PDN}}$ may be asserted (low) at any time. Once $\overline{\text{PDN}}$ is asserted, no I^2C transactions that address this device may be issued until $\overline{\text{PDN}}$ has been deasserted and the part has returned to active mode.

    NOTE: When the device is in a powered down state (initiated via $\overline{\text{PDN}}$), the part is not reset if $\overline{\text{RESET}}$ is asserted.

    NOTE: Once $\overline{\text{RESET}}$ is asserted, and as long as the part is in a reset state, the part does not power down if $\overline{\text{PDN}}$ is asserted. For powering the part down, a negative edge on $\overline{\text{PDN}}$ must be issued when $\overline{\text{RESET}}$ is high and the part is not in a reset state.

    NOTE: No registers besides those explicitly listed in Steps a.–d. should be altered during normal operation (i.e., after exiting all-channel shutdown).

    NOTE: No registers should be read during normal operation (i.e., after exiting all-channel shutdown) .
12. To reconfigure registers:
    (a) Return to all-channel shutdown (observe the shutdown wait time as specified in Step 11.d.).
    (b) Drive $\overline{\text{PDN}}$ = 1, and hold $\overline{\text{MUTE}}$ stable.
    (c) Provide a stable MCLK, LRCLK, and SCLK.
    (d) Repeat configuration starting from step (6).

Table 7. Serial Control Interface Register Summary (1)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x6C
0x01	Device ID register	1	Description shown in subsequent section	0x23
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0xA0
0x04	Serial data interface register	1	Description shown in subsequent section	0x05
0x05	System control register 2	1	Description shown in subsequent section	0x40
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	1	Description shown in subsequent section	0xFF (mute)
0x08	Channel 1 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x09	Channel 2 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x0A	Channel 3 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x0B	Channel 4 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x0C	HP volume	1	Description shown in subsequent section	0x30 (0 dB)
0x0D	Channel 6 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x0E	Volume configuration register	1	Description shown in subsequent section	0x91
0x0F		1	Reserved (2)	
0x10	Modulation limit register	1	Description shown in subsequent section	0x02
0x11	IC delay channel 1	1	Description shown in subsequent section	0xB8

(1) Biquad definition is given in Figure 47 .
(2) Reserved registers should not be accessed.

Table 7. Serial Control Interface Register Summary (1) (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x12	IC delay channel 2	1	Description shown in subsequent section	0x60
0x13	IC delay channel 3	1	Description shown in subsequent section	0xA0
0x14	IC delay channel 4	1	Description shown in subsequent section	0x48
0x15	IC delay channel 5	1	Description shown in subsequent section	0xF4
0x16	IC delay channel 6	1	Description shown in subsequent section	0x0C
0x17	Offset register	1	Reserved	0x00
0x18		1	Reserved (2)	
0x19	PWM shutdown group register	1		0x30
0x1A	Start/stop period register	1		0x0A
0x1B	Oscillator trim register	1		0x82
0x1C	BKND_ERR register	1		0x02
0x1D–0x1F			Reserved (2)	
0x20	Input Mux register	4	Description shown in subsequent section	0x0089 777A
0x21	Downmix input Mux register	4	Description shown in subsequent section	0x0000 4203
0x22	AM tuned frequency	4	Description shown in subsequent section	0x0000 0000
0x23	ch6_bq[2] (Loudness BQ)	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x24	ch6_bq[3] (post volume BQ)	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x25	PWM Mux register		Description shown in subsequent section	0x0102 1345
0x26	1/G register	4	u[31:26], x[25:0]	0x0080 0000
0x27		1	Reserved (3)	
0x28	Scale register	4	u[31:26], x[25:0]	0x0080 0000
0x29	ch1_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2A	ch1_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2B	ch1_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

(3) Reserved registers should not be accessed.

Table 7. Serial Control Interface Register Summary (1) (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x2C	ch1_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2D	ch1_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2E	ch1_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2F	ch1_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x30	ch2_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x31	ch2_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x32	ch2_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x33	ch2_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x34	ch2_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Table 7. Serial Control Interface Register Summary (1) (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x35	ch2_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x36	ch2_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x37	ch6_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x38	ch6_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x39		4	Reserved (4)	
0x3A	DRC1 ae	8	u[31:26], ae[25:0]	0x0080 0000
	DRC1 (1 – ae)		u[31:26], (1 – ae)[25:0]	0x0000 0000
0x3B	DRC1 aa	8	u[31:26], aa[25:0]	0x0080 0000
	DRC1 (1 – aa)		u[31:26], (1 – aa)[25:0]	0x0000 0000
0x3C	DRC1 ad	8	u[31:26], ad[25:0]	0x0080 0000
	DRC1 (1 – ad)		u[31:26], (1 – ad)[25:0]	0x0000 0000
0x3D	DRC2 ae	8	u[31:26], ae[25:0]	0x0080 0000
	DRC 2 (1 – ae)		u[31:26], (1 – ae)[25:0]	0x0000 0000
0x3E	DRC2 aa	8	u[31:26], aa[25:0]	0x0080 0000
	DRC2 (1 – aa)		u[31:26], (1 – aa)[25:0]	0x0000 0000
0x3F	DRC2 ad	8	u[31:26], ad[25:0]	0x0080 0000
	DRC2 (1 – ad)		u[31:26], (1 – ad)[25:0]	0x0000 0000
0x40	DRC1-T	4	T1[31:0]	0xFDA2 1490
0x41	DRC1-K	4	u[31:26], k1[25:0]	0x0384 2109
0x42	DRC1-O	4	u[31:26], O1[25:0]	0x0008 4210
0x43	DRC2-T	4	T2[31:0]	0xFDA2 1490
0x44	DRC2-K	4	u[31:26], k2[25:0]	0x0384 2109
0x45	DRC2-O	4	u[31:26], O2[25:0]	0x0008 4210
0x46	DRC control	4	u[31:2], ch6_enable, ch1_5_enable	0x0000 0000
0x47–0x49		4	Reserved (4)	0x0000 0000
0x50		4	Bank update command register	0x0000 0000
0x51–0xFF		4	Reserved (4)	0x0000 0000

(4) Reserved registers should not be accessed.

CLOCK CONTROL REGISTER (0x00)

In the manual mode, the clock control register provides a way for the system microprocessor to update the data and clock rates based on the sample rate and associated clock frequencies. In the autodetect mode, the clocks are automatically determined by the TAS5705. In this case, the clock control register contains the autodetected FS and MCLK status as automatically detected (D7–D2). Bits D7–D5 select the sample rate. Bits D4–D2 select the MCLK frequency. Bit D0 is used in manual mode only. In this mode, when the clocks are updated a 1 must be written to D0 to inform the DAP that the written clocks are valid.

Table 8. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	–	–	f_S = 32-kHz sample rate
0	0	1	–	–	–	–	–	f_S = 38-kHz sample rate
0	1	0	–	–	–	–	–	f_S = 44.1-kHz sample rate
0	**1**	**1**	**–**	**–**	**–**	–	**–**	**f_S = 48-kHz sample rate** (1)
1	0	0	–	–	–	–	–	f_S = 88.2-kHz sample rate
1	0	1	–	–	–	–	–	f_S = 96-kHz sample rate
1	1	0	–	–	–	–	–	f_S = 176.4-kHz sample rate
1	1	1	–	–	–	–	–	f_S = 192-kHz sample rate
–	–	–	0	0	0	–	–	MCLK frequency = 64 × f_S (2)
–	–	–	0	0	1	–	–	MCLK frequency = 128 × f_S (3)
–	–	–	0	1	0	–	–	MCLK frequency = 192 × f_S
–	**–**	**–**	**0**	**1**	**1**	**–**	**–**	**MCLK frequency = 256 × f_S** (1)
–	**–**	**–**	1	0	0	**–**	**–**	MCLK frequency = 384 × f_S
–	–	–	1	0	1	–	–	MCLK frequency = 512 × f_S (4)
–	–	–	1	1	X	–	–	Reserved
–	–	–	–	–	–	**0**	–	**Bit clock (SCLK) frequency = 64 × f_S or 32 × f_S (selected in register 0x04)** (1)
–	–	–	–	–	–	1	–	Bit clock (SCLK) frequency = 48 × f_S (5)
–	**–**	**–**	–	**–**	**–**	**–**	**0**	**Clock not valid (in manual mode only)** (1)
–	–	–				–	1	Clock valid (in manual mode only)

(1) Default values are in **bold**.
(2) Rate not available for 32-, 44.1-, and 48-kHz data rates
(3) Rate not available for 32-kHz data rate
(4) Rate not available for 176.4-kHz and 192-kHz data rates
(5) Rate only available for 192-f_S and 384-f_S MCLK frequencies

DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the firmware revision.

Table 9. Device ID Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Default** (1)
–	0	1	0	0	0	1	1	Identification code

(1) Default values are in **bold**.

ERROR STATUS REGISTER (0x02)

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if there are any persistent errors.

Table 10. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	1	–	–	–	–	–	–	PLL autolock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors** (1)

(1) Default values are in **bold**.

SYSTEM CONTROL REGISTER 1 (0x03)

System control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled (default).

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery.
If 1, use hard unmute on recovery from clock error (default). This is a fast recovery.

Bit D3: If 0, clock autodetect is enabled (default).
If 1, clock autodetect is disabled.

Bit D2: If 0, soft start is enabled (default).
If 1, soft start is disabled.

Bits D1–D0: Select de-emphasis

Table 11. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	PWM high-pass (dc blocking) disabled
1	–	–	–	–	–	–	–	**PWM high-pass (dc blocking) enabled** (1)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	0	–	–	–	–	–	Soft unmute on recovery from clock error
–	–	**1**	–	–	–	–	–	**Hard unmute on recovery from clock error** (1)
–	–	–	**0**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**Enable clock autodetect** (1)
–	–	–	–	1	–	–	–	Disable clock autodetect
–	–	–	–	–	**0**	–	–	**Enable soft start** (1)
–	–	–	–	–	1	–	–	Disable soft start
–	–	–	–	–	–	**0**	**0**	**No de-emphasis** (1)
–	–	–	–	–	–	0	1	Reserved
–	–	–	–	–	–	1	0	De-emphasis for f_S = 44.1 kHz
–	–	–	–	–	–	1	1	De-emphasis for f_S = 48 kHz

(1) Default values are in **bold**.

SERIAL DATA INTERFACE REGISTER (0x04)

The TAS5705 supports the serial data modes shown in Table 12. The default is 24-bit, I^2S mode.

Table 12. Serial Data Interface Control Register (0x04) Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTH	D7–D5	D4	D3	D2	D1	D0
Right-justified	16	000	0	0	0	0	0
Right-justified	20	000	0	0	0	0	1
Right-justified	24	000	0	0	0	1	0
I^2S	16	000	0	0	0	1	1
I^2S	20	000	0	0	1	0	0
I^2S (1)	**24**	**000**	**0**	**0**	**1**	**0**	**1**
Left-justified	16	000	0	0	1	1	0
Left-justified	20	000	0	0	1	1	1
Left-justified	24	000	0	1	0	0	0
Reserved		000	0	1	0	0	1
Right-justified	18	000	0	1	0	1	0
Reserved		000	0	1	0	1	1
Reserved		000	0	1	1	0	0
Reserved		000	0	1	1	0	1
Reserved		000	0	1	1	1	0
Reserved		000	0	1	1	1	1
Reserved		000	1	0	0	0	0
I^2S (32 f_S SCLK)	16	000	1	0	0	1	1
Left-justified (32 f_S SCLK)		000	1	0	1	1	0
Reserved		000	1	1	0	0	1
Reserved		000	1	1	0	1	1
Reserved		000	1	1	1	0	1

(1) Default values are in **bold**.

SYSTEM CONTROL REGISTER 2 (0x05)

Bit D6 is a **control** bit and bit D5 is a **configuration** bit.

When bit D6 is set low, the system starts playing; otherwise, the outputs are shut down.

Bit D5 defines the configuration of the system, that is, it determines what configuration the system runs in when bit D6 is set low. When this bit is asserted, all channels are switching. Otherwise, only a subset of the PWM channels run. The channels to shut down are defined in the shutdown group register (0x19). Bit D5 should only be changed when bit D6 is set, meaning that it is only possible to switch configurations by resetting the DAP and then restarting it again in the new configuration.

Bit D3 defines which volume register is used to control the volume of the HP_PWMx outputs when in headphone mode. When set to 0, the HP volume register (0x0C) controls the volume of the headphone outputs when in headphone mode. When bit D3 is set to 1, the channel volume registers (0x08–0x0B, 0x0D) are used for all modes (line out, headphone, speaker).

Bits D2–D1 define the output modes. The default is speaker mode with the headphone mode selectable via the external **HPSEL** terminal. The device can also be forced into headphone mode by asserting bit D1 (all other PWM channels are muted). Asserting bit D2 puts the device into a pseudo-line-out mode where the HP_PWMx and all other PWM channels are active. Bit D3 must also be asserted in this mode, and the HP_PWMx volume is controlled with the main speaker output volume controls via registers 0x08–0x0B and 0x0D.

Table 13. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (1)
–	0	0	–	–	–	–	–	When D6 is deasserted, all channels not belonging to shutdown group (SDG) are started. SDG register is 0x19.
–	0	1	–	–	–	–	–	When D6 is deasserted, all channels are started. VALID = 1. No channels in SDG1.
–	1	0	–	–	–	–	–	All channels are shut down (hard mute). VALID = 0.
–	**1**	**1**	–	–	–	–	–	**All channels are shut down (hard mute). VALID = 0** (1)
–	–	–	**0**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**Use HP volume register (0x0C) for adjusting headphone volume when in headphone mode.** (1)
–	–	–	–	1	–	–	–	Use channel volume registers (0x08–0x0B, 0x0D) for all modes.
–	–	–	–	–	**0**	**0**	–	**Speaker mode. Hardware pin, HPSEL = 1, forces device into headphone mode.** (1)
–	–	–	–	–	0	1	–	HP mode. This setting is logically ORed with external HPSEL pin.
–	–	–	–	–	1	0	–	Line out mode. Hardware pin, HPSEL, is ignored for this setting. HP_PWMx pins are active.
–	–	–	–	–	1	1	–	Reserved
–	–	–	–	–	–	–	**0**	**Reserved** (2)

(1) Default values are in **bold**.
(2) Default values are in **bold**.

SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle. Default is 0x00.

Table 14. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	–	1	Soft mute channel 1
–	–	–	–	–	–	1	–	Soft mute channel 2
–	–	–	–	–	1	–	–	Soft mute channel 3
–	–	–	–	1	–	–	–	Soft mute channel 4
–	–	1	–	–	–	–	–	Soft mute subwoofer channel (channel 6)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Unmute all channels** (1)

(1) Default values are in **bold**.

VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D)

Step size is 0.5 dB.

Master volume	– 0x07 (default is mute)
Channel-1 volume	– 0x08 (default is 0 dB)
Channel-2 volume	– 0x09 (default is 0 dB)
Channel-3 volume	– 0x0A (default is 0 dB)
Channel-4 volume	– 0x0B (default is 0 dB)
Headphone volume	– 0x0C (default is 0 dB)
Channel-6 volume (subwoofer)	– 0x0D (default is 0 dB)

Table 15. Volume Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	24 dB
0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0 dB (default for individual channel volume) (1)**
1	1	1	1	1	1	1	0	–100 dB
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**MUTE (default for master volume); 50% duty cycle at output – SOFT MUTE (1)**

(1) Default values are in **bold**.

VOLUME CONFIGURATION REGISTER (0x0E)

Bit D7:	Reserved = 1
Bit D6:	If 0, then biquad 1 (BQ1) volume compensation part only is disabled (default). If 1, then BQ1 volume compensation is enabled.
Bit D4:	Reserved = 1
Bit D3:	Reserved
Bits D2–D0:	Volume slew rate (Used to control volume change and MUTE ramp rates)

Table 16. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	**Reserved (must be 1)**
–	**0**	–	–	–	–	–	–	**Disable biquad volume compensation (1)**
–	1	–	–	–	–	–	–	Enable biquad volume compensation
–	–	**0**	–	–	–	–	–	**Reserved (1)**
–	–	–	**1**	–	–	–	–	**Reserved (must be 1) (1)**
–	–	–	–	**0**	–	–	–	**Reserved (1)**
–	–	–	–	–	0	0	0	Volume slew 512 steps (44 ms volume ramp time)
–	–	–	–	–	**0**	**0**	**1**	**Volume slew 1024 steps(1) (88 ms volume ramp time)**
–	–	–	–	–	0	1	0	Volume slew 2048 steps (176 ms volume ramp time)
–	–	–	–	–	0	1	1	Volume slew 256 steps (22 ms volume ramp time)
–	–	–	–	–	1	X	X	Reserved

(1) Default values are in **bold**.

MODULATION LIMIT REGISTER (0x10)

Set modulation limit. See the appropriate power stage data sheet for recommended modulation limits.

Table 17. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	LIMIT [DCLKs]	MIN WIDTH [DCLKs]	MODULATION LIMIT
–	–	–	–	–	0	0	0	1	2	99.2%
–	–	–	–	–	0	0	1	2	4	98.4%
–	–	–	–	–	**0**	**1**	**0**	**3**	**6**	**97.7%**
–	–	–	–	–	0	1	1	4	8	96.9%
–	–	–	–	–	1	0	0	5	10	96.1%
–	–	–	–	–	1	0	1	6	12	95.3%
–	–	–	–	–	1	1	0	7	14	94.5%
–	–	–	–	–	1	1	1	8	16	93.8%
0	**0**	**0**	**0**	**0**	–	–	–			**RESERVED**

INTERCHANNEL DELAY REGISTERS (0x11, 0x12, 0x13, 0x14, 0x15, 0x16)

Internal PWM channels 1, 2, 3, 4, 5, and 6 are mapped into registers 0x11, 0x12 ,0x13, 0x14, 0x15, and 0x16.

Table 18. Channel Interchannel Delay Register Format

BITS DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Minimum absolute delay, 0 DCLK cycles, default for channel 0** (1)
	0	1	1	1	1	1	0	0	Maximum positive delay, 31 × 4 DCLK cycles
	1	0	0	0	0	0	0	0	Maximum negative delay, –32 × 4 DCLK cycles
							0	0	Unused bits
SUBADDRESS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Delay = (value) × 4 DCLK cycles**
0x11	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**Default value for channel 1** (1) **-18 (0xB8)**
0x12	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**Default value for channel 2** (1) **24 (0x60)**
0x13	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**Default value for channel 3** (1) **-24 (0xA0)**
0x14	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**Default value for channel 4** (1) **18 (0x48)**
0x15	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**Default value for channel 5** (1) **-3 (0xF4)**
0x16	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**Default value for channel 6** (1) **3 (0x0C)**

(1) Default values are in **bold**.

OFFSET REGISTER (0x17)

The offset register is mapped into 0x17.

Table 19. Channel Offset Register Format

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Minimum absolute offset, 0 DCLK cycles, default for channel 0** (1)
1	1	1	1	1	1	1	1	Maximum absolute offset, 255 DCLK cycles

(1) Default values are in **bold**.

PWM SHUTDOWN GROUP REGISTER (0x19)

Settings of this register determine which PWM channels are active. The default is 0x30 for two BTL output channels and no external subwoofer output. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

Table 20. Shutdown Group Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	0	–	–	–	–	–	Channel 6 does not belong to shutdown group. (1)
–	–	**1**	–	–	–	–	–	**Channel 6 belongs to shut down group.**
–	–	–	0	–	–	–	–	Channel 5 does not belong to shutdown group. (1)
–	–	–	**1**	–	–	–	–	**Channel 5 belongs to shutdown group.**
–	–	–	–	**0**	–	–	–	**Channel 4 does not belong to shutdown group.** (1)
–	–	–	–	1	–	–	–	Channel 4 belongs to shutdown group.
–	–	–	–	–	**0**	–	–	**Channel 3 does not belong to shutdown group.** (1)
–	–	–	–	–	1	–	–	Channel 3 belongs to shutdown group.
–	–	–	–	–	–	**0**	–	**Channel 2 does not belong to shutdown group.** (1)
–	–	–	–	–	–	1	–	Channel 2 belongs to shutdown group.
–	–	–	–	–	–	–	**0**	**Channel 1 does not belong to shutdown group.** (1)
–	–	–	–	–	–	–	1	Channel 1 belongs to shutdown group.

(1) Default values are in **bold**.

START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period when starting up or shutting down channels. The value in this register determines the time for which the PWM inputs switch at 50% duty cycle. This helps reduce pops and clicks at start-up and shutdown.

D7 is used to configure the output stage in a bridge-tied mode or a single-ended mode.

Table 21. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Bridge-tied load (BTL)**
1	–	–	–	–	–	–	–	Single-ended load (SE)
–	–	–	0	0	–	–	–	No 50% duty-cycle start/stop period
–	–	–	0	1	0	0	0	16.5-ms 50% duty-cycle start/stop period
–	–	–	0	1	0	0	1	23.9-ms 50% duty-cycle start/stop period
–	–	–	**0**	**1**	**0**	**1**	**0**	**31.4-ms 50% duty-cycle start/stop period**
–	–	–	0	1	0	1	1	40.4-ms 50% duty-cycle start/stop period
–	–	–	0	1	1	0	0	53.9-ms 50% duty-cycle start/stop period
–	–	–	0	1	1	0	1	70.3-ms 50% duty-cycle start/stop period
–	–	–	0	1	1	1	0	94.2-ms 50% duty-cycle start/stop period
–	–	–	0	1	1	1	1	125.7-ms 50% duty-cycle start/stop period
–	–	–	1	0	0	0	0	164.6-ms 50% duty-cycle start/stop period
–	–	–	1	0	0	0	1	239.4-ms 50% duty-cycle start/stop period
–	–	–	1	0	0	1	0	314.2-ms 50% duty-cycle start/stop period
–	–	–	1	0	0	1	1	403.9-ms 50% duty-cycle start/stop period
–	–	–	1	0	1	0	0	538.6-ms 50% duty-cycle start/stop period
–	–	–	1	0	1	0	1	703.1-ms 50% duty-cycle start/stop period
–	–	–	1	0	1	1	0	942.5-ms 50% duty-cycle start/stop period
–	–	–	1	0	1	1	1	1256.6-ms 50% duty-cycle start/stop period
–	–	–	1	1	0	0	0	1728.1-ms 50% duty-cycle start/stop period
–	–	–	1	1	0	0	1	2513.6-ms 50% duty-cycle start/stop period
–	–	–	1	1	0	1	0	3299.1-ms 50% duty-cycle start/stop period
–	–	–	1	1	0	1	1	4241.7-ms 50% duty-cycle start/stop period
–	–	–	1	1	1	0	0	5655.6-ms 50% duty-cycle start/stop period
–	–	–	1	1	1	0	1	7383.7-ms 50% duty-cycle start/stop period
–	–	–	1	1	1	1	0	9897.3-ms 50% duty-cycle start/stop period
–	–	–	1	1	1	1	1	13,196.4-ms 50% duty-cycle start/stop period

OSCILLATOR TRIM REGISTER (0x1B)

The TAS5705 PWM processor contains an internal oscillator for PLL reference. This reduces system cost because an external reference is not required. Currently, TI recommends a trim resistor value of 18.2 kΩ (1%). This should be connected between OSC_RES and DVSS.

The factory-trim procedure simply enables the factory trim that was previously done at the factory.

Note that trim always must be run following reset of the device.

Oscillator Trim Enable Procedure Example

Write data 0x00 to register 0x1B (enable factory trim).

Table 22. Oscillator Trim Register (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	–	–	–	–	–	–	**Oscillator trim not done (read-only)** (1)
–	1	–	–	–	–	–	–	Oscillator trim done (read-only)
–	–	**0**	**0**	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	–	Select factory trim (Write a 0 to select factory trim; default is 1.)
–	–	–	–	–	–	**1**	–	**Factory trim disabled** (1)
–	–	–	–	–	–	–	**0**	**Reserved** (1)

(1) Default values are in **bold**.

BKND_ERR REGISTER (0x1C)

When a back-end error signal is received ($\overline{\text{BKND\_ERR}}$ = LOW), all the output stages are reset by setting all PWM and VALID signals LOW. Subsequently, the modulator waits approximately for the time listed in Table 23 before initiation of a reset.

Table 23. BKND_ERR Register (0x1C)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	0	0	0	0	Set back-end reset period to 0 ms (Reserved)
–	–	–	–	0	0	0	1	Set back-end reset period to 150 ms (Reserved)
–	–	–	–	**0**	**0**	**1**	**0**	**Set back-end reset period to 299 ms** (1)
–	–	–	–	0	0	1	1	Set back-end reset period to 449 ms
–	–	–	–	0	1	0	0	Set back-end reset period to 598 ms
–	–	–	–	0	1	0	1	Set back-end reset period to 748 ms
–	–	–	–	0	1	1	0	Set back-end reset period to 898 ms
–	–	–	–	0	1	1	1	Set back-end reset period to 1047 ms
–	–	–	–	1	0	0	0	Set back-end reset period to 1197 ms
–	–	–	–	1	0	0	1	Set back-end reset period to 1346 ms
–	–	–	–	1	0	1	0	Set back-end reset period to 1496 ms
–	–	–	–	1	0	1	1	Set back-end reset period to 1496 ms
–	–	–	–	1	1	–	–	Set back-end reset period to 1496 ms

(1) Default values are in **bold**.

INPUT MULTIPLEXER REGISTER (0x20)

The hex value for each nibble is the channel number. For each input multiplexer, any input from SDIN1 or SDIN2 can be mapped to any internal TAS5705 channel.

Table 24. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved = 0x00**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	–	–	–	–	–	–	–	Channel-1 AD mode
1	–	–	–	–	–	–	–	**Channel-1 BD mode** (1)
–	**0**	**0**	**0**	–	–	–	–	**SDIN1-L to channel 1** (1)
–	0	0	1	–	–	–	–	SDIN1-R to channel 1
–	0	1	0	–	–	–	–	SDIN2-L to channel 1
–	0	1	1	–	–	–	–	SDIN2-R to channel 1
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 1
–	1	1	1	–	–	–	–	Reserved
–	–	–	–	0	–	–	–	Channel 2 AD mode
–	–	–	–	**1**	–	–	–	**Channel 2 BD mode** (1)
–	–	–	–	–	0	0	0	SDIN1-L to channel 2
–	–	–	–	–	**0**	**0**	**1**	**SDIN1-R to channel 2** (1)
–	–	–	–	–	0	1	0	SDIN2-L to channel 2
–	–	–	–	–	0	1	1	SDIN2-R to channel 2
–	–	–	–	–	1	0	0	Reserved
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	0	Ground (0) to channel 2
–	–	–	–	–	1	1	1	Reserved

(1) Default values are in **bold**.

Table 24. Input Multiplexer Register (0x20) (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (2)
–	0	0	0	–	–	–	–	SDIN1-L to channel 3
–	0	0	1	–	–	–	–	SDIN1-R to channel 3
–	0	1	0	–	–	–	–	SDIN2-L to channel 3
–	0	1	1	–	–	–	–	SDIN2-R to channel 3
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 3
–	**1**	**1**	**1**	–	–	–	–	**Ch1 (BTL–) to channel 3—BTL pair for channel 1** (2)
–	–	–	–	**0**	–	–	–	**Reserved** (2)
–	–	–	–	–	0	0	0	SDIN1-L to channel 4
–	–	–	–	–	0	0	1	SDIN1-R to channel 4
–	–	–	–	–	0	1	0	SDIN2-L to channel 4
–	–	–	–	–	0	1	1	SDIN2-R to channel 4
–	–	–	–	–	1	0	0	Reserved
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	0	Ground (0) to channel 4
–	–	–	–	–	**1**	**1**	**1**	**Ch2 (BTL–) to channel 4—BTL pair for channel 2** (2)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (2)
–	0	X	X	–	–	–	–	Reserved
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 5
–	**1**	**1**	**1**	–	–	–	–	**Ch6 (BTL–) to channel 5—BTL pair to channel 6**
–	–	–	–	0	–	–	–	Channel 6 AD mode
–	–	–	–	**1**	–	–	–	**Channel 6 BD mode** (2)
–	–	–	–	–	0	0	0	SDIN1-L to channel 6
–	–	–	–	–	0	0	1	SDIN1-R to channel 6
–	–	–	–	–	**0**	**1**	**0**	**SDIN2-L to channel 6** (2)
–	–	–	–	–	0	1	1	SDIN2-R to channel 6
–	–	–	–	–	1	0	0	Reserved
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	0	Ground (0) to channel 6
–	–	–	–	–	1	1	1	Reserved

(2) Default values are in **bold**.

DOWNMIX INPUT MULTIPLEXER REGISTER (0x21)

Bits D31–D16:	Unused
Bits D15–D13:	Reserved
Bit D12:	If 1, selects downmix data L' to DAP internal channel 1 If 0, selects channel 1 data (from input Mux 1) to DAP internal channel 1
Bit D11:	If 1, selects downmix data R' to the DAP internal channel 2 If 0, selects channel 2 data (from input Mux 2) to DAP internal channel 2
Bits D10–D8:	Reserved
Bits D7–D3:	Reserved
Bit D1:	If 1, enable data from input Mux 2 to downmix block If 0, disable data from input Mux 2 to downmix block
Bit D0:	If 1, enable data from input Mux 1 to downmix block If 0, disable data from input Mux 1 to downmix block

Table 25. Downmix Input Multiplexer Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
–	–	–	–	–	–	–	–	Unused
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
–	–	–	–	–	–	–	–	Unused
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**1**	**0**	–	–	–	–	–	**Reserved** (1)
–	–	–	**0**	–	–	–	–	**Enable channel 1 data to channel 1** (1)
–	–	–	1	–	–	–	–	Enable downmix data L' to channel 1
–	–	–	–	**0**	–	–	–	**Enable channel 2 data to channel 2** (1)
–	–	–	–	1	–	–	–	Enable downmix data R' to channel 2
–	–	–	–	–	**0**	–	–	Reserved
–	–	–	–	–	–	0	0	Enable channel 6 data to channel 6
–	–	–	–	–	–	0	1	Enable bass management on channel 6
–	–	–	–	–	–	**1**	**0**	**Enable (L'+R')/2 downmix data on channel 6** (1)
–	–	–	–	–	–	1	1	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	–	Disable data from input multiplexer 2 to downmix block
–	–	–	–	–	–	**1**	–	**Enable data from input multiplexer 2 to downmix block** (1)
–	–	–	–	–	–	–	0	Disable data from input multiplexer 1 to downmix block
–	–	–	–	–	–	–	**1**	**Enable data from input multiplexer 1 to downmix block** (1)

(1) Default values are in **bold**.

AM MODE REGISTER (0x22)

See the *PurePath Digital™ AM Interference Avoidance* application note (SLEA040).

Table 26. AM Mode Register (0x22)

D20	D19	D18	D17	D16	FUNCTION
0	–	–	–	–	**AM mode disabled** (1)
1	–	–	–	–	AM mode enabled
–	**0**	**0**	–	–	**Select sequence 1** (1)
–	0	1	–	–	Select sequence 2
–	1	0	–	–	Select sequence 3
–	1	1	–	–	Select sequence 4
–	–	–	**0**	–	**IF frequency = 455 kHz** (1)
–	–	–	1	–	IF frequency = 262.5 kHz
–	–	–	–	**0**	**Use BCD tuned frequency** (1)
–	–	–	–	1	Use binary tuned frequency

(1) Default values are in **bold**.

Table 27. AM Tuned Frequency Register in BCD Mode

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	X	–	–	–	–	BCD frequency (1000s kHz)
–	–	–	–	X	X	X	X	BCD frequency (100s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	–	–	–	–	BCD frequency (10s kHz)
–	–	–	–	X	X	X	X	BCD frequency (1s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value** (1)

(1) Default values are in **bold**.

OR

Table 28. AM Tuned Frequency Register in Binary Mode

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	X	X	X	Binary frequency
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	Binary frequency
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value** (1)

(1) Default values are in **bold**.

PWM OUTPUT MUX REGISTER (0x25)

This DAP output Mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D30–D25: Selects which PWM channel is output to HPL_PWM and HPR_PWM

Bits D23–D20: Selects which PWM channel is output to OUT_A

Bits D19–D16: Selects which PWM channel is output to OUT_B

Bits D15–D12: Selects which PWM channel is output to OUT_C

Bits D11–D08: Selects which PWM channel is output to OUT_D

Bits D07–D04: Selects which PWM channel is output to SUB_PWM–

Bits D03–D00: Selects which PWM channel is output to SUB_PWM+

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 6 = 0x05.

Table 29. PWM Output Mux Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	**0**	**0**	–	–	–	–	**Multiplex channel 1 to HPL_PWM** (1)
–	0	0	1	–	–	–	–	Multiplex channel 2 to HPL_PWM
–	0	1	0	–	–	–	–	Multiplex channel 3 to HPL_PWM
–	0	1	1	–	–	–	–	Multiplex channel 4 to HPL_PWM
–	1	0	0	–	–	–	–	Multiplex channel 5 to HPL_PWM
–	1	0	1	–	–	–	–	Multiplex channel 6 to HPL_PWM
–	1	1	X	–	–	–	–	Reserved
–	–	–	–	**0**	–	–	–	**Reserved**
–	–	–	–	–	0	0	0	Multiplex channel 1 to HPR_PWM
–	–	–	–	–	**0**	**0**	**1**	**Multiplex channel 2 to HPR_PWM** (1)
–	–	–	–	–	0	1	0	Multiplex channel 3 to HPR_PWM
–	–	–	–	–	0	1	1	Multiplex channel 4 to HPR_PWM
–	–	–	–	–	1	0	0	Multiplex channel 5 to HPR_PWM
–	–	–	–	–	1	0	1	Multiplex channel 6 to HPR_PWM
–	–	–	–	–	1	1	X	Reserved

(1) Default values are in **bold**.

Table 29. PWM Output Mux Register (0x25) (continued)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	**0**	**0**	**0**	–	–	–	–	**Multiplex channel 1 to OUT_A** (2)
0	0	0	1	–	–	–	–	Multiplex channel 2 to OUT_A
0	0	1	0	–	–	–	–	Multiplex channel 3 to OUT_A
0	0	1	1	–	–	–	–	Multiplex channel 4 to OUT_A
0	1	0	0	–	–	–	–	Multiplex channel 5 to OUT_A
0	1	0	1	–	–	–	–	Multiplex channel 6 to OUT_A
0	1	1	X	–	–	–	–	Reserved
1	X	X	X	–	–	–	–	Reserved
–	–	–	–	0	0	0	0	Multiplex channel 1 to OUT_B
–	–	–	–	0	0	0	1	Multiplex channel 2 to OUT_B
–	–	–	–	**0**	**0**	**1**	**0**	**Multiplex channel 3 to OUT_B** (2)
–	–	–	–	0	0	1	1	Multiplex channel 4 to OUT_B
–	–	–	–	0	1	0	0	Multiplex channel 5 to OUT_B
–	–	–	–	0	1	0	1	Multiplex channel 6 to OUT_B
–	–	–	–	0	1	1	X	Reserved
–	–	–	–	1	X	X	X	Reserved

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	–	–	–	–	Multiplex channel 1 to OUT_C
0	**0**	**0**	**1**	–	–	–	–	**Multiplex channel 2 to OUT_C** (2)
0	0	1	0	–	–	–	–	Multiplex channel 3 to OUT_C
0	0	1	1	–	–	–	–	Multiplex channel 4 to OUT_C
0	1	0	0	–	–	–	–	Multiplex channel 5 to OUT_C
0	1	0	1	–	–	–	–	Multiplex channel 6 to OUT_C
0	1	1	X	–	–	–	–	Reserved
1	X	X	X	–	–	–	–	Reserved
–	–	–	–	0	0	0	0	Multiplex channel 1 to OUT_D
–	–	–	–	0	0	0	1	Multiplex channel 2 to OUT_D
–	–	–	–	0	0	1	0	Multiplex channel 3 to OUT_D
–	–	–	–	**0**	**0**	**1**	**1**	**Multiplex channel 4 to OUT_D** (2)
–	–	–	–	0	1	0	0	Multiplex channel 5 to OUT_D
–	–	–	–	0	1	0	1	Multiplex channel 6 to OUT_D
–	–	–	–	0	1	1	X	Reserved
–	–	–	–	1	X	X	X	Reserved

(2) Default values are in **bold**.

Table 29. PWM Output Mux Register (0x25) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	–	–	–	–	Multiplex channel 1 to SUB_PWM–
0	0	0	1	–	–	–	–	Multiplex channel 2 to SUB_PWM–
0	0	1	0	–	–	–	–	Multiplex channel 3 to SUB_PWM–
0	0	1	1	–	–	–	–	Multiplex channel 4 to SUB_PWM–
0	**1**	**0**	**0**	–	–	–	–	**Multiplex channel 5 to SUB_PWM– (3)**
0	1	0	1	–	–	–	–	Multiplex channel 6 to SUB_PWM–
0	1	1	X	–	–	–	–	Reserved
1	X	X	X	–	–	–	–	Reserved
–	–	–	–	0	0	0	0	Multiplex channel 1 to SUB_PWM+
–	–	–	–	0	0	0	1	Multiplex channel 2 to SUB_PWM+
–	–	–	–	0	0	1	0	Multiplex channel 3 to SUB_PWM+
–	–	–	–	0	0	1	1	Multiplex channel 4 to SUB_PWM+
–	–	–	–	0	1	0	0	Multiplex channel 5 to SUB_PWM+
–	–	–	–	**0**	**1**	**0**	**1**	**Multiplex channel 6 to SUB_PWM+ (3)**
–	–	–	–	0	1	1	X	Reserved
–	–	–	–	1	X	X	X	Reserved

(3) Default values are in **bold**.

LOUDNESS BIQUAD GAIN INVERSE REGISTER (0x26)

Bit D6 of the volume configuration register (0x0E) enables/disables gain compensation for BQ1. D6 = 0 disables gain compensation (default); D6 = 1 enables gain compensation. Maximum/minimum biquad gain = ±4.

Table 30. Loudness Biquad Gain Inverse Register (3.23 Format)

CONTENT	DEFINITION
u[31:26], x[25:0]	1/G (1)

(1) G = gain of the biquad

LOUDNESS SCALE REGISTER (0x28)

Table 31. Loudness Scale Register (3.23 Format)

CONTENT	DEFINITION
u[31:26], x[25:0]	Scale = 1/(1 – 1/G) (1)

(1) G = gain of the biquad

DRC CONTROL (0x46)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	**0**	–	–	–	**DRC1 independent of channel 4 (1)**
–	–	–	–	1	–	–	–	DRC1 dependent of channel 4
–	–	–	–	–	**0**	–	–	**DRC1 independent of channel 3 (1)**
–	–	–	–	–	1	–	–	DRC1 dependent of channel 3
–	–	–	–	–	–	**0**	–	**DRC2 (subchannel) turned OFF (1)**
–	–	–	–	–	–	1	–	DRC2 (subchannel) turned ON
–	–	–	–	–	–	–	**0**	**DRC1 (satellite channels) turned OFF (1)**
–	–	–	–	–	–	–	1	DRC1 (satellite channels) turned ON

(1) Default values are in **bold**.

BANK SWITCH AND HEADPHONE DRC/EQ CONTROL (0x50)

Table 32. Bank Switching Command

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
–	–	–	–	–	–	–	–	Reserved
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
–	–	–	–	–	–	–	–	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
–	–	–	–	–	–	–	–	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	–	–	–	–	–	–	–	**EQ disabled in headphone mode** (1)
1	–	–	–	–	–	–	–	EQ enabled in headphone mode
–	**0**	–	–	–	–	–	–	**DRC disabled in headphone mode** (1)
–	1	–	–	–	–	–	–	DRC enabled in headphone mode
–	–	**0**	**0**	**0**	–	–	–	**Reserved**
–	–	–	–	–	**0**	**0**	**0**	**No bank switching. All updates to DAP** (1)
–	–	–	–	–	0	0	1	Configure bank 1 (32 kHz)
–	–	–	–	–	0	1	0	Configure bank 2 (44.1/48 kHz)
–	–	–	–	–	0	1	1	Configure bank 3 (88.2/96 kHz and above)
–	–	–	–	–	1	0	0	Automatic bank selection

(1) Default values are in **bold**.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5705PAP	ACTIVE	HTQFP	PAP	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5705	Samples
TAS5705PAPR	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5705	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

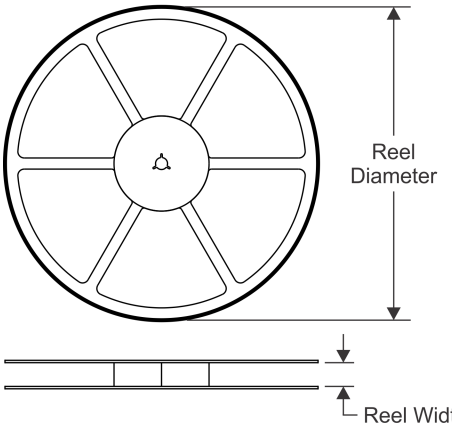
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

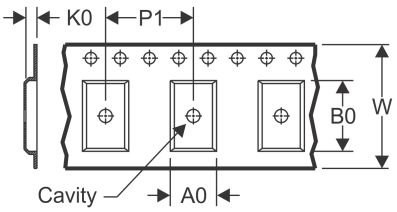
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

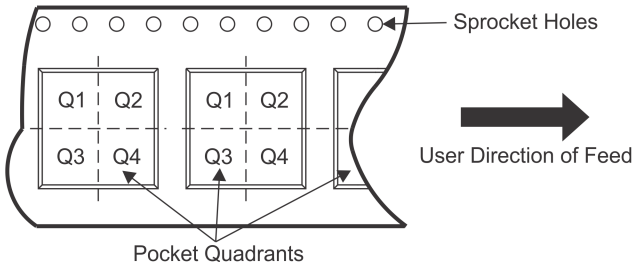


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

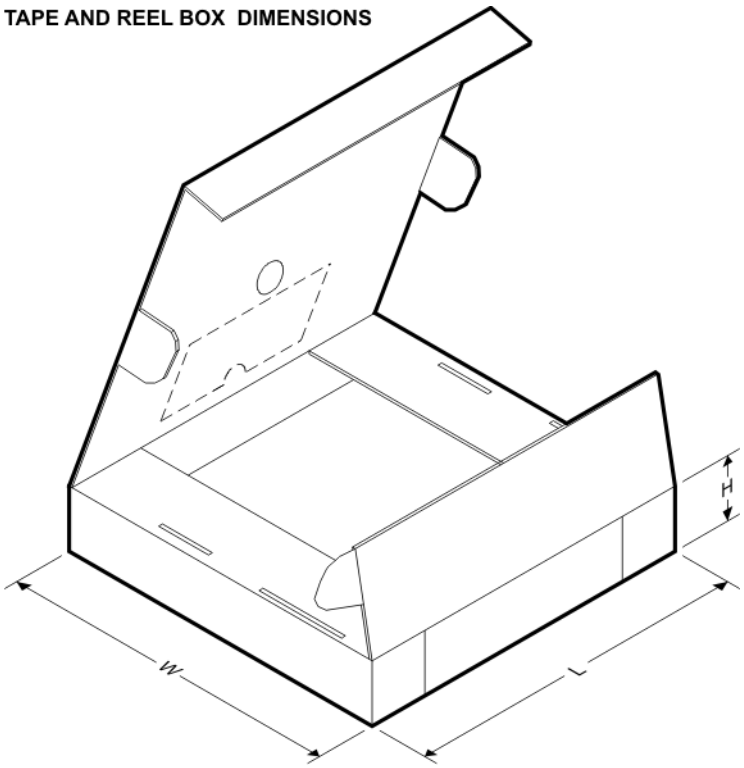
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5705PAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5705PAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

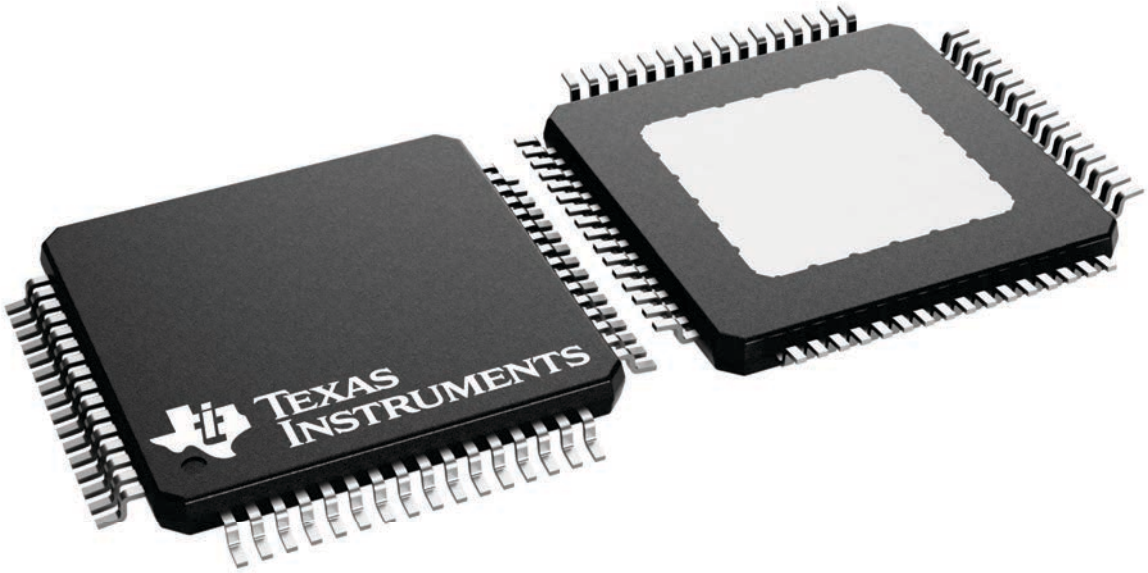
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



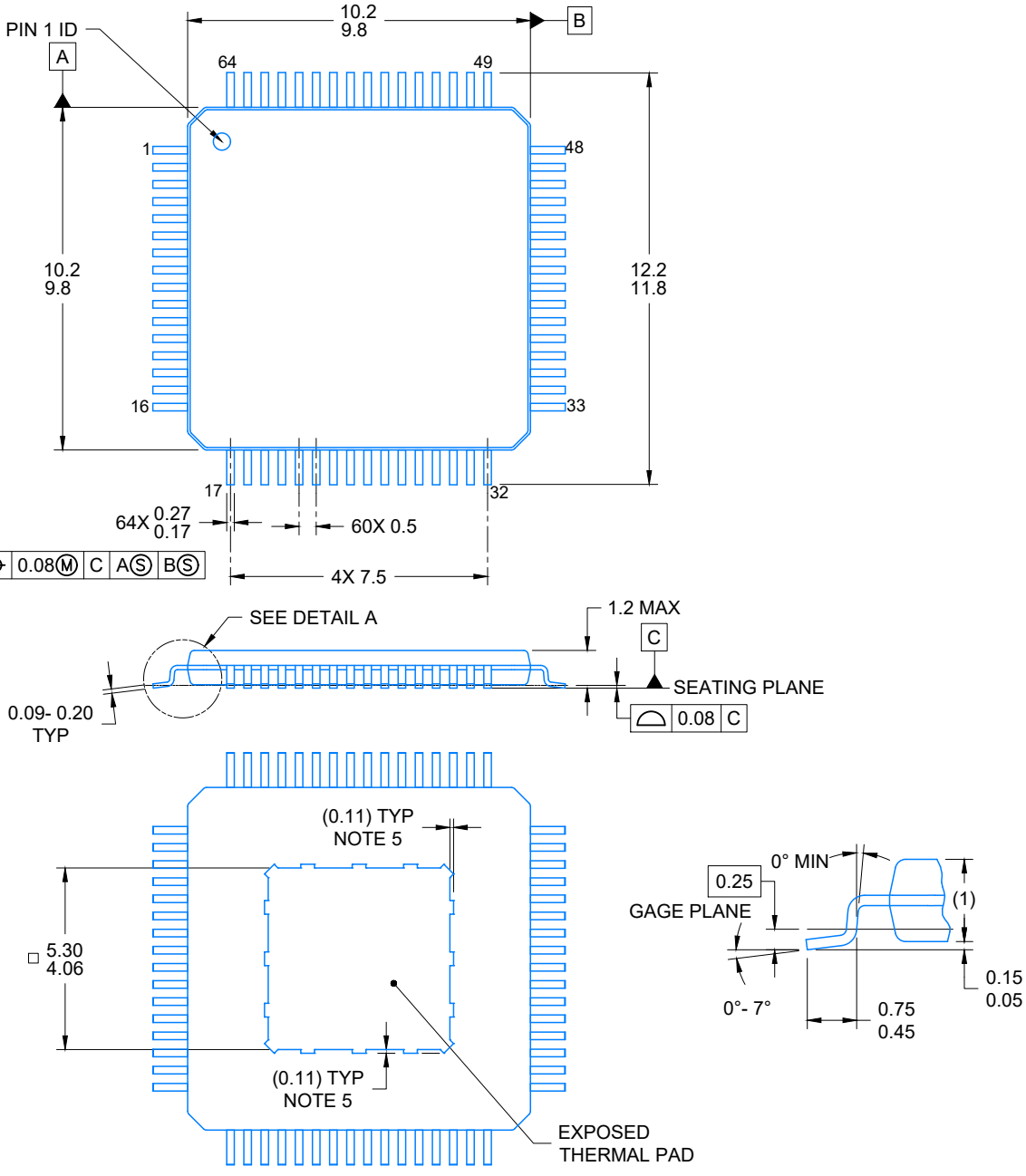
4226442/A

PACKAGE OUTLINE

PAP0064N

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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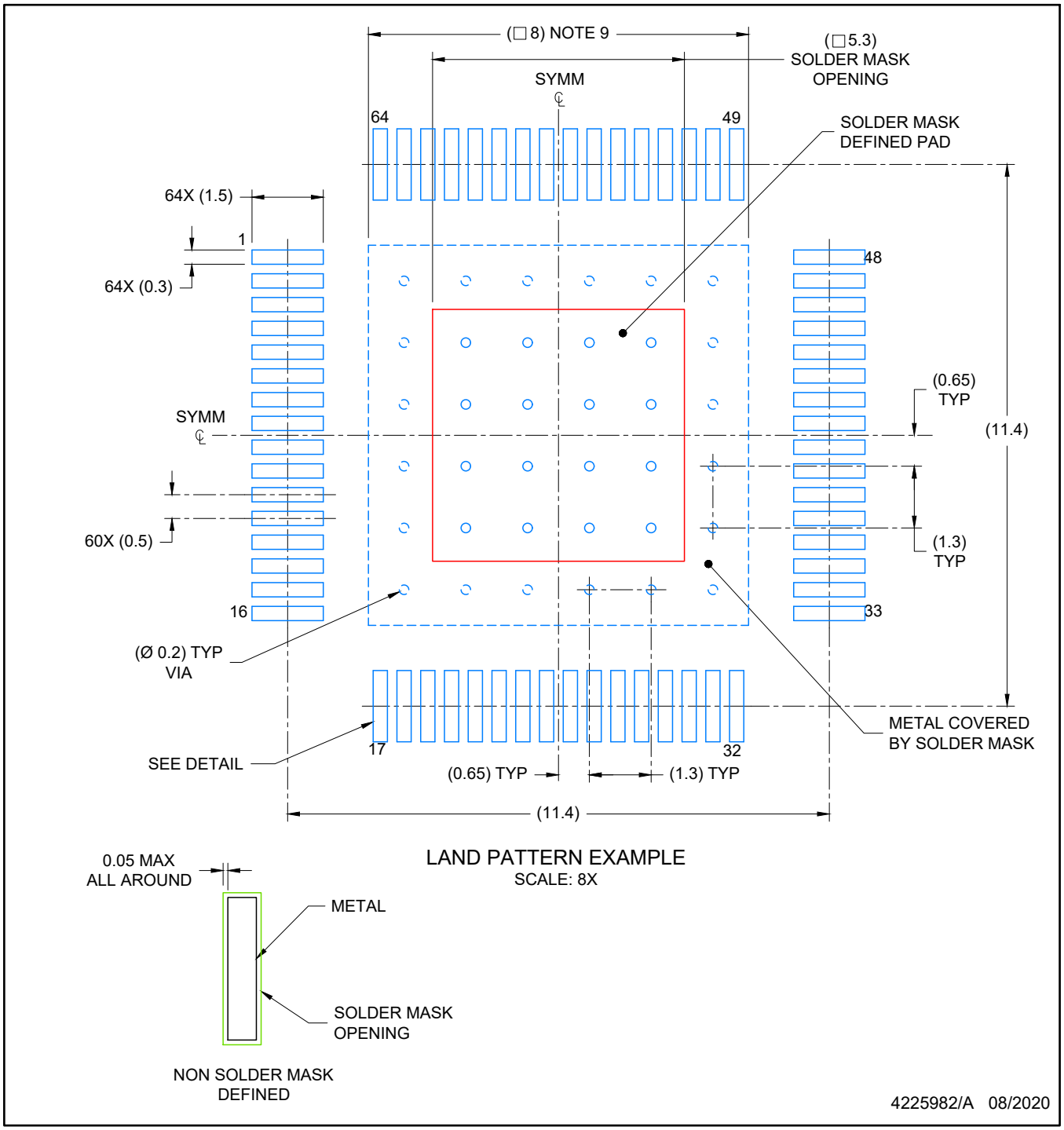
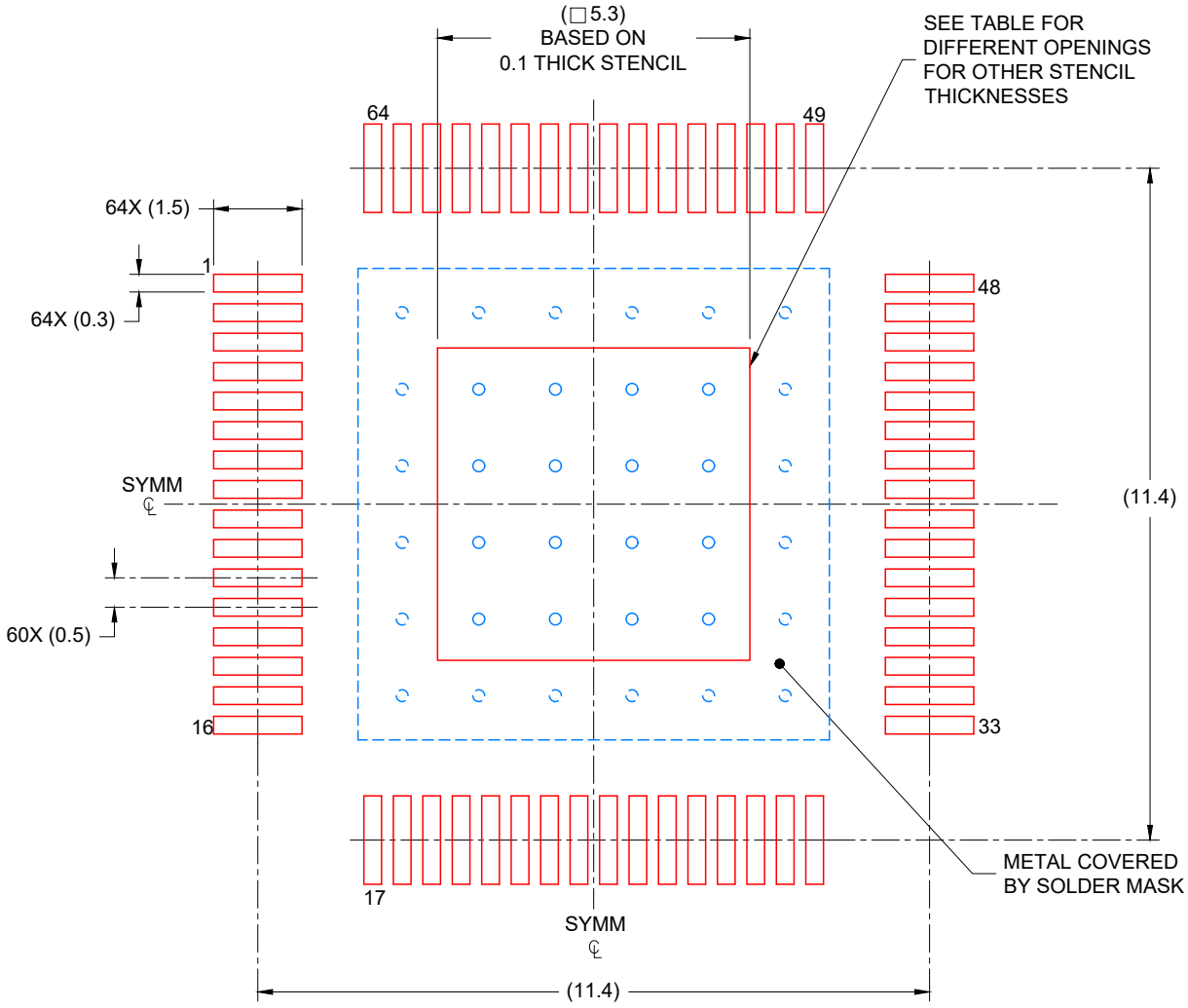
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Strap features may not be present.
6. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED COVERAGE BY AREA
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.3X5.3 (SHOWN)
0.127	4.44 X 4.44
0.152	4.06 X 4.06
0.178	3.75 X 3.75

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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