LM4836 Boomer® Audio Power Amplifier Series Stereo 2W Audio Power Amplifiers with DC Volume Control, Bass Boost, and Input Mux

Check for Samples: LM4836

FEATURES

- **PC98 and PC99 Compliant**
- **DC Volume Control Interface**
- **Input Mux**
- **System Beep Detect**
- **Stereo Switchable Bridged/Single-Ended Power Amplifiers**
- **Selectable Internal/External Gain and Bass Boost Configurable**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection Circuitry**

APPLICATIONS

- **Portable and Desktop Computers**
- **Multimedia Monitors**
- **Portable Radios, PDAs, and Portable TVs**

KEY SPECIFICATIONS

- **P_O at 1% THD+N**
- **Into 3Ω (LM4836LQ, LM4836MTE) 2.2 W (typ)**
- **Into 4Ω (LM4836LQ, LM4836MTE) 2.0 W (typ)**
- **Into 8Ω (LM4836) 1.1 W (typ)**
- **Single-Ended Mode - THD+N at 85 mW Into 32Ω 1.0% (typ)**
- **Shutdown Current 0.2µA (typ)**

DESCRIPTION

The LM4836 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω with less than 1.0% THD+N, or 2.2W into 3Ω with less than 1.0% THD+N (see Notes below).

Boomer audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4836 incorporates a DC volume control, stereo bridged audio power amplifiers, selectable gain or bass boost, and an input mux making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4836 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note: When properly mounted to the circuit board, the LM4836LQ and LM4836MTE will deliver 2W into 4Ω. The LM4836MT will deliver 1.1W into 8Ω. See the APPLICATION INFORMATION section for LM4836LQ and LM4836MTE usage information.

Note: An LM4836LQ and LM4836MTE that have been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Connection Diagram

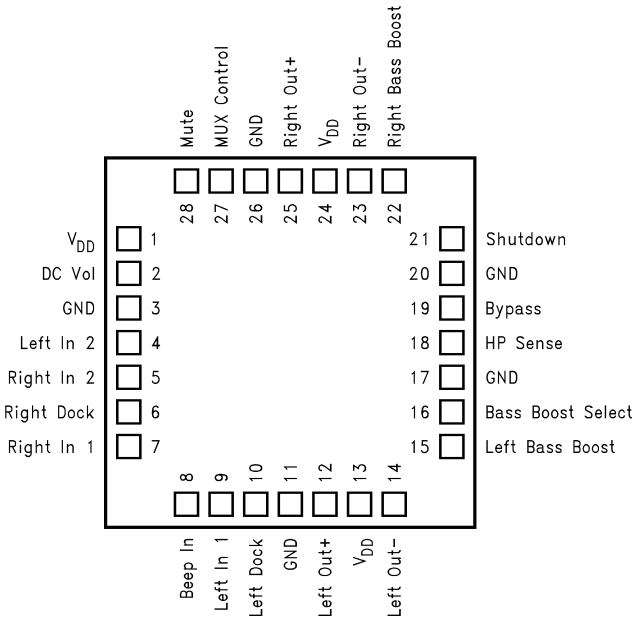


Figure 1. WQFN Package
See Package NJB0028A
for Exposed-DAP WQFN

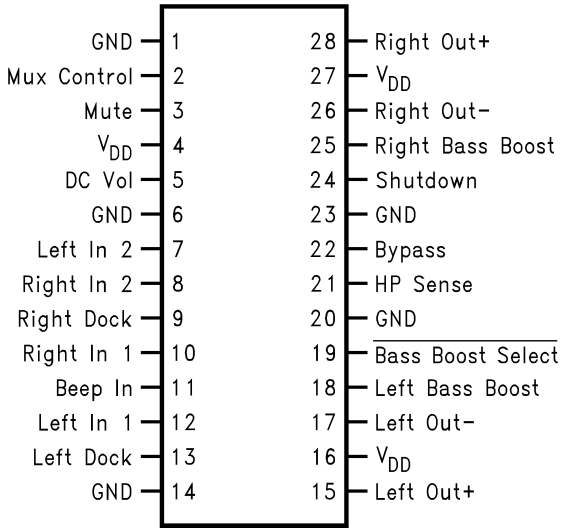


Figure 2. TSSOP Package
See Package PW0028A for TSSOP or
PWP0028A for Exposed-DAP HTSSOP

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2)

Supply Voltage		6.0V
Storage Temperature		-65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation (3)		Internally limited
ESD Susceptibility (4)		2500V
ESD Susceptibility (5)		250V
Junction Temperature		150°C
Soldering Information	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
See http://www.ti.com for other methods of soldering surface mount devices.		
θ_{JC} (typ)—NJB0028A		3.0°C/W
θ_{JA} (typ)—NJB0028A (6)		42°C/W
θ_{JC} (typ)—PW0028A		20°C/W
θ_{JA} (typ)—PW0028A		80°C/W
θ_{JC} (typ)—PWP0028A		2°C/W
θ_{JA} (typ)—PWP0028A (7)		41°C/W
θ_{JA} (typ)—PWP0028A (8)		54°C/W
θ_{JA} (typ)—PWP0028A (9)		59°C/W
θ_{JA} (typ)—PWP0028A (10)		93°C/W

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments' Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4836, T_{JMAX} = 150°C. The typical junction-to-ambient thermal resistance, when board mounted, is 80°C/W for the PW0028A package, 41°C/W for the PWP0028A package, and 42°C/W for the NJB0028A package.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) Machine Model, 220 pF–240 pF discharged through all pins.
(6) The given θ_{JA} is for an LM4836 packaged in an NHW0024A with the exposed-DAP soldered to an exposed $2in^2$ area of 1oz printed circuit board copper.
(7) The θ_{JA} given is for a PWP0028A package whose exposed-DAP is soldered to a $2in^2$ piece of 1 ounce printed circuit board copper on a bottom side layer through 21 8mil vias.
(8) The θ_{JA} given is for a PWP0028A package whose exposed-DAP is soldered to an exposed $2in^2$ piece of 1 ounce printed circuit board copper.
(9) The θ_{JA} given is for a PWP0028A package whose exposed-DAP is soldered to an exposed $1in^2$ piece of 1 ounce printed circuit board copper.
(10) The θ_{JA} given is for a PWP0028A package whose exposed-DAP is not soldered to any copper.

OPERATING RATINGS

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤TA ≤ 85°C
Supply Voltage		2.7V≤ V_{DD} ≤ 5.5V

ELECTRICAL CHARACTERISTICS FOR ENTIRE IC(1) (2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (3)	Limit (4)	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	15	30	mA (max)
I_{SD}	Shutdown Current	$V_{pin\ 24} = V_{DD}$	0.2	2.0	µA (max)
V_{IH}	Headphone Sense High Input Voltage			4	V (min)
V_{IL}	Headphone Sense Low Input Voltage			0.8	V (max)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 71.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS FOR VOLUME ATTENUATORS(1) (2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (3)	Limit (4)	
C_{RANGE}	Attenuator Range	Gain with $V_{pin\ 5} \geq 4.5V$	0	±0.5	dB (max)
			0	−1.0	dB (min)
C_{RANGE}	Attenuator Range	Attenuation with $V_{pin\ 5}$ = 0V	-73	-70	dB (min)
A_M	Mute Attenuation	$V_{pin\ 3}$ = 5V, Bridged Mode	-88	-80	dB (min)
		$V_{pin\ 3}$ = 5V, Single-Ended Mode	-80	-70	dB (min)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 71.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED MODE OPERATION(1) (2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (3)	Limit (4)	
P_O	Output Power	THD+N = 1.0%; f = 1kHz; R_L = 32Ω	85		mW
		THD+N = 10%; f = 1 kHz; R_L = 32Ω	95		mW
THD+N	Total Harmonic Distortion+Noise	V_{OUT} = 1V_{RMS}, f=1kHz, R_L = 10kΩ, A_{VD} = 1	0.065		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f =120 Hz, V_{RIPPLE} = 200 mVrms	58		dB
SNR	Signal to Noise Ratio	P_{OUT} =75 mW, R_L = 32Ω, A-Wtd Filter	102		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	65		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 71.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS FOR BRIDGED MODE OPERATION(1) (2)

The following specifications apply for V_{DD} = 5V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LM4836		Units (Limits)
			Typical (3)	Limit (4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	10	50	mV (max)
P_O	Output Power	THD + N = 1.0%; f=1kHz; R_L = 3Ω (5) (6)	2.2		W
		THD + N = 1.0%; f=1kHz; R_L = 4Ω (7) (6)	2		W
		THD = 1.5% (max);f = 1 kHz; R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%;f = 1 kHz; R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	P_O = 1W, 20 Hz< f < 20 kHz, R_L = 8Ω, A_{VD} = 2	0.3		%
		P_O = 340 mW, R_L = 32Ω	1.0		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f = 120 Hz, V_{RIPPLE} = 200 mVrms; R_L = 8Ω	74		dB
SNR	Signal to Noise Ratio	V_{DD} = 5V, P_{OUT} = 1.1W, R_L = 8Ω, A-Wtd Filter	93		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	70		dB

(1) All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in Figure 71.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) When driving 3Ω loads and operating on a 5V supply the LM4836MTE exposed DAP must be soldered to the circuit board and forced-air cooled.
(6) When driving 3Ω or 4Ω loads and operating on a 5V supply, the LM4836LQ must be mounted to the circuit board that has a minimum of 2.5in^2 of exposed, uninterrupted copper area connected to the WQFN package's exposed DAP.
(7) When driving 4Ω loads and operating on a 5V supply the LM4836MTE exposed DAP must be soldered to the circuit board.

TYPICAL APPLICATION

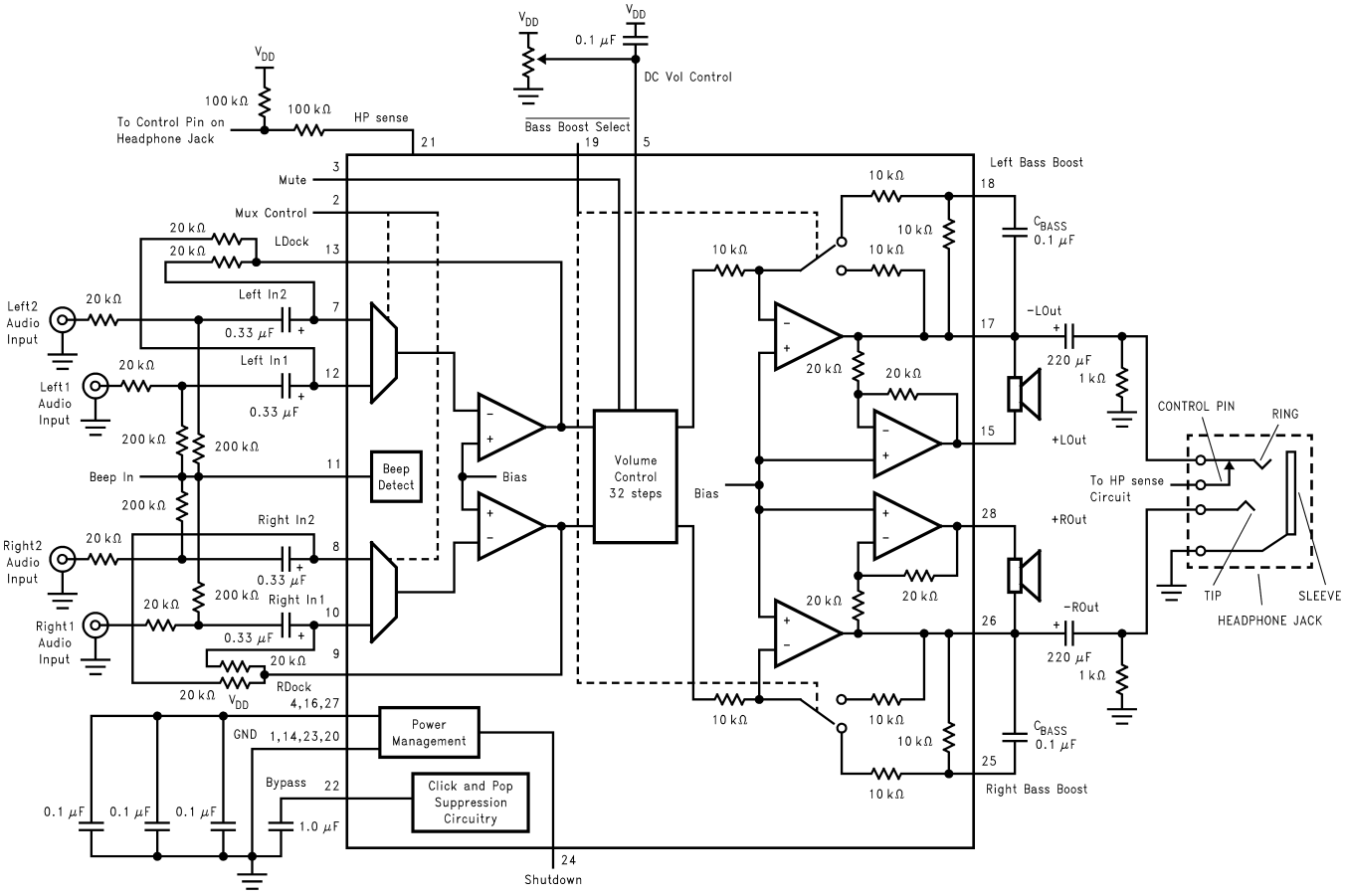


Figure 3. Typical Application Circuit

TRUTH TABLE FOR LOGIC INPUTS (1)

Mute	Mux Control	HP Sense	Inputs Selected	Bridged Output	Single-Ended Output
0	0	0	Left In 1, Right In 1	Vol. Adjustable	-
0	0	1	Left In 1, Right In 1	Muted	Vol. Adjustable
0	1	0	Left In 2, Right In 2	Vol. Adjustable	-
0	1	1	Left In 2, Right In 2	Muted	Vol. Adjustable
1	X	X	-	Muted	Muted

(1) If system beep is detected on the Beep in pin (pin 11) and beep is fed to inputs, the system beep will be passed through the bridged amplifier regardless of the logic of the Mute, HP sense, or DC Volume Control pins.

TYPICAL PERFORMANCE CHARACTERISTICS MTE SPECIFIC CHARACTERISTICS

LM4836MTE THD+N vs Output Power

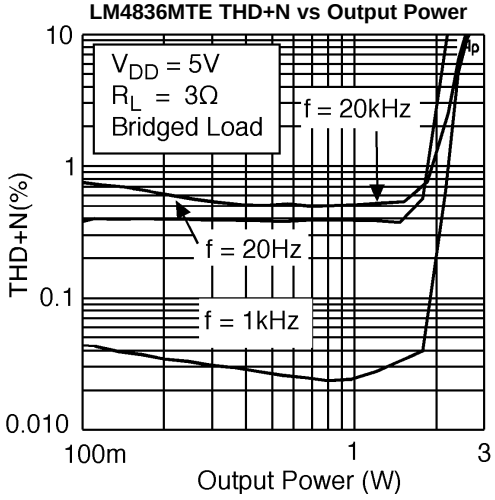


Figure 4.

LM4836MTE THD+N vs Frequency

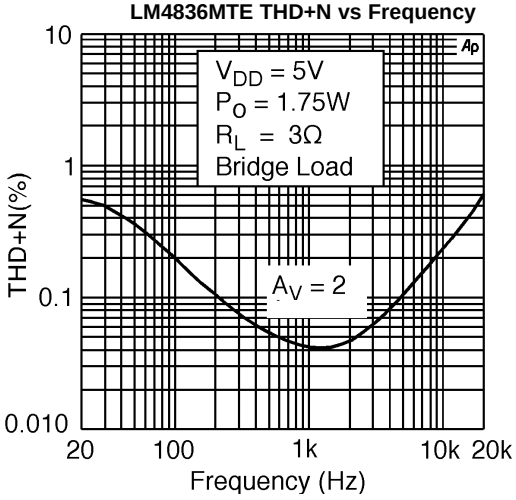


Figure 5.

LM4836MTE THD+N vs Output Power

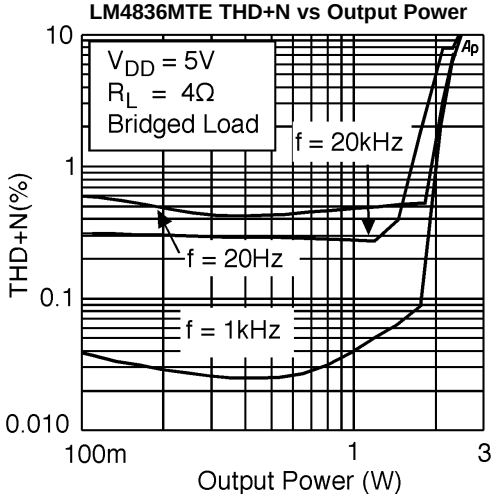


Figure 6.

LM4836MTE THD+N vs Frequency

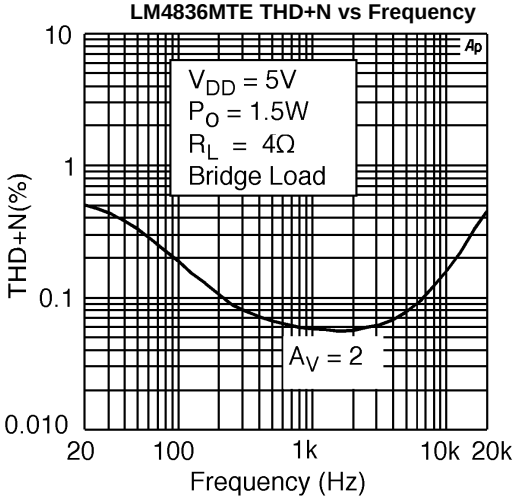


Figure 7.

LM4836MTE Power Dissipation vs Output Power

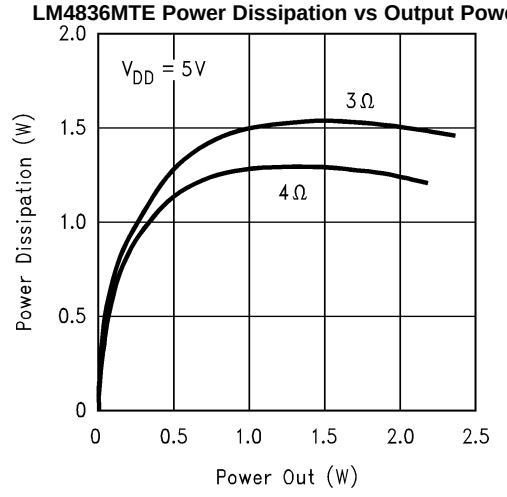


Figure 8.

LM4836LQ Power Derating Curve

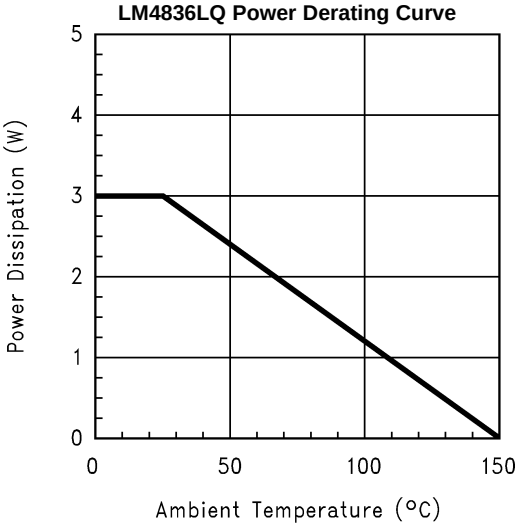


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS MTE SPECIFIC CHARACTERISTICS (continued)

LM4836MTE Power Derating Curve

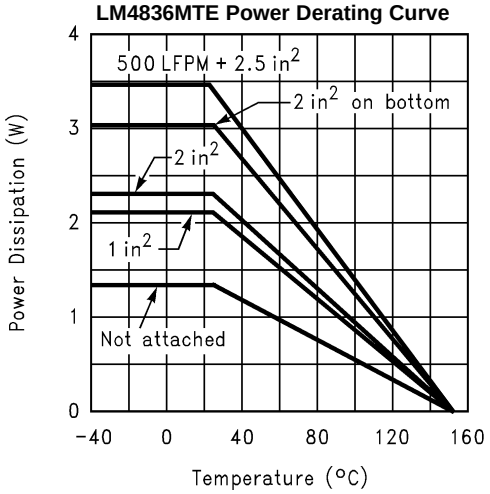


Figure 10 shows the thermal dissipation ability of the LM4836MTE at different ambient temperatures given these conditions: 500LFPM + 2in^2: The part is soldered to a 2in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it. 2in^{2}on bottom: The part is soldered to a 2in^2, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias. 2in^2: The part is soldered to a 2in^2, 1oz. copper plane. 1in^2: The part is soldered to a 1in^2, 1oz. copper plane. Not Attached: The part is not soldered down and is not forced-air cooled.

Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS

THD+N Vs Frequency

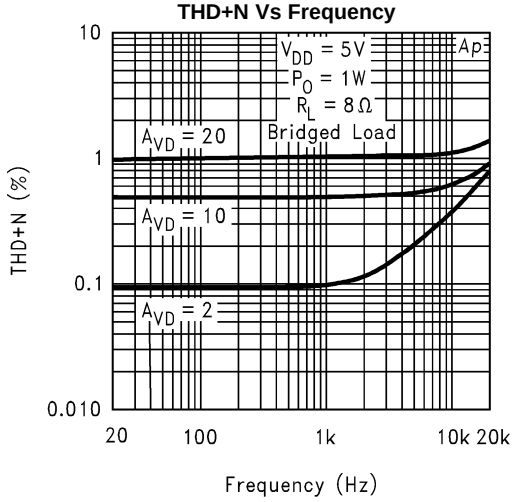


Figure 11.

THD+N Vs Frequency

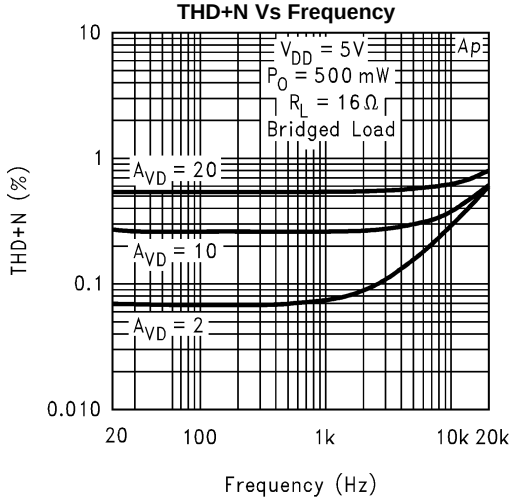


Figure 12.

THD+N Vs Frequency

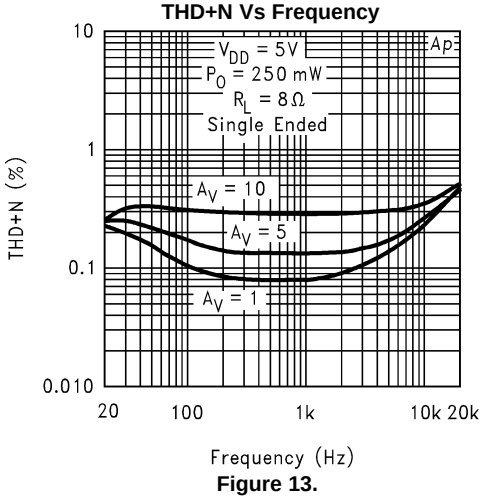


Figure 13.

THD+N Vs Frequency

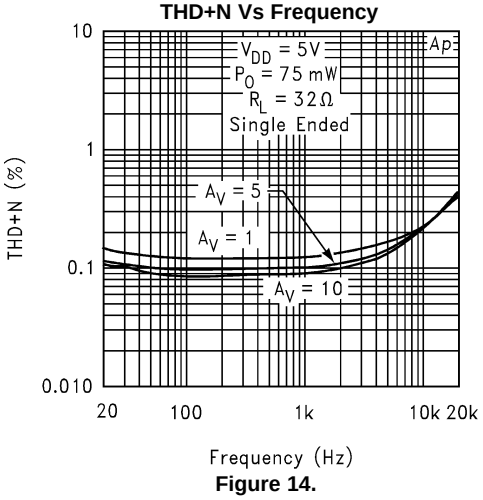


Figure 14.

THD+N Vs Frequency

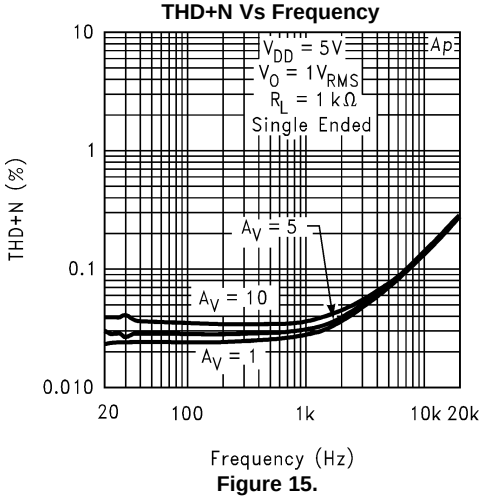


Figure 15.

THD+N Vs Frequency

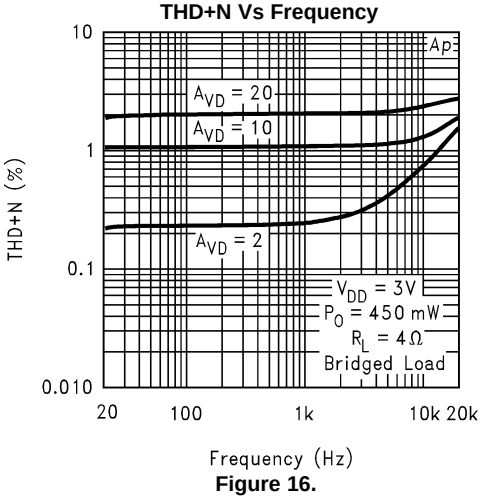


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

THD+N Vs Frequency

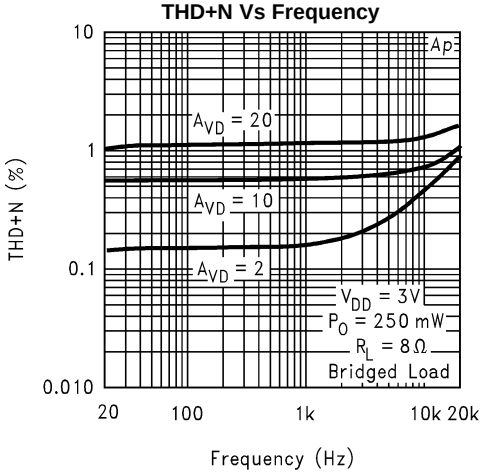


Figure 17.

THD+N Vs Frequency

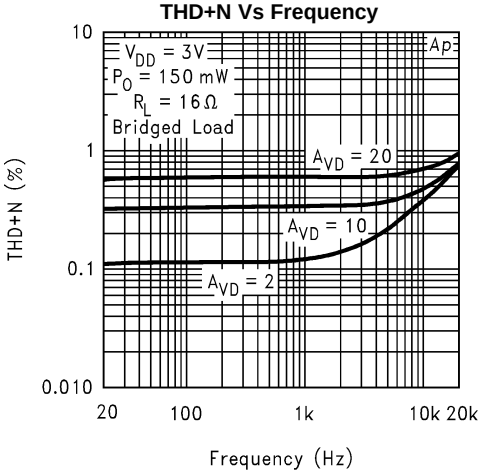


Figure 18.

THD+N Vs Frequency

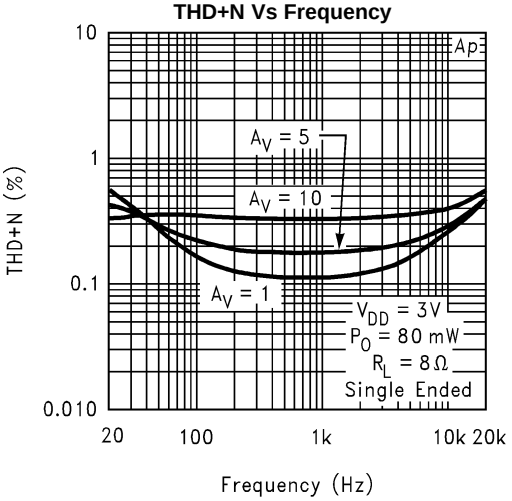


Figure 19.

THD+N Vs Frequency

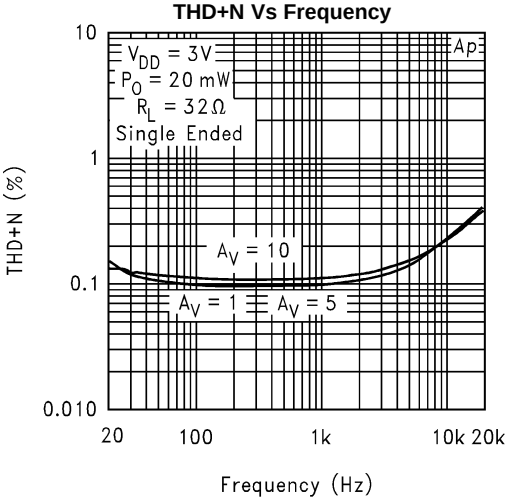


Figure 20.

THD+N Vs Frequency

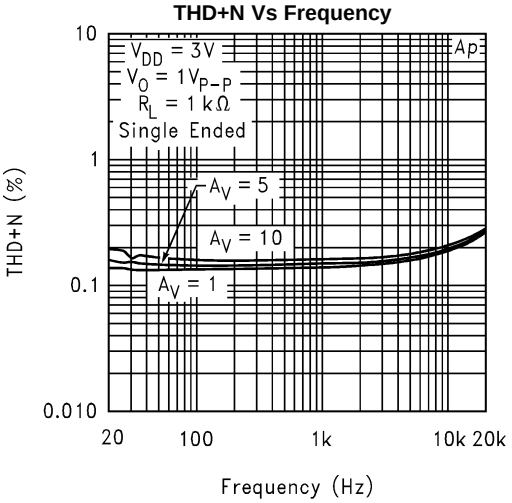


Figure 21.

THD+N Vs Output Power

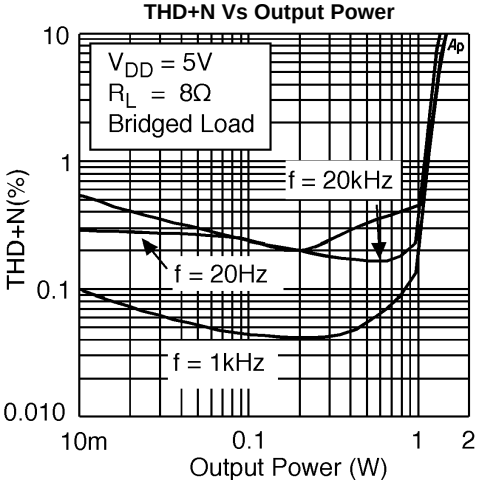


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

THD+N Vs Output Power

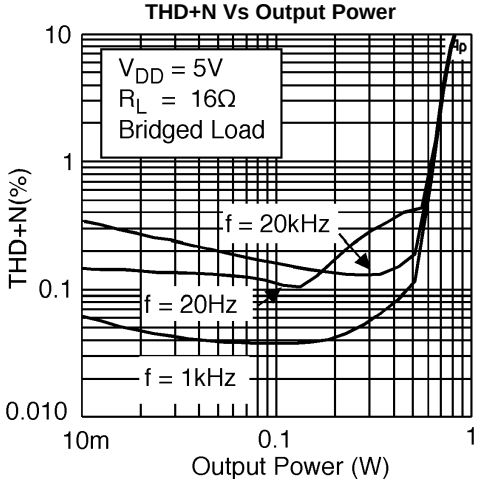


Figure 23.

THD+N Vs Output Power

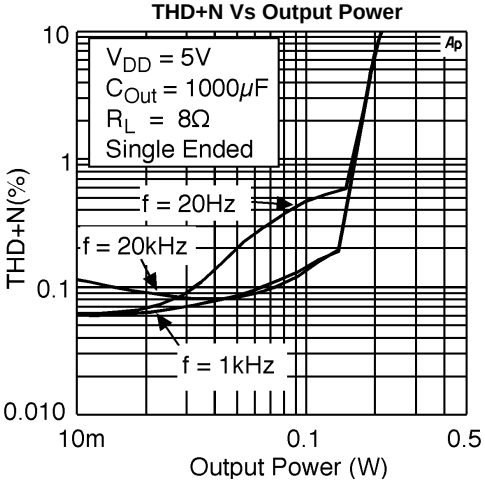


Figure 24.

THD+N Vs Output Power

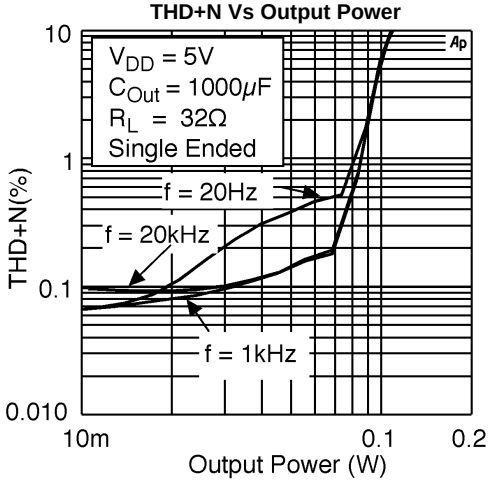


Figure 25.

THD+N Vs Output Power

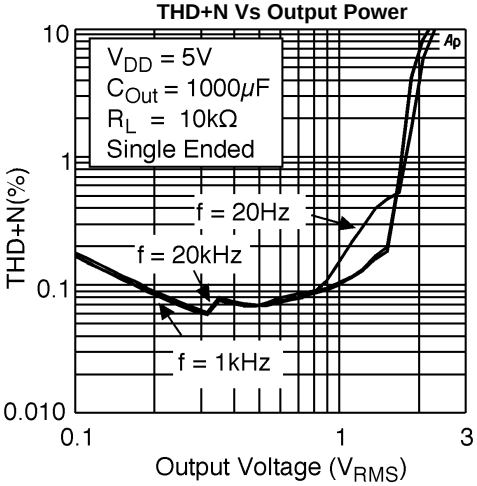


Figure 26.

THD+N vs Output Power

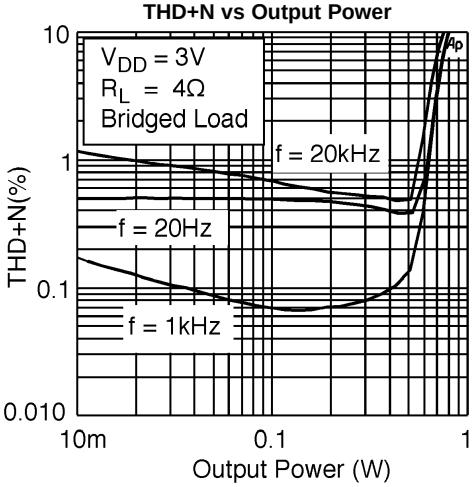


Figure 27.

THD+N Vs Output Power

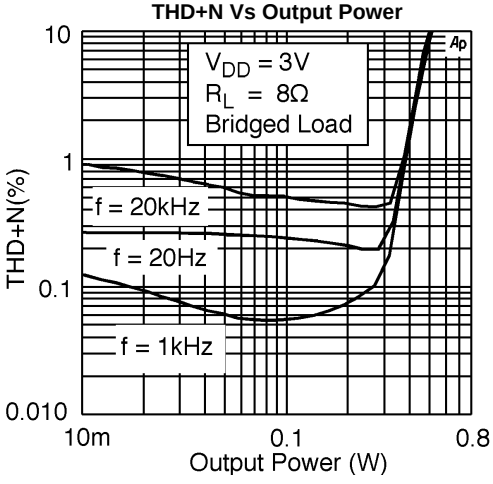


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

THD+N Vs Output Power

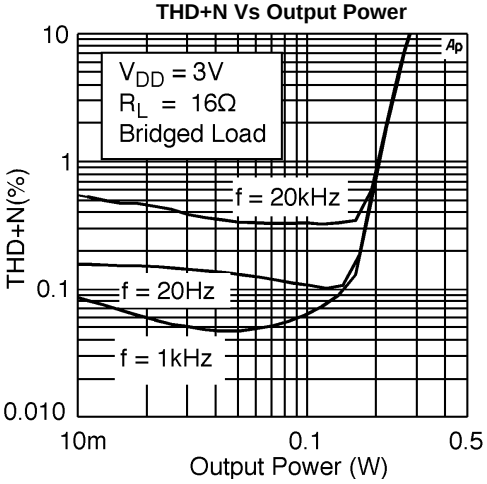


Figure 29.

THD+N Vs Output Power

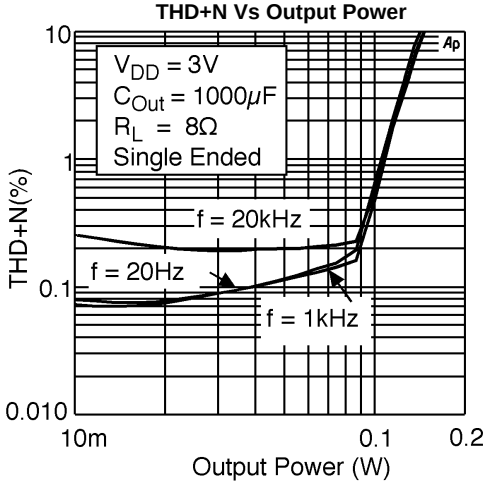


Figure 30.

THD+N Vs Output Power

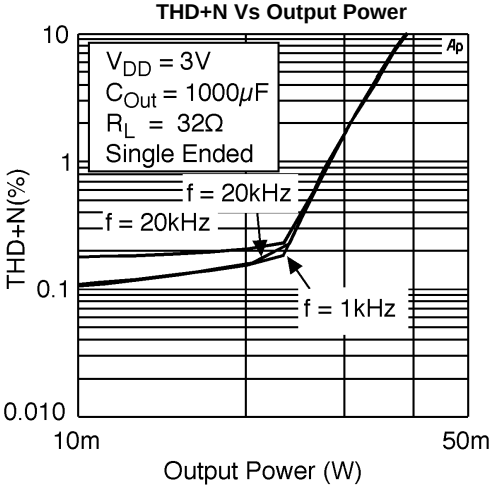


Figure 31.

THD+N Vs Output Power

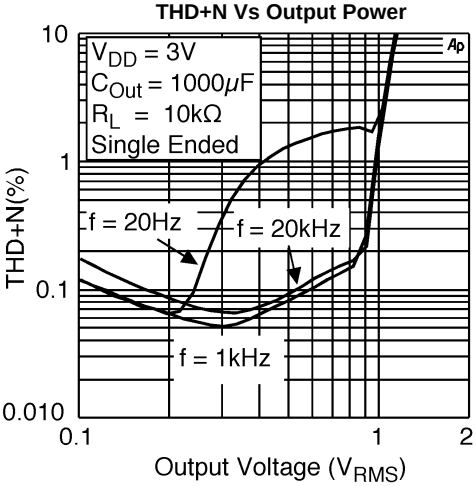


Figure 32.

THD+N Vs Output Voltage Docking Station Pins

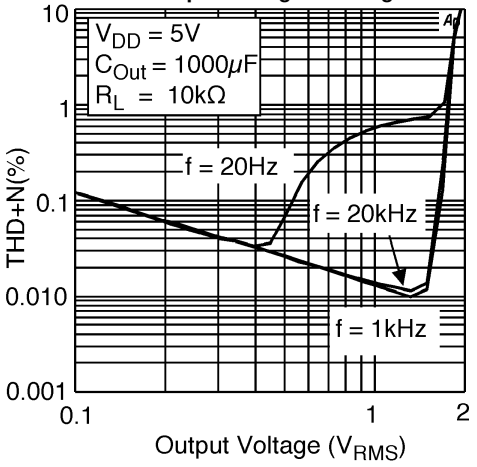


Figure 33.

THD+N Vs Output Voltage Docking Station Pins

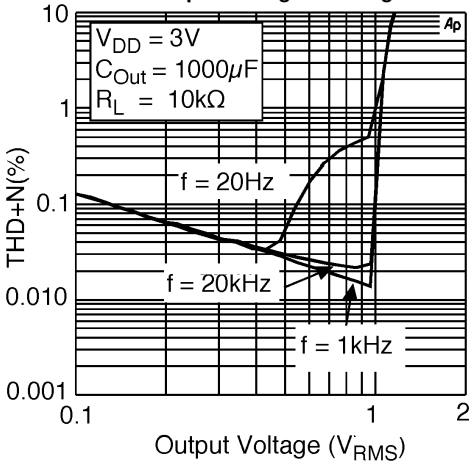


Figure 34.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

Output Power Vs Load Resistance

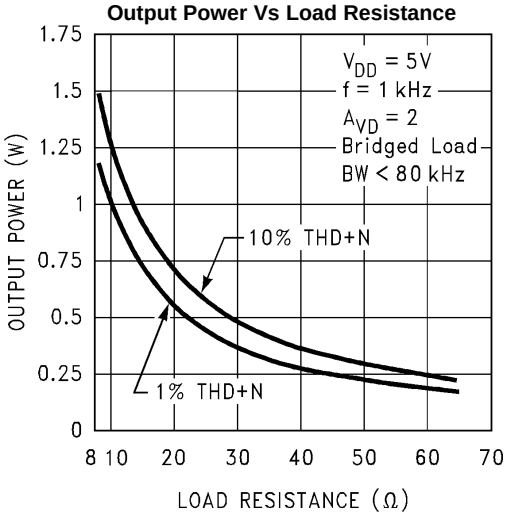


Figure 35.

Output Power Vs Load Resistance

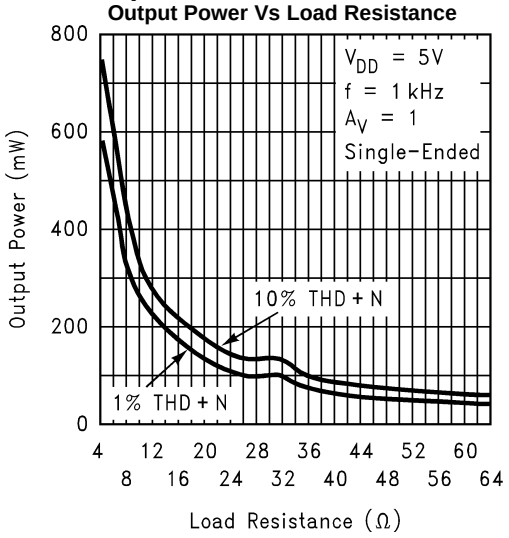


Figure 36.

Output Power Vs Load Resistance

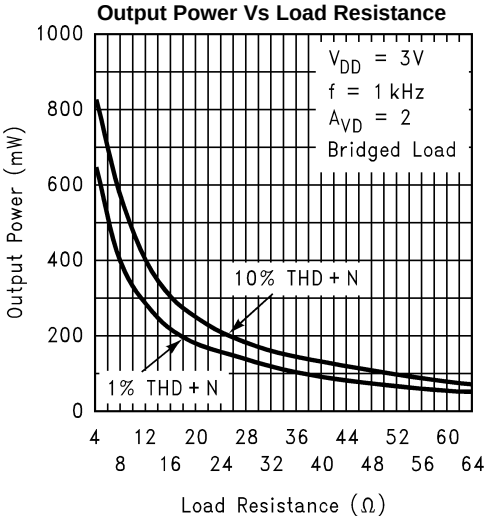


Figure 37.

Power Supply Rejection Ratio

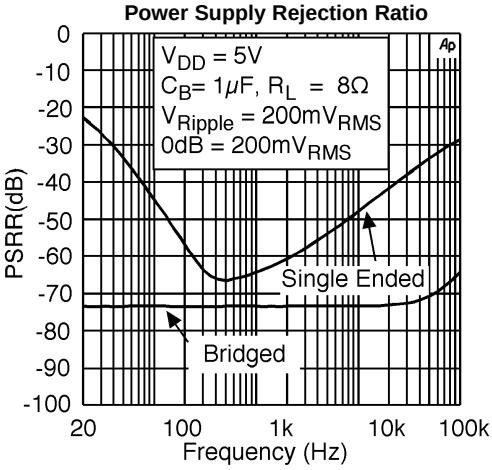


Figure 38.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

Dropout Voltage

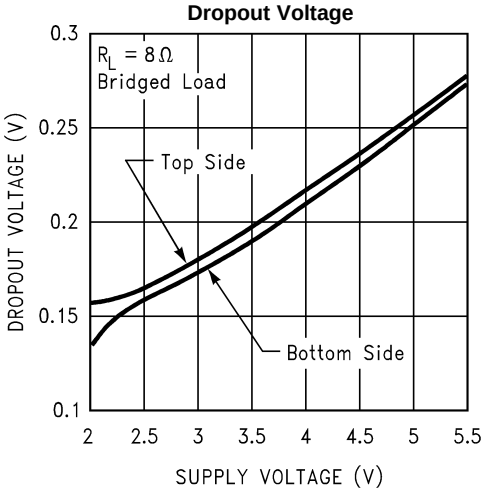


Figure 39.

Output Power Vs Load Resistance

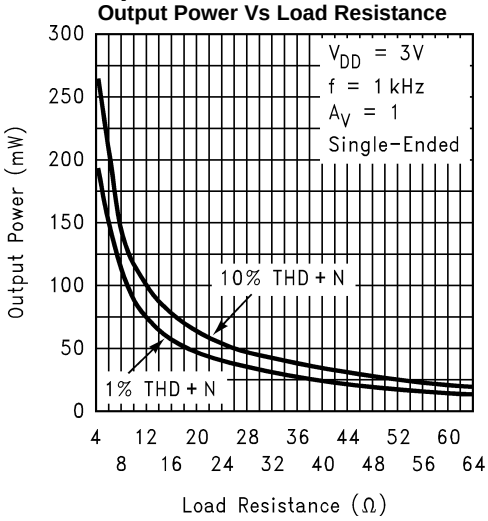


Figure 40.

Noise Floor

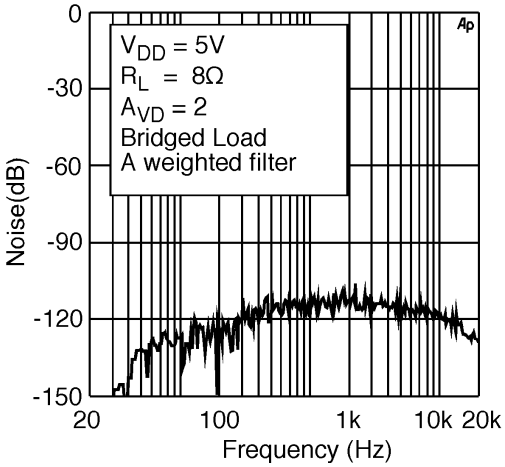


Figure 41.

Noise Floor

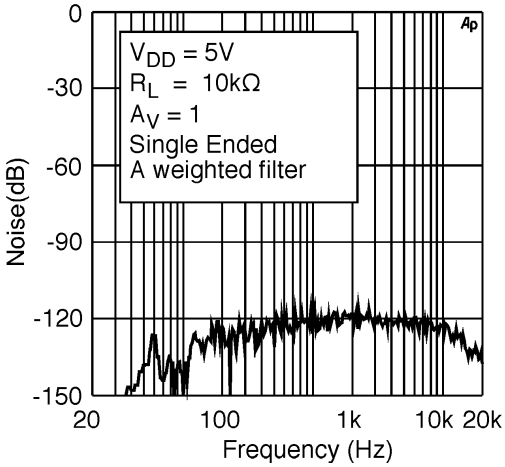


Figure 42.

Volume Control Characteristics

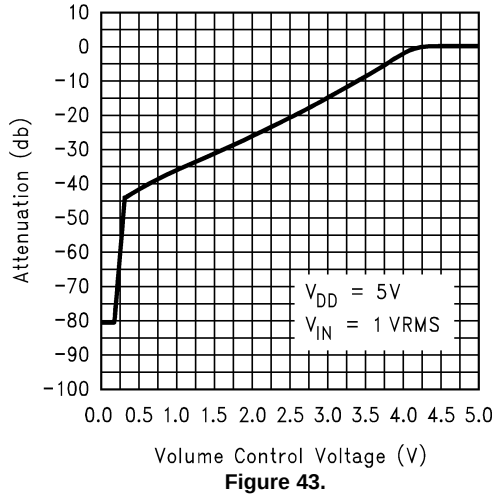


Figure 43.

Power Dissipation Vs Output Power

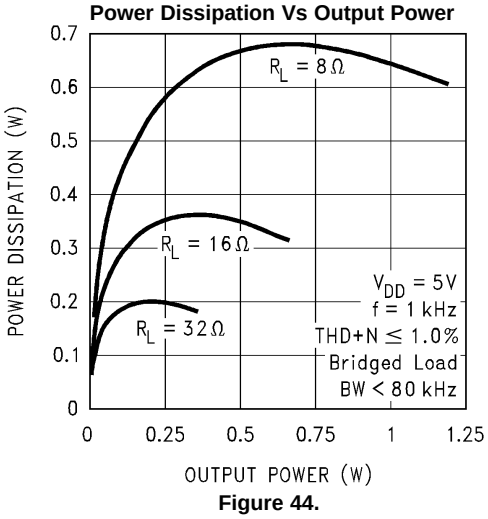


Figure 44.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

Power Dissipation Vs Output Power

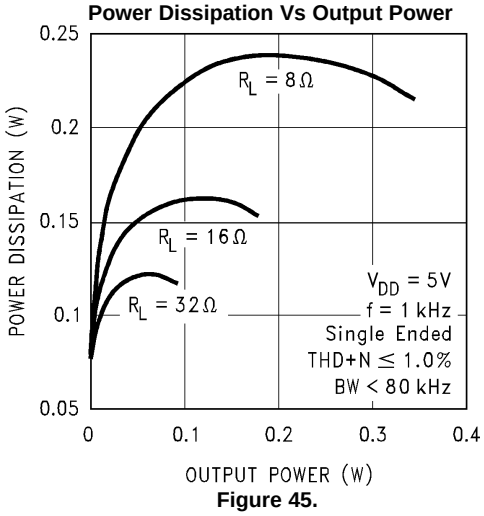


Figure 45.

External Gain/ Bass Boost Characteristics

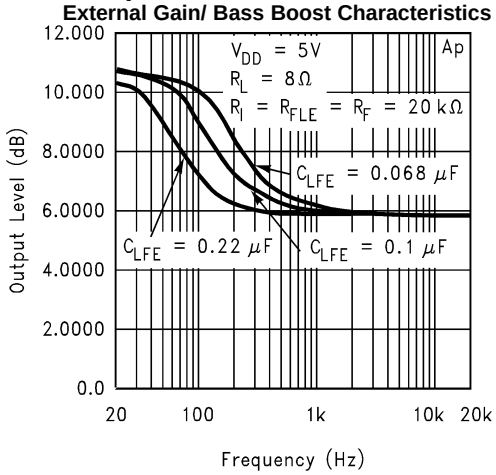


Figure 46.

Power Derating Curve

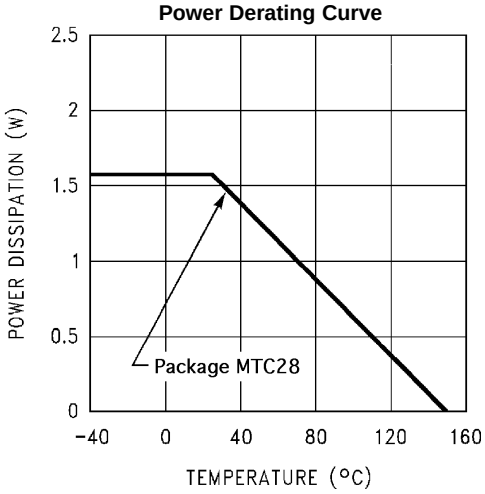


Figure 47.

Crosstalk

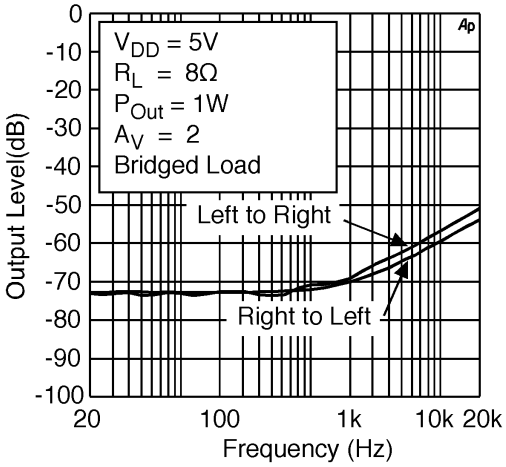


Figure 48.

Crosstalk

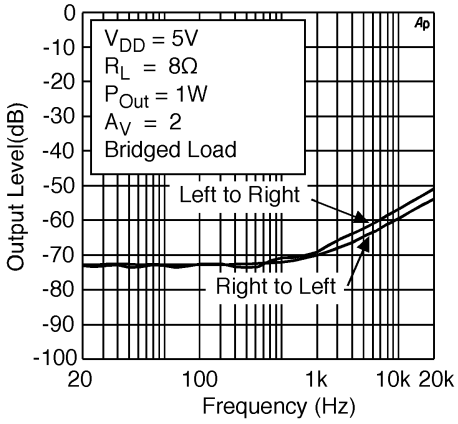


Figure 49.

Output Power Vs Supply Voltage

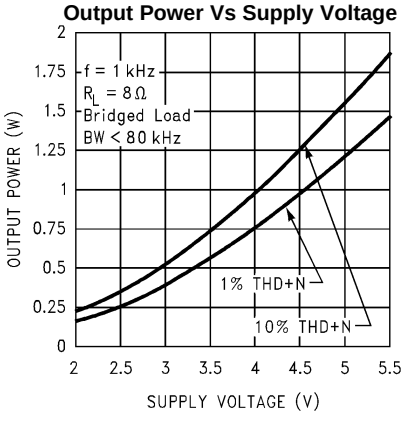


Figure 50.

TYPICAL PERFORMANCE CHARACTERISTICS NON-MTE SPECIFIC CHARACTERISTICS (continued)

Output Power Vs Supply Voltage

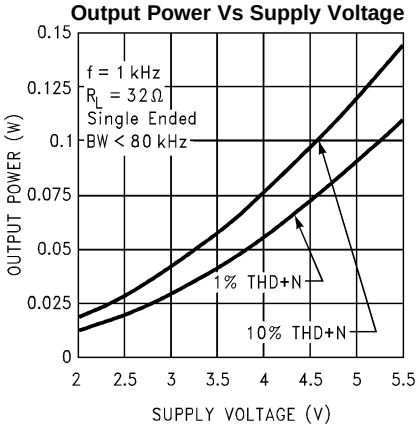


Figure 51.

Supply Current Vs Supply Voltage

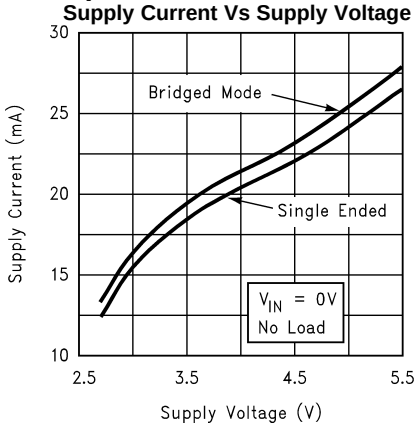


Figure 52.

TYPICAL PERFORMANCE CHARACTERISTICS

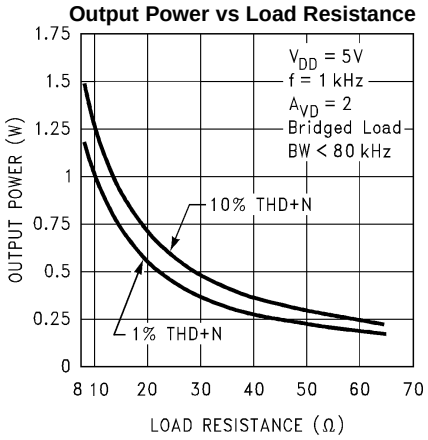


Figure 53.

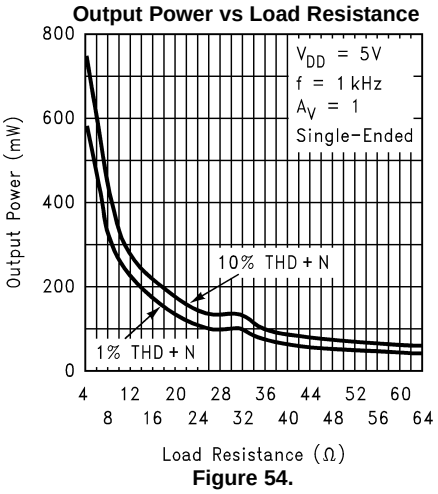


Figure 54.

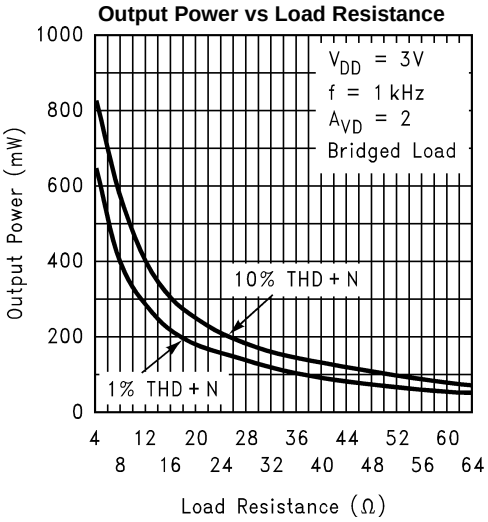


Figure 55.

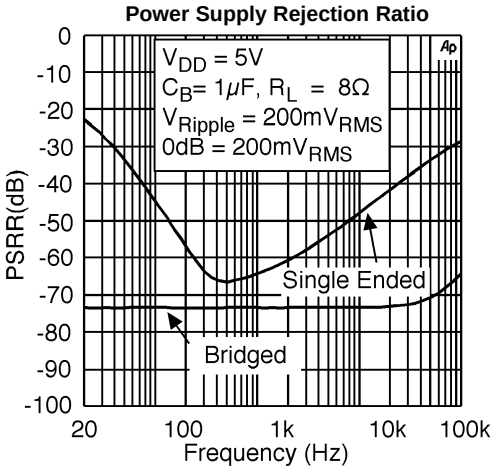


Figure 56.

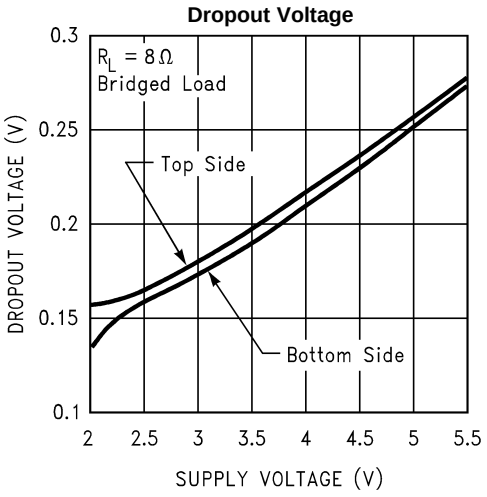


Figure 57.

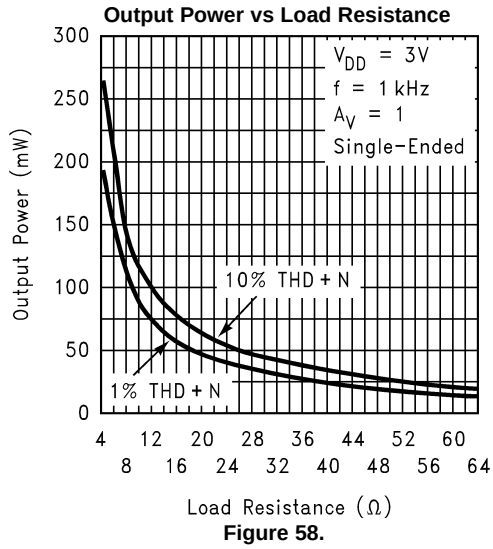


Figure 58.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Noise Floor

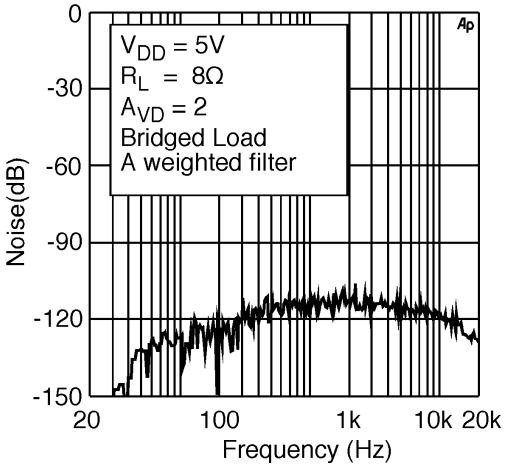


Figure 59.

Noise Floor

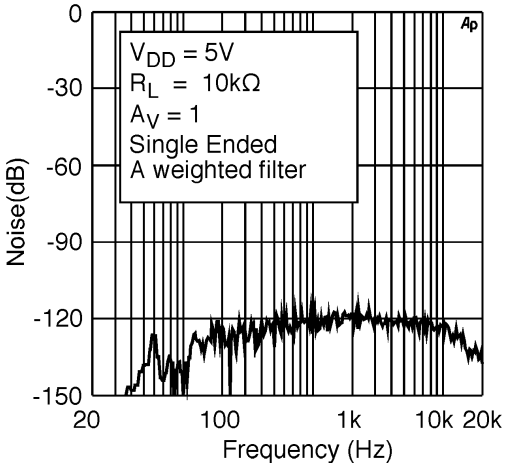


Figure 60.

Volume Control Characteristics

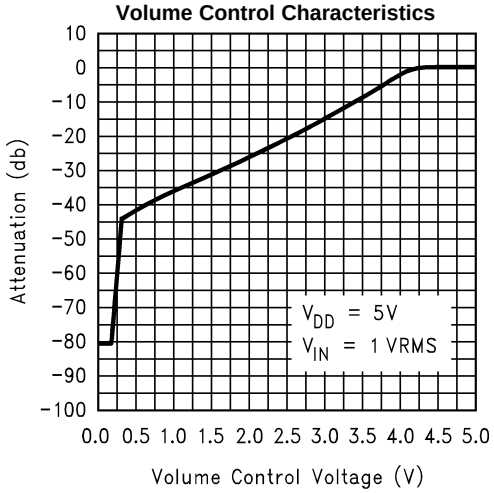


Figure 61.

Power Dissipation vs Output Power

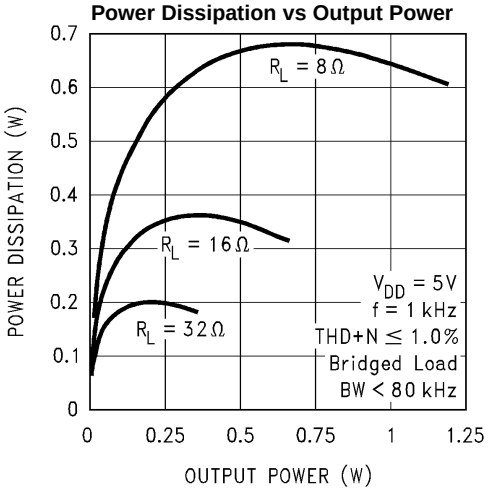


Figure 62.

Power Dissipation vs Output Power

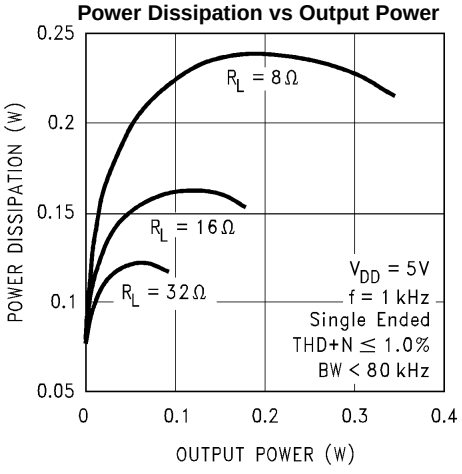


Figure 63.

External Gain/ Bass Boost Characteristics

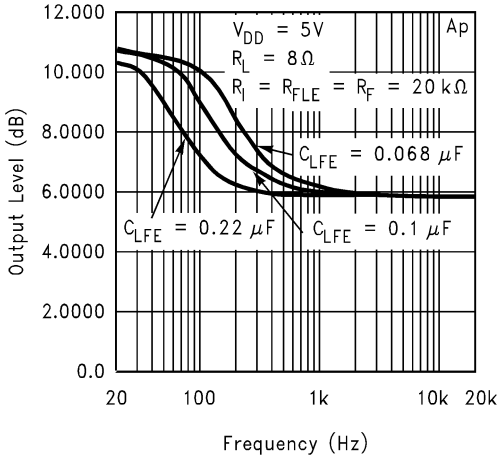


Figure 64.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Derating Curve

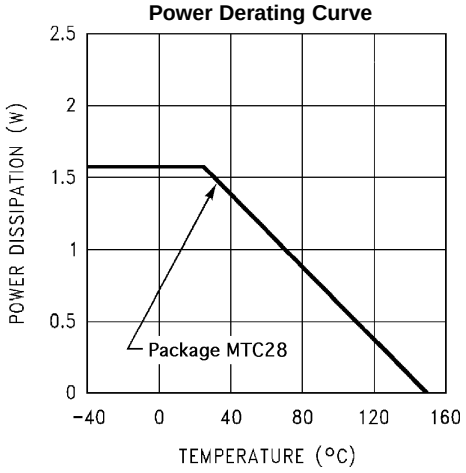


Figure 65.

Crosstalk

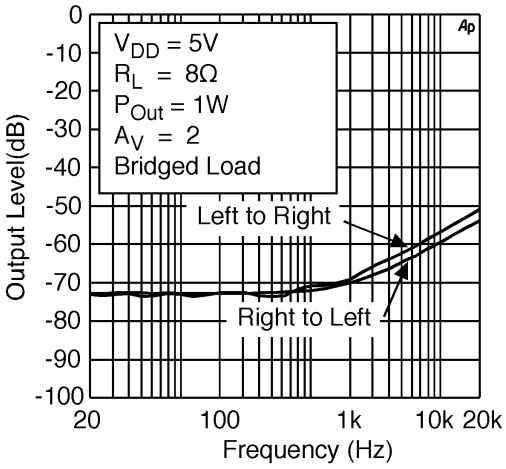


Figure 66.

Crosstalk

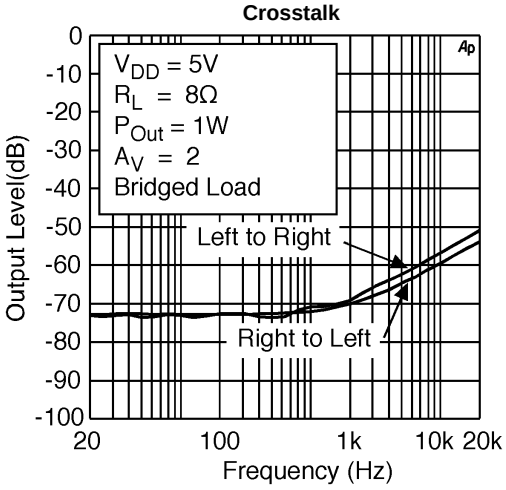


Figure 67.

Output Power vs Supply voltage

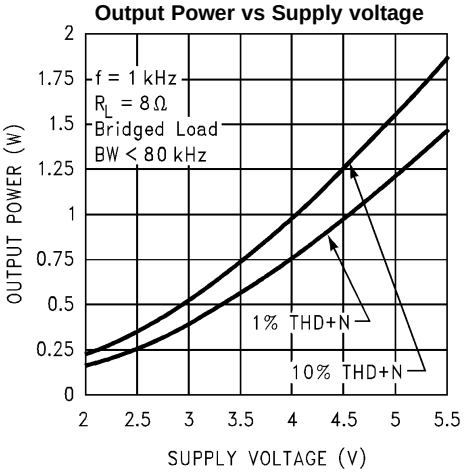


Figure 68.

Output Power vs Supply Voltage

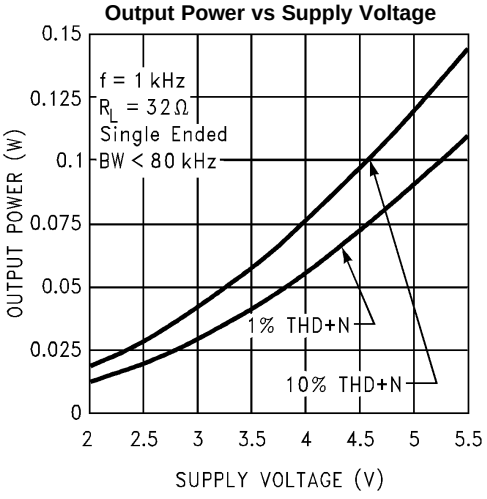


Figure 69.

Supply Current vs Supply Voltage

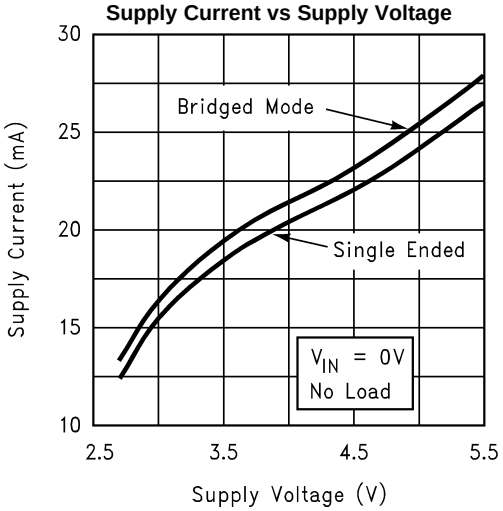


Figure 70.

APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4836's exposed-DAP (die attach paddle) packages (MTE and LQ) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4836's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The MTE and LQ packages must have their DAPs soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 32(4x8) (MTE) or 6(3x2) (LQ) vias. The via diameter should be 0.012in–0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4836 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In systems using cooling fans, the LM4836MTE can take advantage of forced air cooling. With an air flow rate of 450 linear-feet per minute and a 2.5in^2 exposed copper or 5.0in^2 inner layer copper plane heatsink, the LM4836MTE can continuously drive a 3Ω load to full power. The LM4836LQ achieves the same output power level without forced air cooling. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4836's thermal shutdown protection. The LM4836's power de-rating curve in the TYPICAL PERFORMANCE CHARACTERISTICS MTE SPECIFIC CHARACTERISTICS shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP and LQ packages are shown in the RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT section. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LQ (WQFN) package is available in Texas Instruments' AN-1187 (literature number SNOA401).

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 3, the LM4836 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors R_f and R_i set the closed-loop gain of Amp1A, whereas two internal 20kΩ resistors set Amp2A's gain at −1. The LM4836 drives a load, such as a speaker, connected between the two amplifier outputs, −OUTA and +OUTA.

Figure 3 shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as “bridge mode”). This results in a differential gain of

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the AUDIO POWER AMPLIFIER DESIGN section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4836 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2/(2\pi^2 R_L) \text{Bridge Mode} \quad (3)$$

The LM4836's power dissipation is twice that given by Equation 2 or Equation 3 when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

The LM4836's T_{JMAX} = 150°C. In the LQ package soldered to a DAP pad that expands to a copper area of 5in^2 on a PCB, the LM4836's θ_{JA} is 20°C/W. In the MTE package soldered to a DAP pad that expands to a copper area of 2in^2 on a PCB, the LM4836's θ_{JA} is 41°C/W. At any given ambient temperature T_A, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4and substituting P_{DMAX} for P_{DMAX}' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4836's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\,\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the LQ package and 45°C for the MTE package.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \quad (6)$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4836's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation 2 is greater than that of Equation 3, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the TYPICAL PERFORMANCE CHARACTERISTICS MTE SPECIFIC CHARACTERISTICS curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 µF in parallel with a 0.1 µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 µF tantalum bypass capacitance connected between the LM4836's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4836's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

PROPER SELECTION OF EXTERNAL COMPONENTS

Optimizing the LM4836's performance requires properly selecting external components. Though the LM4836 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4836 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (0.33µF in Figure 3). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, the input coupling capacitor has an affect on the LM4835's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 3, the input resistor (20kΩ) and the input capacitor produce a −3dB high pass filter cutoff frequency that is found using Equation 7.

$$f_{-3\,dB} = \frac{1}{2\pi R_{IN} C_1} \tag{7}$$

As an example when using a speaker with a low frequency limit of 150Hz, the input coupling capacitor using Equation 7, is 0.063µF. The 0.33µF input coupling capacitor shown in Figure 3 allows the LM4835 to drive high efficiency, full range speaker whose response extends below 30Hz.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4836 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pop”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4836's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of “clicks and pops”. Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	2ms
0.1µF	20ms
0.22µF	44ms
0.47µF	94ms
1.0µF	200ms

In order eliminate “clicks and pops”, all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause “clicks and pops”. In a single-ended configuration, the output is coupled to the load by C_{OUT}. This capacitor usually has a high value. C_{OUT} discharges through internal 20kΩ resistors. Depending on the size of C_{OUT}, the discharge time constant can be relatively large. To reduce transients in single-ended mode, an external 1kΩ–5kΩ resistor can be placed in parallel with the internal 20kΩ resistor. The tradeoff for using this resistor is increased quiescent current.

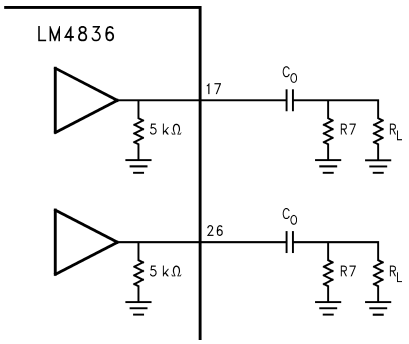


Figure 71. Resistor for Varying Output Loads

DOCKING STATION

Applications such as notebook computers can take advantage of a docking station to connect to external devices such as monitors or audio/visual equipment that sends or receives line level signals. The LM4836 has two outputs, Pin 9 and Pin 13, which connect to outputs of the internal input amplifiers that drive the volume control inputs. These input amplifiers can drive loads of >1kΩ (such as powered speakers) with a rail-to-rail signal. Since the output signal present on the RIGHT DOCK and LEFT DOCK pins is biased to $V_{DD}/2$, coupling capacitors should be connected in series with the load. Typical values for the coupling capacitors are 0.33µF to 1.0µF. If polarized coupling capacitors are used, connect their "+" terminals to the respective output pin.

Since the DOCK outputs precede the internal volume control, the signal amplitude will be equal to the input signal's magnitude and cannot be adjusted. However, the input amplifier's closed-loop gain can be adjusted using external resistors. These resistors are shown in Figure 71 as 20kΩ devices that set each input amplifier's gain to -1. Use Equation 8 to determine the input and feedback resistor values for a desired gain.

$$- A_v = R_F / R_i \quad (8)$$

Adjusting the input amplifier's gain sets the minimum gain for that channel. The DOCK outputs adds circuit and functional flexibility because their use supercedes using the inverting outputs of each bridged output amplifier as line-level outputs.

STEREO-INPUT MULTIPLEXER (STEREO MUX)

The LM4836 has two stereo inputs. The MUX CONTROL pin controls which stereo input is active. Applying 0V to the MUX CONTROL pin selects stereo input 1. Applying V_{DD} to the MUX CONTROL pin selects stereo input 2.

BEEP DETECT FUNCTION

Computers and notebooks produce a system "beep" signal that drives a small speaker. The speaker's auditory output signifies that the system requires user attention or input. To accommodate this system alert signal, the LM4836's pin 11 is a mono input that accepts the beep signal. Internal level detection circuitry at this input monitors the beep signal's magnitude. When a signal level greater than $V_{DD}/2$ is detected on pin 11, the bridge output amplifiers are enabled. The beep signal is amplified and applied to the load connected to the output amplifiers. A valid beep signal will be applied to the load even when MUTE is active. Use the input resistors connected between the BEEP IN pin and the stereo input pins to accommodate different beep signal amplitudes. These resistors are shown as 200kΩ devices in Figure 71. Use higher value resistors to reduce the gain applied to the beep signal. The resistors must be used to pass the beep signal to the stereo inputs. The BEEP IN pin is used only to detect the beep signal's magnitude: it does not pass the signal to the output amplifiers. The LM4836's shutdown mode must be deactivated before a system alert signal is applied to BEEP IN pin.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4836's shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the LM4836's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7 µA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible to the SHUTDOWN pin. A voltage that is less than V_{DD} may increase the shutdown current. Logic Level Truth Table shows the logic signal levels that activate and deactivate micro-power shutdown and headphone amplifier operation.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor specify that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Table 1. Logic Level Truth Table for SHUTDOWN, HP-IN, and MUX Operation

SHUTDOWN PIN	HP-IN PIN	MUX CHANNEL SELECT PIN	OPERATIONAL MODE (MUX INPUT CHANNEL #)
Logic Low	Logic Low	Logic Low	Bridged Amplifiers (1)
Logic Low	Logic Low	Logic High	Bridged Amplifiers (2)
Logic Low	Logic High	Logic Low	Single-Ended Amplifiers (1)
Logic Low	Logic High	Logic High	Single-Ended Amplifiers (2)
Logic High	X	X	Micro-Power Shutdown

MUTE FUNCTION

The LM4836 mutes the amplifier and DOCK outputs when V_{DD} is applied to pin 5, the MUTE pin. Even while muted, the LM4836 will amplify a system alert (beep) signal whose magnitude satisfies the BEEP DETECT circuitry. Applying 0V to the MUTE pin returns the LM4836 to normal, unmated operation. Prevent unanticipated mute behavior by connecting the MUTE pin to V_{DD} or ground. Do not let pin 5 float.

HP SENSE FUNCTION

Applying a voltage between 4V and V_{DD} to the LM4836's HP-IN headphone control pin turns off Amp2A and Amp2B, muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 72 shows the implementation of the LM4836's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP-IN pin (pin 16) at approximately 50mV. This 50mV enables Amp1B and Amp2B, placing the LM4836 in bridged mode operation. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones.

The HP-IN threshold is set at 4V. While the LM4836 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from −OUTA and allows R1 to pull the HP Sense pin up to V_{DD}. This enables the headphone function, turns off Amp2A and Amp2B, and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistor R2 and R3. These resistors have negligible effect on the LM4836's output drive capability since the typical impedance of headphones is 32Ω.

Figure 72 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones.

A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and Amp1A and Amp2A drive a pair of headphones.

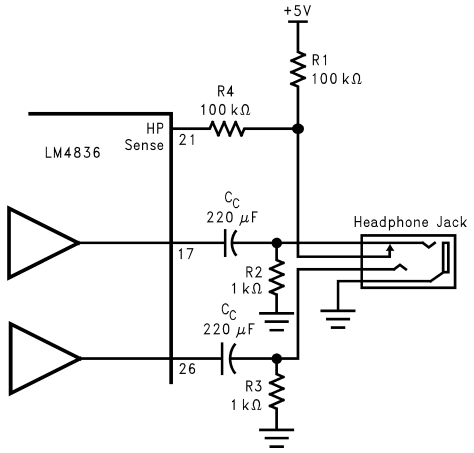


Figure 72. Headphone Sensing Circuit

BASS BOOST FUNCTION

The LM4836 has a bass-boost feature that enhances the low frequency response in applications using small speakers. The voltage level applied to the BASS BOOST SELECT pin controls the bass-boost function. Applying GND activates the bass-boost mode. In bass-boost mode, the LM4836's gain is increased at low frequencies, with a corner frequency set by the external capacitor, C_{BASS}. Applying V_{DD} defeats the bass-boost mode and selects unity gain. Tying the BASS BOOST SELECT pin to V_{DD} permanently defeats the bass-boost function.

Enabling bass-boost forces the output amplifiers to operate with an internally set low frequency gain of 2 (gain of 4 in bridged mode). The capacitor C_{BASS} shown in Figure 3 sets the bass-boost corner frequency. At low frequencies, the capacitor is a virtual open circuit and the feedback resistance consists of two 10kΩ resistors. At high frequencies, the capacitor is a virtual short circuit, which shorts one of the two 10kΩ feedback resistors. The results is bridge amplifier gain that increases at low frequencies. A first-order pole is formed with a corner frequency at

$$f_C = 1/(2\pi 10k\Omega C_{BASS}) \quad (9)$$

At $f << f_C$, the differential gain of this bridged amplifier is

$$2(10k\Omega + 10k\Omega)/10k\Omega = 4 \quad (10)$$

With C_{BASS} = 0.1µF, the first-order pole has a corner frequency of 160Hz. It is assumed when using Equation 9 that C_O, C_i, f_{IC}, and f_{OC}, are chosen for the desired low frequency response as explained in the PROPER SELECTION OF EXTERNAL COMPONENTS section. See the TYPICAL PERFORMANCE CHARACTERISTICS MTE SPECIFIC CHARACTERISTICS section for a graph that includes bass-boost performance with various values of C_{BASS}.

DC VOLUME CONTROL

The LM4836 has an internal stereo volume control whose setting is a function of the DC voltage applied to the DC VOL CONTROL pin. The volume control's voltage input range is 0V to V_{DD}. The volume range is from 0dB (DC control voltage = 80%V_{DD}) to -80dB (DC control voltage = 0V). The volume remains at 0dB for DC control voltages greater than 80%V_{DD}. When the MODE input is 0V, the LM4836 operates at unity gain, bypassing the volume control. A graph showing a typical volume response versus DC control voltage is shown in the TYPICAL PERFORMANCE CHARACTERISTICS MTE SPECIFIC CHARACTERISTICS section.

Like all volume controls, the LM4836's internal volume control is set while listening to an amplified signal that is applied to an external speaker. The actual voltage applied to the DC VOL CONTROL pin is a result of the volume a listener desires. As such, the volume control is designed for use in a feedback system that includes human ears and preferences. This feedback system operates quite well without the need for accurate gain. The user simply sets the volume to the desired level as determined by their ear, without regard to the actual DC voltage that produces the volume. Therefore, the accuracy of the volume control is not critical, as long as the volume changes monotonically, matches well between stereo channels, and the step size is small enough to reach a desired volume that is not too loud or too soft. Since gain accuracy is not critical, there will be volume variation from part-to-part even with the same applied DC control voltage. The gain of a given LM4836 can be set with a fixed external voltage, but another LM4836 may require a different control voltage to achieve the same gain. The typical part-to-part variation can be as large as 8dB for the same control voltage.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	1 W_{RMS}
Load Impedance:	8Ω
Input Level:	1 V_{RMS}
Input Impedance:	20 kΩ
Bandwidth:	100 Hz−20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the TYPICAL PERFORMANCE CHARACTERISTICS section. Another way, using Equation 11, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the TYPICAL PERFORMANCE CHARACTERISTICS curves, must be added to the result obtained by Equation 11. The result is Equation 12.

$$V_{outpeak} = \sqrt{(2R_L P_O)} \quad (11)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (12)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4836 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the POWER DISSIPATION section.

After satisfying the LM4836's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation 13.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (13)$$

Thus, a minimum gain of 2.83 allows the LM4836's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3.

The amplifier's overall gain is set using the input (R_i) and feedback (R_i) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 14.

$$R_f/R_i = A_{VD}/2 \quad (14)$$

The value of R_f is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (15)$$

and an

$$f_H = 20kHz \times 5 = 100kHz \quad (16)$$

As mentioned in the PROPER SELECTION OF EXTERNAL COMPONENTS section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 17.

$$C_i \geq 1/(2\pi R_i f_L) \quad (17)$$

The result is

$$1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F \quad (18)$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4836's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance,restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 73 through Figure 77 show the recommended four-layer PC board layout that is optimized for the 8-pin LQ-packaged LM4836 and associated external components. This circuit is designed for use with an external 5V supply and 4Ω speakers.

This circuit board is easy to use. Apply 5V and ground to the board's V_{DD} and GND pads, respectively. Connect 4Ω speakers between the board's −OUTA and +OUTA and OUTB and +OUTB pads.

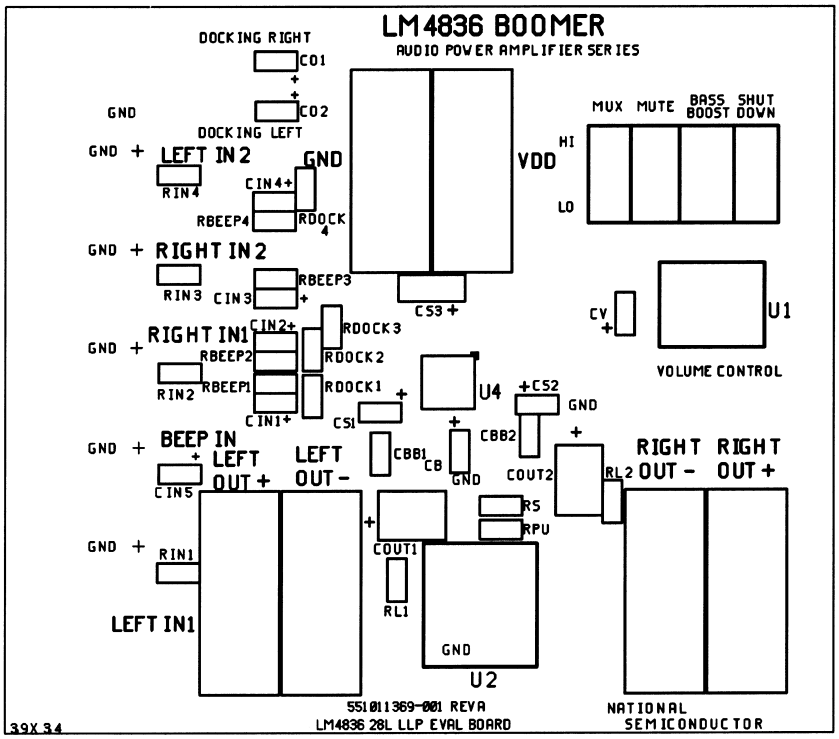


Figure 73. Recommended LQ PC Board Layout: Component-Side Silkscreen

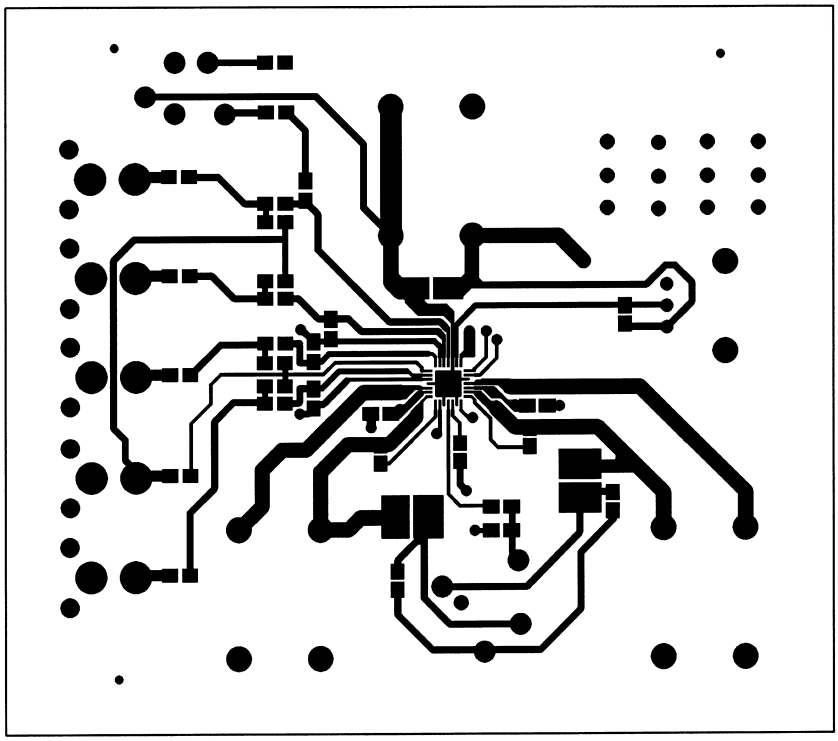


Figure 74. Recommended LQ PC Board Layout: Component-Side Layout

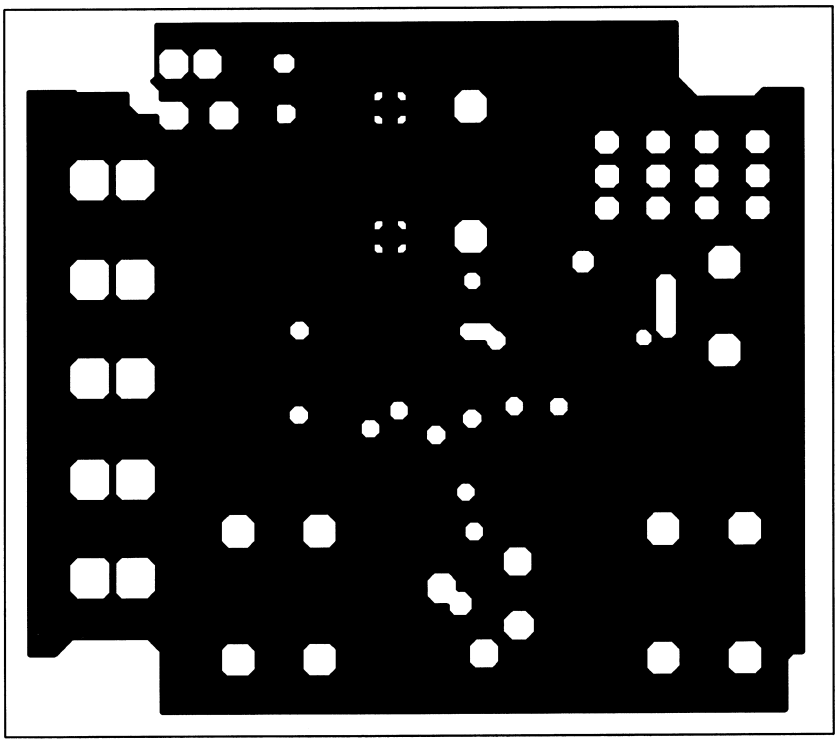


Figure 75. Recommended LQ PC Board Layout: Upper Inner-Layer Layout

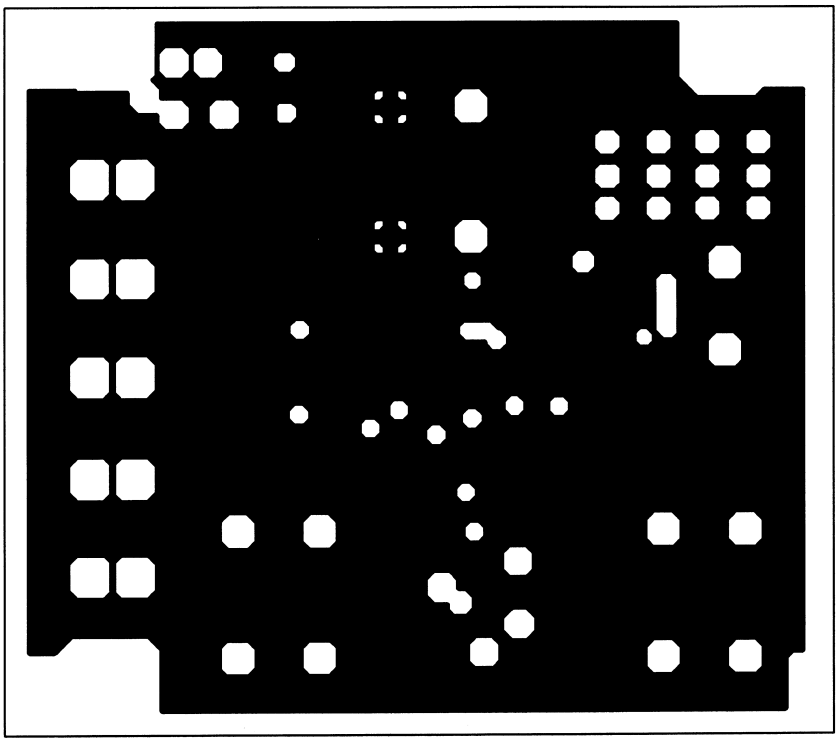


Figure 76. Recommended LQ PC Board Layout: Lower Inner-Layer Layout

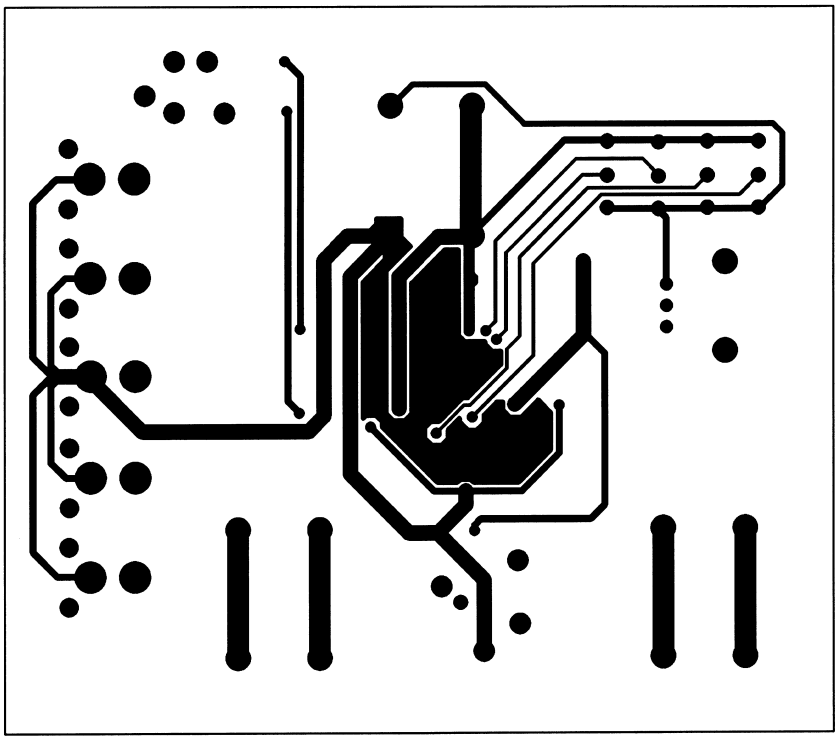


Figure 77. Recommended LQ PC Board Layout: Bottom-Side Layout

REVISION HISTORY

Changes from Revision E (May 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	30

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4836LQ/NOPB	ACTIVE	WQFN	NJB	28	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L4836LQ	Samples
LM4836MTEX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4836MTE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

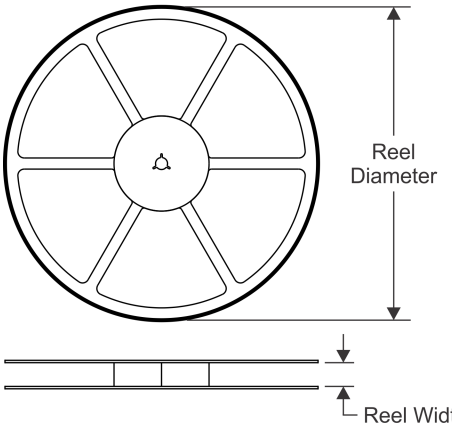
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

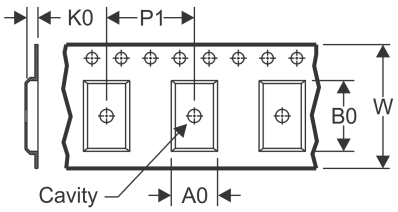
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

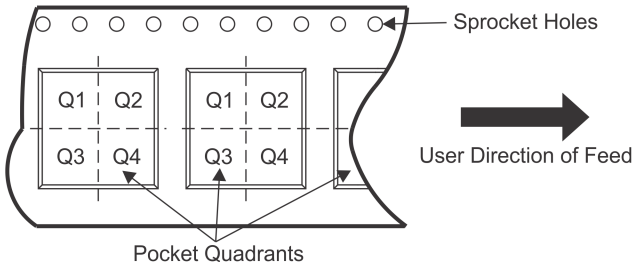


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

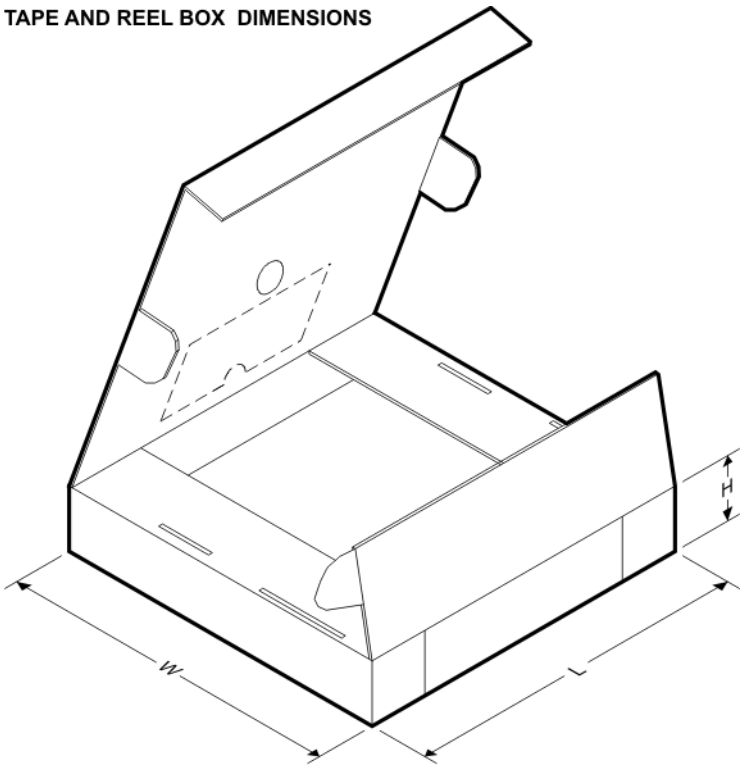
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4836LQ/NOPB	WQFN	NJB	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM4836MTEX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

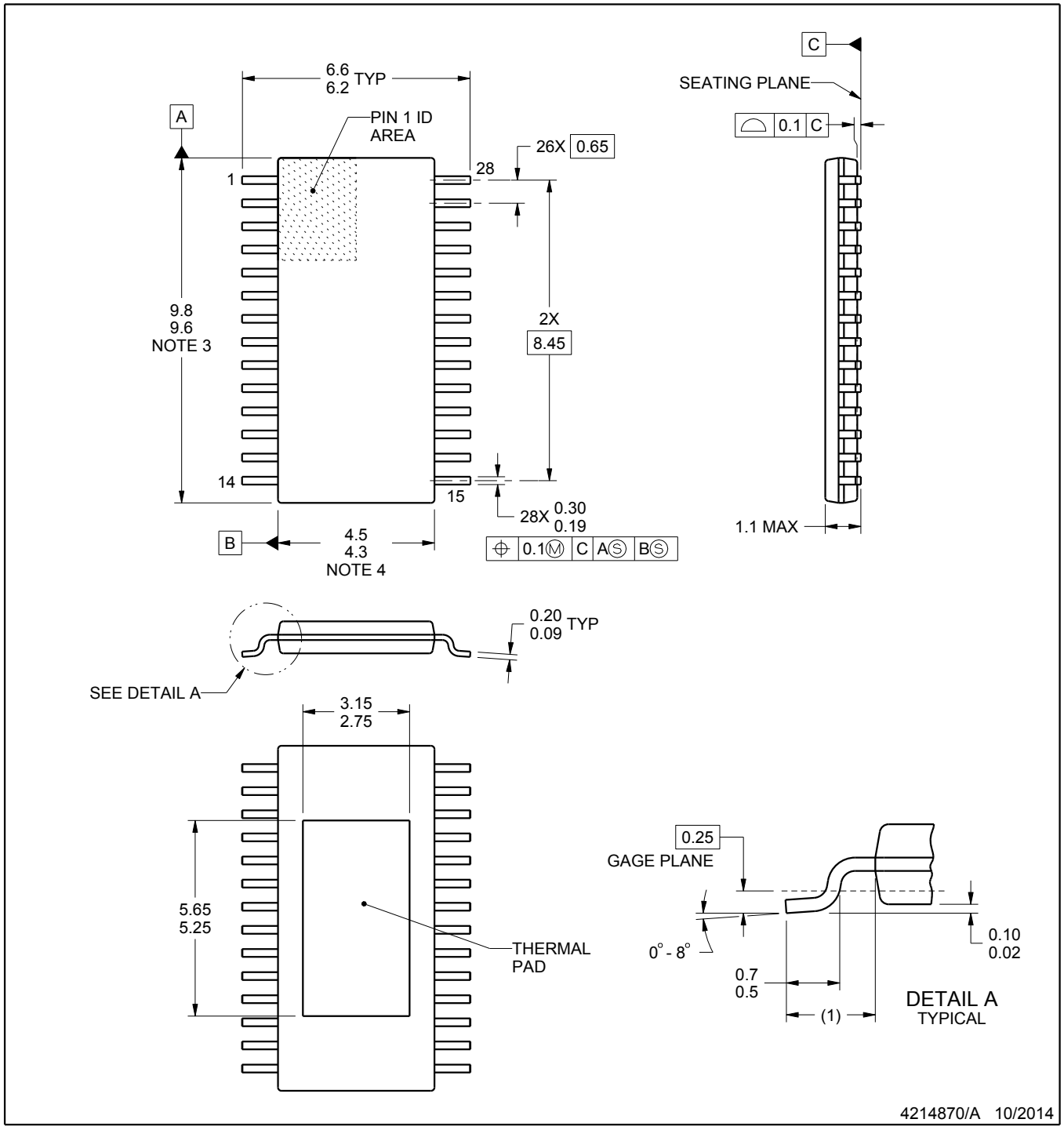
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4836LQ/NOPB	WQFN	NJB	28	1000	210.0	185.0	35.0
LM4836MTEX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

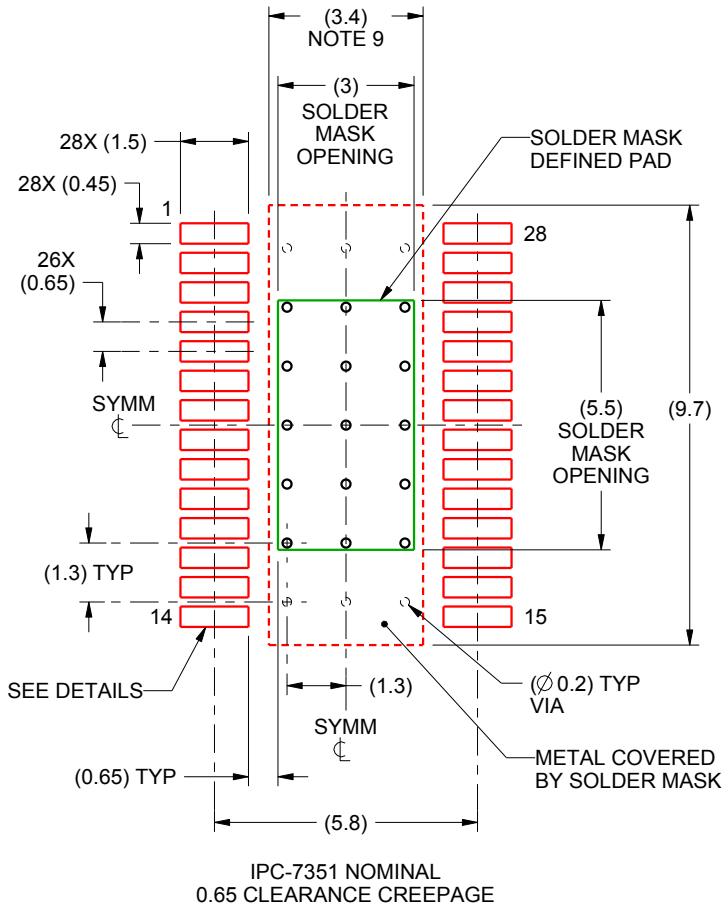
PLASTIC SMALL OUTLINE



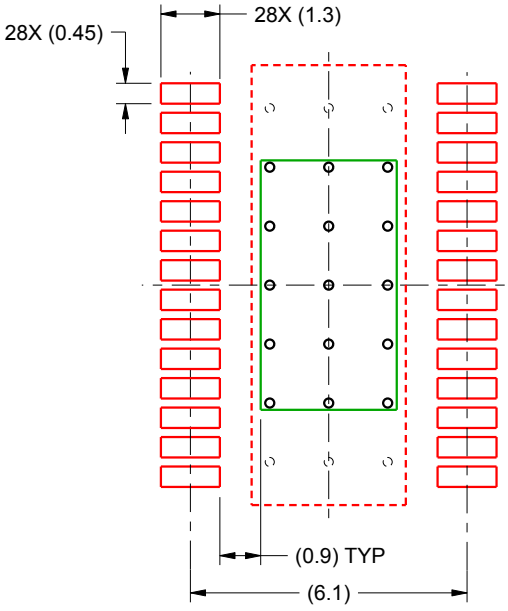
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

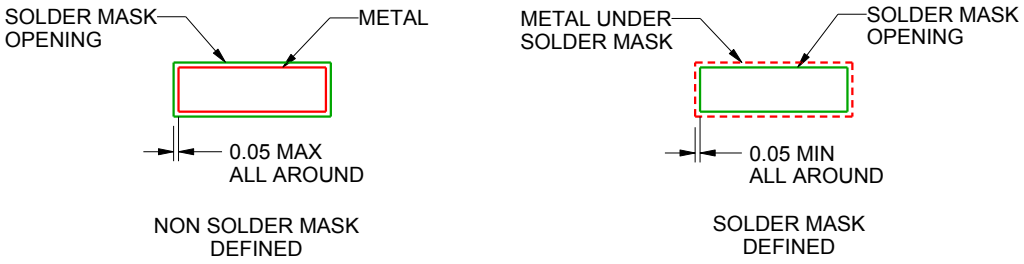


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X

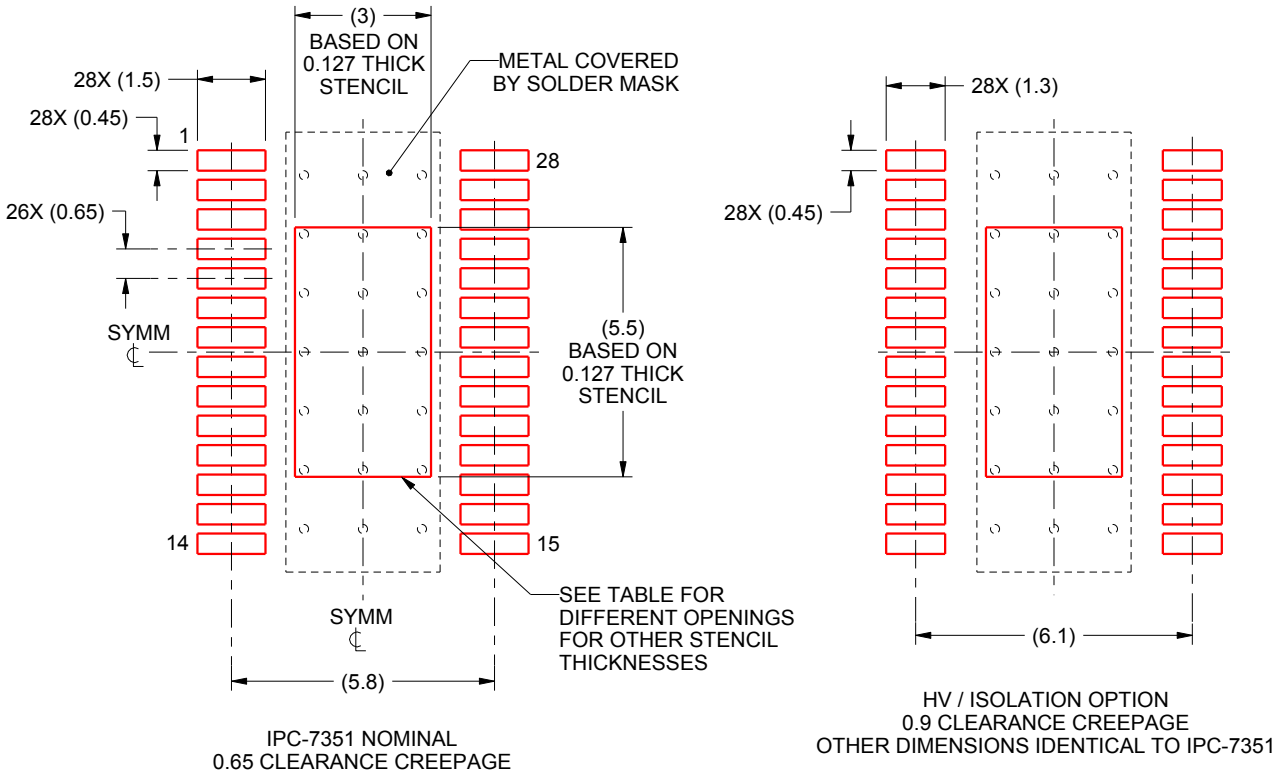


SOLDER MASK DETAILS

4214870/A 10/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

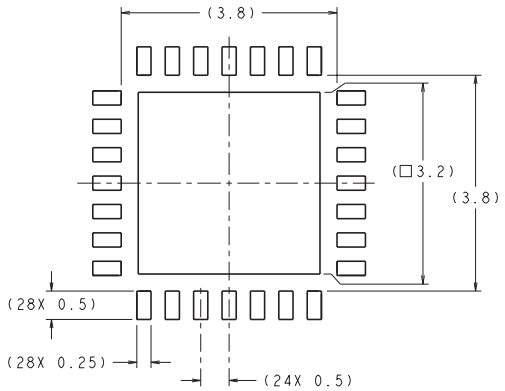
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/A 10/2014

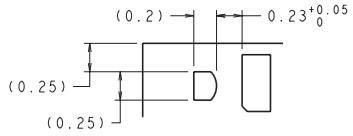
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

NJB0028A

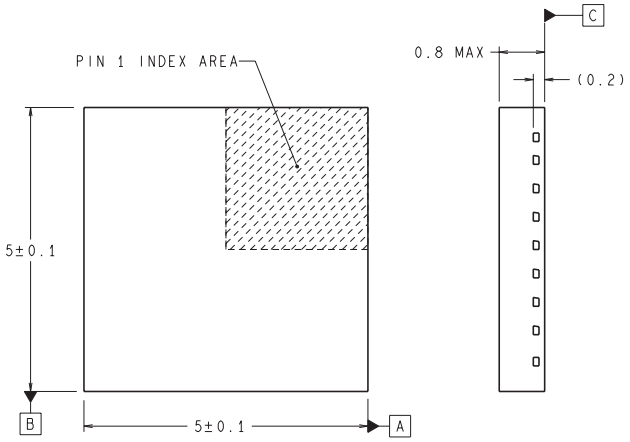


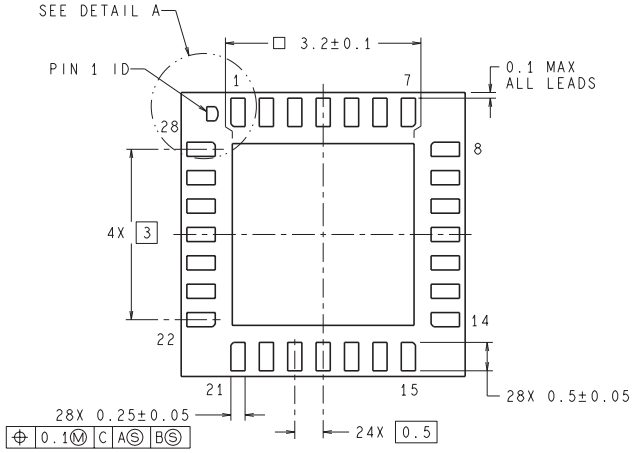
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS



DETAIL A
SCALE:40X

DIMENSIONS ARE IN MILLIMETERS





LQA28A (REV B)

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