

TS5A23157 双通道 10Ω SPDT 模拟开关

1 特性

- 低导通状态电阻（125℃ 条件下为 15Ω）
- 125℃ 运行
- 控制输入可承受 5V 电压
- 指定的先断后合开关
- 低电荷注入
- 出色的导通状态电阻匹配
- 低总谐波失真
- 1.8V 至 5.5V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
 - 2000V 人体放电模式 (A114-B, II 类)
 - 1000V 充电器件模型 (C101)

2 应用

- 采样和保持电路
- 电池供电类设备
- 音频和视频信号路由
- 通信电路

3 说明

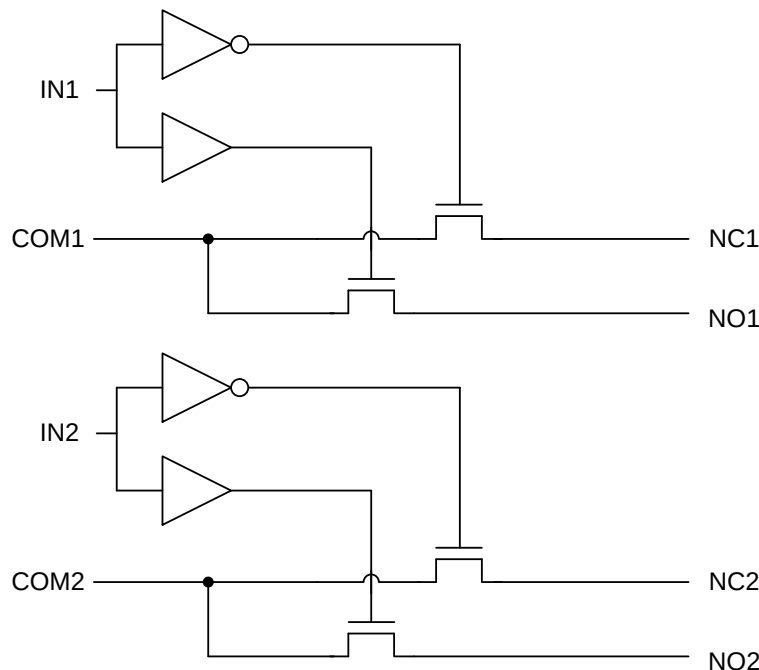
TS5A23157 器件是一款双通道单极双投 (SPDT) 模拟开关，其设计工作电压为 1.65V 至 5.5V。该器件可以同时处理数字和模拟信号。高达 5.5V（峰值）的信号可在任一方向传输。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
TS5A23157DGS	VSSOP (10)	3.00mm × 3.00mm
TS5A23157RSE	UQFN (10)	2.00mm × 1.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

方框图



目录

1	特性	1	8.2	Functional Block Diagram	16
2	应用	1	8.3	Feature Description	16
3	说明	1	8.4	Device Functional Modes	16
4	修订历史记录	2	9	Application and Implementation	17
5	Pin Configuration and Functions	3	9.1	Application Information	17
6	Specifications	4	9.2	Typical Application	17
6.1	Absolute Maximum Ratings	4	10	Power Supply Recommendations	18
6.2	ESD Ratings	4	11	Layout	19
6.3	Recommended Operating Conditions	4	11.1	Layout Guidelines	19
6.4	Thermal Information	4	11.2	Layout Example	19
6.5	Electrical Characteristics for 5-V Supply	5	12	器件和文档支持	20
6.6	Electrical Characteristics for 3.3-V Supply	7	12.1	器件支持	20
6.7	Electrical Characteristics for 2.5-V Supply	8	12.2	文档支持	21
6.8	Electrical Characteristics for 1.8-V Supply	9	12.3	社区资源	21
6.9	Typical Characteristics	10	12.4	商标	21
7	Parameter Measurement Information	12	12.5	静电放电警告	21
8	Detailed Description	16	12.6	术语表	21
8.1	Overview	16	13	机械、封装和可订购信息	21

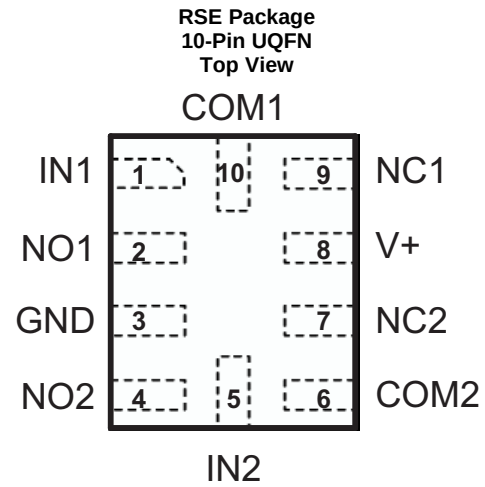
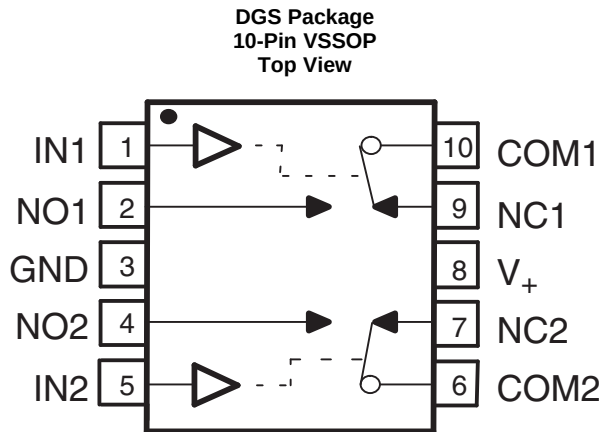
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (June 2015) to Revision F	Page
• 将特性从“低导通状态电阻 (10 Ω)”更改为“低导通状态电阻 (125 $^{\circ}$ C 条件下为 15 Ω)”	1
• 添加了特性: 125 $^{\circ}$ C 运行条件	1
• Added Junction Temperature To the <i>Absolute Maximum Ratings</i> table	4
• Changed the Operating temperature MAX value From: 85 $^{\circ}$ C To: 125 $^{\circ}$ C in the <i>Recommended Operating Conditions</i> table	4
• Changed the <i>Thermal Information</i> table	4
• Changed r_{on} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
• Changed V_{IH} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 5-V Supply</i> table	5
• Changed r_{on} in the <i>Electrical Characteristics for 3.3-V Supply</i> table	7
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 3.3-V Supply</i> table	7
• Changed r_{on} in the <i>Electrical Characteristics for 2.5-V Supply</i> table	8
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 2.5-V Supply</i> table	8
• Changed r_{on} in the <i>Electrical Characteristics for 1.8-V Supply</i> table	9
• Changed t_{ON} and t_{OFF} in the <i>Electrical Characteristics for 1.8-V Supply</i> table	9

Changes from Revision D (October 2013) to Revision E	Page
• 已添加 引脚配置和功能 部分、ESD 额定值 表、特性 说明 部分、器件功能模式、应用和实现 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN1	I	Select pin for switch 1
2	NO1	I/O	Normally open I/O for switch 1
3	GND	—	Ground
4	NO2	I/O	Normally open I/O for switch 2
5	IN2	I	Select pin for switch 2
6	COM2	I/O	Common I/O for switch 2
7	NC2	I/O	Normally closed I/O for switch 2
8	V+	—	Power supply pin
9	NC1	I/O	Normally closed I/O for switch 1
10	COM1	I/O	Common I/O for switch 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V ₊	Supply voltage ⁽²⁾		−0.5	6.5	V
V _{NC} V _{NO} V _{COM}	Analog voltage ⁽²⁾⁽³⁾⁽⁴⁾		−0.5	V ₊ + 0.5	V
I _{I/OK}	Analog port diode current	V _{NC} , V _{NO} , V _{COM} < 0 or V _{NC} , V _{NO} , V _{COM} > V ₊	±50		mA
I _{NC} I _{NO} I _{COM}	On-state switch current	V _{NC} , V _{NO} , V _{COM} = 0 to V ₊	±50		mA
V _{IN}	Digital input voltage ⁽²⁾⁽³⁾		−0.5	6.5	V
I _{IK}	Digital input clamp current	V _{IN} < 0	−50		mA
	Continuous current through V ₊ or GND		±100		mA
T _J	Junction Temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{I/O}	Switch input/output voltage	0	V ₊	V
V ₊	Supply voltage	1.65	5.5	V
V _I	Control input voltage	0	5.5	V
T _A	Operating temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS5A23157		UNIT
		DGS (VSSOP)	RSE (UQFN)	
		10 PINS	10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	210.5	215.4	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	99.1	140.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	132.4	137.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	29.1	13.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	130.5	137.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 5-V Supply

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC} Analog signal range				0		V_+	V
r_{on} ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -30 \text{ mA}$, Switch ON, see Figure 9	Full -40 to 125°C	4.5 V			10 15	Ω
Δr_{on} ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 3.15 \text{ V}$, $I_{COM} = -30 \text{ mA}$, Switch ON, see Figure 9	25°C	4.5 V		0.15		Ω
$r_{on(flat)}$ ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -30 \text{ mA}$, Switch ON, see Figure 9	25°C	4.5 V		4		Ω
$I_{NC(OFF)}, I_{NO(OFF)}$ NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$, Switch OFF, see Figure 10	25°C Full	5.5 V	-1	0.05	1	μA
$I_{NC(ON)}, I_{NO(ON)}$ NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, see Figure 10	25°C Full	5.5 V	-0.1		0.1	μA
$I_{COM(ON)}$ COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, see Figure 10	25°C Full	5.5 V	-0.1		0.1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾							
V_{IH} Input logic high		Full -40 to 125°C	4.75 V to 5.25 V	$V_+ \times 0.7$ 3.1			V
V_{IL} Input logic low		Full				$V_+ \times 0.3$	V
I_{IH}, I_{IL} Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$	25°C Full	5.5 V	-1	0.05	1	μA
DYNAMIC							
t_{ON} Turnon time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	4.5 V to 5.5 V 4.75 V to 5.25 V	1.7		5.7	ns
t_{OFF} Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	4.5 V to 5.5 V 4.75 V to 5.25 V	0.8		3.8	ns
t_{BBM} Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$, see Figure 13	Full	4.5 V to 5.5 V	0.5			ns
Q_C Charge injection	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, See Figure 17	25°C	5 V		7		pC
$C_{NC(OFF)}, C_{NO(OFF)}$ NC, NO OFF capacitance	$V_{NC} \text{ or } V_{NO} = V_+ \text{ or GND}$, Switch OFF, see Figure 11	25°C	5 V		5.5		pF
$C_{NC(ON)}, C_{NO(ON)}$ NC, NO ON capacitance	$V_{NC} \text{ or } V_{NO} = V_+ \text{ or GND}$, Switch ON, see Figure 11	25°C	5 V		17.5		pF
$C_{COM(ON)}$ COM ON capacitance	$V_{COM} = V_+ \text{ or GND}$, Switch ON, see Figure 11	25°C	5 V		17.5		pF
C_{IN} Digital input capacitance	$V_{IN} = V_+ \text{ or GND}$, See Figure 11	25°C	5 V		2.8		pF
BW Bandwidth	$R_L = 50 \Omega$, Switch ON, see Figure 14	25°C	4.5 V		220		MHz

(1) $T_A = 25^\circ\text{C}$.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

Electrical Characteristics for 5-V Supply (continued)

 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
O_{ISO}	OFF isolation	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch OFF, see Figure 15	25°C	4.5 V		–65		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$,	Switch ON, see Figure 16	25°C	4.5 V		–66		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 600\text{ Hz to }20\text{ kHz}$, see Figure 18	25°C	4.5 V		0.01%		
SUPPLY									
I_+	Positive supply current	$V_{IN} = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V			1	μA
				Full				10	
ΔI_+	Change in supply current	$V_{IN} = V_+ - 0.6\text{ V}$		Full	5.5 V			500	μA

6.6 Electrical Characteristics for 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC} Analog signal range				0		V_+	V
r_{on} ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, see Figure 9	Full -40 to 125°C	3 V			18 23	Ω
Δr_{on} ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 2.1\text{ V}$, $I_{COM} = -24\text{ mA}$, Switch ON, see Figure 9	25°C	3 V		0.2		Ω
$r_{on(Flat)}$ ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -24\text{ mA}$, Switch ON, see Figure 11	25°C	3 V		9		Ω
$I_{NC(OFF)}, I_{NO(OFF)}$ NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$, Switch OFF, see Figure 10	25°C Full	3.6 V	-1	0.05	1	μA
$I_{NC(ON)}, I_{NO(ON)}$ NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, see Figure 10	25°C Full	3.6 V	-0.1		0.1	μA
$I_{COM(ON)}$ COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, see Figure 10	25°C Full	3.6 V	-0.1		0.1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾							
V_{IH} Input logic high		Full		$V_+ \times 0.7$			V
V_{IL} Input logic low		Full				$V_+ \times 0.3$	V
I_{IH}, I_{IL} Input leakage current	$V_{IN} = 5.5\text{ V or }0$	25°C Full	3.6 V	-1	0.05	1	μA
DYNAMIC							
t_{ON} Turn-on time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 12	Full -40 to 125°C	3 V to 3.6 V	2.5		7.6	ns
t_{OFF} Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500\ \Omega$, $C_L = 50\text{ pF}$, see Figure 12	Full -40 to 125°C	3 V to 3.6 V	1.5		5.3	ns
t_{BBM} Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, see Figure 13	Full	3 V to 3.6 V	0.5			ns
Q_C Charge injection	$R_L = 50\ \Omega$, $C_L = 0.1\text{ nF}$, see Figure 17	25°C	3.3 V		3		pC
BW Bandwidth	$R_L = 50\ \Omega$, Switch ON, see Figure 14	25°C	3 V		220		MHz
O_{ISO} OFF isolation	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch OFF, see Figure 15	25°C	3 V		-65		dB
X_{TALK} Crosstalk	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, see Figure 16	25°C	3 V		-66		dB
THD Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 600\text{ Hz to }20\text{ kHz}$, see Figure 18	25°C	3 V		0.015%		
SUPPLY							
I_+ Positive supply current	$V_{IN} = V_+ \text{ or GND}$, Switch ON or OFF	25°C Full	3.6 V			1 10	μA
ΔI_+ Change in supply current	$V_{IN} = V_+ - 0.6\text{ V}$	Full	3.6 V			500	μA

(1) $T_A = 25^\circ\text{C}$.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.7 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC} Analog signal range				0		V_+	V
r_{on} ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -8 \text{ mA}$, Switch ON, see Figure 9	Full -40 to 125°C	2.3 V			45 50	Ω
Δr_{on} ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 1.6 \text{ V}$, $I_{COM} = -8 \text{ mA}$, Switch ON, see Figure 9	25°C	2.3 V		0.5		Ω
$r_{on(Flat)}$ ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -8 \text{ mA}$, Switch ON, see Figure 9	25°C	2.3 V		27		Ω
$I_{NC(OFF)}, I_{NO(OFF)}$ NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$, Switch OFF, see Figure 10	25°C Full	2.7 V	-1	0.05	1	μA
$I_{NC(ON)}, I_{NO(ON)}$ NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, see Figure 10	25°C Full	2.7 V	-0.1		0.1	μA
$I_{COM(ON)}$ COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, see Figure 10	25°C Full	2.7 V	-0.1		0.1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾							
V_{IH} Input logic high		Full		$V_+ \times 0.7$			V
V_{IL} Input logic low		Full				$V_+ \times 0.3$	V
I_{IH}, I_{IL} Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$	25°C Full	2.7 V	-1	0.05	1	μA
DYNAMIC							
t_{ON} Turnon time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	2.3 V to 2.7 V	3.5		14	ns
t_{OFF} Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	2.3 V to 2.7 V	2		7.5	ns
t_{BBM} Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, see Figure 13	Full	2.3 V to 2.7 V	0.5			ns
BW Bandwidth	$R_L = 50 \Omega$, Switch ON, see Figure 14	25°C	2.3 V		220		MHz
O_{ISO} OFF isolation	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch OFF, see Figure 15	25°C	2.3 V		-65		dB
X_{TALK} Crosstalk	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch ON, see Figure 16	25°C	2.3 V		-66		dB
THD Total harmonic distortion	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$, $f = 600 \text{ Hz to } 20 \text{ kHz}$, see Figure 18	25°C	2.3 V		0.025%		
SUPPLY							
I_+ Positive supply current	$V_{IN} = V_+ \text{ or GND}$, Switch ON or OFF	25°C Full	2.7 V			1 10	μA
ΔI_+ Change in supply current	$V_{IN} = V_+ - 0.6 \text{ V}$	Full	2.7 V			500	μA

 (1) $T_A = 25^\circ\text{C}$.

 (2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.8 Electrical Characteristics for 1.8-V Supply

 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG SWITCH							
V_{COM}, V_{NO}, V_{NC} Analog signal range				0		V_+	V
r_{on} ON-state resistance	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -4 \text{ mA}$, Switch ON, see Figure 9	Full -40 to 125°C	1.65 V			140 180	Ω
Δr_{on} ON-state resistance match between channels	$V_{NO} \text{ or } V_{NC} = 1.15 \text{ V}$, $I_{COM} = -4 \text{ mA}$, Switch ON, see Figure 9	25°C	1.65 V		1		Ω
$r_{on(Flat)}$ ON-state resistance flatness	$0 \leq V_{NO} \text{ or } V_{NC} \leq V_+$, $I_{COM} = -4 \text{ mA}$, Switch ON, see Figure 9	25°C	1.65 V		110		Ω
$I_{NC(OFF)}, I_{NO(OFF)}$ NC, NO OFF leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = 0 \text{ to } V_+$, Switch OFF, see Figure 10	25°C Full	1.95 V	-1	0.05	1	μA
$I_{NC(ON)}, I_{NO(ON)}$ NC, NO ON leakage current	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$, $V_{COM} = \text{Open}$, Switch ON, see Figure 10	25°C Full	1.95 V	-0.1		0.1	μA
$I_{COM(ON)}$ COM ON leakage current	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0 \text{ to } V_+$, Switch ON, see Figure 10	25°C Full	1.95 V	-0.1		0.1	μA
DIGITAL INPUTS (IN12, IN2)⁽²⁾							
V_{IH} Input logic high		Full		$V_+ \times 0.75$			V
V_{IL} Input logic low		Full				$V_+ \times 0.25$	V
I_{IH}, I_{IL} Input leakage current	$V_{IN} = 5.5 \text{ V or } 0$	25°C Full	1.95 V	-1	0.05	1	μA
DYNAMIC							
t_{ON} Turnon time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	1.65 V to 1.95 V	7		24	ns
t_{OFF} Turnoff time	$V_{NC} = \text{GND and } V_{NO} = V_+$ or $V_{NC} = V_+ \text{ and } V_{NO} = \text{GND}$, $R_L = 500 \Omega$, $C_L = 50 \text{ pF}$, see Figure 12	Full -40 to 125°C	1.65 V to 1.95 V	3		13	ns
t_{BBM} Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$, see Figure 13	Full	1.65 V to 1.95 V	0.5			ns
BW Bandwidth	$R_L = 50 \Omega$, Switch ON, see Figure 14	25°C	1.8 V		220		MHz
O_{ISO} OFF isolation	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch OFF, see Figure 15	25°C	1.8 V		-60		dB
X_{TALK} Crosstalk	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$, Switch ON, see Figure 16	25°C	1.8 V		-66		dB
THD Total harmonic distortion	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$, $f = 600 \text{ Hz to } 20 \text{ kHz}$, see Figure 18	25°C	1.8 V		0.015%		
SUPPLY							
I_+ Positive supply current	$V_{IN} = V_+ \text{ or GND}$, Switch ON or OFF	25°C Full	1.95 V			1 10	μA
ΔI_+ Change in supply current	$V_{IN} = V_+ - 0.6 \text{ V}$	Full	1.95 V			500	μA

(1) $T_A = 25^\circ\text{C}$.

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.9 Typical Characteristics

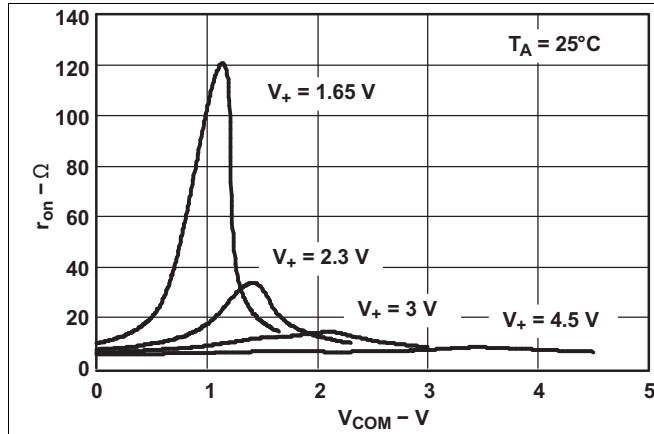


Figure 1. r_{on} vs V_{COM}

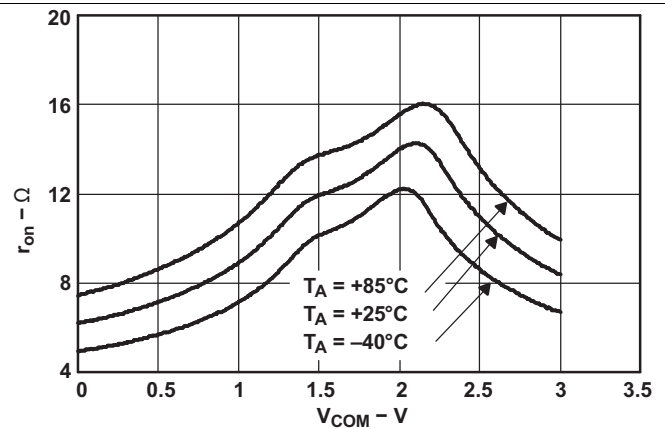


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

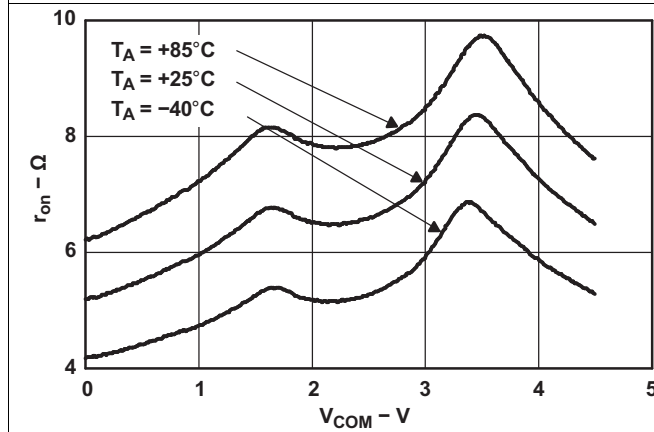


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

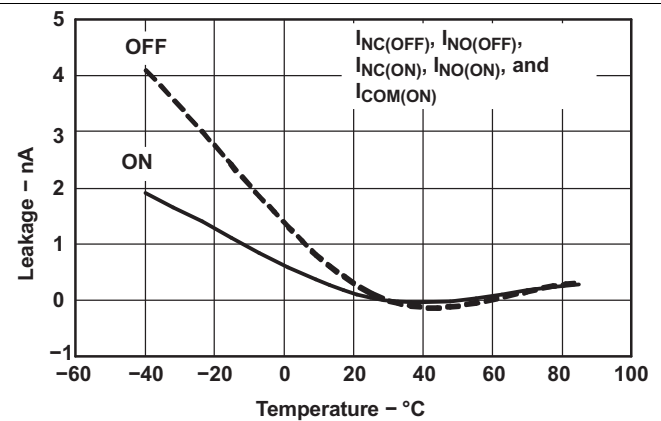


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)

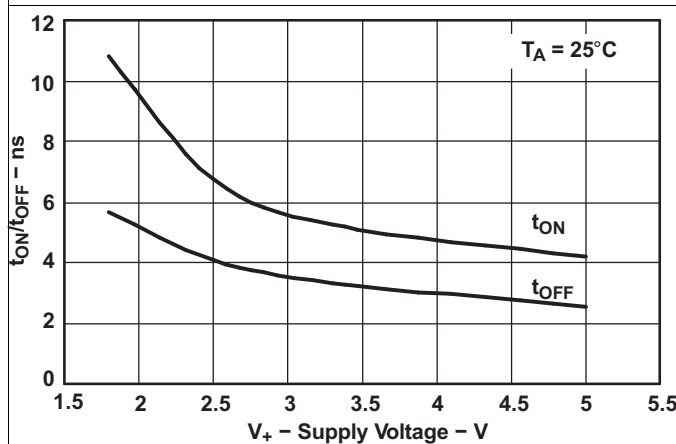


Figure 5. t_{ON} and t_{OFF} vs V_+

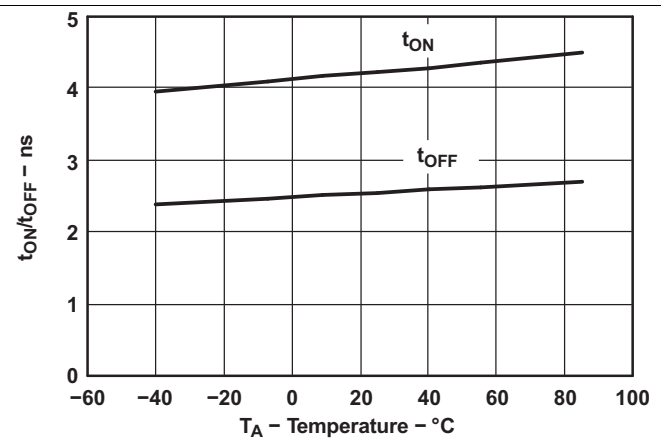


Figure 6. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5$ V)

Typical Characteristics (continued)

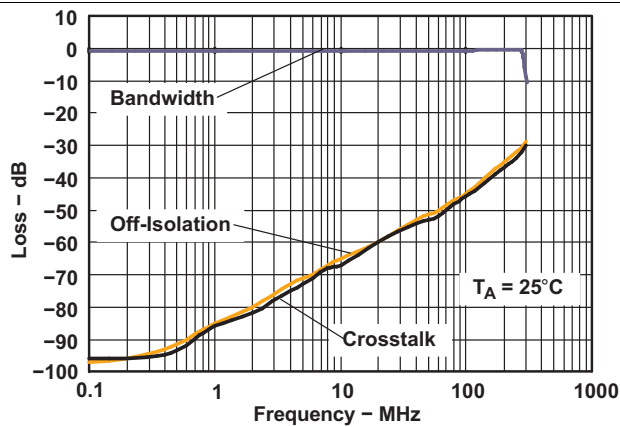


Figure 7. Frequency Response ($V_+ = 3\text{ V}$)

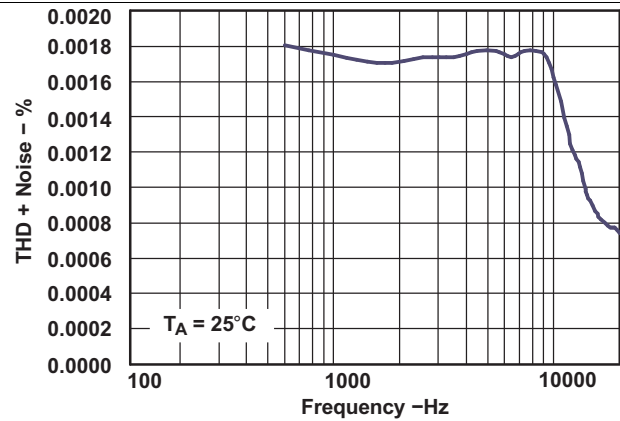


Figure 8. Total Harmonic Distortion (THD) vs Frequency ($V_+ = 3\text{ V}$)

7 Parameter Measurement Information

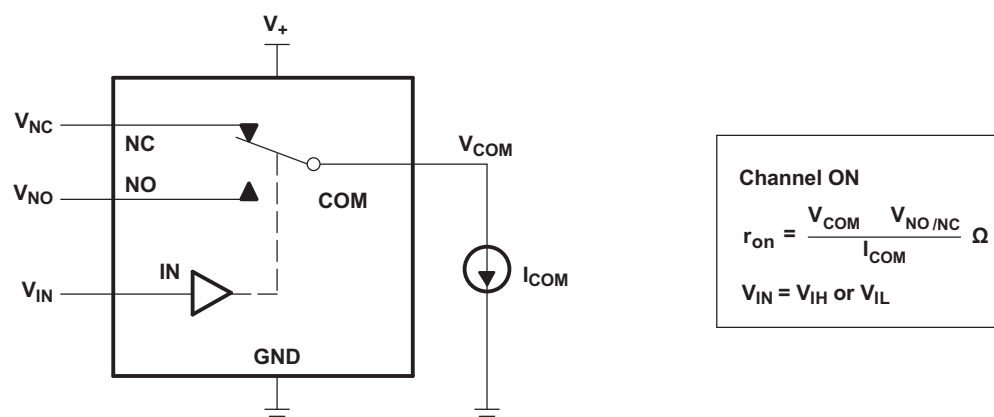


Figure 9. ON-State Resistance (r_{on})

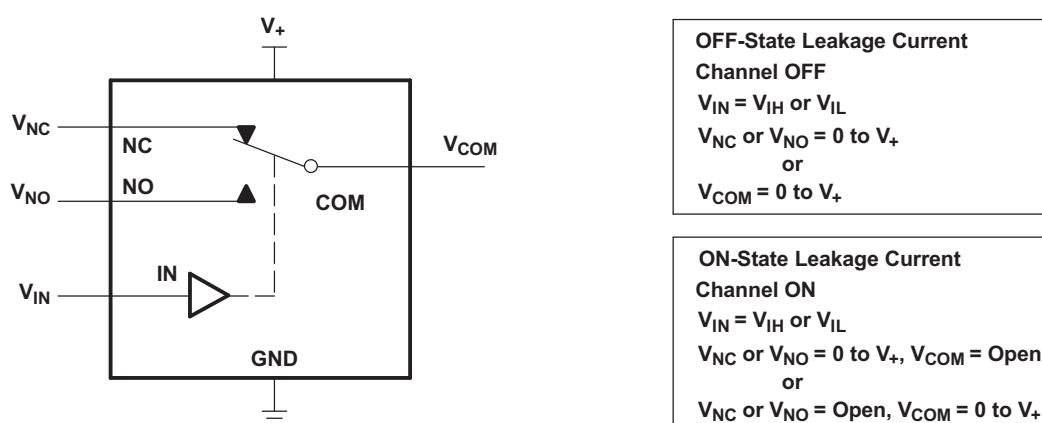


Figure 10. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

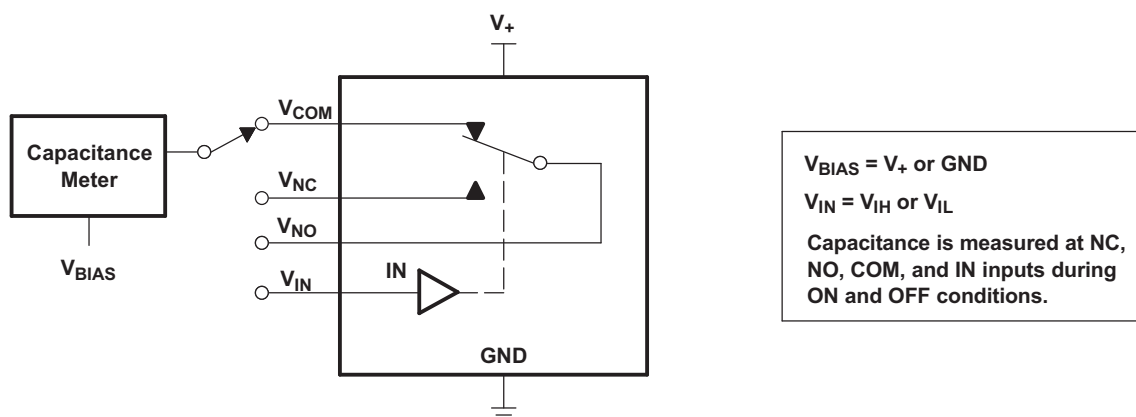


Figure 11. Capacitance (C_{IN} , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)

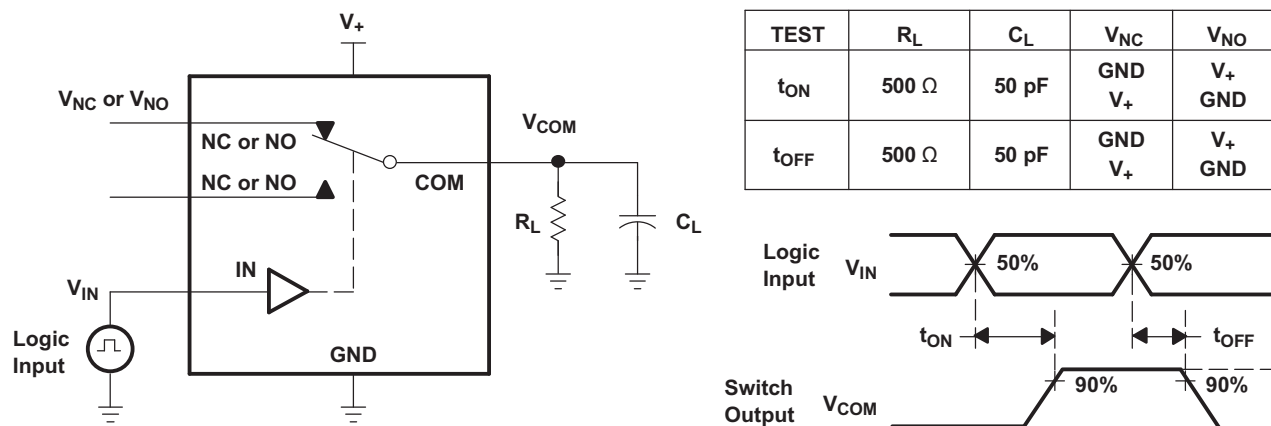


Figure 12. Turnon (t_{ON}) and Turnoff (t_{OFF}) Time

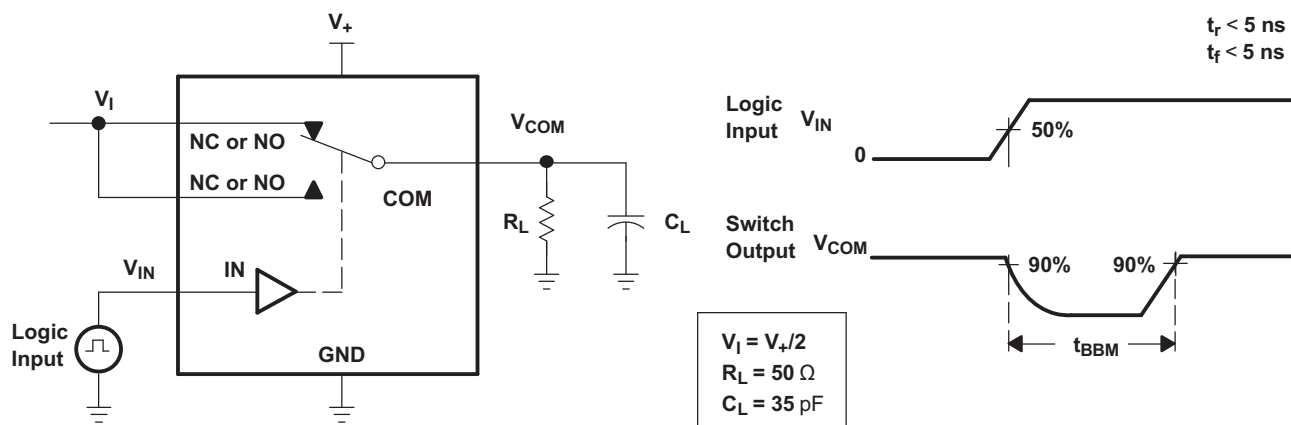


Figure 13. Break-Before-Make (t_{BBM}) Time

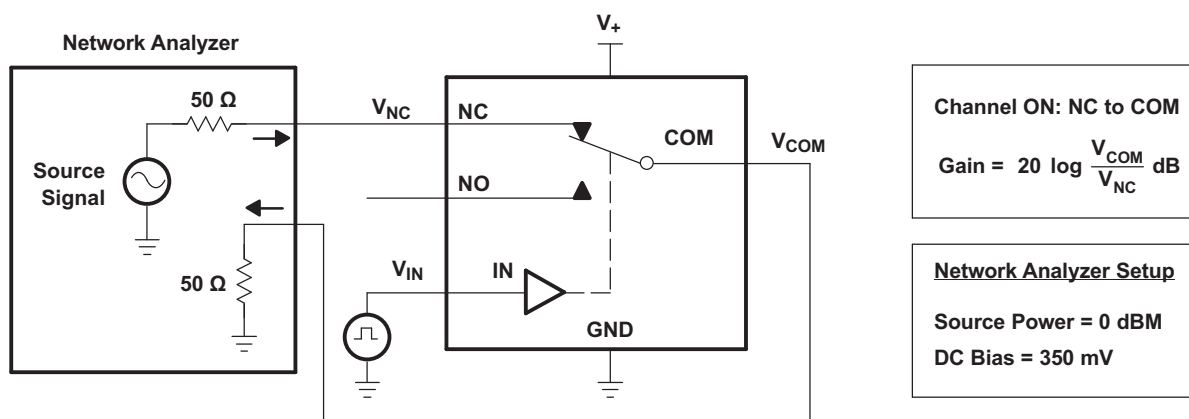


Figure 14. Frequency Response (BW)

Parameter Measurement Information (continued)

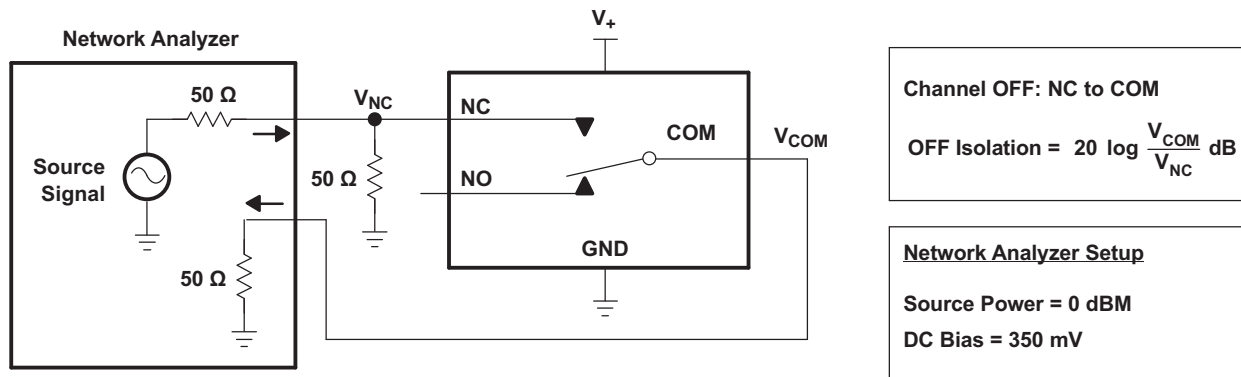


Figure 15. OFF Isolation (O_{ISO})

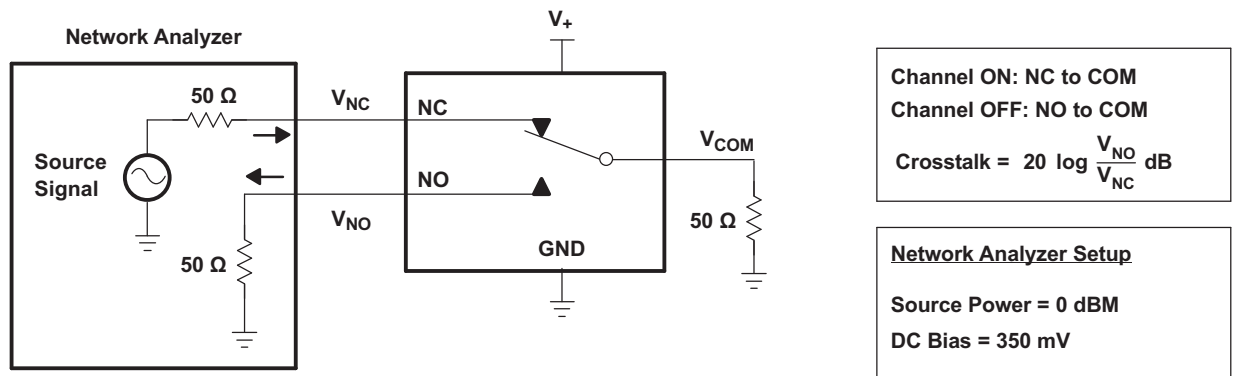


Figure 16. Crosstalk (X_{TALK})

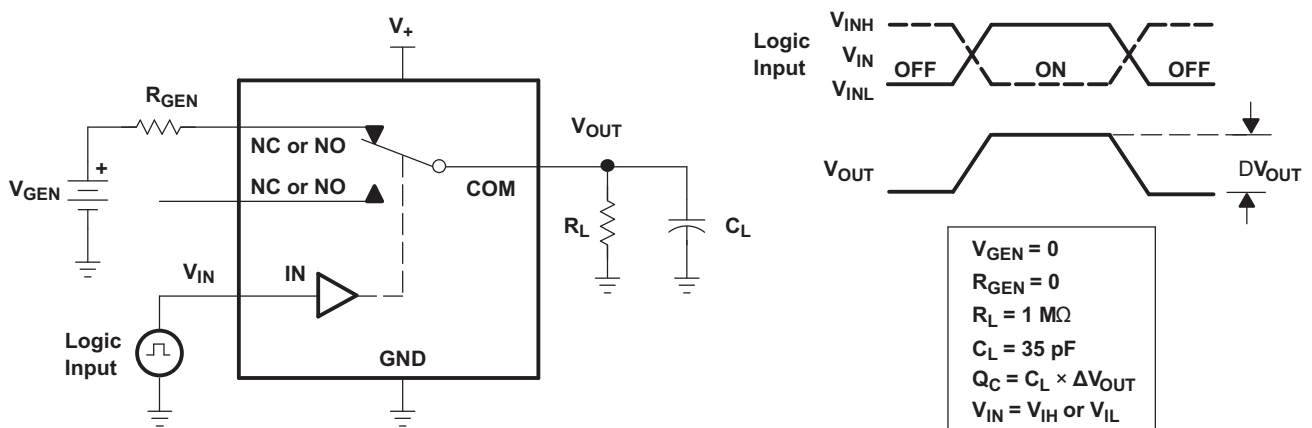


Figure 17. Charge Injection (Q_C)

Parameter Measurement Information (continued)

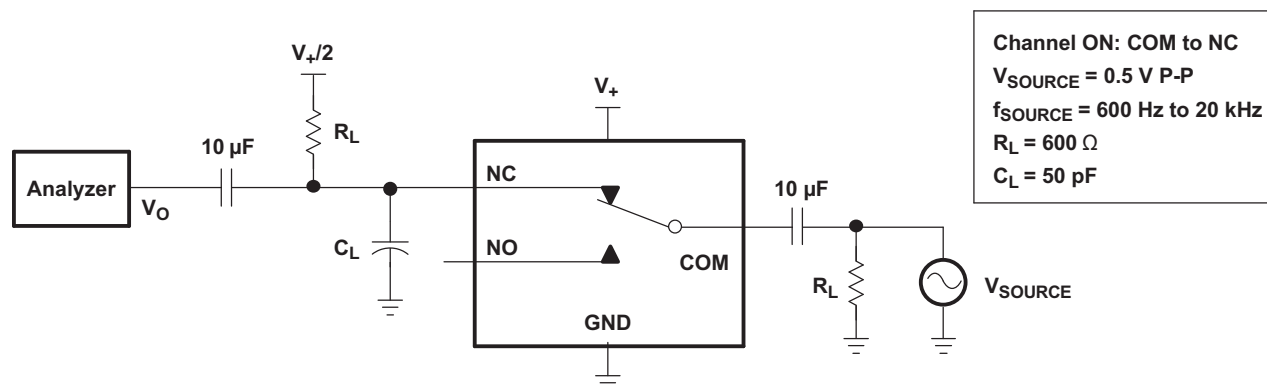


Figure 18. Total Harmonic Distortion (THD)

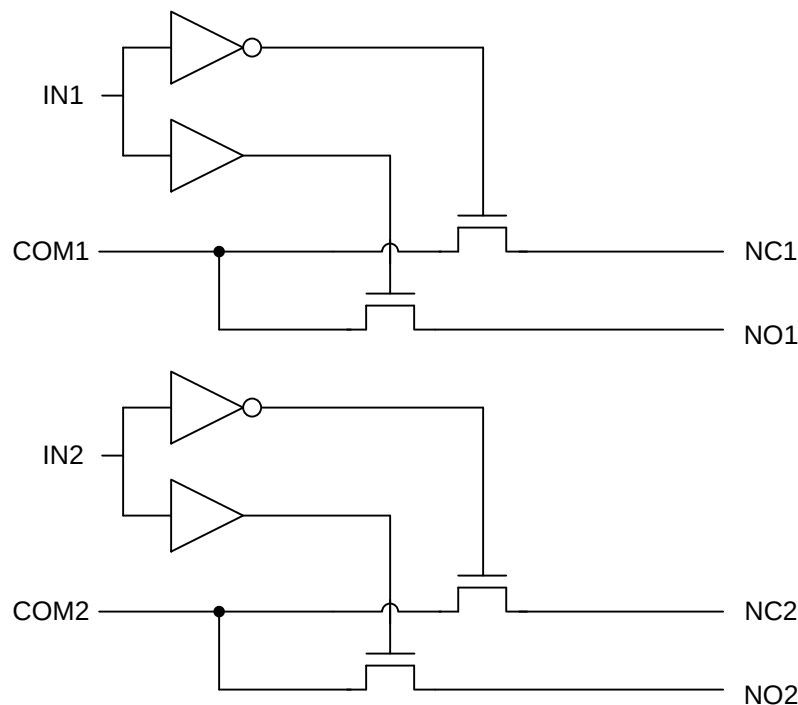
8 Detailed Description

8.1 Overview

The TS5A23157 is a dual single-pole-double-throw (SPDT) solid-state analog switch. The TS5A23157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin when the IN pin is low. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A23157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A23157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion. The control inputs are 5-V tolerant, allowing control signals to be present without V_{CC} .

8.4 Device Functional Modes

[Table 1](#) lists the functional modes for TS5A23157.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

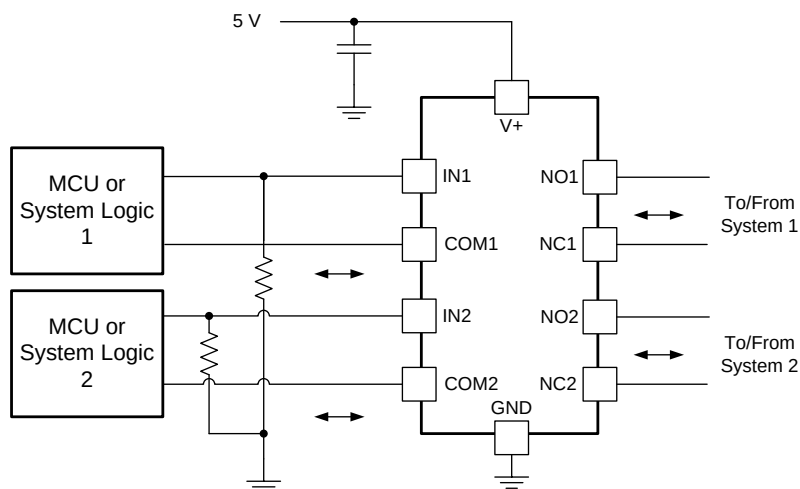


Figure 19. System Schematic for TS5A23157

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in [Recommended Operating Conditions](#). A decoupling capacitor is recommended on the V_+ pin. See [Power Supply Recommendations](#) for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

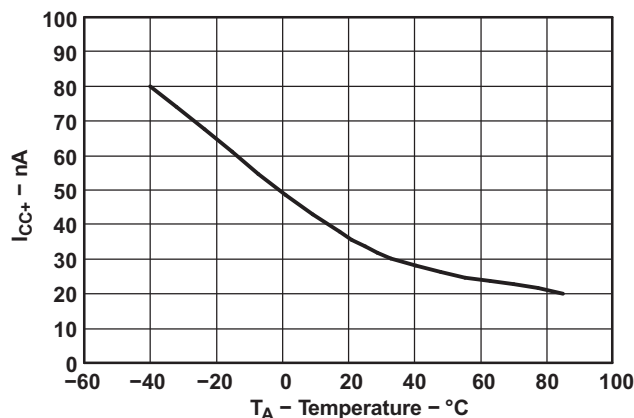


Figure 20. Power-Supply Current vs Temperature ($V_+ = 5\text{ V}$)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

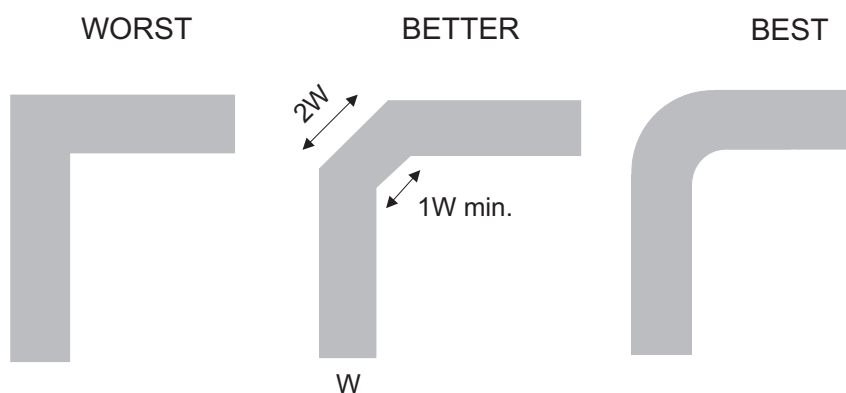


Figure 21. Trace Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 2. 参数 说明

符号	说明
V_{COM}	COM 处的电压
V_{NC}	NC 处的电压
V_{NO}	NO 处的电压
r_{on}	通道导通时 COM 和 NC 端口之间或 COM 和 NO 端口之间的电阻
Δr_{on}	通道间 r_{on} 的差值
$r_{on(Flat)}$	额定条件范围内, 同一通道内 r_{on} 最大值与最小值之间的差值
$I_{NC(OFF)}$	相应通道 (NC 到 COM) 处于关断状态时, 在 NC 端口测得的泄漏电流在最坏输入和输出条件下
$I_{NO(OFF)}$	在最不理想的输入和输出条件下, 相应通道 (NO 到 COM) 处于关断状态时, 在 NO 端口测得的泄漏电流
$I_{NC(ON)}$	相应通道 (NC 到 COM) 处于导通状态且输出 (COM) 处于开路状态时在 NC 端口测量的泄漏电流
$I_{NO(ON)}$	相应通道 (NO 到 COM) 处于导通状态且输出 (COM) 处于开路状态时在 NO 端口测量的泄漏电流
$I_{COM(ON)}$	相应通道 (NO 到 COM 或 NC 到 COM) 处于导通状态且输出 (NC 或 NO) 处于开路状态时在 COM 端口测量的泄漏电流
V_{IH}	控制输入 (IN) 逻辑高电平的最小输入电压
V_{IL}	控制输入 (IN) 逻辑低电平的最小输入电压
V_{IN}	IN 处的电压
I_{IH}, I_{IL}	在 IN 处测量的泄漏电流
t_{ON}	开关导通时间。此参数是在额定条件范围内, 开关导通时, 通过数字控制 (IN) 信号和模拟输出 (COM/NC/NO) 信号之间的传播延迟测量得出。
t_{OFF}	开关关断时间。此参数是在额定条件范围内, 开关关断时, 通过数字控制 (IN) 信号和模拟输出 (COM/NC/NO) 信号之间的传播延迟测量得出。
t_{BBM}	先断后合时间。此参数是在额定条件范围内, 控制信号改变状态时, 通过两个相邻模拟通道 (NC 和 NO) 的输出之间的传播延迟测量得出。
Q_C	电荷注入是测量从控制 (IN) 输入到模拟 (NC、NO、或 COM) 输入产生的不需要的信号耦合的方法。电荷注入以库仑 (C) 为单位, 可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入, $Q_C = C_L \times \Delta V_O$, C_L 是负载电容, ΔV_O 是模拟输出电压的变化。
$C_{NC(OFF)}$	相应通道 (NC 到 COM) 关断时 NC 端口的电容
$C_{NO(OFF)}$	相应通道 (NC 到 COM) 关断时 NO 端口的电容
$C_{NC(ON)}$	相应通道 (NC 到 COM) 导通时 NC 端口的电容
$C_{NO(ON)}$	相应通道 (NC 到 COM) 导通时 NO 端口的电容
$C_{COM(ON)}$	相应通道 (COM 到 NC 或 COM 到 NO) 导通时 COM 端口的电容
C_{IN}	IN 的电容
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位, 当相应通道 (NC 到 COM 或 NO 到 COM) 处于关断状态时, 在额定频率下测量得出。关断隔离, $O_{ISO} = 20 \log (V_{NC}/V_{COM})$ dB, V_{COM} 是输入, V_{NC} 是输出。
X_{TALK}	串扰是测量从导通通道到关断通道 (NC 到 NO 或 NO 到 NC) 产生的不必要信号耦合的方法。串扰在额定频率下测量得出且以 dB 为单位。串扰, $X_{TALK} = 20 \log (V_{NC1}/V_{NO1})$, V_{NO1} 是输入, V_{NC1} 是输出。
BW	开关带宽。这是导通通道增益低于直流增益 -3dB 时的频率。增益的计算方程式是 $20 \log (V_{NC}/V_{COM})$ dB, V_{NC} 是输出, V_{COM} 是输入。
I_+	静态电源电流, 以及 V_+ 或 GND 的控制 (IN) 引脚
ΔI_+	这是在额定电压下的每个控制 (IN) 输入 I_+ 增量, 而不是在 V_+ 或 GND 的控制输入增量。

表 3. 特性总结

配置	2:1 多路复用器/多路解复用器 (2 × SPDT)
通道数量	2
导通状态电阻 (r_{on})	10Ω

表 3. 特性总结 (接下页)

配置	2:1 多路复用器/多路解复用器 (2 × SPDT)
通道间的导通状态电阻匹配 (Δr_{on})	0.15 Ω
导通状态电阻稳定性 ($r_{on(flat)}$)	4 Ω
导通/关断时间 (t_{ON}/t_{OFF})	5.7ns/3.8ns
先断后合时间 (t_{BBM})	0.5ns
电荷注入 (Q_C)	7pC
带宽 (BW)	220MHz
关断 (O_{SIO})	10MHz 时为 -65dB
串扰 9XTALK)	10MHz 时为 -66dB
总谐波失真 (THD)	0.01%
泄漏电流 ($I_{COM(OFF)}/I_{NC(OFF)}$)	$\pm 1\mu A$
封装选项	10 引脚 DGS 和 RSE

12.2 文档支持

12.2.1 相关文档

如需相关文档, 请参阅:

- 《CMOS 输入缓慢变化或悬空的影响》, [SCBA004](#)

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 **TI 的工程师对工程师 (E2E) 社区**。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中, 您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且不会对此文档进行修订。如需获取此数据表的浏览器版本, 请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23157DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	Samples
TS5A23157DGSRE4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	Samples
TS5A23157DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	Samples
TS5A23157DGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBR	Samples
TS5A23157RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JBO	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

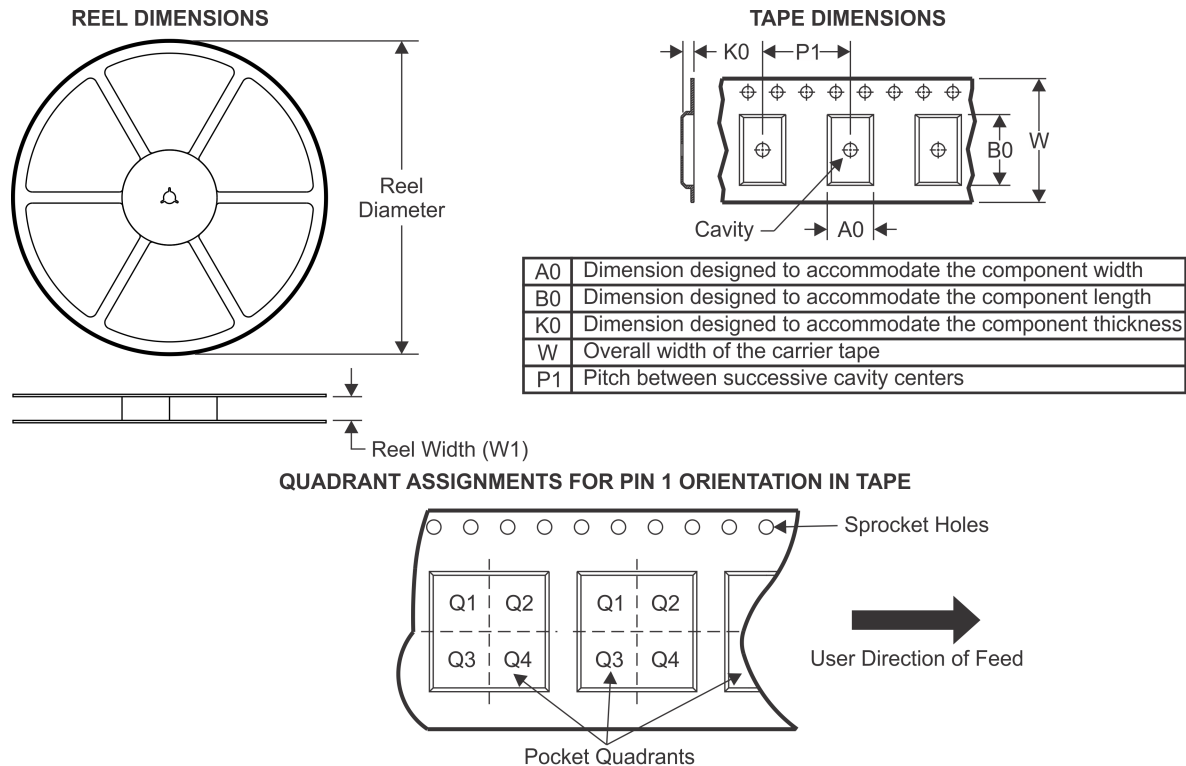
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

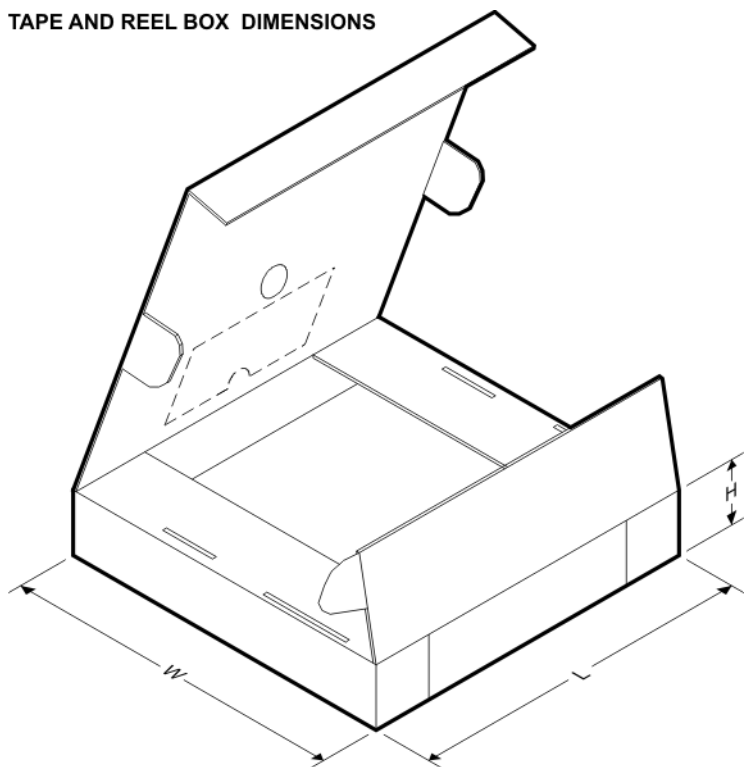
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

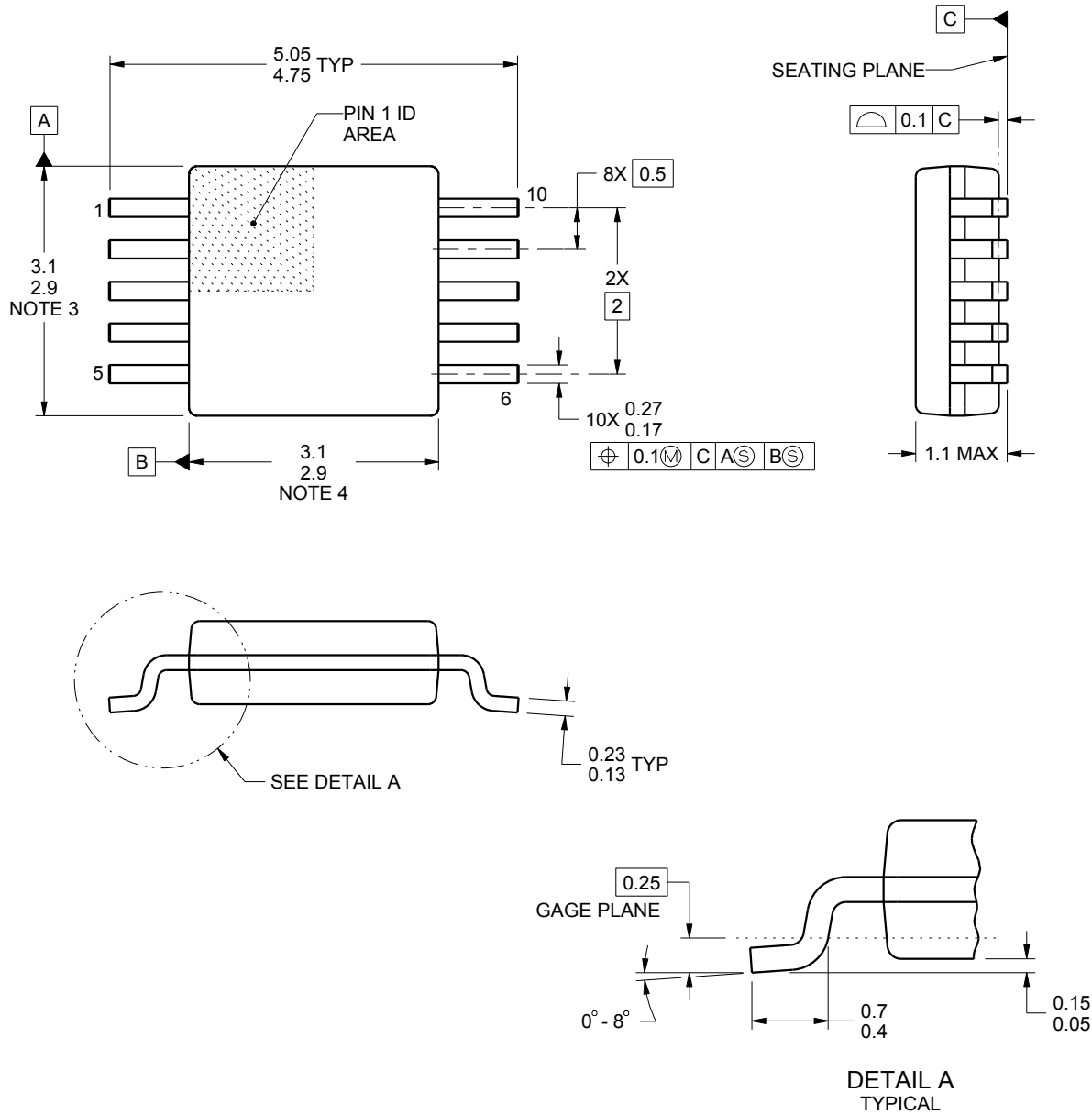
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TS5A23157DGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23157RSER	UQFN	RSE	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23157DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A23157DGSR	VSSOP	DGS	10	2500	346.0	346.0	35.0
TS5A23157DGST	VSSOP	DGS	10	250	358.0	335.0	35.0
TS5A23157RSE	UQFN	RSE	10	3000	200.0	183.0	25.0



4221984/A 05/2015

NOTES:

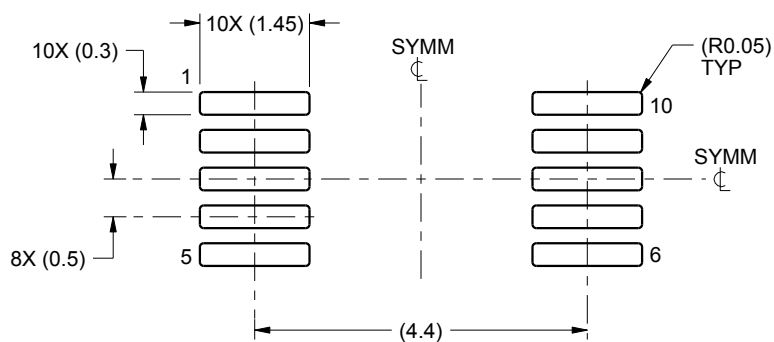
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

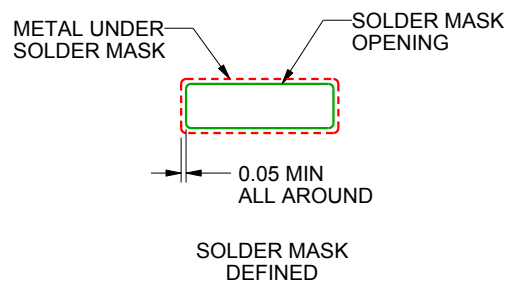
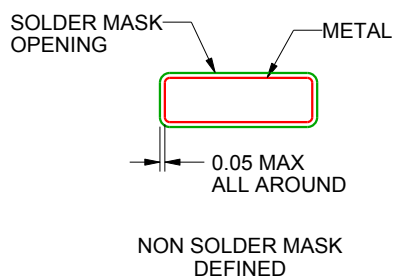
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

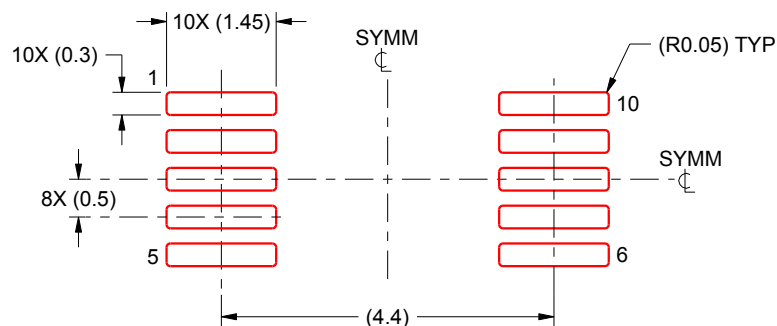
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

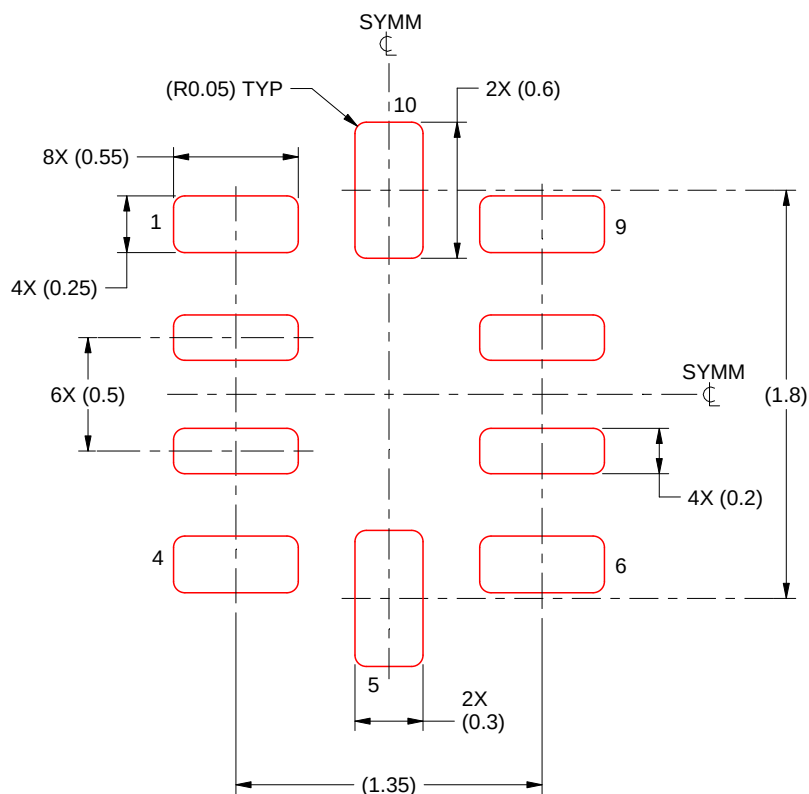
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE STENCIL DESIGN

RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2021 德州仪器半导体技术（上海）有限公司