适用于成本敏感型系统的 TLV930x 40V、1MHz、RRO 运算放大器

1 特性

- 低失调电压：±0.5mV
- 低失调电压漂移：±2μV/°C
- 低噪声：1kHz 时为 33nV/√Hz
- 高共模抑制：110dB
- 低偏置电流：±10pA
- 轨至轨输出
- 宽带宽：1MHz GBW
- 高压摆率：3V/μs
- 低静态电流：每个放大器 150μA
- 宽电源电压范围：±2.25V 至 ±20V，4.5V 至 40V
- 强大的 EMI 性能：在 1GHz 时为 72dB
- 支持多路复用器/比较器的输入：
  - 电源轨的差分和共模输入电压范围
- 行业标准封装：
  - SOT-23-5 和 SC70 单体封装
  - SOIC-8、TSSOP-8 和 VSSOP-8 双列封装
  - 四通道电源版本采用 SOIC-14 和 TSSOP-14 封装

2 应用

- 电网基础设施：断路器
- 电子销售点 (EPOS)
- 电机驱动：交流和伺服驱动器电源
- 楼宇自动化
- 室内外照明
- 高精度高电压比较器

3 说明

TLV930x 系列（TLV9301、TLV9302 和 TLV9304）是 40V 成本优化型运算放大器系列。这些器件具有出色的通用直流和交流规格，包括轨至轨输出、低失调电压（典型值为 ±0.5mV）、低温漂（典型值为 ±2μV/°C）和 1MHz 带宽。

TLV930x 具有便利的 特性 ，例如宽差分输入电压范围、高输出电流 (±60mA) 以及高压摆率 (3V/μs)，是一款可靠的运算放大器，适用于高电压成本敏感型 应用中的机械继电器。

TLV930x 系列运算放大器采用标准封装，额定工作温度范围为 –40°C 至 125°C。

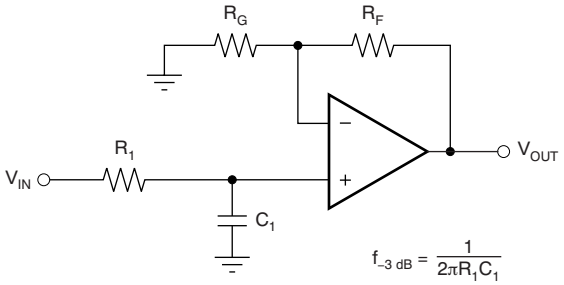
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV9301	SOT-23 (5)(2)	2.90mm × 1.60mm
	SC70 (5)(2)	2.00mm × 1.25mm
TLV9302	SOIC (8)	4.90mm × 3.91mm
	TSOT (8)(2)	2.90mm × 1.60mm
	TSSOP (8)(2)	4.40mm x 3.00mm
	VSSOP (8)(2)	2.30mm × 2.00mm
TLV9304	SOIC (14)(2)	8.65mm × 3.91mm
	TSSOP (14)(2)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

(2) 此封装仅为预览版。

TLV930x 应用于单极低通滤波器



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

目录

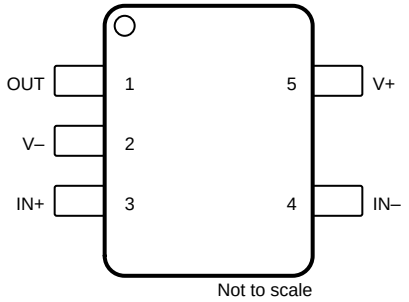
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (February 2019) to Revision A	Page
• 已更改 将 TLV9302 器件状态从*预告信息* 更改为*生产数据*	1

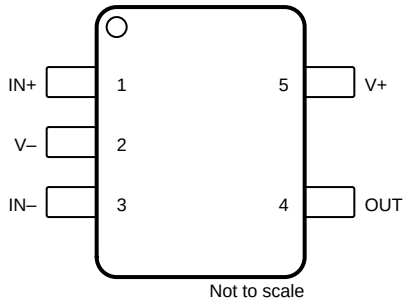
5 Pin Configuration and Functions

TLV9301 DBV Package(1)
5-Pin SOT-23
Top View



(1) Package is preview only.

TLV9301 DCK Package(1)
5-Pin SC70
Top View

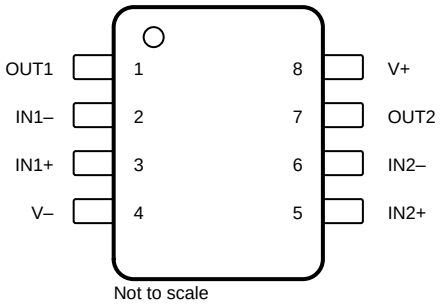


(1) Package is preview only.

Pin Functions: TLV9301

PIN			I/O	DESCRIPTION
NAME	DBV and DRL	DCK		
+IN	3	1	I	Noninverting input
–IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

TLV9302 D, DDF, DGK, and PW Packages(1)
8-Pin SOIC, TSOT, TSSOP, and VSSOP
Top View

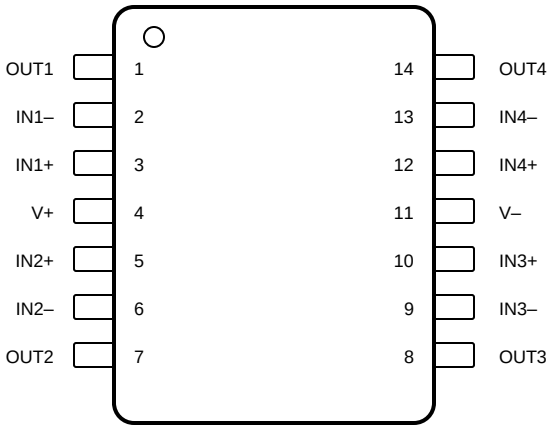


(1) DDF, DGK, and PW packages are preview only.

Pin Functions: TLV9302

PIN		I/O	DESCRIPTION
NAME	SOIC, TSOT, TSSOP, and VSSOP		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

TLV9304 D and PW Packages(1)
14-Pin SOIC and TSSOP
Top View



Not to scale

(1) Package is preview only.

Pin Functions: TLV9304

PIN		I/O	DESCRIPTION
NAME	SOIC and TSSOP		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(2)		V_S + 0.2	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	4.5	40	V
V_I	Input voltage range	(V–) – 0.1	(V+) – 2	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC(1)		TLV9301		UNIT
		DBV (SOT-23)(2)	DCK (SC70)(2)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TLV9301.

6.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		TLV9302				UNIT
		D (SOIC)	DDF (SOT-23-8)(2)	DGK (VSSOP)(2)	PW (TSSOP)(2)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.7	TBD	TBD	188.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.7	TBD	TBD	77.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.2	TBD	TBD	119.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.8	TBD	TBD	14.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.4	TBD	TBD	117.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	TBD	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TLV9302.

6.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		TLV9304		UNIT
		D (SOIC)(2)	PW (TSSOP)(2)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TLV9304.

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.5	±2.5	mV
			T_A = –40°C to 125°C			±2.75	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–	T_A = –40°C to 125°C		±2	±5	µV/V
	Channel separation	f = 0 Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			6		μV_{PP}
					1		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			33		nV/√Hz
		f = 10 kHz			30		
i_N	Input current noise	f = 1 kHz			5		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = 40 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V	T_A = –40°C to 125°C	95	110		dB
		V_S = 4.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V			90		
		(V+) – 2 V < V_{CM} < (V+) + 0.1 V		See *Common-Mode Voltage Range*			
INPUT CAPACITANCE							
Z_{ID}	Differential				110 || 4		MΩ || pF
Z_{ICM}	Common-mode				6 || 1.5		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		120	130		dB
			T_A = –40°C to 125°C	116	127		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			3		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			5		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			2.5		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			6		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			3.5		
	Phase margin	G = +1, R_L = 10 kΩ, C_L = 20 pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			1		µs
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 1 V_{RMS}, G = -1, f = 1 kHz			0.003%		

Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 40 V, R_L = no load		3		mV
			V_S = 40 V, R_L = 10 kΩ		50	75	
			V_S = 40 V, R_L = 2 kΩ		250	350	
		Negative rail headroom	V_S = 4.5 V, R_L = no load		1		
			V_S = 4.5 V, R_L = 10 kΩ		20	30	
			V_S = 4.5 V, R_L = 2 kΩ		40	75	
I_{SC}	Short-circuit current				±60		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			600		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			150	175	µA
			T_A = –40°C to 125°C			175	

6.8 Typical Characteristics

表 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3 , 图 4
Offset Voltage vs Common-Mode Voltage	图 5
Offset Voltage vs Power Supply	图 6
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EMIRR vs Frequency	图 40

6.9 Typical Characteristics

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

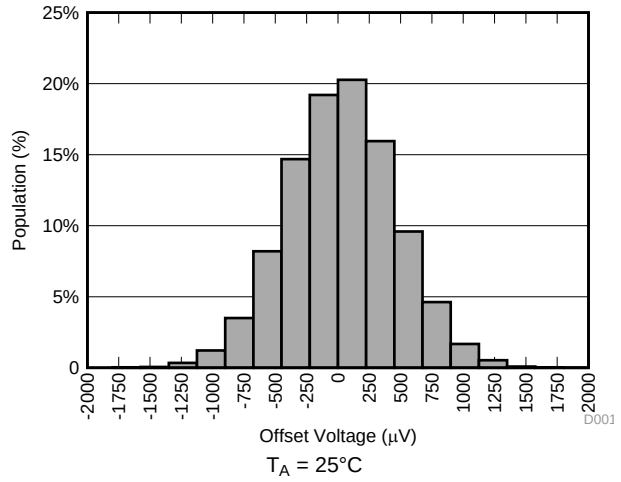


图 1. Offset Voltage Production Distribution

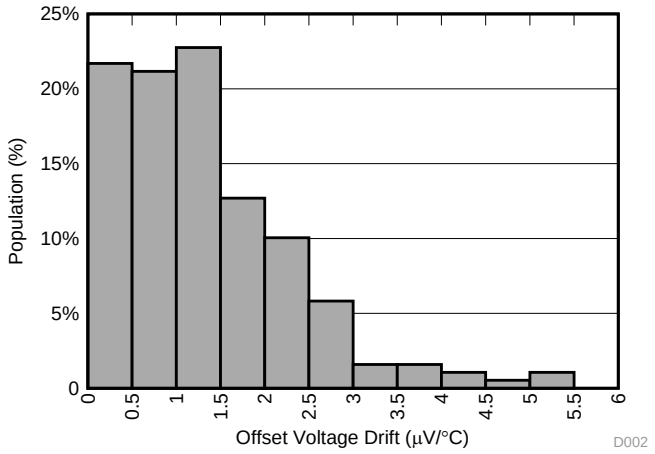


图 2. Offset Voltage Drift Distribution

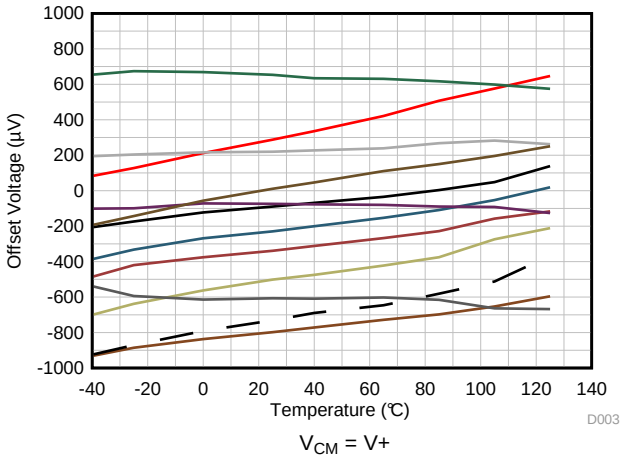


图 3. Offset Voltage vs Temperature

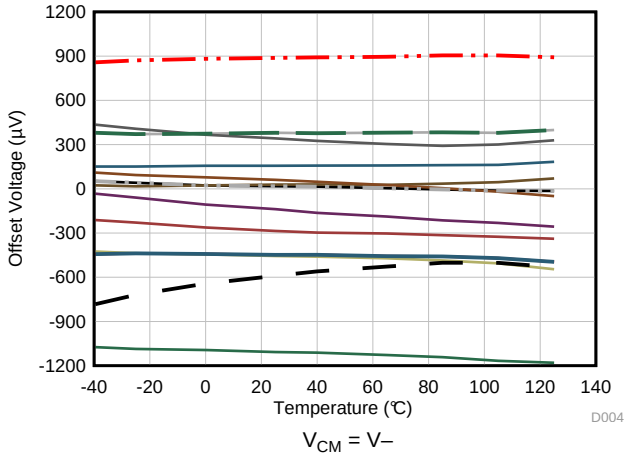


图 4. Offset Voltage vs Temperature

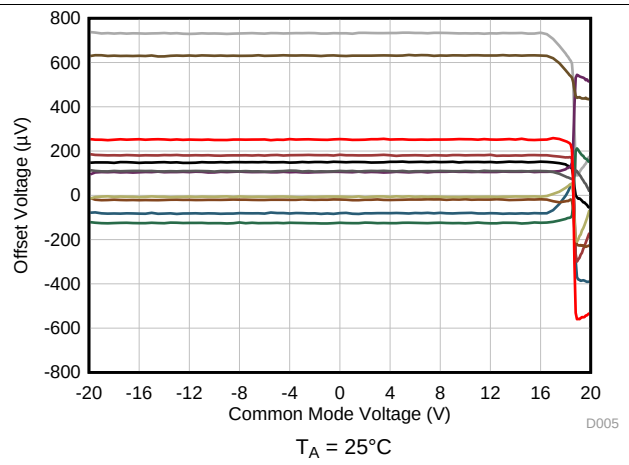


图 5. Offset Voltage vs Common-Mode Voltage

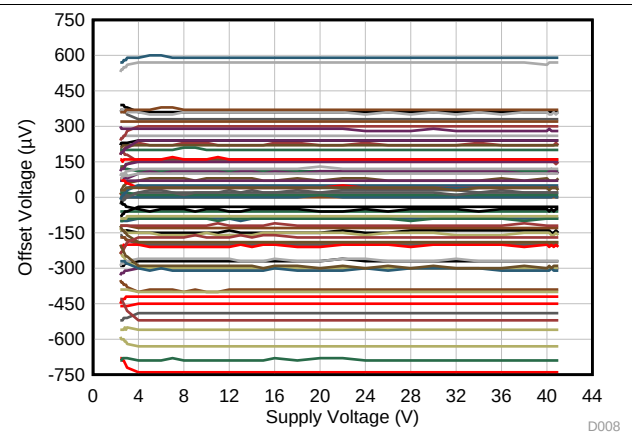
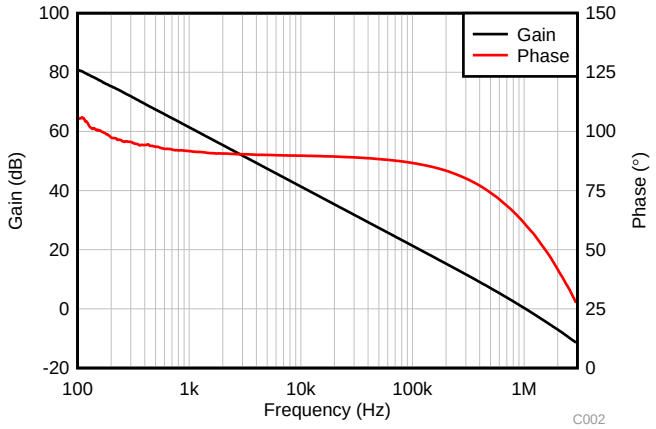


图 6. Offset Voltage vs Power Supply

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



C_{LOAD} = 15 pF

图 7. Open-Loop Gain and Phase vs Frequency

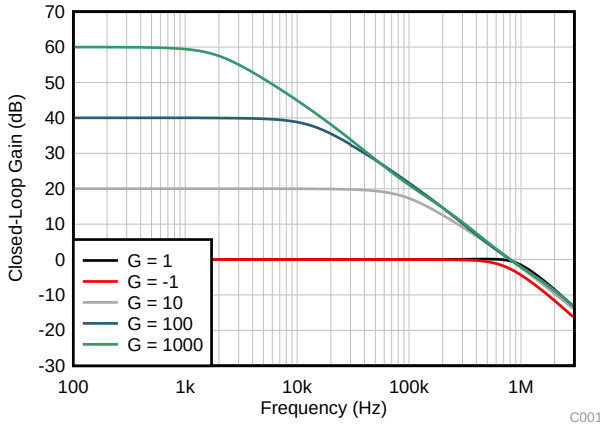


图 8. Closed-Loop Gain and Phase vs Frequency

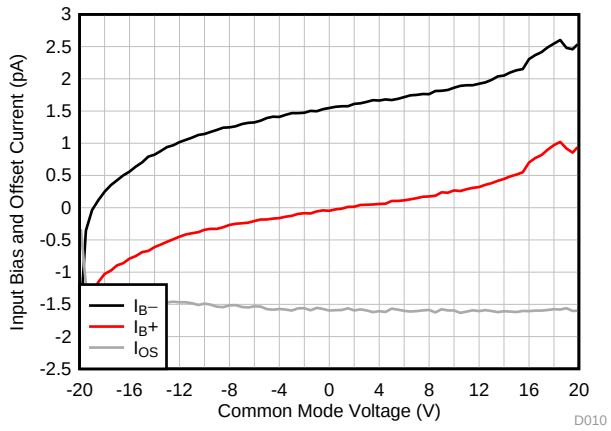


图 9. Input Bias Current vs Common-Mode Voltage

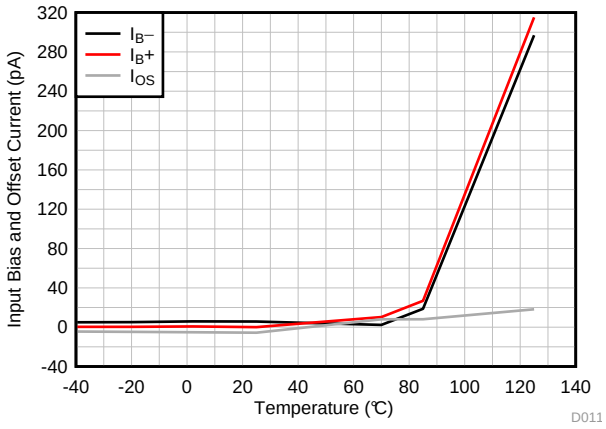


图 10. Input Bias Current vs Temperature

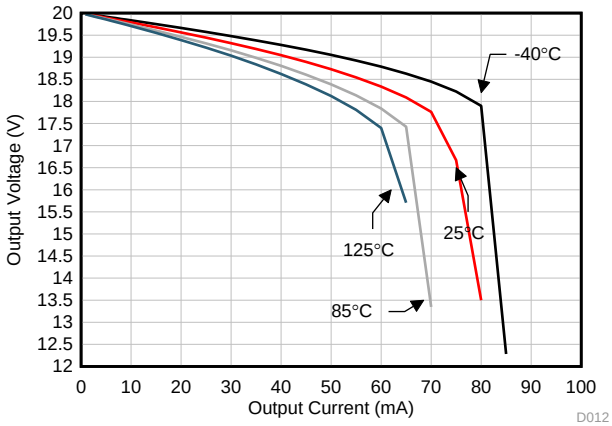


图 11. Output Voltage Swing vs Output Current (Sourcing)

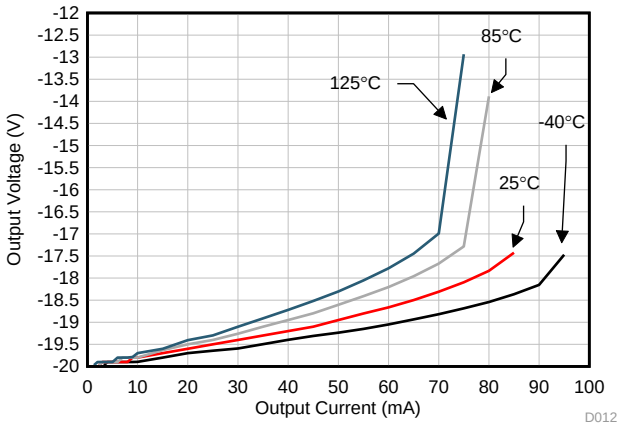


图 12. Output Voltage Swing vs Output Current (Sinking)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

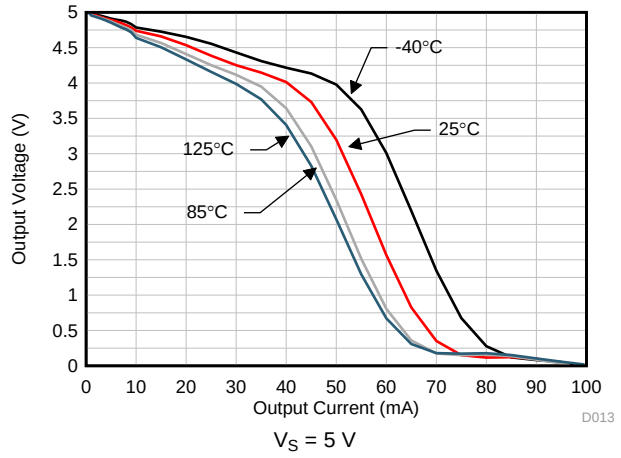


图 13. Output Voltage Swing vs Output Current (Sourcing)

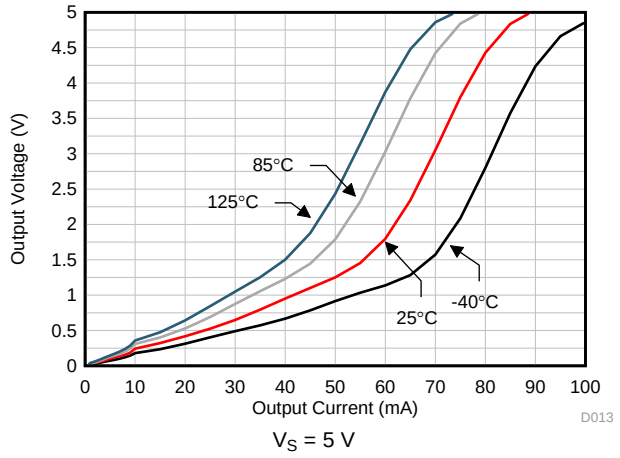


图 14. Output Voltage Swing vs Output Current (Sinking)

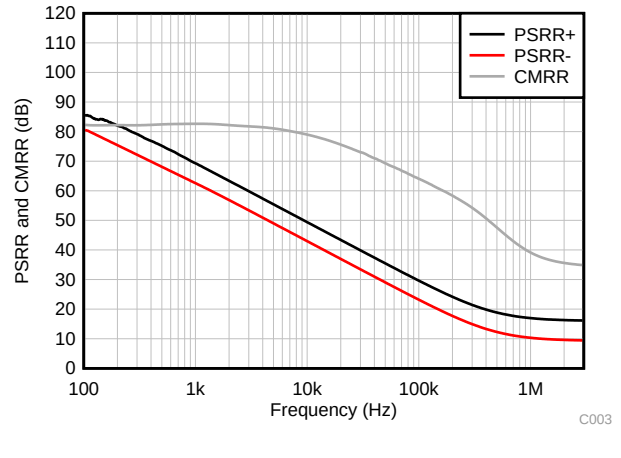


图 15. CMRR and PSRR vs Frequency

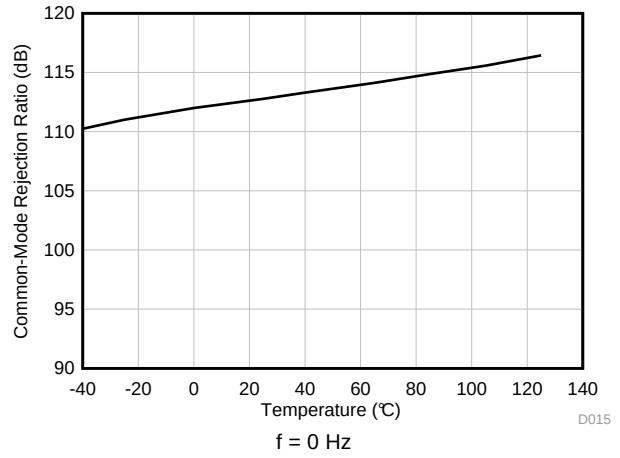


图 16. CMRR vs Temperature (dB)

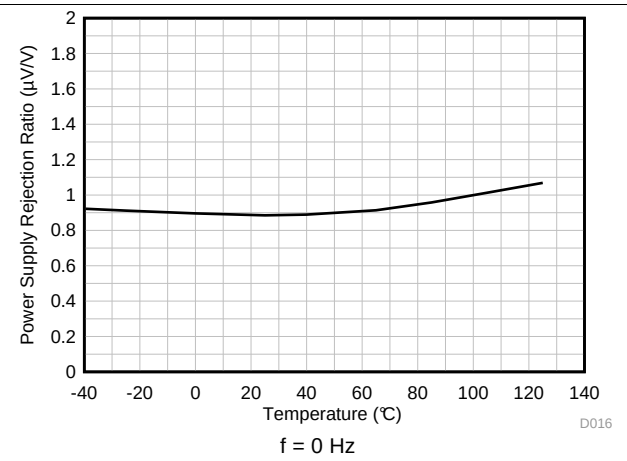


图 17. PSRR vs Temperature (dB)

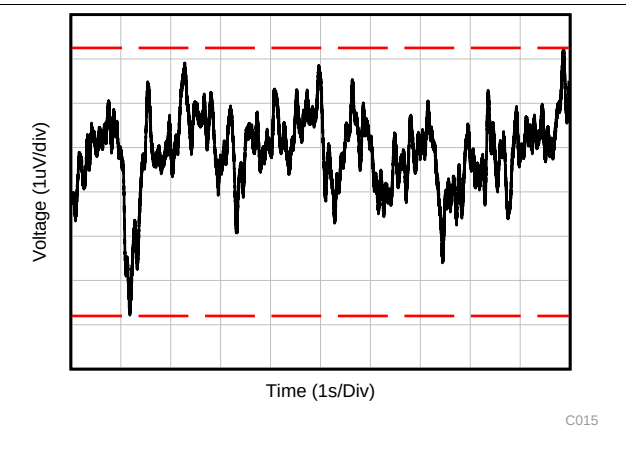


图 18. 0.1-Hz to 10-Hz Noise

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

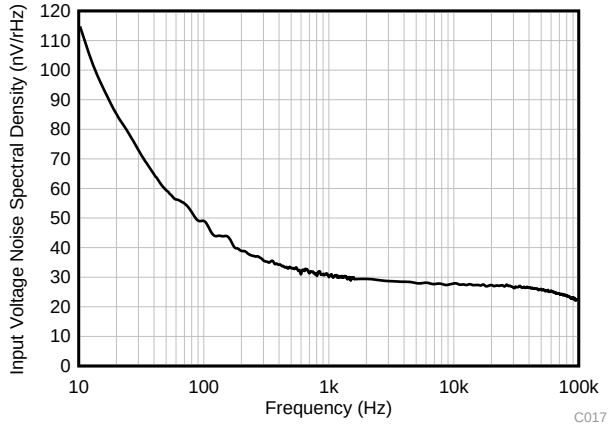
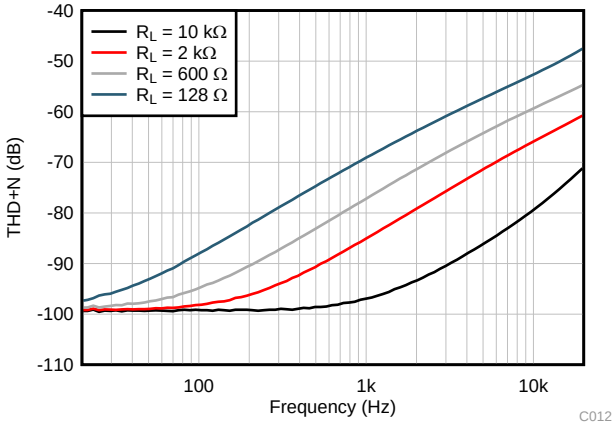
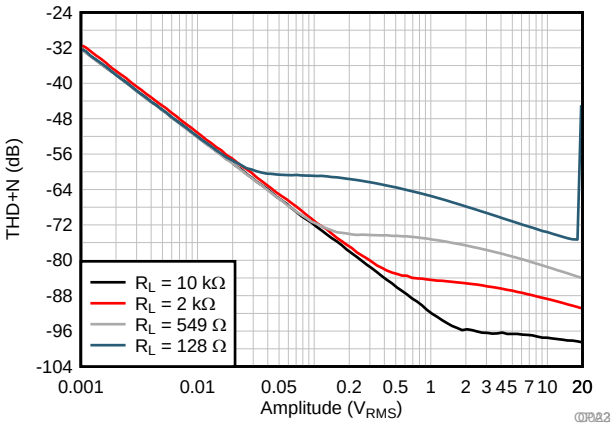


图 19. Input Voltage Noise Spectral Density vs Frequency



BW = 80 kHz, V_{OUT} = 3.5 V_{RMS}

图 20. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

图 21. THD+N vs Output Amplitude

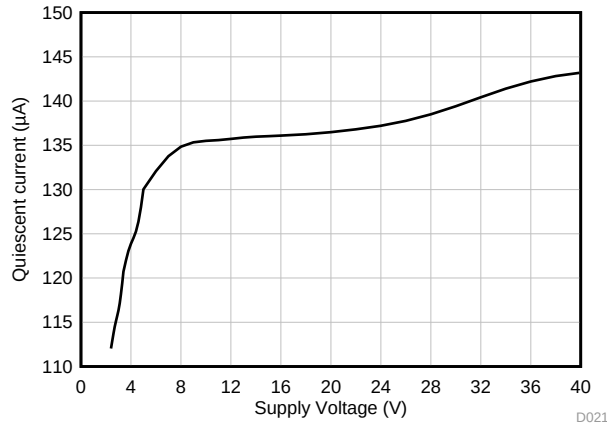


图 22. Quiescent Current vs Supply Voltage

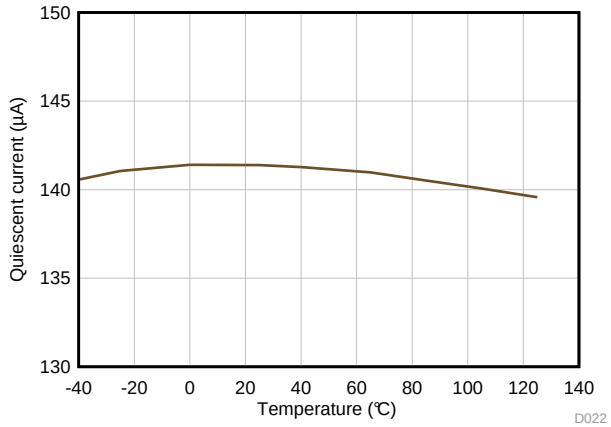


图 23. Quiescent Current vs Temperature

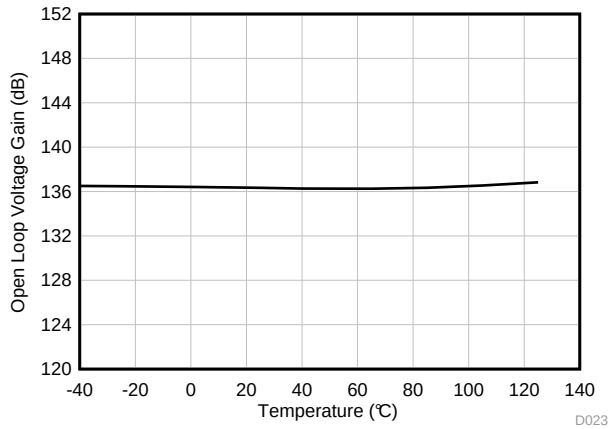


图 24. Open-Loop Voltage Gain vs Temperature (dB)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

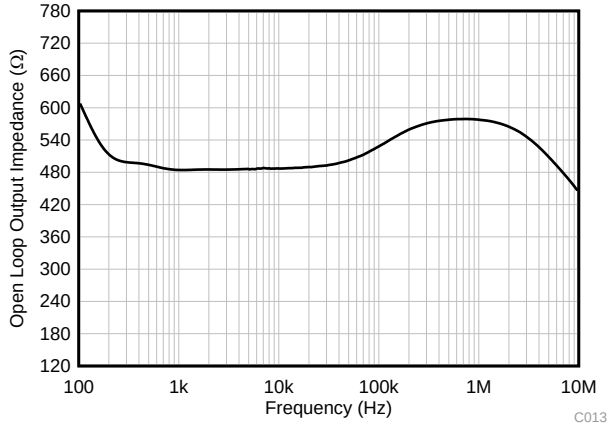
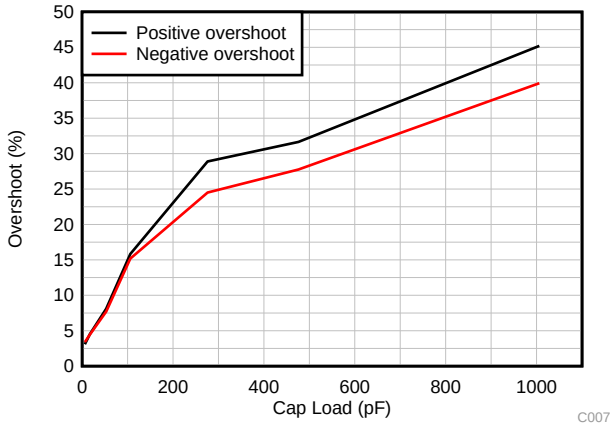
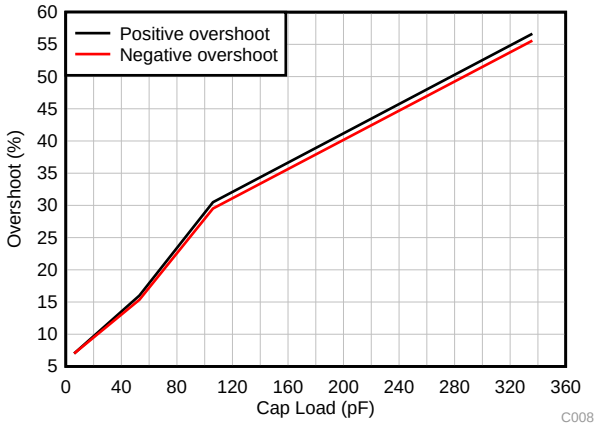


图 25. Open-Loop Output Impedance vs Frequency



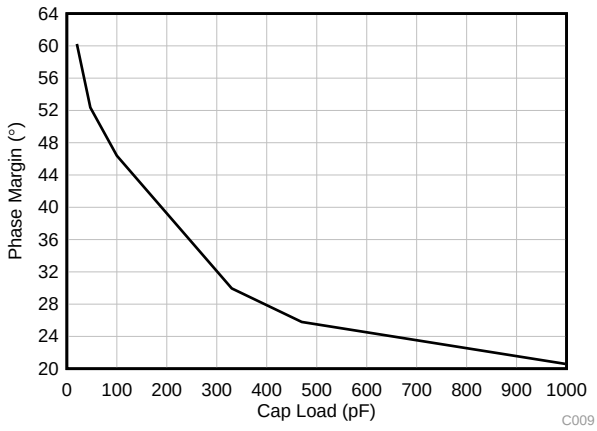
G = –1, 100-mV output step

图 26. Small-Signal Overshoot vs Capacitive Load



G = 1, 100-mV output step

图 27. Small-Signal Overshoot vs Capacitive Load



G = –1, 100-mV output step

图 28. Small-Signal Overshoot vs Capacitive Load

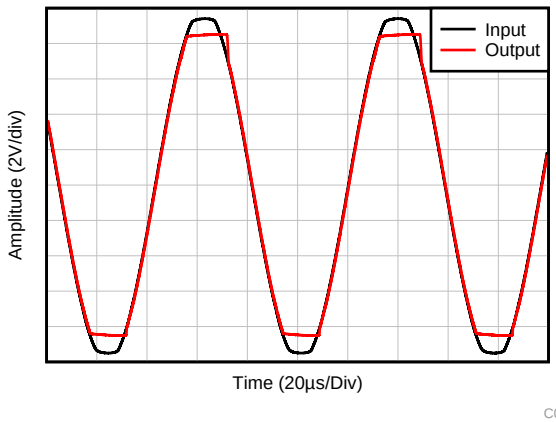
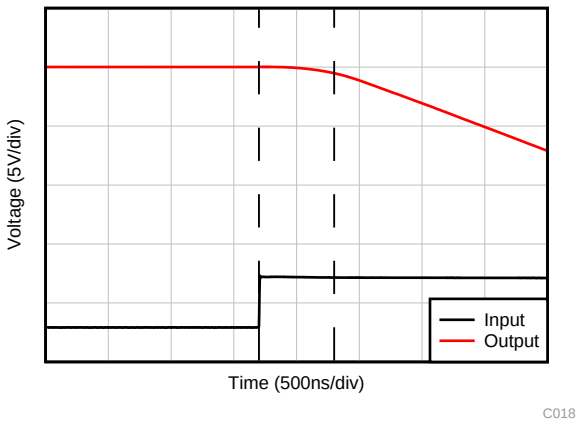


图 29. No Phase Reversal

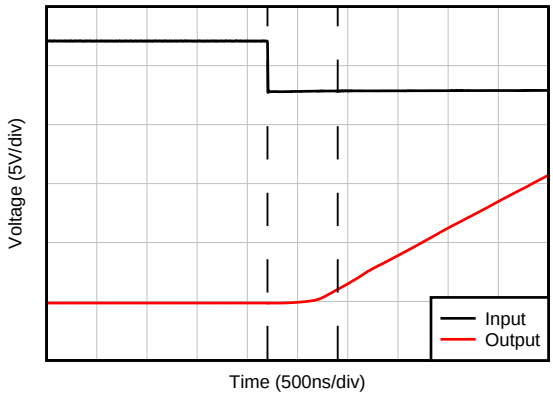


G = –10

图 30. Positive Overload Recovery

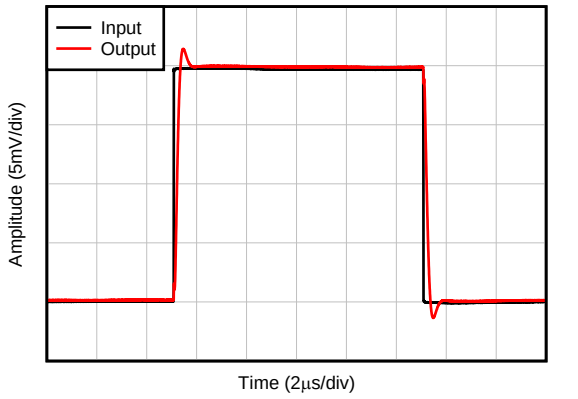
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



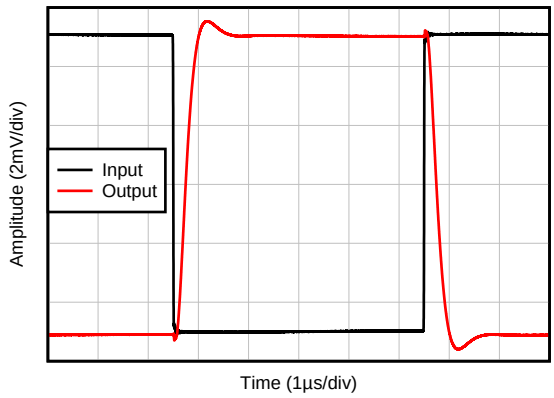
G = –10

图 31. Negative Overload Recovery



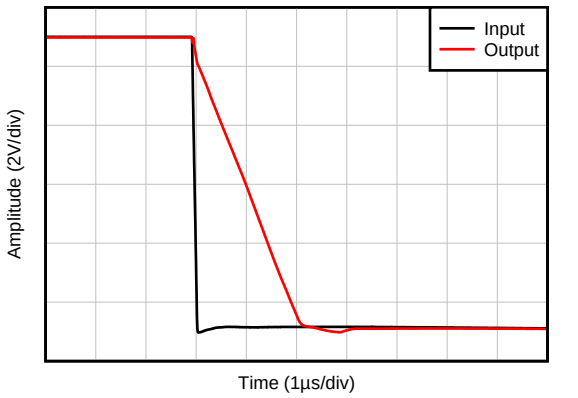
C_L = 20 pF, G = 1, 20-mV step response

图 32. Small-Signal Step Response



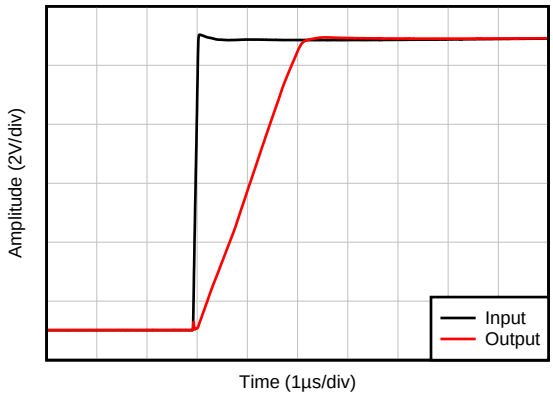
R_L = 1 kΩ, C_L = 20 pF, G = –1, 10-mV step response

图 33. Small-Signal Step Response



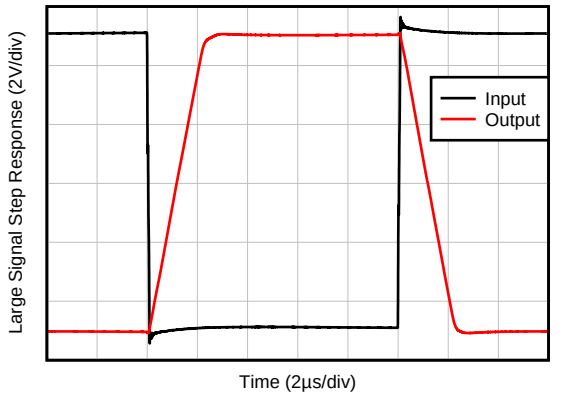
C_L = 20 pF, G = 1

图 34. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

图 35. Large-Signal Step Response (Rising)



C_L = 10 pF, G = –1

图 36. Large-Signal Step Response

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

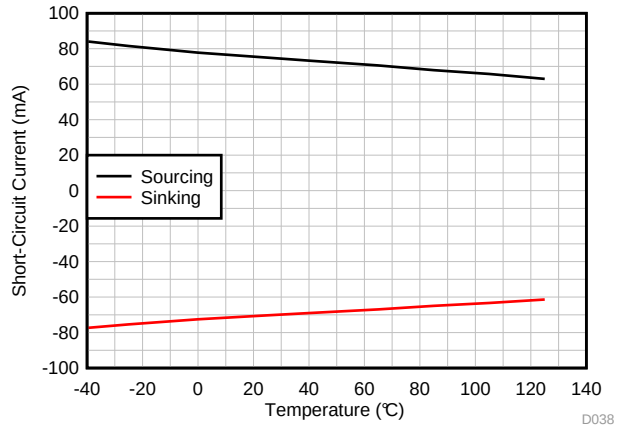


图 37. Short-Circuit Current vs Temperature

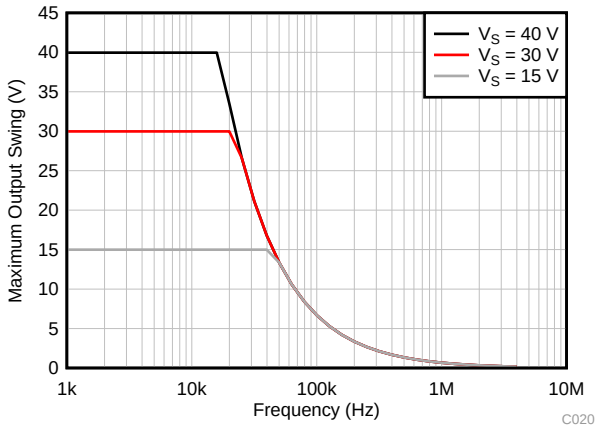


图 38. Maximum Output Voltage vs Frequency

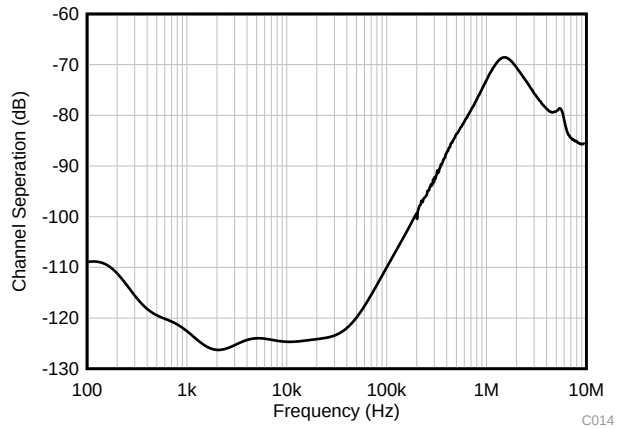


图 39. Channel Separation vs Frequency

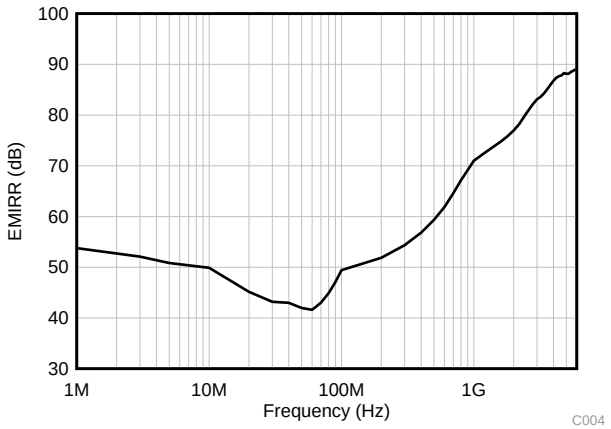


图 40. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7 Detailed Description

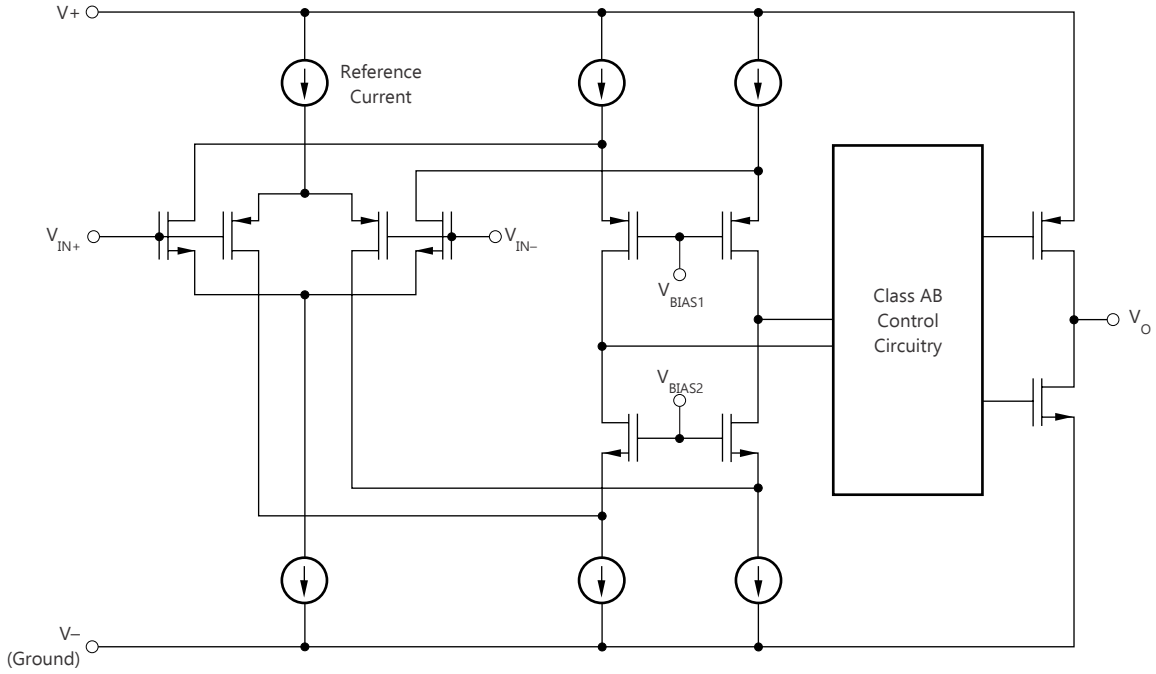
7.1 Overview

The TLV930x family (TLV9301, TLV9302, and TLV9304) is a family of 40-V, cost-optimized operational amplifiers. These devices offer strong general-purpose DC and AC specifications, including rail-to-rail output, low offset (±0.5 mV, typ), low offset drift (±2 µV/°C, typ), and 1-MHz bandwidth.

Convenient features such as wide differential input-voltage range, high output current (±60 mA), and high slew rate (3 V/µs) make the TLV930x a robust operational amplifier for high-voltage, cost-sensitive applications.

The TLV930x family of op amps is available in standard packages and is specified from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Protection Circuitry

The TLV930x uses a patented input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 图 41 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 图 42. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

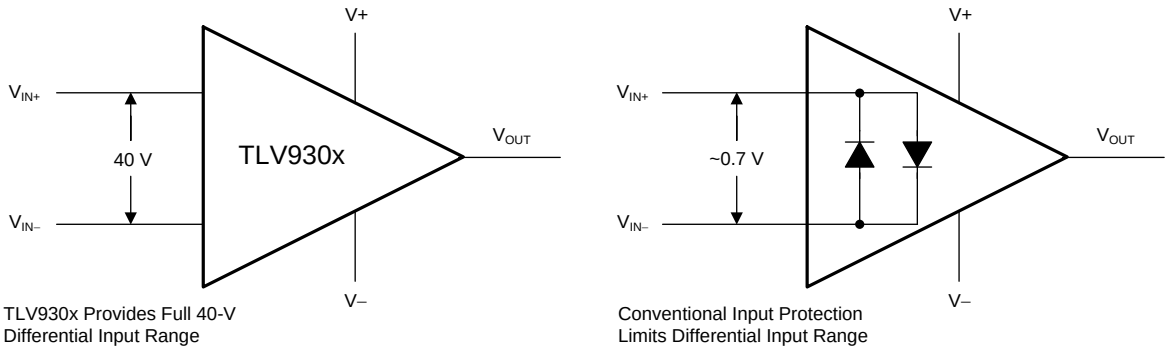


图 41. TLV930x Input Protection Does Not Limit Differential Input Capability

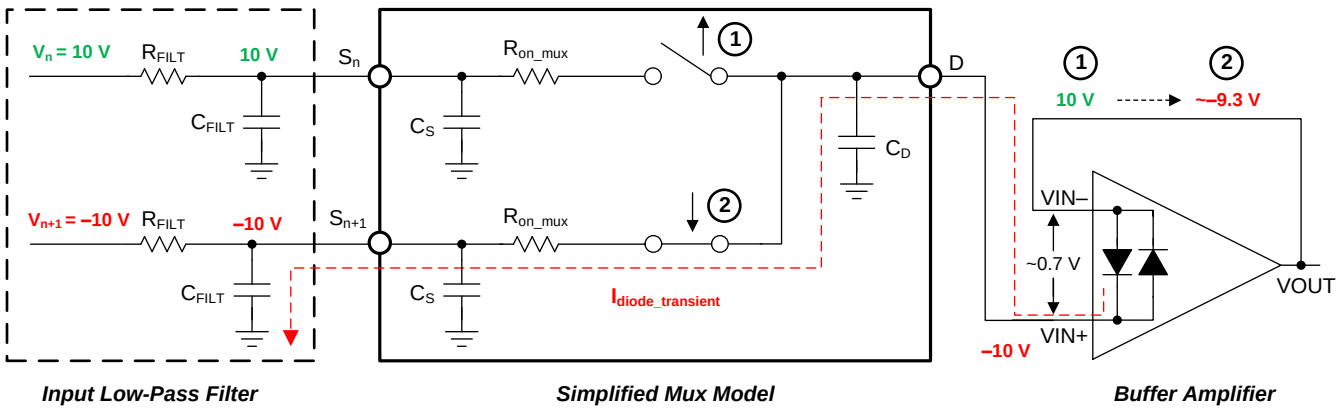


图 42. Back-to-Back Diodes Create Settling Issues

The TLV930x family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The TLV930x tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals.

Feature Description (接下页)

7.3.2 EMI Rejection

The TLV930x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV930x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 43 shows the results of this testing on the TLV930x. 表 2 shows the EMIRR IN+ values for the TLV930x at particular frequencies commonly encountered in real-world applications. 表 2 lists applications that may be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

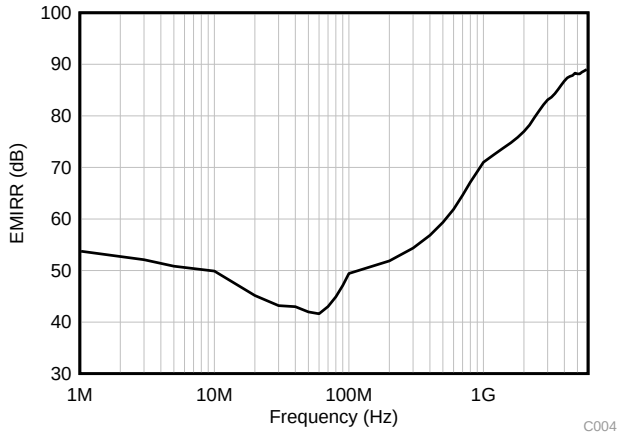


图 43. EMIRR Testing

表 2. TLV930x EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

7.3.3 Phase Reversal Protection

The TLV930x family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV930x is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in 图 44.

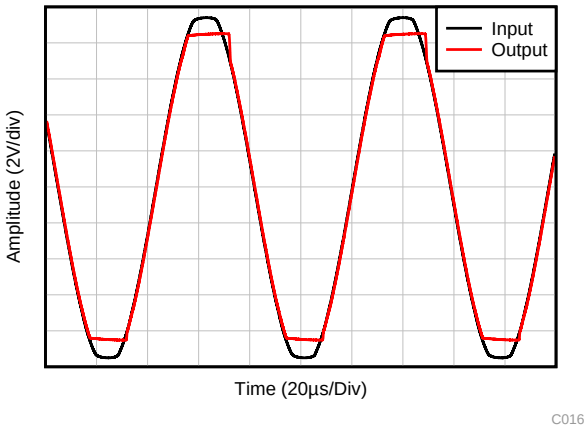


图 44. No Phase Reversal

7.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV930x is 150°C. Exceeding this temperature causes damage to the device. The TLV930x has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. 图 45 shows an application example for the TLV9301 that has significant self heating (159°C) because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. 图 45 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

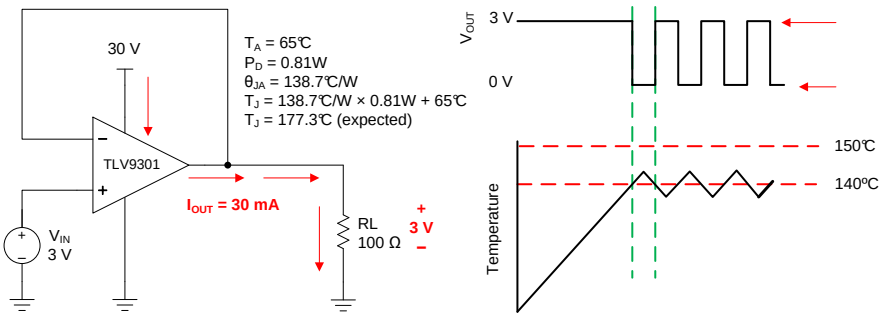


图 45. Thermal Protection

7.3.5 Capacitive Load and Stability

The TLV930x features a resistive output stage capable of driving smaller capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 46 and 图 47. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

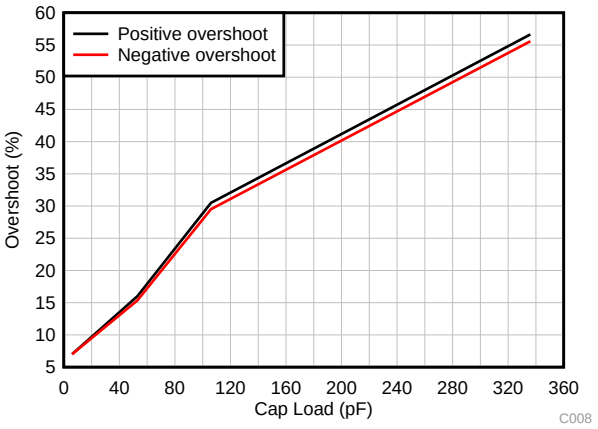


图 46. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = 1)

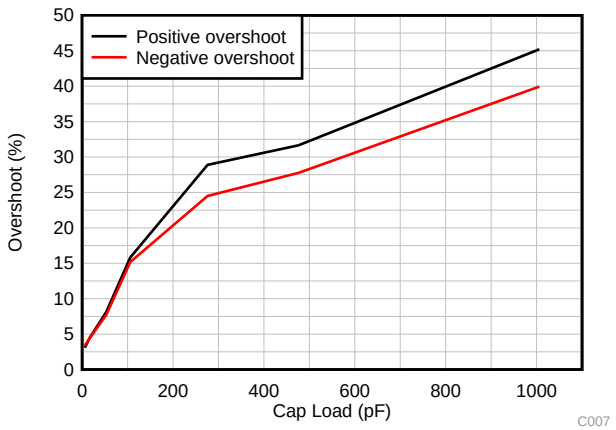


图 47. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in 图 48. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLV930x well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 48 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

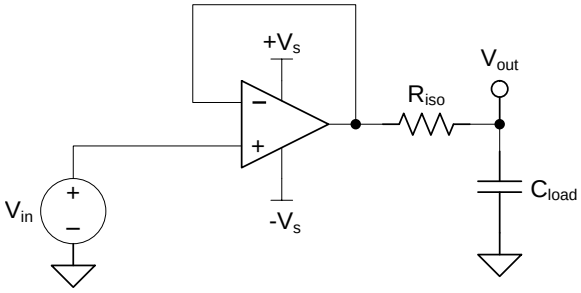


图 48. Extending Capacitive Load Drive With the TLV9301

7.3.6 Common-Mode Voltage Range

The TLV930x is a 40-V, rail-to-rail output operational amplifier with an input common-mode range that extends 100 mV beyond V– and within 2 V of V+ for normal operation. The device accomplishes this performance through a complementary input stage, using a P-channel differential pair. Additionally, a complementary N-channel differential pair has been included in parallel with the P-channel pair to eliminate common undesirable op amp behaviors, such as phase reversal.

The TLV930x can operate with common mode ranges beyond 100 mV of the top rail, but with reduced performance above (V+) – 2 V. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) –2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within the transition region and N-channel region, many specifications of the op amp, including PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation within the P-channel region.

表 3. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		1.5		mV
Offset voltage drift		2		µV/°C
Common-mode rejection		75		dB
Open-loop gain		75		dB
Gain-bandwidth product		0.7		MHz

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 49 shows an illustration of the ESD circuits contained in the TLV930x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

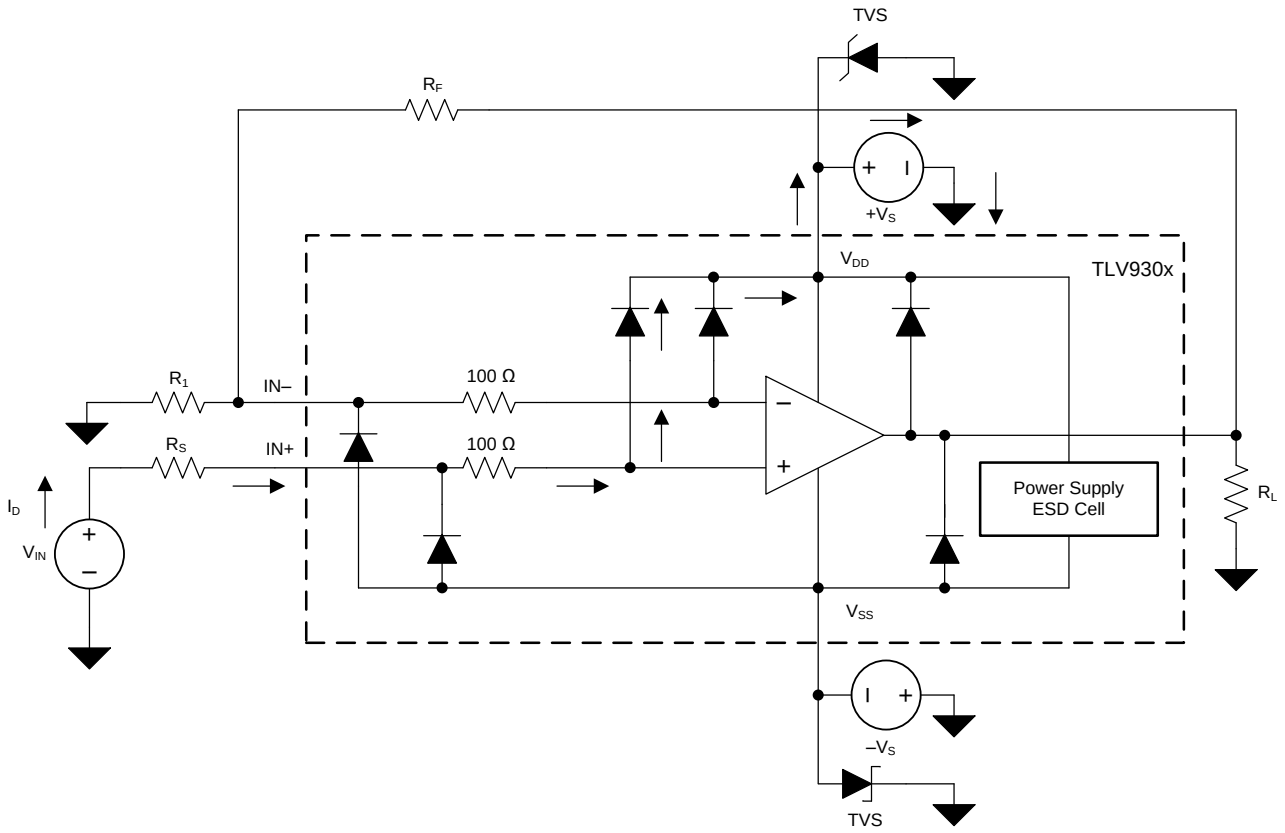


图 49. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV930x is approximately 1 µs.

7.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

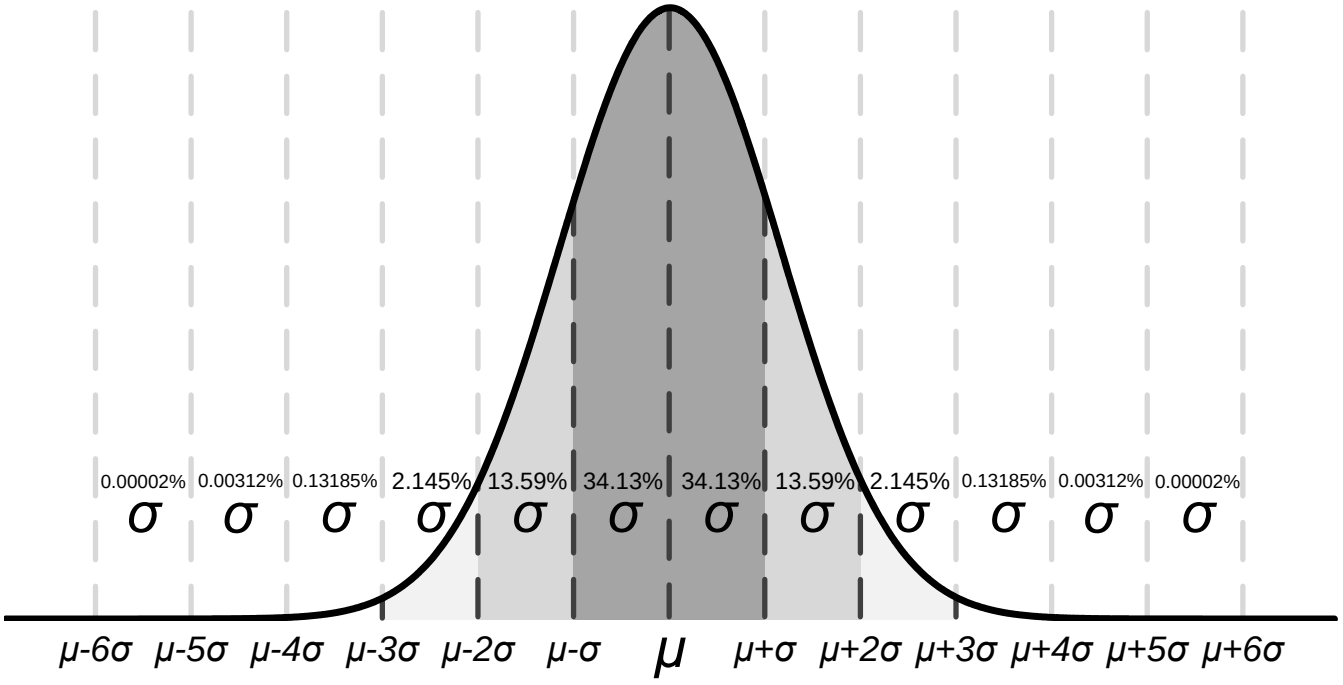


图 50. Ideal Gaussian Distribution

图 50 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from μ–σ to μ+σ).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (µ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (µ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV930x, the typical input voltage offset is 500 µV, so 68.2% of all TLV930x devices are expected to have an offset from –500 µV to +500 µV. At 4 σ (±2000 µV), 99.9937% of the distribution has an offset voltage less than ±2000 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV930x family has a maximum offset voltage of 2.5 mV at 125°C, and even though this corresponds to 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 2.5 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV930x family does not have a maximum or minimum for offset voltage drift, but based on 图 2 and the typical value of 2 µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 12 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

7.4 Device Functional Modes

The TLV930x has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the TLV930x is 40 V (±20 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV930x family offers excellent DC precision and DC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 1-MHz bandwidth and high output drive. These features make the TLV930x a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 High Voltage Precision Comparator

Many different systems require controlled voltages across numerous system nodes to ensure robust operation. A comparator can be used to monitor and control voltages by comparing a reference threshold voltage with an input voltage and providing an output when the input crosses this threshold.

The TLV930x family of op amps make excellent high voltage comparators due to their MUX-friendly input stage (see the *Input Protection Circuitry* section). Previous generation high-voltage op amps often use back-to-back diodes across the inputs to prevent damage to the op amp which greatly limits these op amps to be used as comparators, but the TLV930x's patented input stage allows the device to have a wide differential voltage between the inputs.

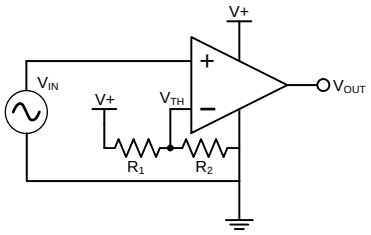


图 51. Typical Comparator Application

8.2.1.1 Design Requirements

The primary objective is to design a 40-V precision comparator.

- System supply voltage (V+): 40 V
- Resistor 1 value: 100 kΩ
- Resistor 2 value: 100 kΩ
- Reference threshold voltage (V_{TH}): 20 V
- Input voltage range (V_{IN}): 0 V – 40 V
- Output voltage range (V_{OUT}): 0 V – 40 V

Typical Applications (接下页)

8.2.1.2 Detailed Design Procedure

This noninverting comparator circuit applies the input voltage (V_{IN}) to the noninverting terminal of the op amp. Two resistors (R_1 and R_2) divide the supply voltage (V+) to create a mid-supply threshold voltage (V_{TH}) as calculated in 公式 1. The circuit is shown in 图 51. When V_{IN} is less then V_{TH}, the output voltage transitions to the negative supply and equals the low-level output voltage. When V_{IN} is greater than V_{TH}, the output voltage transitions to the positive supply and equals the high-level output voltage.

In this example, resistor 1 and 2 have been selected to be 100 kΩ, which sets the reference threshold at 20 V. However, resistor 1 and 2 can be adjusted to modify the threshold using 公式 1. Resistor 1 and 2's values have also been selected to reduce power consumption, but these values can be further increased to reduce power consumption, or reduced to improve noise performance.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ \tag{1}$$

8.2.1.3 Application Curve

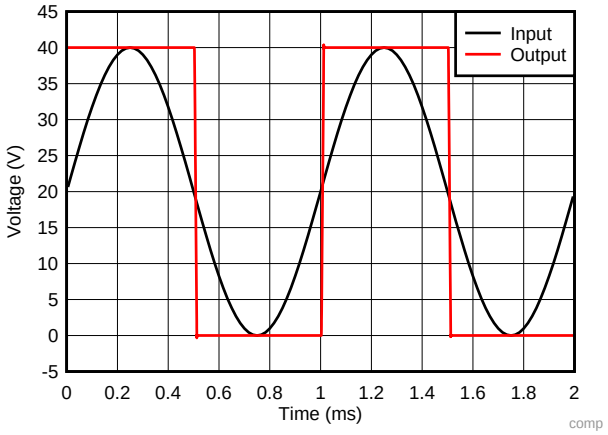


图 52. Comparator Output Response to Input Voltage

9 Power Supply Recommendations

The TLV930x is specified for operation from 4.5 V to 40 V (±2.25 V to ±20 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Electrical Characteristics* table.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 54, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

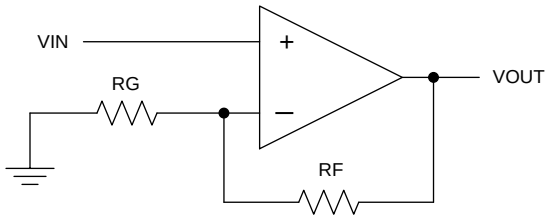


图 53. Schematic Representation

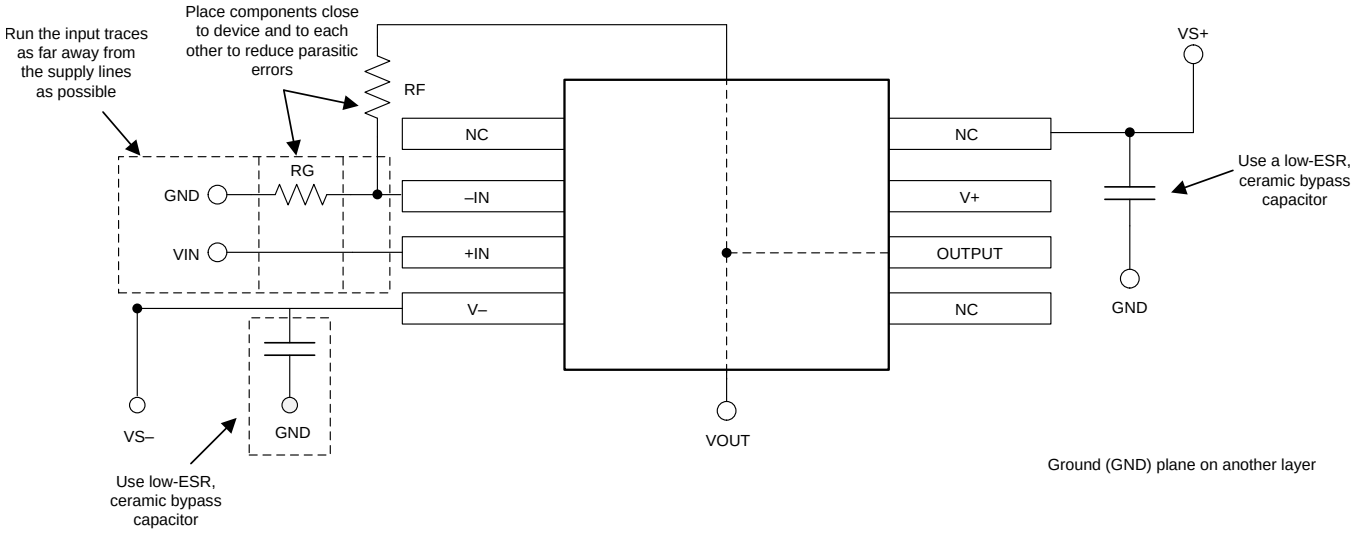


图 54. Operational Amplifier Board Layout for Noninverting Configuration

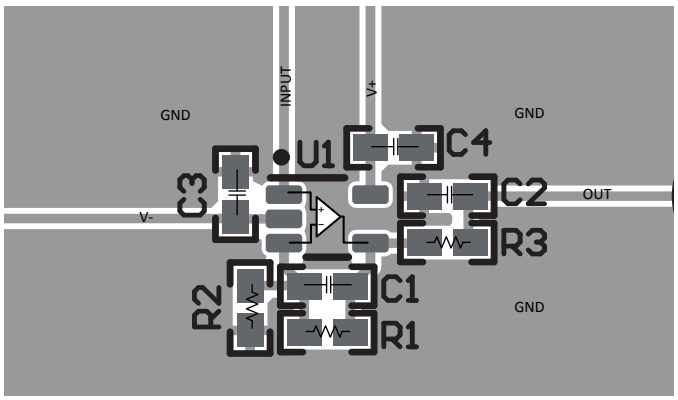


图 55. Example Layout for SC70 (DCK) Package

Layout Example (接下页)

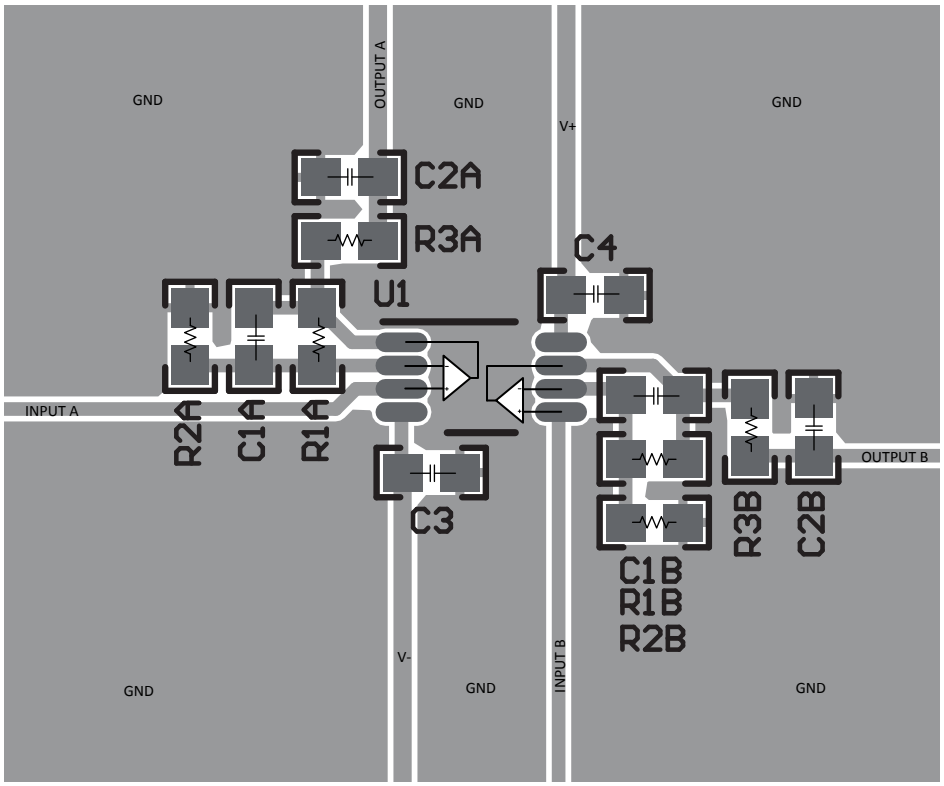


图 56. Example Layout for VSSOP-8 (DGK) Package

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

TLV930x 采用多种 TI 精密设计，有关内容请访问 http://www.ti.com/ww/en/analog/precision-designs/。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.2 文档支持

11.2.1 相关文档

德州仪器 (TI)，*《电路板布局技巧》*

德州仪器 (TI)，*《适合所有人的运算放大器》*

11.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 4. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV9302	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商标

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9301IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T93V	Samples
TLV9301IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1FN	Samples
TLV9302IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T93F	Samples
TLV9302IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9302D	Samples
TLV9302IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9302P	Samples
TLV9304IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9304D	Samples
TLV9304IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	(PTL93PW, T9304PW)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

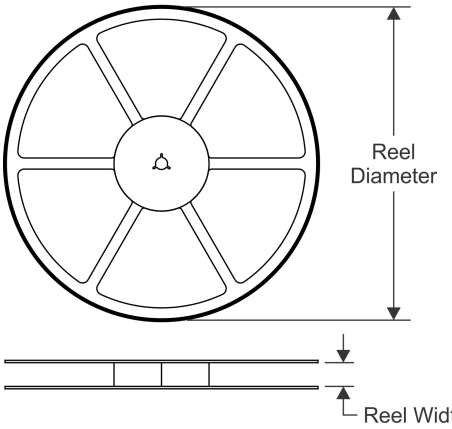
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

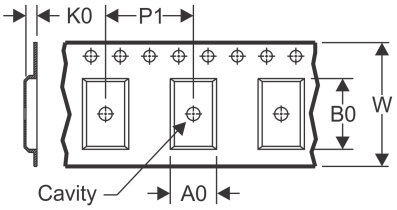
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

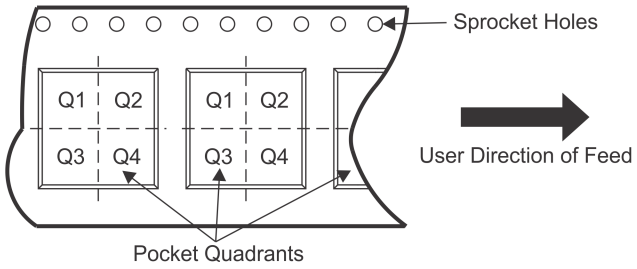


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

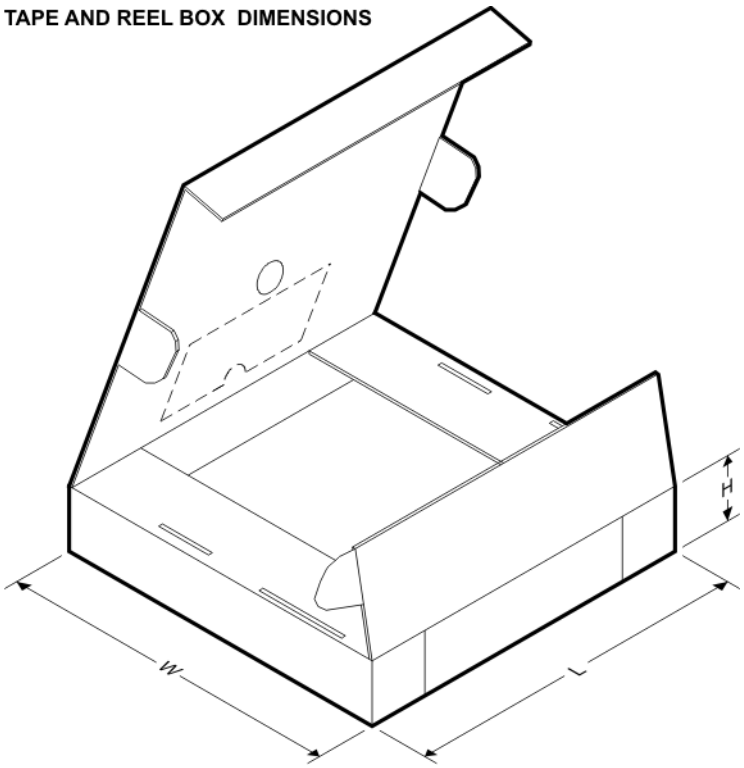
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9301IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9301IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9302IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9302IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9302IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9304IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9304IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

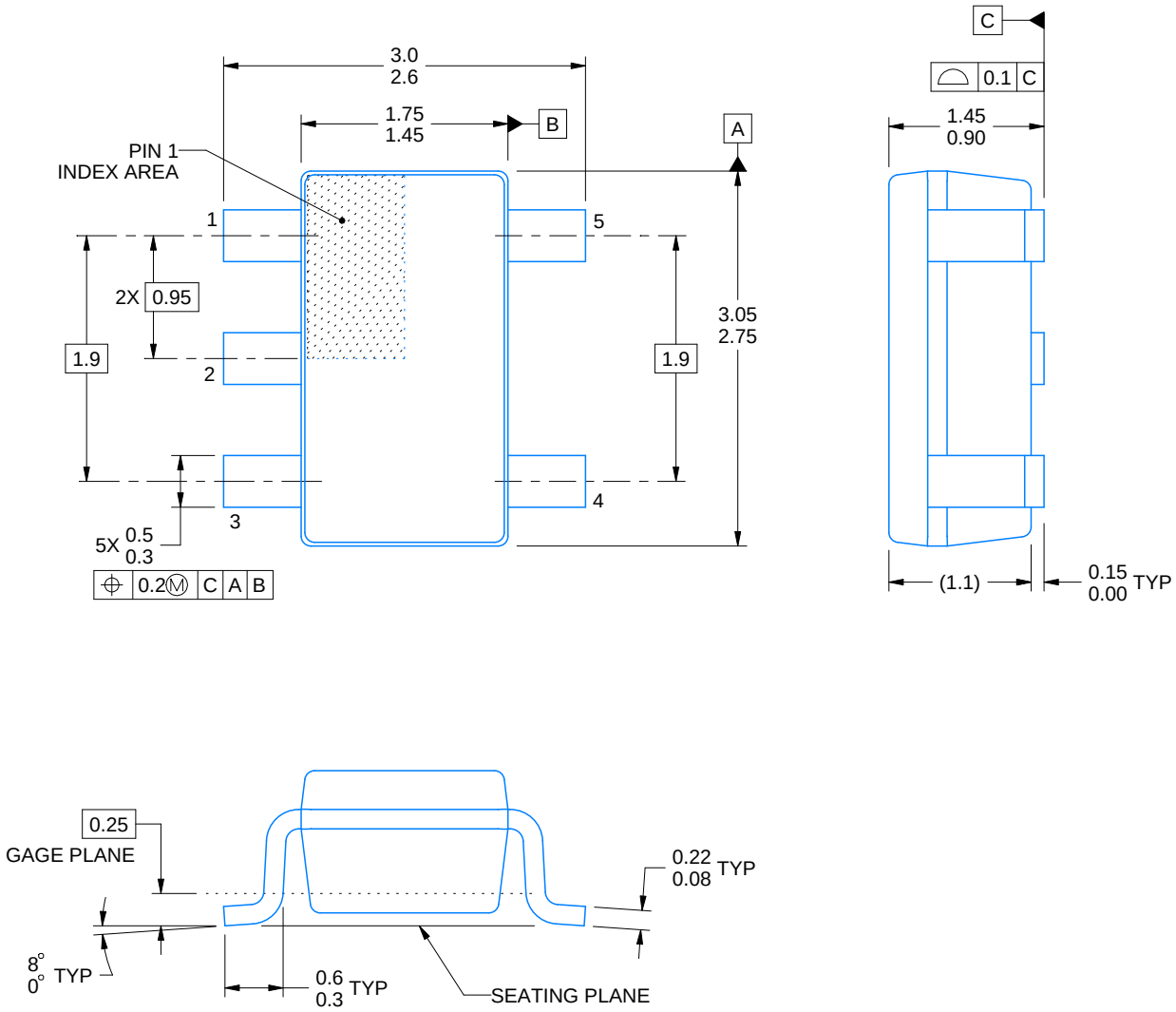
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9301IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9301IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9302IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9302IDR	SOIC	D	8	2500	853.0	449.0	35.0
TLV9302IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV9304IDR	SOIC	D	14	2500	853.0	449.0	35.0
TLV9304IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

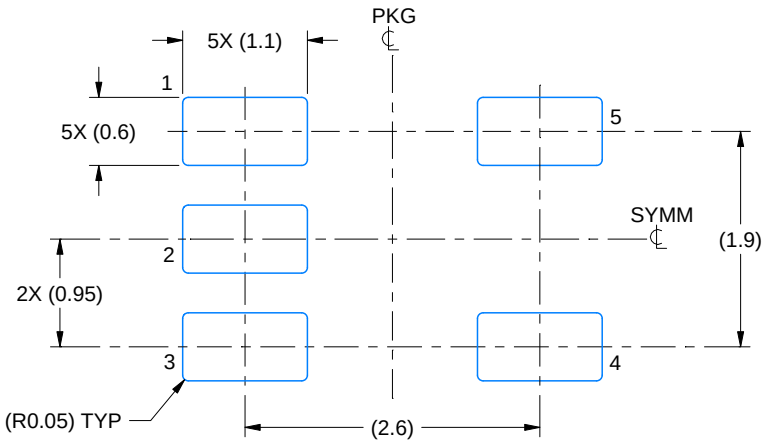
SMALL OUTLINE TRANSISTOR



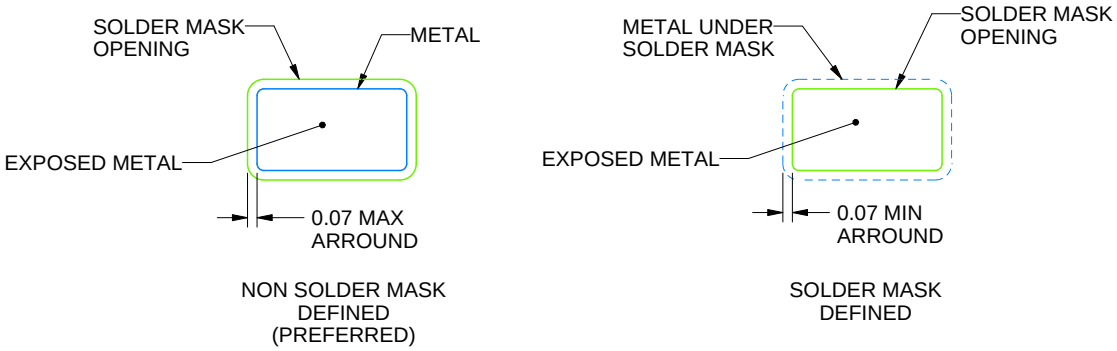
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

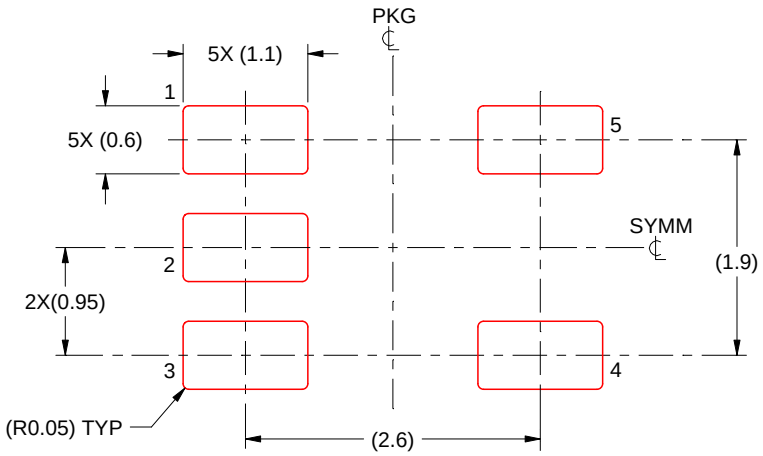


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



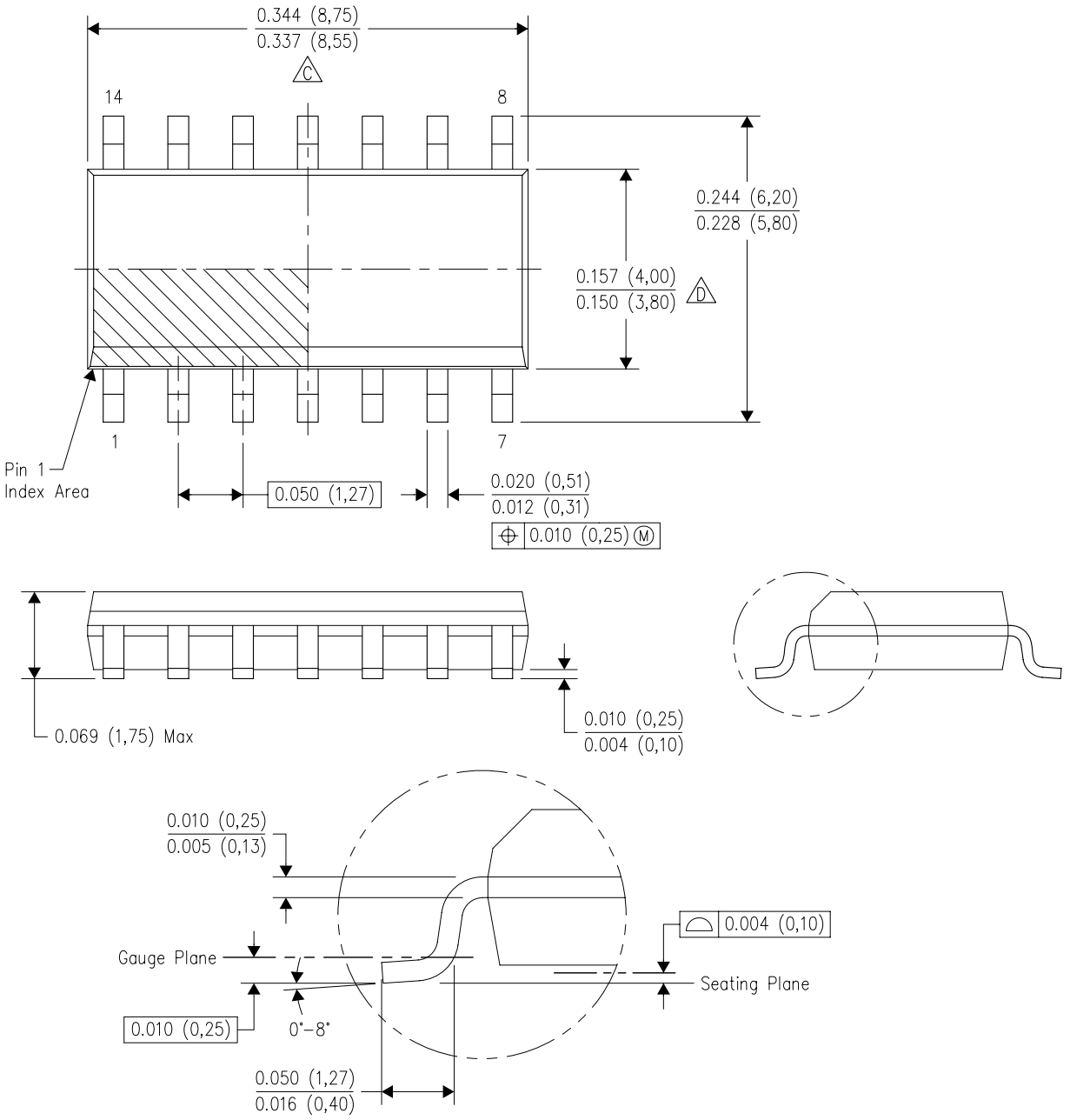
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

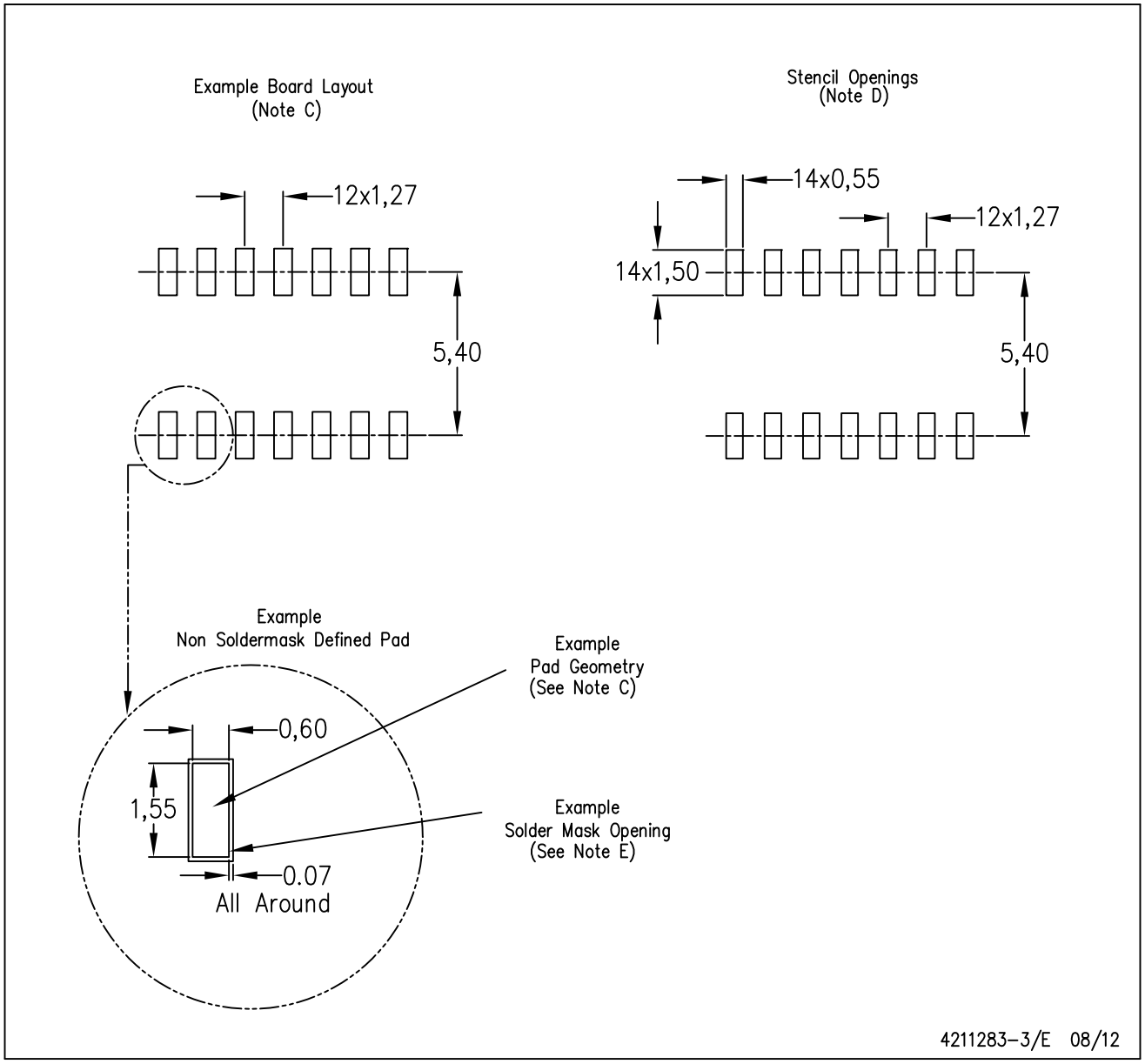
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

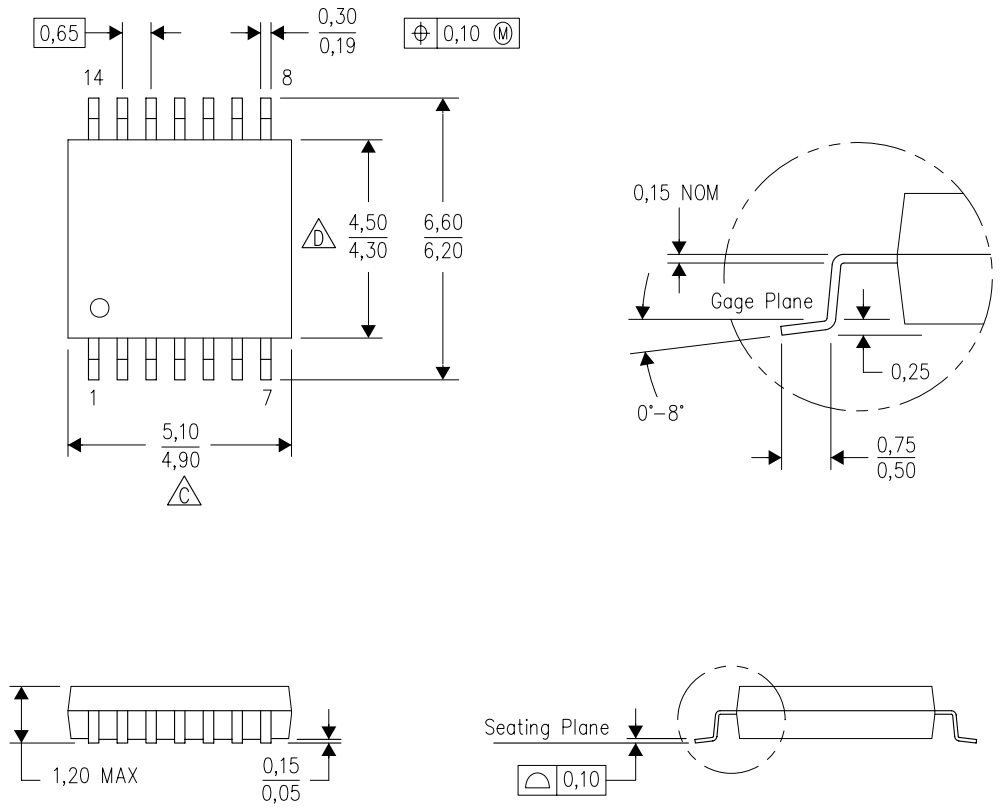
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

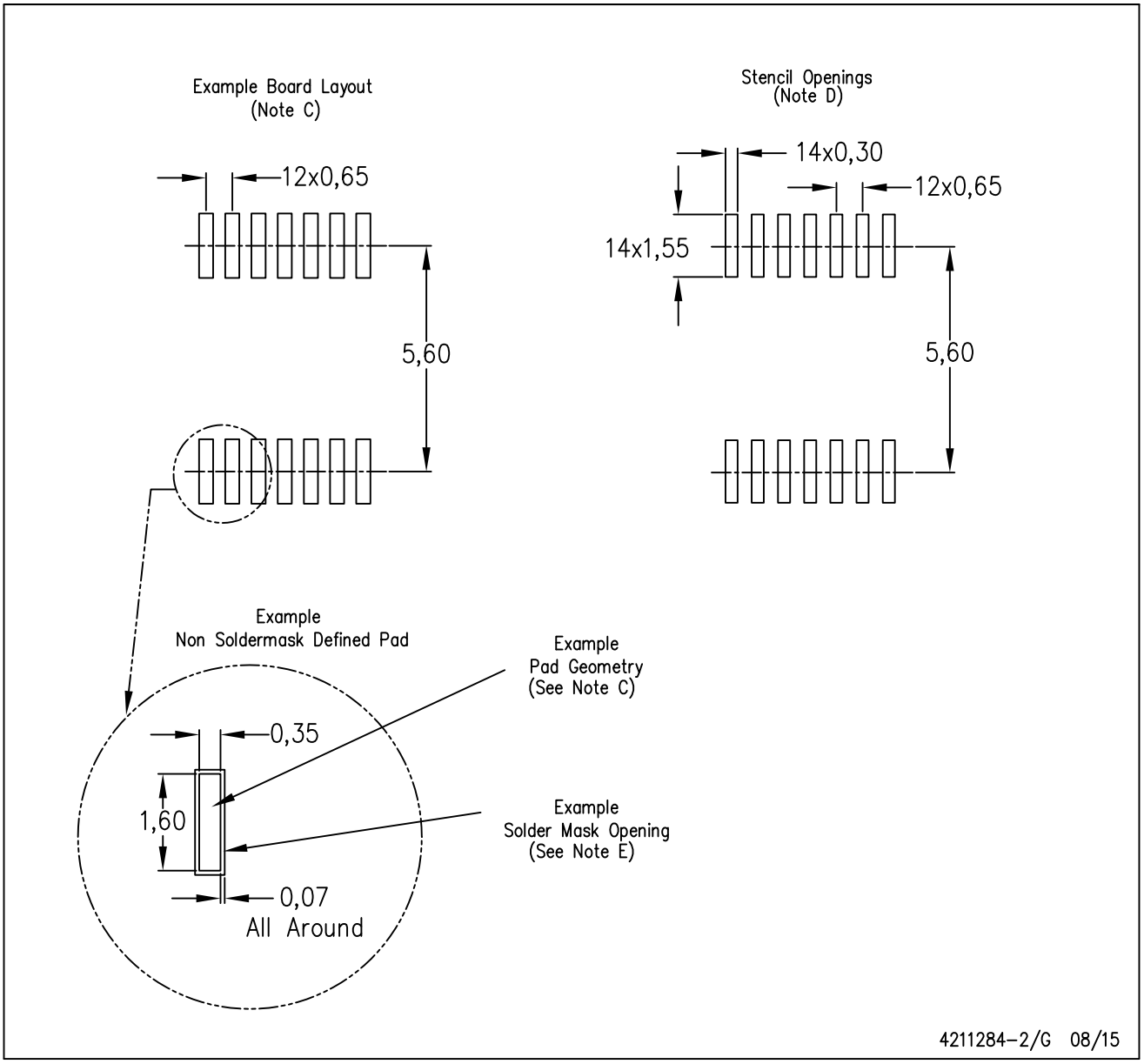
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



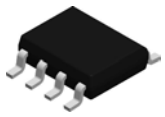
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

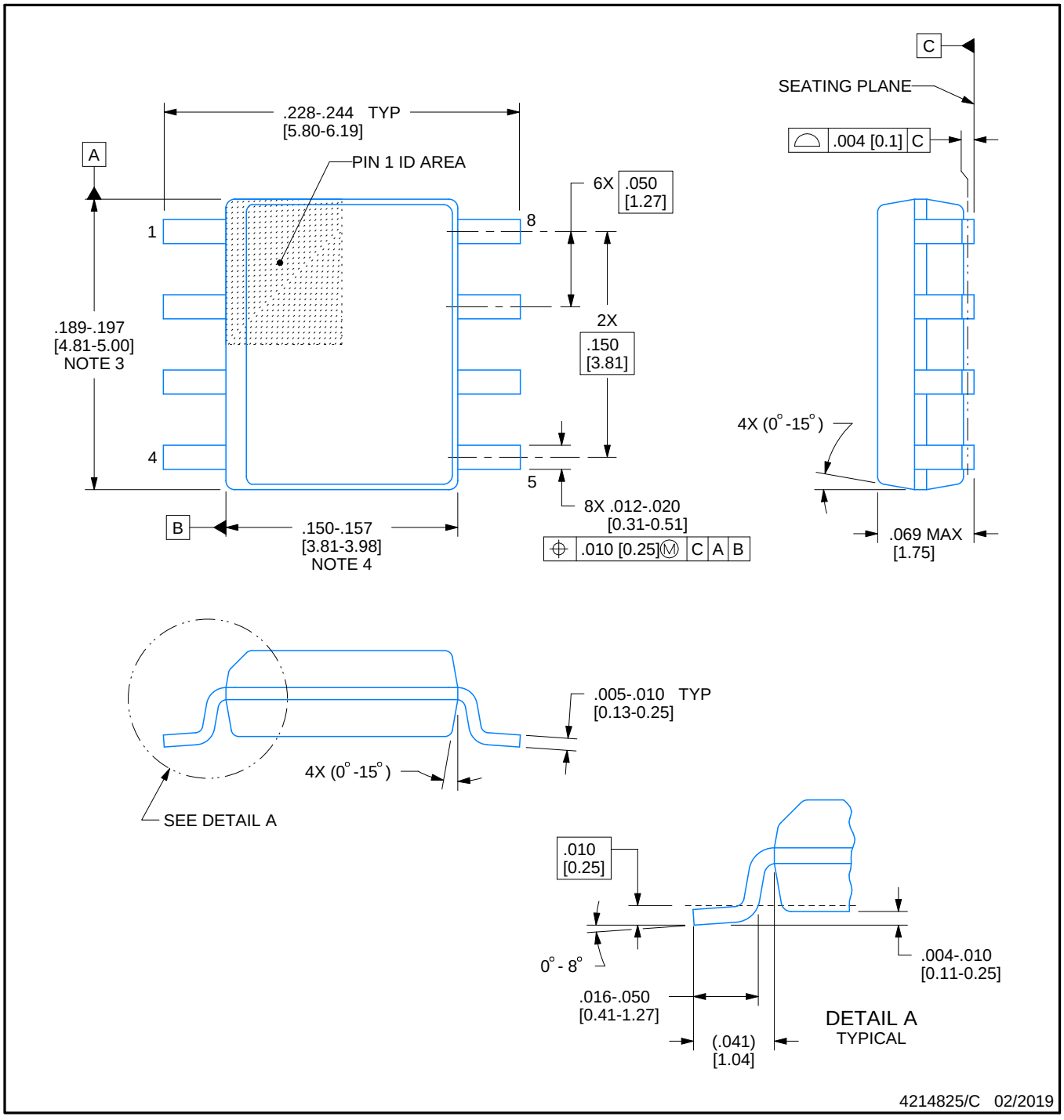


PACKAGE OUTLINE

D0008A

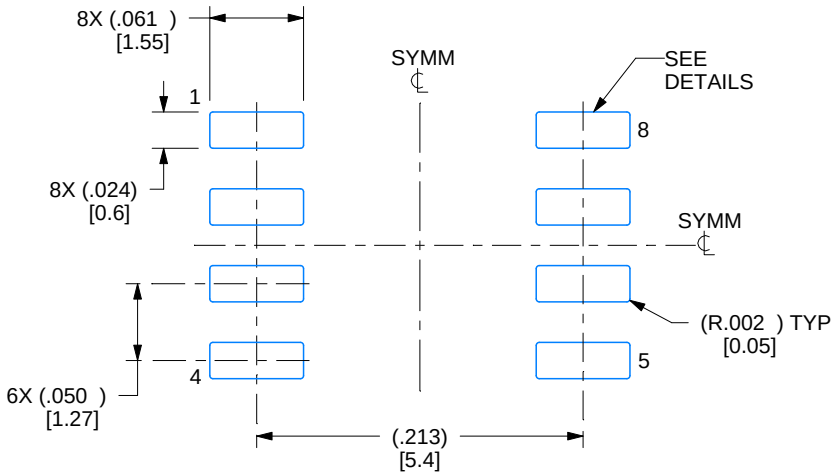
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

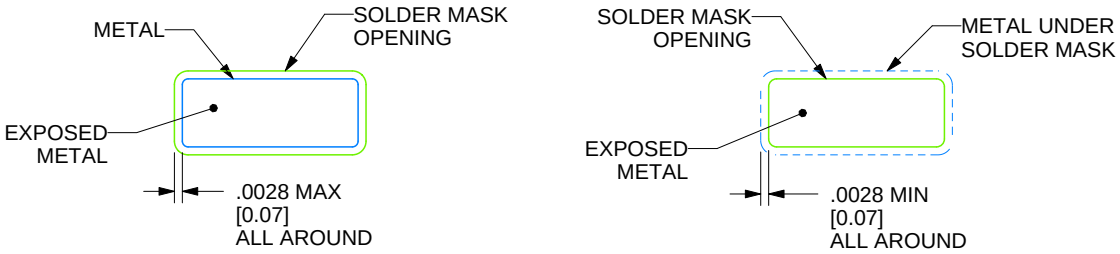


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

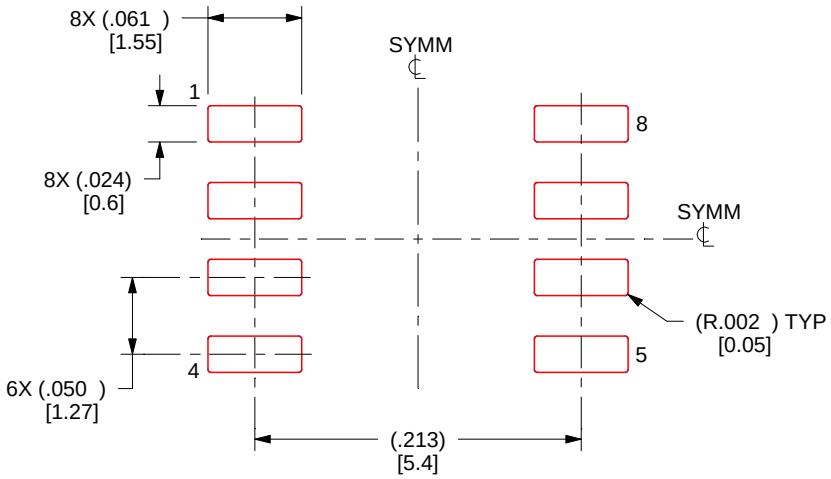
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

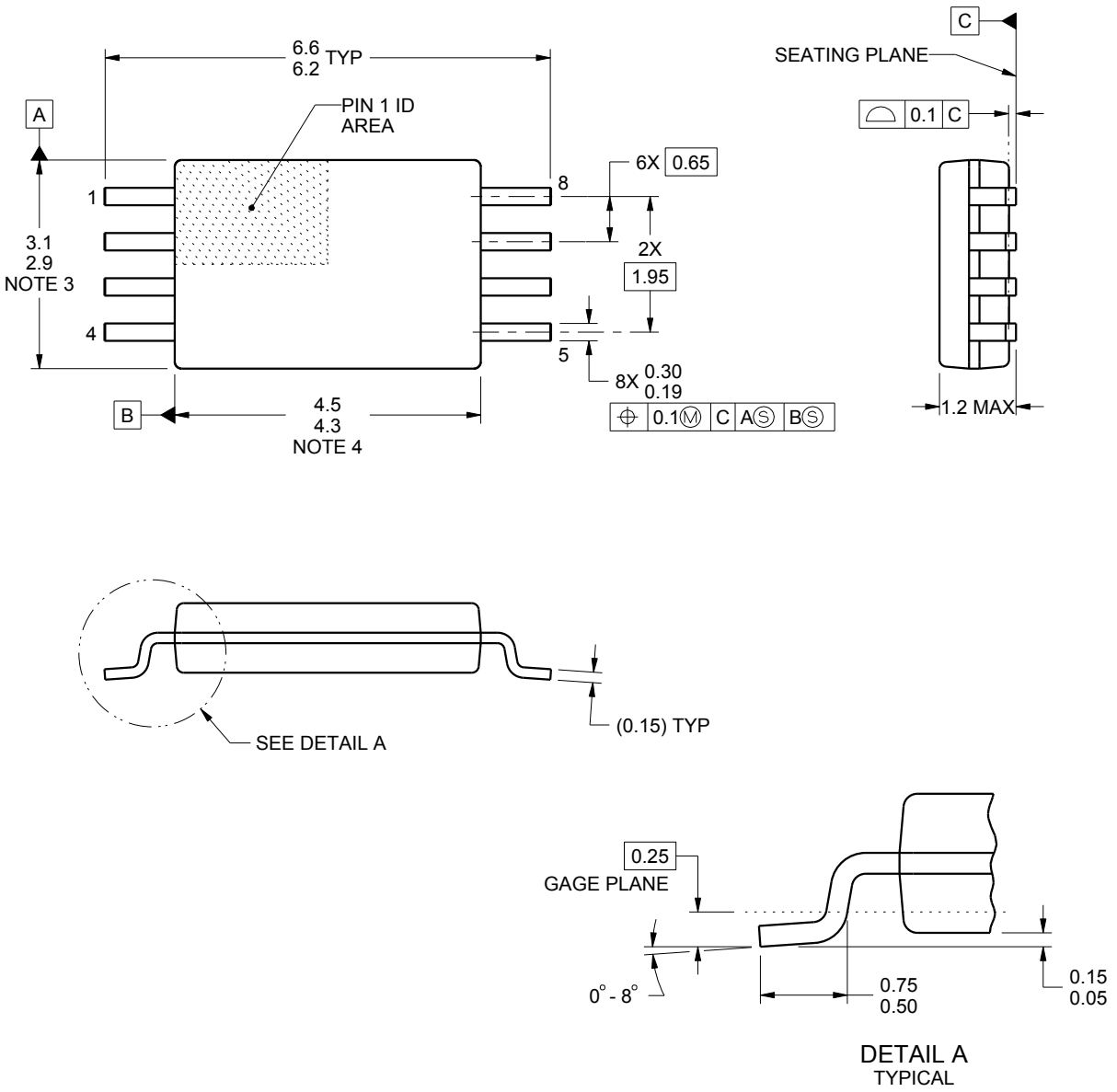
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

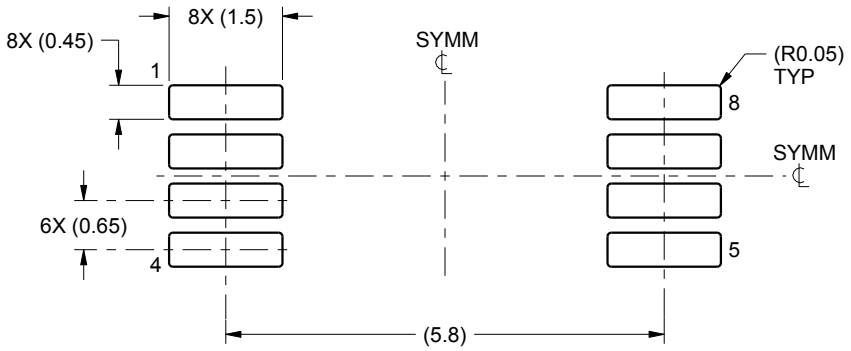
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

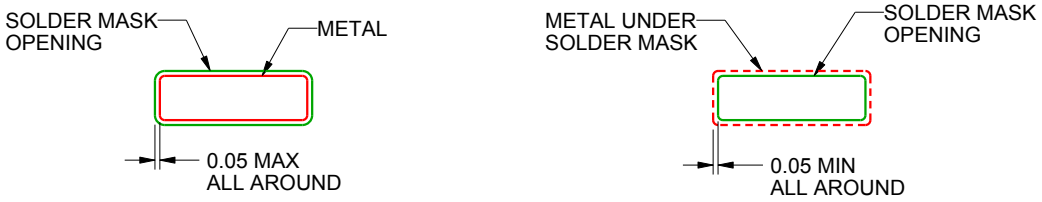


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

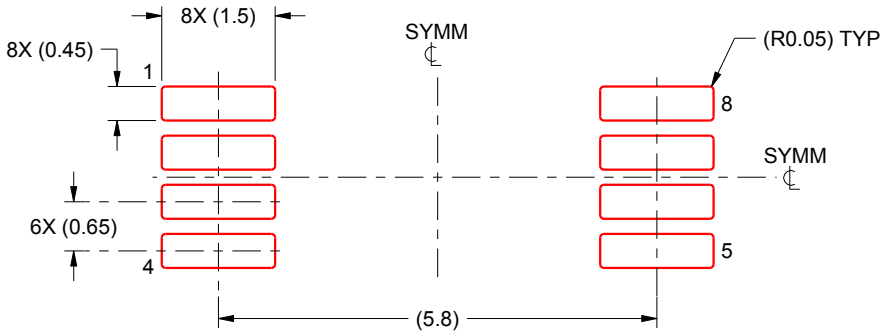


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



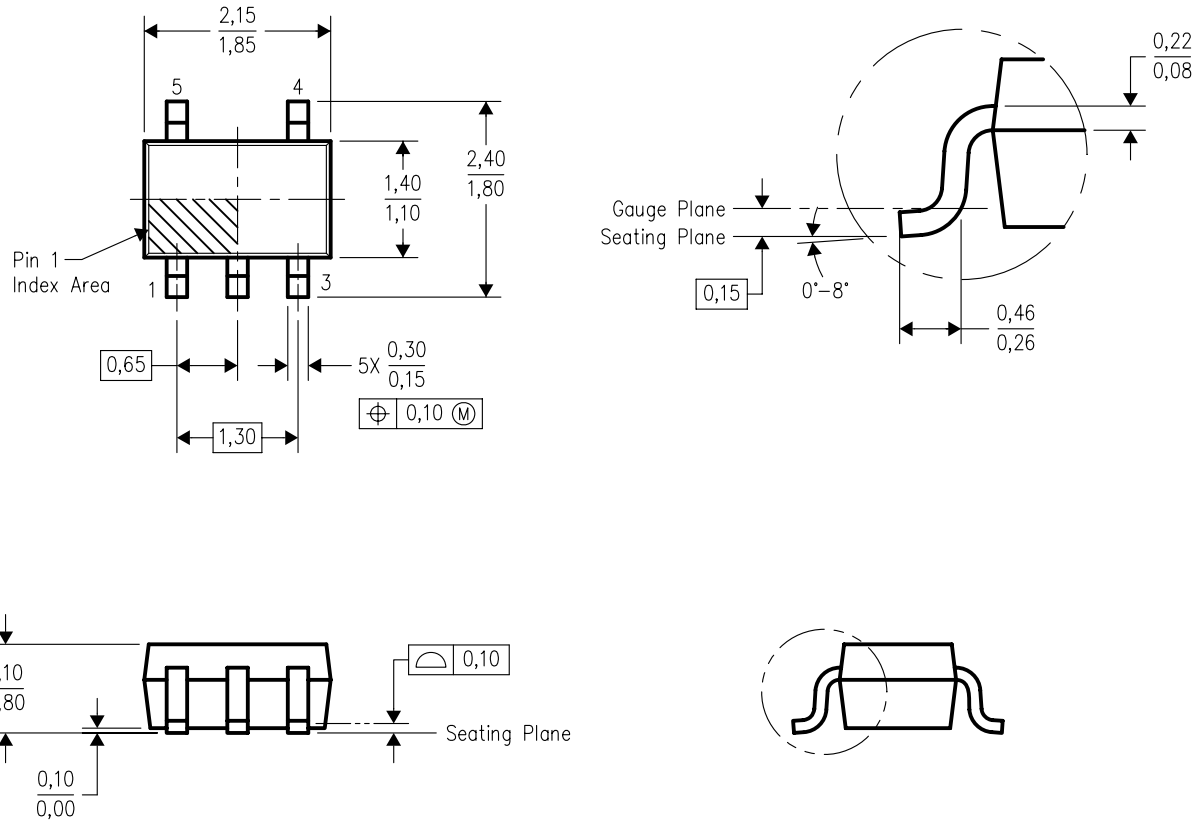
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

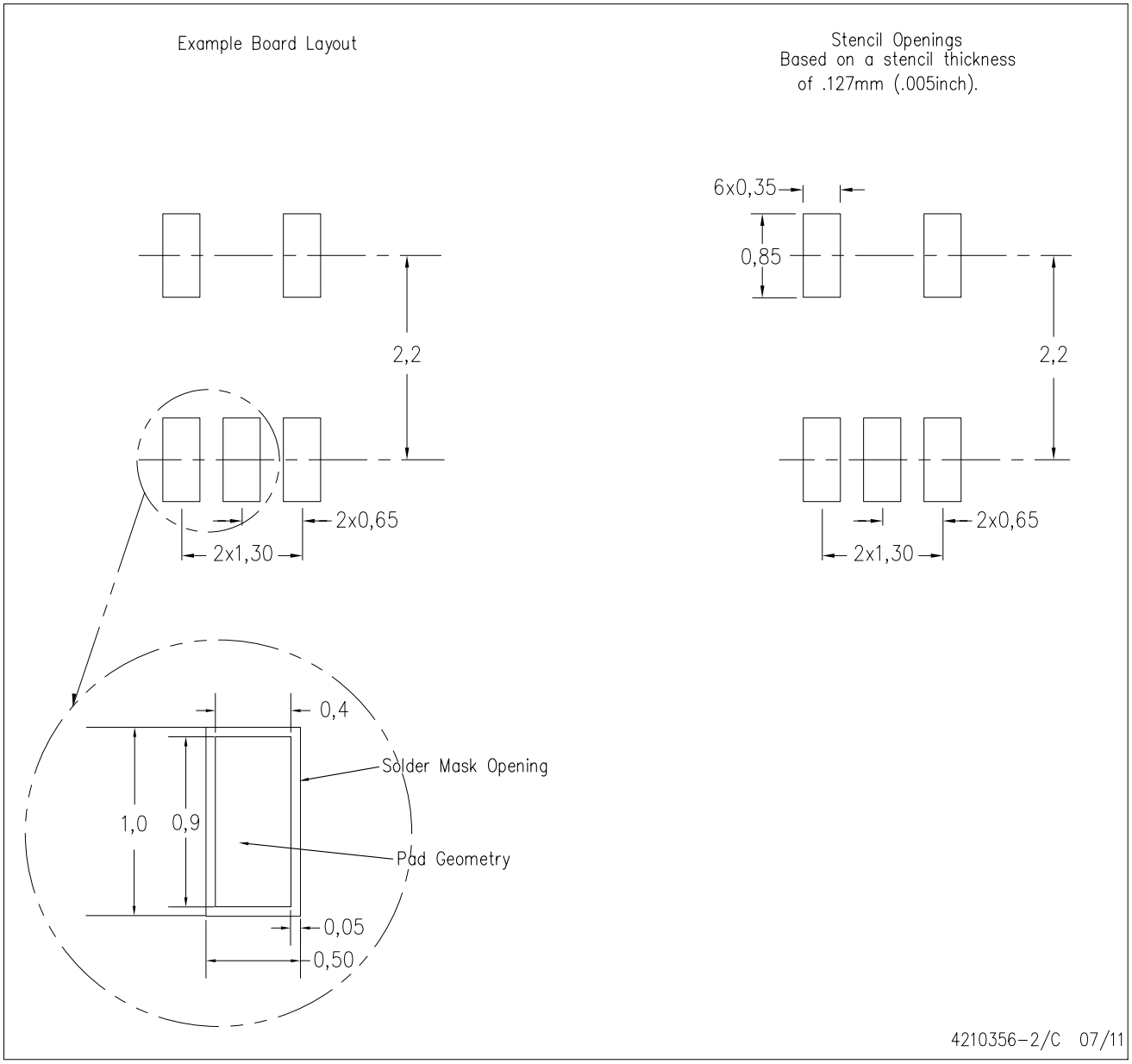
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



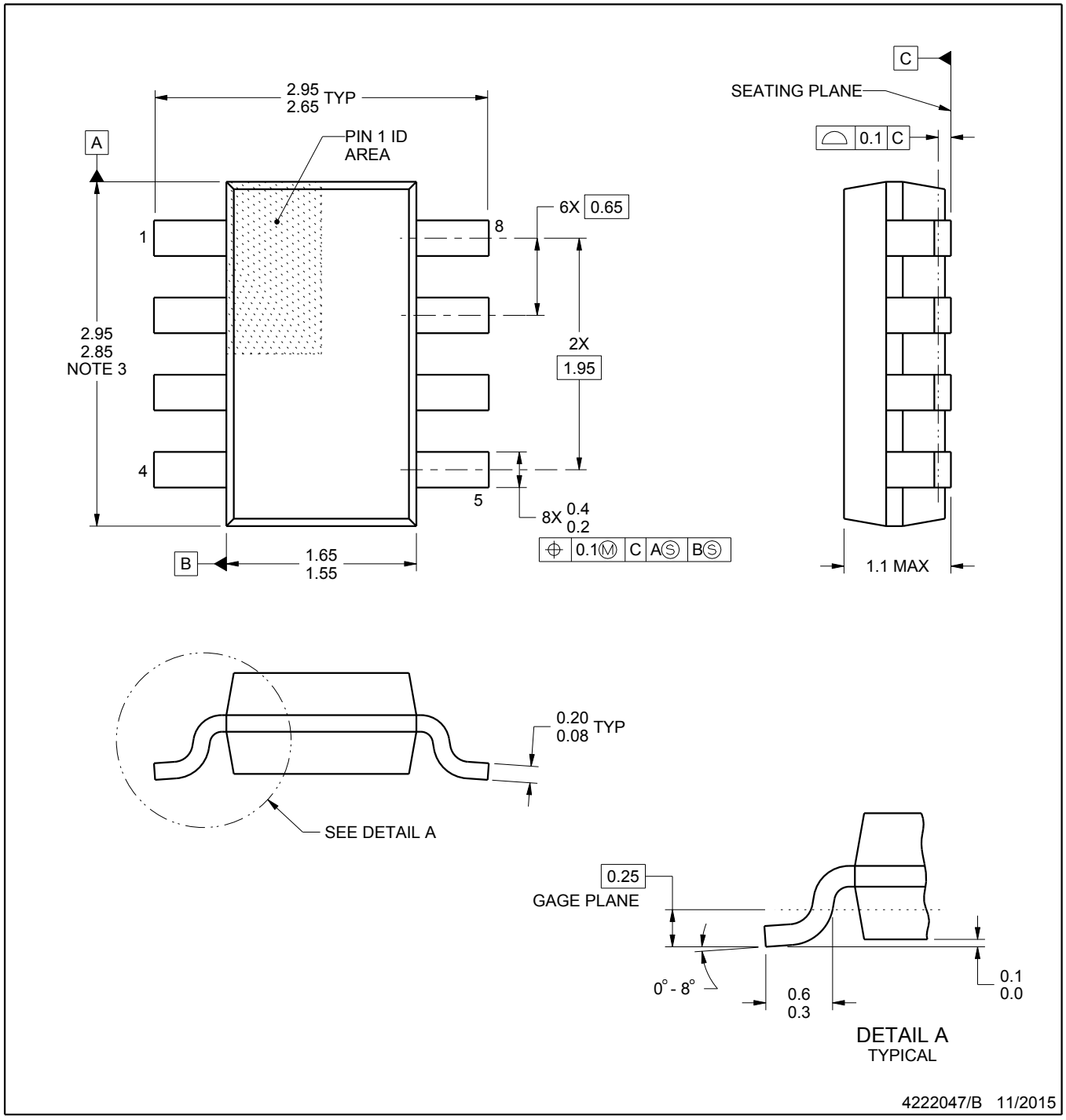
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DDF0008A

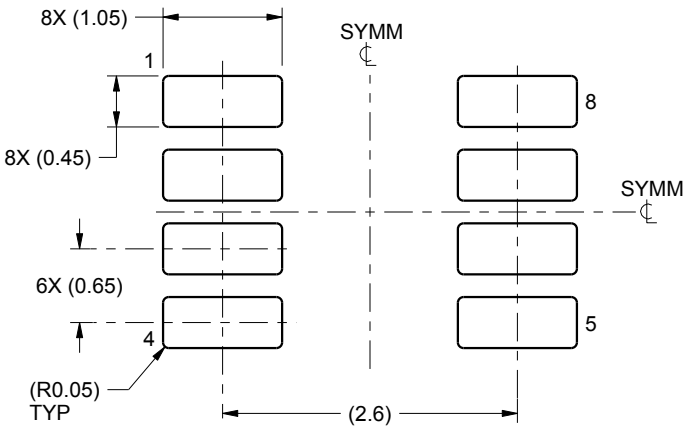
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

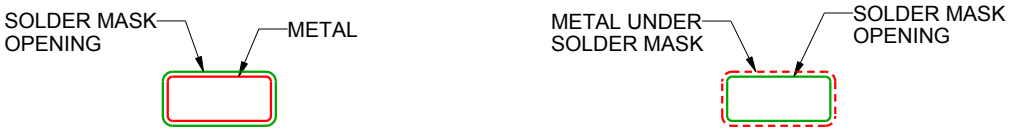


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

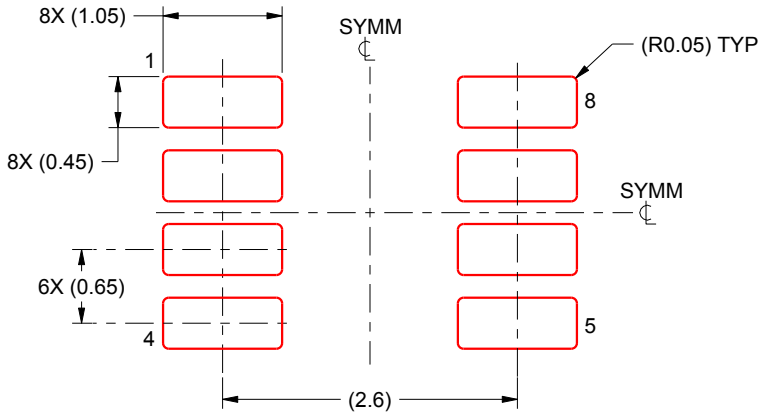
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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