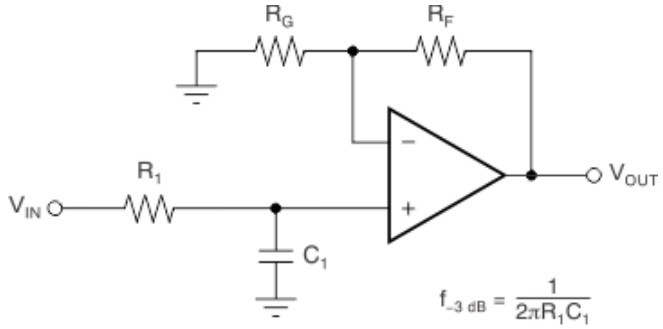
TLV906xS-Q1 汽车类 10MHz、RRIO、CMOS 运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C6
- 轨到轨输入和输出
- 低输入失调电压：±0.3mV
- 单位带宽增益积：10MHz
- 低宽带噪声：10nV/ $\sqrt{Hz}$
- 低输入偏置电流：0.5pA
- 低静态电流：538μA
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 宽电源电压范围：1.8V 至 5.5V
- 由于具有电阻式开环输出阻抗，因此可在更高的容性负载下更轻松地实现稳定
- 关断版本：TLV906xS
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档

2 应用

- 针对 AEC-Q100 1 级应用进行了优化
- 信息娱乐系统与仪表组
- 被动安全
- 车身电子装置和照明
- HEV/EV 逆变器和电机控制
- 车载 (OBC) 和无线充电器
- 动力系统电流传感器
- 高级驾驶辅助系统 (ADAS)
- 单电源、低侧、单向电流感应电路



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器

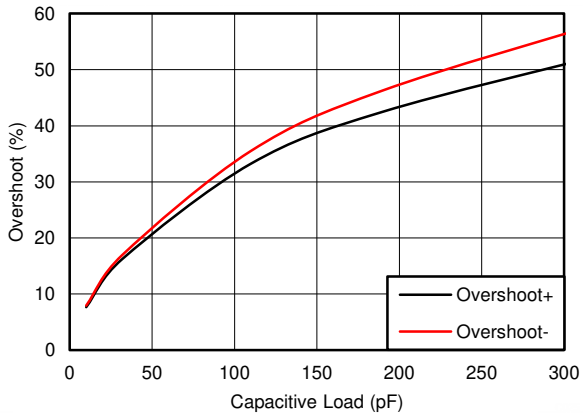
3 说明

TLV9061（单通道）、TLV9062-Q1（双通道）和 TLV9064-Q1（四通道）是单路、双路和四路低压（1.8V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅能力。此类器件是具有成本效益的解决方案，适用于需要低电压运行、小型封装尺寸和高容性负载驱动能力的汽车应用。虽然 TLV906x-Q1 的容性负载驱动能力为 100pF，但电阻式开环输出阻抗便于在更高的容性负载下更轻松地实现稳定。此类运算放大器专为低工作电压（1.8V 至 5.5V）而设计，性能规格类似于 OPAx316 和 TLVx316 器件，并与它们的非汽车级 TLV906x 对应产品相同。

器件信息

器件型号 (1)	封装	封装尺寸（标称值）
TLV9061S-Q1	SOT-23 (6)	1.60mm × 2.90mm
TLV9062-Q1	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)(2)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
TLV9064-Q1	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装仅为预览版。



小信号过冲与负载电容间的关系

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (October 2020) to Revision E (February 2021) — **Page**

- 删除了器件信息 部分中 SOT-23 (6) 封装的预览说明。.....1
- Added separate ESD rating for TLV9061S-Q1 in *ESD Ratings* table.....6
- Updated DBV (SOT-23) thermal information in *Thermal Information: TLV9061S-Q1* table.....6

Changes from Revision C (September 2020) to Revision D (October 2020) — **Page**

- 在整个数据表中添加了 TLV9061-Q1 GPN.....1

Changes from Revision B (September 2020) to Revision C (September 2020) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式.....1
- 向特性 部分添加了“提供功能安全”链接。.....1
- Added note 5 to differential input voltage in *Absolute Maximum Ratings* table.....6

Changes from Revision A (March 2020) to Revision B (September 2020) — **Page**

- 删除了器件信息 部分中 VSSOP (8) 和 TSSOP (14) 封装的预览说明。.....1
- Added thermal information for VSSOP (8) package in *Thermal Information* section.....7
- Added thermal information for TSSOP (14) package in *Thermal Information* section.....7

Changes from Revision * (April 2019) to Revision A (March 2020) — **Page**

- 首次公开发布数据表.....1

5 Description (continued)

The TLV906x-Q1 family of devices serve as general-purpose automotive amplifiers, for use in low-voltage systems requiring low noise and/or wide bandwidth.

The TLV906x-Q1 family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

These devices are available in both dual (TLV9062-Q1), and quad (TLV9064-Q1) versions. Both versions are available in industry standard SOIC and TSSOP packages, with the dual channel also available as a VSSOP.

6 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS		
		D	DGK	PW
TLV9061S-Q1	1	—	—	—
TLV9062-Q1	2	8	8	8
TLV9064-Q1	4	14	—	14

7 Pin Configuration and Functions

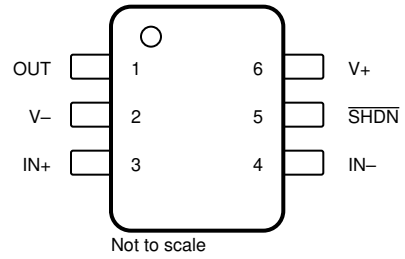


图 7-1. TLV9061S-Q1 DBV Package
6-Pin SOT-23
Top View

表 7-1. Pin Functions: TLV9061S-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN –	4	I	Inverting input
IN+	3	I	Noninverting input
OUT	1	O	Output
$\overline{\text{SHDN}}$	5	I	Shutdown: low = amp disabled, high = amp enabled. See *Shutdown Function* section for more information.
V –	2	I or —	Negative (lowest) supply or ground (for single-supply operation)
V+	6	I	Positive (highest) supply

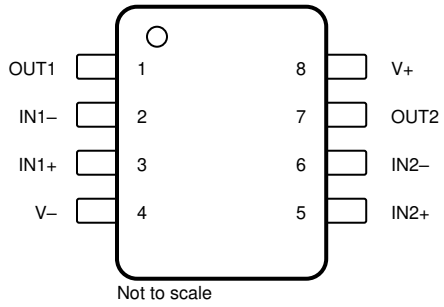


图 7-2. TLV9062-Q1 D, DGK, and PW Package
8-Pin SOIC, VSSOP, and TSSOP
Top View

表 7-2. Pin Functions: TLV9062-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V –	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

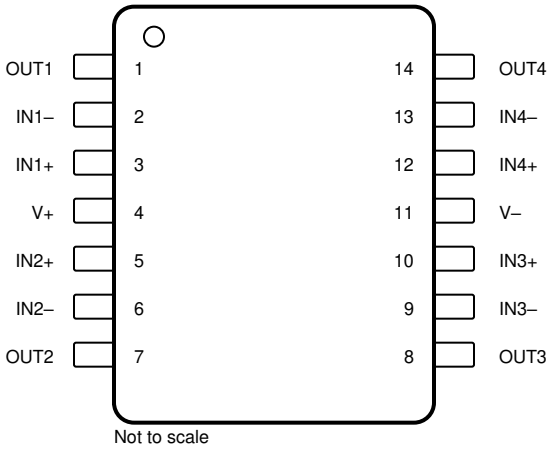


图 7-3. TLV9064-Q1 D and PW Package
14-Pin SOIC and TSSOP
Top View

表 7-3. Pin Functions: TLV9064-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3 –	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4 –	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V –	11	I or —	Negative (lowest) supply or ground (for single-supply operation)
V+	4	I	Positive (highest) supply

8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage [(V+) – (V–)]			0	6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(5)		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3) (4)			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Long term continuous current limit is determined by electromigration limits.
(5) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

8.2 ESD Ratings

			VALUE	UNIT
TLV9061S-Q1 PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
ALL OTHER PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V_S = [V+] – [V–])	1.8	5.5	V
V_I	Input voltage	(V–) – 0.1	(V+) + 0.1	V
V_O	Output voltage	V–	V+	V
V_{SHDN_IH}	High level input voltage at shutdown pin (amplifier enabled)	1.1	V+	V
V_{SHDN_IL}	Low level input voltage at shutdown pin (amplifier disabled)	V–	0.2	V
T_A	Specified temperature	–40	125	°C

8.4 Thermal Information: TLV9061S-Q1

THERMAL METRIC(1)		TLV9061S-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130.5	°C/W

8.4 Thermal Information: TLV9061S-Q1 (continued)

THERMAL METRIC(1)		TLV9061S-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Thermal Information: TLV9062-Q1

THERMAL METRIC(1)		TLV9062-Q1 D (SOIC) 8 PINS	TLV9062-Q1 DGK (VSSOP) 8 PINS	TLV9062-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.0	198.5	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.1	87.2	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.6	120.3	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.1	23.8	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	94.8	118.7	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.6 Thermal Information: TLV9064-Q1

THERMAL METRIC(1)		TLV9064-Q1 PW (TSSOP) 14 PINS	TLV9064-Q1 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.1	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.9	67	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.2	27.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.3	66.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.7 Electrical Characteristics

For V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±1.85	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±0.53		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±7	±80	µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C	57	75		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		88		
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V T_A = –40°C to 125°C		70		
INPUT BIAS CURRENT						
I_B	Input bias current			±5		pA
I_{OS}	Input offset current			±5		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		10		nV/√Hz
		V_S = 5 V, f = 1 kHz		16		
i_n	Input current noise density	f = 1 kHz		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	130		
		V_S = 1.8 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2 kΩ		100		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = +1		10		MHz
Φ_m	Phase margin	V_S = 5 V, G = +1		55		°
SR	Slew rate	V_S = 5 V, G = +1		6.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		0.5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.2		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz		0.0008%		
OUTPUT						

8.7 Electrical Characteristics (continued)

For V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			20	mV
		V_S = 5.5 V, R_L = 2 kΩ			60	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		538	750	µA
		V_S = 5.5 V, I_O = 0 mA T_A = –40°C to 125°C			800	
SHUTDOWN (2)						
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = Low		0.5	1.5	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled		10 || 8		GΩ || pF
$V_{SHDN\_THR\_HI}$	High level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 V to 5.5 V		(V–) + 0.9	(V–) + 1.1	V
$V_{SDHN\_THR\_LO}$	Low level voltage shutdown threshold (amplifier disabled)	V_S = 1.8 V to 5.5 V	(V–) + 0.2	(V–) + 0.7		V
t_{ON}	Amplifier enable time (shutdown)(3)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–		10		µs
t_{OFF}	Amplifier disable time(3)	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2, R_L connected to V–		0.6		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8 V		130		pA
		V_S = 1.8 V to 5.5 V, V– ≤ $\overline{SHDN}$ ≤ V– + 0.8 V		40		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.
(2) Ensured by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

8.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

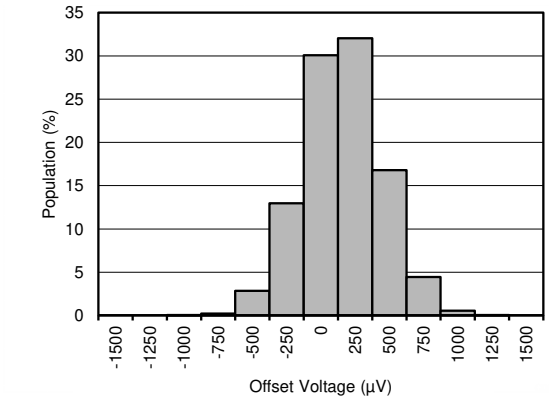
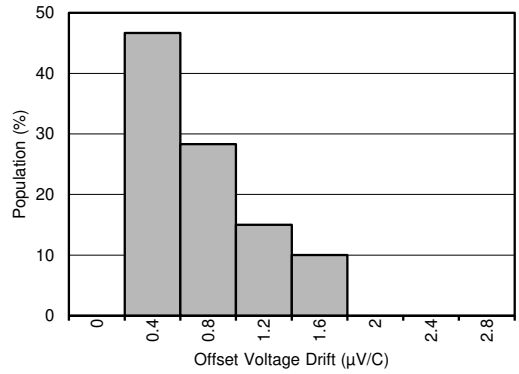


图 8-1. Offset Voltage Production Distribution



T_A = –40°C to 125°C

图 8-2. Offset Voltage Drift Distribution

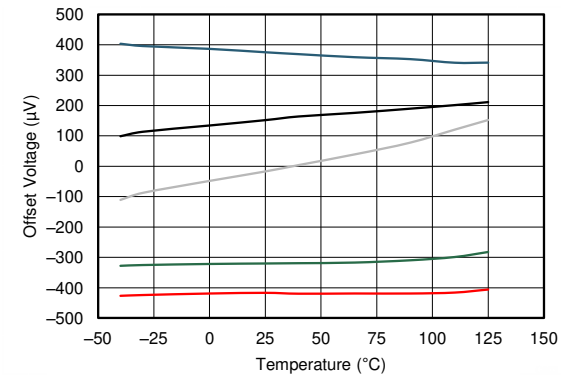
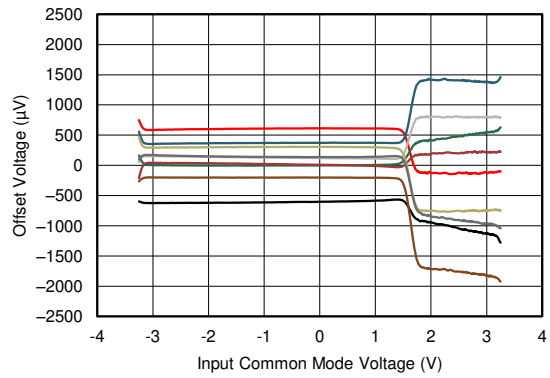
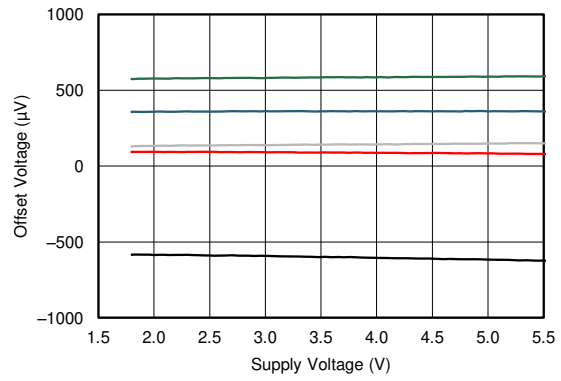


图 8-3. Offset Voltage vs Temperature



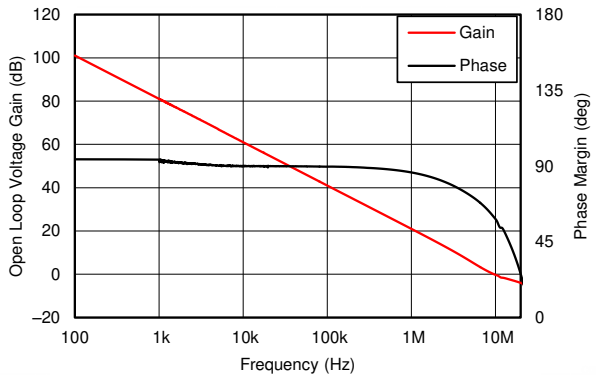
V+ = 2.75 V V– = –2.75 V

图 8-4. Offset Voltage vs Common-Mode Voltage



V_S = 1.8 V to 5.5 V

图 8-5. Offset Voltage vs Power Supply

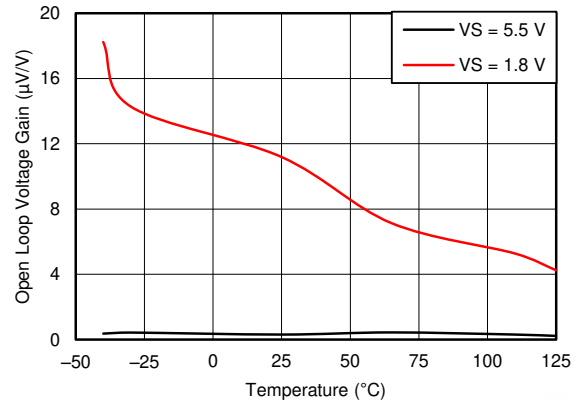


C_L = 10 pF

图 8-6. Open-Loop Gain and Phase vs Frequency

8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



R_L = 2 kΩ

图 8-7. Open-Loop Gain vs Temperature

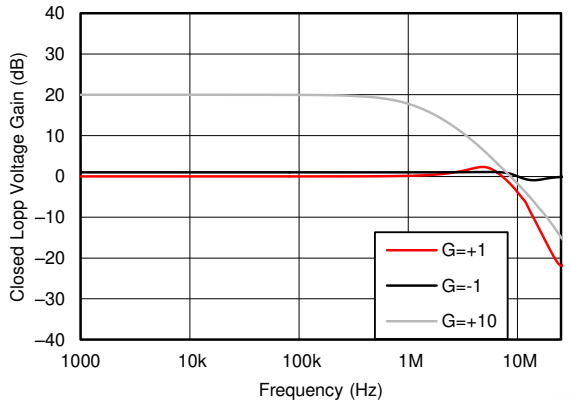


图 8-8. Closed-Loop Gain vs Frequency

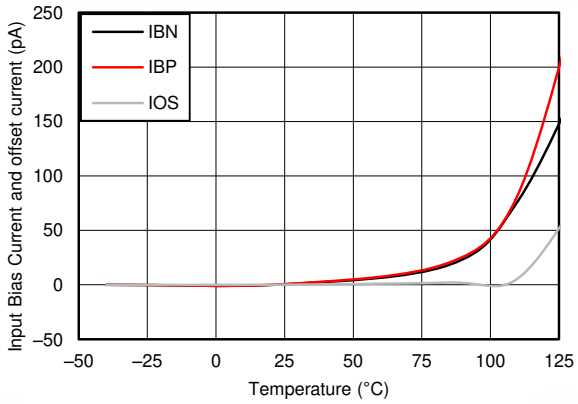
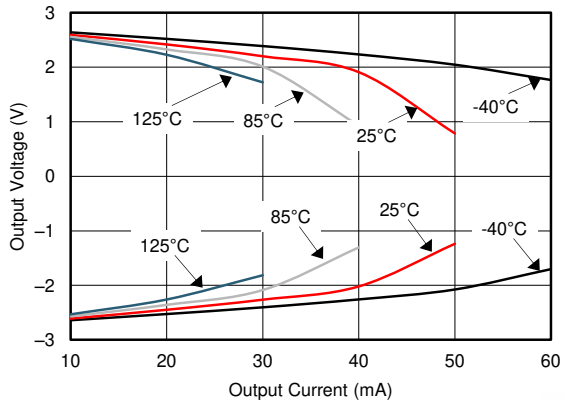


图 8-9. Input Bias Current vs Temperature



V+ = 2.75 V V– = –2.75 V

图 8-10. Output Voltage Swing vs Output Current

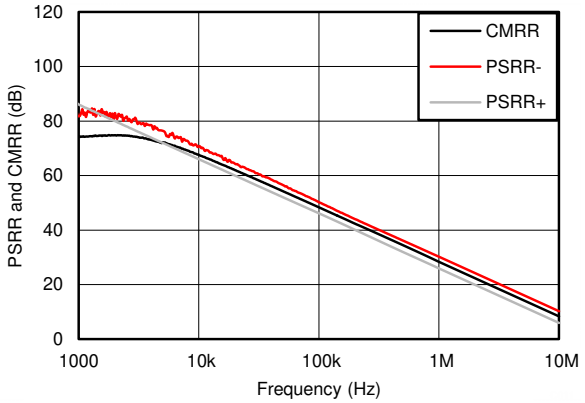
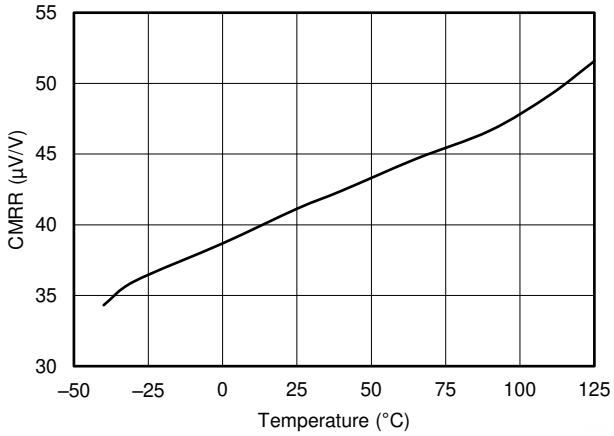


图 8-11. CMRR and PSRR vs Frequency (Referred to Input)

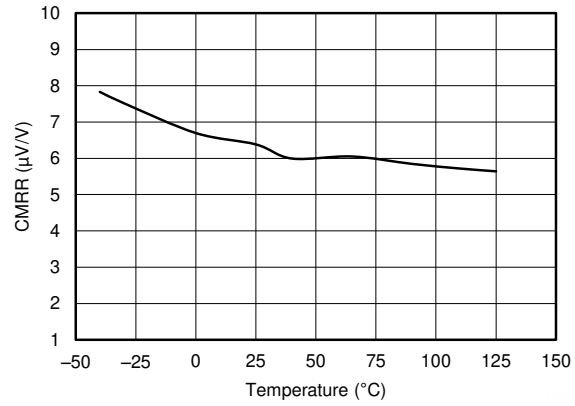


V_S = 5.5 V V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C
R_L = 10 kΩ

图 8-12. CMRR vs Temperature

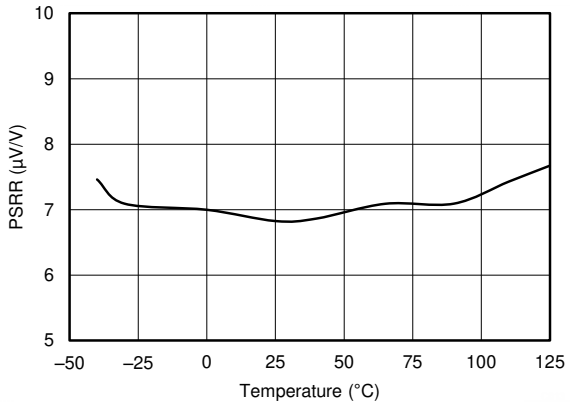
8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



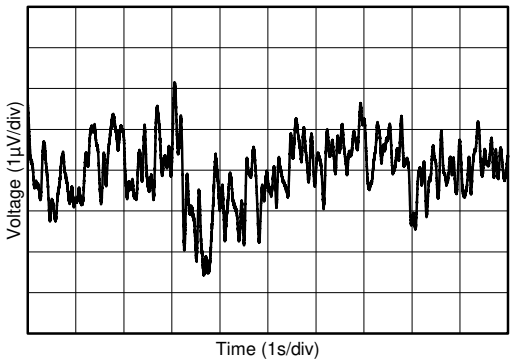
V_{CM} = (V –) – 0.1 V to (V+) – 1.4 V
T_A = –40°C to 125°C R_L = 10 kΩ V_S = 5.5 V

图 8-13. CMRR vs Temperature



V_S = 1.8 V to 5.5 V

图 8-14. PSRR vs Temperature



V_S = 1.8 V to 5.5 V

图 8-15. 0.1-Hz to 10-Hz Input Voltage Noise

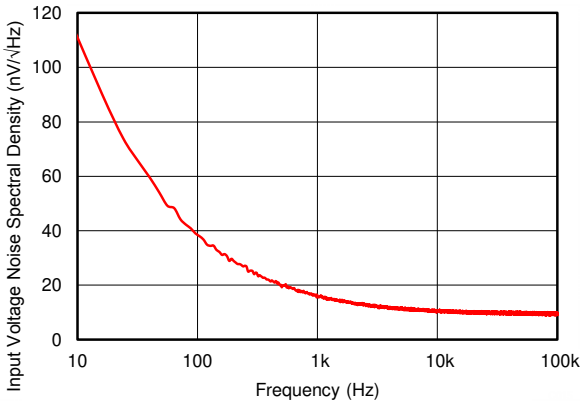
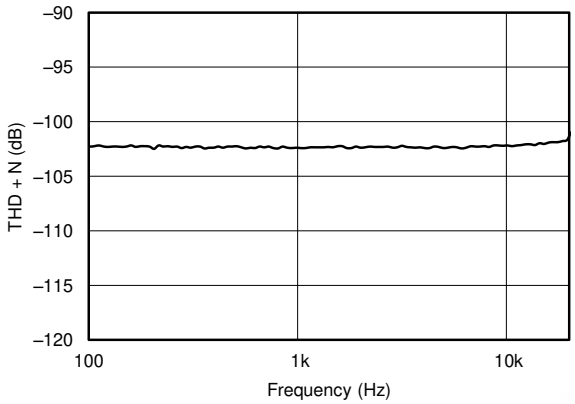
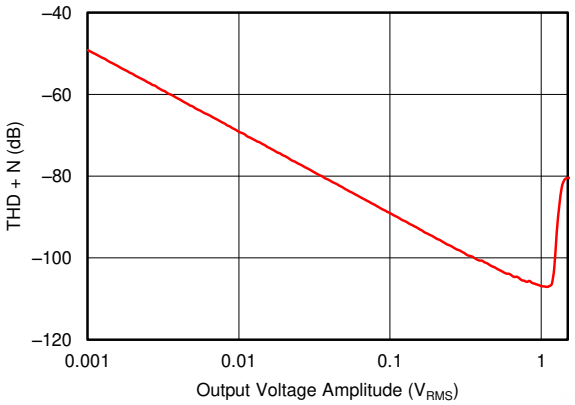


图 8-16. Input Voltage Noise Spectral Density vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V R_L = 2 kΩ
V_{OUT} = 0.5 V_{RMS} BW = 80 kHz G = +1

图 8-17. THD + N vs Frequency

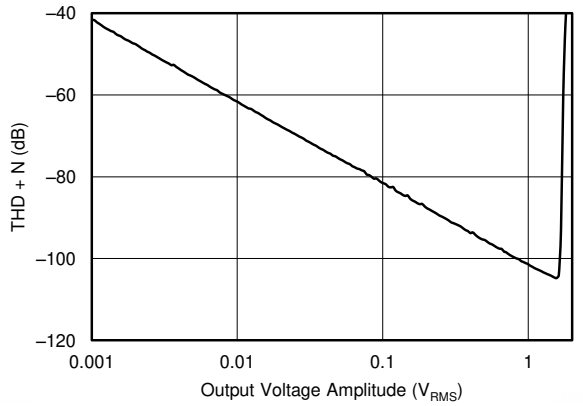


V_S = 5.5 V R_L = 2 kΩ G = +1
V_{CM} = 2.5 V BW = 80 kHz f = 1 kHz

图 8-18. THD + N vs Amplitude

8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{CM} = 2.5 V R_L = 2 kΩ
G = –1 BW = 80 kHz f = 1 kHz

图 8-19. THD + N vs Amplitude

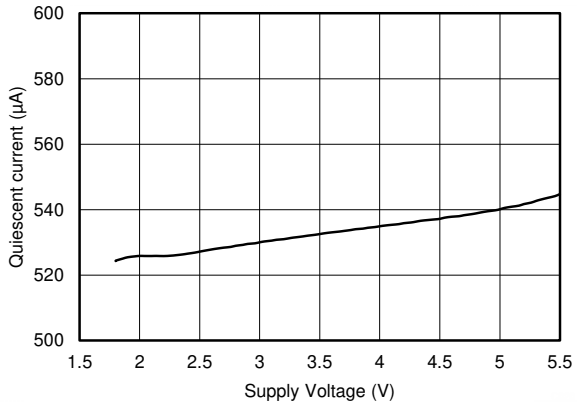


图 8-20. Quiescent Current vs Supply Voltage

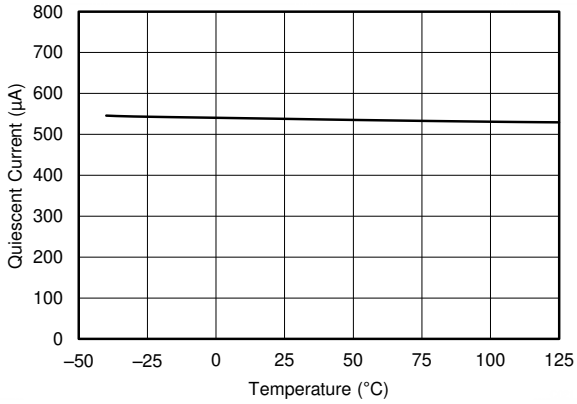


图 8-21. Quiescent Current vs Temperature

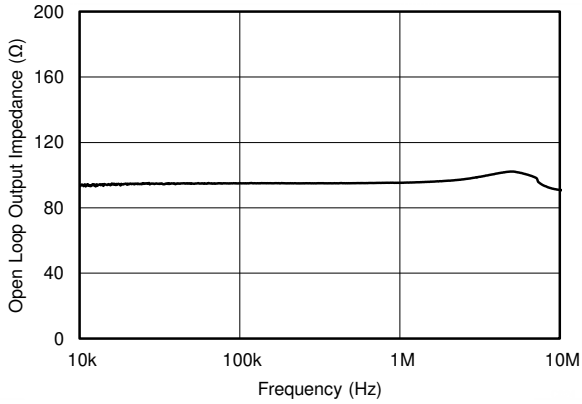
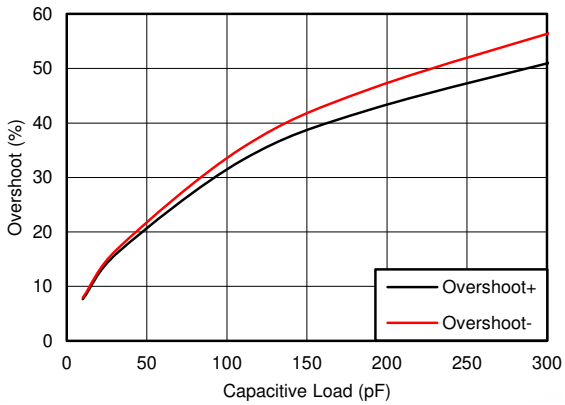
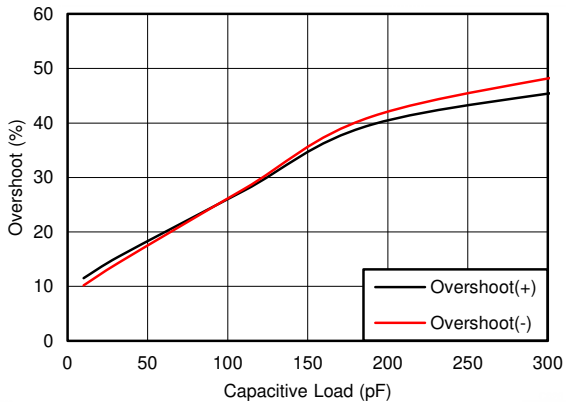


图 8-22. Open-Loop Output Impedance vs Frequency



V+ = 2.75 V V– = –2.75 V G = +1 V/V
V_{OUT} step = 100 mV_{p-p} R_L = 10 kΩ

图 8-23. Small-Signal Overshoot vs Load Capacitance

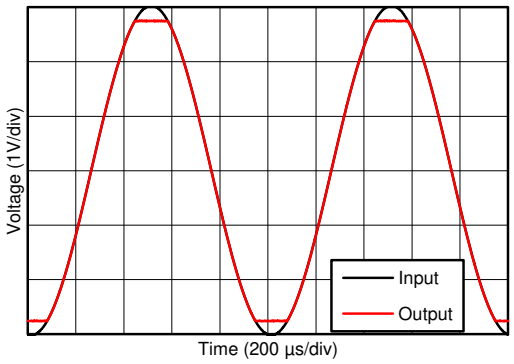


V+ = 2.75 V V– = –2.75 V G = –1 V/V
V_{OUT} step = 100 mV_{p-p} R_L = 10 kΩ

图 8-24. Small-Signal Overshoot vs Load Capacitance

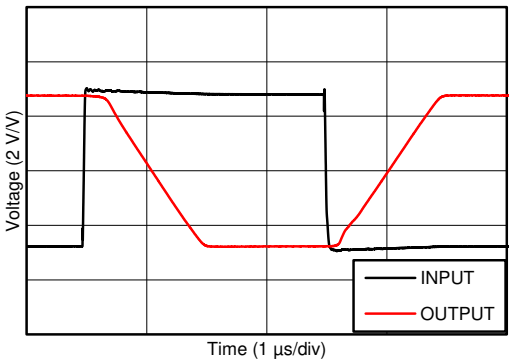
8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



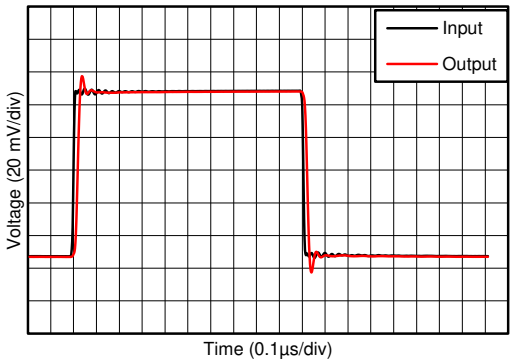
V+ = 2.75 V V– = –2.75 V

图 8-25. No Phase Reversal



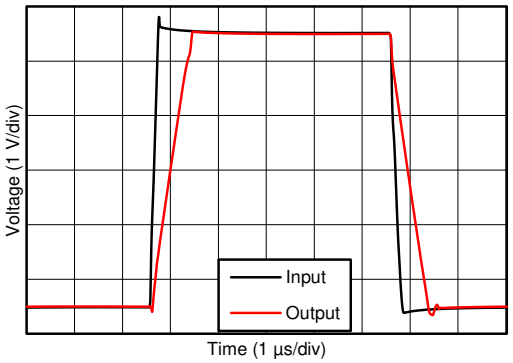
V+ = 2.75 V V– = –2.75 V G = –10 V/V

图 8-26. Overload Recovery



V+ = 2.75 V V– = –2.75 V G = 1 V/V

图 8-27. Small-Signal Step Response



V+ = 2.75 V V– = –2.75 V C_L = 100 pF
G = 1 V/V

图 8-28. Large-Signal Step Response

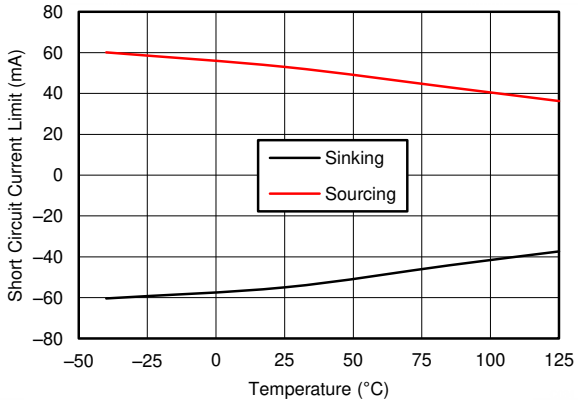
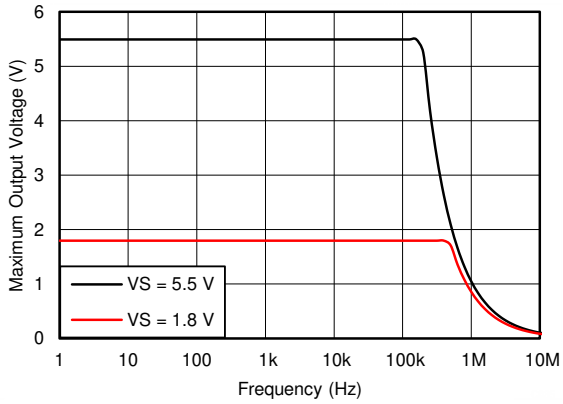


图 8-29. Short-Circuit Current vs Temperature

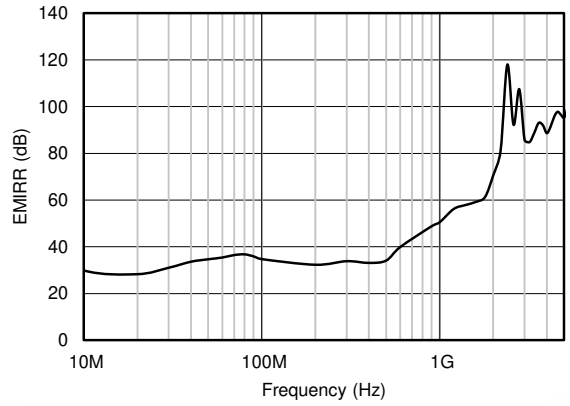


R_L = 10 kΩ C_L = 10 pF

图 8-30. Maximum Output Voltage vs Frequency and Supply Voltage

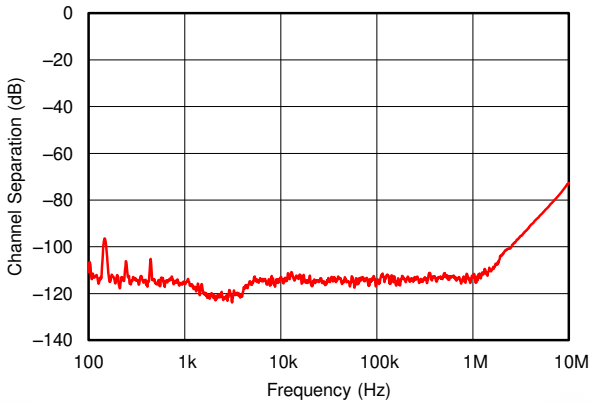
8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



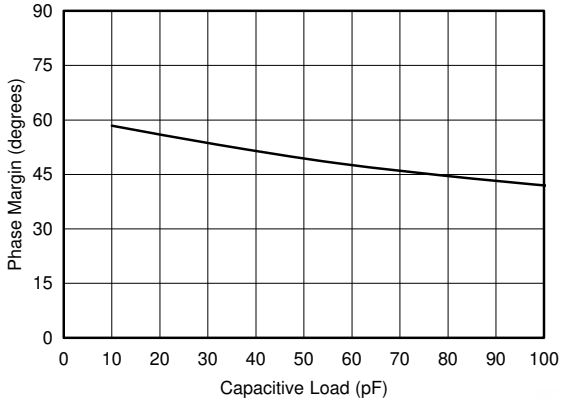
P_{RF} = – 10 dBm

图 8-31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



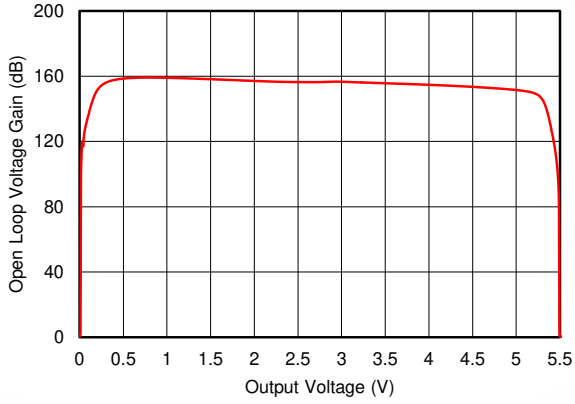
V+ = 2.75 V V – = – 2.75 V

图 8-32. Channel Separation vs Frequency



V_S = 5.5 V

图 8-33. Phase Margin vs Capacitive Load



V_S = 5.5 V

图 8-34. Open Loop Voltage Gain vs Output Voltage

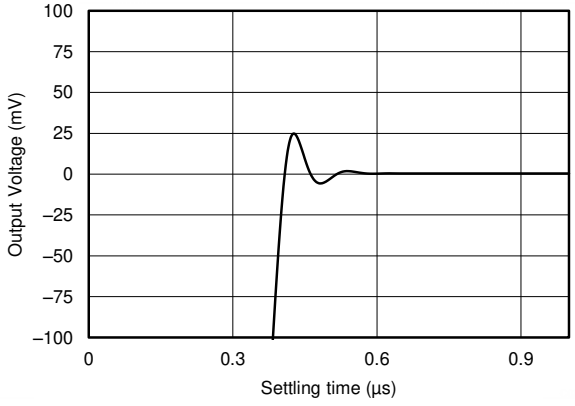


图 8-35. Large Signal Settling Time (Positive)

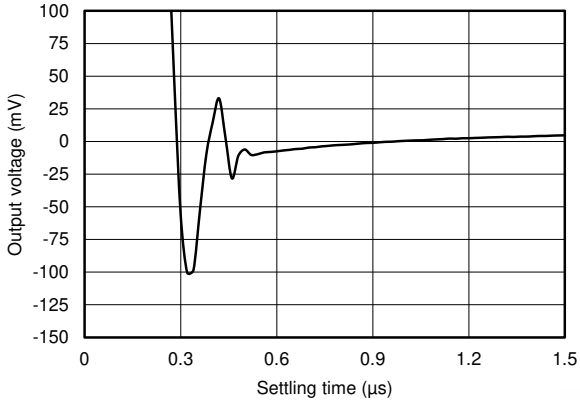


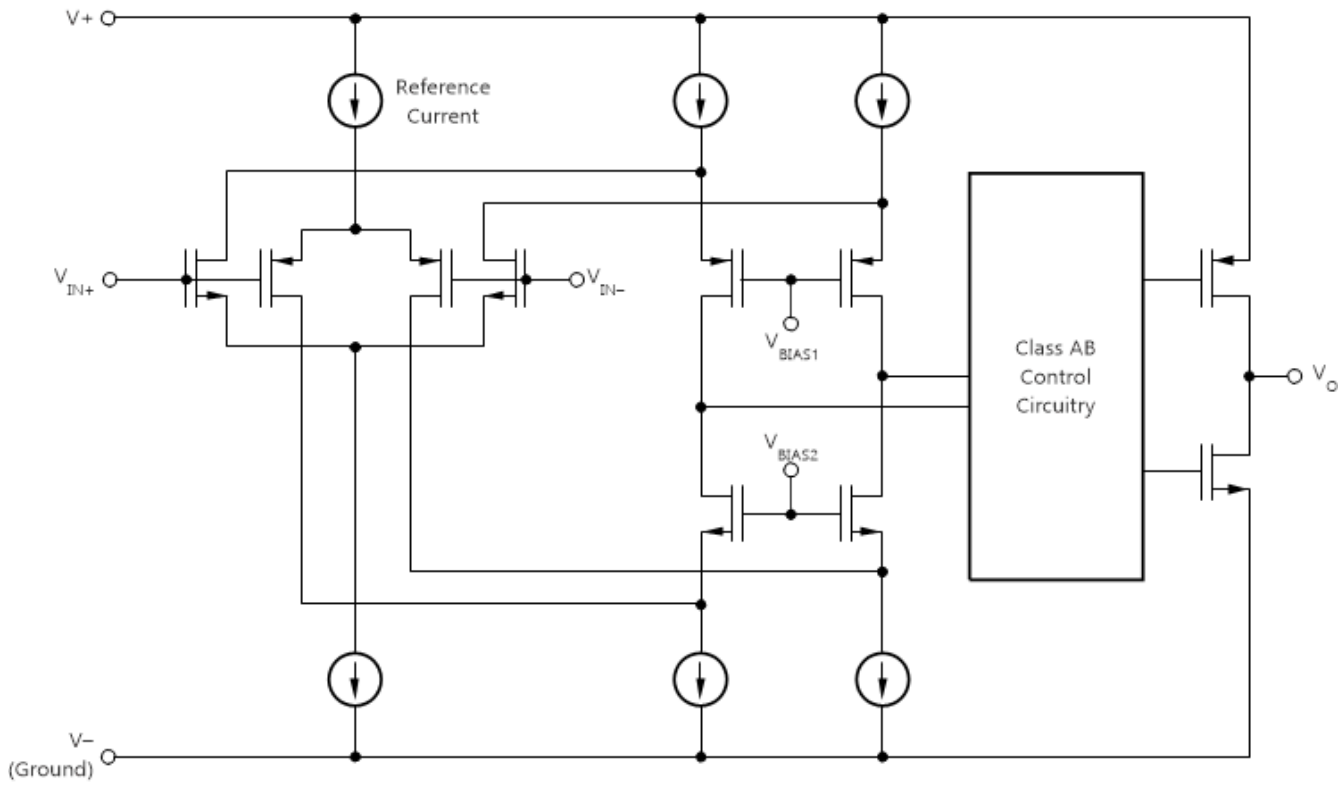
图 8-36. Large Signal Settling Time (Negative)

9 Detailed Description

9.1 Overview

The TLV906x-Q1 devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-hold circuitry of analog-to-digital converters (ADCs).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

9.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x-Q1 series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

9.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x-Q1 family is approximately 200 ns.

9.3.4 Shutdown Function

The TLV906xS-Q1 devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The $\overline{\text{SHDN}}$ pins are active-low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.2 V and V+. The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS-Q1 to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV906xS-Q1 without a load, the resulting turnoff time is significantly increased.

9.4 Device Functional Modes

Devices in the TLV906x-Q1 family are operational when the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TLV906x-Q1 family features 10-MHz bandwidth and 6.5-V/µs slew rate with only 538 µA of supply current per channel, providing good AC performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10 nV/√Hz at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

10.2 Typical Applications

10.2.1 Typical Low-Side Current Sense Application

图 10-1 shows the TLV906x-Q1 configured in a low-side current-sensing application.

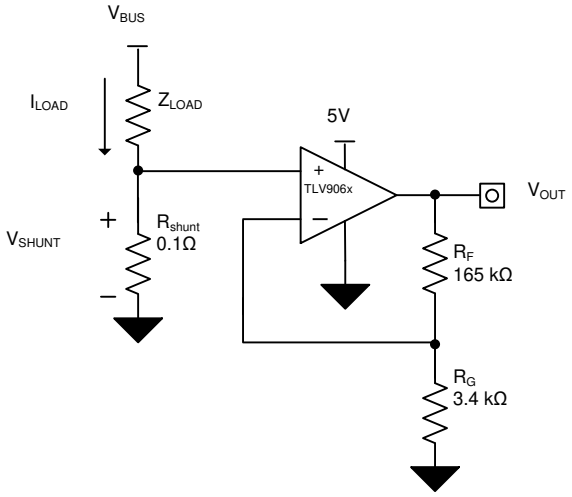


图 10-1. TLV906x-Q1 in a Low-Side, Current-Sensing Application

10.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

10.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 10-1 is given in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 方程式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using 方程式 2, R_{SHUNT} equals 100 m Ω. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV906x-Q1 to produce an output voltage of approximately 0 V to 4.95 V. 方程式 3 calculates the gain required for the TLV906x-Q1 to produce the required output voltage.

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{3}$$

Using 方程式 3, the required gain equals 49.5 V/V, which is set with the R_F and R_G resistors. 方程式 4 sizes the R_F and R_G, resistors to set the gain of the TLV906x-Q1 to 49.5 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Selecting R_F to equal 165 k Ω and R_G to equal 3.4 k Ω provides a combination that equals approximately 49.5 V/V. Low-Side, Current-Sense, Transfer Function shows the measured transfer function of the circuit shown in 图 10-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

10.2.1.3 Application Curve

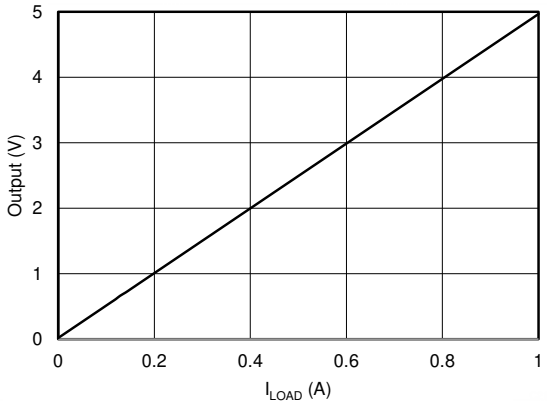


图 10-2. Low-Side, Current-Sense, Transfer Function

10.2.2 Typical Comparator Application

Comparators are used to differentiate between two different signal levels. For example, a comparator can be used to differentiate between an overvoltage situation and normal operation. The TLV9062-Q1 can be used as a comparator by applying the two voltages being compared to each input without any feedback from output to inverting input.

The TLV9062-Q1 features a rail-to-rail input and output stage with an input common-mode range that exceeds the supply rails by 100 mV. The TLV9062-Q1 is designed to prevent phase reversal over the entire input common-mode range. The propagation delay for the TLV9062-Q1 used as a comparator is equal to the overload recovery time plus the slew rate. Overdrive voltages less than 100 mV result in longer propagation delays because the overload recovery time increases and the slew rate decreases.

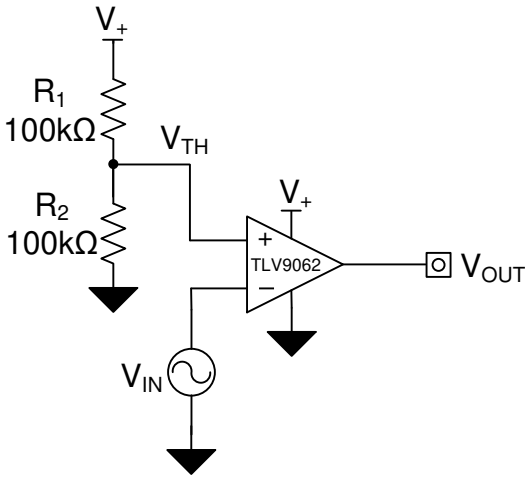


图 10-3. Typical Comparator Application

10.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage (V_+): 5 V
- Input (V_{IN}): 0 V to 5 V
- Threshold voltage (V_{TH}): 2.5 V

10.2.2.2 Detailed Design Procedure

The inverting comparator circuit applies the input voltage (V_{IN}) to the inverting terminal of the op amp. Two resistors (R1 and R2) divide the supply voltage (V_{CC}) to create a midsupply threshold voltage (V_{TH}) as calculated in 方程式 5. The circuit is shown in 图 10-3. When V_{IN} is less then V_{TH}, the output voltage transitions to the positive supply and equals the high-level output voltage. When V_{IN} is greater than V_{TH}, the output voltage transitions to the negative supply and equals the low-level output voltage, V_{TH}.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ = 2.5V \tag{5}$$

10.2.2.3 Application Curves

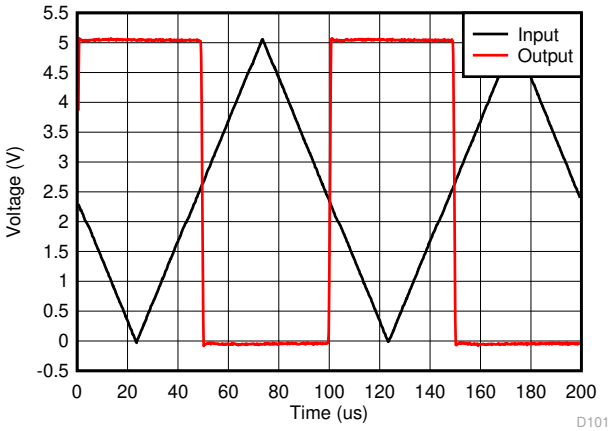


图 10-4. Comparator Response to Input Voltage (Propagation Delay Included)

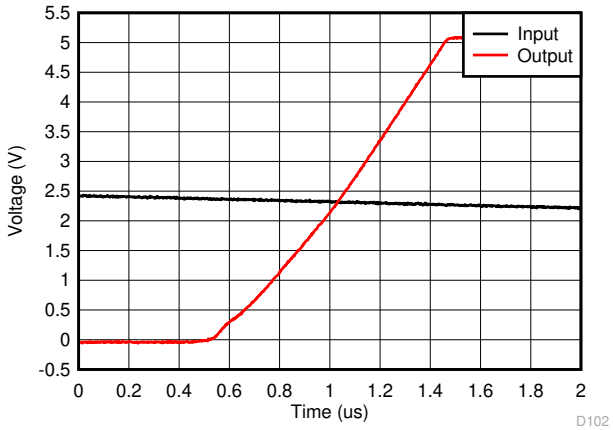


图 10-5. Rising Edge

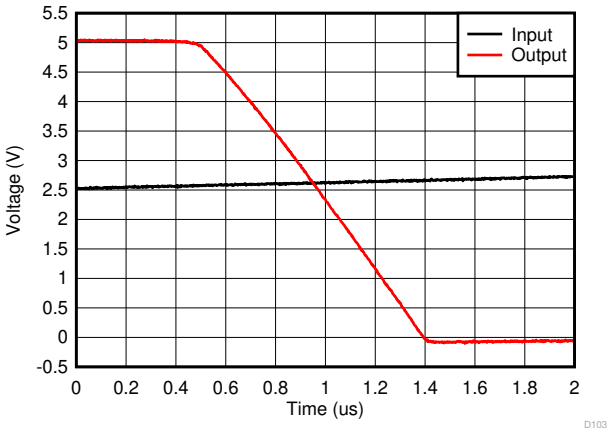


图 10-6. Falling Edge

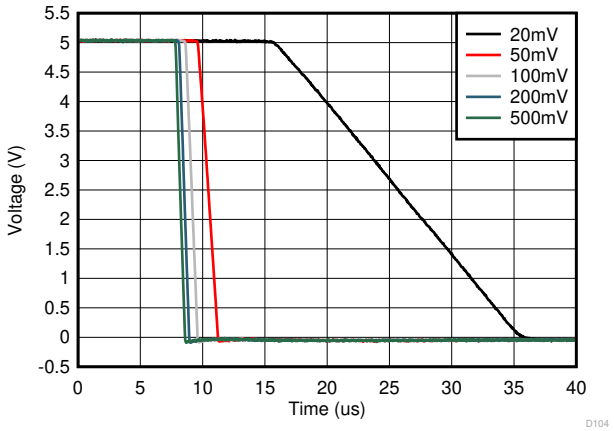


图 10-7. Falling Edge Propagation Delay vs Input Overdrive Voltage

11 Power Supply Recommendations

The TLV906x-Q1 series is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11.1 Input and ESD Protection

The TLV906x-Q1 series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the *Absolute Maximum Ratings* table. 图 11-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

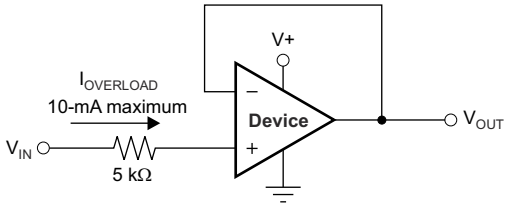


图 11-1. Input Current Protection

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 12-2, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

12.2 Layout Example

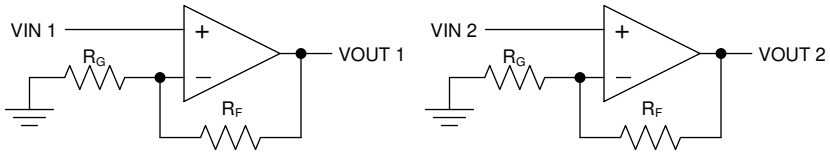


图 12-1. Schematic Representation

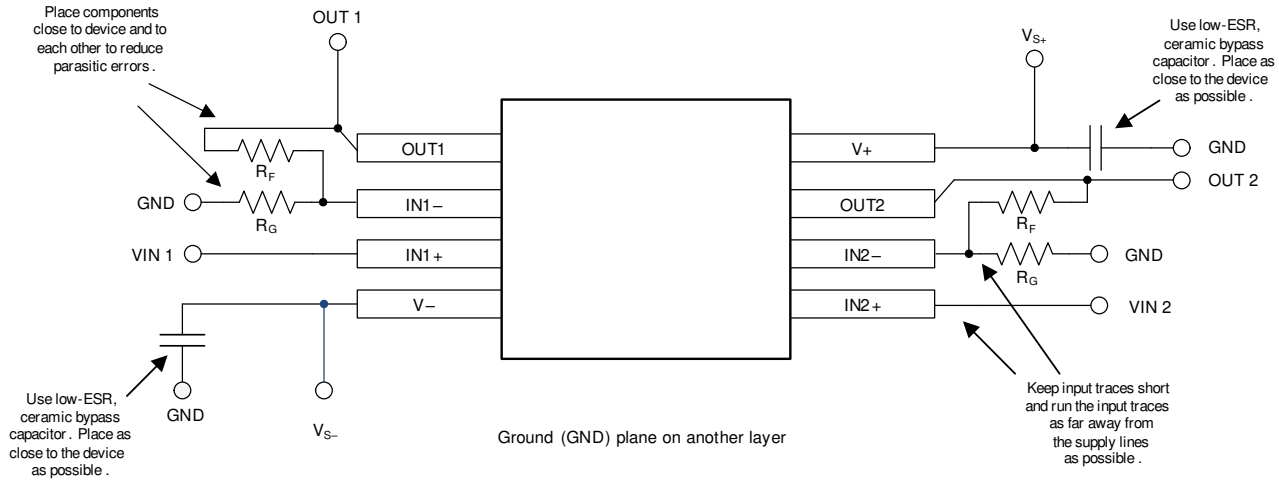


图 12-2. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Texas Instruments, *TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet.

Texas Instruments, *TLVx314-Q1 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier* data sheet.

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report.

Texas Instruments, *QFN/SON PCB Attachment* application report.

Texas Instruments, *Single-Ended Input to Differential Output Conversion Circuit Reference Design*.

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 13-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9062-Q1	Click here	Click here	Click here	Click here	Click here
TLV9064-Q1	Click here	Click here	Click here	Click here	Click here

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9061SQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2CTF	Samples
TLV9062QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27CT	Samples
TLV9062QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9062Q	Samples
TLV9064QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064QD	Samples
TLV9064QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9064Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV9061-Q1, TLV9062-Q1, TLV9064-Q1 :

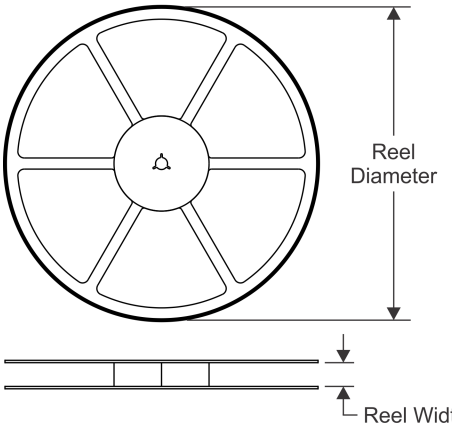
- Catalog : TLV9061, TLV9062, TLV9064

NOTE: Qualified Version Definitions:

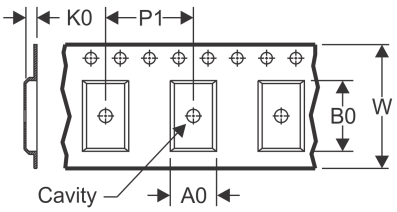
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

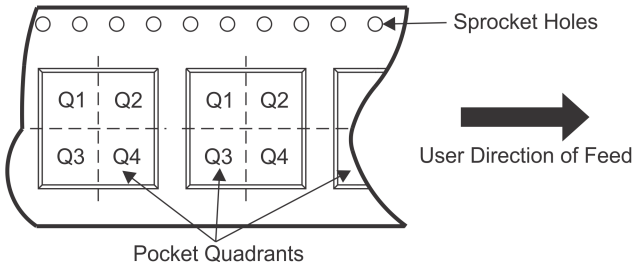


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

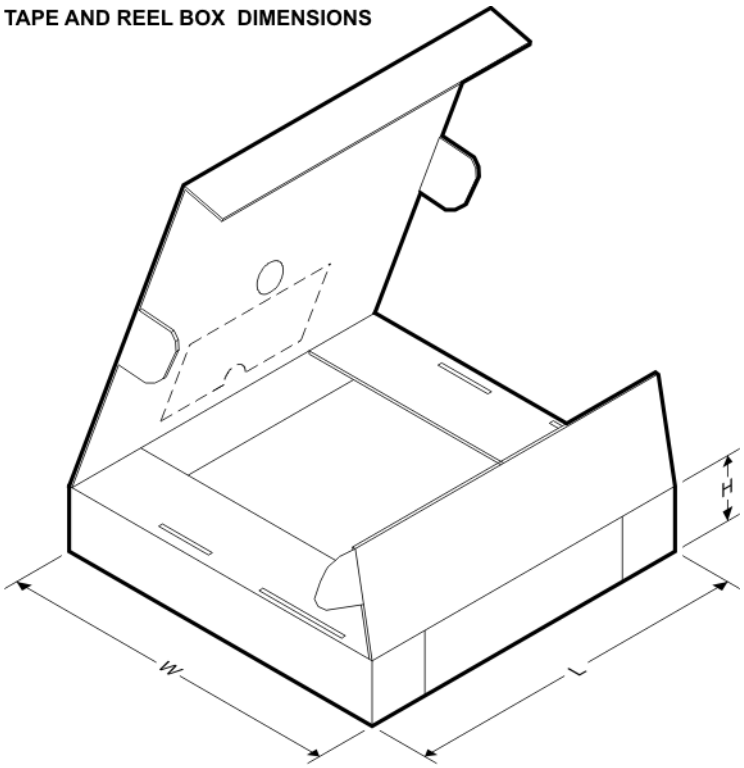
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061SQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9064QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9064QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

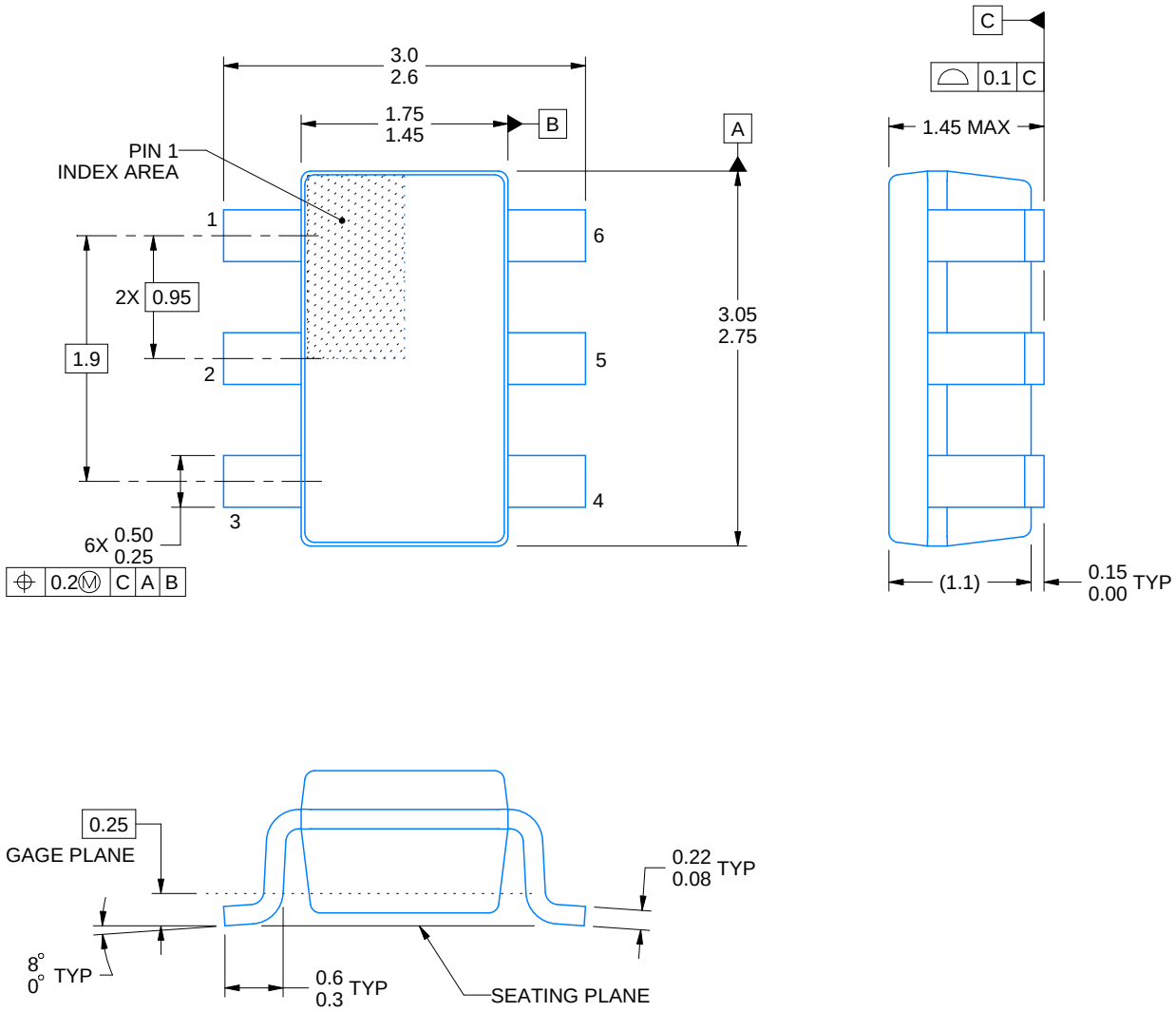
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061SQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9062QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9062QDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TLV9064QDRQ1	SOIC	D	14	2500	853.0	449.0	35.0
TLV9064QPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

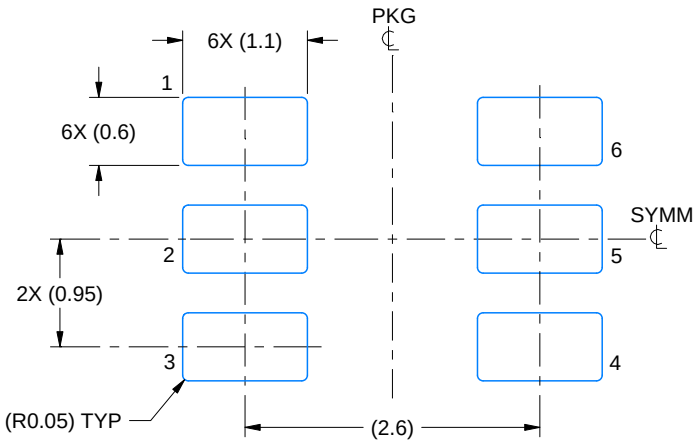
SMALL OUTLINE TRANSISTOR



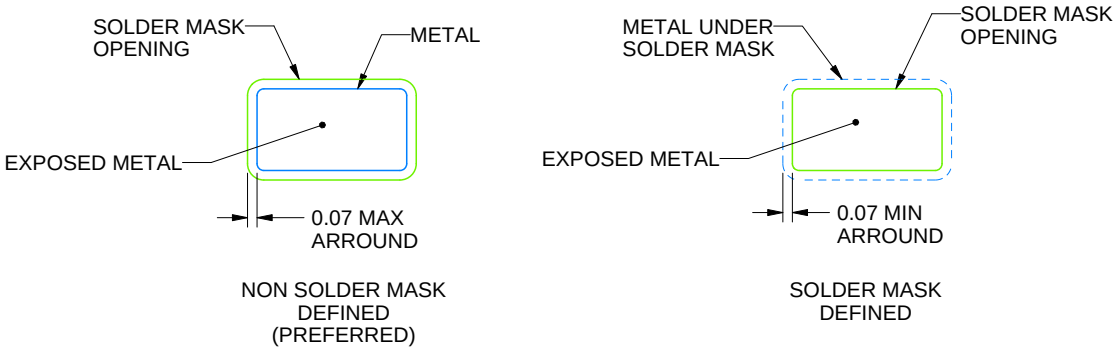
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

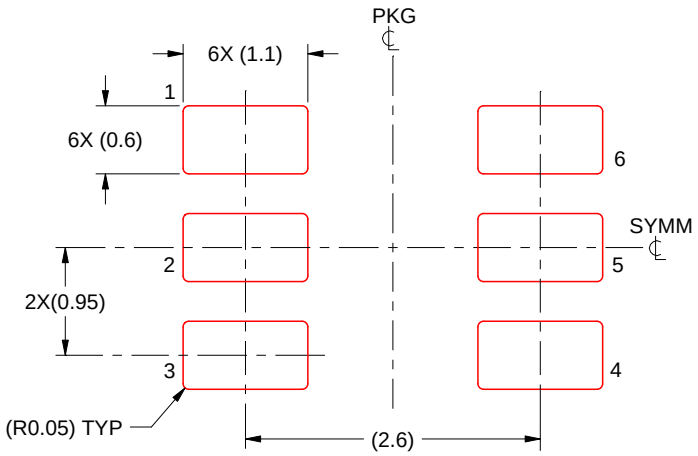


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



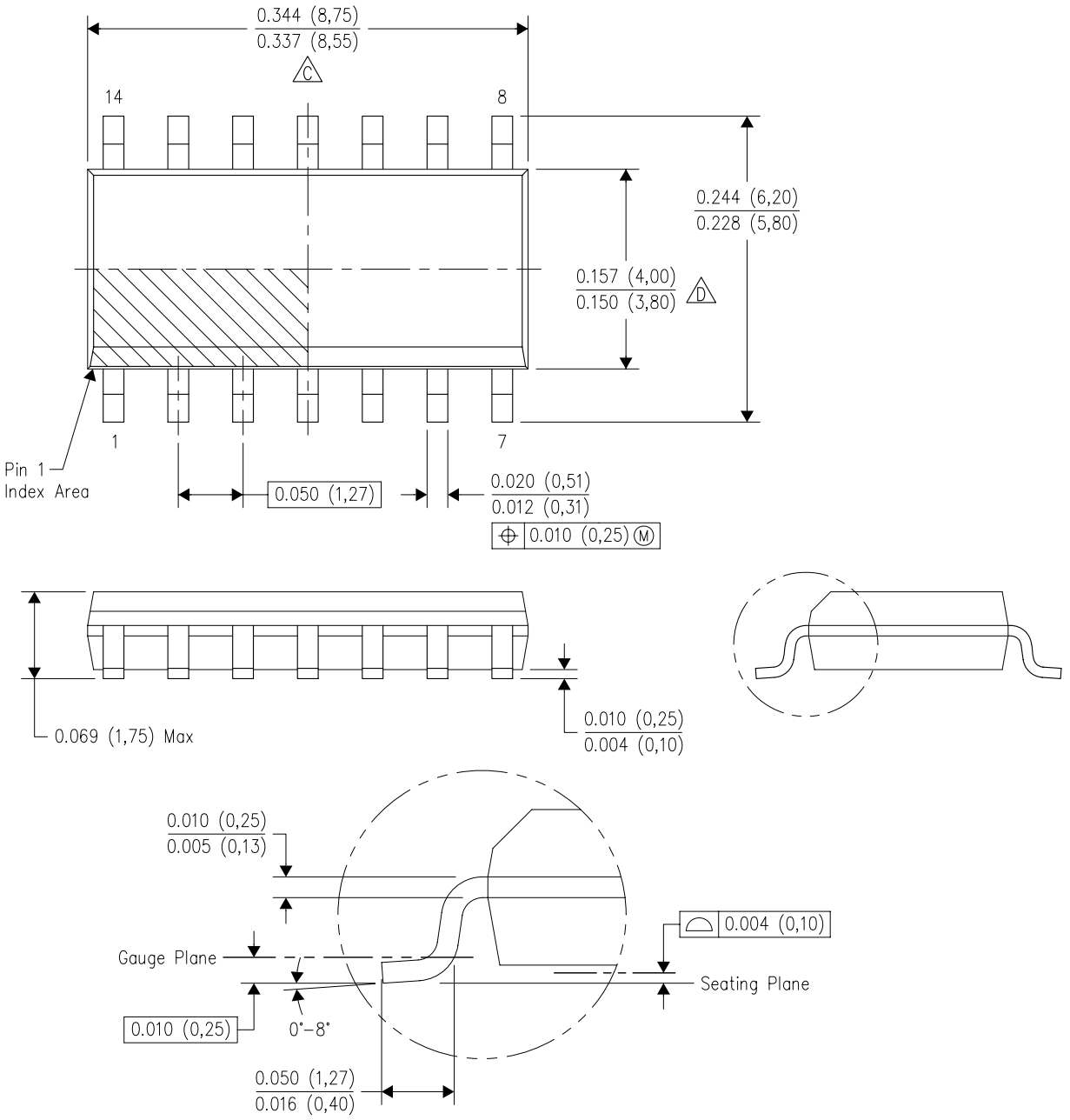
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

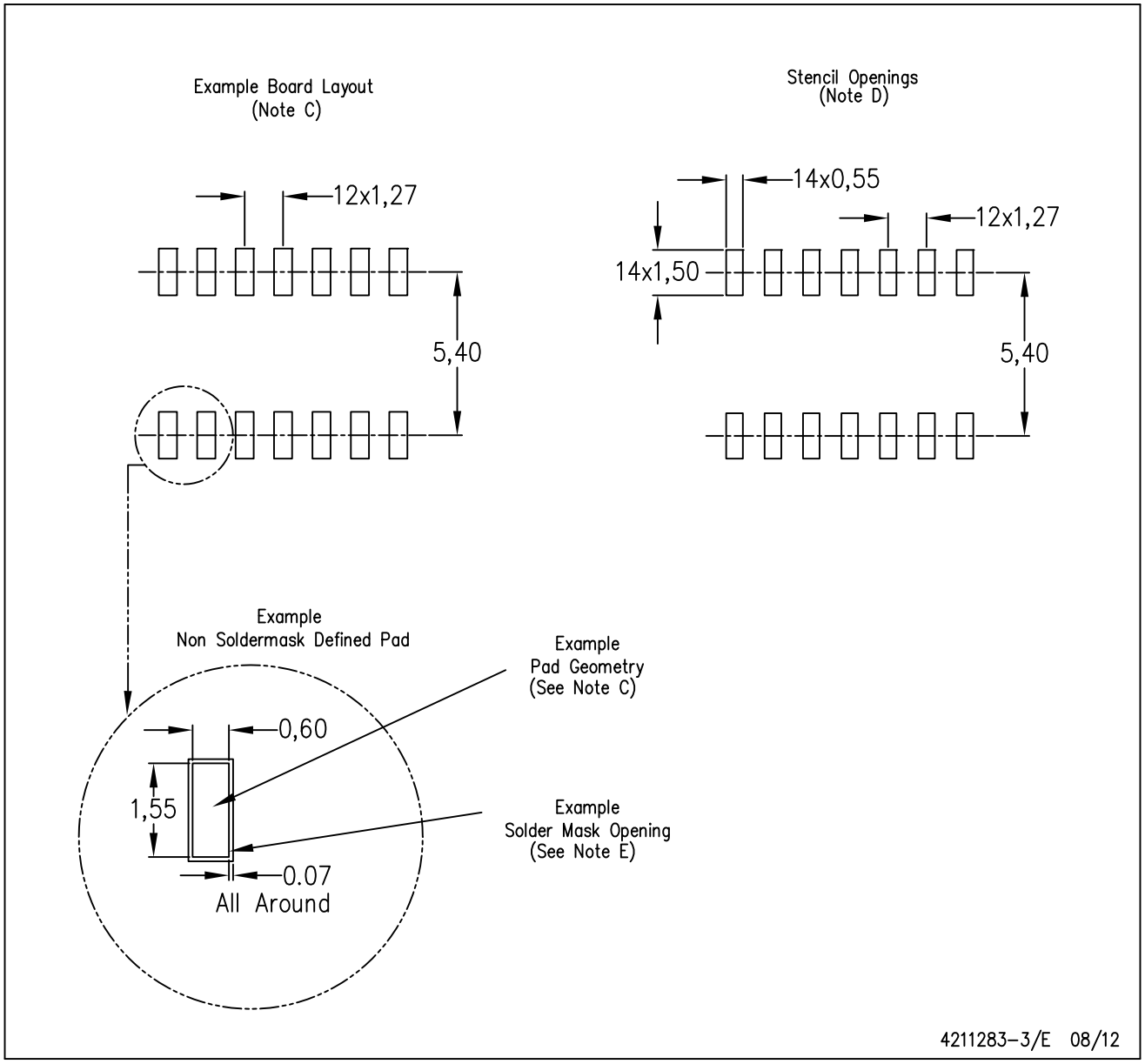
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

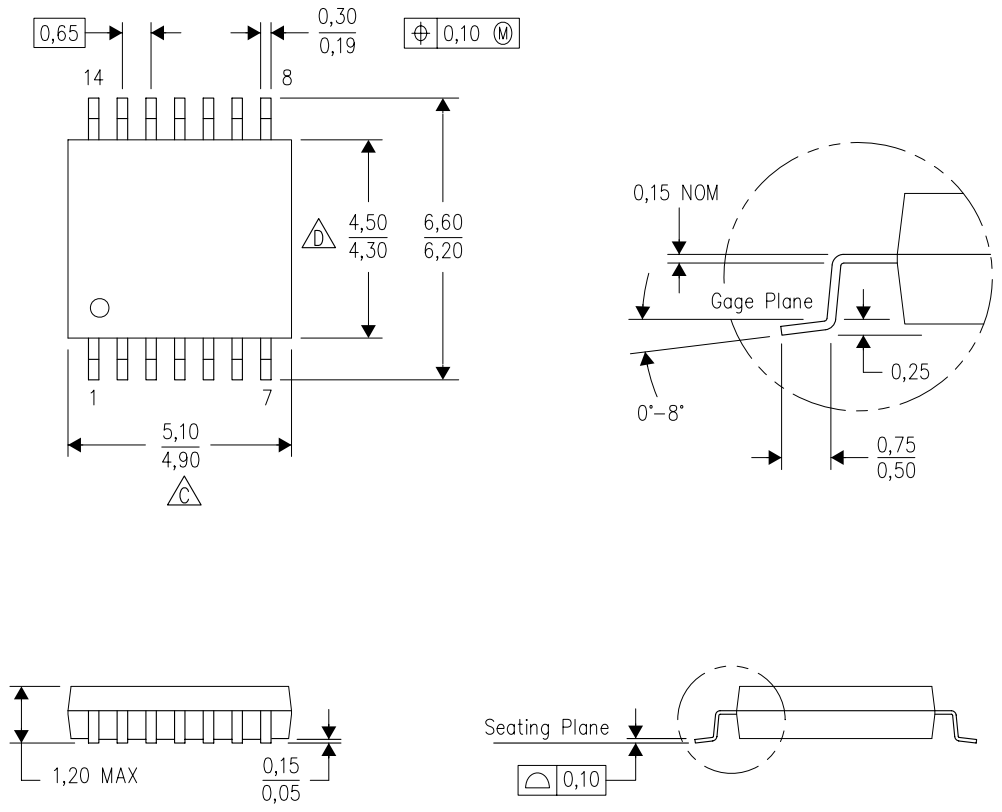
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

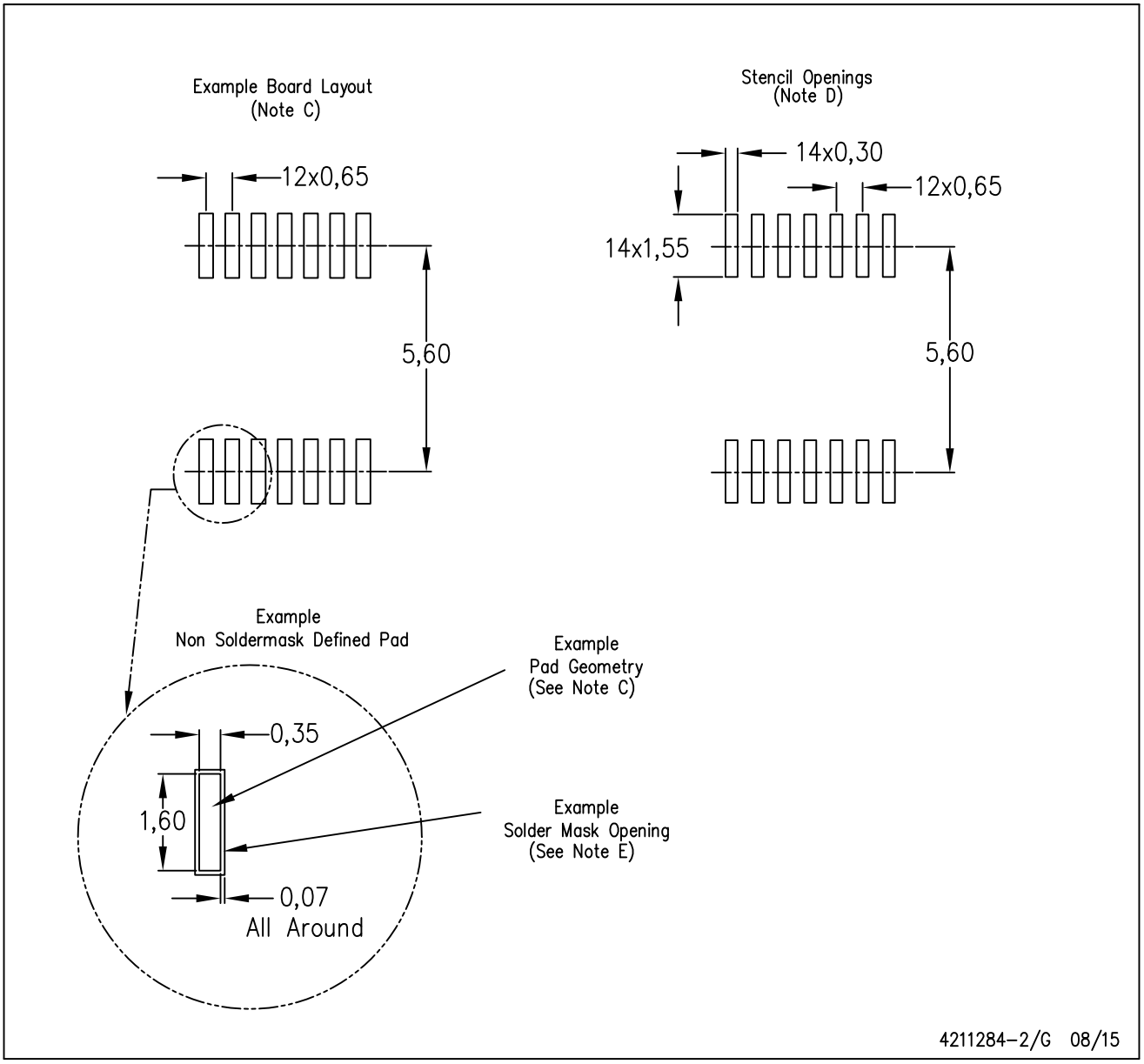
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



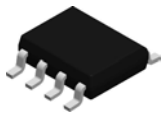
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

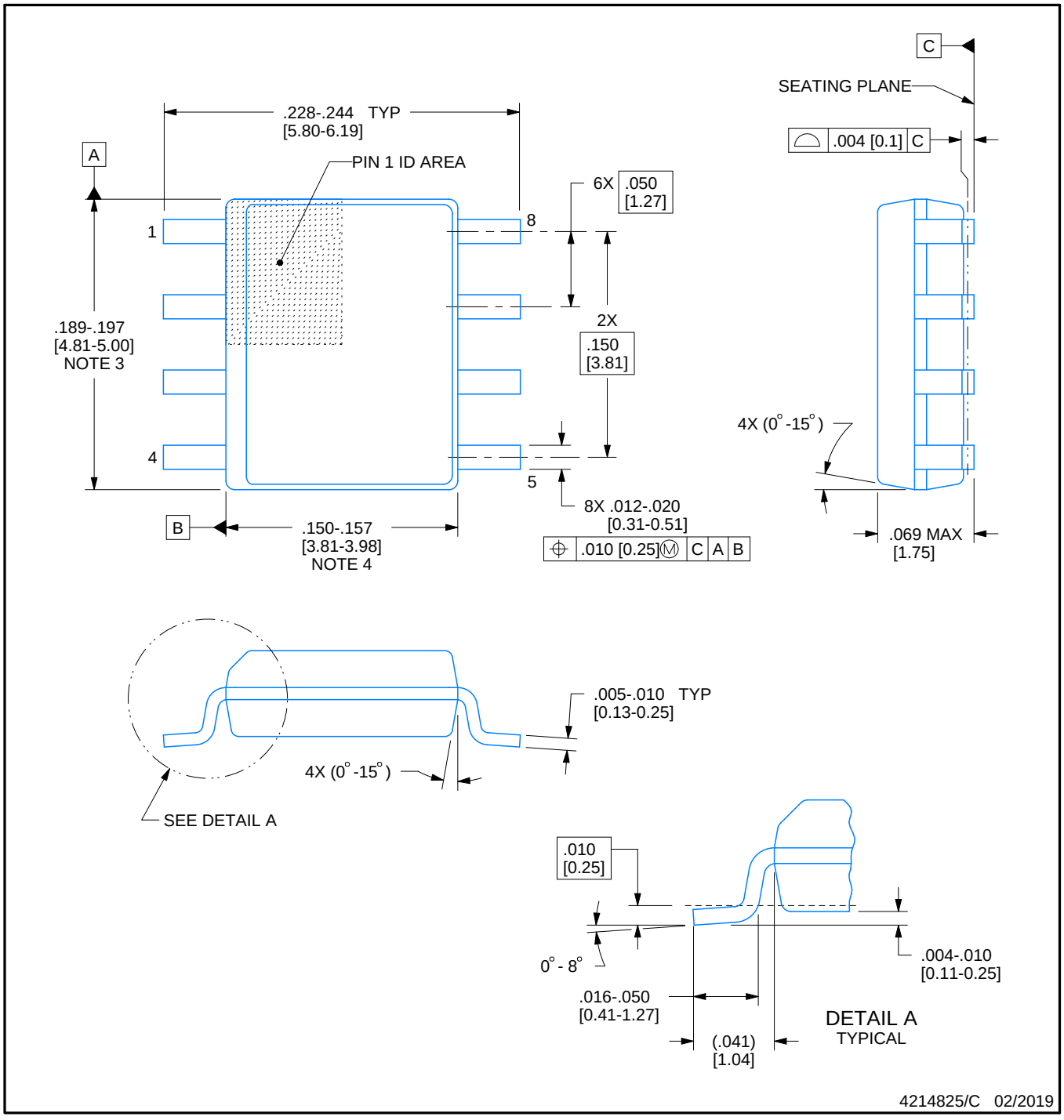


PACKAGE OUTLINE

D0008A

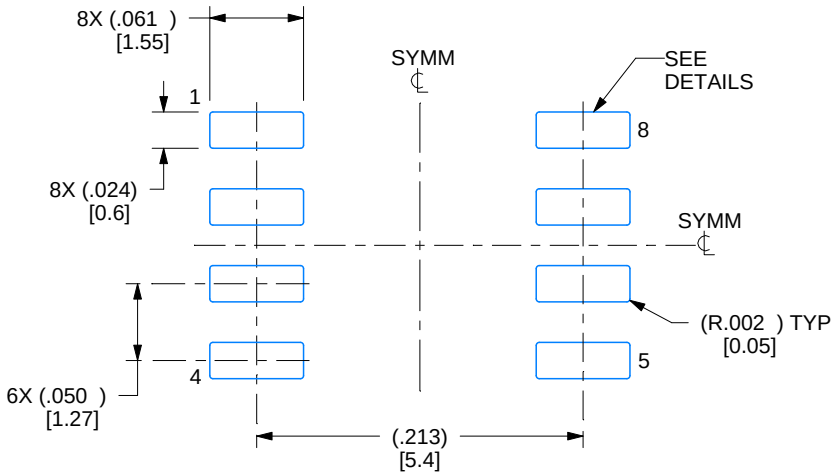
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

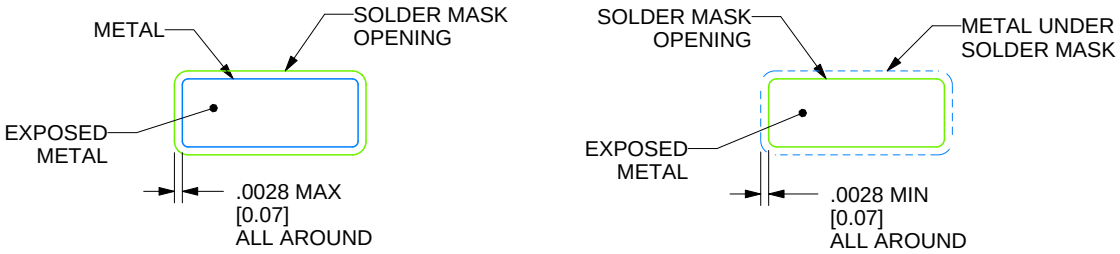


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

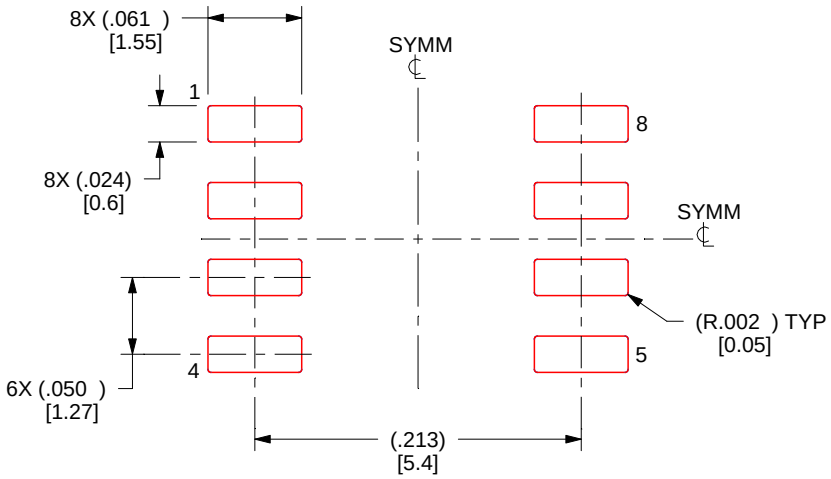
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



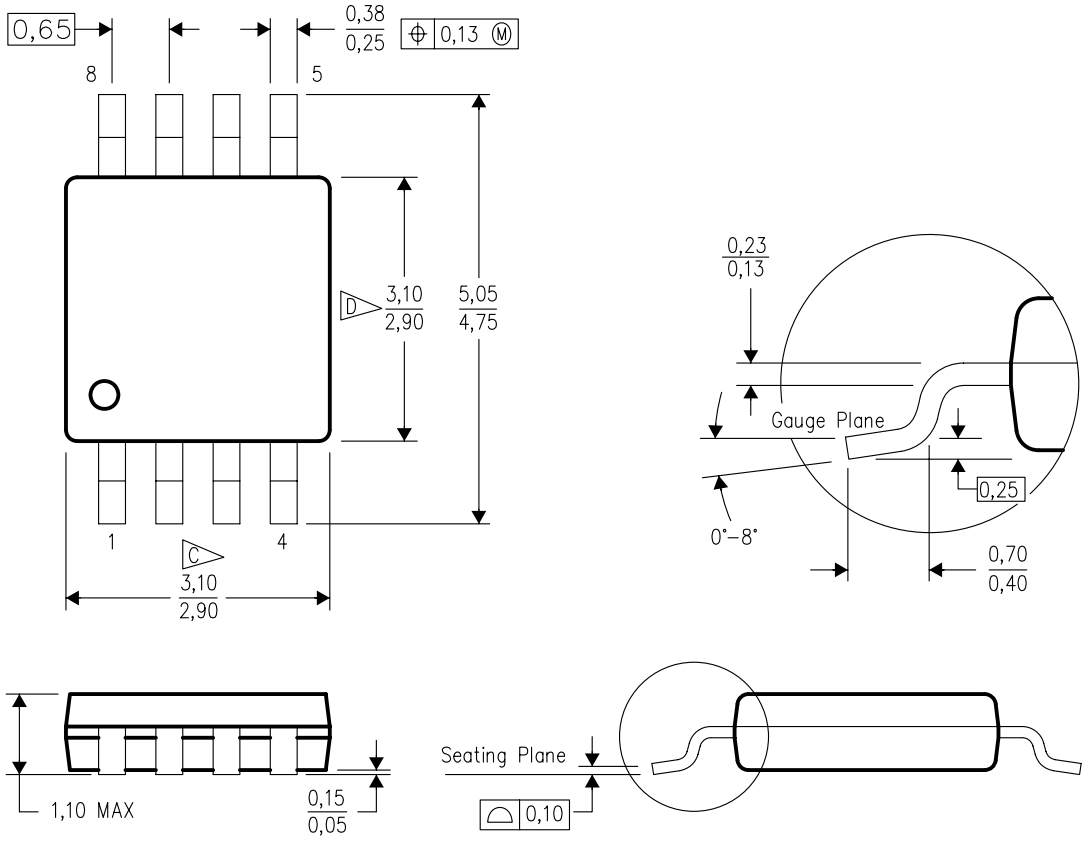
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

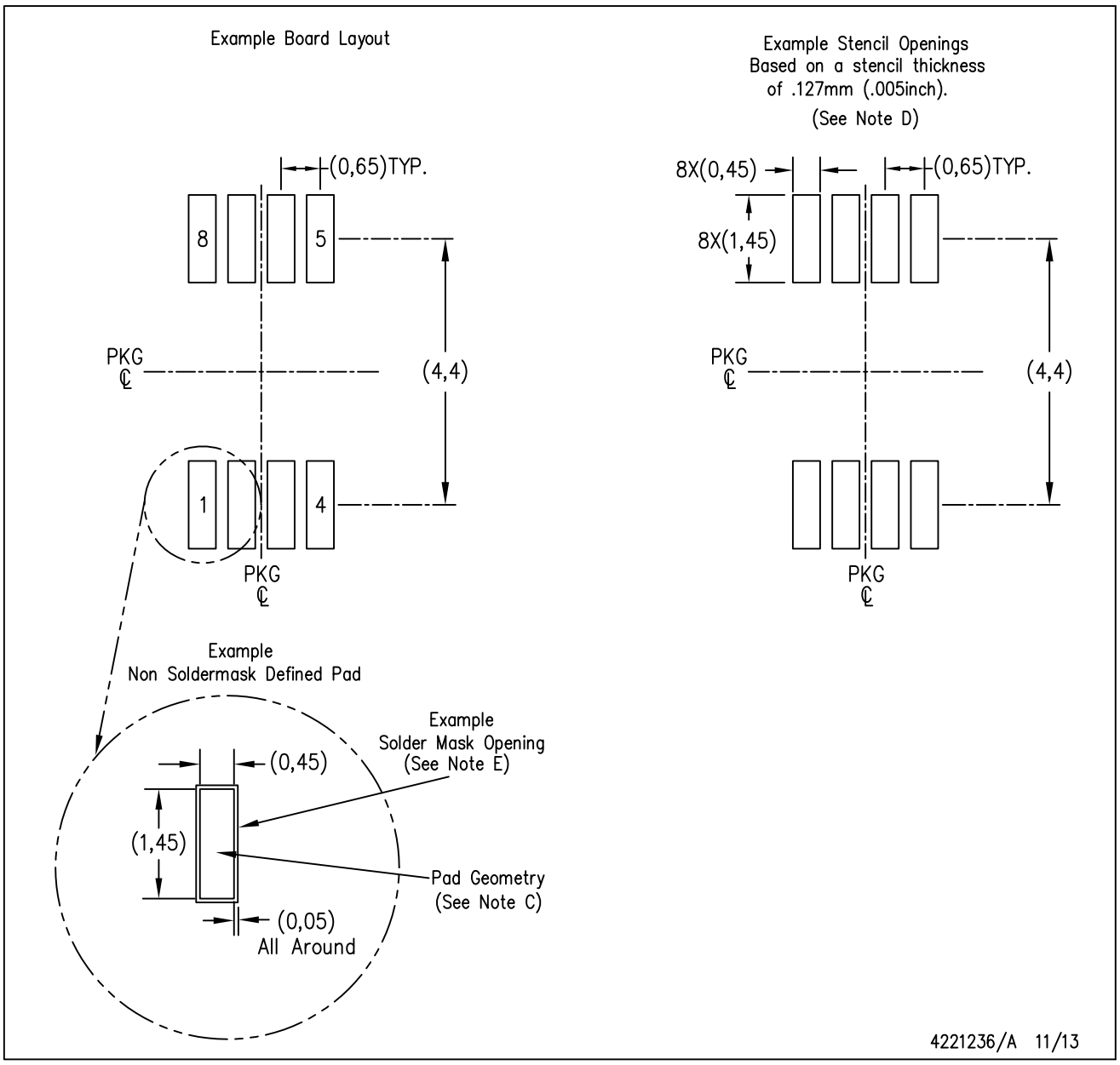
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122