



# TPS54JA20 2.7-V to 16-V Input, 12-A Synchronous Buck Converter With Remote Sense, 3-V Internal LDO and Latch-off Current Limit

## 1 Features

- 4-V to 16-V input range up to 12-A without external bias
- 2.7-V to 16-V input range up to 12 A with external bias ranging from 3.13 V to 5.3 V
- Output voltage range: 0.9 V to 5.5 V
- Integrated 10.2-mΩ and 3.1-mΩ MOSFETs
- D-CAP3™ with ultra fast load-step response
- Supports all ceramic output capacitors
- Differential remote sense with 0.9-V  $\pm 1\%$   $V_{REF}$  for  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  junction temperature
- Auto-skip Eco-mode™ for high light-load efficiency
- Programmable current limit with  $R_{TRIP}$
- Pin-selectable switching frequency: 600 kHz, 800 kHz, 1 MHz
- Programmable soft-start time
- External reference input for tracking
- Prebiased startup capability
- Open-drain power-good output
- Latch-off for OC, UV and OV faults
- 4-mm × 3-mm, 21-pin QFN package
- Pin compatible with 15-A [TPS548A28/TPS548A29](#)
- Fully RoHS compliant without exemption

## 2 Applications

- Rack server and Blade server
- Hardware accelerator and add-in cards
- Data center switches
- Industrial PC

## 3 Description

The TPS54JA20 device is a small high-efficiency synchronous buck converter with an adaptive on-time D-CAP3 control mode. Since external compensation is not required, the device is easy to use and requires few external components. The device is well-suited for space-constrained data center applications.

The TPS54JA20 device has differential remote sense, high-performance integrated MOSFETs, and an accurate  $\pm 1\%$ , 0.9-V reference over the full operating junction temperature range. The device features fast load-transient response, accurate load regulation and line regulation, Skip-mode or FCCM operation, and programmable soft-start.

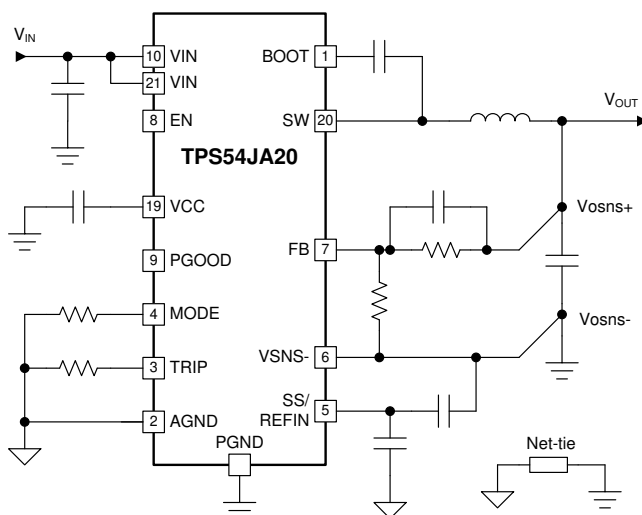
The TPS54JA20 device is a lead-free device. It is fully RoHS compliant without exemption.

### Device Information<sup>1</sup>

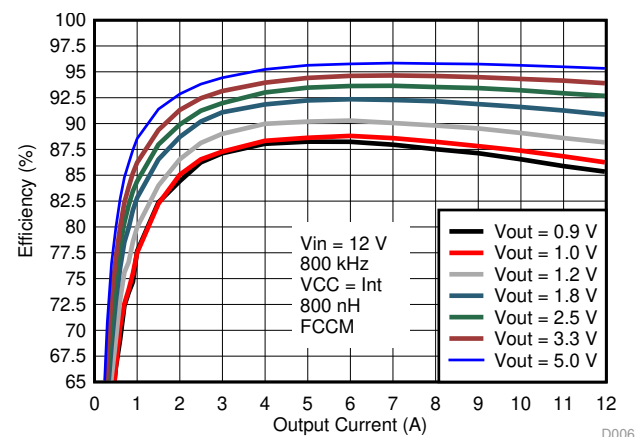
| PART NUMBER | PACKAGE      | BODY SIZE (NOM)   |
|-------------|--------------|-------------------|
| TPS54JA20   | VQFN-HR (21) | 4.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



### Efficiency Graph



D006



## Table of Contents

|  |           |  |           |
|--|-----------|--|-----------|
| <b>1 Features</b> .....                        | <b>1</b>  | 7.4 Device Functional Modes.....                 | <b>20</b> |
| <b>2 Applications</b> .....                    | <b>1</b>  | <b>8 Application and Implementation</b> .....    | <b>23</b> |
| <b>3 Description</b> .....                     | <b>1</b>  | 8.1 Application Information.....                 | <b>23</b> |
| <b>4 Revision History</b> .....                | <b>2</b>  | 8.2 Typical Application .....                    | <b>23</b> |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b>  | <b>9 Power Supply Recommendations</b> .....      | <b>35</b> |
| <b>6 Specifications</b> .....                  | <b>4</b>  | <b>10 Layout</b> .....                           | <b>35</b> |
| 6.1 Absolute Maximum Ratings .....             | 4         | 10.1 Layout Guidelines .....                     | 35        |
| 6.2 ESD Ratings .....                          | 4         | 10.2 Layout Example .....                        | 36        |
| 6.3 Recommended Operating Conditions.....      | 4         | 10.3 Thermal Performance On TI EVM .....         | 36        |
| 6.4 Thermal Information .....                  | 5         | <b>11 Device and Documentation Support</b> ..... | <b>37</b> |
| 6.5 Electrical Characteristics.....            | 5         | 11.1 Documentation Support .....                 | 37        |
| 6.6 Typical Characteristics.....               | 8         | 11.2 Trademarks .....                            | 37        |
| <b>7 Detailed Description</b> .....            | <b>11</b> | 11.3 Electrostatic Discharge Caution.....        | 37        |
| 7.1 Overview .....                             | 11        | 11.4 Glossary .....                              | 37        |
| 7.2 Functional Block Diagram .....             | 11        | <b>12 Mechanical, Packaging, and Orderable</b>   |           |
| 7.3 Feature Description.....                   | 12        | <b>Information</b> .....                         | <b>37</b> |

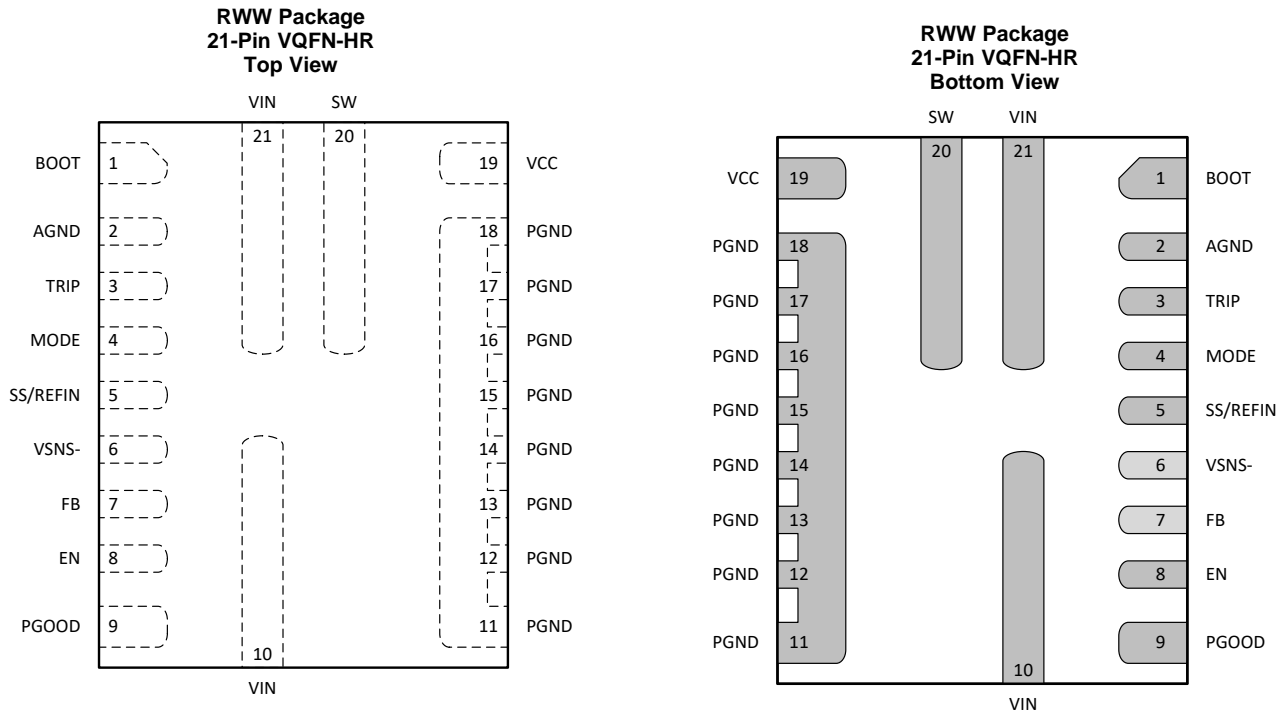
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (June 2020) to Revision B | Page     |
|---|----------|
| • Deleted redundant LDO specification.....        | <b>6</b> |

| Changes from Original (March 2020) to Revision A                            | Page      |
|---|-----------|
| • Changed document title .....  | <b>1</b>  |
| • Changed UVLO threshold in Functional Block Diagram. ....                  | <b>11</b> |
| • Added description for KOCL and how to use it for tolerance analysis. .... | <b>17</b> |
| • Added a new equation, IOCLIM vs KOCL. ....                                | <b>18</b> |

## 5 Pin Configuration and Functions



### Pin Functions

| NO. | NAME     | I/O <sup>(1)</sup> | DESCRIPTION  |
|-----|----------|--------------------|--|
| 1   | BOOT     | I/O                | Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to SW node.  |
| 2   | AGND     | G                  | Ground pin, reference point for the internal control circuits.   |
| 3   | TRIP     | I/O                | Current limit setting pin. Connect a resistor to AGND to set the current limit trip point. ±1% tolerance resistor is highly recommended. See <a href="#">Current Sense and Positive Overcurrent Protection</a> for details on OCL setting.   |
| 4   | MODE     | I                  | The MODE pin sets the forced continuous-conduction mode (FCCM) or Skip-mode operation. It also selects the operating frequency by connecting a resistor from MODE pin to AGND pin. ±1% tolerance resistor is recommended. See <a href="#">Table 1</a> for details.   |
| 5   | SS/REFIN | I/O                | Dual-function pin. Soft-start function: Connecting a capacitor to VSNS– pin programs soft-start time. Minimum soft-start time (1.5 ms) is fixed internally. A minimum 1-nF capacitor is required for this pin to avoid overshoot during the charge of soft-start capacitor. REFIN function: The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. The internal reference voltage can be overridden by an external DC voltage source on this pin for tracking application. |
| 6   | VSNS–    | I                  | The return connection for a remote voltage sensing configuration. It is also used as ground for the internal reference. Short to AGND for single-end sense configuration.  |
| 7   | FB       | I                  | Output voltage feedback input. A resistor divider from the V <sub>OUT</sub> to VSNS– (tapped to FB pin) sets the output voltage.   |
| 8   | EN       | I                  | Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating EN pin before startup disables the converter. The recommended operating condition for EN pin is maximum 5.5-V. DO NOT connect EN pin to VIN pin directly.   |
| 9   | PGOOD    | O                  | Open-drain power-good status signal. When the FB voltage moves outside the specified limits, PGOOD goes low after 2-μs delay.  |

(1) I = Input, O = Output, P = Supply, G = Ground

### Pin Functions (continued)

| NO.                            | NAME | I/O <sup>(1)</sup> | DESCRIPTION  |
|--------------------------------|------|--------------------|--|
| 10, 21                         | VIN  | P                  | Power-supply input pins for both integrated power MOSFET pair and the internal LDO. Place the decoupling input capacitors from VIN pins to PGND pins as close as possible.   |
| 11, 12, 13, 14, 15, 16, 17, 18 | PGND | G                  | Power ground of internal low-side MOSFET. At least 6 PGND vias are required to be placed as close as possible to the PGND pins. This minimizes parasitic impedance and also lowers thermal resistance.   |
| 19                             | VCC  | I/O                | Internal 3-V LDO output. An external bias with 3.3-V or higher voltage can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. Require a 2.2-μF, at least 6.3-V rating ceramic capacitor from VCC pin to PGND pins as the decoupling capacitor and the placement is required to be as close as possible. |
| 20                             | SW   | O                  | Output switching terminal of the power converter. Connect this pin to the output inductor.   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) <sup>(1)</sup>

|  |                                       | MIN  | MAX  | UNIT |
|--|---------------------------------------|------|------|------|
| Pin voltage                                    | VIN                                   | −0.3 | 18   | V    |
| Pin voltage                                    | VIN – SW, DC                          | −0.3 | 18   | V    |
| Pin voltage                                    | VIN – SW, < 10 ns transient           | −1.5 | 25   | V    |
| Pin voltage                                    | SW – PGND, DC                         | −0.3 | 18   | V    |
| Pin voltage                                    | SW – PGND, < 10 ns transient          | −5   | 21.5 | V    |
| Pin voltage                                    | BOOT – PGND                           | −0.3 | 24   | V    |
| Pin voltage                                    | BOOT – SW                             | −0.3 | 6    | V    |
| Pin voltage                                    | VCC                                   | −0.3 | 6    | V    |
| Pin voltage                                    | EN, PGOOD                             | −0.3 | 6    | V    |
| Pin voltage                                    | MODE                                  | −0.3 | 6    | V    |
| Pin voltage                                    | TRIP, SS/REFIN, FB                    | −0.3 | 3    | V    |
| Pin voltage                                    | VSNS−                                 | −0.3 | 0.3  | V    |
| Sinking current                                | Power Good sinking current capability |      | 10   | mA   |
| Operating junction temperature, T <sub>J</sub> |                                       | −40  | 150  | °C   |
| Storage temperature, T <sub>stg</sub>          |                                       | −55  | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

|                 |   | MIN | NOM | MAX | UNIT |
|-----------------|---|-----|-----|-----|------|
| V <sub>IN</sub> | Input voltage range when VCC pin is powered by a valid external bias      | 2.7 |     | 16  | V    |
| V <sub>IN</sub> | Input voltage range when using the internal VCC LDO                       | 4.0 |     | 16  | V    |
| V <sub>IN</sub> | Minimum VIN before enabling the converter when using the internal VCC LDO | 3.0 |     |     | V    |

## Recommended Operating Conditions (continued)

Over operating junction temperature range (unless otherwise noted)

|                     |                                     | MIN  | NOM | MAX | UNIT |
|---------------------|-------------------------------------|------|-----|-----|------|
| V <sub>OUT</sub>    | Output voltage range                | 0.9  |     | 5.5 | V    |
| Pin voltage         | External VCC bias                   | 3.13 |     | 5.3 | V    |
| Pin voltage         | BOOT to SW                          | –0.1 |     | 5.3 | V    |
| Pin voltage         | EN, PGOOD                           | –0.1 |     | 5.5 | V    |
| Pin voltage         | MODE                                | –0.1 |     | VCC | V    |
| Pin voltage         | TRIP, SS/REFIN, FB                  | –0.1 |     | 1.5 | V    |
| Pin voltage         | VSNS– (refer to AGND)               | –50  |     | 50  | mV   |
| I <sub>PG</sub>     | Power Good input current capability | 0    |     | 10  | mA   |
| I <sub>L-PEAK</sub> | Maximum peak inductor current       |      |     | 25  | A    |
|                     | Minimum R <sub>TRIP</sub>           |      |     | 4.0 | kΩ   |
| T <sub>J</sub>      | Operating junction temperature      | –40  |     | 125 | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPS54JA20        |                               | UNIT |
|-------------------------------|--|------------------|-------------------------------|------|
|                               |  | RWW (QFN, JEDEC) | RWW (QFN, TI EVM)             |      |
|                               |  | 21 PINS          | 21 PINS                       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 49.5             | 26.6                          | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 18.2             | Not applicable <sup>(2)</sup> | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 11.2             | Not applicable <sup>(2)</sup> | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.6              | 0.5                           | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 11.2             | 9.2                           | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) Not applicable to an EVM layout.

## 6.5 Electrical Characteristics

T<sub>J</sub> = –40°C to +125°C, VCC = 3 V (unless otherwise noted)

| PARAMETER              |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT |
|------------------------|--|---|------|------|------|------|
| <b>SUPPLY</b>          |  |   |      |      |      |      |
| I <sub>Q(VIN)</sub>    | VIN quiescent current                    | V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 2 V, V <sub>FB</sub> = V <sub>INTREF</sub> + 50mV (non-switching), no external bias on VCC pin                          |      | 680  | 850  | μA   |
| I <sub>SD(VIN)</sub>   | VIN shutdown supply current              | V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 0 V, no external bias on VCC pin  |      | 9.5  | 20   | μA   |
| I <sub>Q(VCC)</sub>    | VCC quiescent current                    | T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 2 V, V <sub>FB</sub> = V <sub>INTREF</sub> + 50mV (non-switching), 3.3V external bias on VCC pin |      | 680  | 820  | μA   |
| I <sub>VCC</sub>       | VCC external bias current <sup>(1)</sup> | 3.3 V external bias on VCC pin, regular switching. T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 2 V, R <sub>MODE</sub> = 0 Ω to AGND          |      | 7    |      | mA   |
|                        |  | 3.3 V external bias on VCC pin, regular switching. T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 2 V, R <sub>MODE</sub> = 30.1 kΩ to AGND      |      | 9.5  |      | mA   |
|                        |  | 3.3 V external bias on VCC pin, regular switching. T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>EN</sub> = 2 V, R <sub>MODE</sub> = 60.4 kΩ to AGND      |      | 11.5 |      | mA   |
| I <sub>SD(VCC)</sub>   | VCC shutdown current                     | V <sub>EN</sub> = 0 V, V <sub>IN</sub> = 0 V, 3.3 V external bias on VCC pin  |      | 40   | 60   | μA   |
| <b>UVLO</b>            |  |   |      |      |      |      |
| V <sub>INUVLO(R)</sub> | VIN UVLO rising threshold                | VIN rising, VCC = 3.3 V external bias   | 2.1  | 2.4  | 2.7  | V    |
| V <sub>INUVLO(F)</sub> | VIN UVLO falling threshold               | VIN falling, VCC = 3.3 V external bias  | 1.55 | 1.85 | 2.15 | V    |
| <b>ENABLE</b>          |  |   |      |      |      |      |
| V <sub>EN(R)</sub>     | EN voltage rising threshold              | EN rising, enable switching   | 1.17 | 1.22 | 1.27 | V    |

(1) Specified by design. Not production tested.

## Electrical Characteristics (continued)

 $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 3\text{ V}$  (unless otherwise noted)

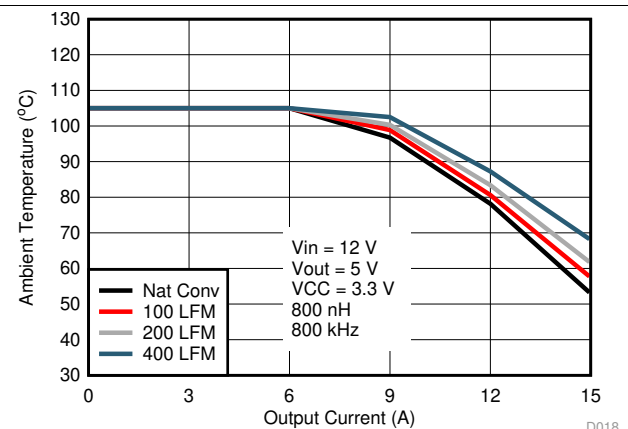
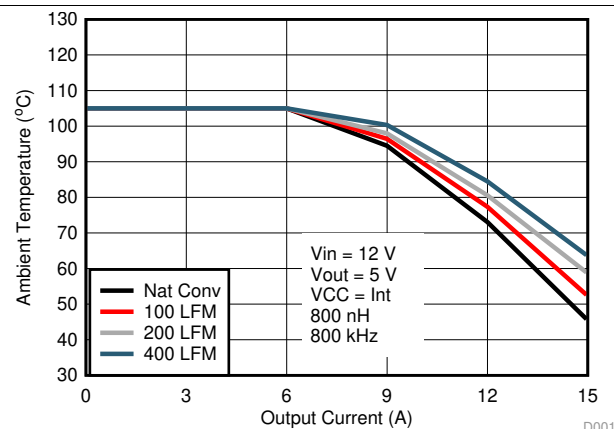
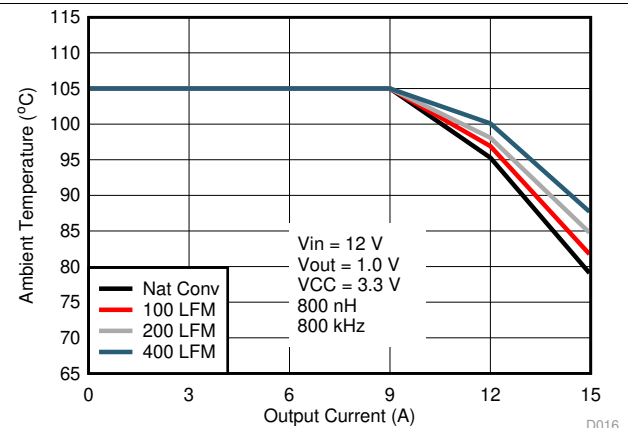
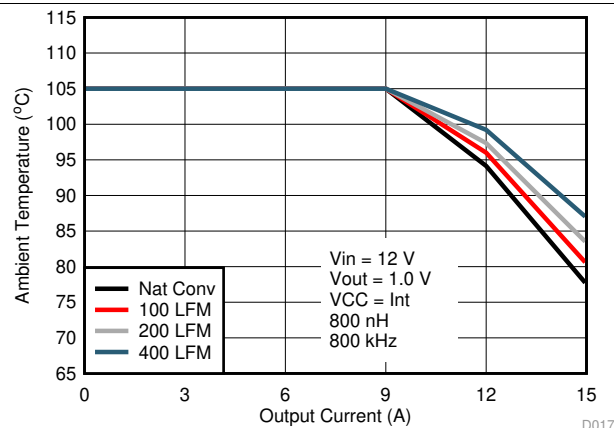
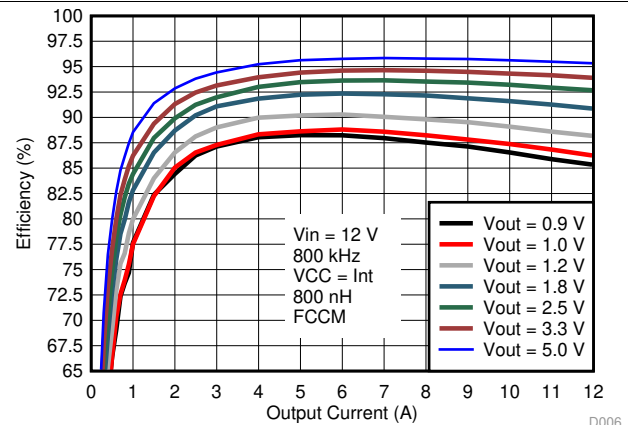
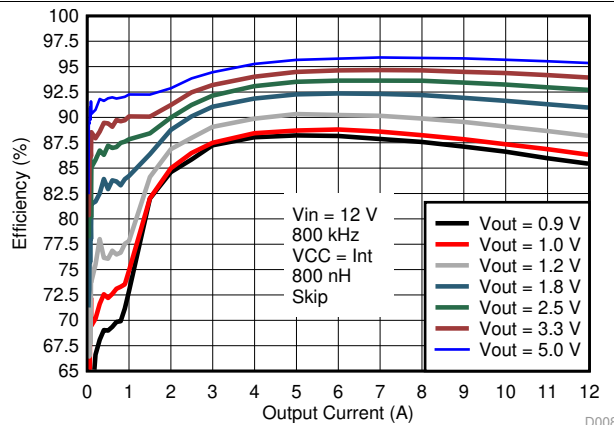
| PARAMETER                  |  | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT |
|----------------------------|--|---|-------|------|------|------|
| V <sub>EN(F)</sub>         | EN voltage falling threshold                   | EN falling, disable switching   | 0.97  | 1.02 | 1.07 | V    |
| V <sub>EN(H)</sub>         | EN voltage hysteresis                          |   |       | 0.2  |      | V    |
| I <sub>EN(LKG)</sub>       | EN input leakage current                       | V <sub>EN</sub> = 3.3 V   |       | 0.5  | 5    | μA   |
|                            | EN internal pull-down resistance               | EN pin to AGND  |       | 6500 |      | kΩ   |
| INTERNAL LDO (VCC PIN)     |  |   |       |      |      |      |
|                            | Internal LDO output voltage                    | V <sub>IN</sub> = 12 V, I <sub>LOAD(VCC)</sub> = 2 mA   | 2.90  | 3.02 | 3.12 | V    |
| V <sub>CC_UVLO(R)</sub>    | VCC UVLO rising threshold                      | VCC rising  | 2.80  | 2.87 | 2.94 | V    |
| V <sub>CC_UVLO(F)</sub>    | VCC UVLO falling threshold                     | VCC falling   | 2.62  | 2.70 | 2.77 |      |
| V <sub>CC_UVLO(H)</sub>    | VCC UVLO hysteresis                            |   |       | 0.17 |      | V    |
|                            | VCC LDO dropout voltage                        | T <sub>J</sub> = 25°C, V <sub>IN</sub> = 3.0 V, I <sub>VCC_LOAD</sub> = 2 mA, non-switching   |       |      | 27   | mV   |
|                            | VCC LDO short-circuit current limit            | V <sub>IN</sub> = 12 V, all temperature   | 52    | 105  | 158  | mA   |
| REFERENCE VOLTAGE          |  |   |       |      |      |      |
|                            | Internal voltage reference range               | T <sub>J</sub> = 0°C to 85°C  | 896   |      | 904  | mV   |
|                            | Internal voltage reference range               | T <sub>J</sub> = −40°C to 125°C   | 891   |      | 909  | mV   |
| I <sub>FB(LKG)</sub>       | Input leakage current into FB pin              | V <sub>FB</sub> = V <sub>INTREF</sub>   |       | 1    | 40   | nA   |
|                            | SS/REFIN-to-FB Accuracy                        | T <sub>J</sub> = -40°C to 125°C, V <sub>SS/REFIN</sub> = 0.9 V, VSNS- = AGND, refer to V <sub>INTREF</sub>  | −0.6% |      | 0.6% |      |
| SWITCHING FREQUENCY        |  |   |       |      |      |      |
| f <sub>SW</sub>            | SW switching frequency, FCCM operation         | T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>OUT</sub> =1.2V, No load, R <sub>MODE</sub> = 0 Ω to AGND   | 0.49  | 0.62 | 0.75 | MHz  |
|                            |  | T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>OUT</sub> =1.2V, No load, R <sub>MODE</sub> = 30.1 kΩ to AGND   | 0.72  | 0.8  | 0.88 |      |
|                            |  | T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>OUT</sub> =1.2V, No load, R <sub>MODE</sub> = 60.4 kΩ to AGND   | 0.84  | 0.97 | 1.1  |      |
| STARTUP                    |  |   |       |      |      |      |
|                            | EN to first switching delay, internal LDO      | The delay from EN goes high to the first SW rising edge with internal LDO configuration. C <sub>VCC</sub> = 2.2 μF. C <sub>SS/REFIN</sub> = 220 nF.                               |       | 0.93 | 2    | ms   |
|                            | EN to first switching delay, external VCC bias | The delay from EN goes high to the first SW rising edge with external VCC bias configuration. VCC bias should reach regulation before EN ramp up. C <sub>SS/REFIN</sub> = 220 nF. |       | 550  | 900  | μs   |
| t <sub>SS</sub>            | Internal fixed Soft-start time                 | V <sub>O</sub> rising from 0 V to 95% of final setpoint, C <sub>SS/REFIN</sub> = 1nF  | 1     | 1.5  |      | ms   |
|                            | SS/REFIN sourcing current                      | V <sub>SS/REFIN</sub> = 0 V   |       | 36   |      | μA   |
|                            | SS/REFIN sinking current                       | V <sub>SS/REFIN</sub> = 1 V   |       | 12   |      | μA   |
| POWER STAGE                |  |   |       |      |      |      |
| R <sub>DS(on)(HS)</sub>    | High-side MOSFET on-resistance                 | T <sub>J</sub> = 25°C, BOOT–SW = 3 V  |       | 10.2 |      | mΩ   |
| R <sub>DS(on)(LS)</sub>    | Low-side MOSFET on-resistance                  | T <sub>J</sub> = 25°C, VCC = 3 V  |       | 3.1  |      | mΩ   |
| t <sub>ON(min)</sub>       | Minimum on-time                                | T <sub>J</sub> = 25°C, VCC = Internal LDO   |       | 70   | 85   | ns   |
| t <sub>OFF(min)</sub>      | Minimum off-time                               | T <sub>J</sub> = 25°C, VCC = Internal LDO, I <sub>O</sub> =1.5A, V <sub>FB</sub> = V <sub>INTREF</sub> − 20 mV, SW falling edge to rising edge                                    |       |      | 220  | ns   |
| BOOT CIRCUIT               |  |   |       |      |      |      |
| I <sub>BOOT(LKG)</sub>     | BOOT leakage current                           | T <sub>J</sub> = 25°C, V <sub>BOOT-SW</sub> = 3.3 V   |       | 35   | 50   | μA   |
| V <sub>BOOT-SW(UV_F)</sub> | BOOT-SW UVLO falling threshold                 | T <sub>J</sub> = 25°C, V <sub>IN</sub> = 12 V, V <sub>BOOT-SW</sub> falling   |       | 2.0  |      | V    |

## Electrical Characteristics (continued)

 $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 3\text{ V}$  (unless otherwise noted)

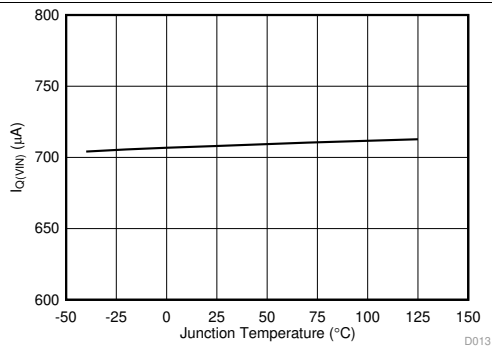
| PARAMETER                     |  | TEST CONDITIONS   | MIN  | TYP    | MAX   | UNIT                |
|-------------------------------|--|---|------|--------|-------|---------------------|
| <b>OVERCURRENT PROTECTION</b> |  |   |      |        |       |                     |
| $R_{TRIP}$                    | TRIP pin resistance range                              |   | 4.0  |        | 14.7  | k $\Omega$          |
|                               | Current limit clamp                                    | Valley current on LS FET, $0\ \Omega \leq R_{TRIP} \leq 3.32\text{ k}\Omega$  | 15.1 | 18.4   | 21.4  | A                   |
| $K_{OCL}$                     | Constant $K_{OCL}$ for $R_{TRIP}$ equation             |   |      | 60000  |       | A $\times$ $\Omega$ |
| $K_{OCL}$                     | Constant $K_{OCL}$ tolerance                           | $4.02\text{ k}\Omega \leq R_{TRIP} \leq 7.5\text{ k}\Omega$   | –15% |        | 18.8% |                     |
| $K_{OCL}$                     | Constant $K_{OCL}$ tolerance                           | $R_{TRIP} = 10\text{ k}\Omega$  | –27% |        | 27%   |                     |
| $I_{NOCL}$                    | Negative current limit threshold                       | All VINs  | –12  | –10    | –8    | A                   |
| $I_{ZC}$                      | Zero-cross detection current threshold, open loop      | $V_{IN} = 12\text{ V}$ , $V_{CC} = \text{Internal LDO}$   |      | 400    |       | mA                  |
| <b>OUTPUT OVP AND UVP</b>     |  |   |      |        |       |                     |
| $V_{OVP}$                     | Output Overvoltage-protection (OVP) threshold voltage  |   | 113% | 116%   | 119%  |                     |
| $t_{OVP(\text{delay})}$       | Output OVP response delay                              | With 100-mV overdrive   |      | 400    |       | ns                  |
| $V_{UVP}$                     | Output Undervoltage-protection (UVP) threshold voltage |   | 77%  | 80%    | 83%   |                     |
| $t_{UVP(\text{delay})}$       | Output UVP filter delay                                |   |      | 68     |       | $\mu\text{s}$       |
| <b>POWER GOOD</b>             |  |   |      |        |       |                     |
| $V_{PGTH}$                    | PGOOD threshold  | FB rising, PGOOD low to high  | 89%  | 92.5%  | 95%   |                     |
|                               |  | FB rising, PGOOD high to low  | 113% | 116%   | 119%  |                     |
|                               |  | FB falling, PGOOD high to low   | 77%  | 80%    | 83%   |                     |
|                               | OOB (Out-Of-Bounds) threshold                          | FB rising, PGOOD stays high   | 103% | 105.5% | 108%  |                     |
| $I_{PG}$                      | PGOOD sink current                                     | $V_{PGOOD} = 0.4\text{ V}$ , $V_{IN} = 12\text{ V}$ , $V_{CC} = \text{Internal LDO}$  |      |        | 10    | mA                  |
| $V_{PG(\text{low})}$          | PGOOD low-level output voltage                         | $I_{PGOOD} = 5.5\text{ mA}$ , $V_{IN} = 12\text{ V}$ , $V_{CC} = \text{Internal LDO}$   |      |        | 400   | mV                  |
| $t_{PGDLY(R)}$                | Delay for PGOOD from low to high                       | During startup only   |      | 1.06   | 1.40  | ms                  |
| $t_{PGDLY(F)}$                | Delay for PGOOD from high to low                       |   |      | 0.5    | 5     | $\mu\text{s}$       |
| $I_{PG(LKG)}$                 | PGOOD leakage current when pulled high                 | $T_J = 25^{\circ}\text{C}$ , $V_{PGOOD} = 3.3\text{ V}$ , $V_{FB} = V_{INTREF}$   |      |        | 5     | $\mu\text{A}$       |
|                               | PGOOD clamp low-level output voltage                   | $V_{IN} = 0\text{ V}$ , $V_{CC} = 0\text{ V}$ , $V_{EN} = 0\text{ V}$ , PGOOD pulled up to 3.3 V through a 100-k $\Omega$ resistor        |      | 710    | 850   | mV                  |
|                               |  | $V_{IN} = 0\text{ V}$ , $V_{CC} = 0\text{ V}$ , $V_{EN} = 0\text{ V}$ , PGOOD pulled up to 3.3 V through a 10-k $\Omega$ resistor         |      | 850    | 1000  | mV                  |
|                               | Minimum VCC for valid PGOOD output                     | $V_{IN} = 0\text{ V}$ , $V_{EN} = 0\text{ V}$ , PGOOD pulled up to 3.3 V through a 100-k $\Omega$ resistor, $V_{PGOOD} \leq 0.4\text{ V}$ |      |        | 1.5   | V                   |
| <b>OUTPUT DISCHARGE</b>       |  |   |      |        |       |                     |
| $R_{Dischg}$                  | Output discharge resistance                            | $V_{IN} = 12\text{ V}$ , $V_{CC} = \text{Internal LDO}$ , $V_{SW} = 0.5\text{ V}$ , power conversion disabled                             |      | 70     |       | $\Omega$            |
| <b>THERMAL SHUTDOWN</b>       |  |   |      |        |       |                     |
| $T_{SDN}$                     | Thermal shutdown threshold <sup>(1)</sup>              | Temperature rising  | 150  | 165    |       | $^{\circ}\text{C}$  |
| $T_{HYST}$                    | Thermal shutdown hysteresis <sup>(1)</sup>             |   |      | 30     |       | $^{\circ}\text{C}$  |

## 6.6 Typical Characteristics

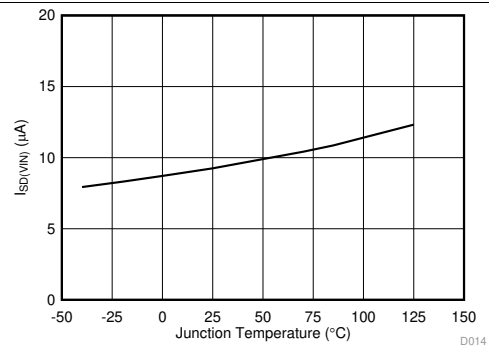




## Typical Characteristics (continued)

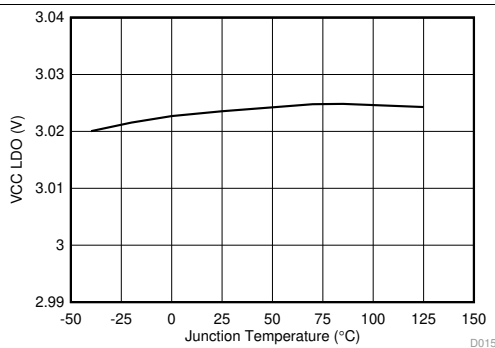


**Figure 7.  $I_{Q(V_{IN})}$  vs Junction Temperature**



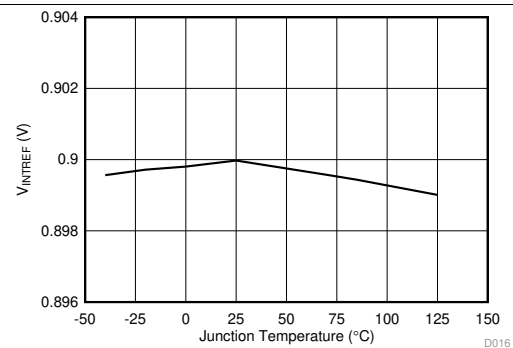
$V_{IN} = 12\text{ V}$   $V_{EN} = 0\text{ V}$  Internal VCC LDO

**Figure 8.  $I_{SD(V_{IN})}$  vs Junction Temperature**



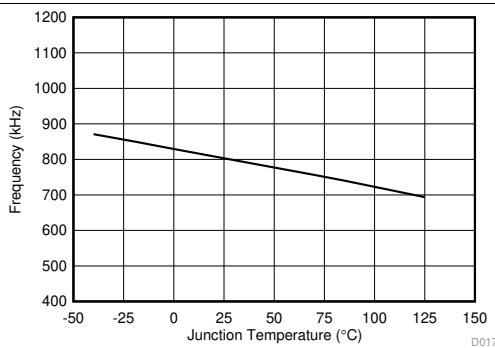
$V_{IN} = 12\text{ V}$   $I_{VCC} = 2\text{ mA}$

**Figure 9. VCC LDO vs Junction Temperature**



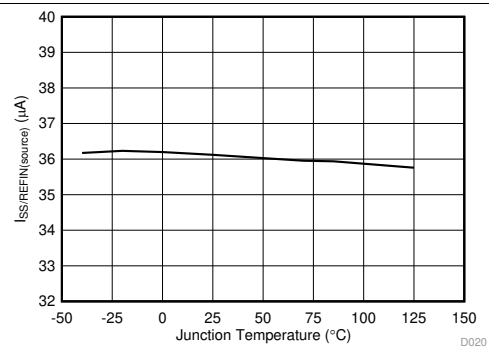
$V_{IN} = 12\text{ V}$

**Figure 10.  $V_{INTREF}$  vs Junction Temperature**



$V_{IN} = 12\text{ V}$

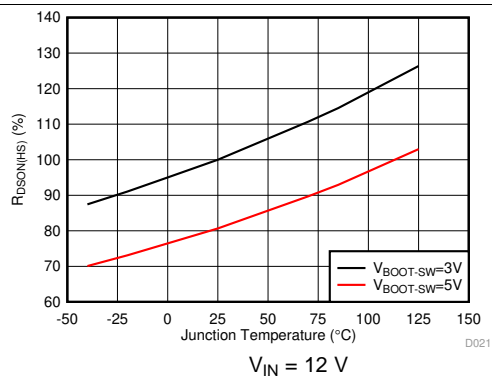
**Figure 11. Switching Frequency vs Junction Temperature**



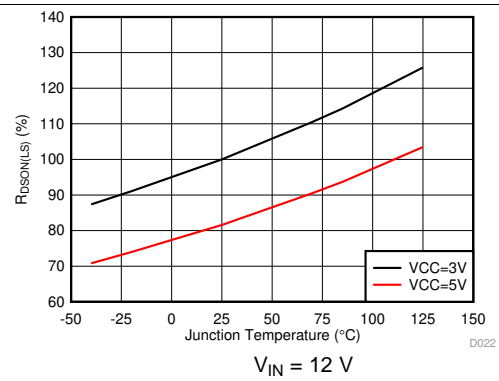
$V_{IN} = 12\text{ V}$

**Figure 12.  $I_{SS(source)}$  vs Junction Temperature**

## Typical Characteristics (continued)



**Figure 13.  $R_{DS(on)(HS)}$  vs Junction Temperature**



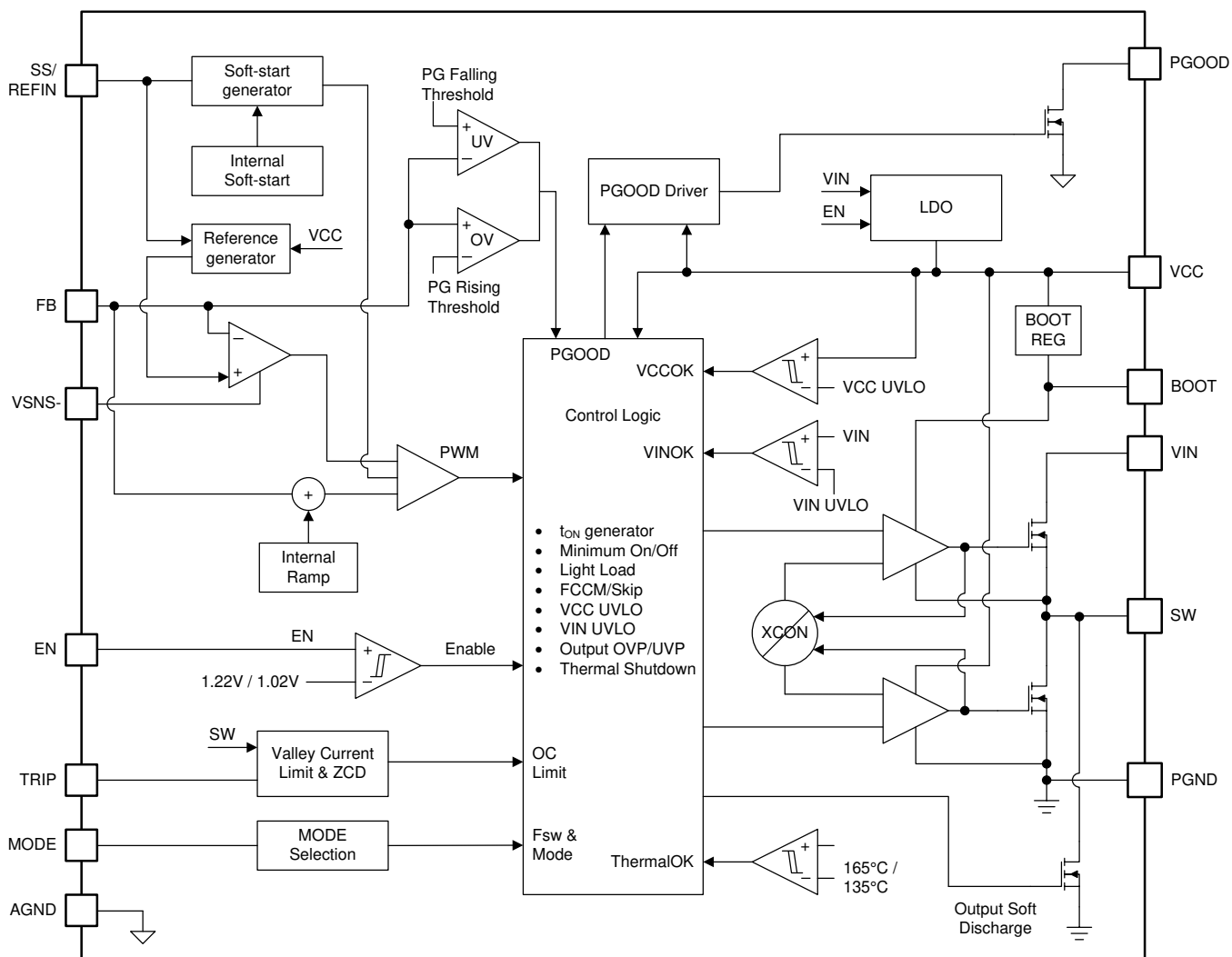
**Figure 14.  $R_{DS(on)(LS)}$  vs Junction Temperature**

## 7 Detailed Description

### 7.1 Overview

The TPS54JA20 device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device suits low output voltage point-of-load applications with 12-A or lower output current in server, storage and similar computing applications. TPS54JA20 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an ideal fashion. The output voltage ranges from 0.9-V to 5.5-V. The conversion input voltage ranges from 2.7-V to 16-V, and the VCC input voltage ranges from 3.13-V to 5.3-V. The D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low external component count. Further advantage of this control scheme is that it supports stable operation with all low ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during load-step transient.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Internal VCC LDO And Using External Bias On VCC Pin

TPS54JA20 has an internal 3-V LDO featuring input from VIN and output to VCC. When the EN voltage rises above enable threshold (typically 1.22-V), the internal LDO is enabled and starts regulating output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.

The VCC pin needs to be bypassed with a 2.2-μF, at least 6.3-V rating ceramic capacitor. An external bias that is above the internal LDO's output voltage can override the internal LDO. This enhances the efficiency of the converter because the VCC current now runs off this external bias instead of the internal linear regulator.

The VCC UVLO circuit monitors the VCC pin voltage and disables the whole converter when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VCC pin are shown below:

- When the external bias is applied on the VCC pin early enough (e.g. before EN signal comes in), the internal LDO will be always forced off and the internal analog circuits will have a stable power supply rail at their power enable.
- (Not recommended) When the external bias is applied on the VCC pin late (e.g. after EN signal comes in), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. It is important to understand that an external discharge path on the VCC pin, which can pull a current higher than the current limit of the internal LDO from the VCC pin, could potentially turn off VCC LDO thereby shutting down the converter output.
- A good power-up sequence is: At least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. For example, a practical power-up sequence is: VIN applied first, then the external bias applied, and then EN signal goes high.

### 7.3.2 Enable

When the EN pin voltage rises above the enable threshold voltage (typically 1.22-V) and VIN rises above the VIN UVLO rising threshold, the device enters its internal power-up sequence. The EN to first switching delay is specified in Startup Section in Electrical Characteristics table.

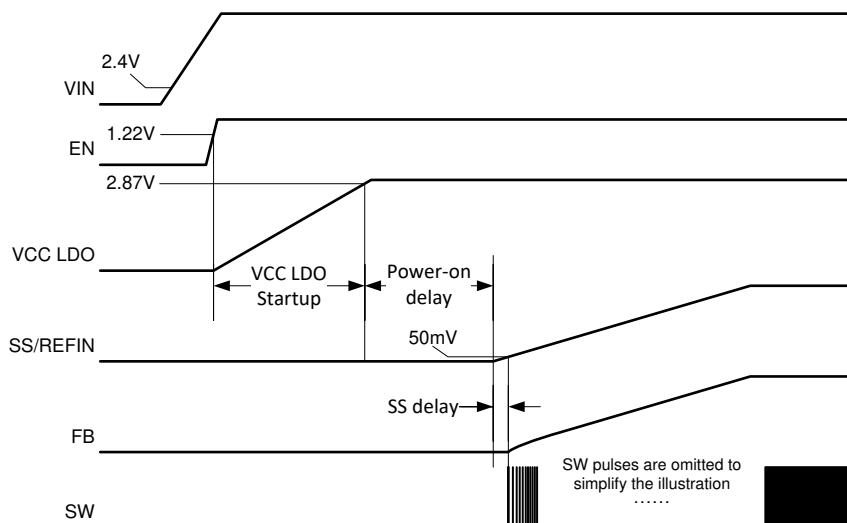
When using the internal VCC LDO, the internal power-up sequence includes 3 sequential steps. During the first period, the VCC voltage is charged up on VCC bypass capacitor by a 11-mA current source. The length of this VCC LDO Startup time varies with the capacitance on VCC pin. However, If VIN voltage ramps up very slowly the VCC LDO output voltage will be limited by VIN voltage level, thus the VCC LDO Startup time could be extended longer. Since the VCC LDO Startup time is relative long the internal  $V_{INTREF}$  build-up happens and finishes during this period. Once the VCC voltage crosses above VCC UVLO rising threshold (typically 2.87-V) the device moves to the second step, power-on delay. The MODE pin setting detection, SS/REFIN pin detection and control loop initialization are finished within this 285-μs delay. Soft-start ramp starts when 285-μs power-on delay finishes. During Soft-start ramp power stage switching doesn't happen until SS/REFIN pin voltage reaches 50-mV. This introduced a SS delay which varies with the external capacitance on SS/REFIN pin.

**Figure 15** shows an example where the VIN UVLO rising threshold is satisfied earlier than the EN rising threshold. In this scenario, the VCC UVLO rising threshold becomes the gating signal to start the internal power-up sequence, and the sequence between VIN and EN doesn't matter.

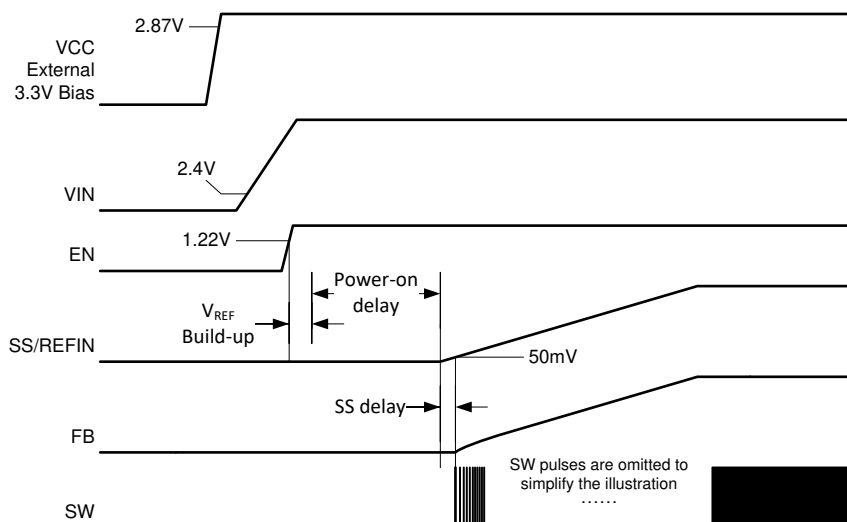
When using an external bias on VCC pin, the internal power-up sequence still includes 3 sequential steps. The first period is much shorter since VCC voltage is built up already. A 100-μs period allows the internal references to start up and reach regulation points. This 100-μs period includes not only the 0.9-V  $V_{INTREF}$  but also all of the other reference voltages for various functions. The device then moves to the second step, power-on delay. The MODE pin setting detection, SS/REFIN pin detection and control loop initialization are finished within this 285-μs delay. Soft-start ramp starts when 285-μs power-on delay finishes. During Soft-start ramp power stage switching doesn't happen until SS/REFIN pin voltage reaches 50-mV. This introduced a SS delay which varies with the external capacitance on SS/REFIN pin.

**Figure 16** shows an example where both VIN UVLO rising threshold and EN rising threshold are satisfied later than VCC UVLO rising threshold. In this scenario, the VIN UVLO rising threshold or EN rising threshold, whoever is satisfied later, becomes the gating signal to start the internal power-up sequence.

## Feature Description (continued)



**Figure 15. Internal Power-up Sequence Using Internal LDO**



**Figure 16. Internal Power-up Sequence Using External Bias**

EN pin has internal filter to avoid unexpected ON or OFF due to small glitches. The time constant of this RC filter is 5- $\mu$ s. For example, when applying 3.3-V voltage source on EN pin which jumps from 0-V to 3.3-V with ideal rising edge, the internal EN signal will reach 2.086-V after 5- $\mu$ s, which is 63.2% of applied 3.3-V voltage level.

A internal pull-down resistor is implemented between EN pin and AGND pin. To avoid impact to EN rising/falling threshold this internal pull-down resistor is set to 6.5M $\Omega$ . With this pull-down resistor, floating EN pin before startup keeps the TPS54JA20 device under disabled state. During nominal operation when the power stage switches, this large internal pull-down resistor may not have enough noise immunity to hold EN pin low.

The recommended operating condition for EN pin is maximum 5.5-V. DO NOT connect EN pin to VIN pin directly.

### 7.3.3 Output Voltage Setting

The output voltage is programmed by the voltage divider resistors,  $R_{FB\_HS}$  and  $R_{FB\_LS}$ . Connect  $R_{FB\_HS}$  between the FB pin and the positive node of the load, and connect  $R_{FB\_LS}$  between the FB pin and VSNS– pin. The recommended  $R_{FB\_LS}$  value is 10-k $\Omega$ , ranging from 1-k $\Omega$  to 20-k $\Omega$ . Determine  $R_{FB\_HS}$  by using [Equation 1](#).

## Feature Description (continued)

$$R_{FB\_HS} = \frac{V_O - V_{INTREF}}{V_{INTREF}} \times R_{FB\_LS} \quad (1)$$

The FB accuracy is determined by two elements. The first element is the accuracy of the internal 900-mV reference which will be applied to SS/REFIN pin unless an external  $V_{REF}$  is applied. The TPS54JA20 device offers  $\pm 0.5\%$   $V_{INTREF}$  accuracy from 0°C to 85°C temperature range, and  $\pm 1.0\%$   $V_{INTREF}$  accuracy from -40°C to 125°C temperature range. The second element is the SS/REFIN-to-FB accuracy which tells how accurately the control loop regulates FB node to SS/REFIN pin. The TPS54JA20 device offers  $\pm 0.6\%$  SS/REFIN-to-FB accuracy from -40°C to 125°C temperature range. For example, when operating from 0°C to 85°C temperature range, the total FB accuracy is  $\pm 1.1\%$  which includes the impact from chip junction temperature and also the variation from part to part.

To improve the overall  $V_{OUT}$  accuracy, using  $\pm 1\%$  accuracy or better resistor for FB voltage divider is highly recommended.

Regardless of remote sensing or single-end sensing connection, FB voltage divider,  $R_{FB\_HS}$  and  $R_{FB\_LS}$ , should be always placed as close as possible to the device.

### 7.3.3.1 Remote Sense

The TPS54JA20 device offers remote sense function through FB and VSNS– pins. Remote sense function compensates a potential voltage drop on the PCB traces thus helps maintain  $V_{OUT}$  tolerance under steady state operation and load transient event. Connecting the FB voltage divider resistors to the remote location allows sensing the output voltage at a remote location. The connections from the FB voltage divider resistors to the remote location should be a pair of PCB traces with at least 12-mil trace width, and should implement Kelvin sensing across a high bypass capacitor of 0.1-μF or higher. The ground connection of the remote sensing signal must be connected to VSNS– pin. The  $V_{OUT}$  connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor,  $R_{FB\_LS}$ , terminated at VSNS– pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines should stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. And it is recommended to shield the pair of remote sensing lines with ground planes above and below.

Single-ended  $V_O$  sensing is often used for local sensing. For this configuration, connect the higher FB resistor,  $R_{FB\_HS}$ , to a high-frequency local bypass capacitor of 0.1-μF or higher, and short VSNS– to AGND.

The recommended VSNS– operating range (refer to AGND pin) is -50-mV to +50-mV.

### 7.3.4 Internal Fixed Soft-Start and External Adjustable Soft-start

TPS54JA20 implements a circuit to allow both internal fixed soft-start and external adjustable soft-start. The internal soft-start time is typically 1.5-ms. The soft-start time can be increased by adding a soft-start (SS) capacitor between SS/REFIN and VSNS– pins. The total SS capacitor value can be determined by [Equation 2](#). The device follows the longer SS ramp among the internal SS time and the SS time determined by the external SS capacitors. The recommended maximum SS capacitor is 1-μF. A minimum 1-nF SS capacitor is required.

The device doesn't require a capacitor from SS/REFIN pin to AGND, thus it is not recommended to place a capacitor from SS/REFIN pin to AGND. If both  $C_{SS/REFIN\text{-to-VSNS-}}$  and  $C_{SS/REFIN\text{-to-AGND}}$  capacitors exist, place  $C_{SS/REFIN\text{-to-VSNS-}}$  more closely with shortest trace back to VSNS– pin.

SS/REFIN pin is discharged internally during the internal power-on delay, to make sure the soft-start ramp always starts from zero.

$$C_{SS}(\text{nF}) = \frac{t_{SS}(\text{ms}) \times 36(\mu\text{A})}{V_{INTREF}(\text{V})} \quad (2)$$

### 7.3.5 External REFIN For Output Voltage Tracking

TPS54JA20 provides an analog input pin (SS/REFIN) to accept an external reference (i.e. a DC voltage source). The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. When an external voltage reference is applied between SS/REFIN pin and VSNS– pin, it acts as the reference voltage thus FB voltage follows this external voltage reference exactly. The same  $\pm 0.6\%$  SS/REFIN-to-FB accuracy from -40°C to 125°C temperature range applies here too.

## Feature Description (continued)

In the middle of internal power-on delay, a detection circuit senses the voltage on SS/REFIN pin to tell whether an active DC voltage source is applied. Before the detection happens SS/REFIN pin tries to discharge any energy on SS/REFIN capacitors through an internal 120-Ω resistor to AGND and this discharge lasts for 125-μs. Then, within a 32-μs window, the detection circuit compares SS/REFIN pin voltage with an internal reference equal to 89% of  $V_{INTREF}$ . This discharge operation ensure a SS capacitor with left-over energy will not be wrongly detected as a voltage reference. If the external voltage reference failed to supply sufficient current and hold voltage level higher than 89% of  $V_{INTREF}$ , the SS/REFIN detection circuit will provide wrong detection result.

If the detection result is that SS/REFIN pin voltage falls below 89% of  $V_{INTREF}$  which tells no external reference is connected, the device firstly uses the internal fixed  $V_{INTREF}$  as the reference for PGOOD threshold,  $V_{OUT}$  OVP and  $V_{OUT}$  UVP threshold. On this configuration, given SS/REFIN pin sees a soft-start ramp on this pin, the slower ramp among the internal fixed soft-start and the external soft-start determines the startup of FB. Once both the internal and external soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2-ms to finish. The external soft-start done signal goes high when FB reaches threshold equal to  $V_{INTREF} - 50\text{mV}$ . The device waits for the PGOOD status transition from low to high, then starts using SS/REFIN pin voltage, instead of the internal  $V_{INTREF}$  as the reference for PGOOD threshold,  $V_{OUT}$  OVP and  $V_{OUT}$  UVP threshold.

If the detection result is that SS/REFIN pin voltage holds higher than 89% of  $V_{INTREF}$  which tells an active DC voltage source is used as an external reference, the device always uses the SS/REFIN pin voltage, instead of the internal  $V_{INTREF}$ , as the reference for PGOOD threshold,  $V_{OUT}$  OVP and  $V_{OUT}$  UVP threshold. On this configuration, since the SS/REFIN pin sees a DC voltage and no soft-start ramp on this pin, the internal fixed soft-start is used for startup. Once the internal soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2-ms to finish because the soft-start ramp goes beyond  $V_{INTREF}$ .

On this external REFIN configuration, applying a stabilized DC external reference to SS/REFIN pin before EN high signal is recommended. During the internal power-on delay, the external reference should be capable to hold the SS/REFIN pin equal to or higher than 89% of  $V_{INTREF}$ , so that the device can correctly detect the external reference and choose the right thresholds for Power Good,  $V_{OUT}$  OVP and  $V_{OUT}$  UVP. After Power Good status transits from low to high, the external reference can be set in a range of 0.5-V to 1.2-V. To overdrive SS/REFIN pin during nominal operation, the external reference has to be able to sink more than 36-μA current if the external reference is lower than the internal  $V_{INTREF}$ , or source more than 12-μA current if the external reference is higher than the internal  $V_{INTREF}$ . When driving SS/REFIN pin by an external reference through a resistor divider, the resistance of the divider should be low enough to provide the sinking, or sourcing current capability.

The configuration of, applying EN high signal first, then applying an external ramp on the SS/REFIN pin as a tracking reference can be achieved, as long as design considerations for Power Good,  $V_{OUT}$  OVP and  $V_{OUT}$  UVP have been taken. Please contact Texas Instruments for detailed information about this configuration.

If the external voltage source must transition up and down between any two voltage levels, the slew rate must be no more than 1-mV/μs.

### 7.3.6 Frequency and Operation Mode Selection

TPS54JA20 provides forced CCM operation for tight output ripple application and auto-skip Eco-mode for high light-load efficiency. TPS54JA20 allows users to select the switching frequency and operation mode by connecting a resistor from MODE pin to AGND pin. [Table 1](#) lists the resistor values for the switching frequency and operation mode selection. TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

The MODE state will be set and latched during the internal power-on delay period. Changing the MODE pin resistance after the power-on delay will not change the status of the device. The internal circuit will set the MODE pin status to 600kHz / Skip-mode if MODE pin is left open during the power-on delay period.

To make sure the internal circuit detects the desired option correctly, DO NOT place any capacitor on MODE pin.



**Table 1. MODE Pin Selection**

| MODE PIN CONNECTIONS  | OPERATION MODE UNDER LIGHT LOAD | SWITCHING FREQUENCY (f <sub>sw</sub> ) (kHz) |
|-----------------------|---------------------------------|--|
| Short to VCC          | Skip-mode                       | 600  |
| 243-kΩ ± 10% to AGND  | Skip-mode                       | 800  |
| 121-kΩ ± 10% to AGND  | Skip-mode                       | 1000   |
| 60.4-kΩ ± 10% to AGND | Forced CCM                      | 1000   |
| 30.1-kΩ ± 10% to AGND | Forced CCM                      | 800  |
| Short to AGND         | Forced CCM                      | 600  |

### 7.3.7 D-CAP3 Control

TPS54JA20 uses D-CAP3 mode control to achieve the fast load transient while maintaining the ease-of-use feature. The D-CAP3 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP3 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop operation. The amplitude of the ramp is determined by V<sub>IN</sub>, V<sub>OUT</sub>, operating frequency and the R-C time-constant of the internal ramp circuit. At different switching frequency settings (see [Table 1](#)), the R-C time-constant varies to maintain relatively constant ramp amplitude. Also, the device utilizes internal circuitry to cancel the dc offset caused by injected ramp, and significantly reduce the dc offset caused by the output ripple voltage, especially under light load condition.

For any control topologies supporting no external compensation design, there is a minimum and/or maximum range of the output filter it can support. The output filter used with TPS54JA20 is a low-pass L-C circuit. This L-C filter has double pole that is described in [Equation 3](#).

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54JA20. The low frequency L-C double pole has a 180-degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase by 90 degrees per decade above the zero frequency.

After identifying the application requirements, the output inductance should be designed so that the inductor peak-to-peak ripple current is approximately between 15% and 40% of the maximum output current.

The inductor and capacitor selected for the output filter must be such that the double pole of [Equation 3](#) is located no higher than 1/30 of operating frequency. Choose very small output capacitance leads to relative high frequency L-C double pole which allows that overall loop gain stays high until the L-C double frequency. Give the zero from the internal ripple generation network is relative high frequency as well, the loop with very small output capacitance may have too high crossover frequency which is not desired. Use [Table 2](#) to help locate the internal zero based on the selected switching frequency.

**Table 2. Locating the Zero**

| SWITCHING FREQUENCIES (f <sub>sw</sub> ) (kHz) | ZERO (f <sub>z</sub> ) LOCATION (kHz) |
|--|---------------------------------------|
| 600  | 84.5                                  |
| 800  | 84.5                                  |
| 1000   | 106                                   |

In general, where reasonable (or smaller) output capacitance is desired, output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation.

For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100 of operating frequency. With this starting point, verify the small signal response on the board using the following one criteria:



- Phase margin at the loop crossover is greater than 50 degrees

The actual maximum output capacitance may go higher as long as phase margin is greater than 50 degrees. However, small signal measurement (bode plot) should be done to confirm the design.

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10- $\mu$ F, X5R and 6.3-V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4- $\mu$ F. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system/applications.

For higher output voltage at or above 2-V, additional phase boost might be required in order to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on-time ( $t_{ON}$ )) setting in a fixed-on-time topology based operation. A feed-forward capacitor placing in parallel with  $R_{FB\_HS}$  is found to be very effective to boost the phase margin at loop crossover. Refer to [Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor](#) for details.

Besides boost the phase, a feed-forward capacitor feeds more  $V_{OUT}$  node information into FB node by the AC coupling. This feed-forward during load transient event enables the control loop a faster response to  $V_{OUT}$  deviation. However, this feed-forward during steady state operation also feeds more  $V_{OUT}$  ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double pulse behavior. To determine the final feed-forward capacitor value, impacts to phase margin, load transient performance and ripple & noise on FB should be all considered. Using Frequency Analysis equipment to measure the crossover frequency and the phase margin is recommended.

### 7.3.8 Low-side FET Zero-Crossing

TPS54JA20 uses a zero-crossing circuit to perform the zero inductor-current detection during skip-mode operation. The function compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. The zero-crossing threshold is set to a positive value to avoid negative inductor current. As a result, the device delivers better light-load efficiency.

### 7.3.9 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on-time of the high-side FET, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on-time of the low-side FET, this current decreases linearly. The average value of the switch current equals to the load current.

The output overcurrent limit (OCL) in TPS54JA20 device is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the on-time of the low-side FET by measuring the low-side FET drain-to-source current. If the measured drain-to-source current of the low-side FET is above the current limit threshold, the low-side FET stays ON until the current level becomes lower than the current limit threshold. This type of behavior reduces the average output current sourced by the device. During an overcurrent condition, the current to the load exceeds the current to the output capacitors. Thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold (80%), the UVP comparator detects it and shuts down the device after a wait time of 68- $\mu$ s. The device remains latched off state (both high-side and low-side FETs are latched off) until a reset of VIN or a re-toggling on EN pin. [Figure 17](#) shows the cycle-by-cycle valley current limit behavior as well as the wait time before the device shuts down.

If an OCL condition happens during start-up the device still has cycle-by-cycle current limit based on low-side valley current. After soft-start is finished, the UV event which is caused by the OC event shuts down the device and enters latch-off mode with a wait time of 68- $\mu$ s.

The resistor,  $R_{TRIP}$  connected from the TRIP pin to AGND sets current limit threshold.  $\pm 1\%$  tolerance resistor is highly recommended because a worse tolerance resistor provides less accurate OCL threshold. [Equation 4](#) calculates the  $R_{TRIP}$  for a given overcurrent limit threshold on the device. To simplify the calculation, use a constant,  $K_{OCL}$ , to replace the value of  $6 \times 10^4$ . [Equation 5](#) calculates the overcurrent limit threshold for a given  $R_{TRIP}$  value. The tolerance of  $K_{OCL}$  is listed in Electrical Characteristics table to help customer to analyze the tolerance of the overcurrent limit threshold.

To protect the device from unexpected connection on TRIP pin, an internal fixed OCL clamp is implemented. This internal OCL clamp limits the maximum valley current on LS FET when TRIP pin has too small resistance to AGND, or is accidentally shorted to ground.

$$R_{\text{TRIP}} = \frac{6 \times 10^4}{I_{\text{OCLIM}} - \frac{1}{2} \times \frac{(V_{\text{IN}} - V_{\text{O}}) \times V_{\text{O}}}{V_{\text{IN}}} \times \frac{1}{L \times f_{\text{SW}}}} = \frac{K_{\text{OCL}}}{I_{\text{OCLIM}} - \frac{1}{2} \times \frac{(V_{\text{IN}} - V_{\text{O}}) \times V_{\text{O}}}{V_{\text{IN}}} \times \frac{1}{L \times f_{\text{SW}}}}$$

where

- $I_{\text{OCLIM}}$  is overcurrent limit threshold for load current in A
- $R_{\text{TRIP}}$  is TRIP resistor value in  $\Omega$
- $K_{\text{OCL}}$  is a constant for the calculation
- $V_{\text{IN}}$  is input voltage value in V
- $V_{\text{O}}$  is output voltage value in V
- $L$  is output inductor value in  $\mu\text{H}$
- $f_{\text{SW}}$  is switching frequency in MHz

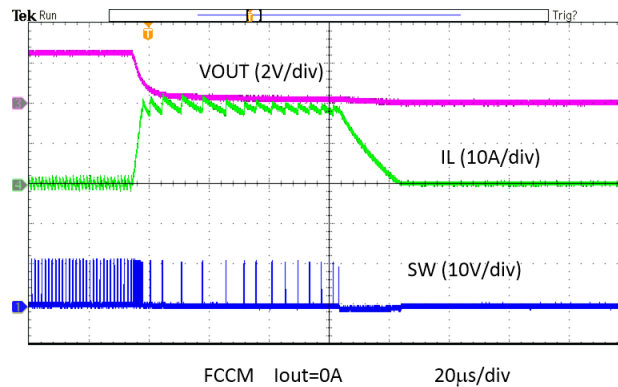
(4)

$$I_{\text{OCLIM}} = \frac{K_{\text{OCL}}}{R_{\text{TRIP}}} + \frac{1}{2} \times \frac{(V_{\text{IN}} - V_{\text{O}}) \times V_{\text{O}}}{V_{\text{IN}}} \times \frac{1}{L \times f_{\text{SW}}}$$

where

- $I_{\text{OCLIM}}$  is overcurrent limit threshold for load current in A
- $R_{\text{TRIP}}$  is TRIP resistor value in  $\Omega$
- $K_{\text{OCL}}$  is a constant for the calculation
- $V_{\text{IN}}$  is input voltage value in V
- $V_{\text{O}}$  is output voltage value in V
- $L$  is output inductor value in  $\mu\text{H}$
- $f_{\text{SW}}$  is switching frequency in MHz

(5)



**Figure 17. Overcurrent Protection**

### 7.3.10 Low-side FET Negative Current Limit

The device has a fixed, cycle-by-cycle negative current limit. Similar with the positive overcurrent limit, the inductor current is monitored during the on-time of the low-side FET. To prevent too large negative current flowing through low-side FET, when the low-side FET detects  $-10\text{-A}$  current (typical threshold), the device turns off low-side FET and then turns on high-side FET for a proper ON-time (determined by  $V_{\text{IN}}/V_{\text{O}}/f_{\text{SW}}$ ). After high-side FET on-time expires, the low-side FET turns on again.

The device should not trigger the  $-10\text{A}$  negative current limit threshold during nominal operation, unless too small inductor value is chosen or the inductor becomes saturated. This negative current limit is utilized to discharge output capacitors during an output OVP or an OOB event. See [Overvoltage and Undervoltage Protection](#) and [Out-Of-Bounds \(OOB\) Operation](#) for details.

### 7.3.11 Power Good

The device has power-good output that indicates high when the converter output is within the target. The power-good output is an open-drain output and must be pulled up to VCC pin or an external voltage source (<5.5-V) through a pullup resistor (typically 30.1-k $\Omega$ ). The recommended power-good pull-up resistor value is 1-k $\Omega$  to 100-k $\Omega$ .

Once both the internal and external soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2-ms to finish. The external soft-start done signal goes high when FB reaches threshold equal to  $V_{INTREF} - 50\text{mV}$ . If the FB voltage drops to 80% of the  $V_{INTREF}$  voltage or exceeds 116% of the  $V_{INTREF}$  voltage, the power-good signal latches low after a 2- $\mu\text{s}$  internal delay. The power-good signal can only be pulled high again after re-toggling EN or a reset of VIN.

If the input supply fails to power up the device, for example VIN and VCC both stays at zero volt, the power-good pin clamps low by itself when this pin is pulled up through an external resistor.

Once VCC voltage level rises above the minimum VCC threshold for valid PGOOD output (maximum 1.5-V), internal power-good circuit is enabled to hold PGOOD pin to the default status. By default, PGOOD is pulled low and this low-level output voltage is no more than 400-mV with 5.5mA sinking current. The power-good function is fully activated after the soft-start operation is completed.

### 7.3.12 Overvoltage and Undervoltage Protection

The device monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage events. When the FB voltage becomes lower than 80% of the  $V_{INTREF}$  voltage, the UVP comparator detects and an internal UVP delay counter begins counting. After the 68- $\mu\text{s}$  UVP delay time, the device latches OFF both high-side and low-side FETs drivers. The UVP function enables after the soft-start period is complete.

When the FB voltage becomes higher than 116% of the  $V_{INTREF}$  voltage, the OVP comparator detects and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit  $I_{NOCL}$ . Upon reaching the negative current limit, the low-side FET is turned off, and the high-side FET is turned on again, for a proper on-time (determined by  $V_{IN}/V_O/f_{SW}$ ). The device operates in this cycle until the output voltage is pulled lower than the UVP threshold voltage for 68- $\mu\text{s}$ . After the 68- $\mu\text{s}$  UVP delay time, both the high-side FET and the low-side FET are latched OFF. The fault is cleared with a reset of VIN or by re-toggling the EN pin.

During the 68- $\mu\text{s}$  UVP delay time, if output voltage becomes higher than UV threshold, thus is not qualified for UV event, the timer will be reset to zero. When the output voltage triggers UV threshold again, the timer of the 68- $\mu\text{s}$  re-starts.

### 7.3.13 Out-Of-Bounds (OOB) Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 5% above the  $V_{INTREF}$  voltage. OOB protection does not trigger an overvoltage fault, so the device is on non-latch mode after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced CCM mode. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus helps the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

### 7.3.14 Output Voltage Discharge

When the device is disabled through EN, it enables the output voltage discharge mode. This mode forces both high-side and low-side FETs to latch off, but turns on the discharge FET, which is connected from SW to PGND, to discharge the output voltage. Once the FB voltage drops below 90-mV, the discharge FET is turned off.

The output voltage discharge mode is activated by any of below fault events:

1. EN pin goes low to disable the converter.
2. Thermal shutdown (OTP) is triggered.
3. VCC UVLO (falling) is triggered.
4. VIN UVLO (falling) is triggered.

### 7.3.15 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the  $V_{CC_{UVLO}}$  falling threshold voltage, the device shuts off. If the VCC voltage increases beyond the  $V_{CC_{UVLO}}$  rising threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

When the VIN pin voltage is lower than the  $V_{IN_{UVLO}}$  falling threshold voltage but VCC pin voltage is still higher than  $V_{CC_{UVLO}}$  rising threshold voltage, the device stops switching and discharges SS/REFIN pin. Once the VIN voltage increases beyond the  $V_{IN_{UVLO}}$  rising threshold voltage, the device re-initiates the soft-start and switches again. VIN UVLO is a non-latch protection.

### 7.3.16 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 165°C), the device stops switching and discharges SS/REFIN pin. When the temperature falls approximately 30°C below the threshold value, the device turns back on with a re-initiated soft-start. Thermal shutdown is a non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 Auto-Skip Eco-mode Light Load Operation

While the MODE pin is pulled to VCC directly or connected to AGND pin through a resistor larger than 121 kΩ, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation  $I_{O(LL)}$  (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in [Equation 6](#).

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- $f_{SW}$  is the switching frequency (6)

Using only ceramic capacitors is recommended for Skip-mode.

### 7.4.2 Forced Continuous-Conduction Mode

When the MODE pin is tied to the AGND pin through a resistor less than 60.4-kΩ, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

### 7.4.3 Powering The Device From A 12-V Bus

The device works well when powering from a 12-V Bus with single Vin configuration. As single VIN configuration, the internal LDO is powered by 12-V Bus and generates 3.0-V output to bias the internal analog circuitry and also powers up the gate drives. The VIN input range under this configuration is 4-V to 16-V for up to 15A load current. The VIN range can be extended down to 3-V if the desired load current is no more than 12A. [Figure 18](#) shows an example for this single VIN configuration.

VIN and EN are the two signals to enable the part. For startup sequence, any sequence between the VIN and EN signals can power the device up correctly.

## Device Functional Modes (continued)

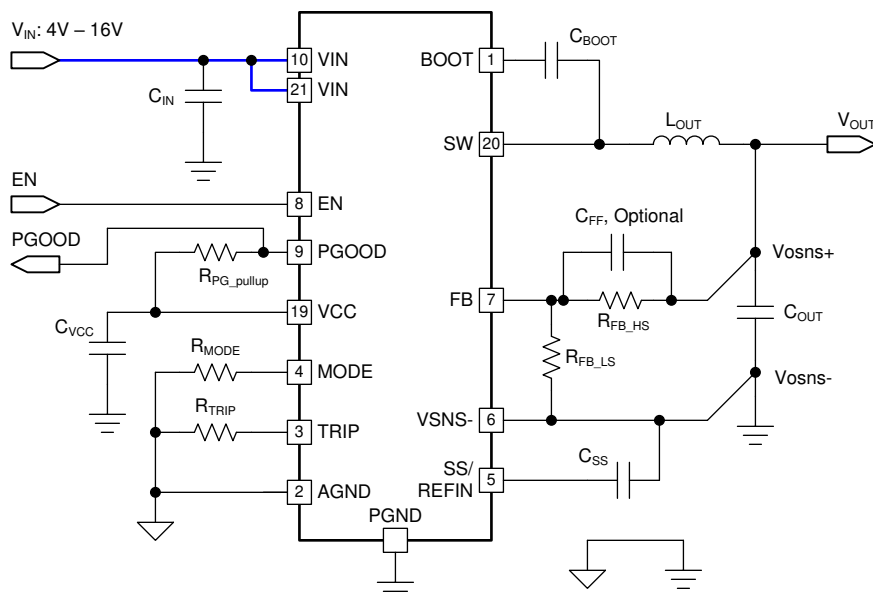


Figure 18. Single VIN Configuration With 12-V Bus

### 7.4.4 Powering The Device From A 3.3-V Bus

The device can also work for up to 15A load current when powering from a 3.3-V Bus with single Vin configuration. To ensure the internal analog circuitry and the gate drives are powered up properly, VCC pin should be shorted to VIN pins with low impedance trace. A trace with at least 24-mil width is recommended. A 2.2- $\mu$ F, at least 6.3-V rating VCC-to-PGND decoupling capacitor is still recommended to be placed as close as possible to VCC pin. Due to the maximum rating limit on VCC pin, the VIN input range under this configuration is 3-V to 5.3-V. The input voltage must stay higher than both VIN UVLO and VCC UVLO, otherwise the device will shut down immediately. Figure 19 shows an example for this single VIN configuration.

VIN and EN are the two signals to enable the part. For start-up sequence, any sequence between the VIN and EN signals can power the device up correctly.

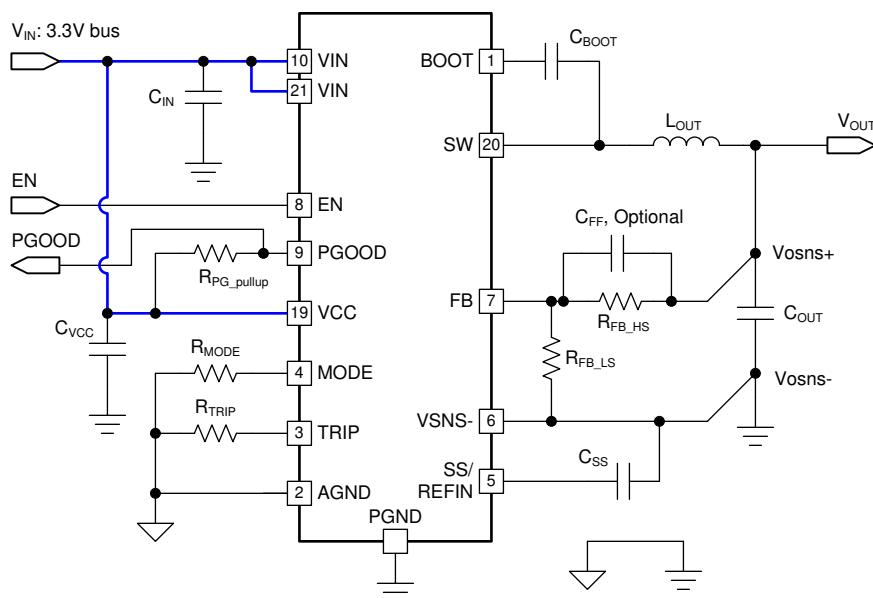


Figure 19. Single VIN Configuration With 3.3-V Bus

## Device Functional Modes (continued)

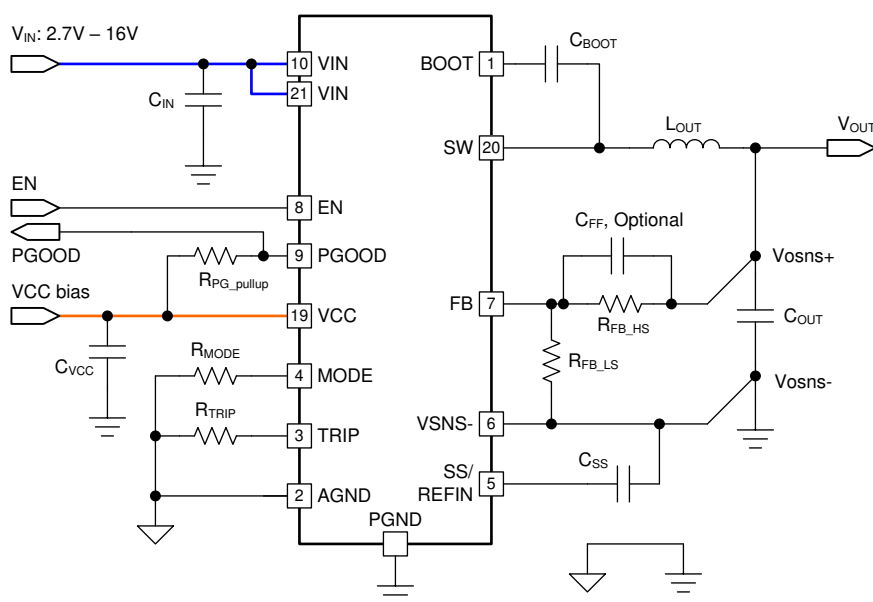
### 7.4.5 Powering The Device From A Split-rail Configuration

When an external bias, which is at a different level from main VIN bus, is applied onto VCC pin the device can be configured to split-rail by utilizing both the main VIN bus and VCC bias. Connecting a valid VCC bias to VCC pin overrides the internal LDO, thus saves power loss on that linear regulator. This configuration helps to improve overall system level efficiency but requires a valid VCC bias. 3.3-V or 5.0-V rail is the common choice as VCC bias. With a stable VCC bias, the VIN input range under this configuration can be as low as 2.7-V and up to 16-V.

The noise of the external bias affects the internal analog circuitry. To ensure a proper operation, a clean, low-noise external bias and good local decoupling capacitor from VCC pin to PGND pin are required. [Figure 20](#) shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and also the operating frequency. For example, by setting the device to skip-mode, the VCC pins draws less and less current from the external bias when the frequency decreases under light load condition. The typical VCC external bias current under FCCM operation is listed in Electrical Characteristics table to help customer to prepare the capacity of the external bias.

Under split rail configuration, VIN, VCC bias and EN are the signals to enable the part. For start-up sequence, it is recommended that at least one of VIN UVLO rising threshold and EN rising threshold is satisfied later than VCC UVLO rising threshold. A practical startup sequence example is: VIN applied first, then the external bias applied, and then EN signal goes high.



**Figure 20. Split Rail Configuration With External VCC Bias**

## 8 Application and Implementation

### NOTE

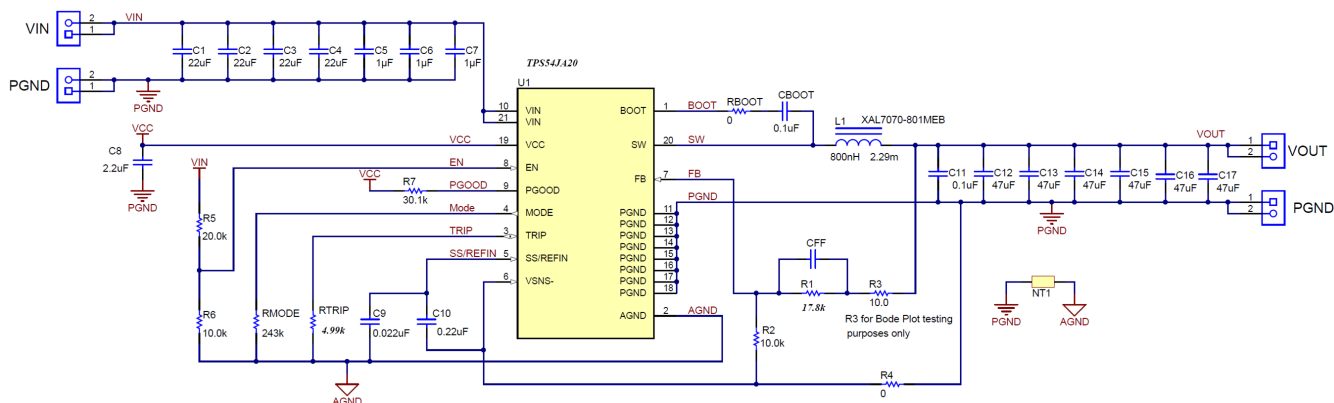
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS54JA20 device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device suits low output voltage point-of-load applications with 12-A or lower output current in server, storage and similar computing applications. The TPS54JA20 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an ideal fashion. The output voltage ranges from 0.9-V to 5.5-V. The conversion input voltage ranges from 2.7-V to 16-V, and the VCC input voltage ranges from 3.13-V to 5.3-V. The D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require an external phase-compensation network, which makes the device easy-to-use and also allows for a low external component count. Another advantage of this control scheme is that it supports stable operation with all low ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during a load-step transient.

### 8.2 Typical Application

The schematic shows a typical application for TPS54JA20. This example describes the design procedure of converting an input voltage range of 4-V to 16-V down to 2.5-V with a maximum output current of 12 A.



**Figure 21. Application Circuit Diagram**



## Typical Application (continued)

### 8.2.1 Design Requirements

This design uses the parameters listed in [Table 3](#).

**Table 3. Design Example Specifications**

| DESIGN PARAMETER   | CONDITION  | MIN | TYP       | MAX | UNIT             |
|--|--|-----|-----------|-----|------------------|
| V <sub>IN</sub> Voltage range  |  | 4   | 12        | 16  | V                |
| V <sub>OUT</sub> Output voltage  |  |     | 2.5       |     | V                |
| I <sub>LOAD</sub> Output load current                                      |  |     |           | 12  | A                |
| V <sub>RIPPLE</sub> Output voltage ripple                                  | V <sub>IN</sub> = 12 V, I <sub>OUT</sub> = 12 A      |     | 10        |     | mV <sub>PP</sub> |
| V <sub>TRANS</sub> Output voltage undershoot and overshoot after load step | I <sub>OUT</sub> = 25% to 75% step, 2 A/μs slew rate |     | 50        |     | mV               |
| I <sub>OVER</sub> Output overcurrent                                       |  |     | 12        |     | A                |
| t <sub>SS</sub> Soft-start time  |  |     | 5.5       |     | ms               |
| f <sub>SW</sub> Switching frequency  |  |     | 0.8       |     | MHz              |
| Operating mode   |  |     | Skip-mode |     |                  |
| T <sub>A</sub> Operating temperature                                       |  |     | 25        |     | °C               |

### 8.2.2 Detailed Design Procedure

The external component selection is a simple process using D-CAP3 mode. Select the external components using the following steps.

#### 8.2.2.1 Output Voltage Setting Point

The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in [Equation 7](#). Connect R1 between the FB pin and the output, and connect R2 between the FB pin and VSNS–. The recommended R2 value is 10 kΩ, but it can also be set to another value between the range of 1 kΩ to 20 kΩ. Determine R1 for TPS54JA20 by using [Equation 7](#).

$$R1 = \frac{V_{OUT} - V_{INTREF}}{V_{INTREF}} \times R2 = \frac{2.5V - 0.9V}{0.9V} \times 10k\Omega = 17.8k\Omega \quad (7)$$

#### 8.2.2.2 Choose the Switching Frequency and the Operation Mode

The switching frequency and operation mode are configured by the resistor on MODE pin. Select one of three switching frequencies: 600-kHz, 800-kHz, or 1-MHz. Refer to [Table 1](#) for the relationship between the switching frequency, operation mode and R<sub>MODE</sub>.

Switching frequency selection is a tradeoff between higher efficiency and smaller system solution size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, a 243-kΩ resistor is chosen for MODE pin to set the switching frequency to 0.8-MHz and set operation mode as Skip-mode.

When selecting the switching frequency of a buck converter, the minimum on-time and minimum off-time must be considered. [Equation 8](#) calculates the maximum f<sub>SW</sub> before being limited by the minimum on-time. When hitting the minimum on-time limits of a converter with D-CAP3 control, the effective switching frequency will change to keep the output voltage regulated. This calculation ignores resistive drops in the converter to give a worst case estimation.

$$f_{SW}(\max) = \frac{V_{OUT}}{V_{IN}(\max)} \times \frac{1}{t_{ON\_MIN}(\max)} = \frac{2.5V}{16V} \times \frac{1}{85ns} = 1838kHz \quad (8)$$



**Equation 9** calculates the maximum  $f_{SW}$  before being limited by the minimum off-time. When hitting the minimum off-time limits of a converter with D-CAP3 control, the operating duty cycle will max out and the output voltage will begin to drop with the input voltage. This equation requires the DC resistance of the inductor,  $R_{DCR}$ , selected in the following step so this preliminary calculation assumes a resistance of 2.2 mΩ. If operating near the maximum  $f_{SW}$  limited by the minimum off-time, the variation in resistance across temperature must be considered when using **Equation 9**. The selected  $f_{SW}$  of 800 kHz is below the two calculated maximum values.

$$f_{SW}(\max) = \frac{V_{IN}(\min) - V_{OUT} - I_{OUT}(\max) \times (R_{DCR} + R_{DS(ON)_{HS}})}{t_{OFF\_MIN}(\max) \times (V_{IN}(\min) - I_{OUT}(\max) \times (R_{DS(ON)_{HS}} - R_{DS(ON)_{LS}}))}$$

$$f_{SW}(\max) = \frac{8\text{ V} - 2.5\text{ V} - 12\text{ A} \times (2.2\text{ m}\Omega + 10.2\text{ m}\Omega)}{220\text{ ns} \times (8\text{ V} - 12\text{ A} \times (10.2\text{ m}\Omega - 3.1\text{ m}\Omega))} = 3020\text{ kHz} \quad (9)$$

### 8.2.2.3 Choose the Inductor

To calculate the value of the output inductor ( $L_{OUT}$ ), use **Equation 10**. The output capacitor filters the inductor-ripple current ( $I_{IND(ripple)}$ ). Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. On the other hand, larger ripple current increases output ripple voltage, but improves signal-to-noise ratio and helps to stabilize operation. Generally speaking, the inductance value should set the ripple current at approximately 15% to 40% of the maximum output current for a balanced performance.

For this design, the inductor-ripple current is set to 30% of 12-A output current. With 0.8-MHz switching frequency, 16-V as maximum  $V_{IN}$ , and 2.5-V as the output voltage, the **Equation 10** calculated inductance is 0.732-μH. A nearest standard value of 0.80-μH is chosen.

$$L = \frac{(V_{IN}(\max) - V_{OUT}) \times V_{OUT}}{I_{RIPPLE} \times V_{IN}(\max) \times f_{SW}} = \frac{(16\text{ V} - 2.5\text{ V}) \times 2.5\text{ V}}{0.3 \times 12\text{ A} \times 16\text{ V} \times 800\text{ kHz}} = 0.732\text{ }\mu\text{H} \quad (10)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using **Equation 12**. For this design, by selecting 4.99-kΩ as the  $R_{TRIP}$ ,  $I_{OC(valley)}$  is set to 12.8-A, thus peak inductor current under maximum  $V_{IN}$  is calculated as 14.06-A.

$$I_{RIPPLE} = \frac{(V_{IN}(\max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(\max) \times f_{SW}} = \frac{(16\text{ V} - 2.5\text{ V}) \times 2.5\text{ V}}{0.8\text{ }\mu\text{H} \times 16\text{ V} \times 800\text{ kHz}} = 4.12\text{ A} \quad (11)$$

$$I_{L(PEAK)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 12\text{ A} + \frac{4.12\text{ A}}{2} = 14.06\text{ A} \quad (12)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}} = \sqrt{12\text{ A}^2 + \frac{4.12\text{ A}^2}{12}} = 12.06\text{ A} \quad (13)$$

The selected inductance is a XAL7070-801MEB. This has a saturation current rating of 37.8 A, RMS current rating of 20.8-A and a DCR of 2.29 mΩ max. This inductor was selected for its low DCR to get high efficiency.

### 8.2.2.4 Set the Current Limit (TRIP)

The  $R_{TRIP}$  resistor sets the valley current limit. **Equation 14** calculates the recommended current limit target. This includes the tolerance of the inductor and a factor of 0.85 for the tolerance of the current limit threshold. **Equation 15** calculates the  $R_{TRIP}$  resistor to set the current limit. The typical valley current limit target is 12.8 A and the closest standard value for  $R_{TRIP}$  is

$$I_{LIM\_VALLEY} = \left( I_{OUT} - \frac{1}{2} \times \frac{(V_{IN}(\min) - V_{OUT}) \times V_{OUT}}{L \times (1 + L_{TOL}) \times V_{IN}(\min) \times f_{SW}} \right) \times \frac{1}{0.85}$$

$$I_{LIM\_VALLEY} = \left( 12\text{ A} - \frac{1}{2} \times \frac{(8\text{ V} - 2.5\text{ V}) \times 2.5\text{ V}}{0.8\text{ }\mu\text{H} \times (1 + 0.2) \times 8\text{ V} \times 800\text{ kHz}} \right) \times \frac{1}{0.85} = 12.8\text{ A} \quad (14)$$

$$R_{TRIP} = \frac{60000}{I_{LIM\_VALLEY}} = \frac{60000}{12\text{ A}} = 5.0\text{ k}\Omega \quad (15)$$

With the current limit set, Equation 16 calculates the typical maximum output current at current limit. Equation 17 calculates the typical peak current at current limit. As mentioned in Choose the Inductor, the saturation behavior of the inductor at the peak current during current limit must be considered. For worst case calculations, the tolerance of the inductance and the current limit must be included.

$$I_{OUT\_LIM}(\min) = I_{LIM\_VALLEY} + \frac{1}{2} \times \frac{(V_{IN}(\min) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(\min) \times f_{SW}} = 12\text{ A} + \frac{1}{2} \times \frac{(8\text{ V} - 2.5\text{ V}) \times 2.5\text{ V}}{0.8\text{ }\mu\text{H} \times 8\text{ V} \times 800\text{ kHz}} = 13.14\text{ A} \quad (16)$$

$$I_{L(PEAK)} = I_{LIM\_VALLEY} + \frac{(V_{IN}(\max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(\max) \times f_{SW}} = 12\text{ A} + \frac{(16\text{ V} - 2.5\text{ V}) \times 2.5\text{ V}}{0.8\text{ }\mu\text{H} \times 16\text{ V} \times 800\text{ kHz}} = 14.08\text{ A} \quad (17)$$

### 8.2.2.5 Choose the Output Capacitor

There are three considerations for selecting the value of the output capacitor.

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

First the minimum output capacitance should be calculated based on these 3 requirements. Equation 18 calculates the minimum capacitance to keep the LC double pole below 1/30th the  $f_{SW}$  in order to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero. Equation 19 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 10-mV. This calculation is for CCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors.

$$C_{OUT\_STABILITY} > \left( \frac{30}{2\pi \times f_{SW}} \right)^2 \times \frac{1}{L} = \left( \frac{30}{2\pi \times 800\text{ kHz}} \right)^2 \times \frac{1}{0.8\text{ }\mu\text{H}} = 44.5\text{ }\mu\text{F} \quad (18)$$

$$C_{OUT\_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times f_{SW}} = \frac{4.12\text{ A}}{8 \times 10\text{ mV} \times 800\text{ kHz}} = 64.4\text{ }\mu\text{F} \quad (19)$$

Equation 20 and Equation 21 calculate the minimum capacitance to meet the transient response requirement of 50-mV with a 6-A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step.

$$C_{OUT\_UNDERSHOOT} > \frac{L \times I_{STEP}^2 \times \left( \frac{V_{OUT}}{V_{IN}(\min) \times f_{SW}} + t_{OFF\_MIN}(\max) \right)}{2 \times V_{TRANS} \times V_{OUT} \times \left( \frac{V_{IN}(\min) - V_{OUT}}{V_{IN}(\min) \times f_{SW}} - t_{OFF\_MIN}(\max) \right)} \quad (20)$$

$$C_{OUT\_UNDERSHOOT} > \frac{0.8\text{ }\mu\text{H} \times 6\text{ A}^2 \times \left( \frac{2.5\text{ V}}{8\text{ V} \times 800\text{ kHz}} + 220\text{ ns} \right)}{2 \times 50\text{ mV} \times 2.5\text{ V} \times \left( \frac{8\text{ V} - 2.5\text{ V}}{8\text{ V} \times 800\text{ kHz}} - 220\text{ ns} \right)} = 110\text{ }\mu\text{F}$$

$$C_{OUT\_OVERSHOOT} > \frac{L \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{0.8\text{ }\mu\text{H} \times 6\text{ A}^2}{2 \times 50\text{ mV} \times 2.5\text{ V}} = 115.2\text{ }\mu\text{F} \quad (21)$$

The output capacitance needed to meet the overshoot requirement is the highest value so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance and Equation 22 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the  $f_{SW}$ . It may be possible to use more output capacitance but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 6 x 47  $\mu$ F 6.3V eramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to 60% their nominal value giving an effective total capacitance of 169.2  $\mu$ F. This effective capacitance meets the minimum and maximum requirements.

$$C_{OUT\_STABILITY} < \left( \frac{50}{\pi \times f_{SW}} \right)^2 \times \frac{1}{L} = \left( \frac{50}{\pi \times 800 \text{ kHz}} \right)^2 \times \frac{1}{0.8 \mu\text{H}} = 494 \mu\text{F} \quad (22)$$

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If using non ceramic capacitors, as a starting point, the ESR should be below the values calculated in Equation 23 to meet the ripple requirement and Equation 24 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors should be used to determine if the ripple and transient requirements can be met.

$$R_{ESR\_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{10 \text{ mV}}{4.1 \text{ A}} = 2.5 \text{ m}\Omega \quad (23)$$

$$R_{ESR\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{50 \text{ mV}}{6 \text{ A}} = 8.3 \text{ m}\Omega \quad (24)$$

### 8.2.2.6 Choose the Input Capacitors ( $C_{IN}$ )

The device requires input bypass capacitors between the VIN and PGND pins to bypass the power-stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout will allow. At least 10- $\mu$ F of ceramic capacitance and 1- $\mu$ F high frequency ceramic bypass capacitors are required. A 1- $\mu$ F, 16-V X6S size 0402 ceramic capacitor on VIN pin 21 is required. A 1- $\mu$ F, 16-V X6S ceramic capacitor on VIN pin 10 is required. A 1- $\mu$ F 16-V X6S ceramic capacitor on bottom layer is recommended for high current applications. The high frequency bypass capacitor minimizes high frequency voltage overshoot across the power-stage. The ceramic capacitors must be high-quality dielectric of X6S or better for their high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this, more bulk capacitance may be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

The input capacitance required to meet a specific input ripple target can be calculated with Equation 25. A recommended target input voltage ripple is 5% the minimum input voltage, 400-mV in this example. The calculated input capacitance is 8.06  $\mu$ F and the minimum input capacitance of 10  $\mu$ F exceeds this. This example meets these two requirements with 4 x 22  $\mu$ F ceramic capacitors.

$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left( 1 - \frac{V_{OUT}}{V_{IN}(\min)} \right)}{f_{SW} \times V_{IN}(\min) \times V_{IN\_RIPPLE}} = \frac{2.5 \text{ V} \times 12 \text{ A} \times \left( 1 - \frac{2.5}{8} \right)}{800 \text{ kHz} \times 8 \text{ V} \times 400 \text{ mV}} = 8.06 \mu\text{F} \quad (25)$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. The input RMS current the input capacitors must support is calculated by Equation 26 and is 5.57 A in this example. The ceramic input capacitors have a current rating greater than this.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}(\min)} \times \left( \frac{(V_{IN}(\min) - V_{OUT})}{V_{IN}(\min)} \times I_{OUT}^2 + \frac{I_{ripple}^2}{12} \right)} =$$

$$I_{CIN(RMS)} = \sqrt{\frac{2.5 \text{ V}}{8 \text{ V}} \times \left( \frac{(8 \text{ V} - 2.5 \text{ V})}{8 \text{ V}} \times 12^2 + \frac{4.12^2}{12} \right)} = 5.57 \text{ A} \quad (26)$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, the selection process in this [article](#) is recommended.

### 8.2.2.7 Soft Start Capacitor (SS/REFIN Pin)

The capacitor placed on the SS/REFIN pin can be used to extend the soft start time past the internal 1.5-ms soft start. This example uses a 5.5-ms soft start time and the required external capacitance can be calculated with [Equation 27](#). In this example a 220-nF capacitor is used.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} = \frac{36 \mu A \times 5.5 \text{ ms}}{0.9 \text{ V}} = 220 \text{ nF} \quad (27)$$

A minimum capacitor value of 1 nF is required at the SS/REFIN pin. The SS/REFIN capacitor must use the VSNS– pin for its ground.

### 8.2.2.8 EN Pin Resistor Divider

A resistor divider on the EN pin can be used to increase the input voltage the converter begins its startup sequence. To set the start voltage, first select the bottom resistor ( $R_{EN\_B}$ ). The recommended value is between 1-k $\Omega$  and 100-k $\Omega$ . There is an internal pull down resistance with a nominal value of 6 M $\Omega$  and this must be included for the most accurate calculations. This is especially important when the bottom resistor is a higher value, near 100-k $\Omega$ . This example uses a 10-k $\Omega$  resistor and this combined with the internal resistance in parallel results in an equivalent bottom resistance of 9.98 k $\Omega$ . The top resistor value for the target start voltage is calculated with [Equation 28](#). In this example, the nearest standard value of 20-k $\Omega$  is selected for  $R_{EN\_T}$ . When selecting a start voltage in a wide input range application, be cautious that the EN pin absolute maximum voltage of 6-V is not exceeded.

$$R_{EN\_T} = \frac{R_{EN\_B} \times V_{START}}{V_{ENH}} - R_{EN\_B} = \frac{10 \text{ k}\Omega \times 3.7 \text{ V}}{1.22 \text{ V}} - 10 \text{ k}\Omega = 20 \text{ k}\Omega \quad (28)$$

The start and stop voltages with the selected EN resistor divider can be calculated with [Equation 27](#) and [Equation 30](#).

$$V_{START} = V_{ENH} \times \frac{R_{EN\_B} + R_{EN\_T}}{R_{EN\_B}} = 1.22 \text{ V} \times \frac{10 \text{ k}\Omega + 20 \text{ k}\Omega}{10 \text{ k}\Omega} = 3.66 \text{ V} \quad (29)$$

$$V_{STOP} = V_{ENL} \times \frac{R_{EN\_B} + R_{EN\_T}}{R_{EN\_B}} = 1.02 \text{ V} \times \frac{10 \text{ k}\Omega + 20 \text{ k}\Omega}{10 \text{ k}\Omega} = 3.06 \text{ V} \quad (30)$$

### 8.2.2.9 VCC Bypass Capacitor

At a minimum, a 2.2- $\mu$ F, at least 6.3V rating, X5R ceramic bypass capacitor is needed on VCC pin located as close to the pin as the layout will allow.

### 8.2.2.10 BOOT Capacitor

At a minimum, a 0.1- $\mu$ F 10V X5R ceramic bypass capacitor is needed between the BOOT and SW pins located as close to the pin as the layout will allow. It is good practice to use a 0- $\Omega$  resistor in series with BOOT capacitor.

### 8.2.2.11 PGOOD Pull-up Resistor

The PGOOD pin is open-drain so a pull-up resistor is required when using this pin. The recommended value is between 1-k $\Omega$  and 100-k $\Omega$ .

## 8.2.3 Application Curves

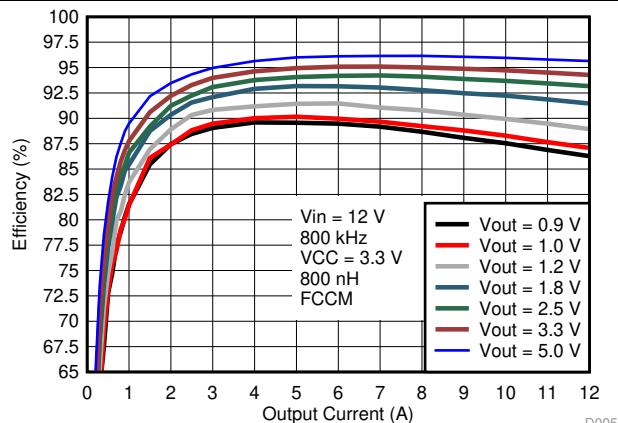


Figure 22. Efficiency vs Output Current, VCC = 3.3V  
External VCC Bias

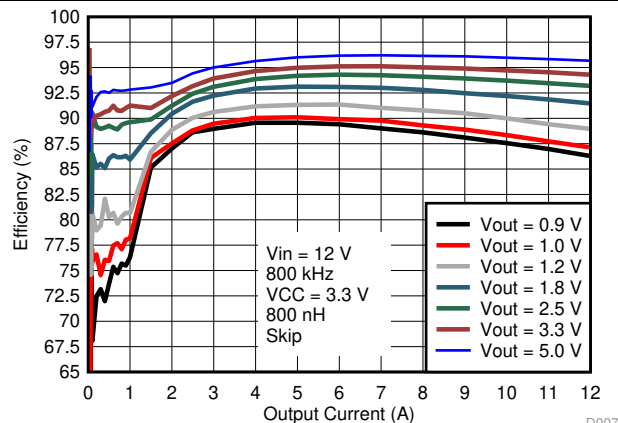


Figure 23. Efficiency vs Output Current, VCC = 3.3V  
External VCC Bias

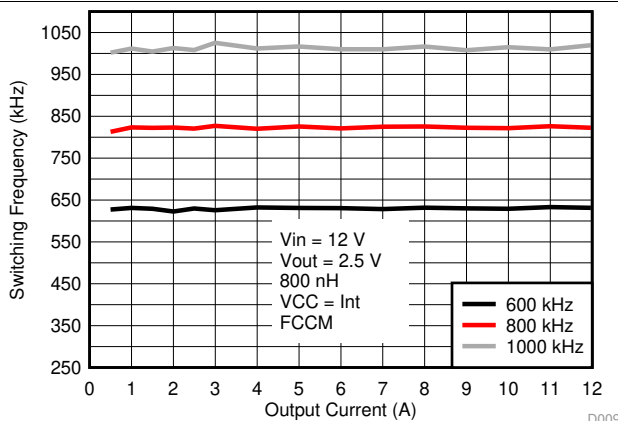


Figure 24. Switching Frequency vs Output Current

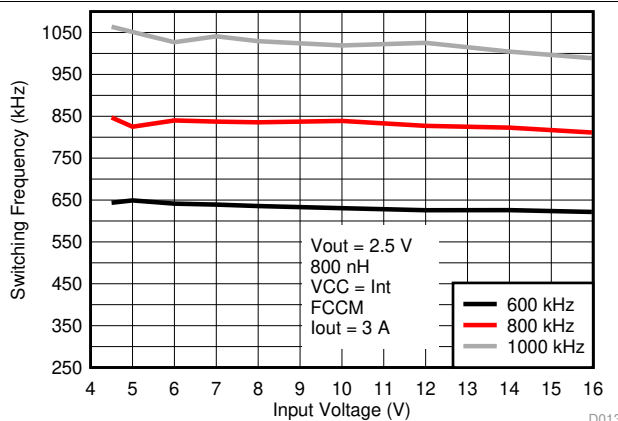


Figure 25. Switching Frequency vs Input Voltage

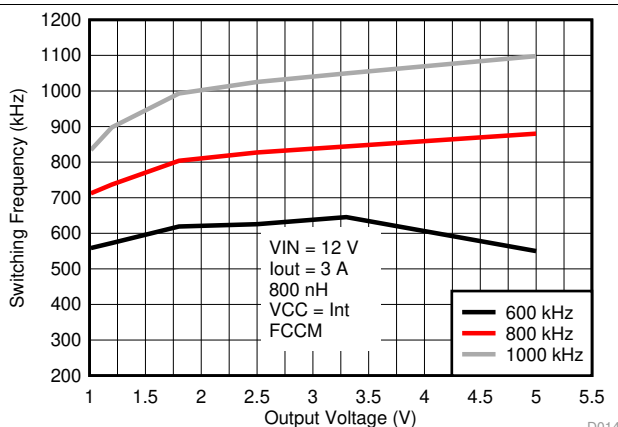


Figure 26. Switching Frequency vs Output Voltage

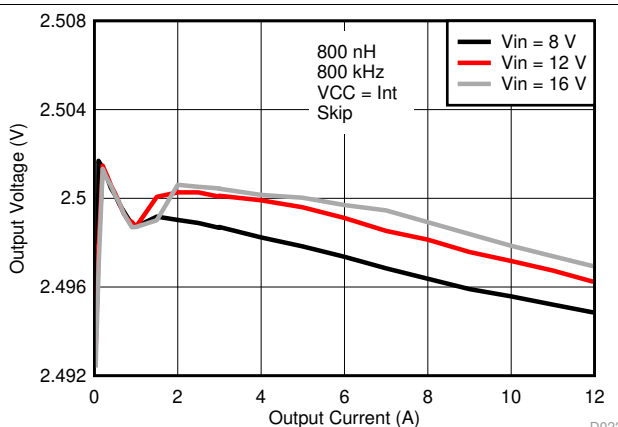


Figure 27. Output Voltage vs Output Current

# TPS54JA20

SNVSB02B – MARCH 2020 – REVISED JUNE 2020

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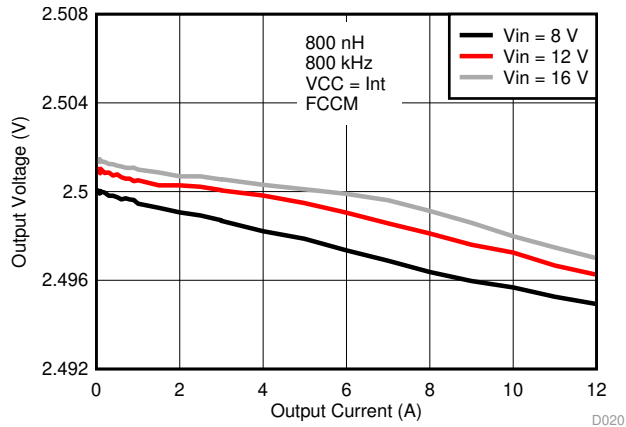


Figure 28. Output Voltage vs Output Current

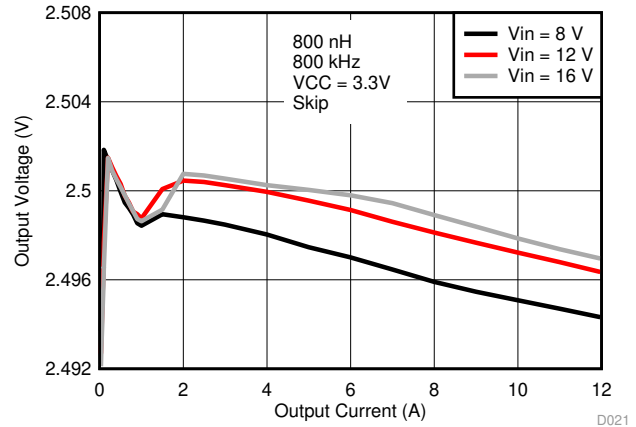


Figure 29. Output Voltage vs Output Current, VCC = 3.3V External Bias

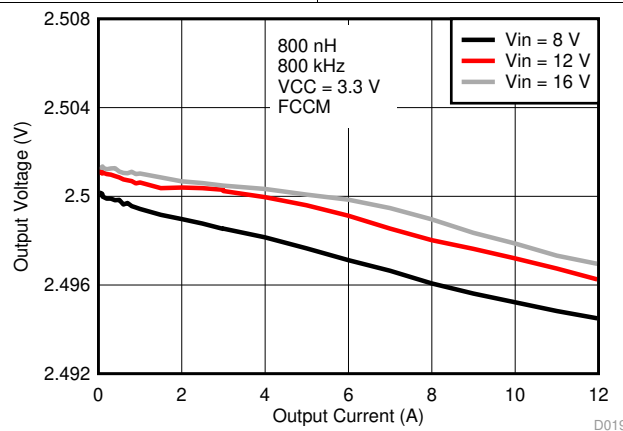


Figure 30. Output Voltage vs Output Current, VCC = 3.3V External Bias

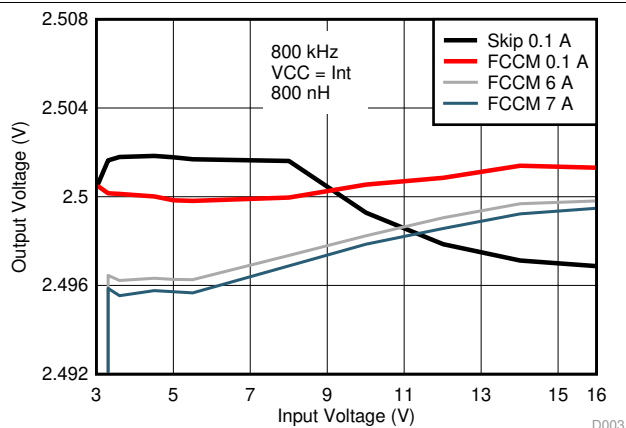


Figure 31. Output Voltage vs Input Voltage VCC = Int

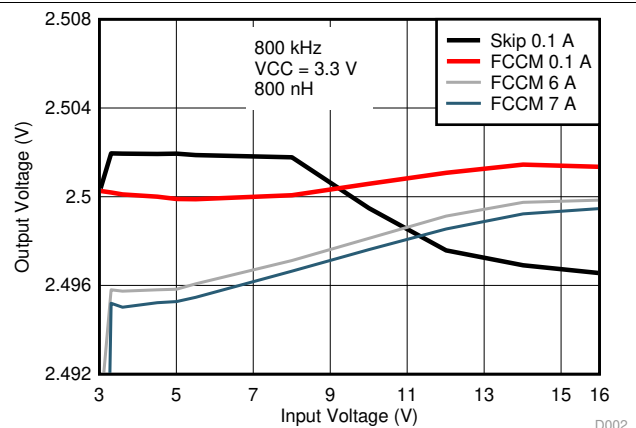


Figure 32. Output Voltage vs Input Voltage VCC = 3.3V External Bias

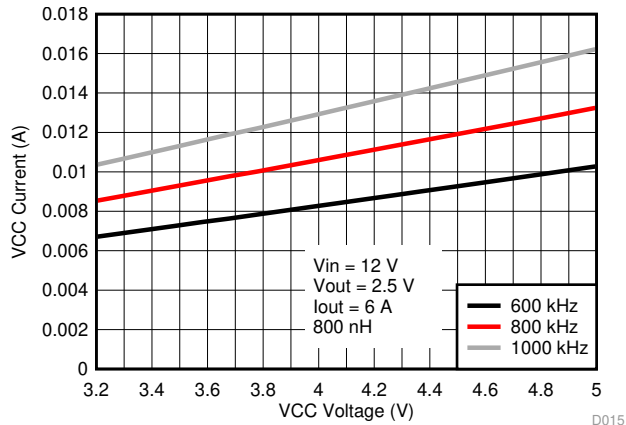


Figure 33. ICC Current vs External VCC Voltage

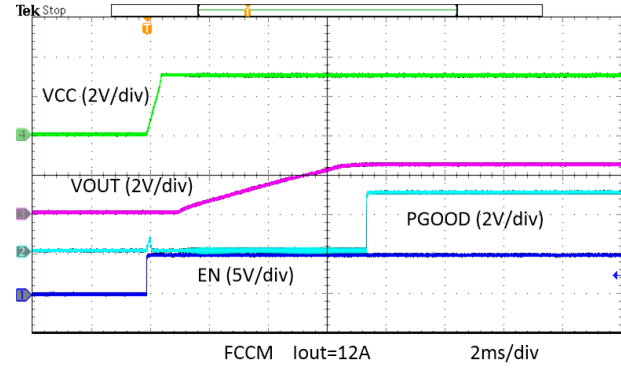


Figure 34. Enable Start-Up, Full Load

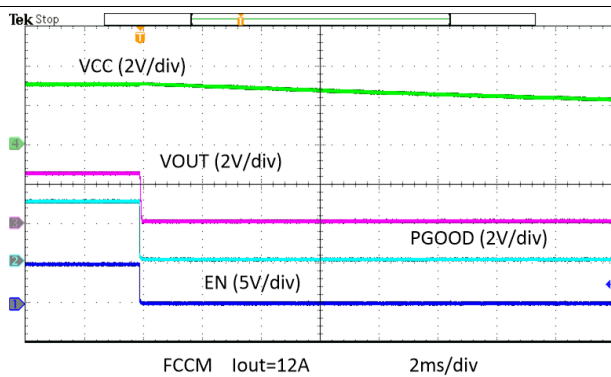


Figure 35. Enable Power Down Full Load

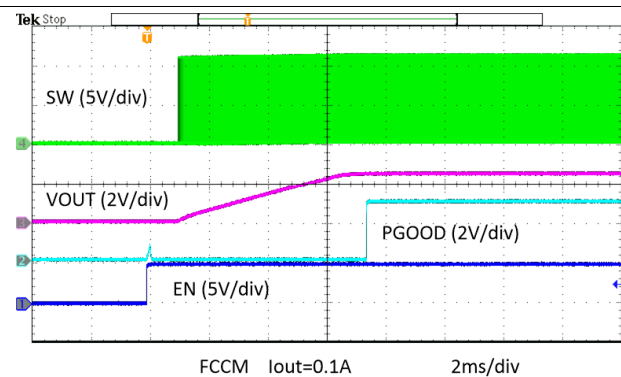


Figure 36. Enable to Power Up Iout = 0.1 A

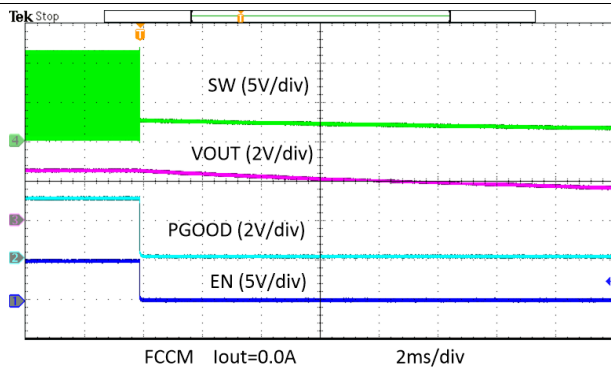


Figure 37. Enable to over Down Iout = 0 A

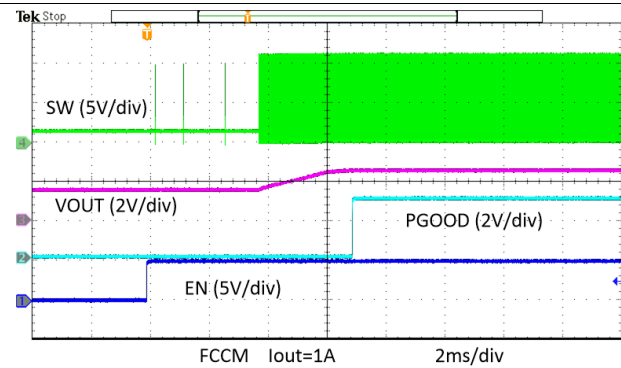


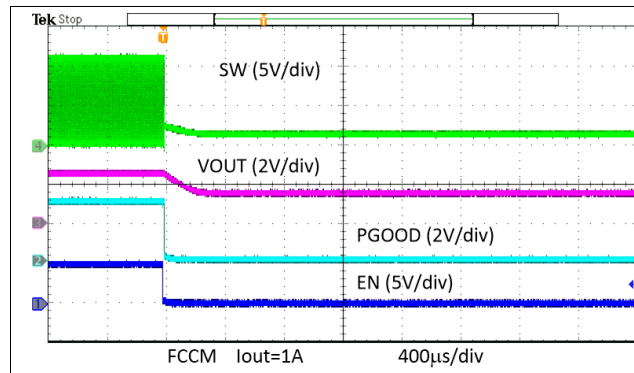
Figure 38. Enable Start-Up, Prebias



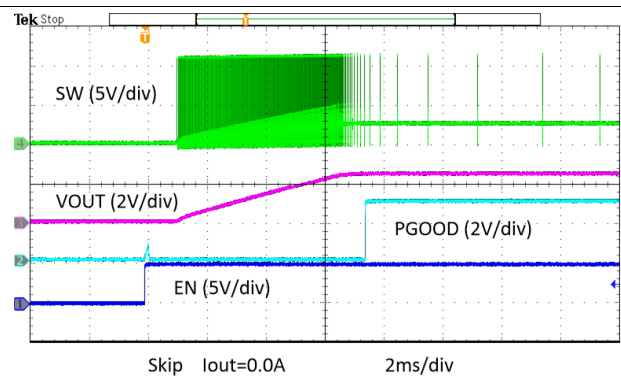
# TPS54JA20

SNVSB02B – MARCH 2020 – REVISED JUNE 2020

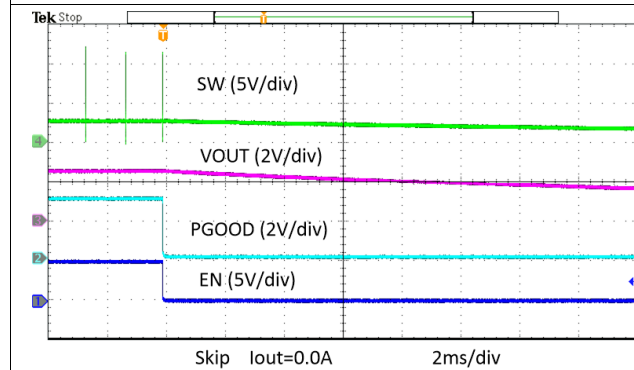
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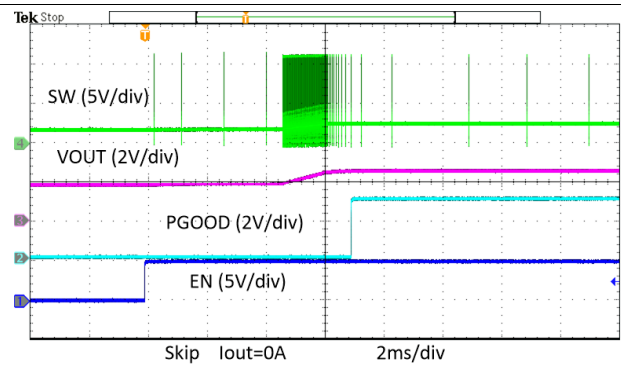
**Figure 39. Prebias Power-Up**



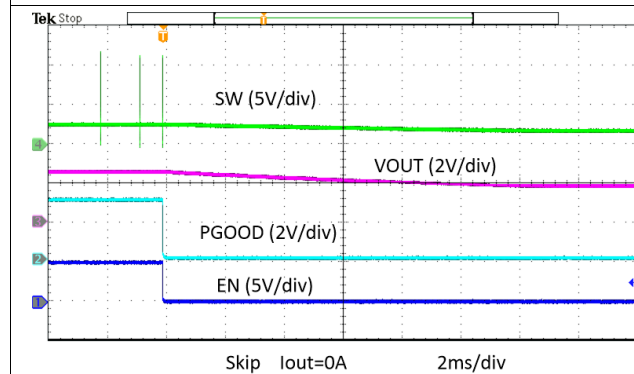
**Figure 40. Enable Power Up, Skip**



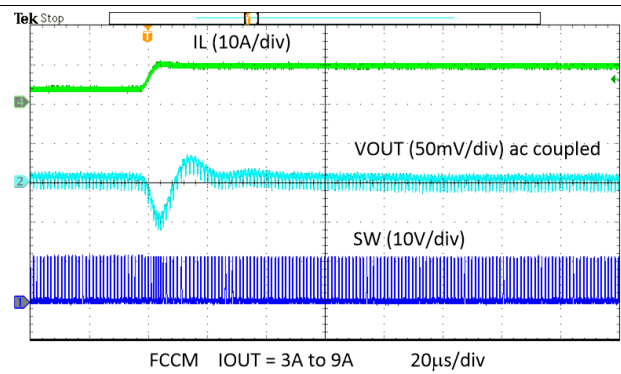
**Figure 41. Enable Power Down, Skip**



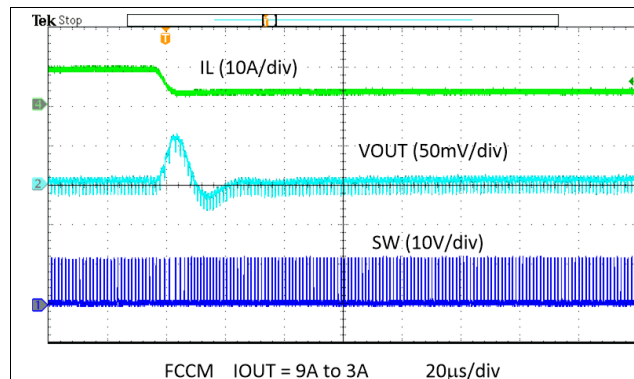
**Figure 42. Enable Power Up into Pre-bias, Skip**



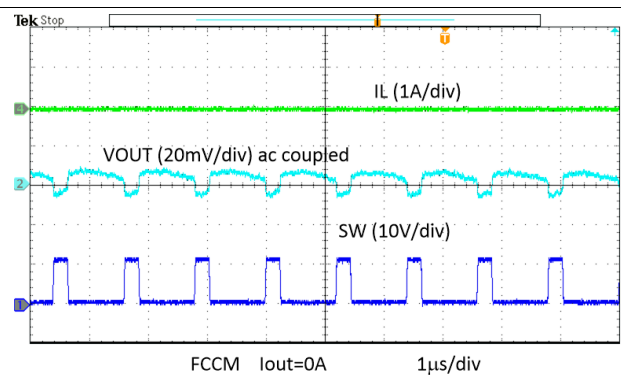
**Figure 43. Enable Power Down with Pre-bias, Skip**



**Figure 44. FCCM Mode Load Transient**

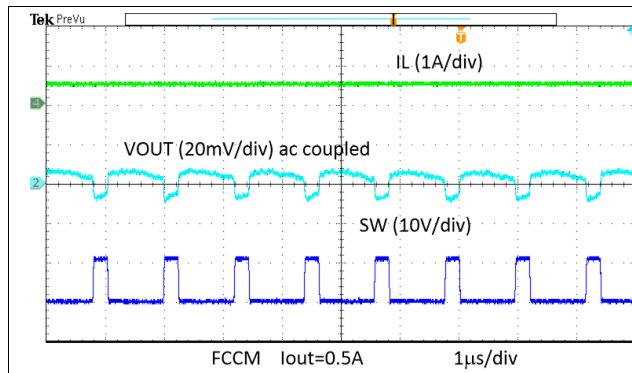


**Figure 45. Unload Transient**

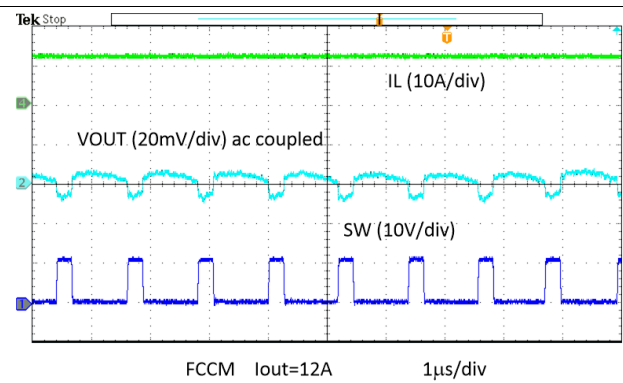


**Figure 46. Output Voltage Ripple**

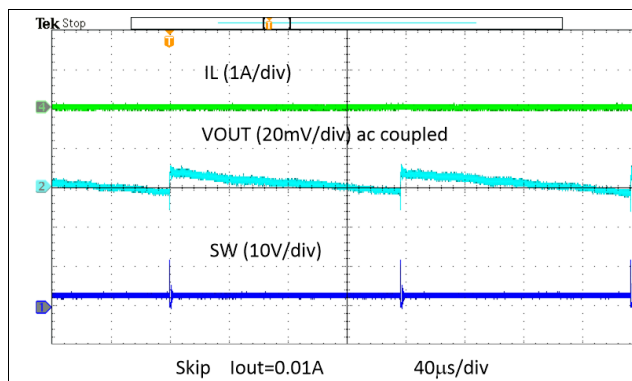




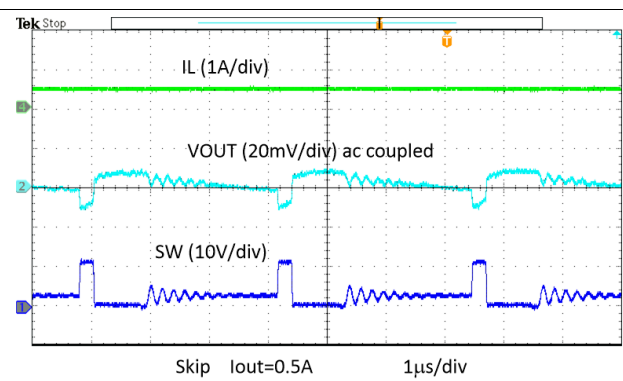
**Figure 47. Output Voltage Ripple**



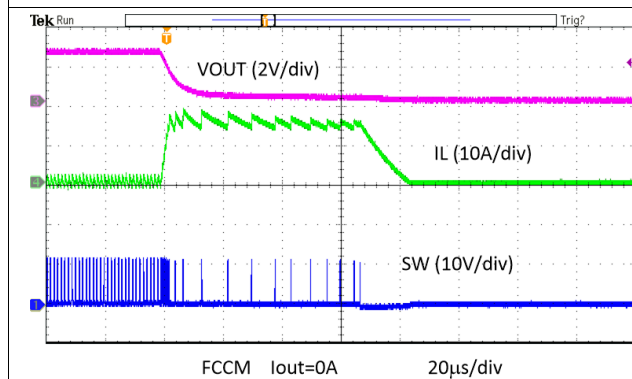
**Figure 48. Output Voltage Ripple**



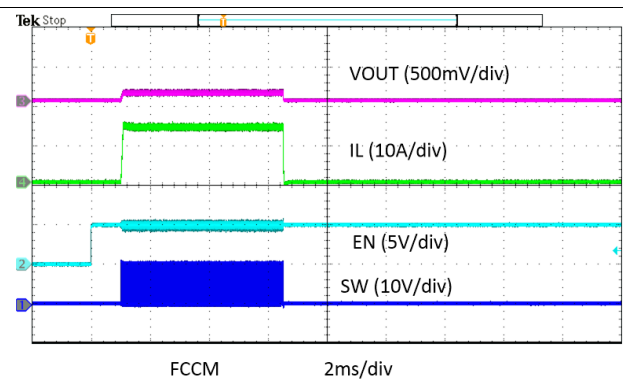
**Figure 49. Output Voltage Ripple, Skip**



**Figure 50. Output Voltage Ripple, Skip**



**Figure 51. Over Current Protection**

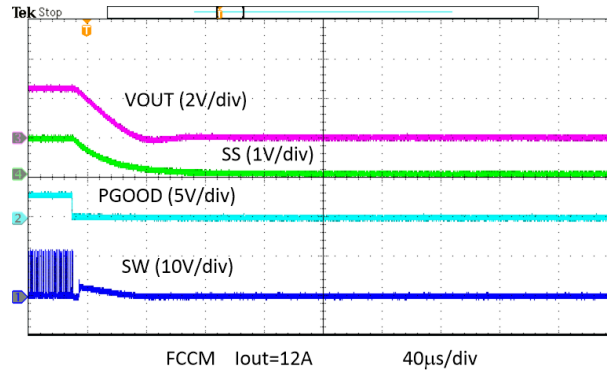


**Figure 52. Enable into Overcurrent**

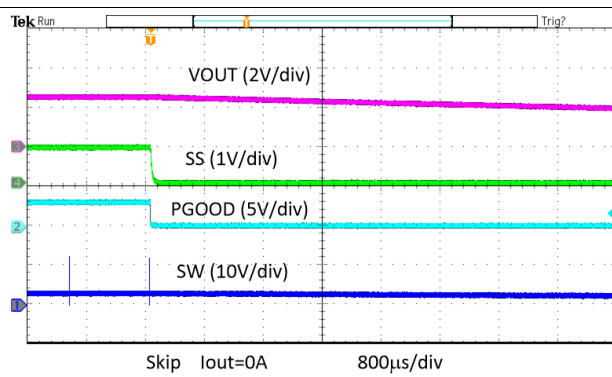
## TPS54JA20

SNVSB02B – MARCH 2020 – REVISED JUNE 2020

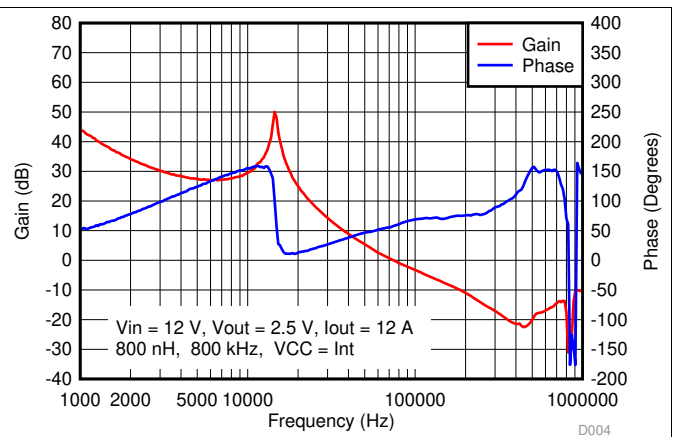
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**Figure 53. Over Temperature Protection in FCCM**



**Figure 54. Over Temperature Protection in Skip**



**Figure 55. Frequency Response, 12 A Load**

## 9 Power Supply Recommendations

The device is designed to operate from a wide input voltage supply range between 2.7-V and 16-V when VCC pin is powered by external bias ranging from 3.13-V to 5.3-V. Both input supplies (VIN and VCC bias) must be well regulated. Proper bypassing of input supplies (VIN and VCC bias) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in the [Layout](#) section.

## 10 Layout

### 10.1 Layout Guidelines

Before beginning a design using the device, consider the following:

- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. In order to shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- VIN decoupling capacitors are important for FET robustness. A 1 $\mu$ F/25V/X6S/0402 ceramic capacitor on VIN pin 21 is required. The PGND vias for this decoupling capacitor should be placed so that the decoupling capacitor is closer to IC than the PGND vias. To lower ESL from via connection, two 8-mil vias are recommended for the PGND connection to inner PGND plane.
- A 1 $\mu$ F/25V/X6S/0402 ceramic capacitor on VIN pin 10 is highly recommended. If this 0402 size capacitor is not used, the bigger size VIN decoupling capacitors (0603 or 0805 size) are required to be placed as close as possible to IC pin 10 and pin 11.
- Two 1 $\mu$ F/25V/X6S/0402 ceramic capacitors on bottom layer are recommended for high current applications ( $I_{out} > 13A$ ). One of these two capacitors should be centered between VIN pin 10 and pin 21. To have good connection for this capacitor, a VIN copper on bottom layer and two VIN vias are needed. The other one can be placed close to IC package just like a mirrored copy to the 0402 capacitor on top layer.
- At least 6 PGND vias are required to be placed as close as possible to the PGND pins (pin 11 to pin 15). This minimizes parasitic impedance and also lowers thermal resistance.
- Place the VCC decoupling capacitor (2.2 $\mu$ F/6.3V/X6S/0402 or 2.2 $\mu$ F/6.3V/X7R/0603) as close as possible to the device. Ensure the VCC decoupling loop is smallest.
- Place BOOT capacitor as close as possible to the BOOT and SW pins. Use traces with a width of 12 mil or wider to route the connection. TI recommends using a 0.1- $\mu$ F to 1- $\mu$ F bootstrap capacitor with 10-V rating.
- The PCB trace, which connects the SW pin and high-voltage side of the inductor, is defined as switch node. The switch node must be as short and wide as possible.
- Always place the feedback resistors near the device to minimize the FB trace distance, no matter single-end sensing or remote sensing.
  - For remote sensing, the connections from the FB voltage divider resistors to the remote location should be a pair of PCB traces with at least 12-mil trace width, and should implement Kelvin sensing across a high bypass capacitor of 0.1- $\mu$ F or higher. The ground connection of the remote sensing signal must be connected to VSNS– pin. The  $V_{OUT}$  connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VSNS– pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines should stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. And it is recommended to shield the pair of remote sensing lines with ground planes above and below.
  - For single-end sensing, connect the higher FB resistor to a high-frequency local bypass capacitor of 0.1- $\mu$ F or higher, and short VSNS– to AGND with shortest trace.
- This device doesn't require a capacitor from SS/REFIN pin to AGND, thus it is not recommended to place a capacitor from SS/REFIN pin to AGND. If both  $C_{SS/REFIN-to-VSNS-}$  and  $C_{SS/REFIN-to-AGND}$  capacitors exist, place  $C_{SS/REFIN-to-VSNS-}$  more closely with shortest trace to VSNS– pin.
- Pin 2 (AGND pin) must be connected to a solid PGND plane on inner layer. Use the common AGND via to connect the resistors to the inner ground plane if applicable.
- See [Figure 56](#) for the layout recommendation.

## TPS54JA20

SNVSB02B – MARCH 2020 – REVISED JUNE 2020

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### 10.2 Layout Example

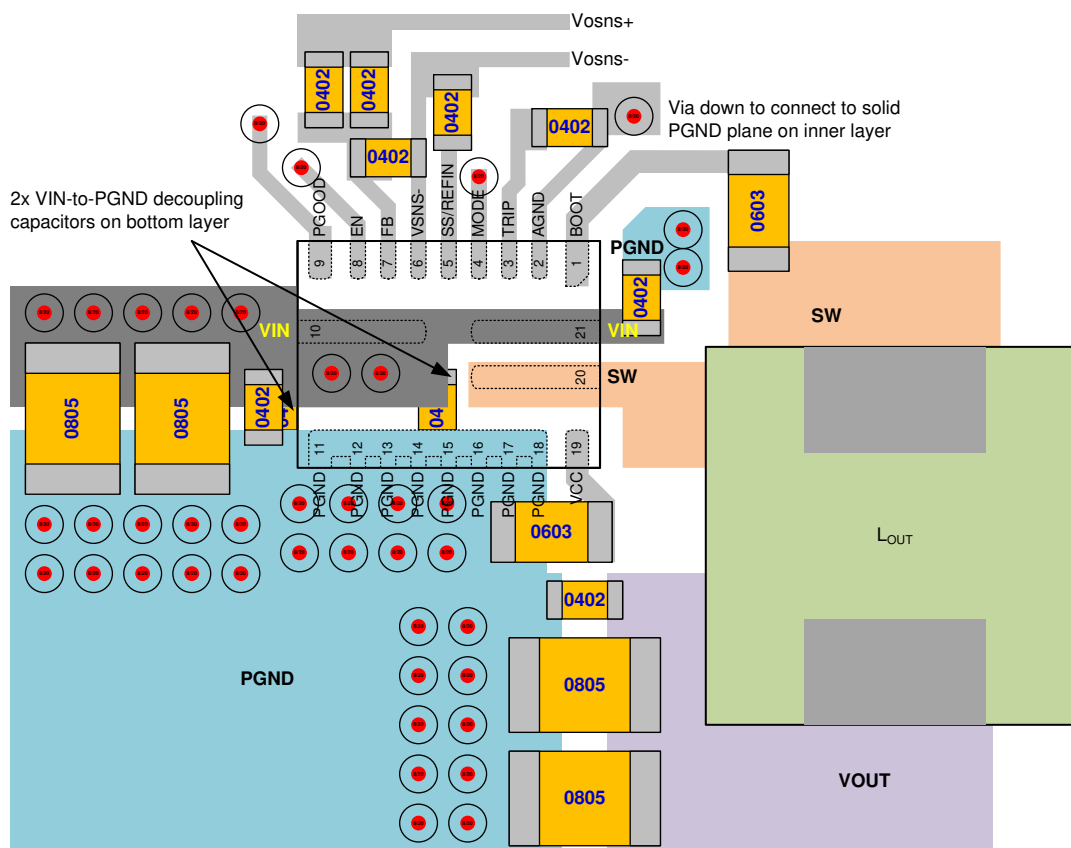


Figure 56. Layout Recommendation

### 10.3 Thermal Performance On TI EVM

Test conditions:

$f_{SW} = 800 \text{ kHz}$ ,  $V_{IN} = 12 \text{ V}$ ,  $V_{CC} = \text{Int LDO}$ ,  $V_{OUT} = 1 \text{ V}$ ,  $I_{OUT} = 15 \text{ A}$ , Inductor  $L_{OUT} = 0.8 \mu\text{H}$  (2.29 mΩ typ),  $C_{OUT} = 6 \times 22\text{-}\mu\text{F}$  (1206/6.3V/X7R), no  $R_{BOOT}$ , no RC Snubber  
SP1 (IC): 75.4°C, SP2 (Inductor): 53.3°C

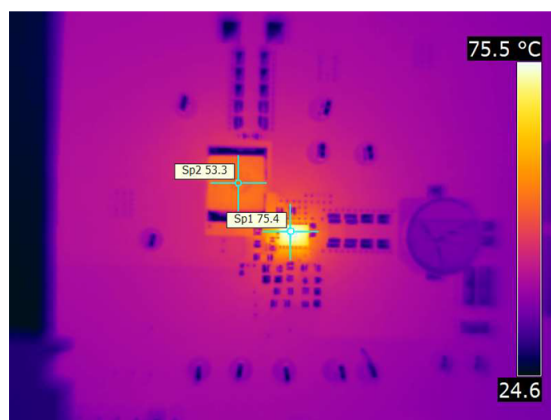


Figure 57. Thermal Image At 25°C Ambient

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

*[Optimizing transient response of internally compensated dc-dc converters with feedforward capacitor](#)*

*[Non-isolated point-of-load solutions for VR13.HC in rack server and datacenter applications](#)*

### 11.2 Trademarks

D-CAP3, Eco-mode are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS54JA20RWW     | ACTIVE        | VQFN-HR      | RWW                | 21   | 3000           | RoHS & Green    | Call TI   NIPDAU                     | Level-2-260C-1 YEAR  | -40 to 125   | T54JA20                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS54JA20RWWR | VQFN-HR      | RWW             | 21   | 3000 | 330.0              | 12.4               | 3.3     | 4.3     | 1.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

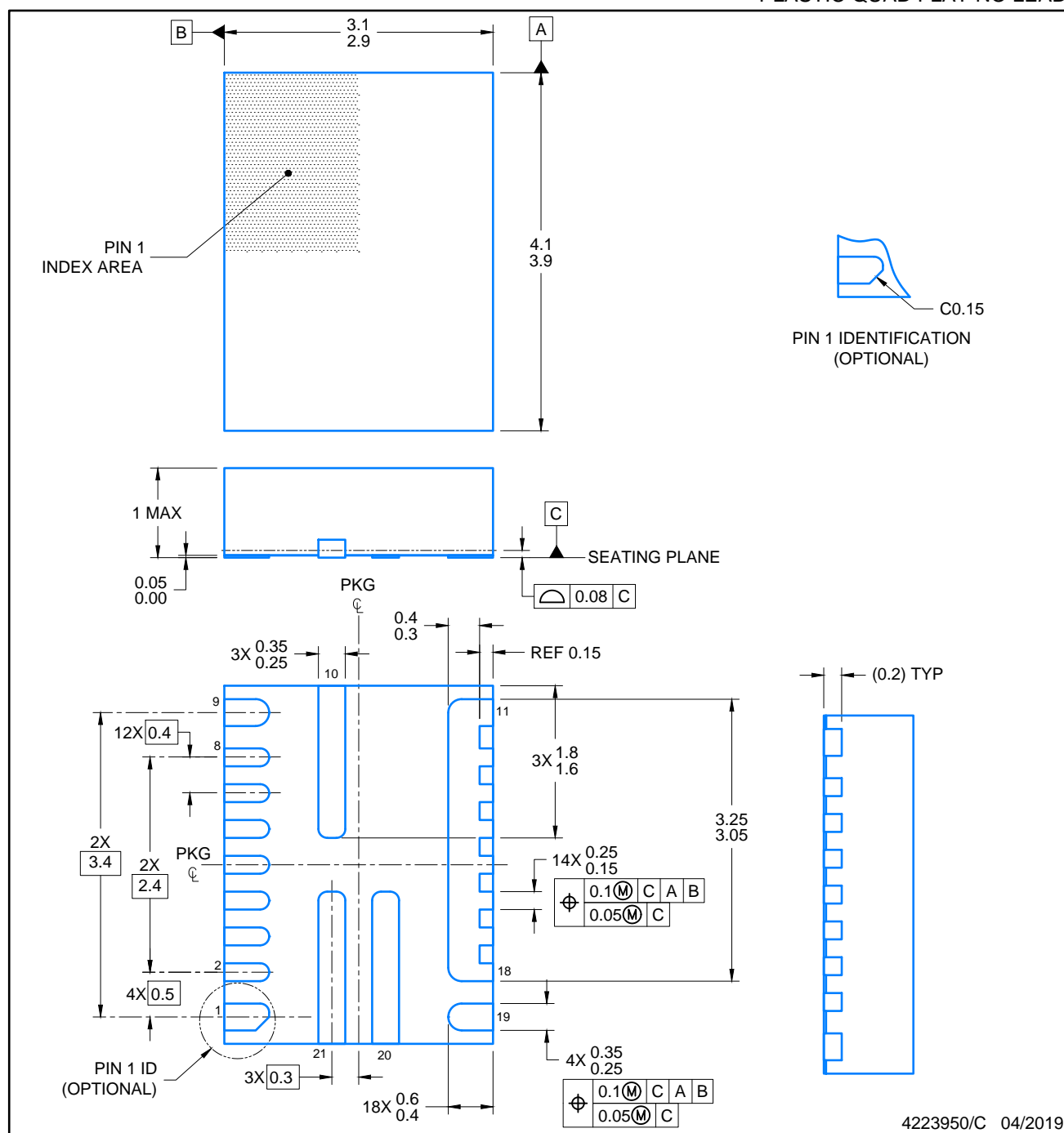
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS54JA20RWWR | VQFN-HR      | RWW             | 21   | 3000 | 367.0       | 367.0      | 35.0        |



## PACKAGE OUTLINE

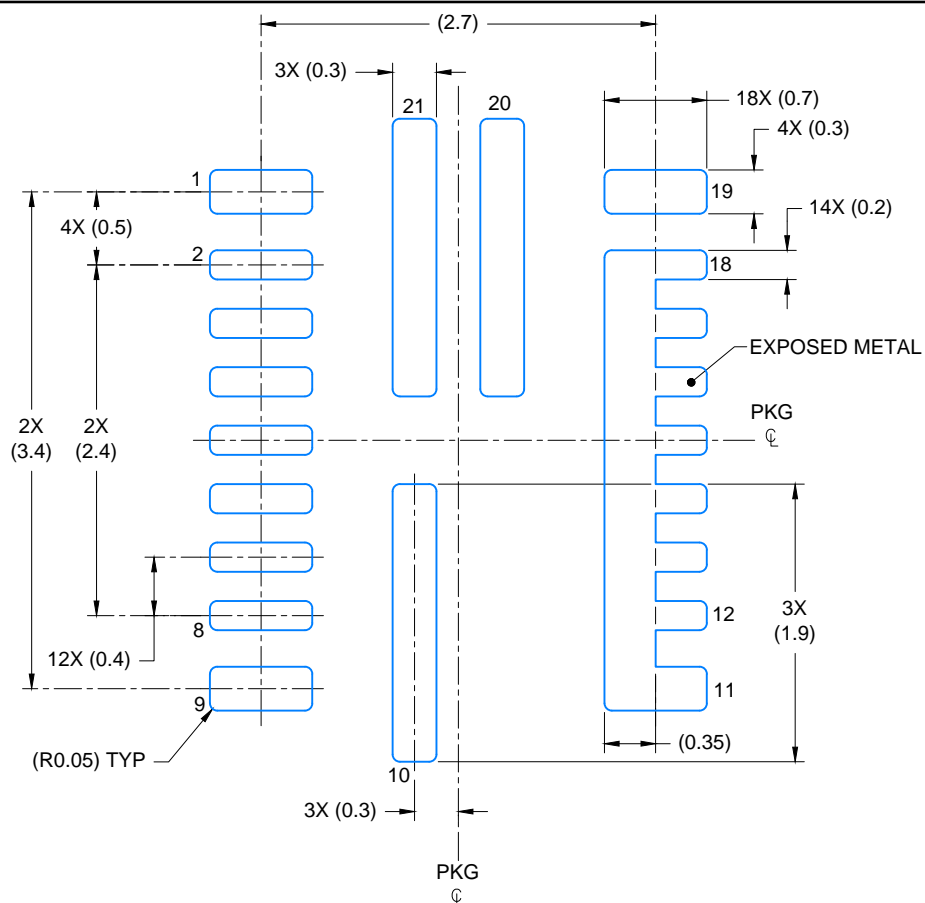
### VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD

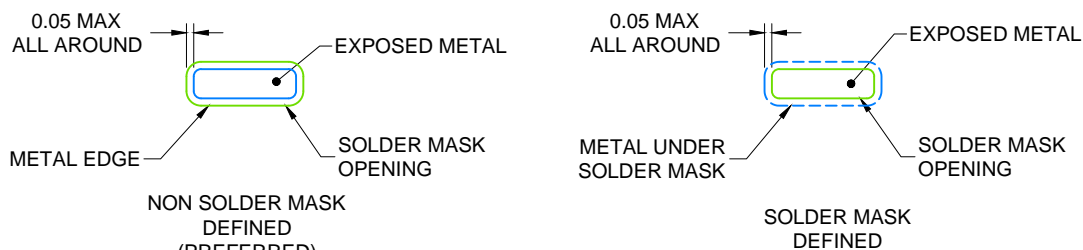


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE: 20X

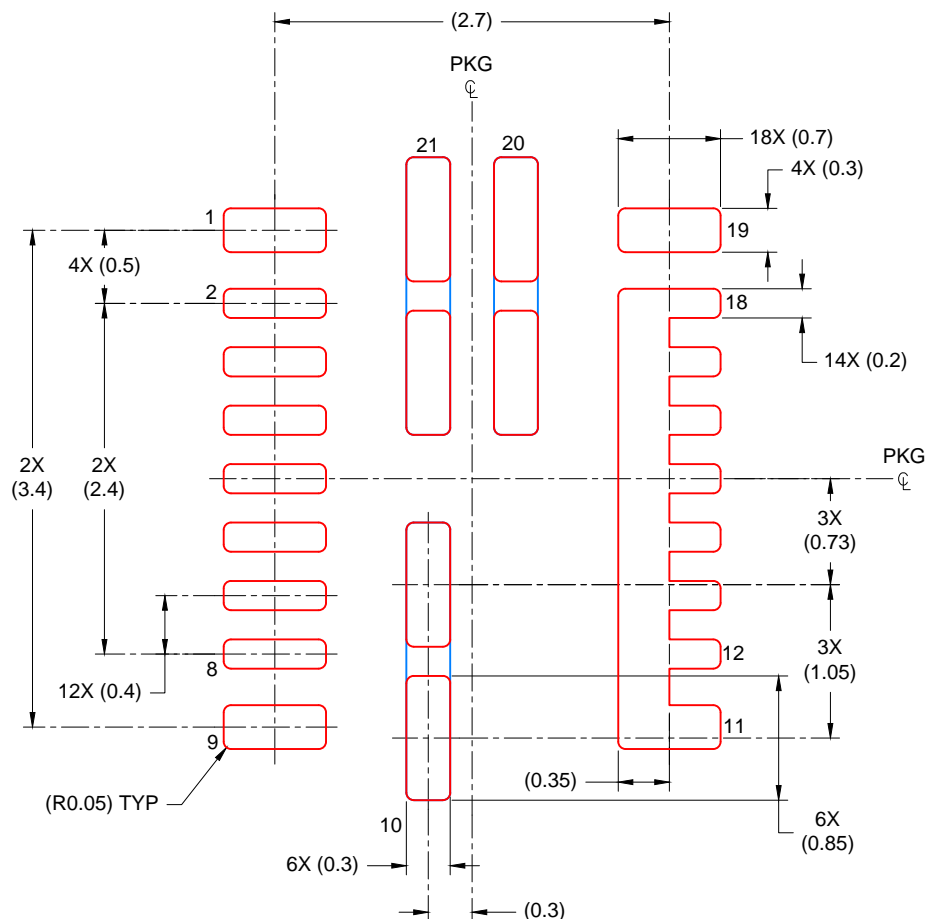


SOLDER MASK DETAILS

4223950/C 04/2019

NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD  
89% PRINTED COVERAGE BY AREA  
SCALE: 20X

4223950/C 04/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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