集成电流镜的 TPS61391 85V_{OUT} 升压转换器

1 特性

- 输入电压范围：2.5V 至 5.5V
- 输出电压范围：高达 85V
- 开关 FET 的 $R_{(DS)on}$：0.9Ω
- 开关电流限制：1000mA
- 具有 0.5µs 响应时间的高光功率保护
- 开关频率：700kHz
- 瞬态电流：来自 VIN 时为 110µA，来自 VOUT 时为 340µA，来自 AVCC 时为 140µA
- 软启动时间：4.8ms
- 封装：3mm × 3mm × 0.75mm QFN

2 应用

- APD 偏置
- 光线路终端
- 高压传感器电源

3 说明

TPS61391 是一个 700kHz 脉宽调制 (PWM) 升压转换器，具有 85V 开关 FET，输入范围为 2.5V 至 5.5V。开关峰值电流高达 1000mA。TPS61391 包括具有两个可选增益选项（1:5 或 4:5）的精确电流镜。

TPS61391 还提供高光功率保护，并将一个额外的 FET 与 APD 电源路径串联在一起，典型响应时间为 0.5µs。当高光功率下降时，它能够自动恢复。

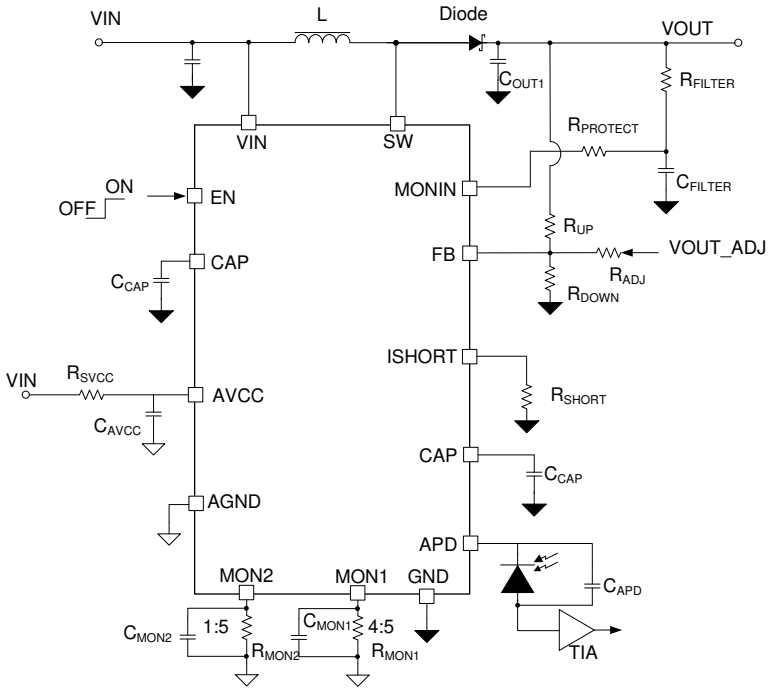
TPS61391 可采用下面带有外露焊盘的 3mm × 3mm QFN 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS61391	WQFN (16)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路



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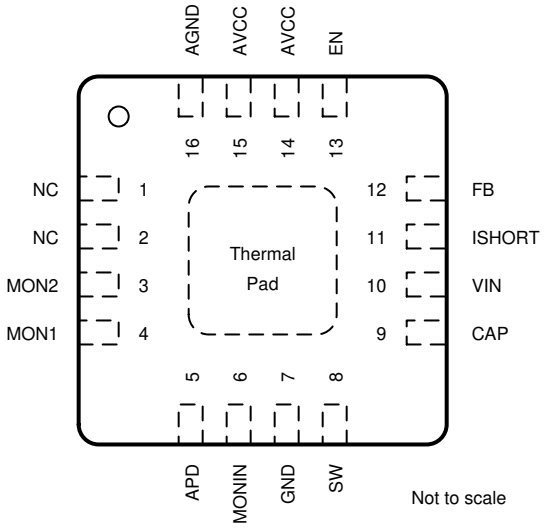
4 修订历史记录

日期	修订版本	说明
2019 年 11 月	*	初始发行版。

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1,2	N/A	No internal connection
MON2	3	O	Current mirror output pin of 1 : 5 ratio (Mirror current: APD current)
MON1	4	O	Current mirror output pin of 4 : 5 ratio (Mirror current: APD current)
APD	5	O	Power supply for the APD, connect this pin with the cathode of APD
MONIN	6	I	Current mirror input pin
GND	7	–	Power Ground
SW	8	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET
CAP	9	O	Connecting a capacitor externally to lower the noise for current mirror.
VIN	10	I	IC power supply input
ISHORT	11	O	Programming the current limit for high optical power protection by a resistor between this pin and GND.
FB	12	I	Feedback voltage
EN	13	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode
AVCC	14,15	I	Power supply for the current monitor circuitry
AGND	16	–	Analog ground for the current monitor circuitry
Exposed Thermal Pad			Connect with GND, TI recommends connecting to Power GND on PCB

6 Specifications

6.1 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage	20		85	V
T_J	Junction temperature	–40		125	°C
L	Effective Inductance		4.7		µH
C_{IN}	Effective Input Capacitance		1		µF
C_{OUT}	Effective Output Capacitance		0.1		µF

6.2 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	SW, APD, MONIN,CAP	–0.3	85	V
	Other pins	–0.3	6	V
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±1500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC(1)		TPS61391 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Y_{JB}	Junction-to-board characterization parameter	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended free-air temperature range, V_{IN} = 3.3 V, AV_{CC} = 3.3 V, V_{MONIN} = 20 V to 85 V, T_J = - 40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

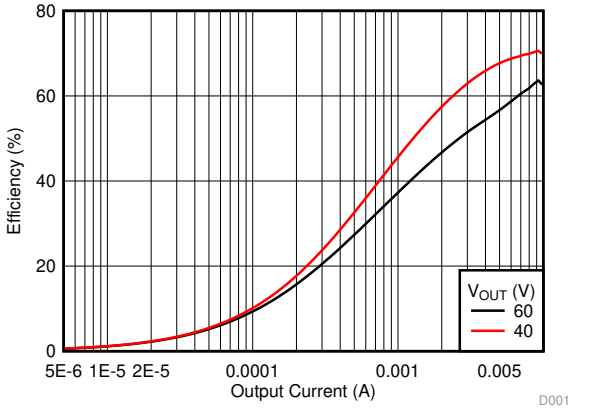
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V

Electrical Characteristics (continued)

Over recommended free-air temperature range, V_{IN} = 3.3 V, AV_{CC} = 3.3 V, V_{MONIN} = 20 V to 85 V, T_J = - 40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

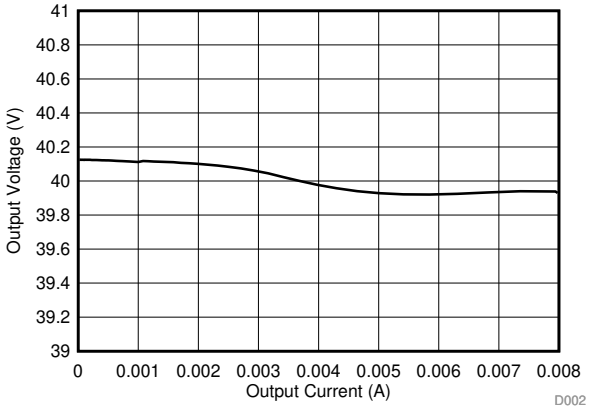
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.4	2.5	V
	Under voltage lock out hysteresis	V_{UVLO} rising - V_{UVLO} falling		200		mV
I_{Q_IN}	Quiescent current into VIN pin	V_{IN} = 3.3 V, V_{FB} =V_{REF} + 0.1 V, No switching, -40 °C ≤ T_J ≤ 85 °C		110	140	uA
I_{Q_OUT}	Quiescent current into VOUT pin	V_{IN} = 3.3 V, V_{FB} =V_{REF} + 0.1 V,No switching, -40 °C ≤ T_J ≤ 85 °C		340	430	uA
I_{Q_VCC}	Quiescent current into AVCC pin	AVCC = 3.3 V -40 °C ≤ T_J ≤ 85 °C		140	180	uA
I_{SD}	Shutdown current into VIN pin	2.5 V ≤ VIN ≤ 5.5 V, EN = 0, -40 °C ≤ T_J ≤ 85 °C			1	uA
	Shutdown current into VOUT pin	EN = 0, -40 °C ≤ T_J ≤ 85 °C			1	uA
	Shutdown current into AVCC pin	AVCC = 3.3 V, EN = 0, -40 °C ≤ T_J ≤ 85 °C			1	uA
OUTPUT						
V_{OUT}	Output voltage range				85	V
V_{REF}	Feedback regulation reference voltage	V_{IN} = 2.5 V to 5.5 V, T_J = 25 °C	1.188	1.2	1.212	V
		V_{IN} = 2.5 V to 5.5 V, -40 °C ≤ T_J ≤ 125 °C	1.182	1.2	1.218	V
I_{FB}	Feedback input leakage current			1	25	nA
POWER SWITCH						
$R_{DS(on)}$	Low-side FET on resistance	3 V ≤ V_{IN} ≤ 5.5 V		900	1300	mΩ
SWITCHING CHARACTERISTIC						
f_{SW}	Switching frequency	V_{IN} = 3.3 V, V_{OUT} = 60 V	600	700	800	kHz
CURRENT MIRROR						
k_{MON1}	4:5 Current mirror gain	I_{APD} = 5 µA to 200 µA	0.76	0.8	0.84	
k_{MON2}	1:5 Current mirror gain	I_{APD} = 100 µA to 2 mA	0.19	0.2	0.21	
V_{MON}	MON1 / MON2 Threshold		380	400	420	mV
V_{APD_DRP}	Current mirror voltage drop	I_{APD} = 1 mA	2.2	2.5	2.8	V
		I_{APD} = 5 µA		2.45		V
I_{BIAS}	Current mirror bias current		15	20	25	µA
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit	V_{IN} = 3.3 V, V_{OUT} = 60 V	800	1000	1200	mA
I_{SHORT}	High optical power current limit	R_{ISHORT} = 25 kΩ	3.7	4	4.3	mA
		R_{ISHORT} = 50 kΩ	1.8	2	2.2	mA
CONTROL (EN)						
V_{EN_H}	EN Logic high threshold				1.2	V
V_{EN_L}	EN Logic low threshold		0.4			V
R_{EN}	EN pull down resistor			800		kΩ
TIMING						
t_{SS}	Soft start time	Ref voltage 0 to 1.2V		4.8		ms
t_{DELAY}	Delay time for high optical power protection	I_{APD} = 5 mA, I_{SHORT} = 3 mA		0.5		µs
THERMAL PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

6.6 Typical Characteristics



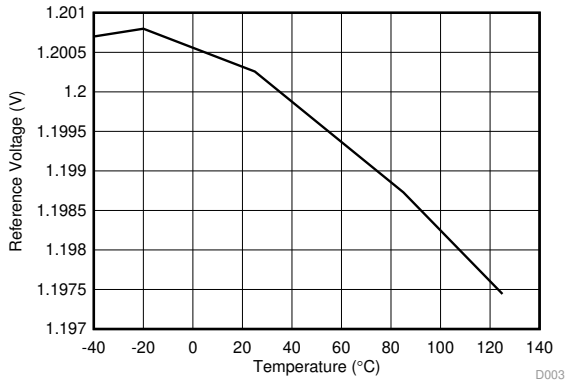
V_{IN} = 3.3 V L = 4. 7 µH C_{OUT} = 0.1 µF
Output current (boost) = 0 to 8 mA

图 1. Efficiency vs. Output Current



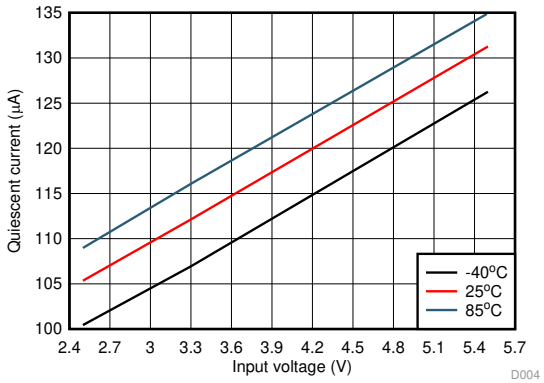
V_{IN} = 3.3 V L = 4. 7 µH C_{OUT} = 0.1 µF
Output current (boost) = 0 to 8 mA

图 2. Load regulation



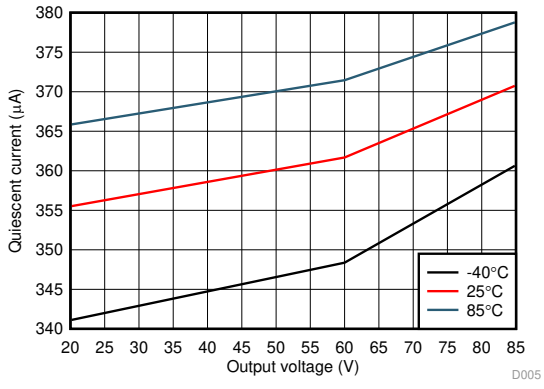
V_{IN} = 3.3 V V_{OUT} = 60 V C_{OUT} = 0.1 µF

图 3. Reference voltage



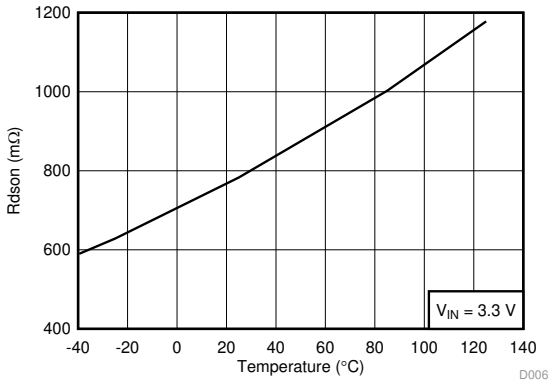
V_{OUT} = 60 V

图 4. Quiescent current vs. Input voltage



V_{IN} = 3.3 V

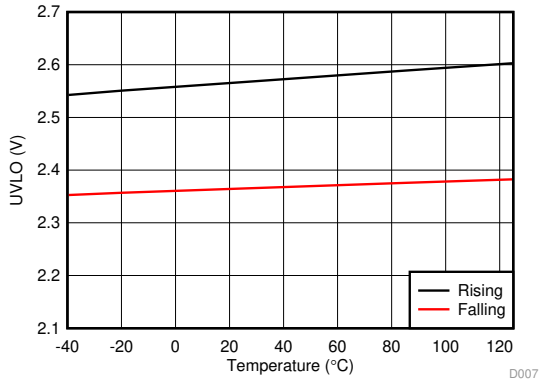
图 5. Quiescent current vs. Output voltage



V_{IN} = 3.3 V V_{OUT} = 60 V

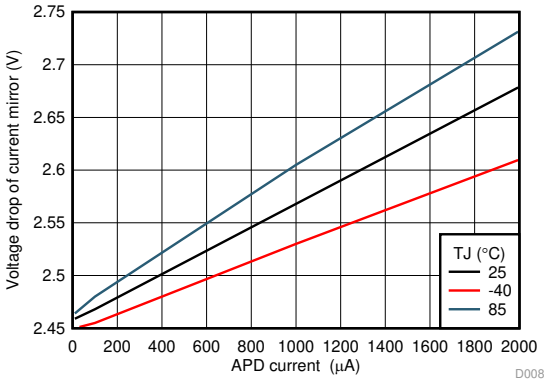
图 6. Rdson vs. Temperature

Typical Characteristics (接下页)



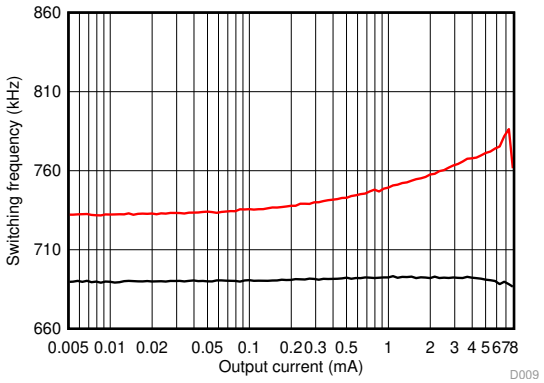
V_{OUT} = 60 V

图 7. Vin UVLO



V_{IN} = 3.3 V V_{OUT} = 60 V

图 8. Voltage drop of current mirror vs. current



V_{IN} = 3.3 V V_{OUT} = 60 V

图 9. Switching frequency vs. Output current

7 Detailed Description

7.1 Overview

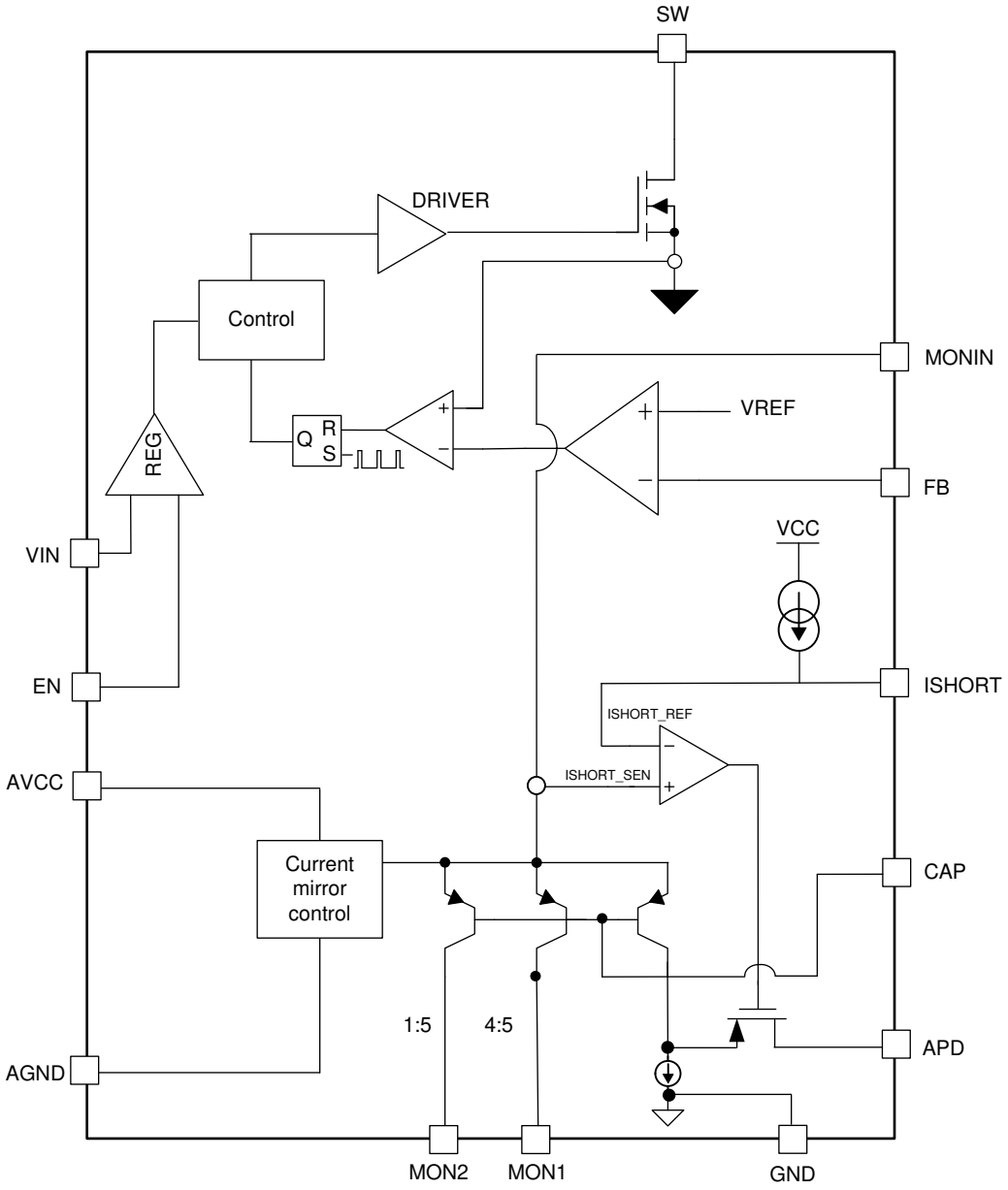
The TPS61391 is a fully integrated boost converter with an 85-V FET to convert a low input voltage to a higher voltage for biasing the APD. The TPS61391 supports an input voltage ranging from 2.5 V to 5.5 V. The device operates at a 700 kHz pulse-width modulation (PWM) crossing the whole load range.

There are two ratio options for the current proportional to APD current: the MON1 (4 : 5) and MON2 (1 : 5). By connecting a resistor from the mirror output (MON1 or MON2) to GND, the current flowing through the APD is converted into the voltage crossing the resistor from MON1 / MON2 to GND.

Additionally, a high power optical protection is integrated by clamping the pre-set current limit (program by the I_{SHORT} resistor). The response time of the high optical power is typically 0.5 µs. The device could recovery automatically when the high optical power is removed.

The device comes in a 3-mm × 3-mm QFN package with the operating junction temperature covering from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.5 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 200 mV.

Feature Description (接下页)

7.3.2 Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 2.5 V and the EN pin is pulled above the high threshold (1.2 V min.), the TPS61391 is enabled. When the EN pin is pulled below the low threshold (0.4 maximum), the device goes into shutdown mode.

7.3.3 Current Mirror

There are two current mirror options for TPS61391: the gain of 4: 5 (MON1) and 1: 5 (MON2). The maximum voltage of MON1 and MON2 is 2.5 V.

7.3.4 High Optical Power Protection

There is an additional FET in series of power path connecting with the APD. When the current flowing through the APD exceeds the short protection threshold (set by connecting the resistor from I_{SHORT} to GND), the on resistance of the FET becomes larger to clamp the current within the protection threshold by lowering the APD bias voltage. It takes typically 0.5 µs for the FET to respond in case of high optical power occuring.

When the high optical power condition releases, the TPS61391 recovers automatically back to the normal operation mode.

7.4 Device Functional Mode

7.4.1 PFM Operation

The TPS61391 integrates a power save mode with pulse frequency modulation (PFM) at the light load. When a light load condition occurs, the COMP pin voltage naturally decreases and reduces the peak current. When the COMP pin voltage further goes down with the load lowered and reaches the pre-set low threshold, the output of the error amplifier is clamped at this threshold and does not go down any more. If the load is further lowered, the device skips the switching cycles and reduces the switching losses and improves efficiency at the light load condition by reducing the average switching frequency.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61391 is a step-up DC/DC converter with current monitor circuitry integrated. The following design procedure can be used to select component values for the TPS61391. This section presents a simplified discussion of the design process.

8.2 Typical Application

This application is designed for 2.5-V to 5.5-V input, and 60-V output user case

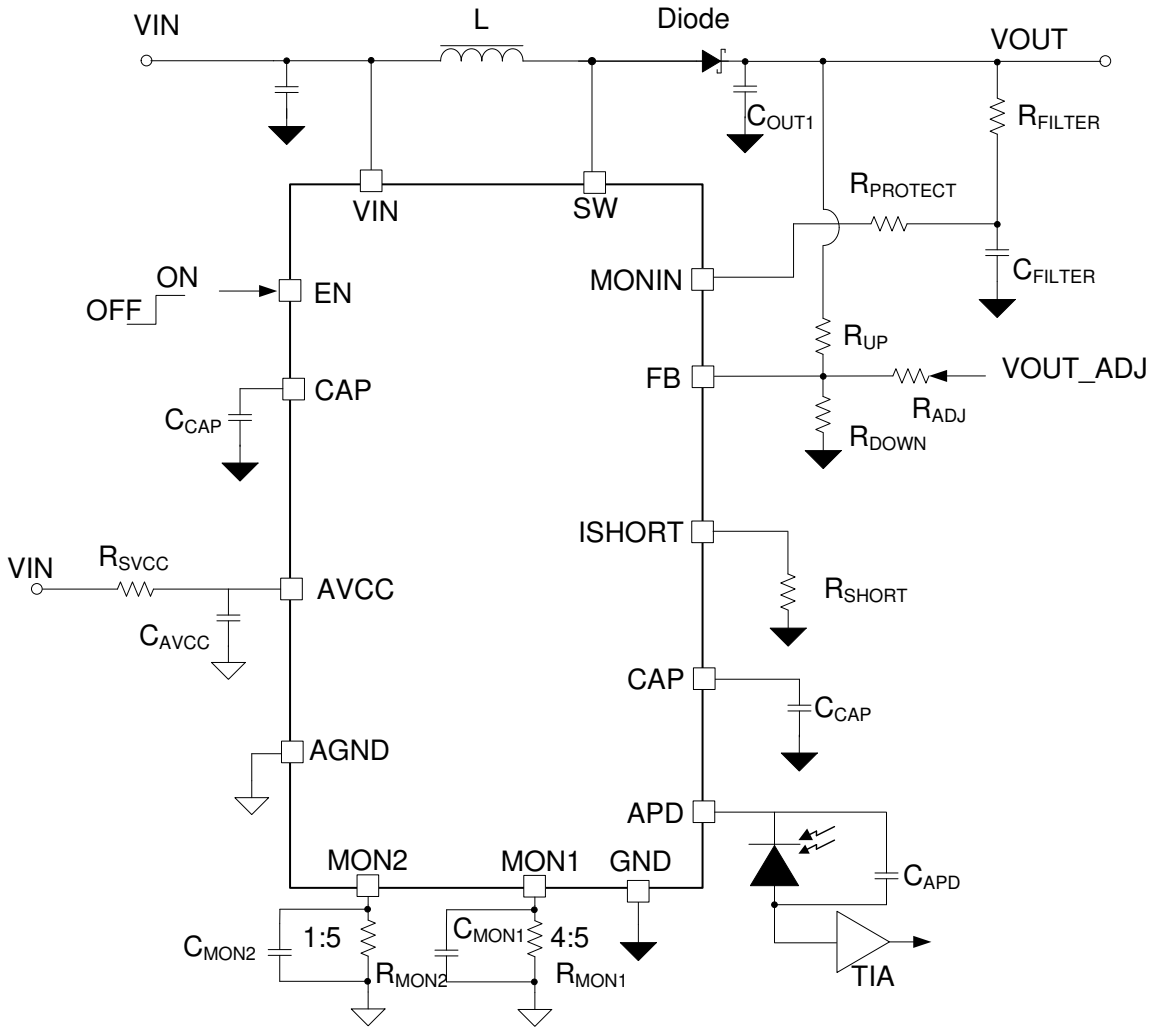


图 10. TPS61391 Typical Application

8.2.1 Design Requirement

For this design example, use 表 1 as the design parameters.

Typical Application (接下页)

表 1. Design Parameters

PARAMETER	VALUE
Input voltage range	2.5 V to 5.5 V
Output voltage	60 V
Operating frequency	700 kHz
APD Current	0 to 2 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Rectifier Diode

A Schottky diode is the preferred type for the rectifier diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus the switching node ringing. Also, it must be able to handle the average output current.

8.2.2.2 Selecting the Inductor

It is suggested that the TPS61391 device works in the DCM operation; otherwise the output voltage would not be delivered for low input voltage to high output voltage.

With the device working in DCM operation, the maximum inductor could be calculated by equation 公式 1 and 公式 2:

$$L_{MAX} = \frac{V_{IN} \times D}{f_{SW} \times I_{LIM}} \quad (1)$$

where

- V_{IN} is input voltage
- D is duty cycle
- f_{SW} is switching frequency
- I_{LIM} is current limit

For instance, if V_{IN} = 3.3 V, V_{OUT} = 60 V, f_{SW} = 600 kHz, I_{LIM} = 0.8 A, the L_{MAX} = 6.5 µH

However, there is minimum inductance is determined by the power delivered to the output side at given input condition.

$$L_{MIN} = 2 \times \frac{V_{OUT} \times I_{OUT}}{eff \times f_{SW} \times I_{LIM}^2} \quad (2)$$

where

- V_{OUT} is output voltage
- I_{OUT} is output current
- eff is the efficiency
- f_{SW} is switching frequency
- I_{LIM} is current limit

For instance, if I_{OUT} = 8 mA, V_{OUT} = 60 V, f_{SW} = 600 kHz, I_{LIM} = 0.8 A, eff = 0.6, the L_{MIN} = 4.2 µH

With the calculation aforementioned, the operating inductor is recommended between the L_{MIN} and L_{MAX}.

The 4.7 µH inductance is optimum value for using the TPS61391 in application.

8.2.2.3 Selecting Output Capacitor

Use low ESR capacitors at the output to minimize output voltage ripple. Use only X5R and X7R types, which retain their capacitance over wider voltage and temperature ranges than other types. Typically use a 0.1-µF to 1-µF capacitor for output voltage. Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate its capacitance at its rated voltage. Therefore, consider enough margins on the voltage rating to ensure adequate capacitance at the required output voltage.

8.2.2.4 Selecting Filter Resistor and Capacitor

TI recommends an additional R-C filter be added for low ripple applications. The filter parameters is characterized based on the ripple requirement. Typically, use a 100-Ω and 0.1-µF filter to reduce the switching output ripple.

8.2.2.5 Setting the Output Voltage

The output voltage of the TPS61391 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by 公式 3.

$$V_{OUT} = V_{FB} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

where

- V_{OUT} is the output voltage
- R_{UP} the top divider resistor
- R_{DOWN} is the bottom divider resistor

(3)

Choose R_{DOWN} to be approximately 10 kΩ. Slightly increasing or decreasing R_{DOWN} can result in closer output voltage matching when using standard value resistors. In this design, R_{DOWN} = 10 kΩ and R_{UP} = 487 kΩ, resulting in an output voltage of 60 V.

8.2.2.6 Selecting Capacitor for CAP pin

TI recommends placing a ceramic capacitor from CAP pin to GND to lower the noise for the APD current mirror. A ceramic capacitor between 10 nF and 100 nF is recommended from CAP pin to GND.

8.2.2.7 Selecting Capacitor for AVCC pin

The control circuitry is powered by AVCC. A ceramic capacitor must be placed close to AVCC, with a typical capacitor value of 2.2 µF.

8.2.2.8 Selecting Capacitor for APD pin

A ceramic capacitor is required to make the APD current mirror more accurately against the noise coupling. The recommended values are from 100 pF to 470 pF.

8.2.2.9 Selecting the Resistors of MON1 or MON2

The TPS61391 provides two currents proportional to APD current on the MON pins, 4 : 5 and 1 : 5. The voltage of the resistors connecting to the MON pins convert the APD current to voltage.

8.2.2.10 Selecting the Capacitors of MON1 or MON2

The capacitors are added to the MON1 or MON2 pins to decouple the noise of APD transient current.

8.2.2.11 Selecting the Short Current Limit

The output current short-protection threshold of the TPS61391 can be programmed by an external resistor using 公式 4.

$$I_{SHORT} = \frac{100}{R_{SHORT}} \quad (4)$$

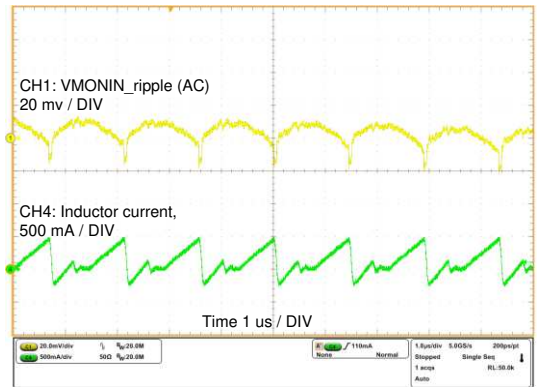
where

- I_{SHORT} (mA) is the short protection threshold
- R_{SHORT}(kΩ) is the resistor connecting from ISHORT pin to GND

For instance, if R_{SHORT} = 25 kΩ, the I_{SHORT} = 4 mA.

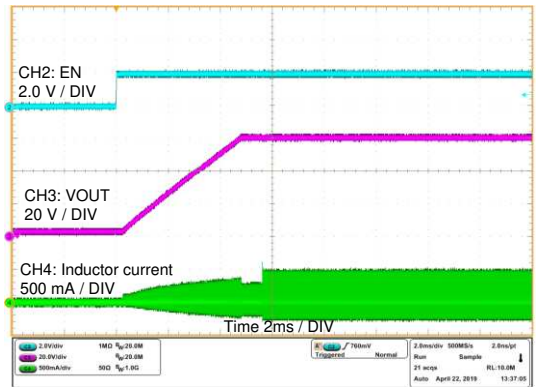
8.2.3 Application Curves

Typical condition V_{IN} = 3.3 V, V_{OUT} = 60 V, R_{SHORT} = 5 kΩ, $R_{MON1/2}$ = 3.01 kΩ and $C_{MON1/2}$ = 10 pF.
Application waveforms are measured with the inductor 4.7 µH and the output capacitance 0.1 µF at room temperature.



V_{IN} = 3.3 V V_{OUT} = 60 V APD current = 1 mA

图 11. Output voltage ripple with 100 Ω / 0.1 µF filter



V_{IN} = 3.3 V V_{OUT} = 60 V APD current = 1mA

图 12. Startup

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems. Use the following checklist to get good performance for a well-designed board:

- Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di / dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;
- Place the noise sensitive network like current mirror output (MON1, MON2) being far away from the SW trace;
- Split the ground for the power GND, signal GND. Use a separate ground trace to connect the current monitor and boost circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

10.2 Layout Example

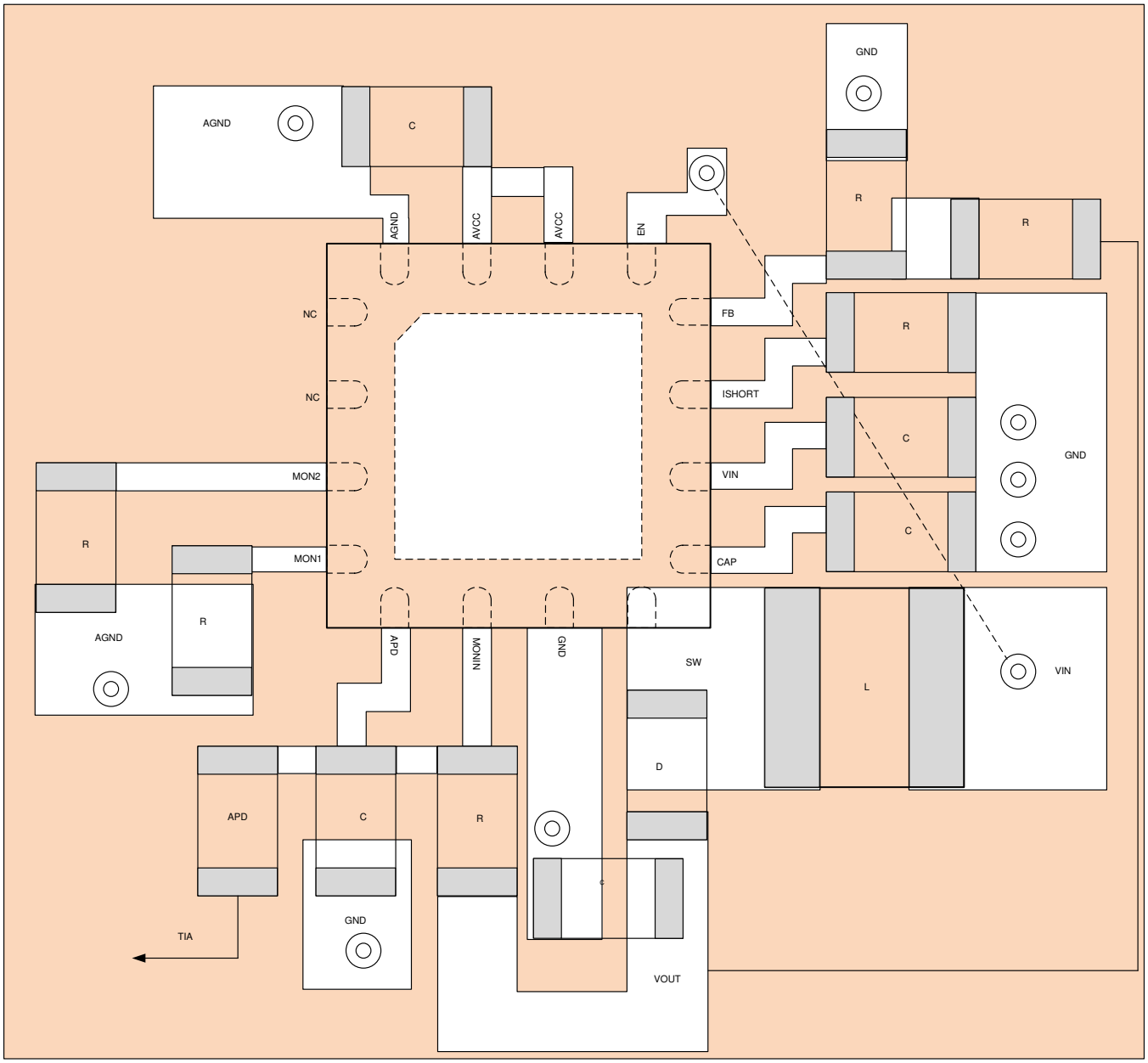


图 13. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 《TPS61391EVM-058 评估模块》用户指南SLVUBS9

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

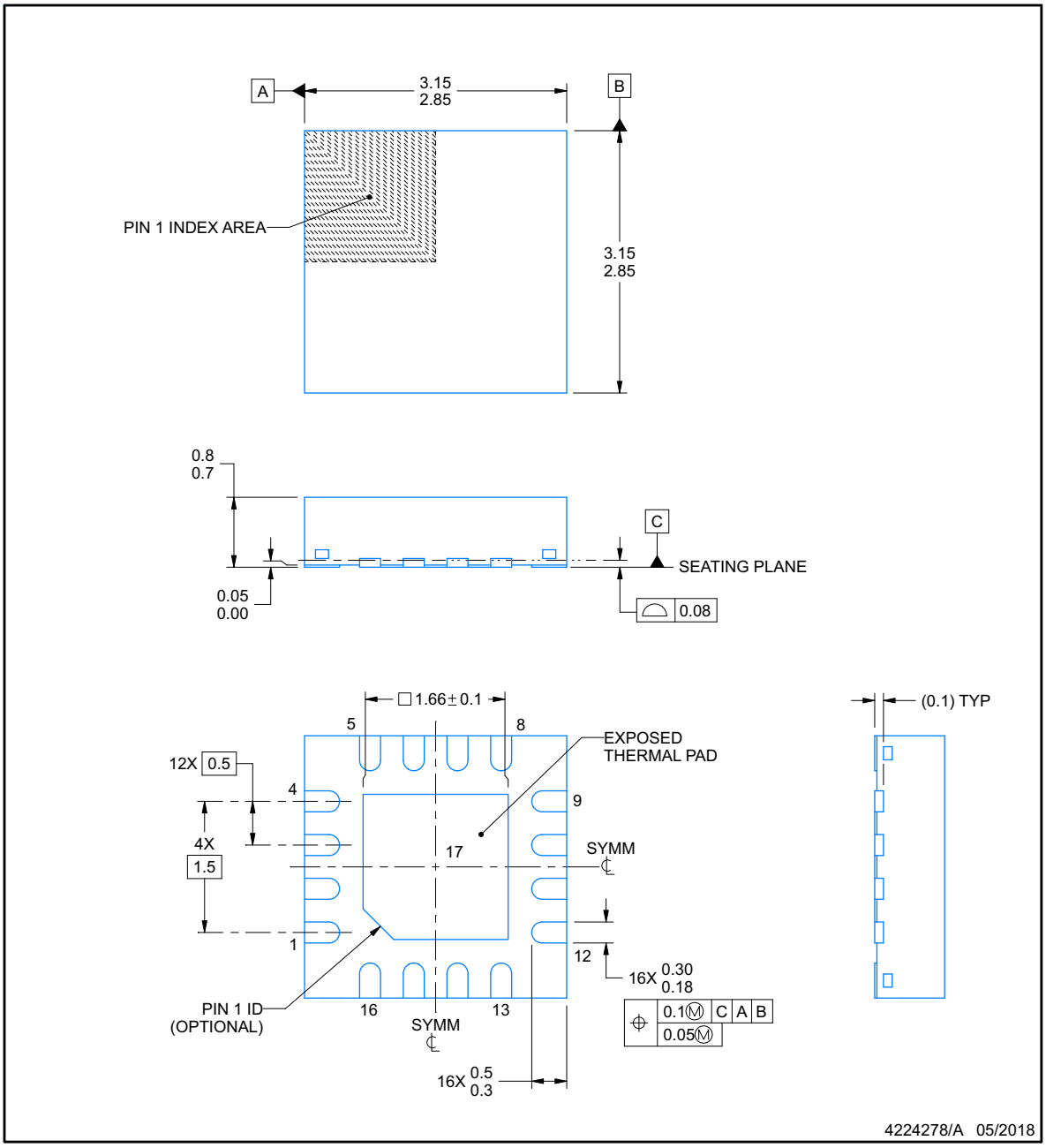
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

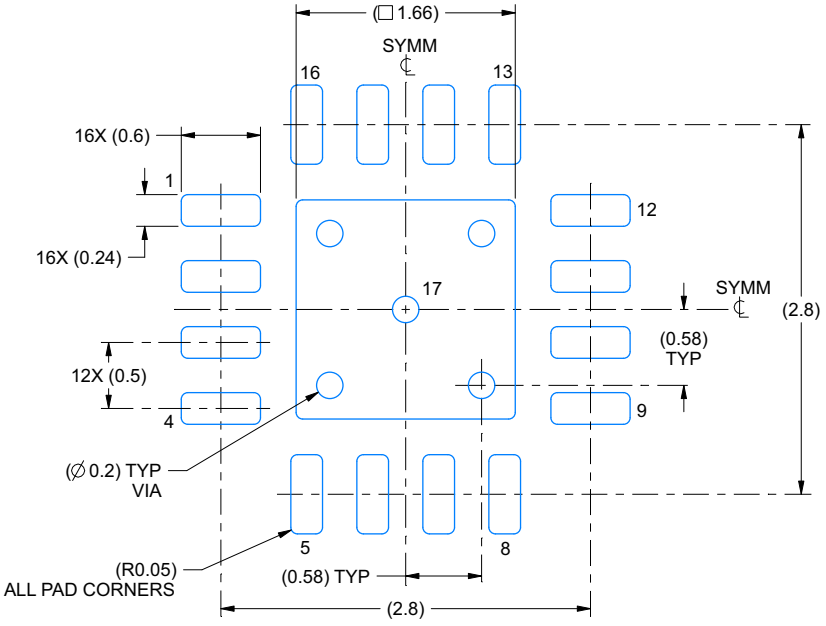
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

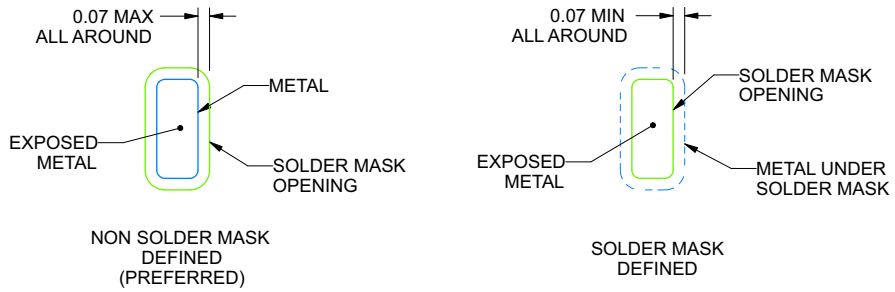
RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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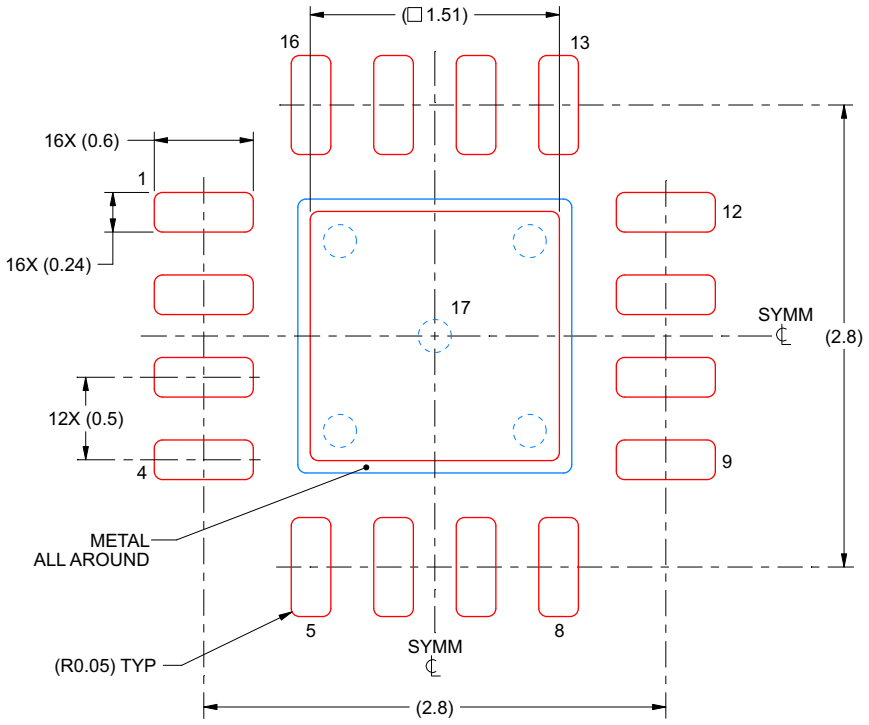
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016J **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61391RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22GH	Samples
TPS61391RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22GH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

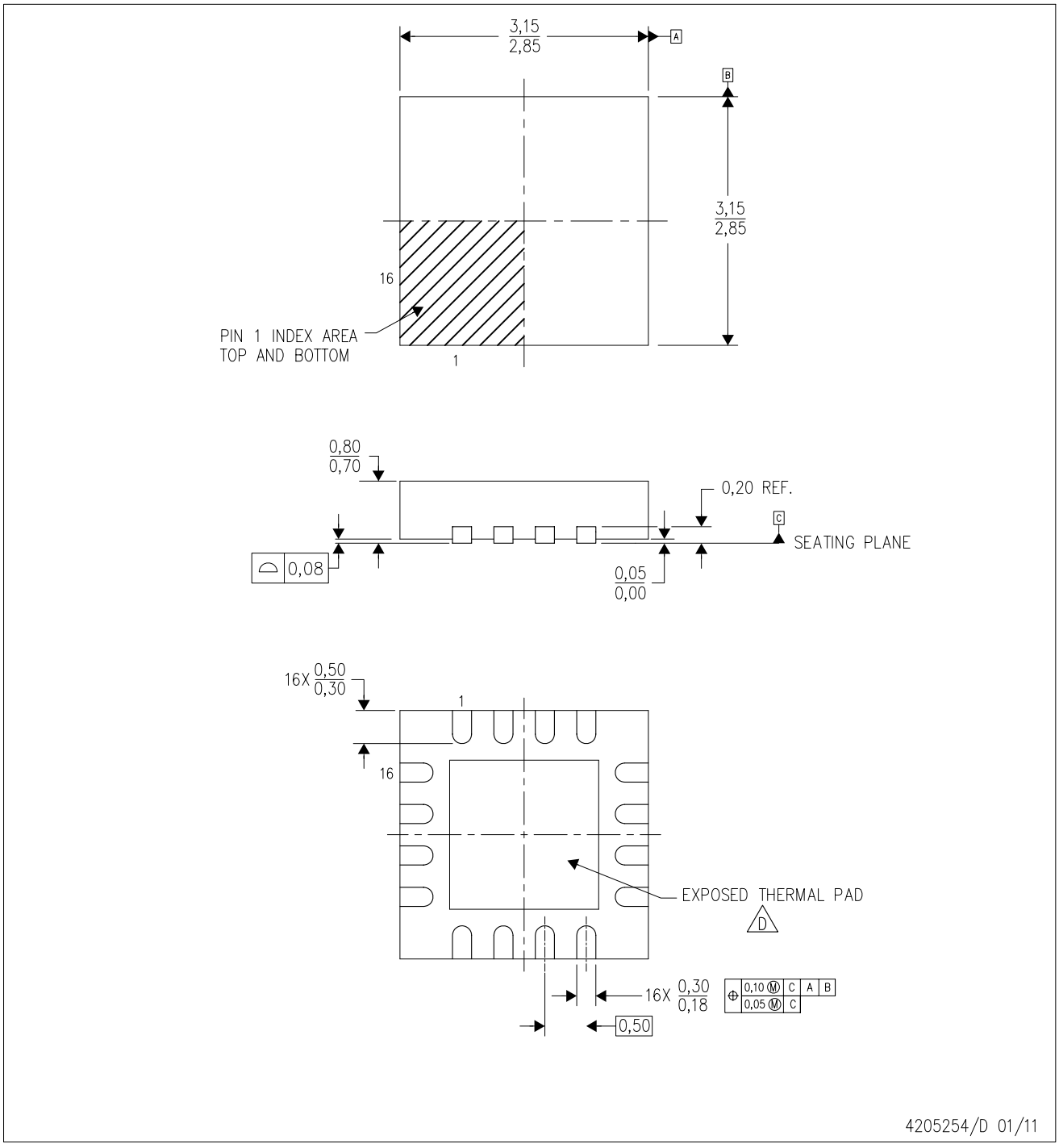
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

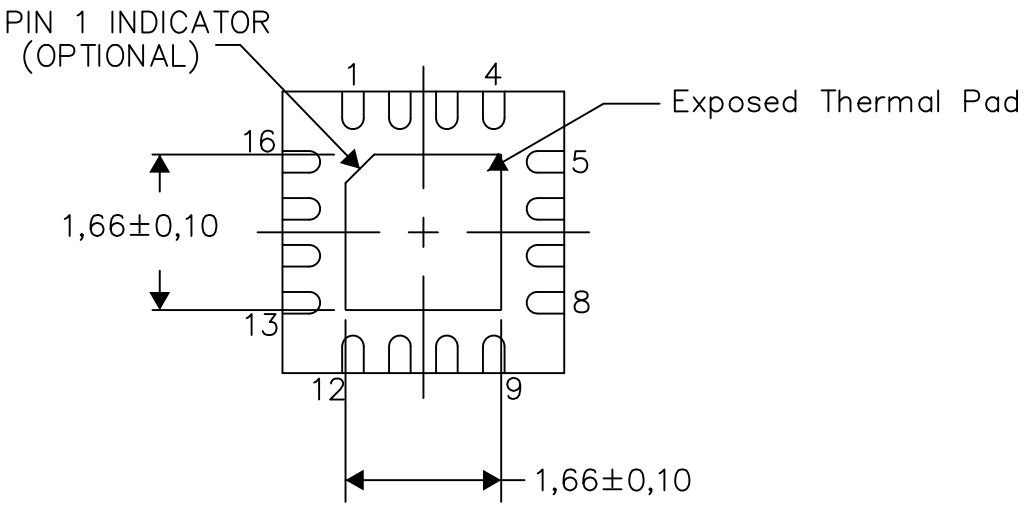
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



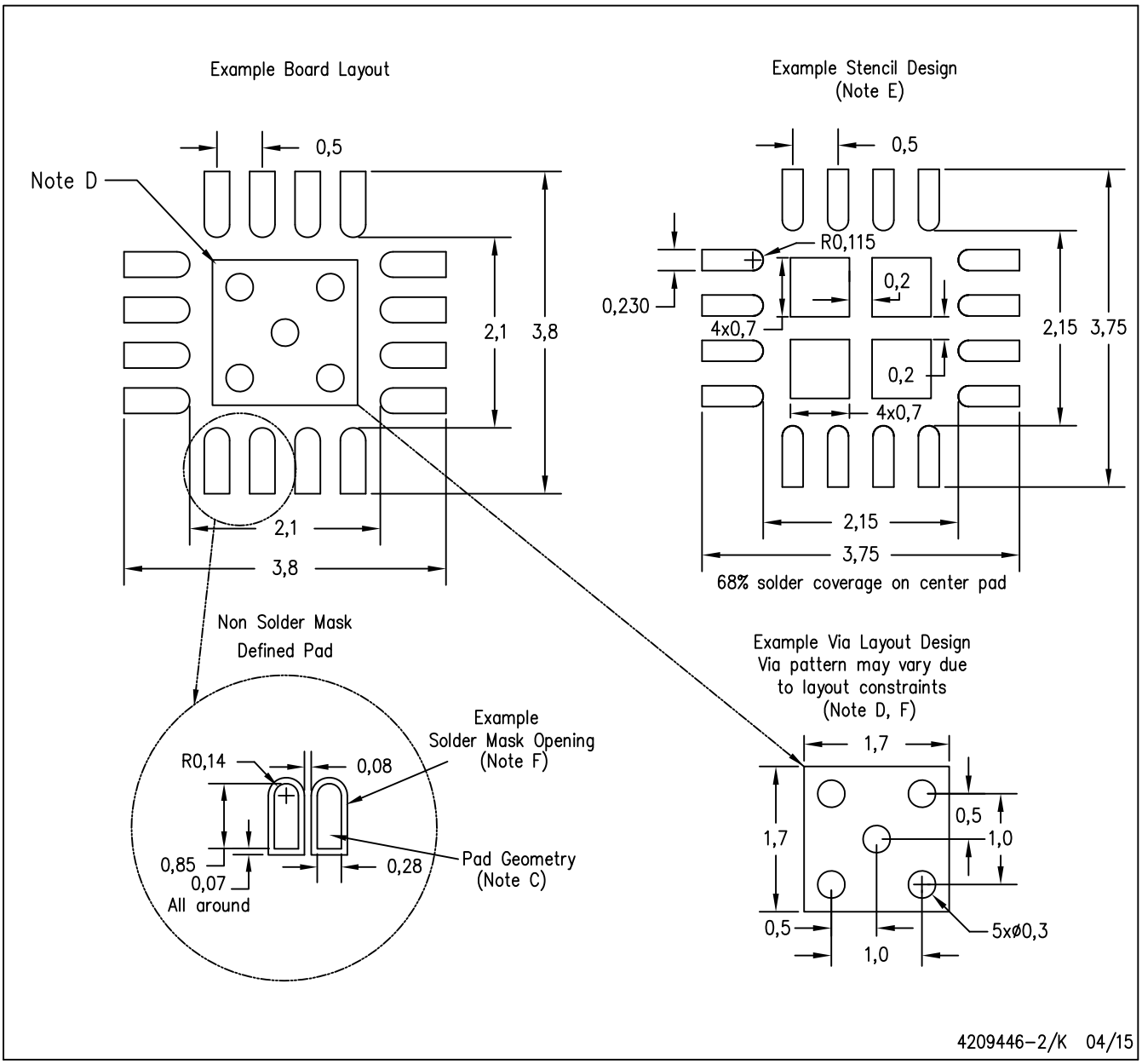
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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