INTEGRATED LDO WITH SWITCHOVER CIRCUIT FOR NOTEBOOK COMPUTERS

FEATURES

- **Wide Input Voltage Range: 4.5 V to 28 V**
- **5-V/3.3-V, 100-mA, LDO Output**
- **Glitch Free Switch Over Circuit**
- ***Always-On* 3.3-V, 5-mA LDO Output for RTC**
- **250 kHz Clock Output for Charge Pump**
- **Thermal Shutdown (Non-latch)**
- **10Ld QFN (DRC) Package**

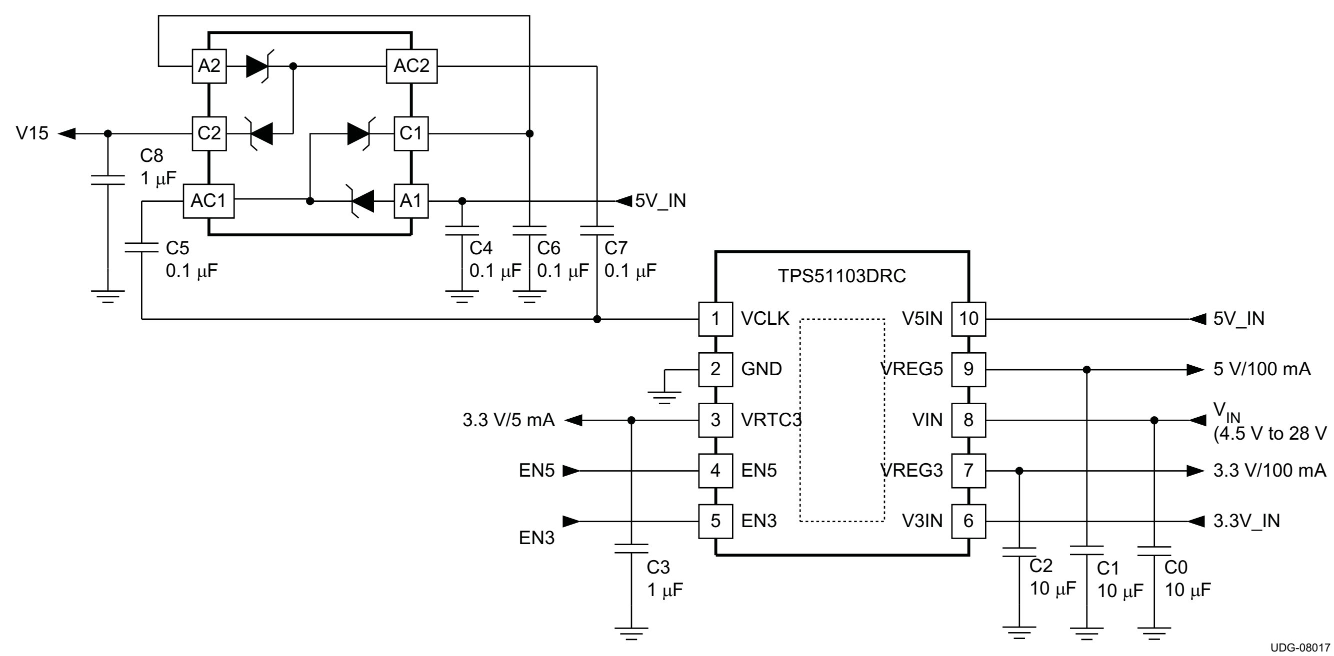
APPLICATIONS

- **Notebook Computers**
- **Mobile Digital Consumer Products**

DESCRIPTION

The TPS51103 integrates three LDOs. The 5-V and 3.3-V LDOs are both rated at 100 mA and also include a glitch-free switch-over feature allowing for optimized battery life. An additional 3.3-V LDO is designed to provide an *always on* power output for the real time clock (RTC). The TPS51103 integrates a clock output to use with an external charge pump. The TPS51103 offers an innovative solution for optimizing the complex and multiple power rails typically found in a Notebook Computer. The TPS51103 is available in the 10-pin QFN package and is specified from –40°C to 85°C.

TYPICAL APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER	TAPE & REEL QUANTITY	ECO-PLAN
–40°C to 85°C	Plastic DRC[1]	TPS51103DRCT	250	Green (RoHS and No Sb/Br)
		TPS51103DRCR	3000	

(1) For the most current package and ordering information, seet he *Package Option Addendum* at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

		VALUE	UNIT
Input voltage range[2]	VIN	–0.3 to 30	V
	EN3, EN5, V3IN	–0.3 to 6	
	V5IN	–0.3 to 6	
	V5IN , (V_{VIN}< 5.7 V)	–0.3 to V_{VIN} + 0.3	
Output voltage range[2]	VRTC3, VCLK, VREG3, VREG5	–0.3 to 6	
Junction temperature, T_J		150	°C
Storage temperature, T_{st}		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS[1]

PACKAGE	POWER RATING BELOW AND AT T_A = 25°C	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
10-pin DRC	1.256 W	12.6 mW/°C	0.502 W

(1) θ_{JA} (junction to air) for high-K board in still air environment is 80°C/W.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Input voltage range	VIN	4.5		28	V
	EN5, EN3, V3IN	–0.1		5.5	
	V5IN	–0.1		5.5	
	V5IN, (V_{VIN}< 5.5 V)	–0.1		V_{VIN}	
Output voltage range	VCLK, VRTC3, VREG3, VREG5	–0.1		5.5	
Operating free-air temperature, T_A		–40		85	°C

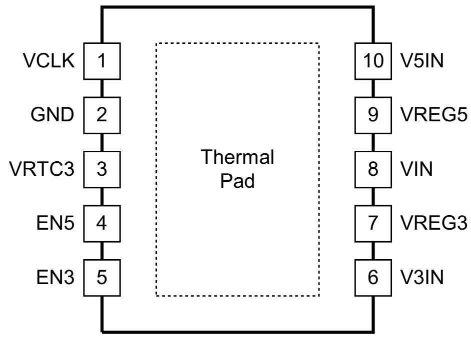
ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V_{VIN}=12 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	VIN supply current	I_{VIN} current, T_A = 25°C, No Load, V_{EN3}=V_{EN5}=5 V, V_{V5IN} = V_{V3IN} = 0 V		35	50	µA
$I_{VINSTBY}$	VIN standby current	I_{VIN} current, T_A = 25°C, No Load, V_{EN3}=V_{EN5}= 0 V, V_{V5IN} = V_{V3IN} = 0 V		7	20	µA
VRTC3 OUTPUT						
V_{VRTC3}	VRTC3 output voltage	I_{VRTC3} = 1 mA, T_A = 25°C	3.27	3.32	3.37	V
		0 A < I_{VRTC3} < 5 mA, 5.5 V < V_{VIN} < 28 V	3.17		3.43	
		0 A < I_{VRTC3} < 5 mA, 4.5 V < V_{VIN} ≤ 5.5 V	3.15		3.43	
I_{VRTC3}	VRTC3 output current	V_{VRTC3} = 2 V	5	10	15	mA
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	V_{V5IN} = 0 V, I_{VREG5} = 1 mA, T_A = 25°C	4.95	5.05	5.15	V
		V_{V5IN} = 0 V, 10 µA < I_{VREG5} < 100 mA, 6.5V < V_{VIN} < 28 V	4.80		5.20	
		V_{V5IN} = 0 V, 0 A ≤ I_{VREG5} < 50 mA, 5.5V < V_{VIN} < 28V	4.75		5.25	
$V_{VREG5DO}$	VREG5 drop out voltage	V_{V5IN} = 0 V, I_{VREG5} = 50 mA, V_{VREG5} = 4.5 V		400	750	mV
I_{VREG5}	VREG5 output current	V_{V5IN} = 0 V, V_{VREG5} = 4.5 V	100	160	250	mA
V_{TH5VSW}	Switch ovethreshold	Turns on	4.45	4.65	4.80	V
		Hysteresis	25	50	75	mV
R_{5VSW}	5V SW $R_{DS(on)}$	V_{V5IN} = 5 V, I_{VREG5} = 100 mA		1		Ω
Td_5	Delay for 5V SW	Turns on		1		ms
VREG3 OUTPUT						
V_{VREG3}	VREG3 output voltage	V_{V3IN} =0 V, I_{VREG3} = 1 mA, T_A = 25°C	3.23	3.33	3.37	V
		V_{V3IN} =0 V, 10 µA < I_{VREG3} < 100 mA, 6.5 V < V_{VIN} < 28 V	3.17		3.43	
		V_{V3IN} = 0V, 0A < I_{VREG3} < 50 mA, 5.5 V < V_{VIN} < 28 V	3.14		3.47	
		V_{V3IN} = 0V, 0A < I_{VREG3} < 50 mA, 4.5 V < V_{VIN} ≤ 5.5 V	3.00		3.47	
I_{VREG3}	VREG3 output current	V_{V3IN}= 0V, V_{VREG3} = 3 V	100	150	250	mA
V_{TH3VSW}	Switchover threshold	Turns on	2.95	3.07	3.17	V
		Hysteresis	20	35	50	mV
R_{3VSW}	3V SW $R_{DS(on)}$	V_{V3IN} = 3.3 V, I_{VREG5} = 100 mA		1.5		Ω
Td_3	Delay for 3V SW	Turns on		1		ms
LOGIC THRESHOLD						
V_{THEN}	EN3, EN5 threshold	Enable		1.05	2.0	V
		Shutdown	0.3	0.7		
$I_{EN3,5}$	EN3, EN5 pulldown current	V_{EN3} = 3 V, V_{EN5} = 3 V	0.5	1.5	3.0	µA
VCLK OUTPUT						
f_{VCLK}	Clock frequency	T_A = 25°C	200	250	320	kHz
R_{VCLK}	Driver impedance	V5IN to VCLK, I_{VCLK} = 10 mA		6	15	Ω
		VCLK to GND, I_{VCLK} = 10 mA		4	15	
V_{THV5IN}	V5IN threshold	VCLK on	1.5	2.0	2.5	V
		Hysteresis		0.3		
THERMAL SHUTDOWN						
TSDN	Thermal SDN threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		20		

(1) Ensured by design. Not production tested.

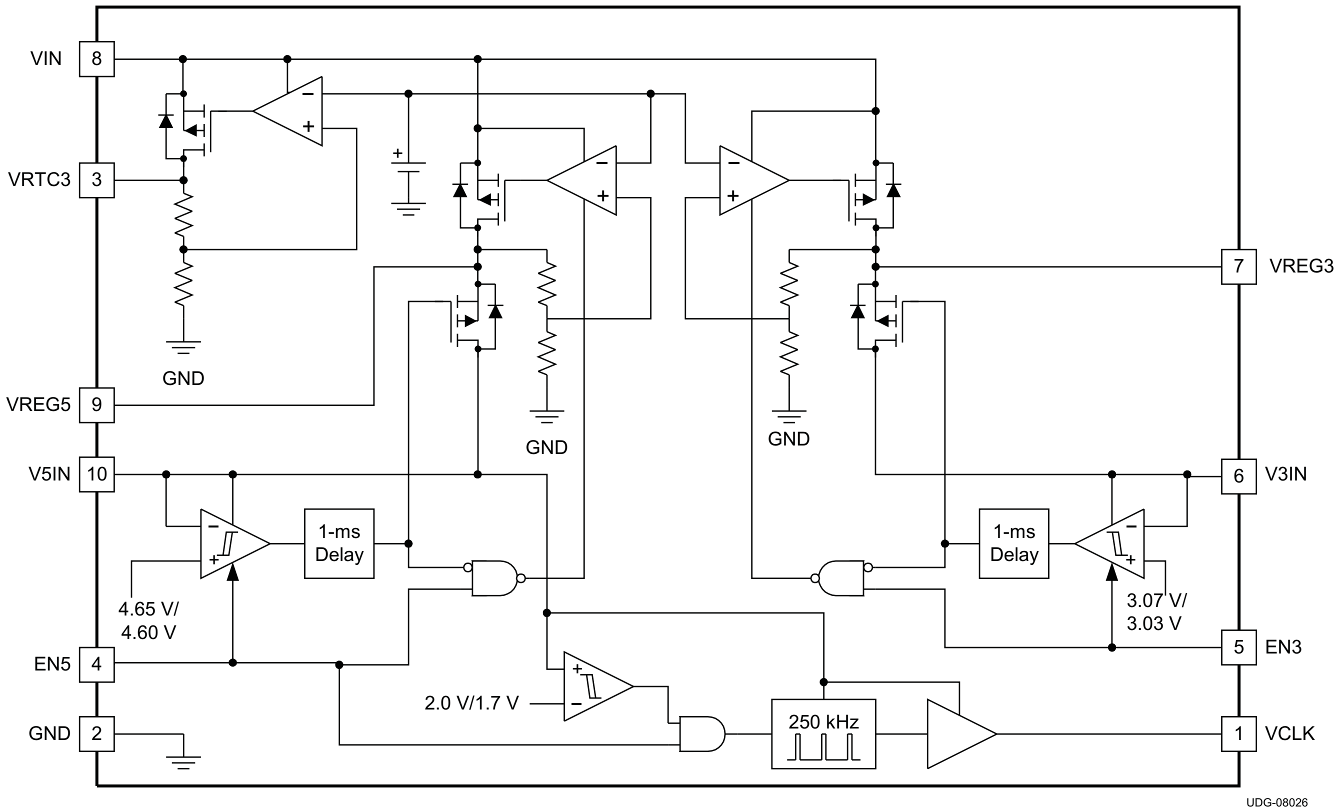
DRC PACKAGE
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN3	5	I	3.3-V LDO enable input.
EN5	4	I	5-V LDO enable input.
GND	2	–	Ground.
V3IN	6	I	3.3-V switchover power supply input. Switchover occurs 1 ms after this input voltage reaches the threshold voltage.
V5IN	10	I	5-V switchover power supply input. Switchover occurs 1 ms after this input voltage reaches to threshold voltage.
VCLK	1	O	50% duty 250-kHz clock output for charge pump power supply.
VIN	8	I	Power supply input for LDOs.
VREG3	7	O	3.3-V 100 mA LDO output.
VREG5	9	O	5-V 100 mA LDO output.
VRTC3	3	O	3.3-V 5 mA always on LDO output for RTC.

FUNCTIONAL BLOCK DIAGRAM



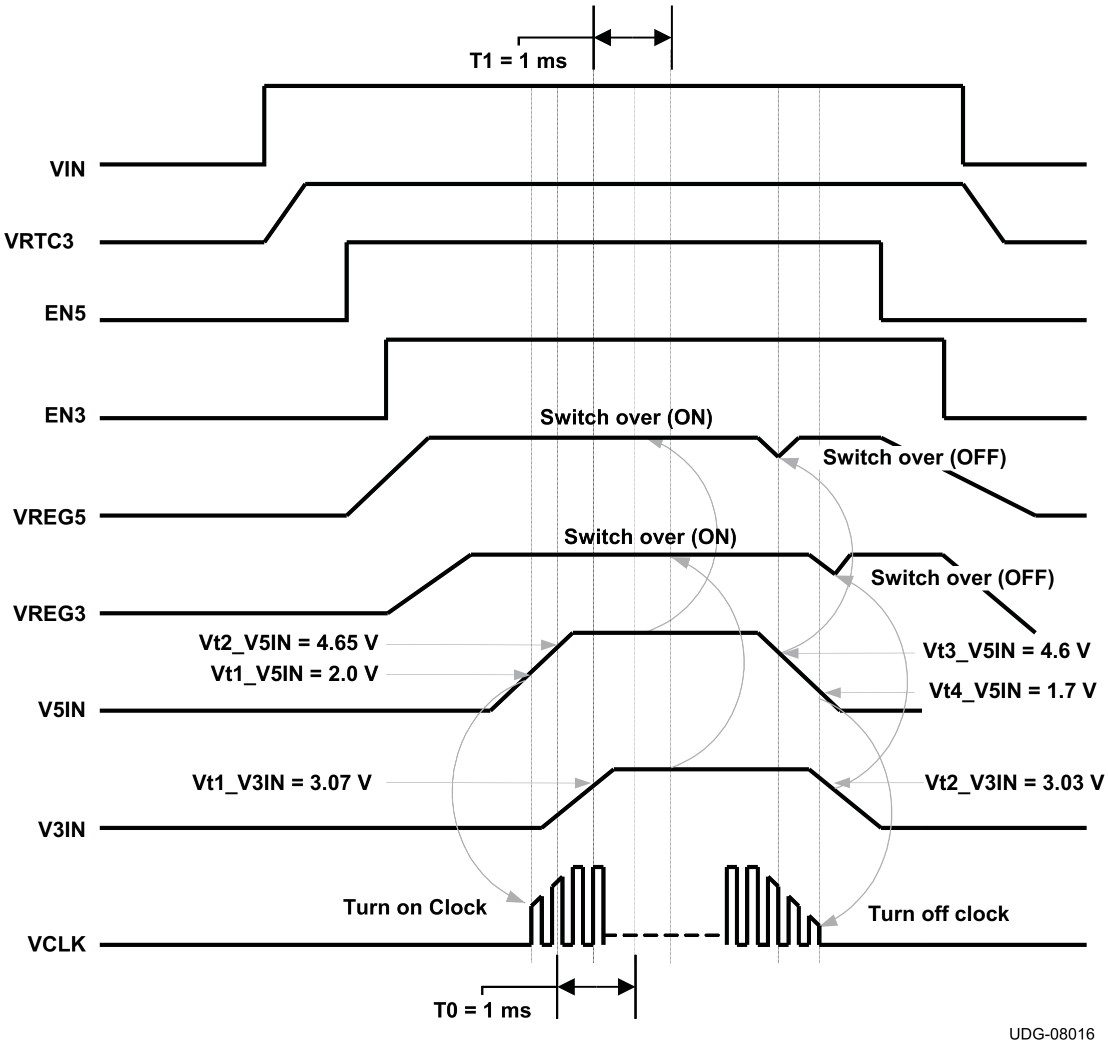


Figure 1. Power Sequencing

DETAILED DESCRIPTION

GENERAL DESCRIPTION

The TPS51103 integrates three LDOs. The VREG5 and VREG3 can each deliver 100 mA of current. The device includes glitch free switch-over circuits which turn off VREG5 and VREG3 LDOs and switch VREG5 and VREG3 to V5IN and V3IN external power inputs respectively when the external high efficiency 5V and 3.3V power rails are available. It improves overall system efficiency and therefore extends battery life. An additional 5-mA VRTC3 LDO is designed to provide an *always on* feature for the real time clock (RTC). A 5-V clock with 50% duty cycle runs at 250 kHz. It can be used as a simple external charge pump driver to generate a 10-V or 15-V low-current voltage rail (see Figure 2). In the notebook application, the 10 V or 15 V created by this circuit could be used to drive an N-channel MOSFET instead of the traditional P-channel MOSFET load switch. The TPS51103 boosts performance and reduce the cost of load switch.

VREG5

When EN5 is asserted high, VREG5 supplies 5 V through an LDO from V_{IN}. Its maximum sourcing current is 100 mA. If EN5 is high and the V5IN voltage becomes higher than 4.65 V, then the VREG5 output is switched over to the V5IN input after a 1-ms delay. In the switched over condition, the LDO is turned off and VREG5 is connected to V5IN through the 1.0-Ω $R_{DS(on)}$ MOSFET switch. When the V5IN voltage becomes lower than 4.6 V, this MOSFET turns off and 5-V LDO is turned back on immediately. A bypass ceramic capacitor is required to stabilize LDO. The recommended value is between 10 µF and 22 µF. Place the bypass capacitor close to the VREG5 pin. When EN5 is asserted low, both the 5-V LDO and switchover circuit are turned off.

VREG3

When EN3 is asserted high, VREG3 supplies 3.3 V through an LDO from VIN. Its maximum sourcing current is 100 mA. If EN3 is high and the V3IN voltage becomes higher than 3.07 V, then the VREG3 output is switched over to the V3IN input after a 1-ms delay. In the switched over condition, LDO is turned off and VREG3 is connected to V3IN through the 1.5-Ω $R_{DS(on)}$ MOSFET switch. When the V3IN voltage becomes lower than 3.03 V, this MOSFET turns off and the 3.3-V LDO is turned back on immediately. A bypass ceramic capacitor is needed to stabilize LDO, recommended value is between 10 µF and 22 µF. Place the bypass capacitor close to the VREG3 pin. When EN3 is asserted low, both the 3.3-V LDO and the switchover circuit are turned off.

VRTC3

This 3.3-V low-current auxiliary power source is typically used for the system's RTC bias voltage. It is powered on after VIN is applied. A ceramic capacitor with a value between 1 µF and 2.2 µF placed close to the VRTC3 pin is needed to stabilize the LDO.

VCLK OUTPUT

When the V5IN voltage becomes higher than 2.0 V, the internal 250-kHz clock turns on and the VCLK pin outputs a 50% duty-cycle clock signal. The voltage swing of VCLK is equal to the GND to V5IN voltage

THERMAL SHUTDOWN

When the device temperature exceeds the internal threshold value (typically 150C) the TPS51103 shuts off the VREG3, VREG5 and VCLK outputs. This is a non-latch protection.

THERMAL DESIGN

The thermal performance greatly depends on the printed circuit board (PCB) layout. The TPS51103 is housed in a thermally-enhanced PowerPAD™ package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to ground via thermal land on the PCB. This ground trace acts as a heatsink and a heat spreader. For further information regarding the PowerPAD™ package and the recommended board layout, refer to the PowerPAD™ package application note (SLMA002). This document is available at www.ti.com.

LAYOUT GUIDELINES

Consider the following points before starting the TPS51103 layout design.

- The input bypass capacitor for VIN should be placed as close as possible to the pin with short and wide connection.
- The output capacitors for VREG5, VREG3 and VRTC3 should be placed close to the pins with short and wide connections.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. Wide copper traces connected to the thermal land help to dissipate heat. Numerous 0.33 mm diameter vias are connected from the thermal land to the internal and/or solder-side system ground plane(s) can also be used to help dissipation.
- The GND pin, output capacitors for VREG5, VREG3 and VRTC3 should be connected to the internal and/or solder-side system ground plane(s) with multiple vias. Use as many vias as possible to reduce the impedance between them and the system ground plane.

APPLICATION INFORMATION

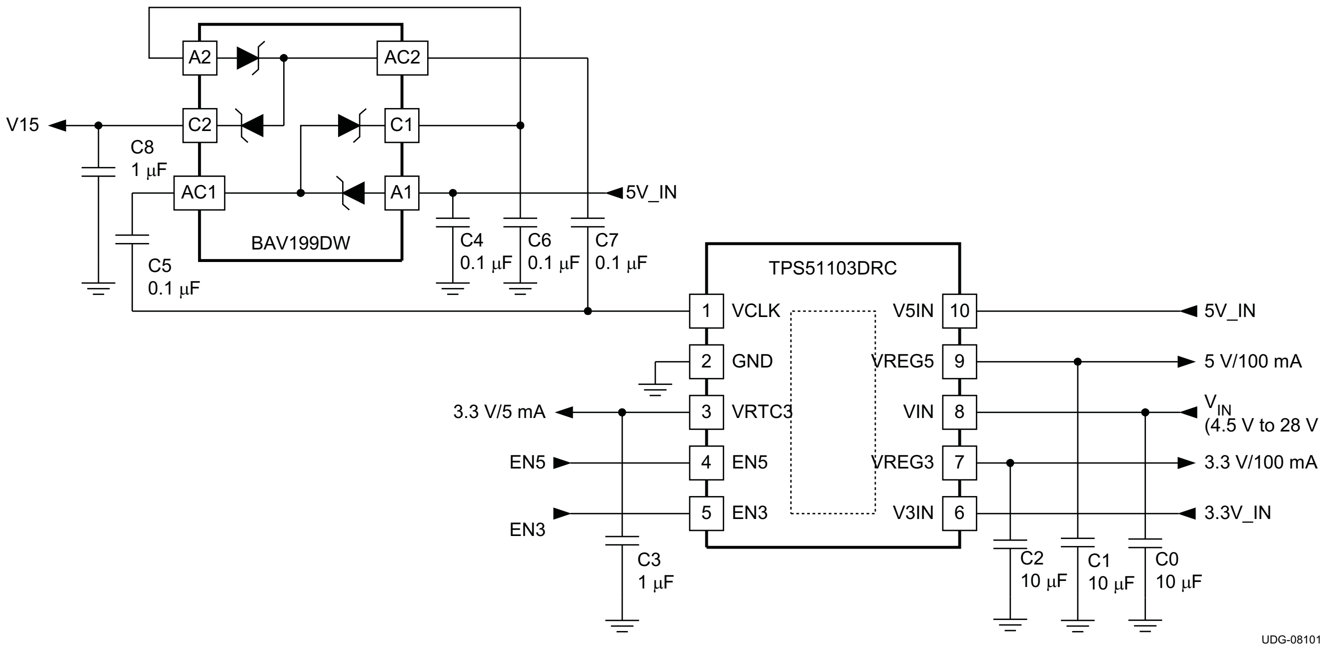


Figure 2. Typical Application

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

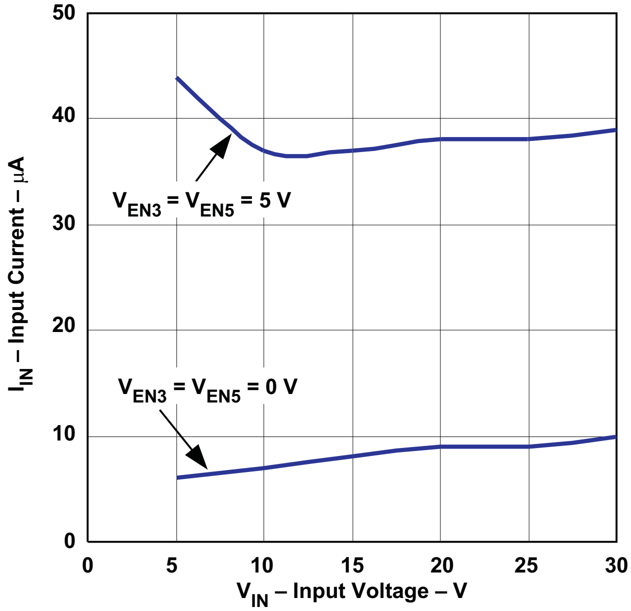


Figure 3.

VREG3 LDO OUTPUT VOLTAGE
vs
LDO OUTPUT CURRENT

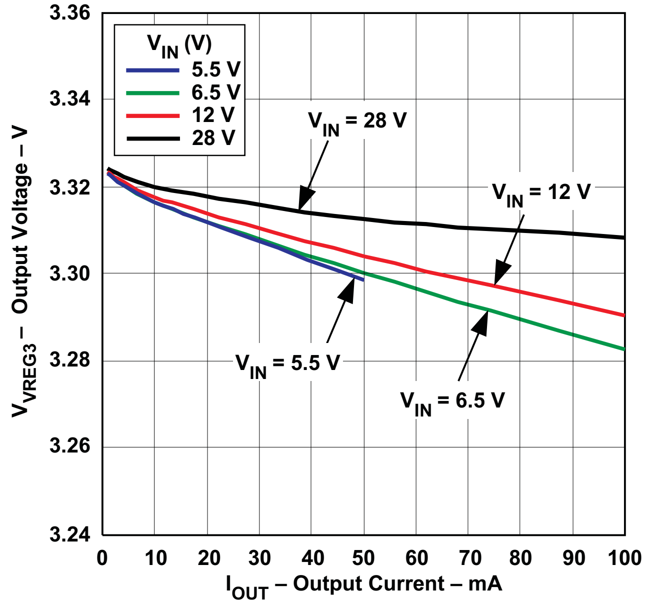


Figure 4.

VREG5 LDO OUTPUT VOLTAGE
vs
LDO OUTPUT CURRENT

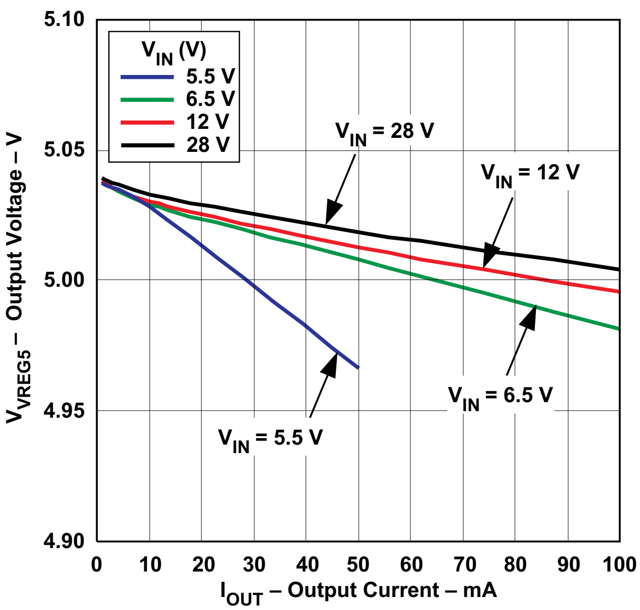


Figure 5.

CHARGE PUMP OUTPUT VOLTAGE
vs
CHARGE PUMP OUTPUT CURRENT

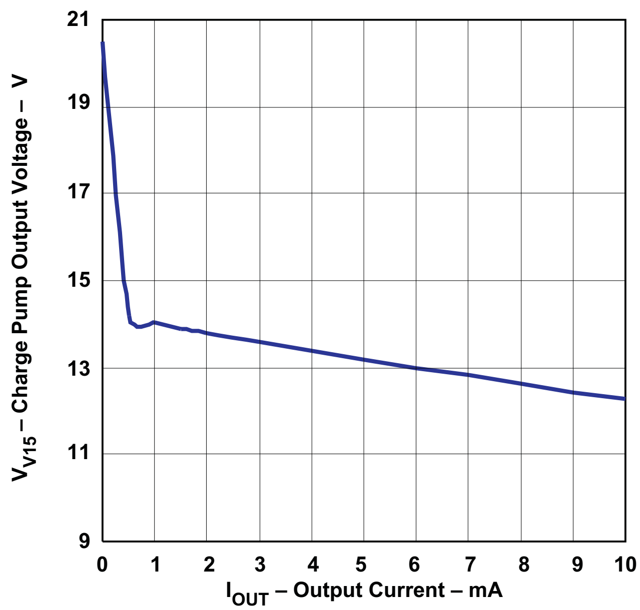


Figure 6.

TYPICAL CHARACTERISTICS (continued)

ALWAYS ON OUTPUT VOLTAGE
vs
ALWAYS ON OUTPUT CURRENT

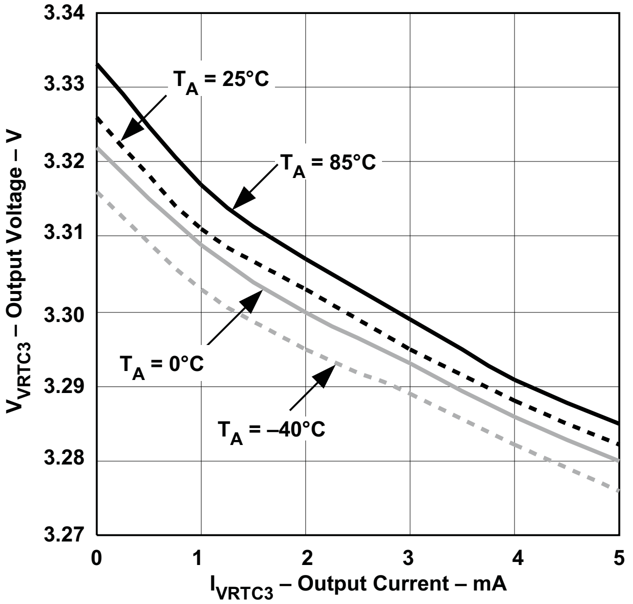


Figure 7.

VREG5 SWITCHOVER OUTPUT VOLTAGE
vs
VREG5 SWITCHOVER OUTPUT CURRENT

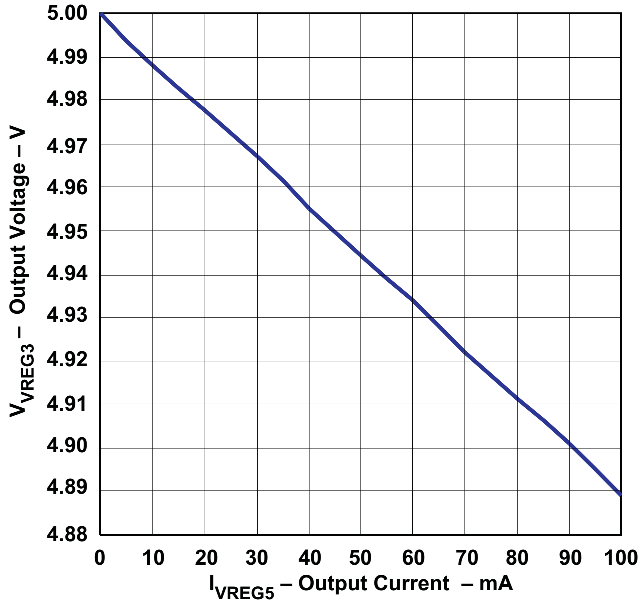


Figure 8.

VREG3 SWITCHOVER OUTPUT VOLTAGE
vs
VREG3 SWITCHOVER OUTPUT VOLTAGE

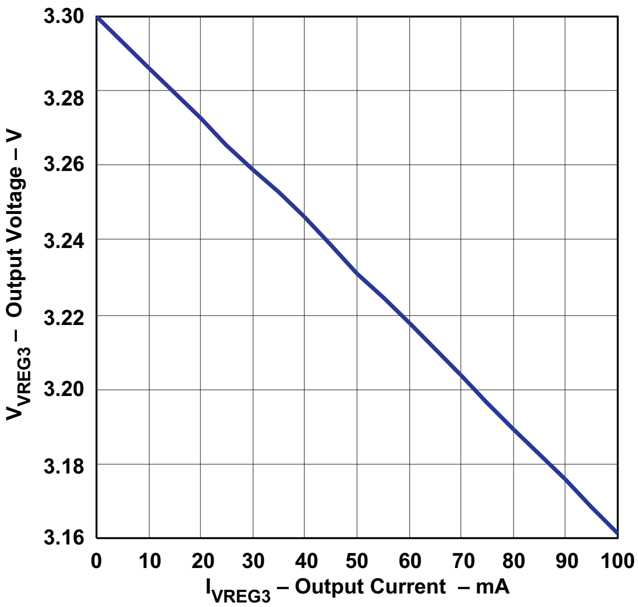


Figure 9.

INPUT CURRENT
vs
JUNCTION TEMPERATURE

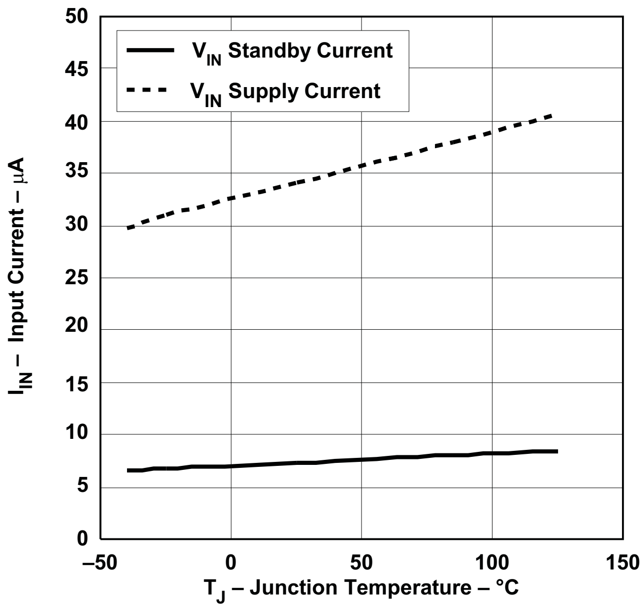


Figure 10.

TYPICAL CHARACTERISTICS (continued)

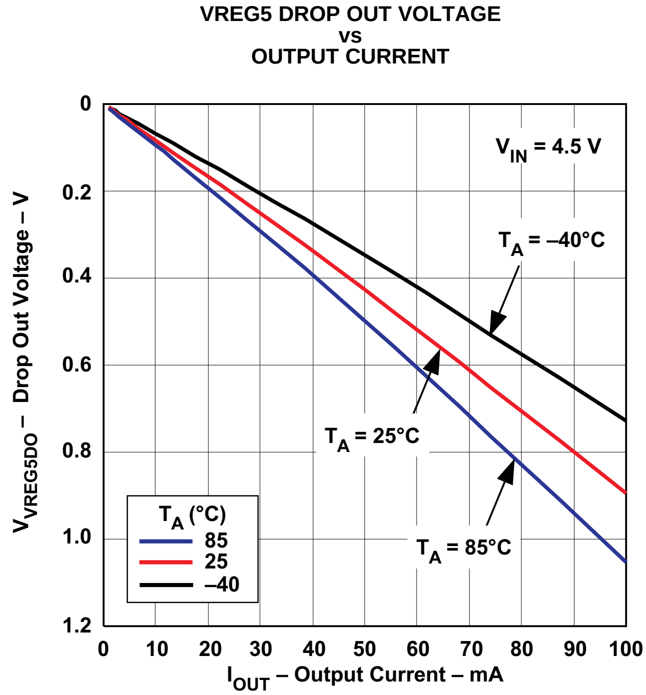
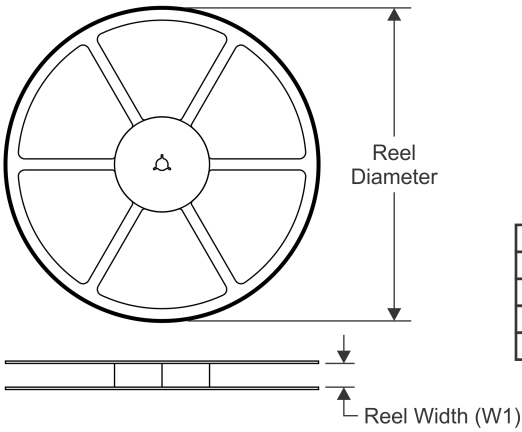


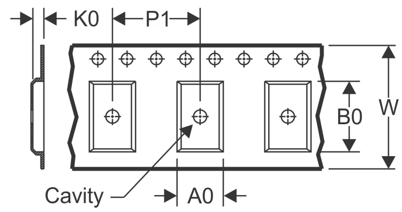
Figure 11.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

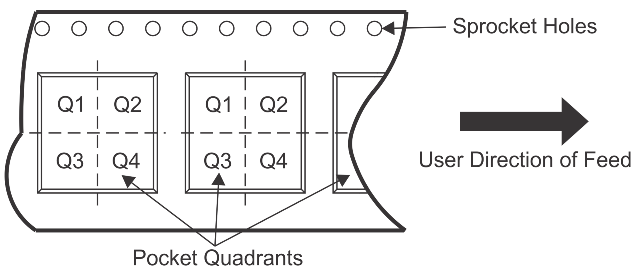


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

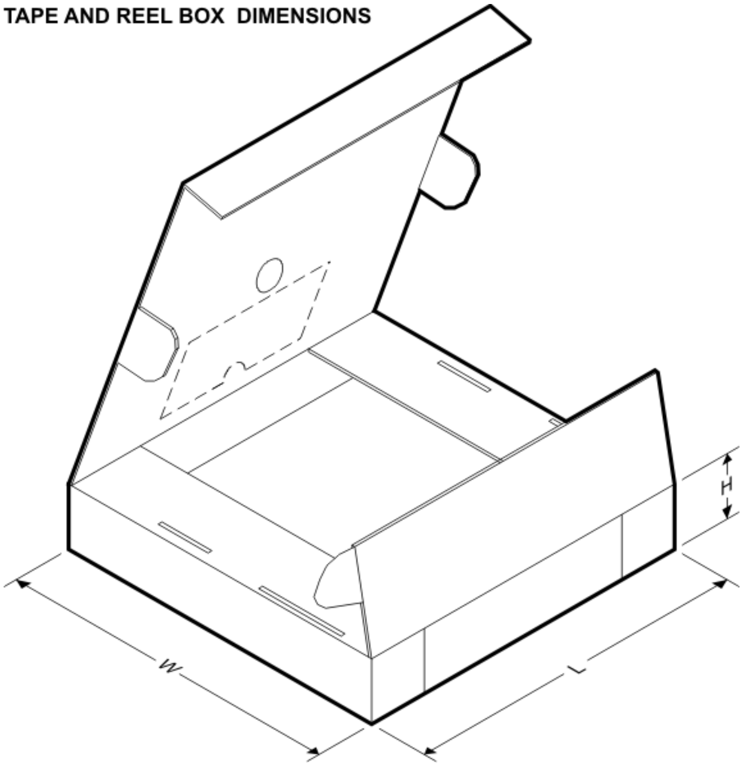
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51103DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51103DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

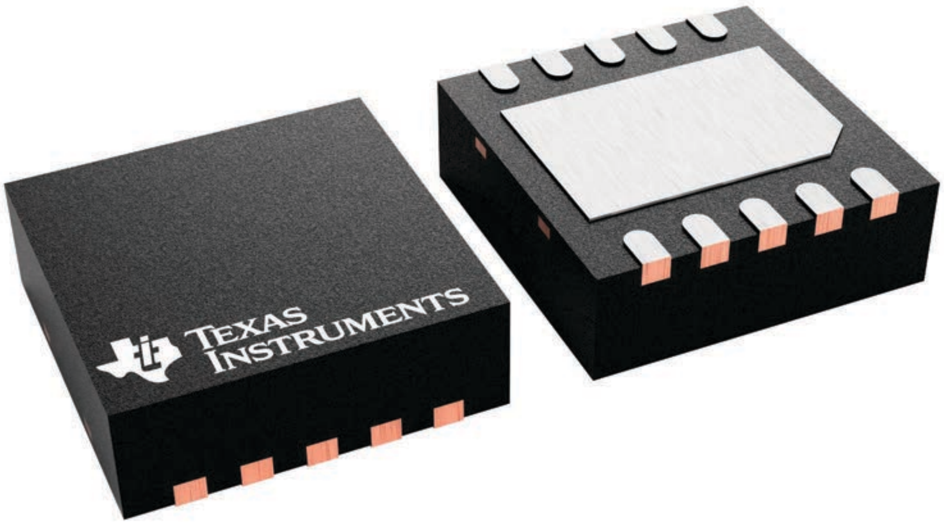
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51103DRCR	VSON	DRC	10	3000	853.0	449.0	35.0
TPS51103DRCT	VSON	DRC	10	250	210.0	185.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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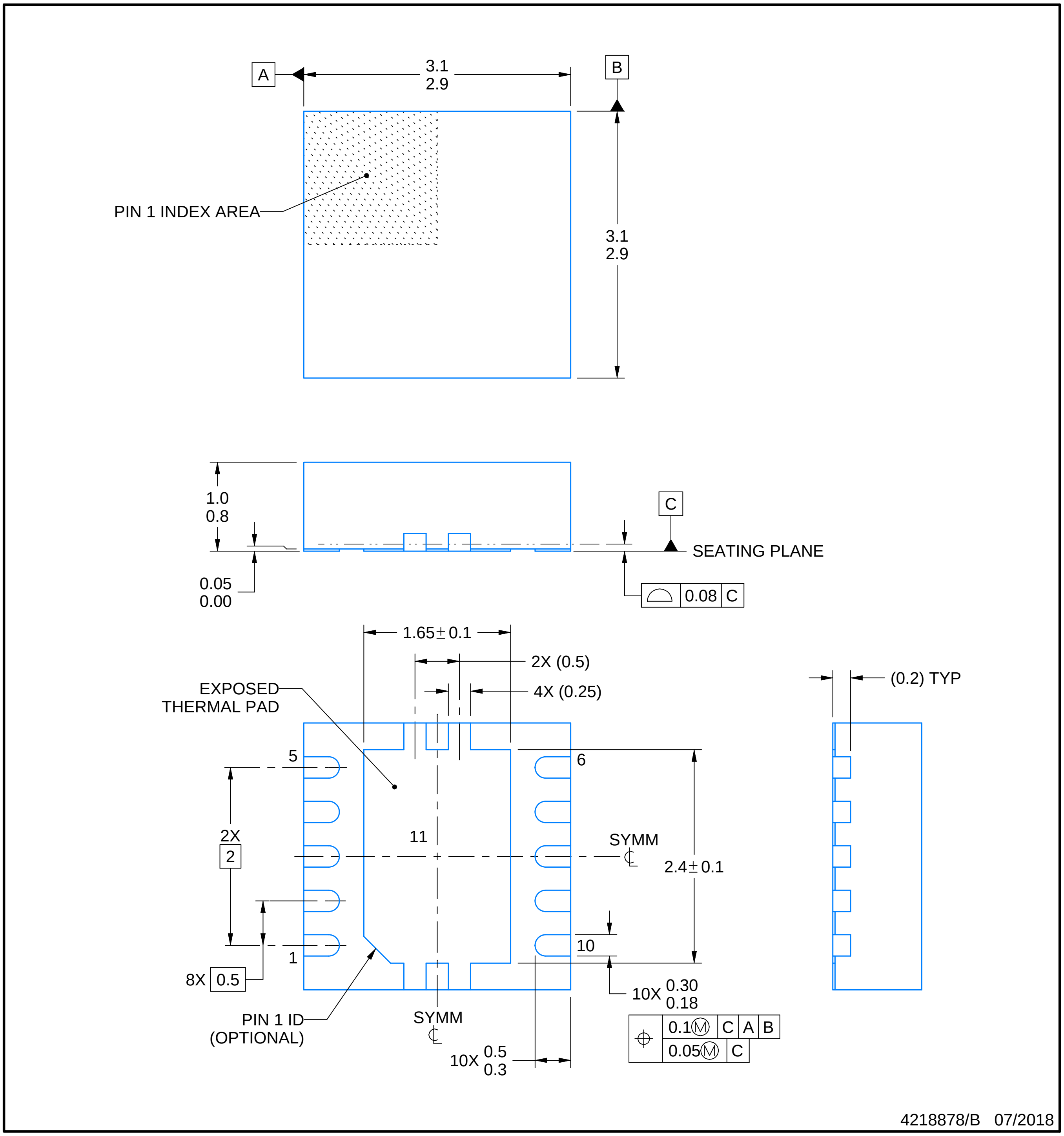
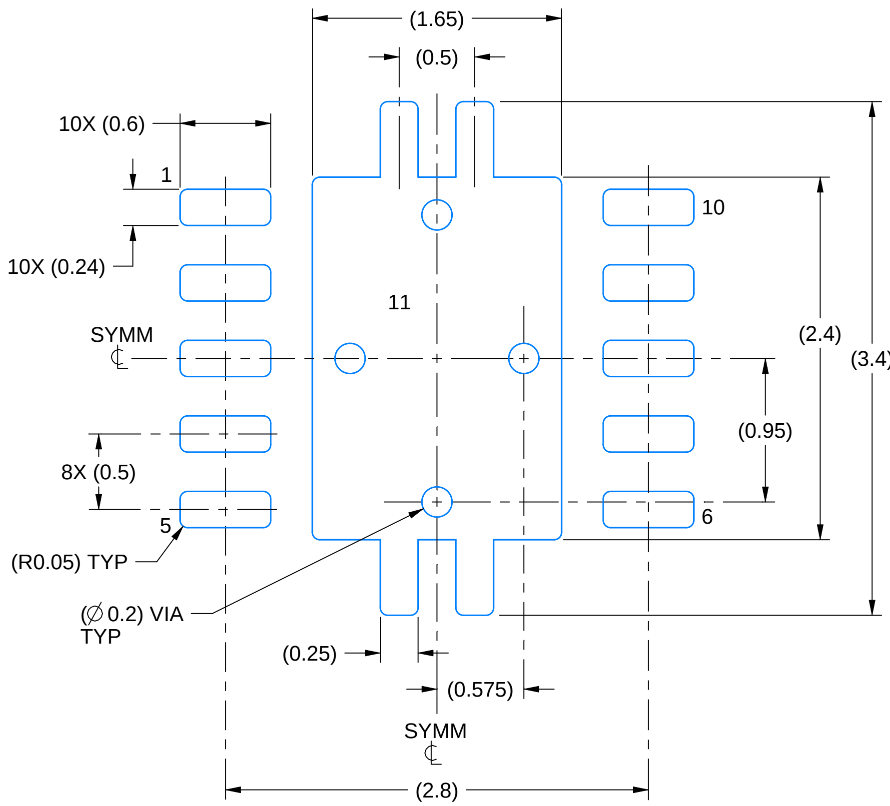
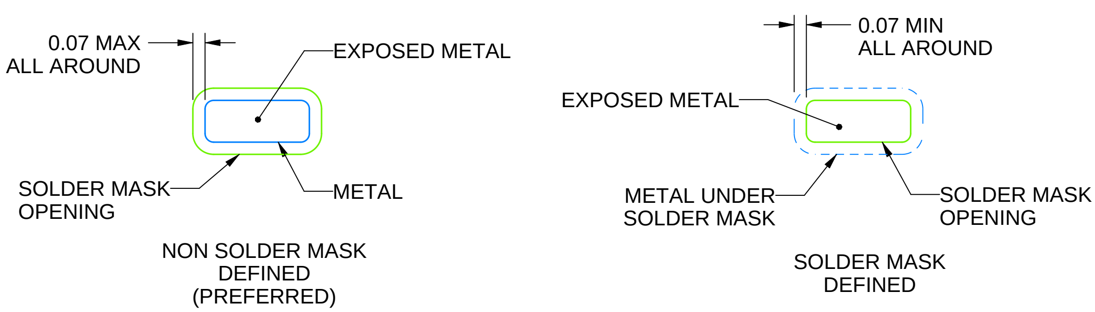


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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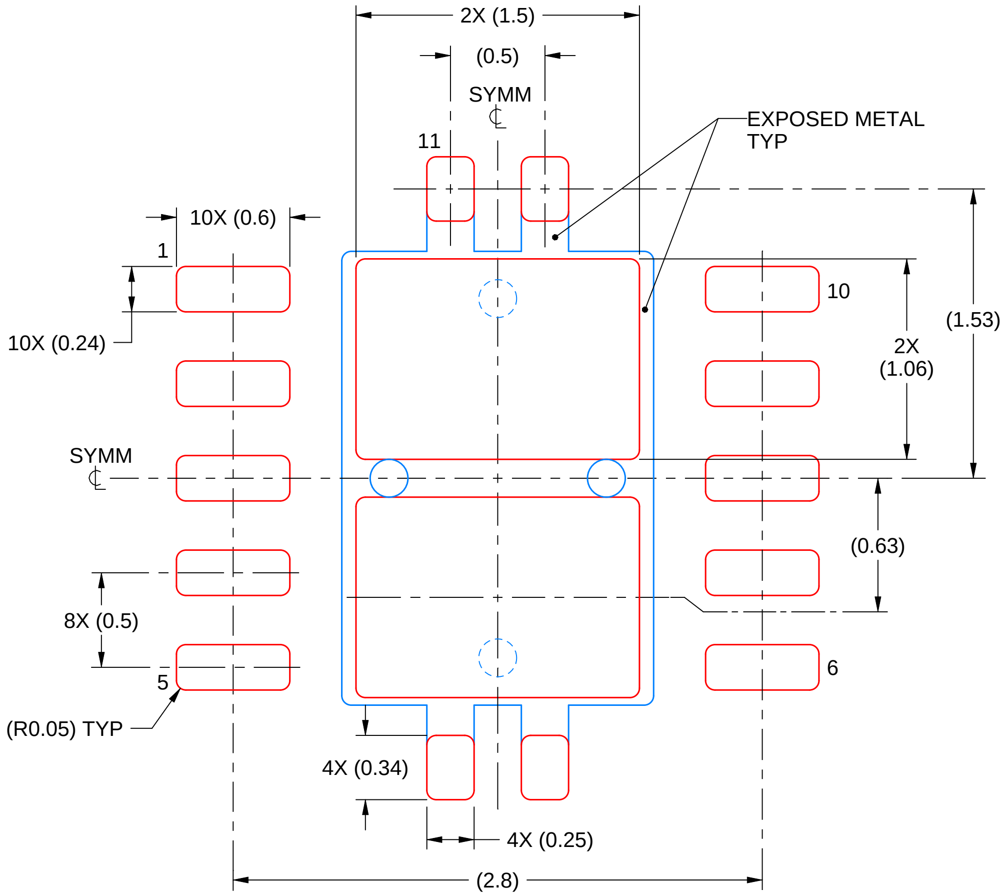
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265