Low Dropout 1 Ampere Linear Regulator Family

FEATURES

- Precision Positive Linear Voltage Regulation
- 0.5V Dropout at 1A
- Guaranteed Reverse Input/ Output Voltage Isolation with Low Leakage
- Low Quiescent Current Irrespective of Load
- Adjustable Output Voltage Version
- Fixed Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of 3% • V_{IN} • Current Limit
- Remote Load Voltage for Accurate Load Regulation

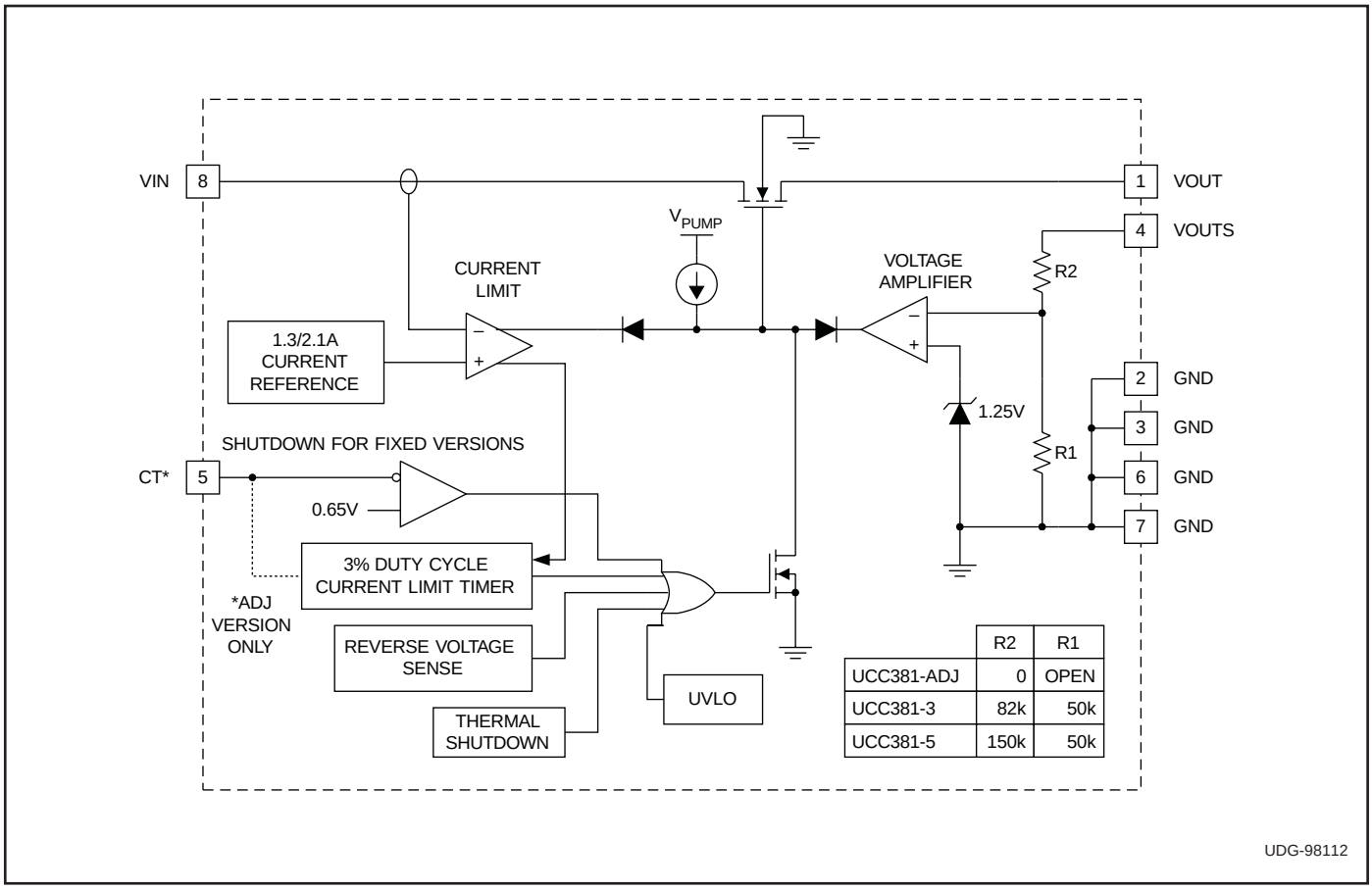
DESCRIPTION

The UCC381-3/-5/-ADJ family of positive linear series pass regulators is tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC381 will pass 1A while requiring only 0.5V of input voltage headroom. Dropout voltage decreases linearly with output current, so that dropout at 200mA is less than 100mV. Quiescent current is always less than 650µA. To prevent reverse current conduction, on-chip circuitry limits the minimum forward voltage to typically 50mV. Once the forward voltage limit is reached, the input-output differential voltage is maintained as the input voltage drops until undervoltage lockout disables the regulator.

UCC381-3 and UCC381-5 versions have on-chip resistor networks preset to regulate either 3.3V or 5.0V, respectively. Furthermore, remote sensing of the load voltage is possible by connecting the VOUTS pin directly at the load. The output voltage is then regulated to 1.5% at room temperature and better than 2.5% over temperature. The UCC381-ADJ version has a regulated output voltage programmed by an external user-definable resistor ratio.

(continued)

BLOCK DIAGRAM



	R2	R1
UCC381-ADJ	0	OPEN
UCC381-3	82k	50k
UCC381-5	150k	50k

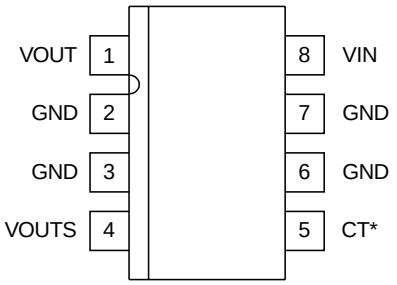
ABSOLUTE MAXIMUM RATINGS

VIN. 9V
CT . . . . . –0.3 to 3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



** ADJ version only*

DESCRIPTION (cont.)

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a T_{ON} delay. The device then stays off for a period, T_{OFF}, that is 32 times the T_{ON} delay. The device then begins pulsing on and off at the T_{ON} /(T_{ON}+T_{OFF}) duty cycle of 3%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. On the fixed output versions of the device T_{ON} is fixed at 400µs – a guaranteed minimum. On the adjustable version an external capacitor sets the on time. The off time is always 32 times T_{ON}.

The UCC381 can be shutdown to 25µA (max) by pulling the CT pin low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

The UCC281 series is specified for operation over the industrial range of –40°C to +85°C, and the UCC381 series is specified from 0°C to +70°C. These devices are available in the 8 pin DP surface mount power package. For other packaging options consult the factory.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC381-X series and –40°C to +85°C for the UCC283-X series, V_{IN} = V_{OUT} + 1.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF. C_T = 1500pF for the UCC381-ADJ version and V_{OUT} set to 5V. T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC381-5 Fixed 5V, 1A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	V_{IN} = 5.15V to 9V		1	3	mV
Load Regulation	I_{OUT} = 0mA to 1A		2	5	mV
Drop Out Voltage, V_{IN} – V_{OUT}	I_{OUT} = 1A, V_{OUT} = 4.85V, TA < 85°C		0.5	0.6	V
	I_{OUT} = 200mA, V_{OUT} = 4.85V, TA < 85°C		100	200	mV
Peak Current Limit	V_{OUT} = 0V		2	3.5	A
Overcurrent Threshold		1		1.8	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{OUT} = 0V	400	750	1600	µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	V_{IN} = 9V		10	25	µA
Shutdown Threshold	At C_T Input	0.25	0.65		V
Reverse Leakage Current	1V < V_{IN} < V_{OUT}, V_{OUT} < 5.1V, at V_{OUT}			75	µA
UVLO Threshold	V_{IN} where V_{OUT} passes current	2.5	2.8	3.0	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC381-X series and –40°C to +85°C for the UCC283-X series, $V_{IN} = V_{OUT} + 1.5V$, I_{OUT} = 0mA, C_{OUT} = 2.2µF. C_T = 1500pF for the UCC381-ADJ version and V_{OUT} set to 5V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC381-3 Fixed 3.3V, 1A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	V
	Over Temperature	3.22		3.38	V
Line Regulation	V_{IN} = 3.45V to 9V		1	3	mV
Load Regulation	I_{OUT} = 0mA to 1A		2	5	mV
Dropout Voltage, V_{IN} - V_{OUT}	I_{OUT} = 1A, V_{OUT} = 3.15V, T_A < 85°C		0.6	0.8	V
	I_{OUT} = 200mA, V_{OUT} = 3.15V, T_A < 85°C		100	200	mV
Peak Current Limit	V_{OUT} = 0V		2	3.5	A
Overcurrent Threshold		1		1.8	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{OUT} = 0V	400	750	1600	µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	V_{IN} = 9V		10	25	µA
Shutdown Threshold	At C_T Input	0.25	0.65		V
Reverse Leakage Current	1V < V_{IN} < V_{OUT}, V_{OUT} < 3.35V, at V_{OUT}			75	µA
UVLO Threshold	V_{IN} where V_{OUT} passes current	2.5	2.8	3.0	V
UCC381-ADJ Adjustable Output, 1A Family					
Regulating Voltage at ADJ Input	T_J = 25°C	1.23	1.25	1.27	V
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	$V_{IN} = V_{OUT}$ + 150mV to 9V		1	3	mV
Load Regulation, at ADJ Input	I_{OUT} = 0mA to 1A		2	5	mV
Dropout Voltage, V_{IN} - V_{OUT}	I_{OUT} = 1A, V_{OUT} = 4.85V		0.5	0.6	V
	I_{OUT} = 200mA, V_{OUT} = 4.85V		100	200	mV
Peak Current Limit	V_{OUT} = 0V		2	3.5	A
Overcurrent Threshold		1		1.8	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{OUT} = 0V, C_T = 1500pF	400	1000	1600	µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	V_{IN} = 9V		10	25	µA
Shutdown Threshold	At C_T Input	0.25	0.65		V
Reverse Leakage Current	1V < V_{IN} < V_{OUT}, V_{OUT} < 9V, at V_{OUT}			100	µA
Bias Current at ADJ Input			100	250	nA
UVLO Threshold	V_{IN} where V_{OUT} passes current	2.5	2.8	3.0	V

PIN DESCRIPTIONS

CT: For UCC381-3 and UCC381-5 versions, this is the shutdown pin which, when pulled low, turns off the regulator output and puts the device in a low current state. For the UCC381-ADJ version, a capacitor is required between the CT pin and GND to set the T_{ON} time during overcurrent according to the following (typical) equation:

$$T_{ON} = 660{,}000 \bullet C_{CT}$$

GND: All voltages are measured with respect to this pin. This is the low noise ground reference input for regulation. The output decoupling capacitor should be tied to PIN 7.

VIN: Positive supply input for the regulator. Bypass this pin to GND with at least 1µF of low ESR, ESL capacitance if the source is located further than 1 inch from the device.

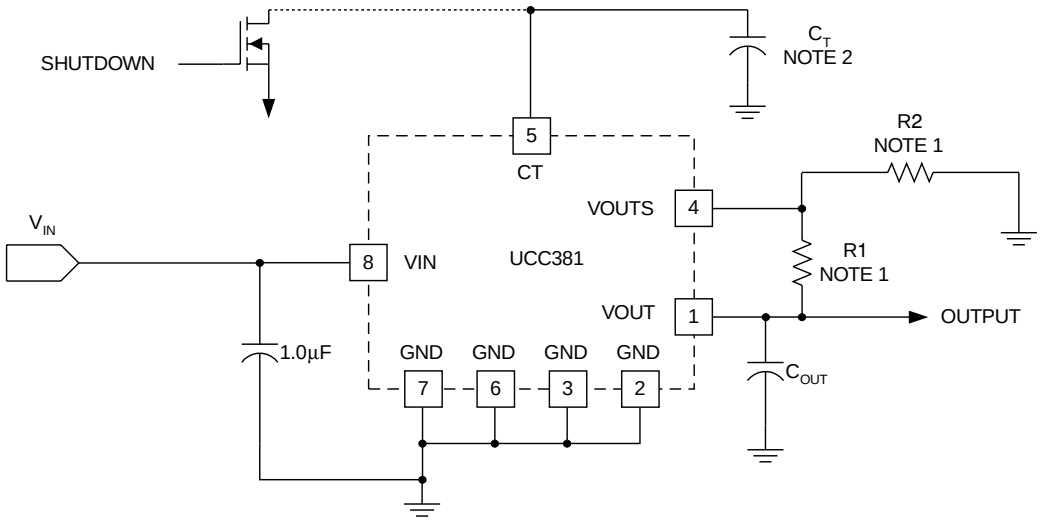
VOUT: Output for regulator. The regulator does not require a minimum output capacitor for stability. Choose the appropriate size capacitor for the application with respect to the required transient loading. For example, if the load is very dynamic, a large capacitor will smooth out the response to load steps.

VOUTS: Feedback for regulator sensing of the output voltage. For loads which are a considerable resistive distance from the VOUT pin, the VOUTS pin can be used to move the resistance into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path. For local regulation, merely connect this pin directly to the VOUT pin. For the UCC381-ADJ version, the output voltage can be set by two external resistors according to the following relationship:

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R2}{R1}\right)$$

where R1 is a resistor connected between VOUT and VOUTS and R2 is a resistor connected between VOUTS and GND.

TYPICAL APPLICATION CIRCUIT



Note 1: R1 and R2 for adjustable version only. For 3.3V and 5V versions connect VOUT to VOUTS. See Pin Descriptions.

Note 2: C_T timing capacitor is for adjustable version only. For 3.3V and 5V versions, the CT pin is used to enable or shutdown the part. See Pin Descriptions.

APPLICATION INFORMATION

Overview

The UCC381 family of low dropout linear (LDO) regulators provide a regulated output voltage for applications with up to 1A of load current. The regulator features a low dropout voltage and short circuit protection, making their use ideal for demanding high current applications requiring fault tolerance.

Short Circuit Protection

The UCC381 provides unique short circuit protection circuitry that reduces power dissipation during a fault. When an overload situation is detected, the device enters a pulsed mode of operation at 3% duty cycle reducing the heat sink requirements during a fault. The UCC381 has two current thresholds that determine its behavior during a fault as shown in Fig. 1.

When the regulator current exceeds the **Overcurrent Threshold** for a period longer than the T_{ON}, the UCC381 shuts off for a period (T_{OFF}) which is 32 times T_{ON}. If the short circuit current exceeds the **Peak Current Limit**, the regulator limits the current to peak current limit during the T_{ON} period. The peak current limit is nominally 1 Amp greater than the overcurrent threshold. The regulator will continue in pulsed mode until the fault is cleared as illustrated in Fig. 1.

A capacitive load on the regulator's output will appear as a short circuit during start-up. If the capacitance is too large, the output voltage will not come into regulation during the initial T_{ON} period and the UCC381 will enter pulsed mode operation. The peak current limit, T_{ON} period, and load characteristics determine the maximum value of output capacitor that can be charged. For a constant current load the maximum output capacitance is given as follows:

$$C_{OUT(\max)} = \left(I_{CL} - I_{LOAD}\right) \bullet \frac{T_{ON}}{V_{OUT}} \; Farads \tag{1}$$

For worst case calculations the minimum values of on time (T_{ON}) and peak current limit (I_{CL}) should be used. The adjustable version allows the T_{ON} time to be adjusted with a capacitor on the CT pin:

$$T_{ON(adj)}\left(\mu\sec\right) = 660{,}000 \bullet C\left(\mu Farads\right) \tag{2}$$

For a resistive load (R_{LOAD}) the maximum output capacitor can be estimated from:

$$C_{OUT(\max)} = \frac{T_{ON}}{R_{LOAD} \bullet \ell n\left(\frac{1}{1-\left(\frac{V_{OUT}}{I_{CL} \bullet R_{LOAD}}\right)}\right)} \; Farads \tag{3}$$

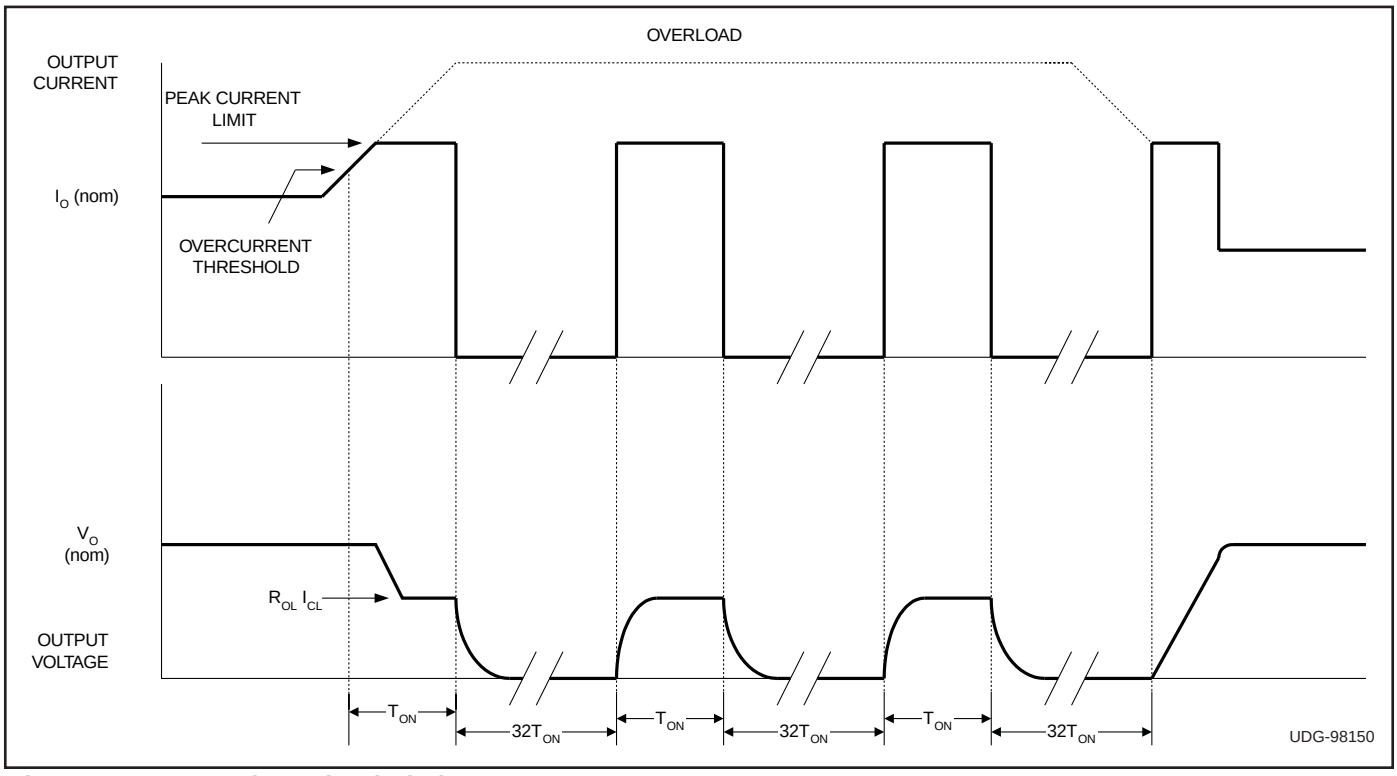


Figure 1. UCC381 short circuit timing.

APPLICATION INFORMATION (cont.)

Dropout Performance

Referring to the Block Diagram, the dropout voltage of the UCC381 is equal to the minimum voltage drop (V_{IN} to V_{OUT}) across the N-Channel MOSFET. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, as well as temperature. The UCC381 achieves a low $Rds_{(ON)}$ through the use of an internal charge-pump (V_{PUMP}) that drives the MOSFET gate. Fig. 2 depicts typical dropout voltages versus load current for the 3.3V and 5V versions of the part, as well as the adjustable version programmed to 3.0V.

Fig. 3 depicts the typical dropout performance of the adjustable version with various output voltages and load currents.

Operating temperatures effect the RDS(ON) and dropout voltage of the UCC381. Fig. 4 graphs the typical dropout for the 3.3V and 5V versions with a 3A load over temperature.

Voltage Programming

Referring to the Typical Application Circuit, the output voltage for the adjustable version is externally programmed through a resistive divider at the VOUTS pin as shown.

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R2}{R1}\right) Volts \quad (4)$$

For the fixed Voltage versions the resistive divider is internally set, and the VOUTS pin should be connected to the VOUT pin. The maximum programmed output voltage for the adjustable part is constrained by the 9V absolute rating of the IC (including the charge pump voltage) and its ability to enhance the N-Channel MOSFET. Unless the load current is well below the 1A rating of the device, output voltages above 7V are not recommended. The minimum output voltage can be programmed down to 1.25V, however, the input voltage must always be greater than the UVLO of the part.

Shutdown Feature

All versions include a shutdown feature, limiting quiescent current to 25µA typical. The UCC381 is shut down by pulling the CT pin to below 0.25V. As shown in the applications circuit, a small logic level MOSFET or BJT transistor connected to the CT pin can be driven with a digital signal, putting the device in shutdown. If the CT pin is not pulled low, the IC will internally pull up on the pin, enabling the regulator. The CT pin should not be forced high, as this will interfere with the short circuit protection feature. Selection of the timing capacitor for the adjustable version is explained in the *Short Circuit Protection* section.

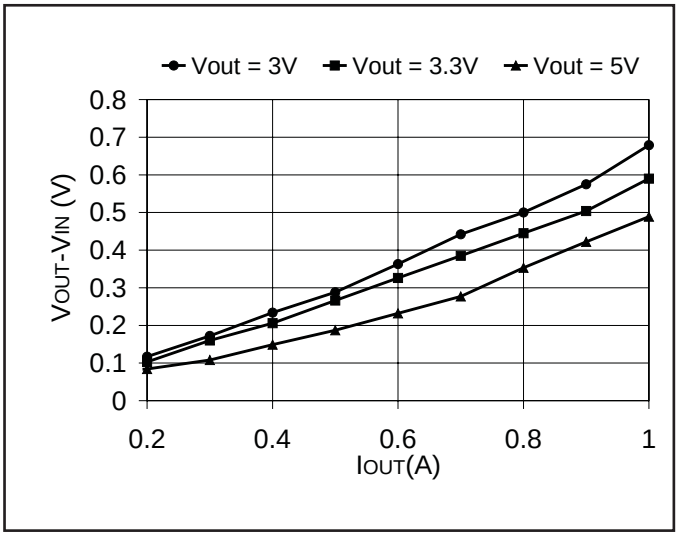


Figure 2. Typical dropout vs. load current.

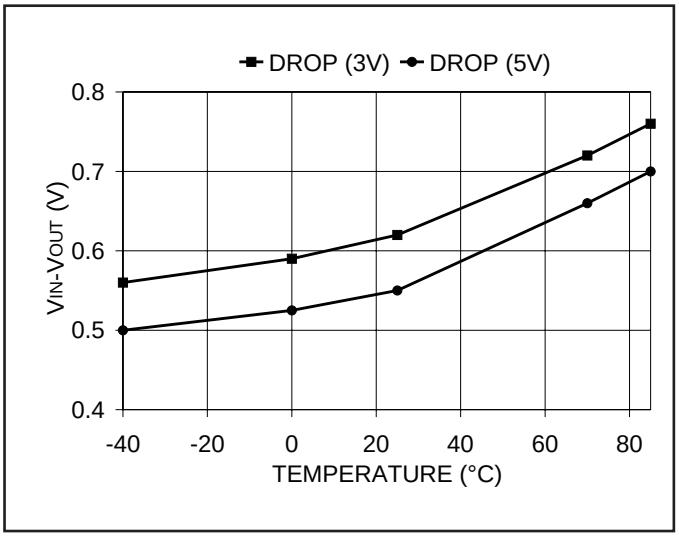


Figure 4. Typical dropout vs. temperature (1A load).

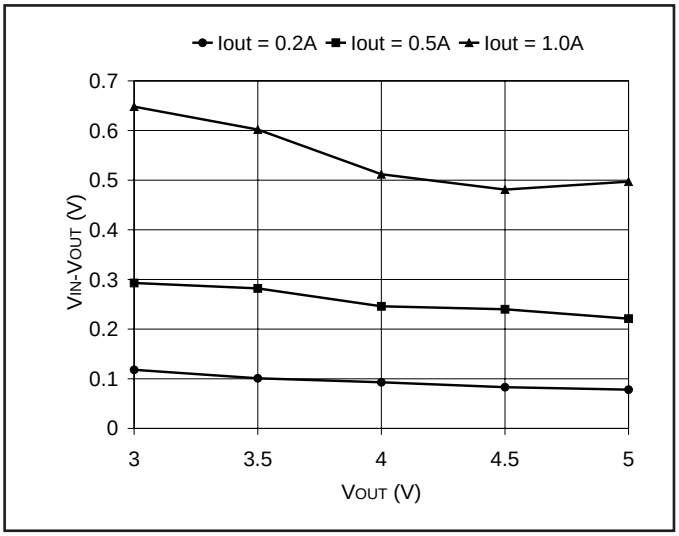


Figure 3. Typical dropout voltate vs. I_{OUT} and V_{OUT}.

APPLICATION INFORMATION (cont.)

Thermal Design

The Packing Information section of the data book contains reference material for the thermal ratings of various packages. The section also includes an excellent article *Thermal Characteristics of Surface Mount Packages*, that is the basis of the following discussion.

Thermal design for the UCC381 includes two modes of operation, normal and pulsed mode. In normal operation, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$T_{RISE} = P_{DISS} \bullet (\theta jc + \theta ca)\ ^{\circ}C \qquad (5)$$

Where theta is thermal resistance and P_{DISS} is the power dissipated. The thermal resistance of both the SOIC-8 DP package (junction to case) is 22 degrees Celsius per Watt. In order to prevent the regulator from going into thermal shutdown, the case to ambient theta must keep the junction temperature below 150C. If the LDO is mounted on a 5 square inch pad of 1 ounce copper, for example, the thermal resistance from junction to ambient becomes 40-70 degrees Celsius per Watt. If a lower thermal resistance is required by the application, the device heat sinking would need to be improved.

When the UCC381 regulator is in pulsed mode, due to an overload or short circuit in the application, the maximum *average* power dissipation is calculated as follows:

$$P_{PULSE\,(avg)} = \qquad (6)$$

$$(V_{IN} - V_{OUT}) \bullet I_{CL} \bullet \left(\frac{T_{ON}}{33 \bullet T_{ON}} \right) Watts$$

As seen in equation 6, the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the T_{ON} period can be significant, the thermal mass of the package will generally keep the junction temperature from rising unless the T_{ON} period is increased to tens of milliseconds.

Ripple Rejection

Even though the UCC381 linear regulators are not optimized for fast transient applications (Refer to UC182 "Fast LDO Linear Regulator"), they do offer significant power supply rejection at lower frequencies. Fig 5. depicts ripple rejection performance in a typical application. The performance can be improved with additional filtering.

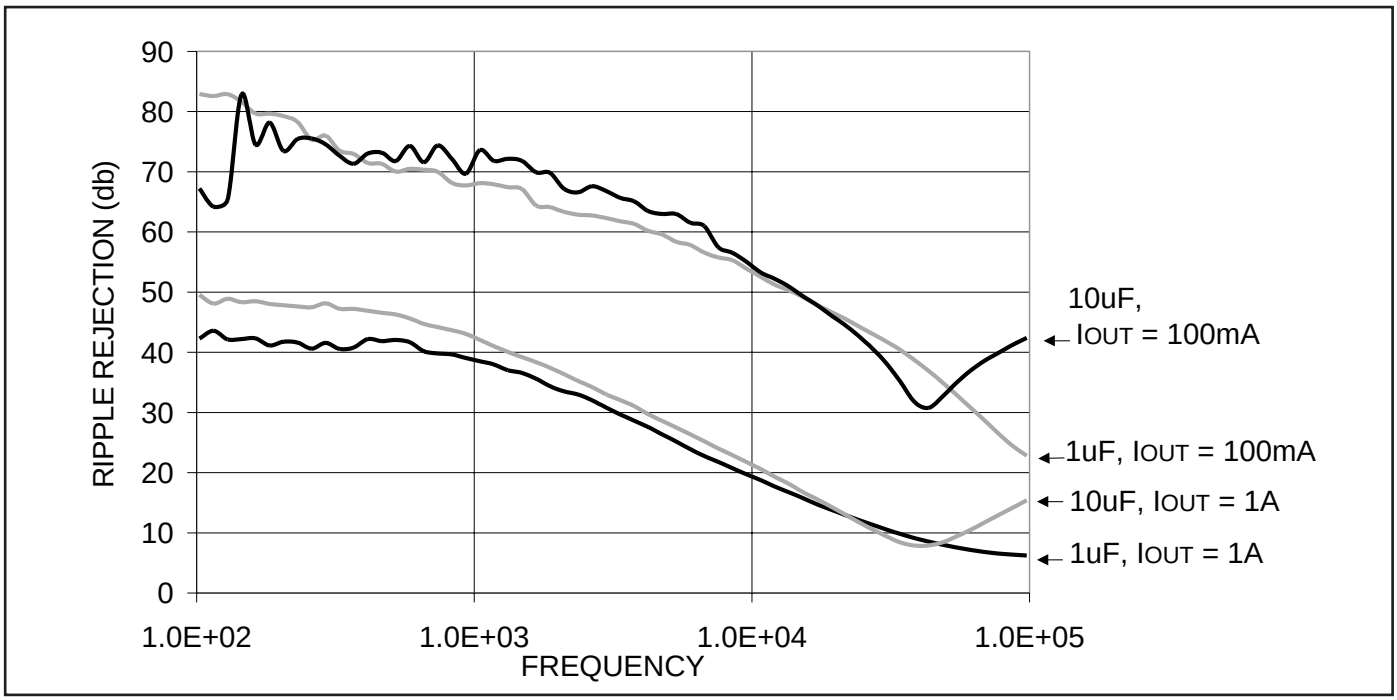


Figure 5. Ripple rejection vs. frequency.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC281DP-5	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC281 DP-5 281-5	Samples
UCC281DP-ADJ	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC281D P-ADJ 281-ADJ	Samples
UCC381DP-3	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		UCC381 DP-3 381-3	Samples
UCC381DP-5	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		UCC381 DP-5 381-5	Samples
UCC381DP-5G4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC381 DP-5 381-5	Samples
UCC381DP-ADJ	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		UCC381D P-ADJ 381-ADJ	Samples
UCC381DPTR-5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		UCC381 DP-5 381-5	Samples
UCC381DPTR-5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC381 DP-5 381-5	Samples
UCC381DPTR-ADJ	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		UCC381D P-ADJ 381-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

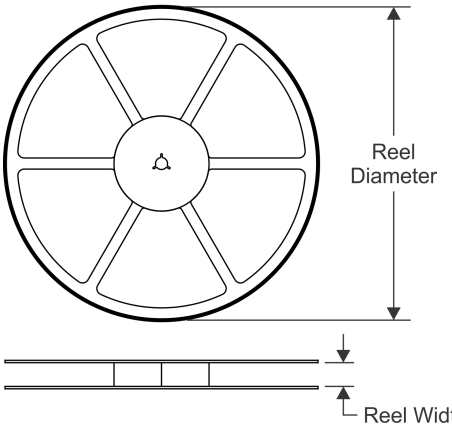
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

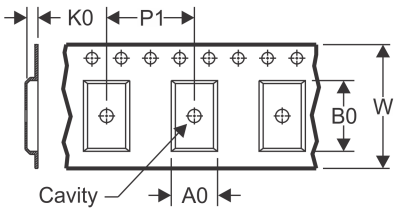
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

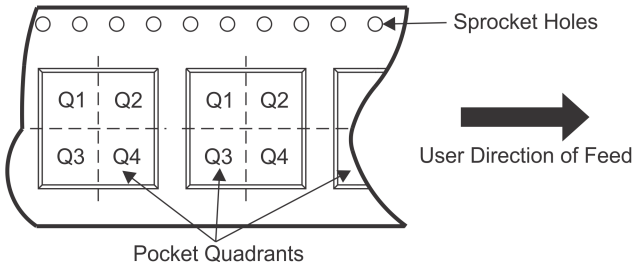


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

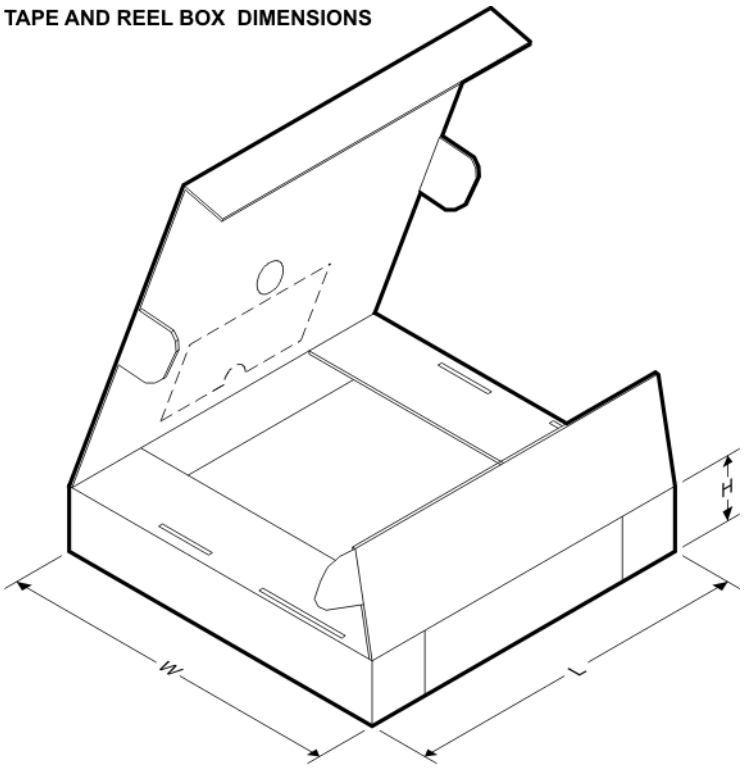
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC381DPTR-5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC381DPTR-ADJ	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC381DPTR-5	SOIC	D	8	2500	853.0	449.0	35.0
UCC381DPTR-ADJ	SOIC	D	8	2500	853.0	449.0	35.0

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