

CSD19538Q2 100V N 沟道 NexFET™ 功率 MOSFET

1 特性

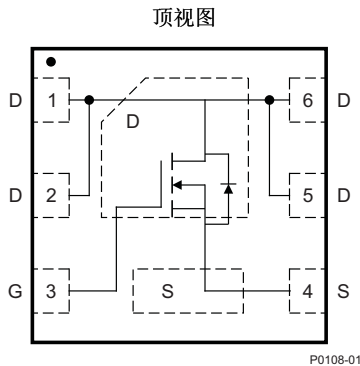
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

2 应用

- 以太网供电 (PoE)
- 电源设备 (PSE)
- 电机控制

3 说明

这款 100V、49mΩ、采用 2mm × 2mm SON 封装的 NexFET™ 功率 MOSFET 被设计成在功率转换应用中大大降低 损耗。



产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	4.3		nC
Q_{gd}	栅极电荷 (栅极到漏极)	0.8		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 6V$	58	mΩ
		$V_{GS} = 10V$	49	
$V_{GS(th)}$	阈值电压	3.2		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD19538Q2	3000	7 英寸卷带	SON 2.00mm x 2.00mm 塑料封装	卷带封装
CSD19538Q2T	250			

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

绝对最大额定值

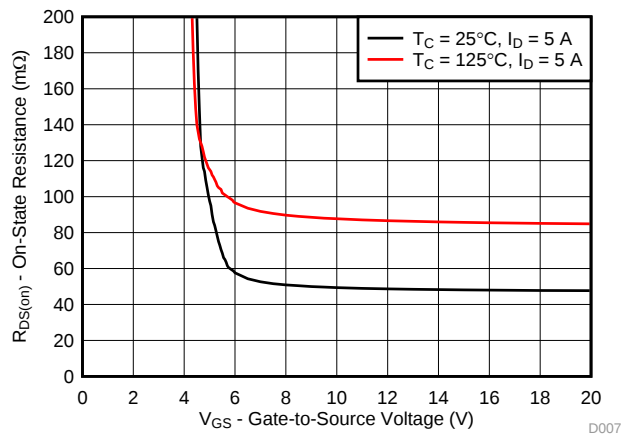
$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	14.4	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	13.1	
	持续漏极电流(1)	4.6	
I_{DM}	脉冲漏极电流(2)	34.4	A
P_D	功率耗散(1)	2.5	W
	功率耗散, $T_C = 25^\circ\text{C}$	20.2	
T_J, T_{stg}	工作结温, 储存温度	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D = 12.6A, L = 0.1mH, R_G = 25\Omega$	8	mJ

(1) $R_{\theta JA} = 50^\circ\text{C/W}$ 。这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸², 2 盎司铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC} = 6.2^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。

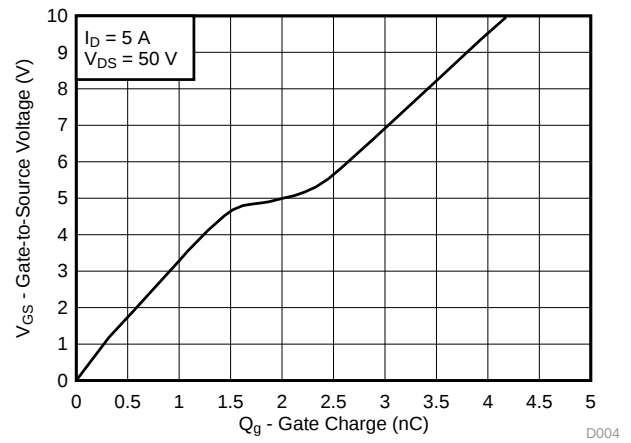


$R_{DS(on)}$ 与 V_{GS} 对比



中的测试电压 V_{DS} 从 100V 更改为 50V

栅极电荷



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4 修订历史记录

Changes from Original (July 2016) to Revision A	Page
• 已更改 将栅极电荷曲线	2
• Changed test voltage V_{DS} from 100 V : to 50 V in Figure 4	5

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

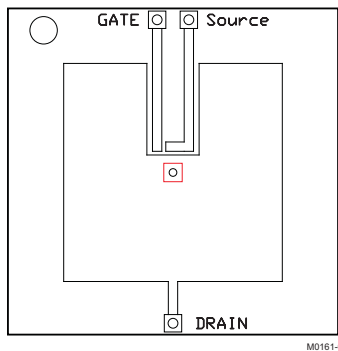
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.8	3.2	3.8	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 6 V, I _D = 5 A		58	72	mΩ
		V _{GS} = 10 V, I _D = 5 A		49	59	
g _{fs}	Transconductance	V _{DS} = 10 V, I _D = 5 A		19		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz		349	454	pF
C _{oss}	Output capacitance			69	90	pF
C _{rss}	Reverse transfer capacitance			12.6	16.4	pF
R _G	Series gate resistance			4.6	9.2	Ω
Q _g	Gate charge total (10 V)	V _{DS} = 50 V, I _D = 5 A		4.3	5.6	nC
Q _{gd}	Gate charge gate-to-drain			0.8		nC
Q _{gs}	Gate charge gate-to-source			1.6		nC
Q _{g(th)}	Gate charge at V _{th}			1.0		nC
Q _{oss}	Output charge	V _{DS} = 50 V, V _{GS} = 0 V		12.3		nC
t _{d(on)}	Turnon delay time	V _{DS} = 50 V, V _{GS} = 10 V, I _{DS} = 5 A, R _G = 0 Ω		5		ns
t _r	Rise time			3		ns
t _{d(off)}	Turnoff delay time			7		ns
t _f	Fall time			2		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 5 A, V _{GS} = 0 V		0.85	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 50 V, I _F = 5 A, di/dt = 300 A/μs		94		nC
t _{rr}	Reverse recovery time			32		ns

5.2 Thermal Information

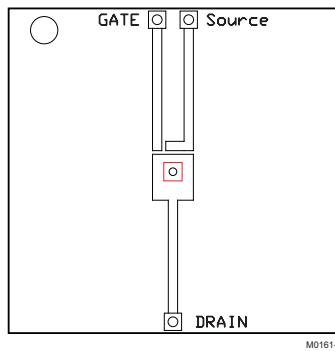
 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			6.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			65	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in $\times$ 1.5-in (3.81-cm $\times$ 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.



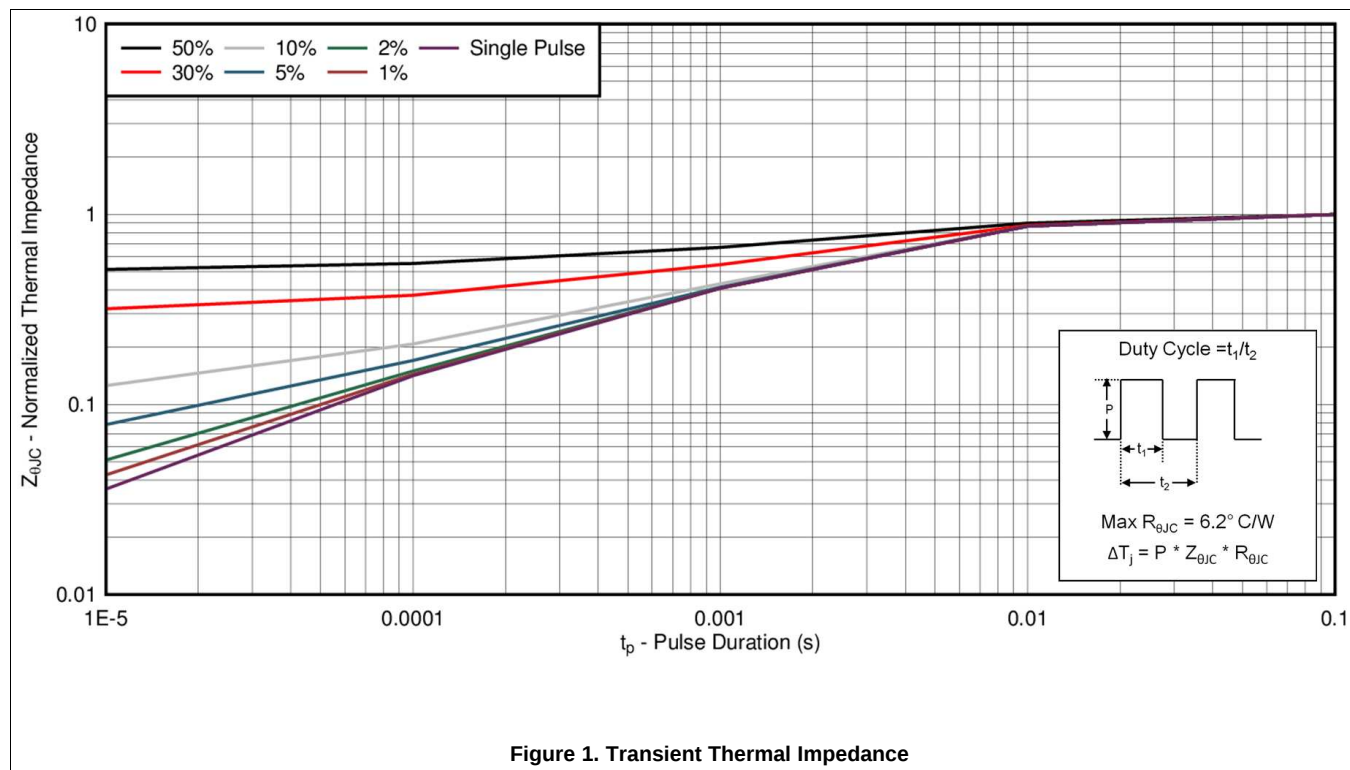
Max $R_{\theta JA} = 65^{\circ}\text{C/W}$
when mounted on 1 in²
(6.45 cm²) of 2-oz
(0.071-mm) thick Cu.



Max $R_{\theta JA} = 250^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz (0.071-mm) thick
Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

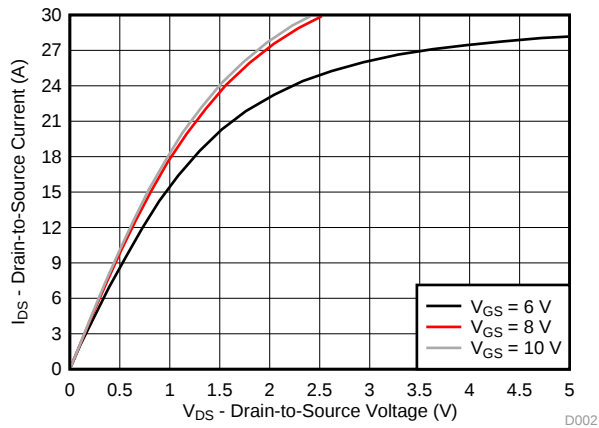


Figure 2. Saturation Characteristics

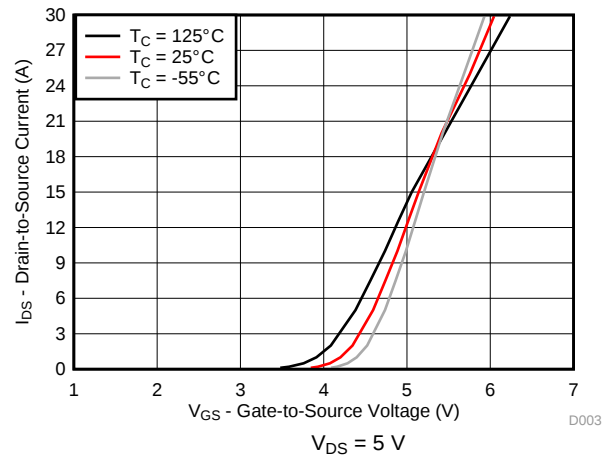


Figure 3. Transfer Characteristics

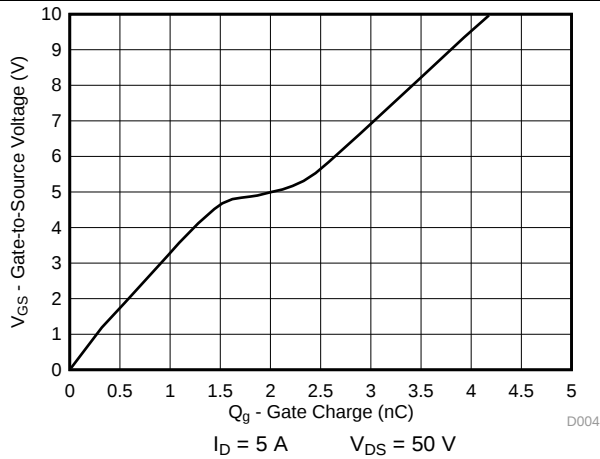


Figure 4. Gate Charge

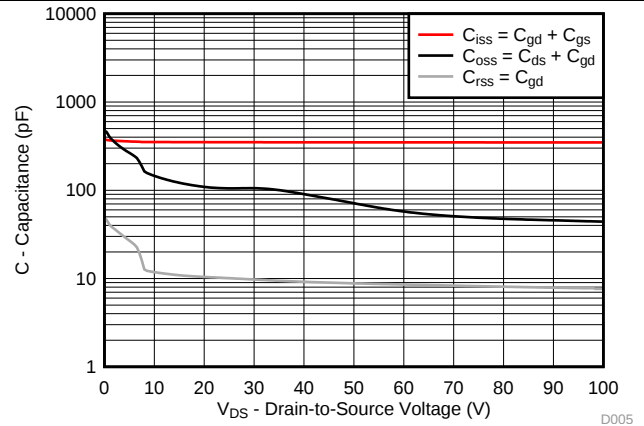


Figure 5. Capacitance

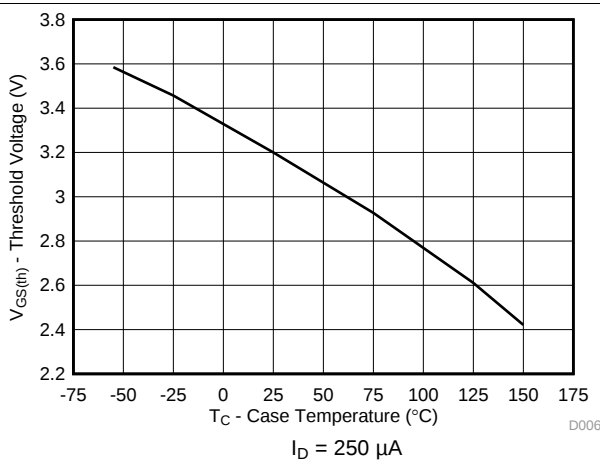


Figure 6. Threshold Voltage vs Temperature

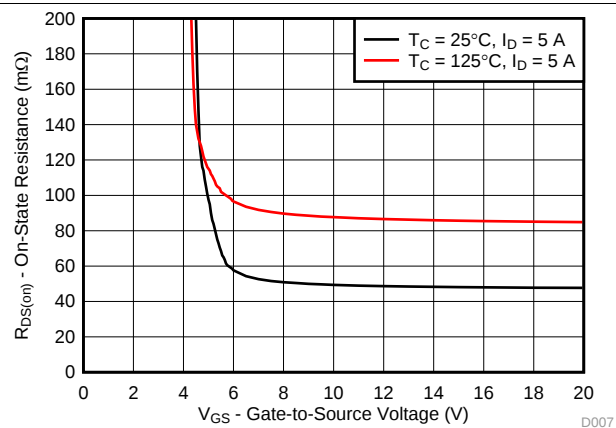


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

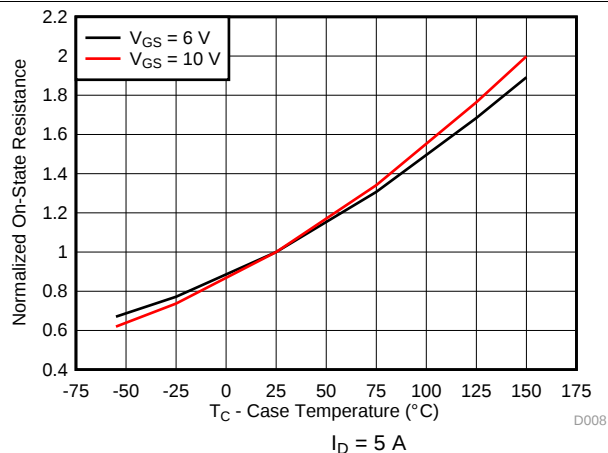


Figure 8. Normalized On-State Resistance vs Temperature

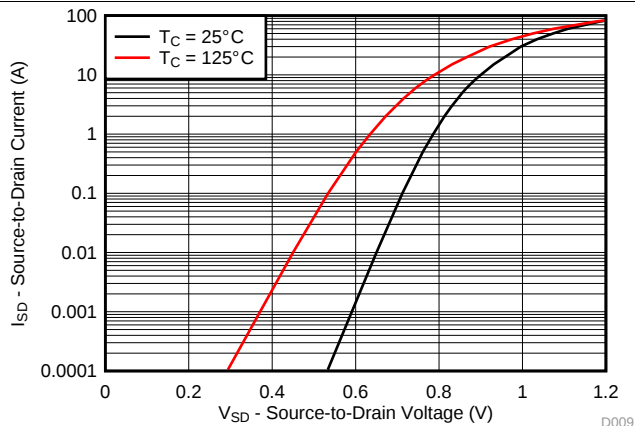


Figure 9. Typical Diode Forward Voltage

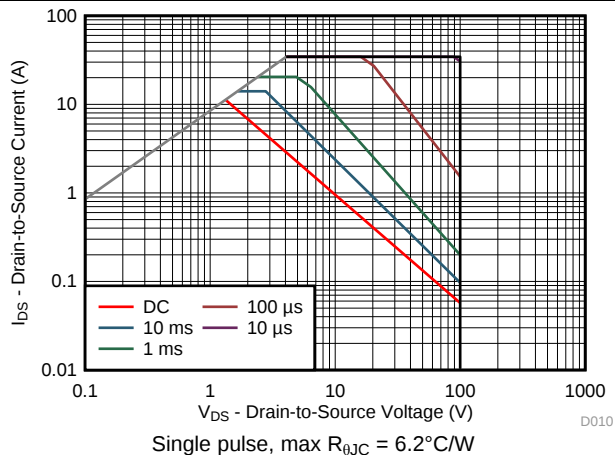


Figure 10. Maximum Safe Operating Area

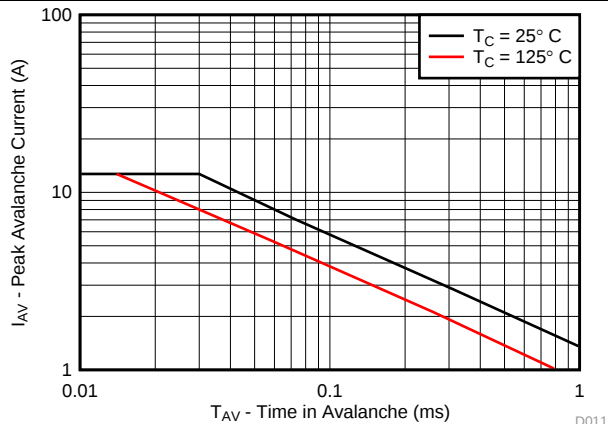


Figure 11. Single Pulse Unclamped Inductive Switching

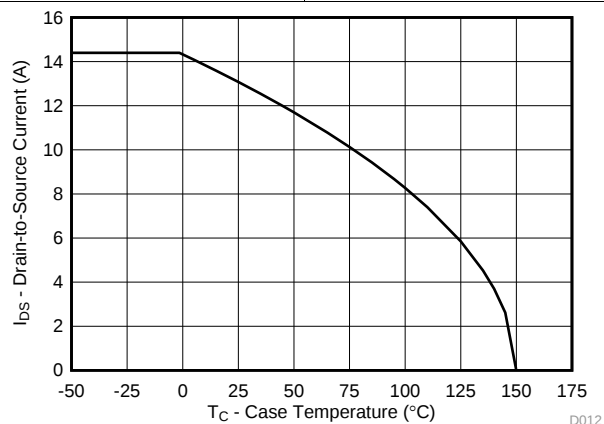


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

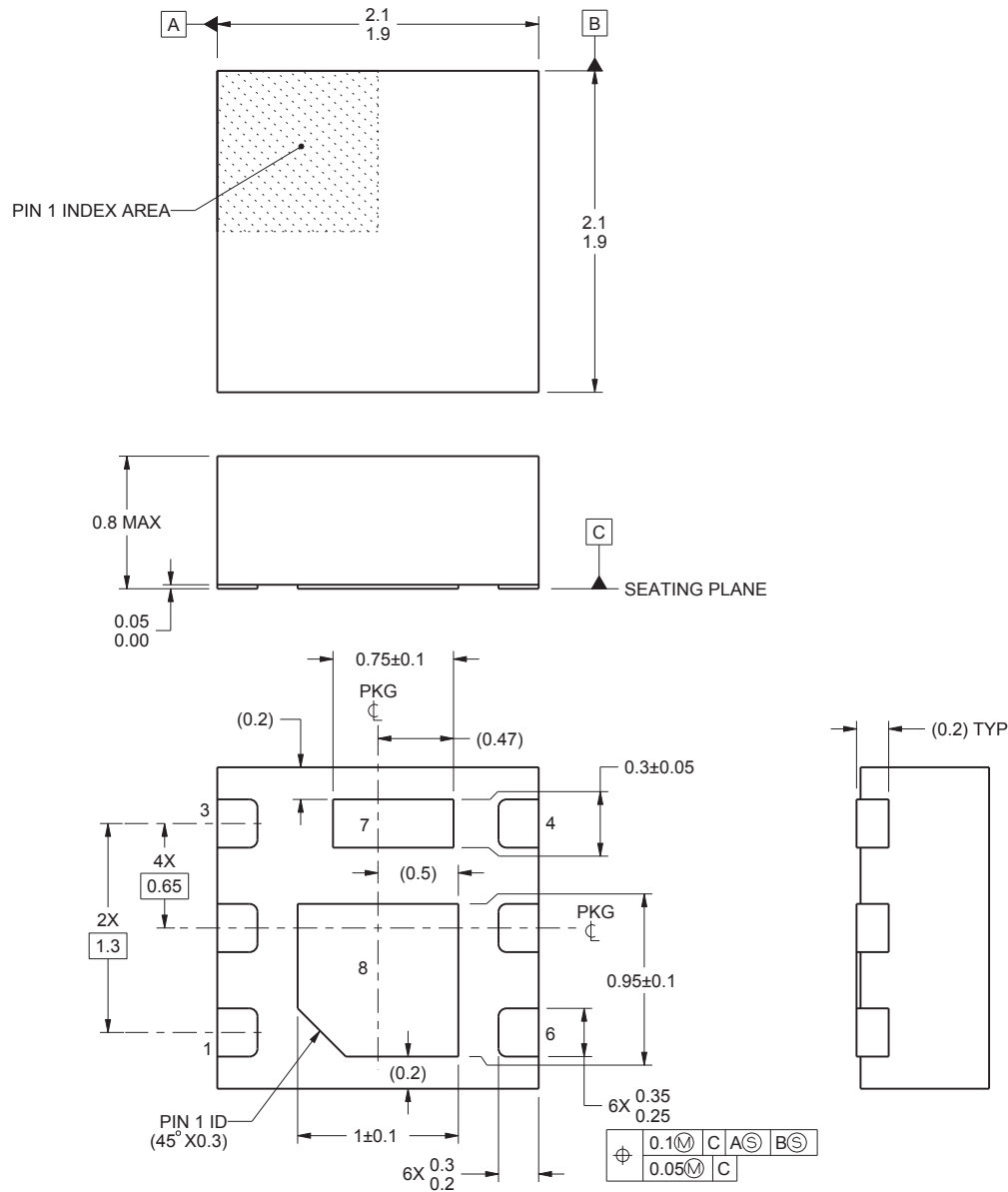
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

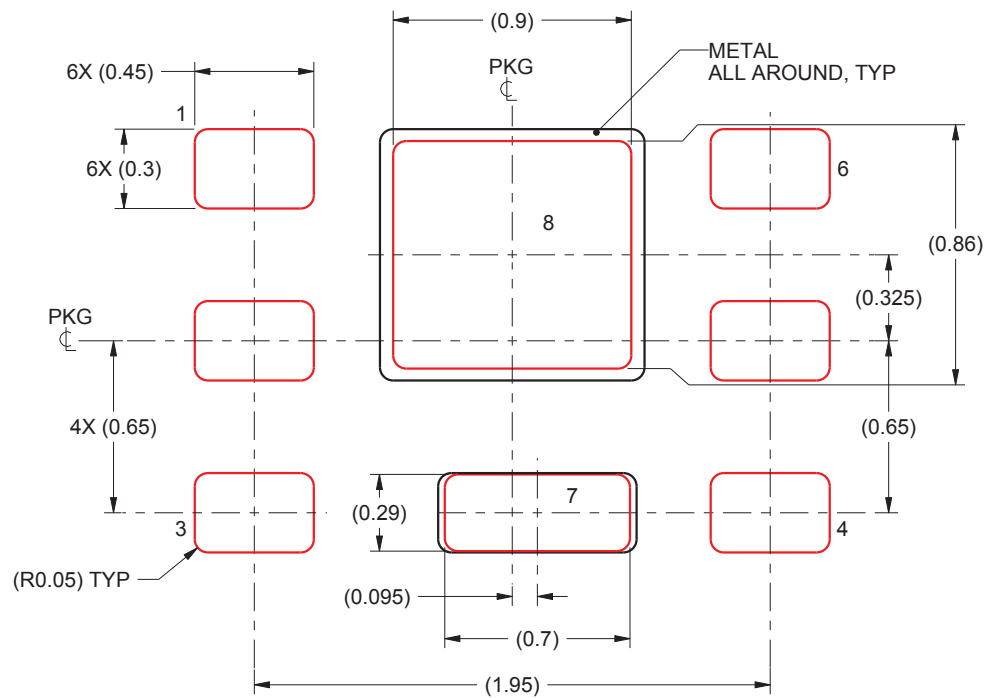
7.1 Q2 封装尺寸



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和容限值遵循 ASME Y14.5M。
2. 本图纸如有变更，恕不通知。
3. 封装散热盘必须在印刷电路板上焊接，包装散热和机械性能。

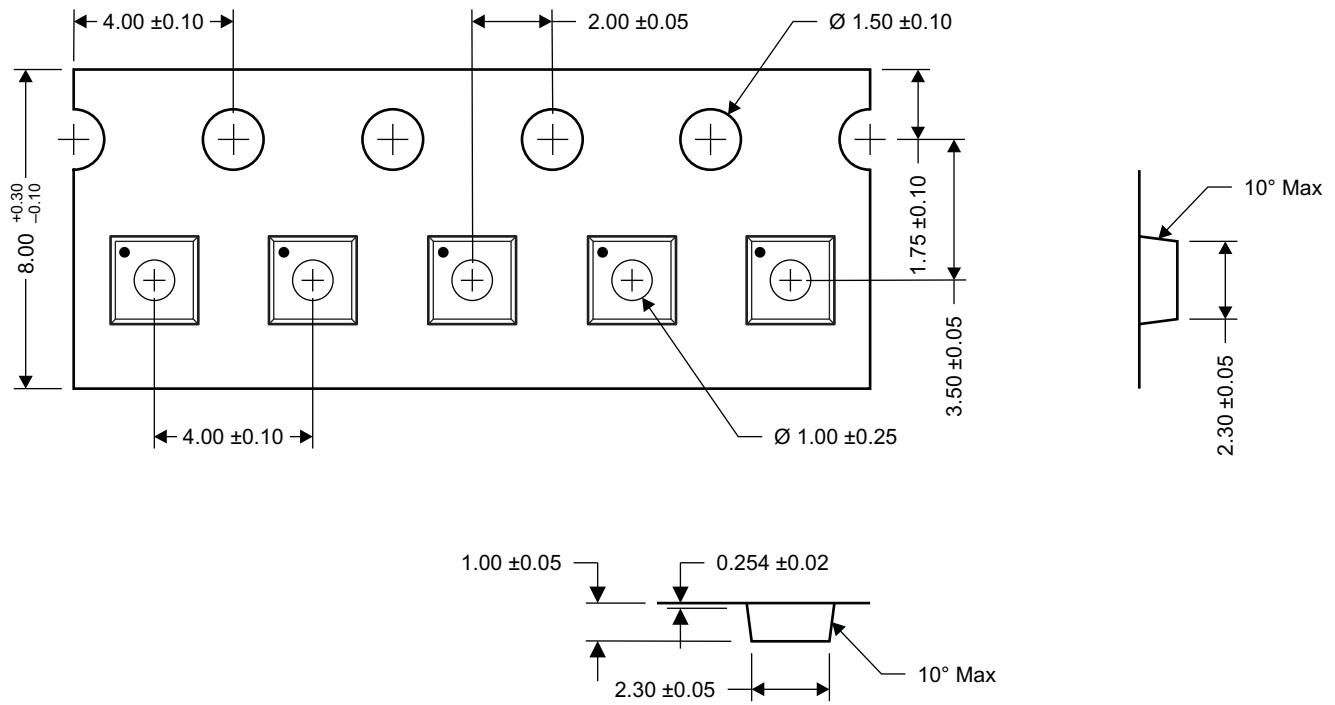
Q2 封装尺寸 (接下页)

7.1.2 推荐的模版布局



1. 所有线性尺寸的单位均为毫米。
2. 具有漏斗形壁和圆角的激光切割窗孔将提供更佳的焊锡膏脱离。IPC-7525 可能提供其他替代性设计建议。

7.2 Q2 卷带信息



M0168-01

- Notes:
1. 测自链齿孔中心线到孔眼中心线。
 2. 10 个链齿孔的累积容差为 ± 0.2 。
 3. 提供了其他材料。
 4. 卷带的 SR 典型值最大为 10^9 OHM/SQ 。
 5. 所有尺寸单位均为 mm，除非另有说明。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19538Q2	ACTIVE	WSO	DQK	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	1958	Samples
CSD19538Q2T	ACTIVE	WSO	DQK	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	1958	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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