



#### P-CHANNEL ENHANCEMENT MODE MOSFET

### **Product Summary**

V <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> T <sub>A</sub> = +25°C
40)/	70mΩ @ V <sub>GS</sub> = -4.5V	-3.6A
-12V	100mΩ @ V <sub>GS</sub> = -2.5V	-3.0A

### **Description and Applications**

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Battery Management
- Load Switch
- Battery Protection

#### **Features and Benefits**

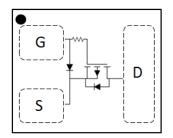
- Low Q<sub>g</sub> & Q<sub>gd</sub>
- Small Footprint
- Low Profile 0.22mm Height
- ESD Protected Gate 4kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

#### **Mechanical Data**

- Case: X4-DSN0607-3
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu or NiAu. Solderable per MIL-STD-202, Method 208

X4-DSN0607-3





Top View Equivalent Circuit

#### Ordering Information (Note 4)

Part Number	Case	Pitch	Packaging	Site
DMP1070UCA3-7	X4-DSN0607-3	4mm	3000/Tape & Reel	Α
DMP1070UCA3-7A	X4-DSN0607-3	2mm	10000/Tape & Reel	В

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

### **Marking Information**

Site A:

M9 YM M9 = Product Type Marking Code YM = Date Code Marking

Y = Year (ex: G = 2019) M = Month (ex: 9 = September) Site B:

M9 <u>Y</u>M M9 = Product Type Marking Code  $\underline{YM}$  = Date Code Marking  $\overline{Y}$  = Year (ex: G = 2019) M = Month (ex: 9 = September)

Date Code Key

Year	2019	20	20	2021	2022	20	23	2024	2025	20	26	2027
Code	G	ŀ	1	I	J	ŀ	<	L	М	1	٧	0
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



# Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		$V_{DSS}$	-12	V
Gate-Source Voltage		$V_{GSS}$	-6	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = -4.5V	$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	-3.6 -2.9	А
Continuous Drain Current (Note 5) V <sub>GS</sub> = -2.5V	$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	-3.0 -2.4	А
Pulsed Drain Current (Note 6)	·	I <sub>DM</sub>	-15	Α

## **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 7)	P <sub>D</sub>	0.71	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 7)	R <sub>0JA</sub>	179.3	°C/W
Power Dissipation (Note 5)	P <sub>D</sub>	1.36	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 5)	R <sub>0JA</sub>	92.2	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

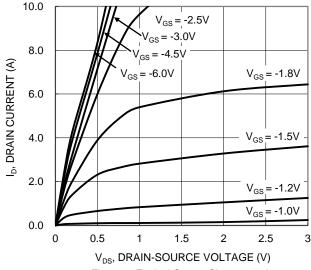
# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

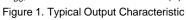
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-12	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	_	_	-50	nA	$V_{DS} = -9.6V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	-25	nA	$V_{GS} = -5V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.40	-0.66	-0.95	V	$V_{DS} = V_{GS}$ , $I_D = -250\mu A$	
			52	70		$V_{GS} = -4.5V, I_D = -0.4A$	
Static Drain-Source On-Resistance		_	69	100	mΩ	$V_{GS} = -2.5V, I_D = -0.4A$	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	93	150	11122	$V_{GS} = -1.8V, I_D = -0.4A$	
		_	120	210		$V_{GS} = -1.5V, I_D = -0.1A$	
Diode Forward Voltage	V <sub>SD</sub>	_	-0.7	-1.0	V	$V_{GS} = 0V, I_S = -0.4A$	
DYNAMIC CHARACTERISTICS (Note 9)				•	•		
Input Capacitance	C <sub>iss</sub>	_	147	_		24 24 24	
Output Capacitance	Coss	_	79	_	pF	$V_{DS} = -6V, V_{GS} = 0V,$ f = 1MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	30	_		I = IIVIMZ	
Series Gate Resistance	Rg	_	13	_	Ω	$f = 1MHz$ , $V_{GS} = 0V$ , $V_{DS} = 0V$	
Total Gate Charge	Qq	_	1.45	_			
Gate-Source Charge	Qgs	_	0.14	_	nC	$V_{DS} = -6V$ , $V_{GS} = -4.5V$ ,	
Gate-Drain Charge	Q <sub>qd</sub>	_	0.28	_	IIC	$I_D = -0.4A$	
Gate Charge at V <sub>TH</sub>	Q <sub>g(th)</sub>	_	0.10	_			
Turn-On Delay Time	t <sub>D(ON)</sub>	_	3.2	_			
Turn-On Rise Time	t <sub>R</sub>	_	6.0	_		$V_{DS} = -6V, V_{GS} = -4.5V,$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>		8.6	_	ns	$R_G = 0\Omega$ , $I_D = -0.4A$	
Turn-Off Fall Time	t <sub>F</sub>	_	5.8	_	1		

Notes:

- 5. Device mounted on FR-4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.
- Repetitive rating, pulse width limited by junction temperature.
  Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
- 8. Short duration pulse test used to minimize self-heating effect.
- 9. Guaranteed by design. Not subject to production testing.







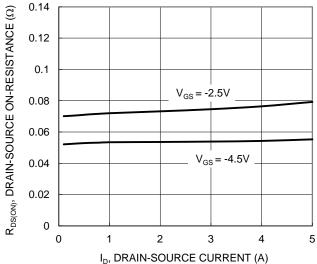


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

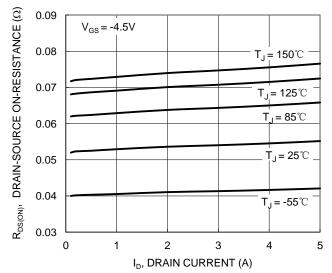


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

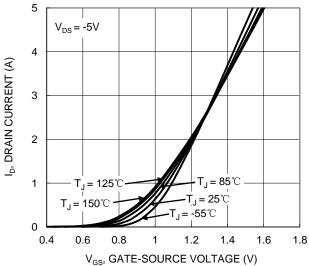


Figure 2. Typical Transfer Characteristic

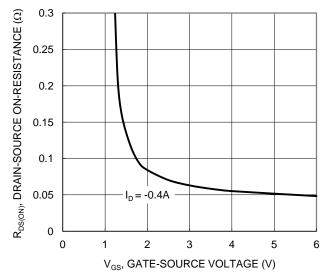


Figure 4. Typical Transfer Characteristic

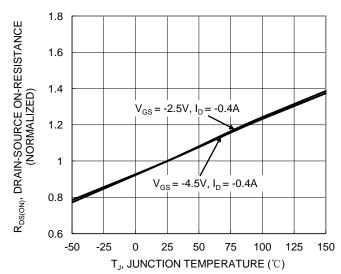


Figure 6. On-Resistance Variation with Junction Temperature





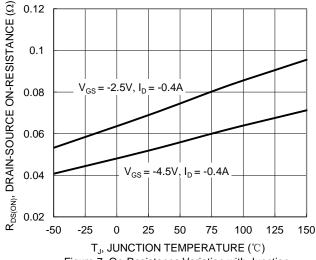
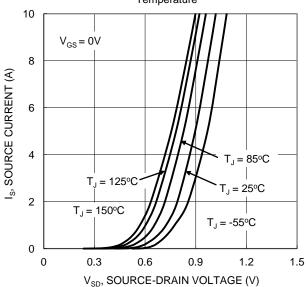
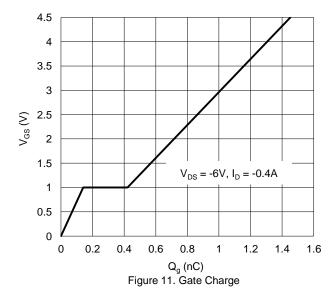


Figure 7. On-Resistance Variation with Junction Temperature

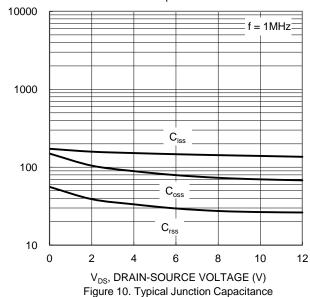


V<sub>SD</sub>, SOURCE-DRAIN VOLTAGE (V) Figure 9. Diode Forward Voltage vs. Current



 $V_{GS(TH)}$ , GATE THRESHOLD VOLTAGE (V) 0.8  $I_D = -1mA$ 0.6  $I_{D} = -250 \mu A$ 0.4 0.2 -50 -25 25 50 75 100 125 150 T<sub>J</sub>, JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. Junction Temperature



100  $R_{DS(ON)}$  Limited  $P_W = 100 \mu s$ ID, DRAIN CURRENT (A) 10 100ms  $P_W = 1 ms$ 0.1  $T_{J(Max)} = 150^{\circ}C \quad T_C = 25^{\circ}C$ Single Pulse DUT on 1\*MRP Board  $V_{GS} = -4.5V$ 0.01 0.1 10 100 V<sub>DS</sub>, DRAIN-SOURCE VOLTAGE (V) Figure 12. SOA, Safe Operation Area

C<sub>T</sub>, JUNCTION CAPACITANCE (pF)

August 2019



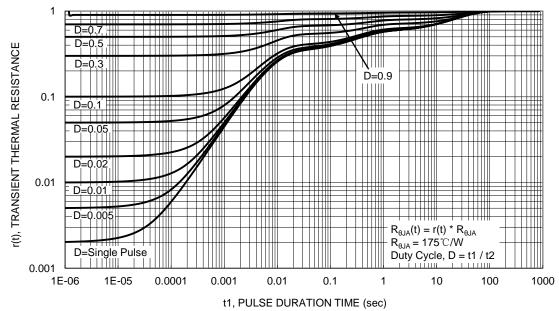


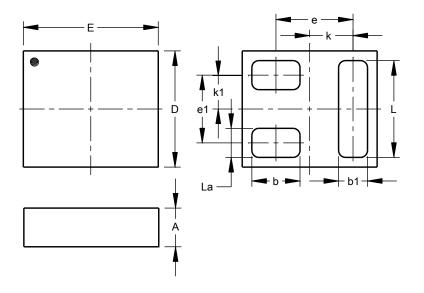
Figure 13. Transient Thermal Resistance



## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### X4-DSN0607-3

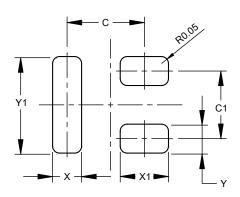


X4-DSN0607-3						
Dim	Min	Max	Тур			
Α	0.18	0.22	0.20			
b	0.24	0.26	0.25			
b1	0.14	0.16	0.15			
ם	0.56	0.64	0.60			
Е	0.65	0.73	0.69			
е			0.40			
e1			0.35			
k			0.225			
k1			0.175			
Ш	0.49	0.51	0.50			
La	0.14	0.16	0.15			
All Dimensions in mm						

## **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### X4-DSN0607-3



Dimensions	Value (in mm)		
С	0.40		
C1	0.35		
Х	0.15		
X1	0.25		
Y	0.15		
Y1	0.50		



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