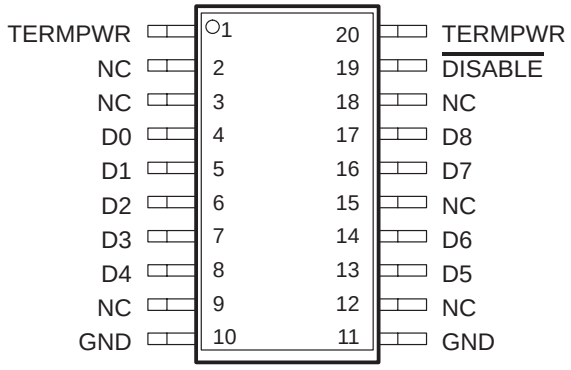
available features

- **Fully Integrated 9-Channel SCSI Termination**
- **No External Components Required**
- **Maximum Allowed Current Applied at First High-Level Step**
- **6-pF Typical Power-Down Output Capacitance**
- **Wide V_{term}† (Termination Voltage) Operating Range, 3.5 V to 5.5 V**
- **TTL-Compatible Disable Feature**
- **Compatible With Active Negation**
- **Thermal Regulation**

PW PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TL2218-285 is a current-mode 9-channel monolithic terminator specially designed for single-ended small-computer-systems-interface (SCSI) bus termination. A user-controlled disable function is provided to reduce standby power. No impedance-matching resistors or other external components are required for its operation as a complete terminator.

The device operates over a wide termination-voltage (V_{term}†) range of 3.5 V to 5.5 V, offering an extra 0.5 V of operating range when compared to the minimum termination voltage of 4 V required by other integrated active terminators. The TL2218-285 functions as a current-sourcing terminator and supplies a constant output current of 23 mA into each asserted line. When a line is deasserted, the device senses the rising voltage level and begins to function as a voltage source, supplying a fixed output voltage of 2.85 V. The TL2218-285 features compatibility with active negation drivers and has a typical sink current capability of 20 mA.

The TL2218-285 is able to ensure that maximum current is applied at the first high-level step. This performance means that the device should provide a first high-level step exceeding 2 V even at a 10-MHz rate. Therefore, noise margins are improved considerably above those provided by resistive terminators.

A key difference between the TL2218-285 current-mode terminator and a Boulay terminator is that the TL2218-285 does not incorporate a low dropout regulator to set the output voltage to 2.85 V. In contrast with the Boulay termination concept, the accuracy of the 2.85 V is not critical with the current-mode method used in the TL2218-285 because this voltage does not determine the driver current. Therefore, the primary device specifications are not the same as with a voltage regulator but are more concerned with output current.

The $\overline{\text{DISABLE}}$ terminal is TTL compatible and must be taken low to shut down the outputs. The device is normally active, even when $\overline{\text{DISABLE}}$ is left floating. In the disable mode, only the device startup circuits remain active, thereby reducing the supply current to just 500 μA. Output capacitance in the shutdown mode is typically 6 pF.

The TL2218-285 has on-board thermal regulation and current limiting, thus eliminating the need for external protection circuitry. A thermal regulation circuit that is designed to provide current limiting, rather than an actual thermal shutdown, is included in the individual channels of the TL2218-285. When a system fault occurs that leads to excessive power dissipation by the terminator, the thermal regulation circuit causes a reduction in the asserted-line output current sufficient to maintain operation. This feature allows the bus to remain active during a fault condition, which permits data transfer immediately upon removal of the fault. A terminator with thermal shutdown does not allow for data transfer until sufficient cooling has occurred. Another advantage offered by the TL2218-285 is a design that does not require costly laser trimming in the manufacturing process.

The TL2218-285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

† This symbol is not presently listed within EIA/JEDEC standards for letter symbols.

AVAILABLE OPTIONS

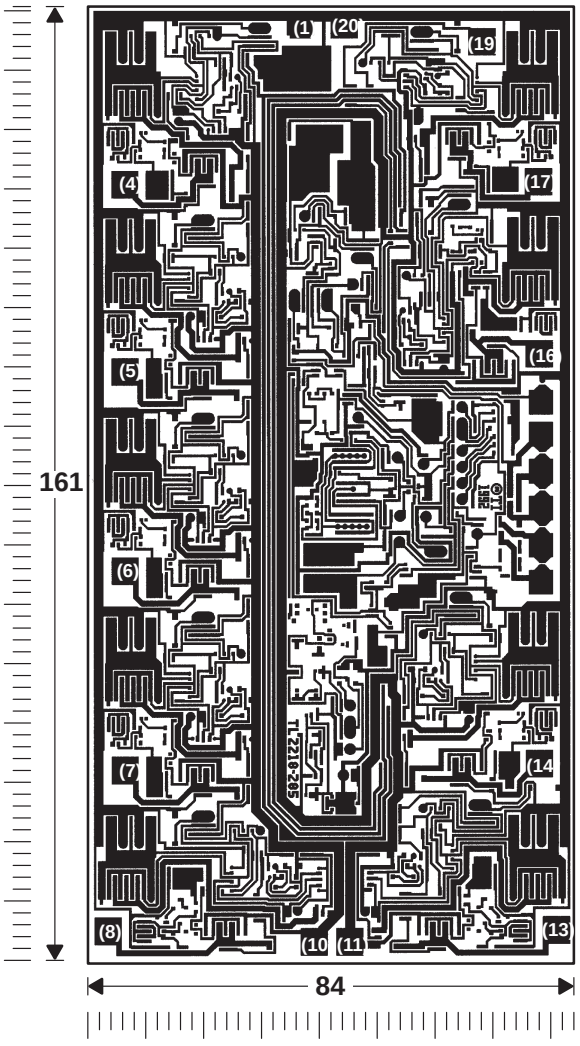
T_J	SURFACE MOUNT (PW)†	CHIP FORM (Y)
0°C to 125°C	TL2218-285PWLE	TL2218-285Y

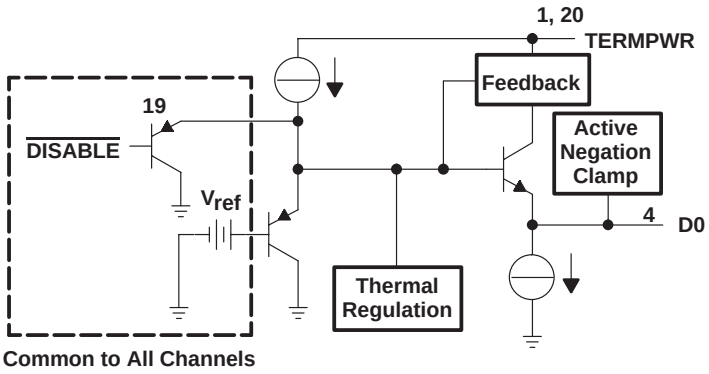
† The PW package is only available left-end taped and reeled.

TL2218-285Y chip information

This chip, when properly assembled, displays characteristics similar to the TL2218-285. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

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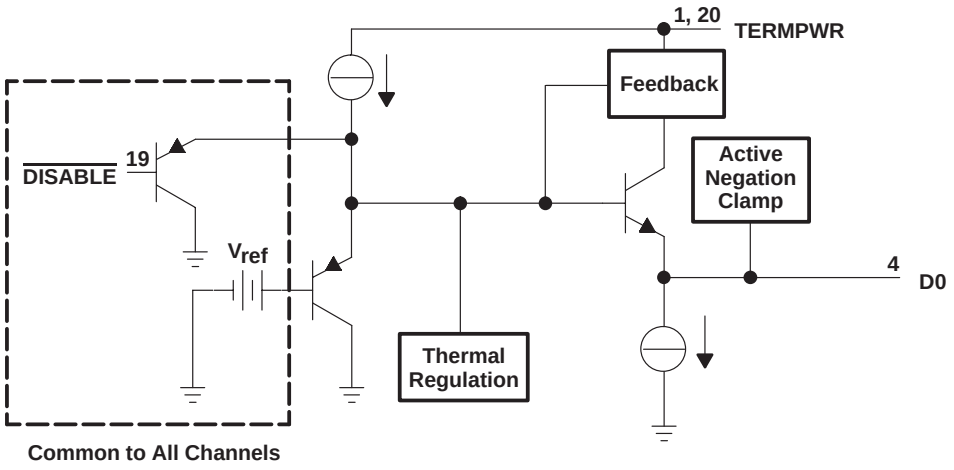
functional block diagram (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Figures 1, 2, and 3)†

Continuous termination voltage . . . . . 10 V
Continuous output voltage range . . . . . 0 V to 5.5 V
Continuous disable voltage range . . . . . 0 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . −55°C to 150°C
Storage temperature range, T_{stg} . . . . . −60°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	430 mW	166 mW
	T_C	4032 mW	32.2 mW/°C	2583 mW	2100 mW	812 mW
	T_L‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

**FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE**

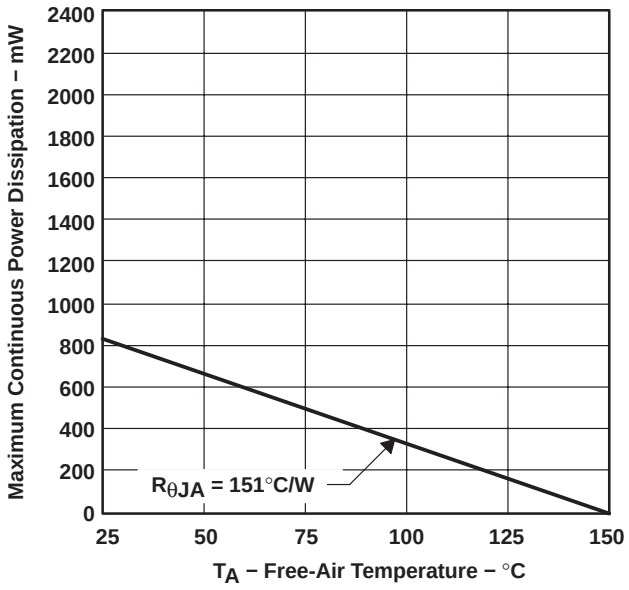


Figure 1

**CASE TEMPERATURE
DISSIPATION DERATING CURVE**

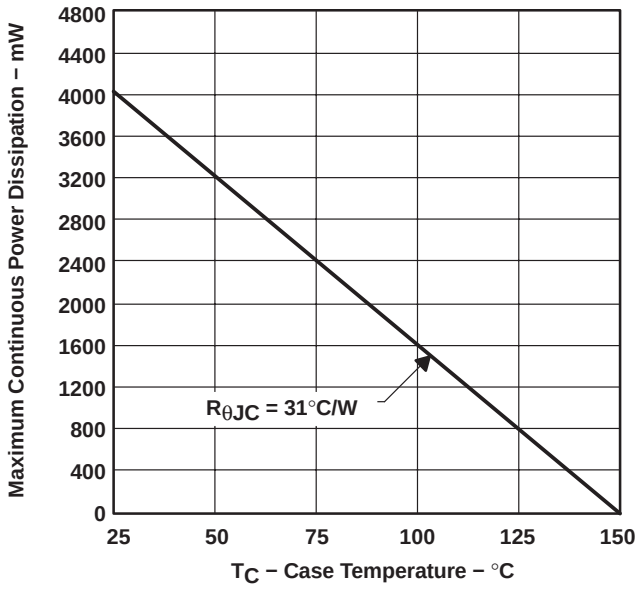


Figure 2

**LEAD TEMPERATURE
DISSIPATION DERATING CURVE**

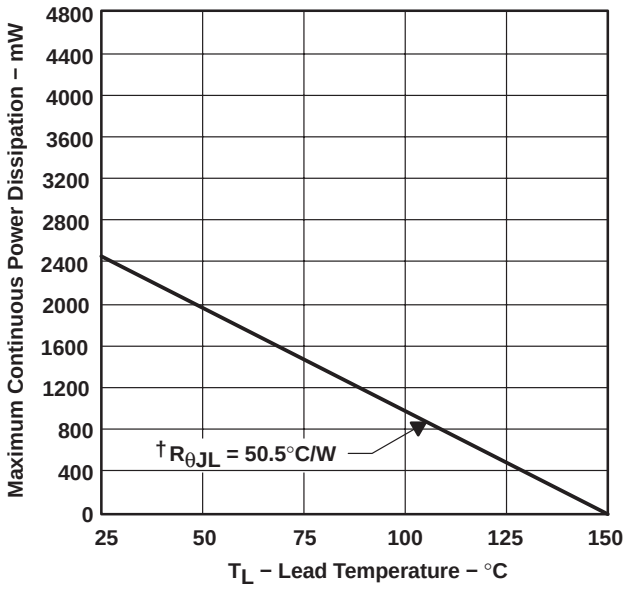


Figure 3

† $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device, and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

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recommended operating conditions

	MIN	MAX	UNIT
Termination voltage	3.5	5.5	V
High-level disable input voltage, V_{IH}	2	V_{term}	V
Low-level disable input voltage, V_{IL}	0	0.8	V
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics, V_{term} = 4.75 V, V_O = 0.5 V, T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage		2.5	2.85		V
TERMPWR supply current	All data lines open		9		mA
	All data lines = 0.5 V		228		
	$\overline{\text{DISABLE}}$ = 0 V		500		µA
Output current		−20.5	−23	−24	mA
Disable input current (see Note 1)	$\overline{\text{DISABLE}}$ = 4.75 V			1	µA
	$\overline{\text{DISABLE}}$ = 0 V			600	
Output leakage current	$\overline{\text{DISABLE}}$ = 0 V		100		nA
Output capacitance, device disabled	V_O = 0 V, 1 MHz		6		pF
Termination sink current, total	V_O = 4 V		20		mA

NOTE 1: When $\overline{\text{DISABLE}}$ is open or high, the terminator is active.

THERMAL INFORMATION

The need for smaller surface-mount packages for use on compact printed-wiring boards (PWB) causes an increasingly difficult problem in the area of thermal dissipation. In order to provide the systems designer with a better approximation of the junction temperature rise in the thin-shrink small-outline package (TSSOP), the junction-to-lead thermal resistance ($R_{\theta JL}$) is provided along with the more typical values of junction-to-ambient and junction-to-case thermal resistances, $R_{\theta JA}$ and $R_{\theta JC}$.

$R_{\theta JL}$ is used to calculate the device junction temperature rise measured from the leads of the unit. Consequently, the junction temperature is dependent upon the board temperature at the leads, $R_{\theta JL}$, and the internal power dissipation of the device. The board temperature is contingent upon several variables, including device packing density, thickness, material, area, and number of interconnects. The $R_{\theta JL}$ value depends on the number of leads connecting to the die-mount pad, the lead-frame alloy, area of the die, mount material, and mold compound. Since the power level at which the TSSOP can be used is highly dependent upon both the temperature rise of the PWB and the device itself, the systems designer can maximize this level by optimizing the circuit board. The junction temperature of the device can be calculated using the equation $T_J = (P_D \times R_{\theta JL}) + T_L$ where T_J = junction temperature, P_D = power dissipation, $R_{\theta JL}$ = junction-to-lead thermal resistance, and T_L = board temperature at the leads of the unit.

The values of thermal resistance for the TL2218-285 PW are as follows:

Thermal Resistance	Typical Junction Rise
$R_{\theta JA}$	151°C/W
$R_{\theta JC}$	31 °C/W
$R_{\theta JL}$	50.5°C/W

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_O	Output current	vs Input voltage	4
V_O	Output voltage	vs Input voltage	5
I_O	Output current	vs Junction temperature	6
V_O	Output voltage	vs Junction temperature	7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs INPUT VOLTAGE

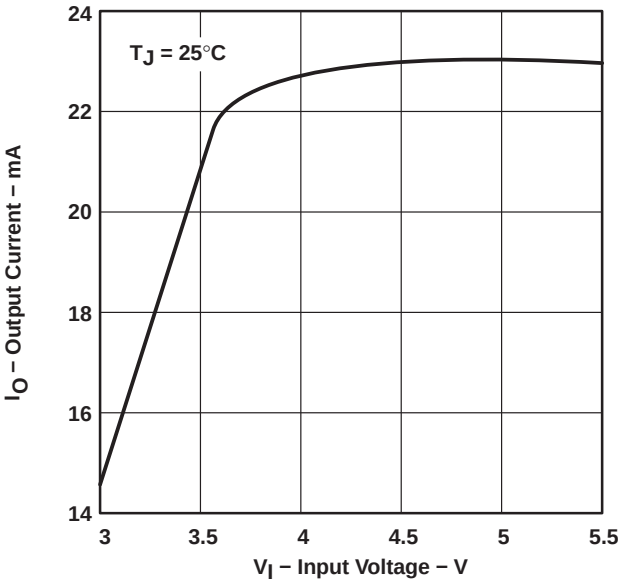


Figure 4

OUTPUT VOLTAGE vs INPUT VOLTAGE

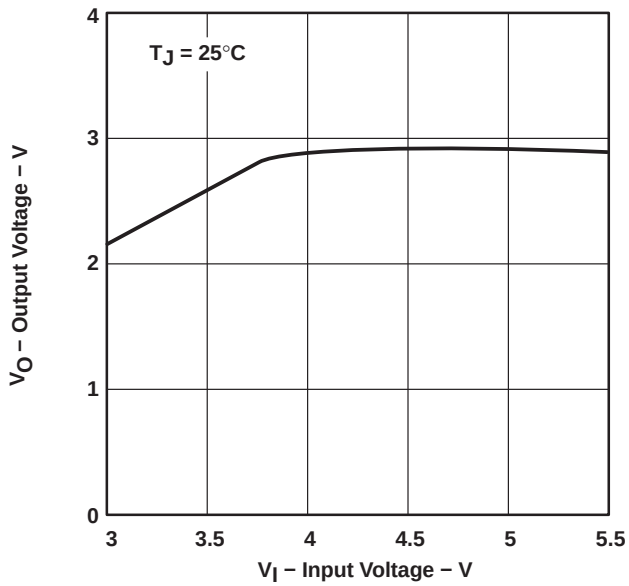


Figure 5

OUTPUT CURRENT vs JUNCTION TEMPERATURE

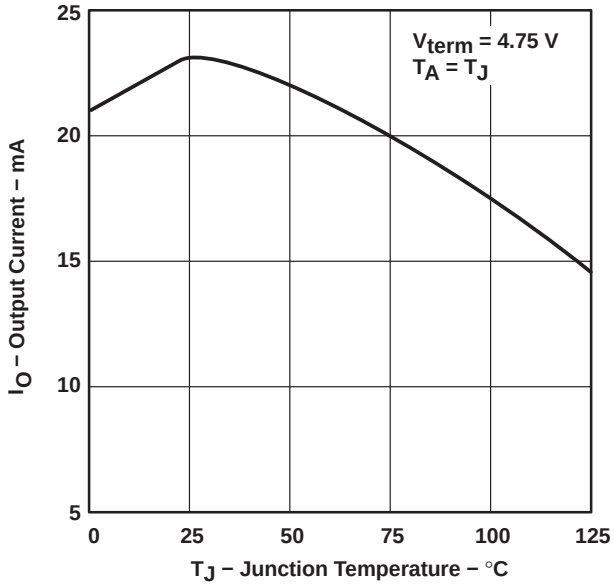


Figure 6

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

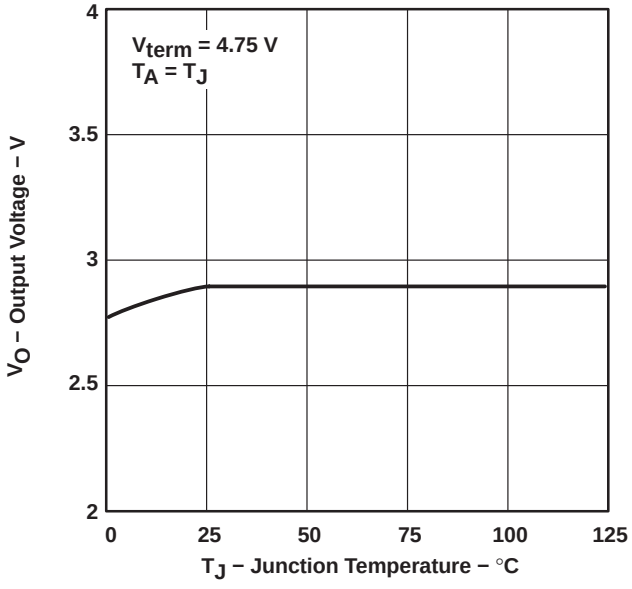


Figure 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL2218-285PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	2218285	Samples
TL2218-285PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	2218285	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

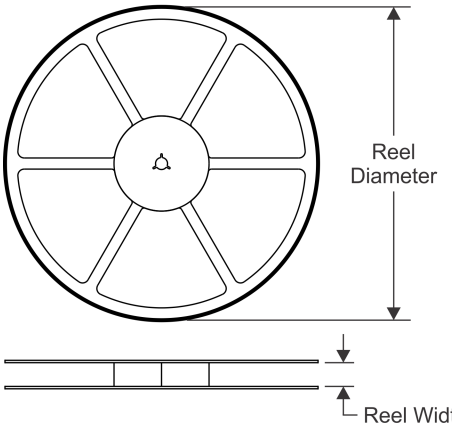
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

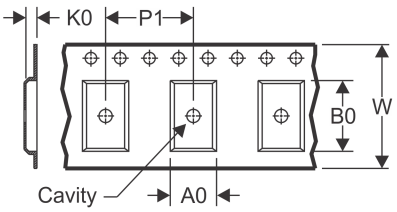
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

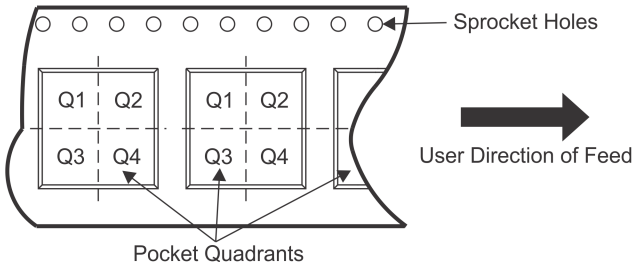


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

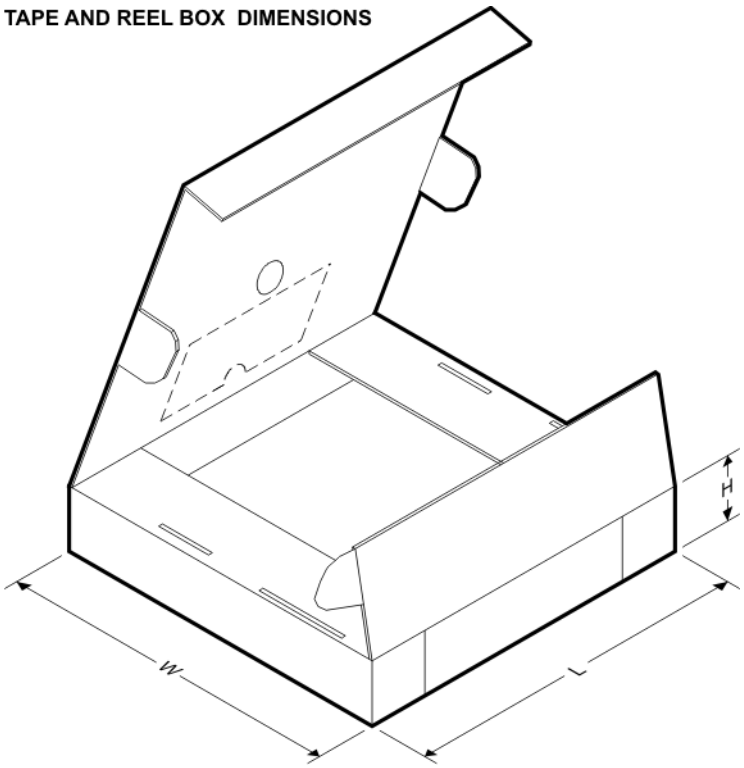
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL2218-285PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL2218-285PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

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