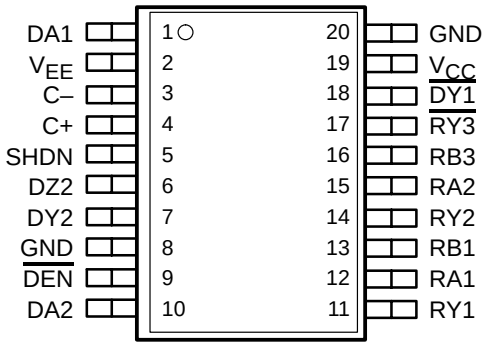
- **Single-Chip Interface Solution for the 9-terminal GeoPort™ Host (DTE)**
- **Designed to Operate up to 4 Mbit/s Full Duplex**
- **Single 5-V Supply Operation**
- **6-kV ESD Protection on All Terminals**
- **Backward compatible With AppleTalk™ and LocalTalk™**
- **Combines Multiple Components into a Single-chip Solution**
- **Complements the SN75LBC777 9-Terminal GeoPort Peripheral (DCE) Interface Device**
- **LinBiCMOS™ Process Technology**

DB or DW PACKAGE
(TOP VIEW)



description

The SN75LBC776 is a low-power LinBiCMOS device that incorporates the drivers and receivers for a 9-pin GeoPort host interface. GeoPort combines hybrid EIA/TIA-422-B and EIA/TIA-423-B drivers and receivers to transmit data up to four megabits per second (Mbit/s) full duplex. GeoPort is a serial communications standard that is intended to replace the RS-232, Appletalk, and LocalTalk printer ports all in one connector in addition to providing real-time data transfer capability. It provides point-to-point connections between GeoPort-compatible devices with data transmission rates up to 4 Mbit/s full duplex and a hot-plug feature. Applications include connection to telephony, integrated services digital network (ISDN), digital sound and imaging, fax-data modems, and other serial and parallel connections. The GeoPort is backwardly compatible to both LocalTalk and AppleTalk.

While the SN75LBC776 is powered-off (V_{CC} = 0) the outputs are in a high-impedance state. When the shutdown (SHDN) terminal is high, the charge pump is powered down and the outputs are in a high-impedance state. The driver enable ($\overline{DEN}$) terminal sends the outputs of the differential driver into a high-impedance state with a high input signal. All drivers and receivers have fail-safe mechanisms to ensure a high output state when the inputs are left open.

A switched-capacitor voltage converter generates the negative voltage required from a single 5-V supply using four 0.1-µF capacitors, two capacitors between the C+ and C- terminals and two capacitors between V_{EE} and ground.

The SN75LBC776 is characterized for operation over the 0°C to 70°C temperature range.

GeoPort, LocalTalk, and AppleTalk are trademarks of Apple Computer, Incorporated.
LinBiCMOS is a trademark of Texas Instruments Incorporated.

DRIVER FUNCTION TABLE†

INPUT DA1	INPUT DA2	ENABLE SHDN	ENABLE $\overline{\text{DEN}}$	OUTPUT $\overline{\text{DY1}}$	OUTPUT DY2	OUTPUT DZ2
H	X	L	X	L	X	X
L	X	L	X	H	X	X
X	H	L	L	X	H	L
X	L	L	L	X	L	H
OPEN	OPEN	L	L	L	H	L
X	X	H	X	Z	Z	Z
X	X	X	H	X	Z	Z
X	X	OPEN	OPEN	Z	Z	Z

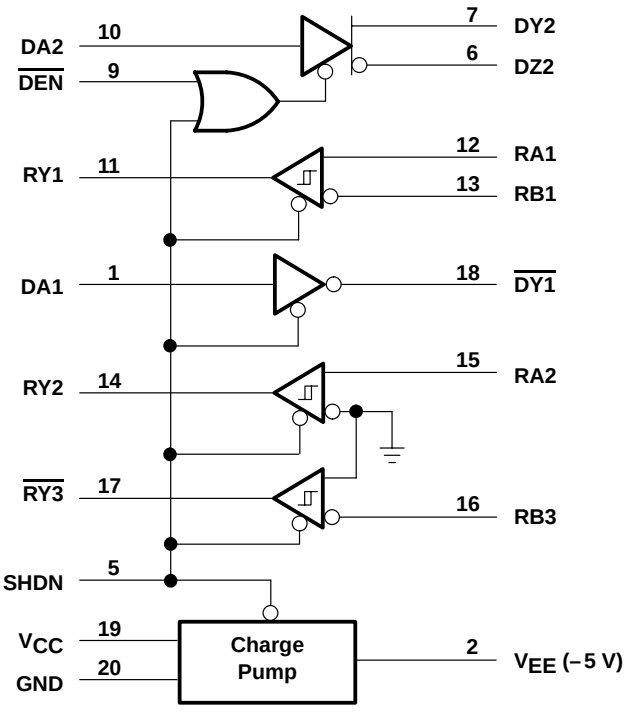
† H = high level L = low level X = irrelevant ? = indeterminate Z = high impedance (off)

RECEIVER FUNCTION TABLE†

INPUT RA1	INPUT RB1	INPUT RA2 & RB3	ENABLE SHDN	OUTPUT RY1	OUTPUT RY2	OUTPUT $\overline{\text{RY3}}$
H	L	H	L	H	H	L
L	H	L	L	L	L	H
OPEN		OPEN	L	H	H	H
SHORT‡		SHORT‡	L	?	?	?
X	X	X	H	Z	Z	Z
X	X	X	OPEN	Z	Z	Z

† H = high level L = low level X = irrelevant ? = indeterminate Z = high impedance (off)
‡ $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$

function logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 to 7 V
Negative supply voltage range, V_{EE} (see Note 1) . . . . . –7 to 0.5 V
Receiver input voltage range (RA, RB) . . . . . –15 V to 15 V
Receiver differential input voltage range, V_{ID} . . . . . –12 to 12 V
Receiver output voltage range (RY) . . . . . –0.5 V to 5.5 V
Driver output voltage range (Power Off) ($\overline{DY1}$, DY2, DZ2) . . . . . –15 V to 15 V
Driver output voltage range (Power On) ($\overline{DY1}$, DY2, DZ2) . . . . . –11 V to 11 V
Driver input voltage range (DA, SHND, $\overline{DEN}$) . . . . . –0.5 V to V_{CC+} 0.4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Electrostatic discharge (see Note 2): (Bus terminals), Class 3, A . . . . . 6 kV
(Bus terminals), Class 3, B . . . . . 500 V
(All terminals), Class 3, A . . . . . 6 kV
(All terminals), Class 3, B . . . . . 500 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal unless otherwise noted.
2. This parameter is measured in accordance with MIL-STD-883C, Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1035 mW	8.3 mW/°C	660 mW
DW	1125 mW	9.0 mW/°C	720 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DA, SHDN, $\overline{DEN}$	2		5.25	V
Low-level input voltage, V_{IL}	DA, SHDN, $\overline{DEN}$			0.8	V
Receiver common-mode input voltage, V_{IC}		–7		7	V
Receiver differential input voltage, V_{ID}		–12		12	V
Voltage-converter filter capacitance		0.2			μF
Voltage-converter filter-capacitor equivalent series resistance (ESR)				0.2	Ω
Operating free-air temperature, T_A		0		70	°C

driver electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Single ended, See Figure 1	R_L = 12 kΩ	3.6	4.53		V
			R_L = 120 Ω	2	3.63		V
V_{OL}	Low-level output voltage		R_L = 12 kΩ		–4.53	–3.6	V
			R_L = 120 Ω		–2.7	–1.8	V
$\|V_{OD}\|$	Magnitude of differential output voltage $\|(V_{(DY)} – V_{(DZ)}\|$	R_L = 120 Ω, See Figure 2		4			V
$\Delta\|V_{OD}\|$	Change in differential voltage magnitude					250	mV
V_{OC}	Common-mode output voltage	See Figure 3		–1		3	V
$\|\Delta V_{OC(SS)}\|$	Magnitude of change, common-mode steady state output voltage					200	mV
$\|\Delta V_{OC(PP)}\|$	Magnitude of change, common-mode peak-to-peak output voltage				700		mV
I_{CC}	Supply current	SHDN = $\overline{DEN}$ = 0 V,	No load		7	15	mA
		SHDN = $\overline{DEN}$ = 5 V,	No load			100	μA
I_{OZ}	High-impedance output current	V_O = –10 V to 10 V,	V_{CC} = 0 or 5 V			±100	μA
I_{OS}	Short-circuit output current (see Note 3)	V_O = –5 V to 5 V			±170	±450	mA

NOTE 3: Not more than one output should be shorted at one time.

driver switching characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output		Single ended, See Figure 4		42	75	ns
t_{PLH}	Propagation delay time, low-to-high level output				41	75	ns
t_{PZL}	Driver output enable time to low-level output	SHDN			25	100	µs
t_{PZH}	Driver output enable time to high-level output	SHDN			25	100	µs
t_{PLZ}	Driver output disable time from low-level output	SHDN			28	100	ns
t_{PHZ}	Driver output disable time from high-level output	SHDN			37	100	ns
t_r	Rise time			10	25	75	ns
t_f	Fall time			10	23	75	ns
t_{PHL}	Propagation delay time, high-to-low level output		Differential, See Figure 5		40	75	ns
t_{PLH}	Propagation delay time, low-to-high level output				42	75	ns
t_{PZL}	Driver output enable time to low-level output	SHDN			25	100	µs
		$\overline{DEN}$			29	150	ns
t_{PZH}	Driver output enable time to high-level output	SHDN			25	100	µs
		$\overline{DEN}$			35	150	ns
t_{PLZ}	Driver output disable time from low-level output	SHDN			28	100	ns
		$\overline{DEN}$			34	100	ns
t_{PHZ}	Driver output disable time from high-level output	SHDN			37	100	ns
		$\overline{DEN}$			34	100	ns
t_r	Rise time			10	27	75	ns
t_f	Fall time			10	26	75	ns
$t_{SK(p)}$	Pulse skew, $\lvert t_{PLH} - t_{PHL} \rvert$					22	ns

receiver electrical characteristics over operating free-air temperature range (unless otherwise noted)

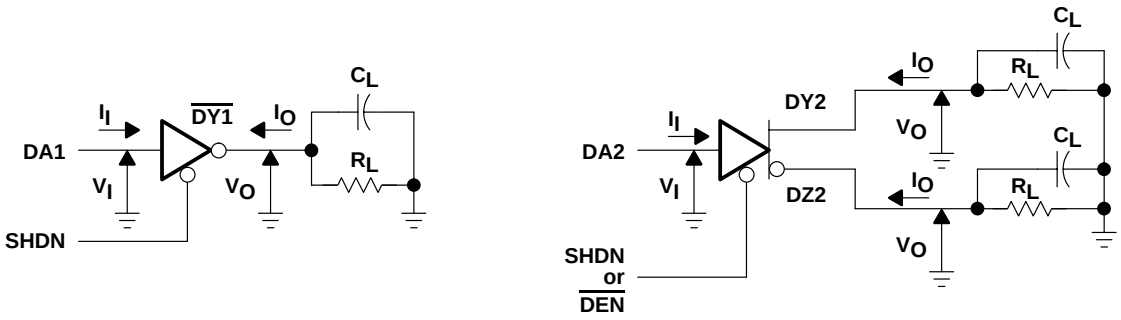
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 6			200	mV
V_{IT-}	Negative-going input threshold voltage		–200			
V_{hys}	Differential input voltage hysteresis ($V_{IT+} - V_{IT-}$)			50		mV
V_{OH}	High-level output voltage (see Note 4)	V_{IC} = 0, I_{OH} = –2 mA, See Figure 6	2	4.9		V
V_{OL}	Low-level output voltage	V_{IC} = 0, I_{OL} = 2 mA, See Figure 6		0.2	0.8	V
I_{OS}	Short-circuit output current	V_O = 0	–85	–45		mA
		$V_O = V_{CC}$		47	+85	
R_I	Input resistance	V_{CC} = 0 or 5.25 V, V_I = –12 V to 12 V	6	30		kΩ

NOTE 4: When the inputs are left unconnected, receivers one and two interpret these as high-level inputs and receiver three interprets these as low-level inputs so that all outputs are at a high level.

receiver switching characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 2 kΩ, See Figure 6	C_L = 15 pF,		31	75	ns
t_{PLH}	Propagation delay time, low-to-high level output				30	75	ns
t_r	Rise time				15	30	ns
t_f	Fall time				15	30	ns
$t_{SK(P)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$					20	ns
t_{PZL}	Receiver output enable time to low level output	Differential, See Figure 7	C_L =50 pF,		35	100	ns
t_{PZH}	Receiver output enable time to high level output				32	100	ns
t_{PLZ}	Receiver output disable time from low level output				21	100	ns
t_{PHZ}	Receiver output disable time from high level output				21	100	ns
t_{PZL}	Receiver output enable time to low level output	Single ended, See Figure 7	C_L =50 pF,		12	25	µs
t_{PZH}	Receiver output enable time to high level output				12	25	µs
t_{PLZ}	Receiver output disable time from low level output				25	100	ns
t_{PHZ}	Receiver output disable time from high level output				125	400	ns

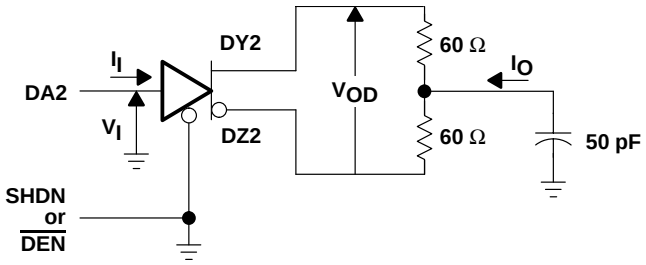
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L = 50 pF

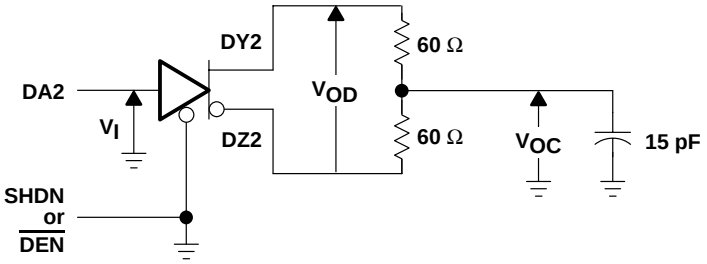
TEST CIRCUIT

Figure 1. Single-Ended Driver DC Parameter Test

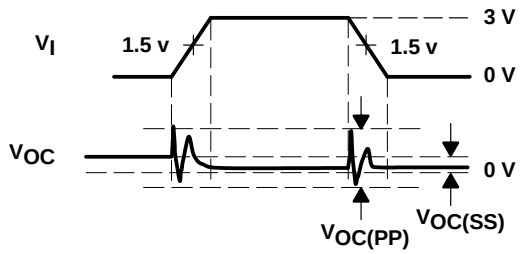


TEST CIRCUIT

Figure 2. Differential Driver DC Parameter Test



TEST CIRCUIT (see Note A)

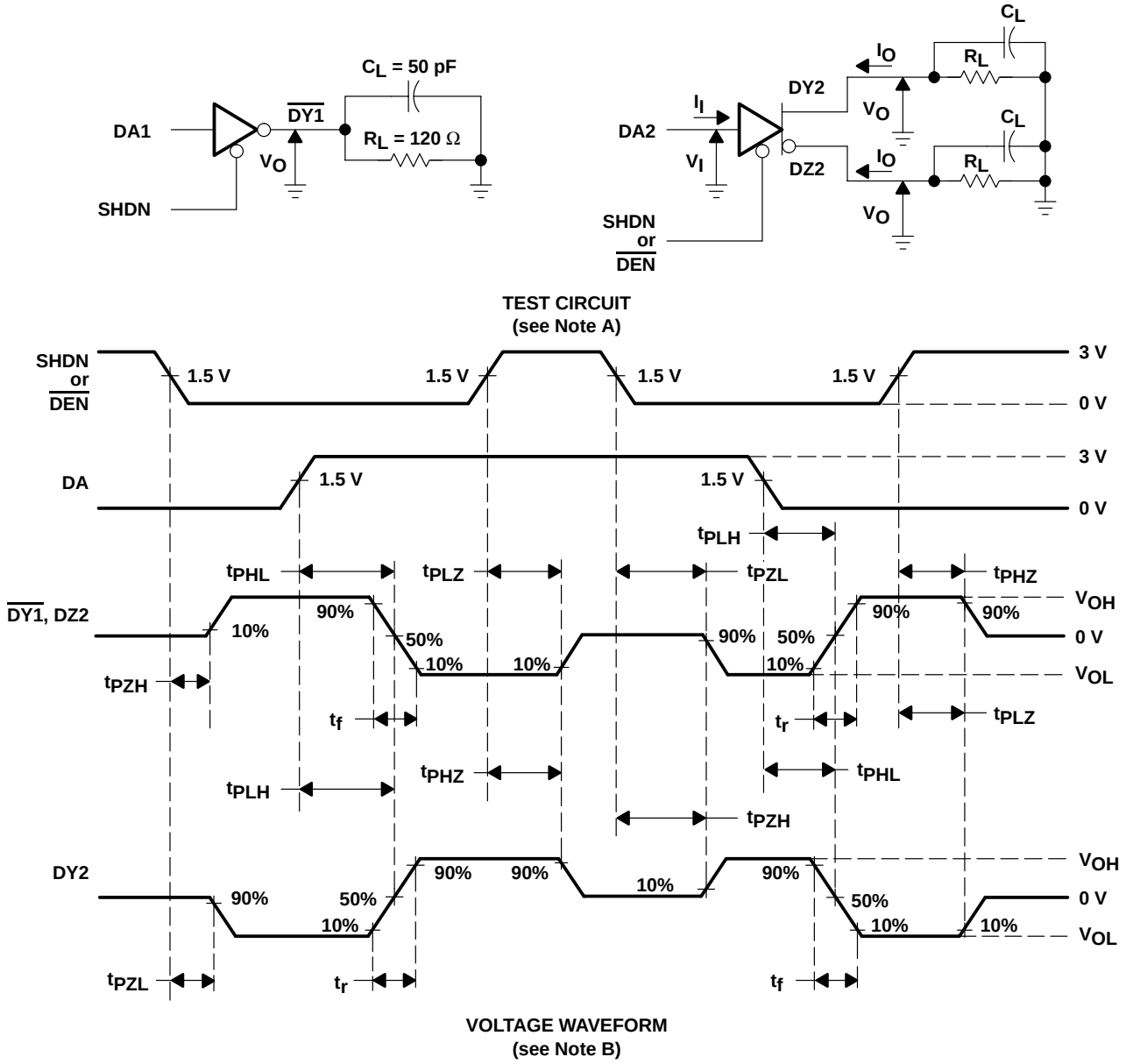


VOLTAGE WAVEFORM

NOTE A: Measured 3dB bandwidth = 300 MHz

Figure 3. Differential-Driver Common-Mode Output Voltage Tests

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L = 50 pF, R_L = 120 Ω
B. The input waveform t_r, $t_f \leq$ 10 ns.

Figure 4. Single-Ended Driver Propagation and Transition Times

PARAMETER MEASUREMENT INFORMATION

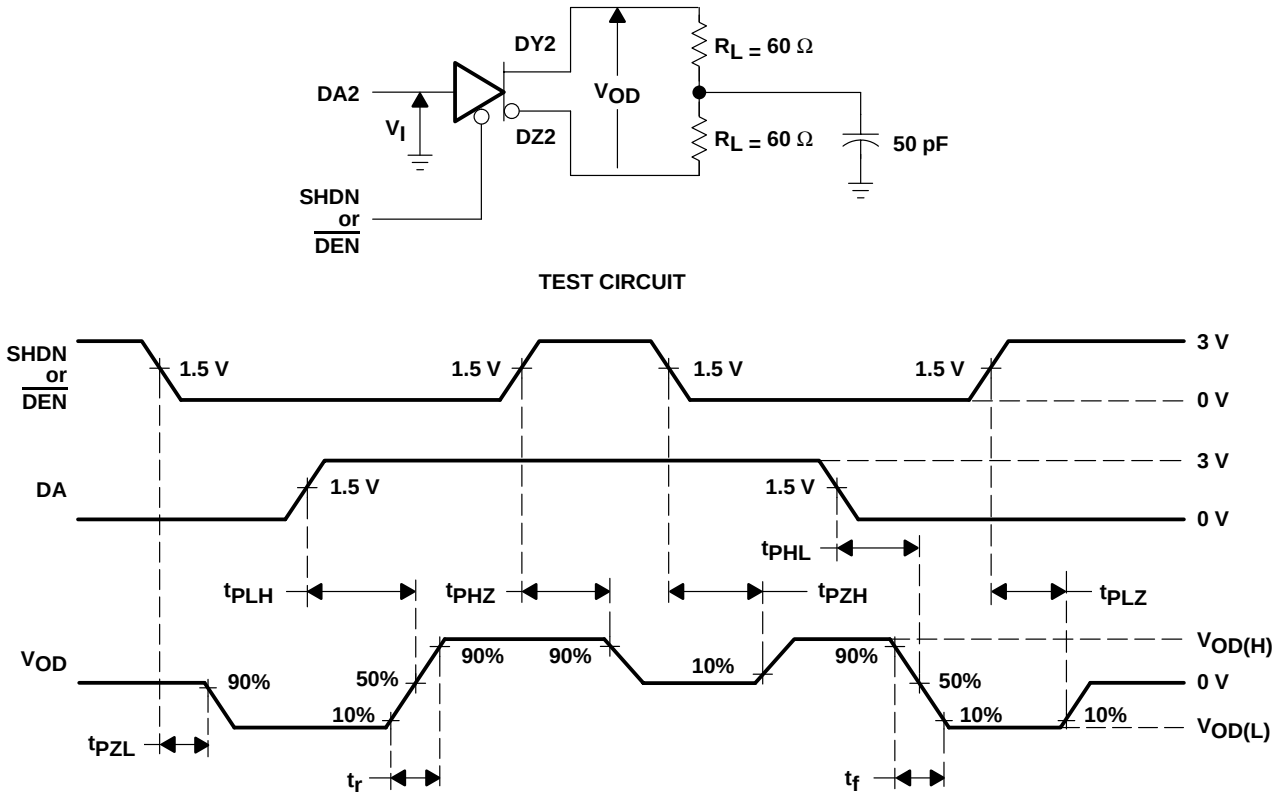


Figure 5. Differential Driver Propagation and Transition Times

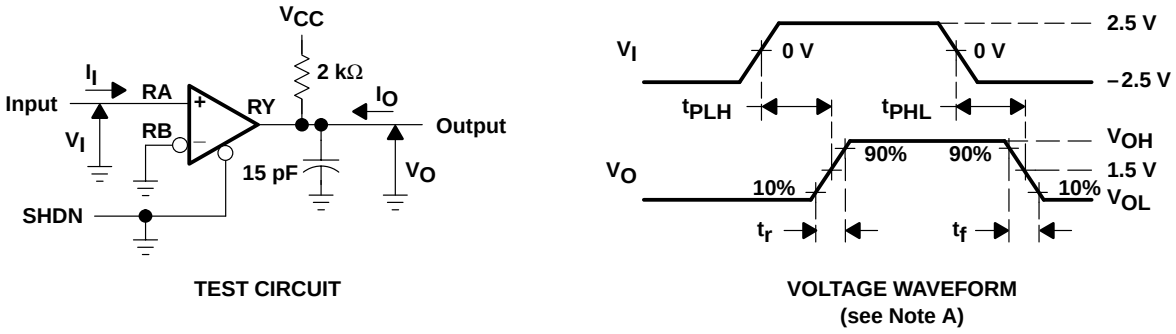
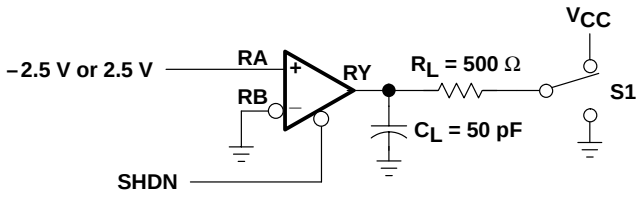


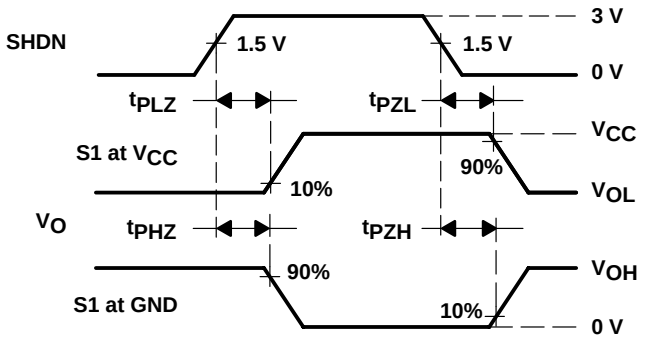
Figure 6. Receiver Propagation and Transition Times

NOTE A: The input waveform t_r, $t_f \leq 10$ ns.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

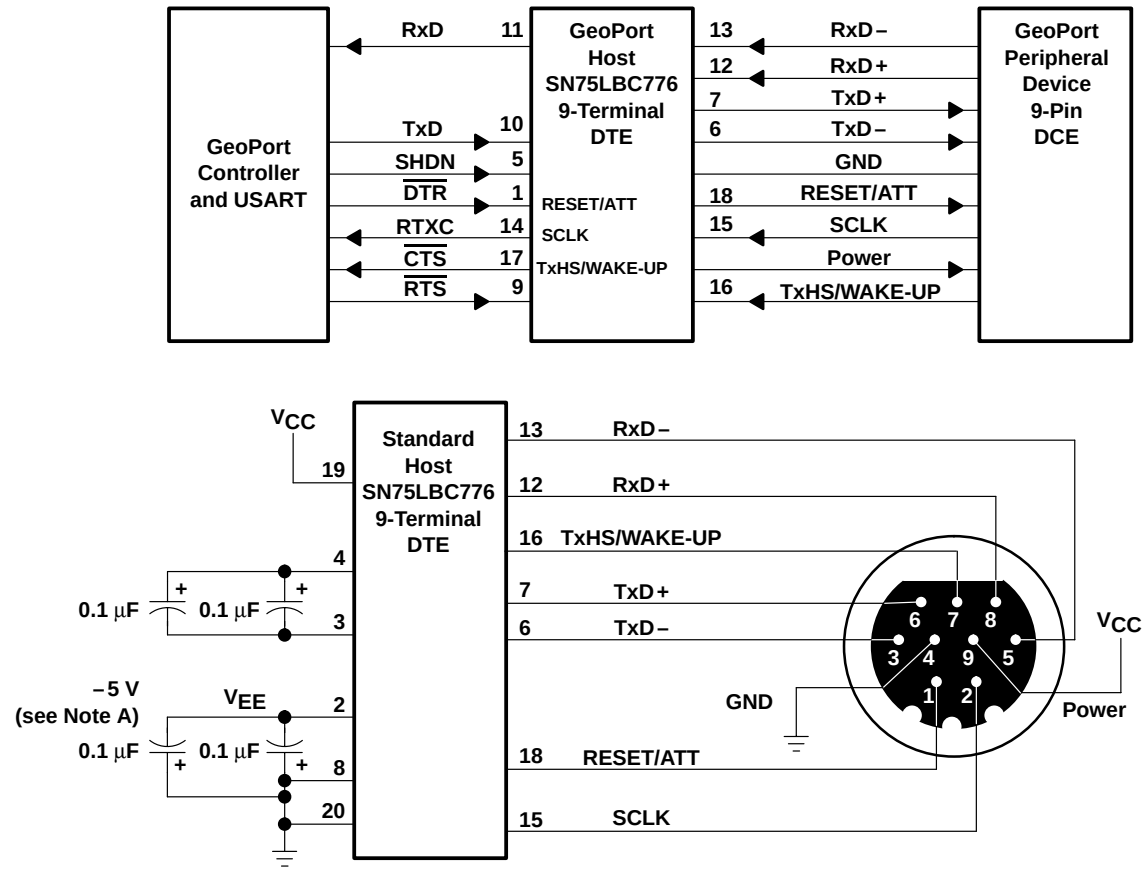


VOLTAGE WAVEFORM
(see Note A)

NOTE A: The input waveform t_r, $t_f \leq 10$ ns.

Figure 7. Receiver Enable and Disable Test Circuit and Waveforms

APPLICATION INFORMATION



NOTE A: The AVX 0603YC104MATXA or equivalent is one of the possible capacitors that can be used as the charge pump capacitor.

Figure 8. GeoPort 9-Terminal DTE Connection Application

APPLICATION INFORMATION

generator characteristics

PARAMETER		TEST CONDITIONS	EIA/TIA-232/V.28		EIA/TIA-423/V.10		562		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$\|V_O\|$	Output voltage magnitude	Open circuit		25	4	6		13.2	V
		$3\ k\Omega \le R_L \le 7\ k\Omega$	5	15	NA		3.7		V
		$R_L = 450\ \Omega$	NA		3.6		NA		V
$V_{O(RING)}$	Output voltage ringing		NA			10%		5%	
I_{OS}	Short-circuit output current	$V_O = 0$		100		150		60	mA
$I_{O(OFF)}$	Power-off output current	$V_{CC} = 0$, $\|V_O\| < 2$ V	300		NA		300		Ω
		$V_{CC} = 0$, $\|V_O\| < 6$ V	NA			±100	NA		µA
SR	Output voltage slew rate			30	NA		4	30	V/µs
t_t	Transition time	±3.3 V to ±3.3 V	NA		NA		0.22	2.1	µs
		±3 V to ±3 V		0.04	NA		NA		ui†
		10% to 90%	NA			0.3	NA		ui†

† ui is the unit interval and is the inverse of the signaling rate (bit transmit time).

receiver characteristics

PARAMETER		TEST CONDITIONS	EIA/TIA-232/V.28		EIA/TIA-423/V.10		562		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$\|V_I\|$	Input voltage magnitude			25		10		25	V
V_{IT}	Input voltage threshold	$\|V_I\| < 15$ V	−3	3	NA		−3	3	V
		$\|V_I\| < 10$ V	NA		−0.2	0.2	NA		
R_I	Input resistance	$3\ V < \|V_I\| < 15$ V	3	7	NA		3	7	kΩ
		$\|V_I\| < 10$ V	NA		4		NA		kΩ

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LBC776DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LB776	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

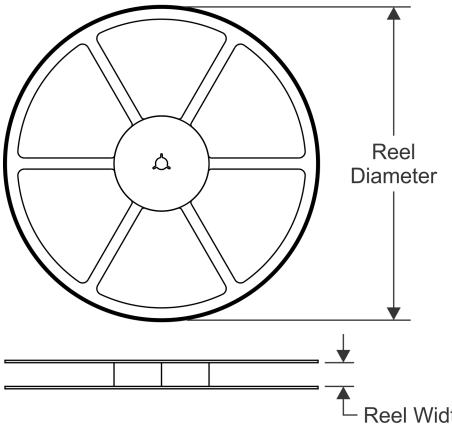
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

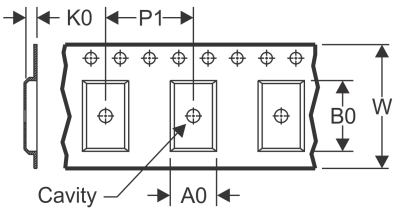
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

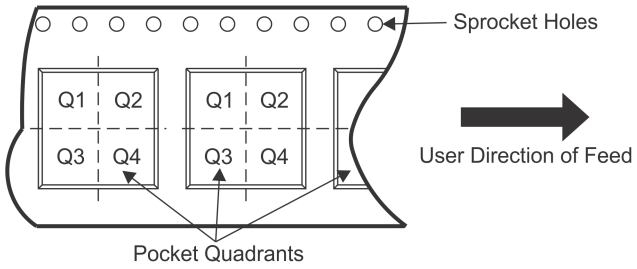


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

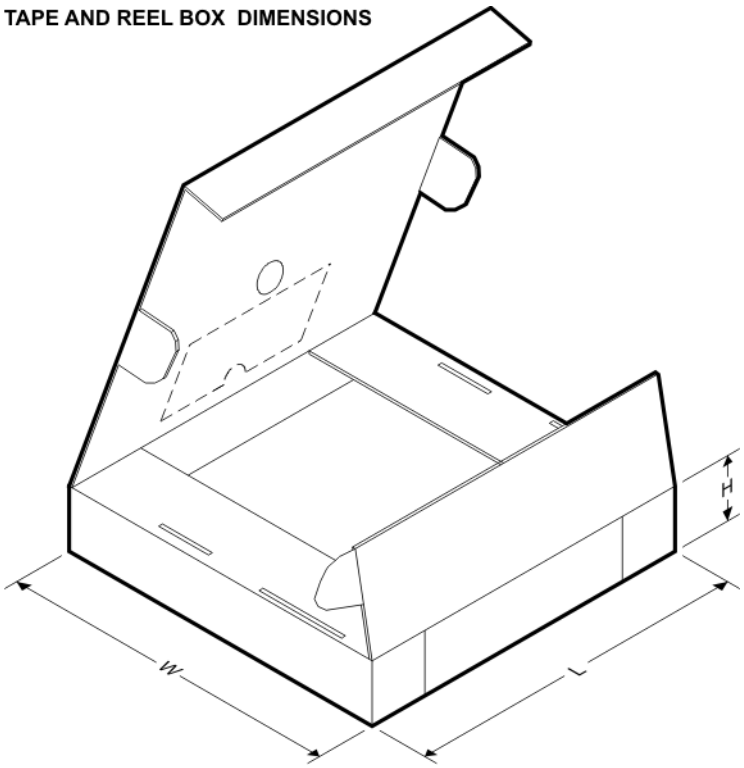
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC776DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

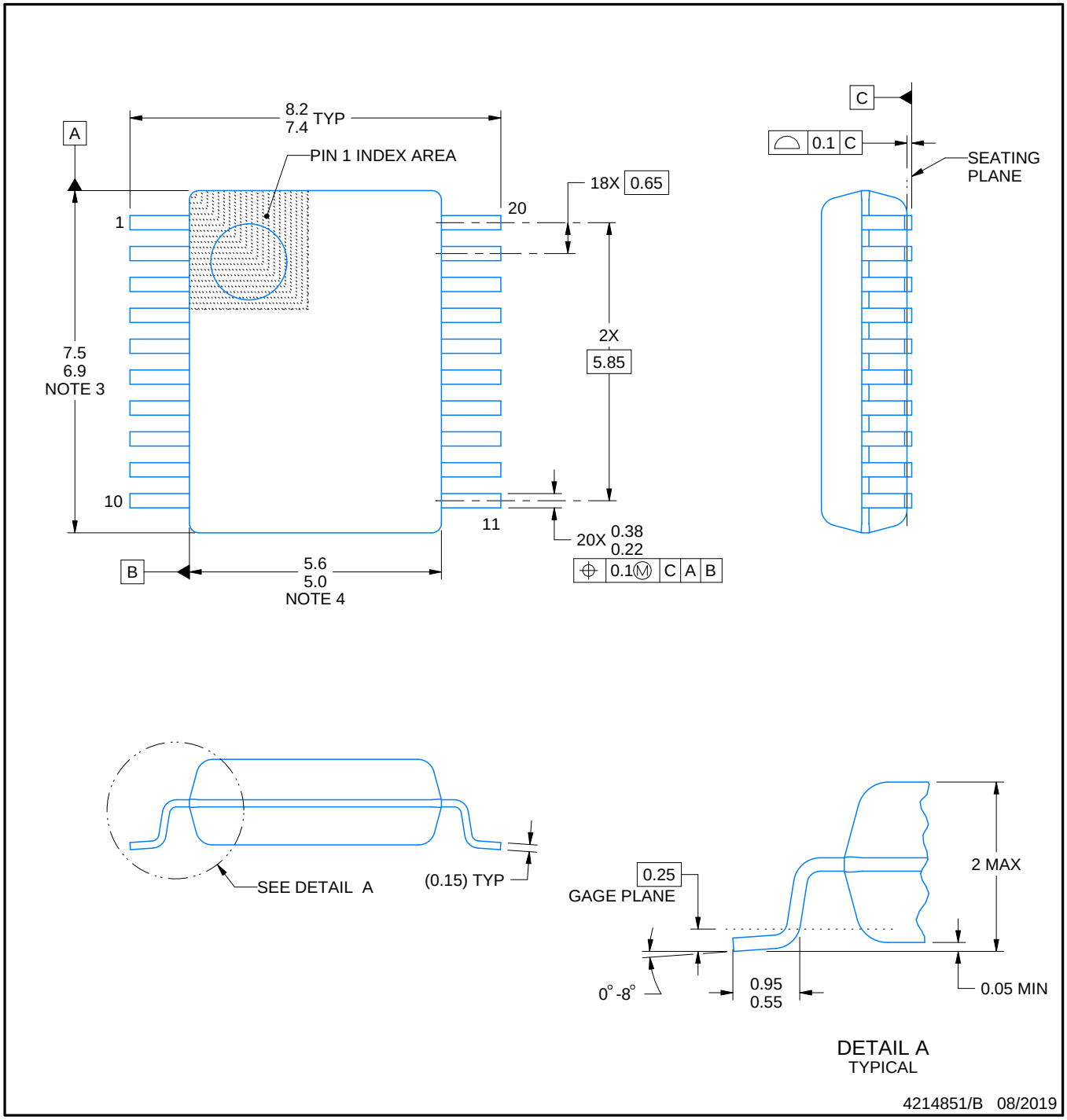
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC776DBR	SSOP	DB	20	2000	853.0	449.0	35.0

PACKAGE OUTLINE

DB0020A

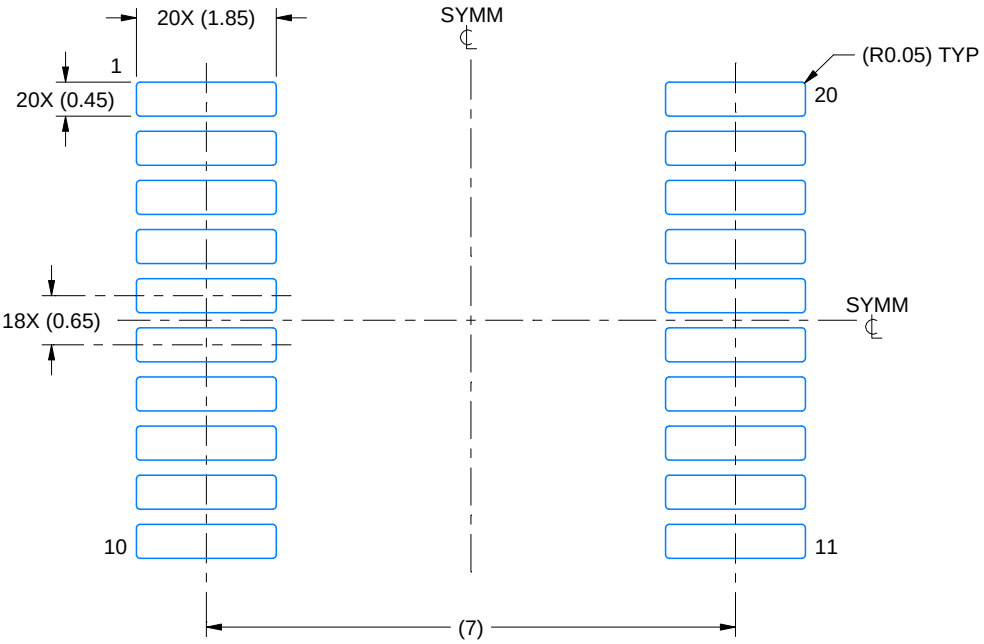
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

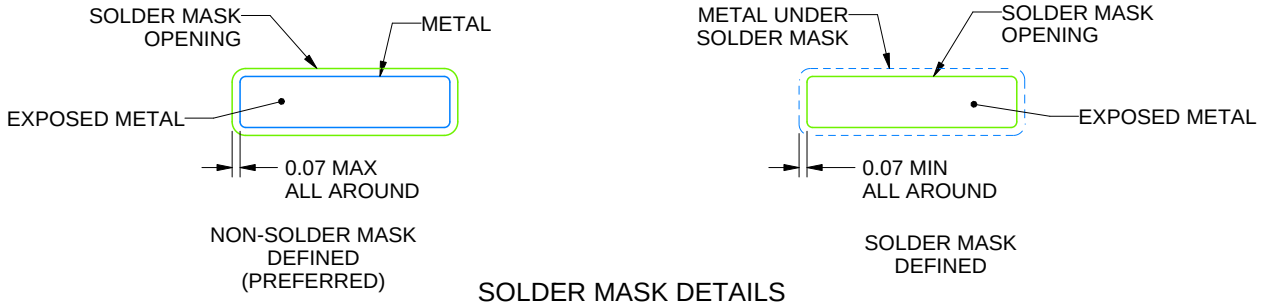


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

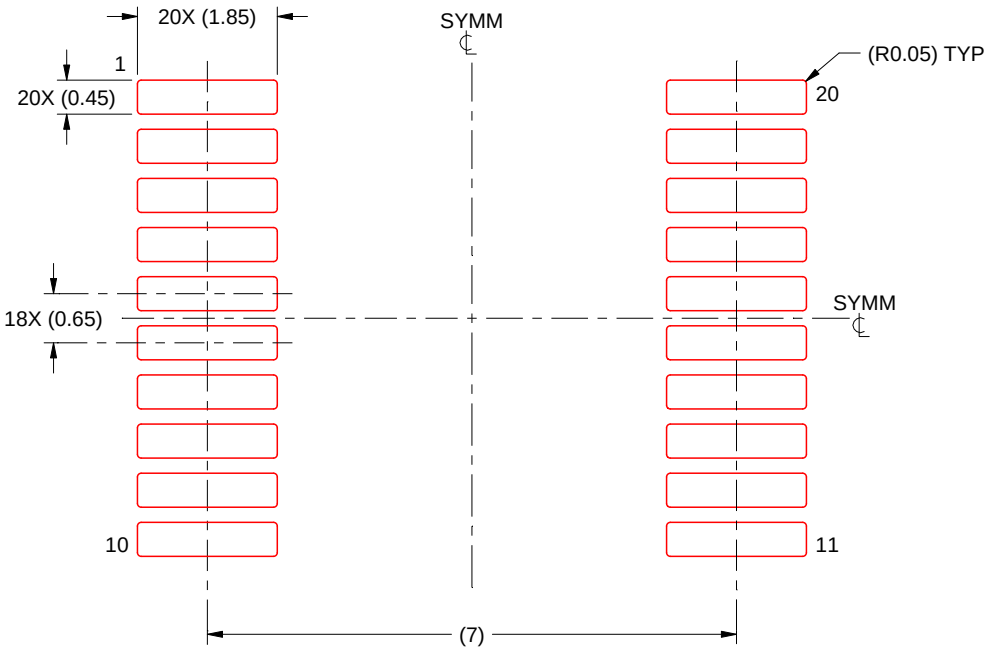
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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