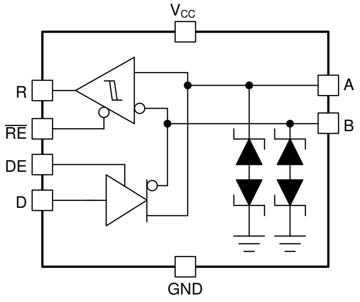
THVD14x9x 3.3-V to 5-V RS-485 Transceivers With 4-kV Surge Protection and 1.8-V VIO Capability

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3-V to 5.5-V Supply Voltage
- V_{IO} Support from 1.65-V to VCC supply level (THVD1439V, THVD1449V)
- Bus I/O protection
  - ± 4-kV IEC 61000-4-5 1.2/50-µs surge
  - ± 15-kV IEC 61000-4-2 Contact discharge
  - ± 15-kV IEC 61000-4-2 Air-gap discharge
  - ± 4-kV IEC 61000-4-4 Electrical fast transient
  - ± 15-kV HBM ESD
  - ± 15-V DC bus fault
- Available in two speed grades
  - THVD1439, THVD1439V: 250 kbps
  - THVD1449, THVD1449V: 12 Mbps
- Extended ambient temperature range: -40°C to 125°C
- Extended operational common-mode range: ± 12 V
- Large receiver hysteresis for noise rejection
- Low Power Consumption
  - Standby supply current: < 1 µA
  - Current during operation: < 5 mA
- Glitch-free power-up/down for hot plug-in capability
- Open, short, and idle bus failsafe
- 1/8 Unit load (up to 256 bus nodes)
- Industry standard 8-pin SOIC for drop-in compatibility



THVD14x9 Block Diagram

2 Applications

- Wireless infrastructure
- Factory automation
- Motor drives
- Building automation
- HVAC
- Grid infrastructure

3 Description

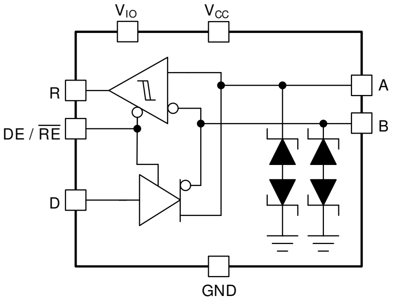
THVD14x9(V) devices are half-duplex RS-485 transceivers with integrated surge protection. Surge protection is achieved by integrating transient voltage suppressor (TVS) diodes in the standard 8-pin SOIC (D) package. This feature increases the reliability by providing better immunity to noise transients coupled to the data cable which eliminates the need for external protection components.

THVD1439 and THVD1449 operate from a single 3.3-V or 5-V supply. The THVD1439V and THVD1449V devices support an additional V_{IO} supply to operate the IOs from 1.65 V to VCC supply level. The devices in this family feature a wide common-mode voltage range making them suitable for multi-point applications over long cable runs.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
THVD1439 THVD1439V THVD1449 THVD1449V	SOIC (8)	4.90 mm × 3.91 mm

[1] For all available devices, see the orderable addendum at the end of the data sheet.



THVD14x9V Block Diagram

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4 Revision History

Changes from Revision * (April 2021) to Revision A (June 2021) **Page**

- Changed THVD1439, THVD1449 and THVD1449V from *Product Preview* to *Advanced Information* 1

Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	V_{IO}	SIGNALING RATE	NODES
THVD1439	Half	Separate DE and $\overline{RE}$	No	up to 250 kbps	256
THVD1439V		Combined DE / $\overline{RE}$	Yes		
THVD1449		Separate DE and $\overline{RE}$	No	up to 12 Mbps	
THVD1449V		Combined DE / $\overline{RE}$	Yes		

5 Pin Configuration and Functions

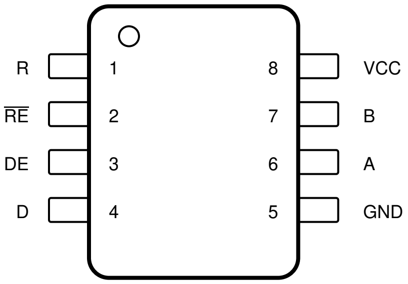

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Figure 5-1. D Package (Non-V), 8-Pin (SOIC), Top View

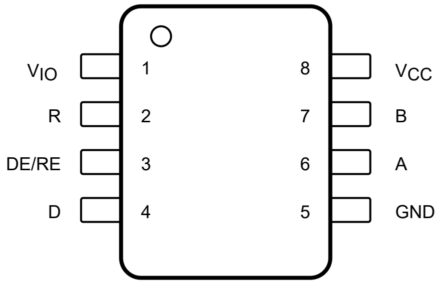

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Figure 5-2. D Package (V), 8-Pin (SOIC), Top View

PIN			I/O	DESCRIPTION
NAME	**Non-V**	**V**		
V_{IO}	-	1	Power	IO 1.8-V to 5-V supply, for R, D, and $\overline{\text{RE}}$/DE
R	1	2	Digital output	Receive data output
$\overline{\text{RE}}$	2	-	Digital input	Receiver enable, active low (2 MΩ internal pull-up)
DE	3	-	Digital input	Driver enable, active high
DE/ $\overline{\text{RE}}$	-	3	Digital Input	Driver enable (Active high), Receiver enable (Active Low). (2 MΩ internal pull-down)
D	4	4	Digital input	Driver data input
GND	5	5	Ground	Device ground
A	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	Bus input/output	Bus I/O port, B (complementary to A)
V_{CC}	8	8	Power	3.3-V to 5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	7	V
Logic supply voltage	V_{IO}	-0.5	V_{CC}+0.2	V
Bus voltage	Range at any bus pin (A or B)	–15	15	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$) THVD1439, THVD14149	–0.3	5.7	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$) THVD1439V, THVD1449V	–0.3	V_{IO}+0.2	V
Receiver output current	I_O	–24	24	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	Bus terminals	±15,000	V
			All pins except bus terminals	±4,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 ESD Ratings, IEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact Discharge, per IEC 61000-4-2	Bus terminals	±15,000	V
		Air-Gap Discharge, per IEC 61000-4-2		±15,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V
$V_{(surge)}$	Surge	Per IEC 61000-4-5, 1.2/50 µs	Bus terminals	±4,000	V

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	IO Supply Voltage (V Variant)		1.65		V_{CC}	V
V_I	Input voltage on logic pins		-0.5		V_{IO}	V
V_I	Input voltage at any bus terminal[1]		-12		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	THVD1439V, THVD1449V	0.67 * V_{IO}			V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)				0.33 * V_{IO}	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	THVD1439, THVD1449	2			V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)				0.8	V
V_{ID}	Differential input voltage		-12		12	V
I_O	Output current, driver		-60		60	mA
I_{OR}	Output current, receiver		-8		8	mA
R_L	Differential load resistance		54			Ω
$1/t_{UI}$	Signaling rate	THVD1439, THVD1439V			250	kbps
		THVD1449, THVD14149V			12	Mbps
T_A	Operating ambient temperature		-40		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.5 Thermal Information

THERMAL METRIC[1]		THVD1439 THVD1439V THVD1449 THVD1449V	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Dissipation

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			VALUE	UNIT
PD	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, 50% duty cycle square wave at signaling rate	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	THVD1439	250 kbps	180	mW
			THVD1449	12 Mbps	300	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	THVD1439	250 kbps	240	mW
			THVD1449	12 Mbps	350	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	THVD1439	250 kbps	290	mW
			THVD1449	12 Mbps	400	

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, -12 V ≤ V_{test} ≤ 12 V (See Figure 7-1)			1.5	2		V
		R_L = 60 Ω, -12 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See Figure 7-1)			2.1			V
		R_L = 100 Ω (See Figure 7-2)			2	2.5		V
		R_L = 54 Ω (See Figure 7-2)			1.5	2		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω (See Figure 7-2)			–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω (See Figure 7-2)			1	V_{CC} / 2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω (See Figure 7-2)			–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -12 V ≤ V_O ≤ 12 V			–250		250	mA
Receiver								
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V			75	135	μA
			V_I = -7 V		–100	–40		
			V_I = -12 V		–135	–75		
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of ±12 V			40	125	200	mV
V_{TH-}	Negative-going input threshold voltage(1)				–200	–125	–40	mV
V_{HYS}	Input hysteresis					250		mV
V_{TH_HYS}	Input fail-safe threshold				–40		40	mV
V_{OH}	Output high voltage	I_{OH} = -8 mA			V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA				0.2	0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	μA
Logic								
I_{IN}	Input current (D, DE/$\overline{RE}$) (V Variant)	3 V ≤ V_{CC} ≤ 5.5 V, 1.65 ≤ V_{IO} ≤ V_{CC} V, 0 V ≤ V_{IN} ≤ V_{IO}			–5		5	μA
I_{IN}	Input current (D, DE, $\overline{RE}$)	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}			–5		5	μA
Thermal Protection								
T_{SHDN}	Thermal shutdown threshold	Temperature rising			150	170		℃
T_{HYS}	Thermal shutdown hysteresis					10		℃
Supply								
I_{CC}	Supply current (quiescent)	V_{CC}=3.6 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{CC}, No load		3	4	mA
			Driver enabled, receiver disabled (Non V only)	$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2	3	mA
			Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		1	2	mA
			Driver and receiver disabled (Non V only)	$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1.5	μA
	Supply current (quiescent)	V_{CC}=5.5 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{CC}, No load		3.5	5	mA
			Driver enabled, receiver disabled (Non V only)	$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2.5	3.8	mA
			Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		1.5	2.4	mA
			Driver and receiver disabled (Non V only)	$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	3	μA

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{IO}	VIO supply current (quiescent)	THVD1439V, THVD1449V	Driver Enabled	DE/$\overline{\text{RE}}$=V_{IO}, D=open, No load			5	µA
			Receiver enabled	DE/$\overline{\text{RE}}$= 0 V, D=open, No load			5	µA

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(1) Under any specific conditions, V_{TH+} isassured to be at least V_{HYS} higher than$V_{TH–}$.

6.8 Switching Characteristics (THVD1439, THVD1439V)

250-kbps devices (THVD1439, 39V), over recommended operating conditions. All typical values are at 25 ℃.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 7-3	300	700	1200	ns
t_{PHL}, t_{PLH}	Propagation delay				450	650	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					40	ns
t_{PHZ}, t_{PLZ}	Disable time		See Figure 7-4 and Figure 7-5		50	200	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			300	600	ns
		$\overline{RE}$ = V_{CC}			2	4	μs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{CC}		50		500	ns
Receiver							
t_r, t_f	Differential output rise/fall time	C_L = 15 pF	See Figure 7-6		13	25	ns
t_{PHL}, t_{PLH}	Propagation delay				70	110	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					7	ns
t_{PHZ}, t_{PLZ}	Disable time				45	60	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = V_{CC}	See Figure 7-7		120	185	ns
		DE = 0 V	See Figure 7-8		4	10	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See Figure 7-9	14	25	36	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			25	35	66	ns
t_{SHDN}	Time to shutdown	DE = 0 V		50		500	ns

6.9 Switching Characteristics (THVD1449, THVD1449V)

12-Mbps devices (THVD1449, 49V), over recommended operating conditions. All typical values are at 25 ℃.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 7-3	2	10	25	ns
t_{PHL}, t_{PLH}	Propagation delay			7	15	25	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					3.5	ns
t_{PHZ}, t_{PLZ}	Disable time		See Figure 7-4 and Figure 7-5		30	75	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			30	65	ns
		$\overline{RE}$ = V_{CC}			2	4	μs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{CC}		50		500	ns
Receiver							
t_r, t_f	Differential output rise/fall time	C_L = 15 pF	See Figure 7-6		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay			40	55	73	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					2	ns
t_{PHZ}, t_{PLZ}	Disable time				15	30	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = V_{CC}	See Figure 7-7		90	130	ns
		DE = 0 V	See Figure 7-8		4	10	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See Figure 7-9	14	25	36	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			25	35	55	ns
t_{SHDN}	Time to shutdown	DE = 0 V		50		500	ns

7 Parameter Measurement Information

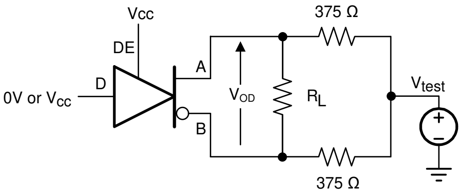

Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

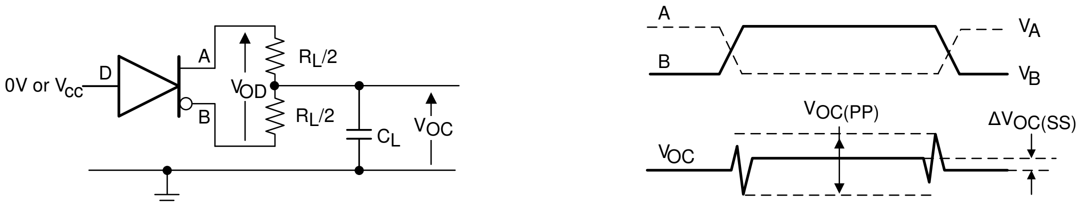

Figure 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

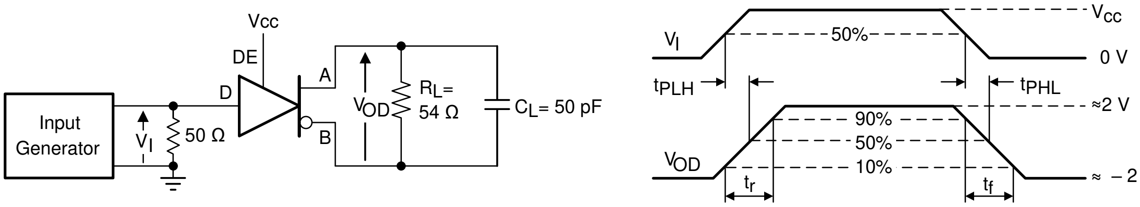

Figure 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

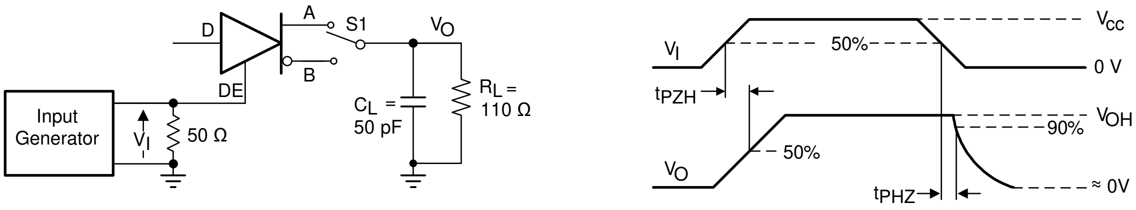

Figure 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

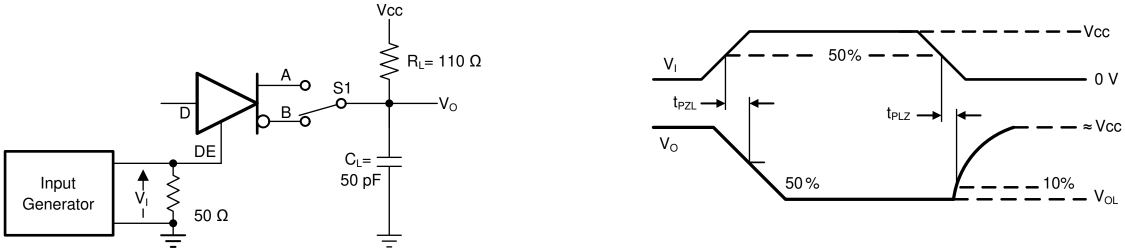

Figure 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

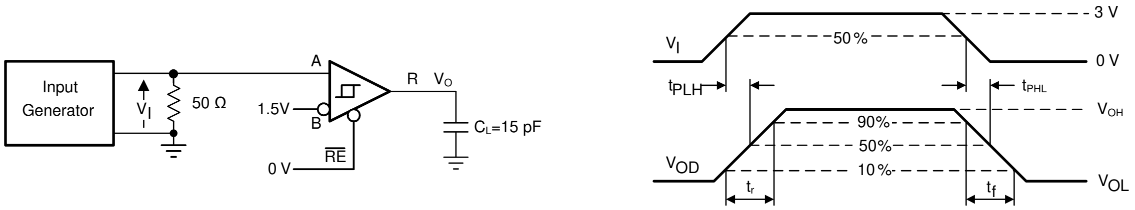

Figure 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

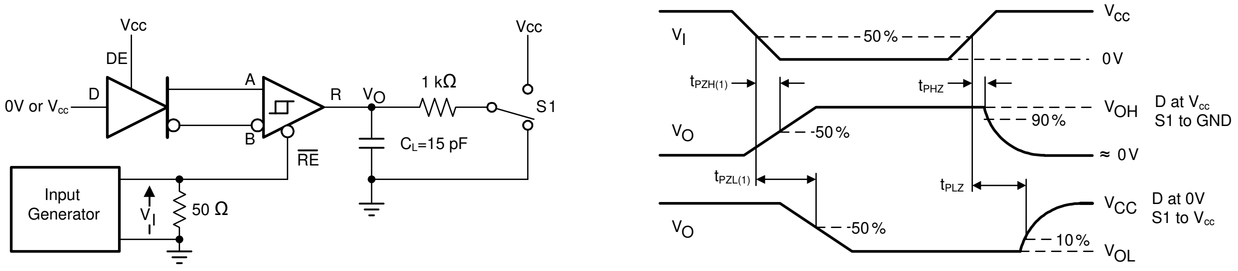

Figure 7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

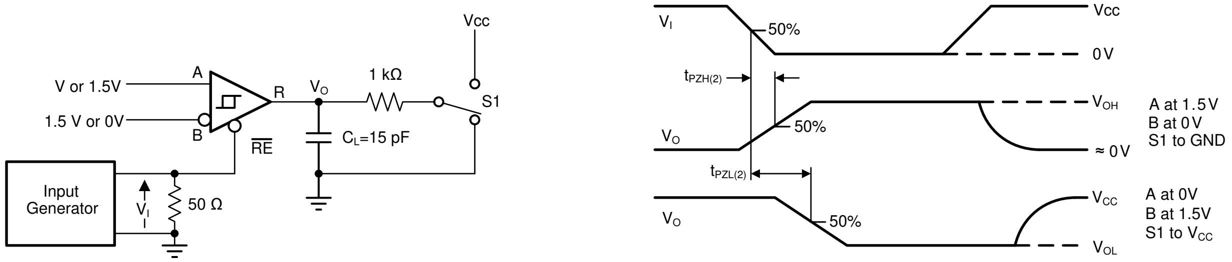

Figure 7-8. Measurement of Receiver Enable Times With Driver Disabled

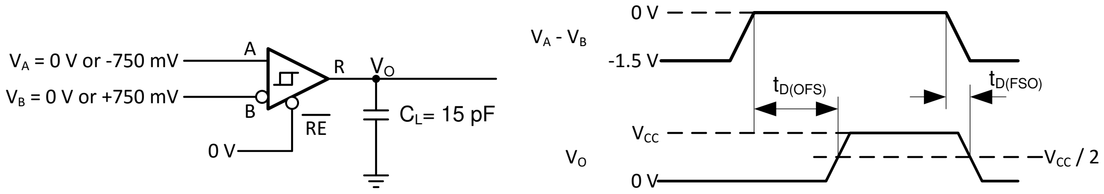

Figure 7-9. Fail-Safe Delay Measurements

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

THVD14x9(V) devices are surge-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 250 kbps and 12 Mbps respectively. Surge protection is achieved by integrating transient voltage suppressor (TVS) diodes in the standard 8-pin SOIC (D) package.

THVD1439 and THVD1449 devices have active-high driver enables and active-low receiver enables. A standby current of less than 1.5 µA can be achieved by disabling both driver and receiver. THVD1439V and THVD1449V have a single enable/diable pin that either enables the driver or the receicer at a time.

8.2 Functional Block Diagrams

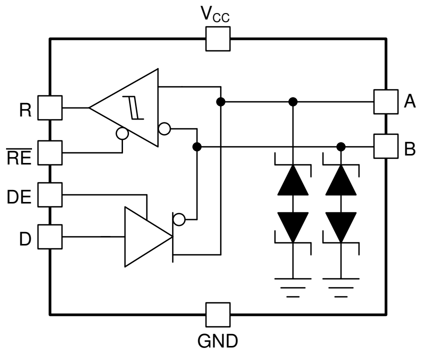

Figure 8-1. THVD1439 and THVD1449 Block Diagram

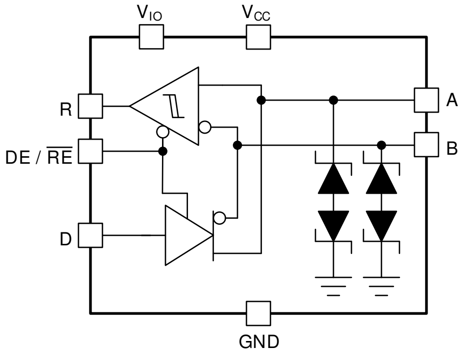

Figure 8-2. THVD1439V and THVD1449V Block Diagram

8.3 Feature Description

8.3.1 Electrostatic Discharge (ESD) Protection

The bus pins of the THVD14x9(V) transceiver family include on-chip ESD protection against ±15-kV HBM and ±15-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

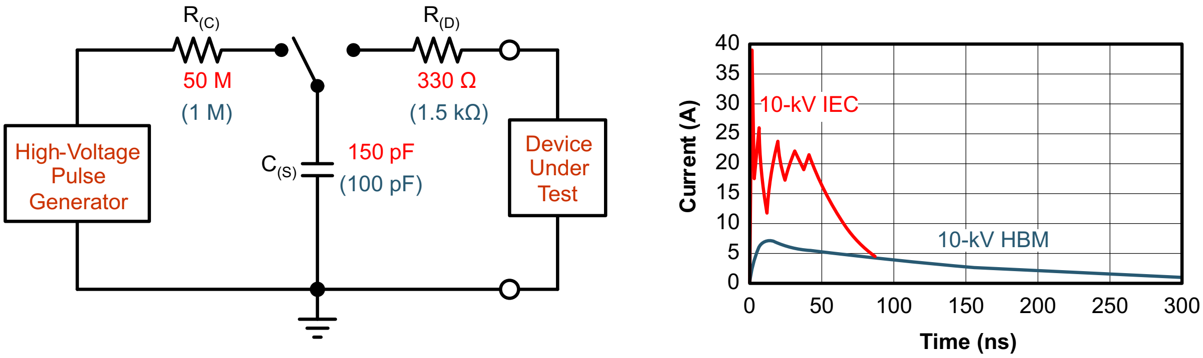

Figure 8-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables.

8.3.2 Electrical Fast Transient (EFT) Protection

Inductive loads such as relays, switch contactors, or heavy-duty motors can create high-frequency bursts during transition. The IEC 61000-4-4 test is intended to simulate the transients created by such switching of inductive loads on AC power lines. Figure 8-4 shows the voltage waveforms in to 50-Ω termination as defined by the IEC standard.

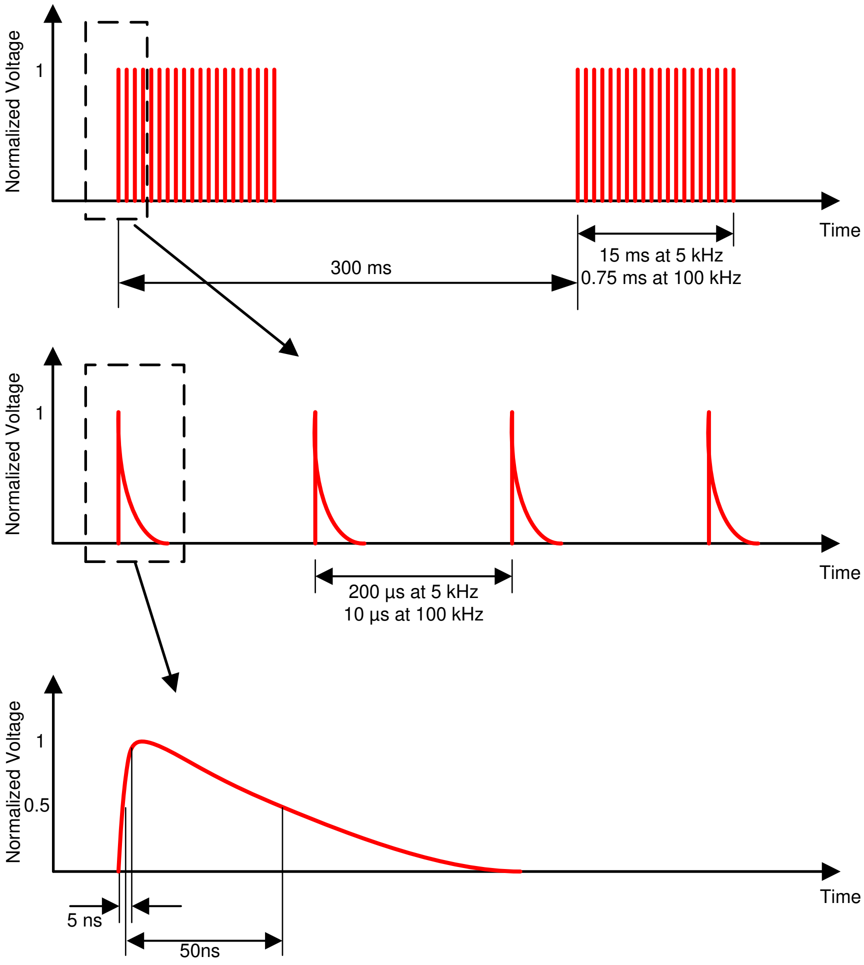

Figure 8-4. EFT Voltage Waveforms

Internal ESD protection circuits of the THVD14x9(V) protect the transceivers against ±4-kV EFT. With careful system design, one could achieve EFT Criterion A (no data loss when transient noise is present).

8.3.3 Surge Protection

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 8-5 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

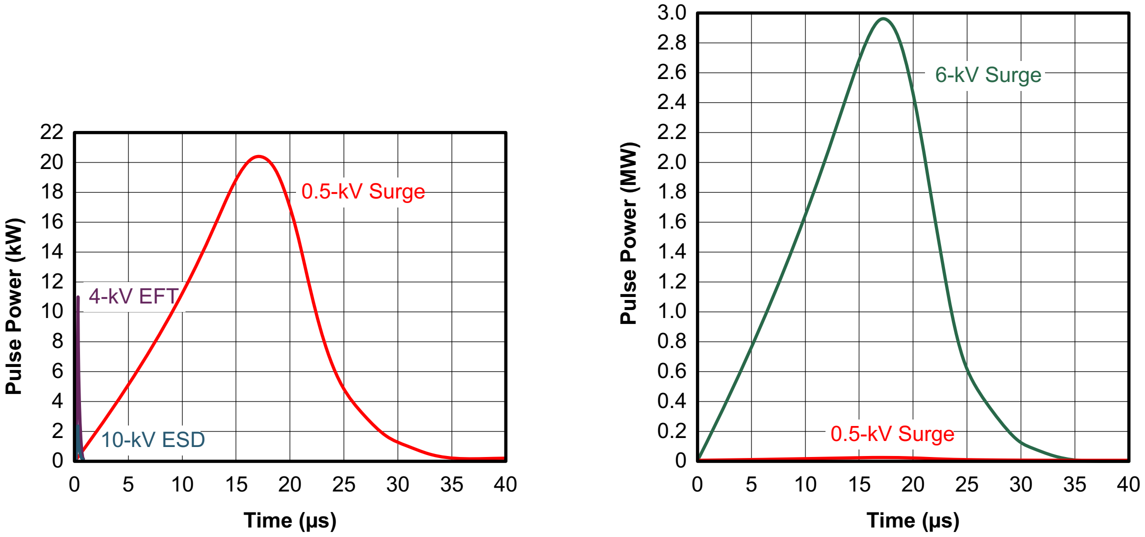

Figure 8-5. Power Comparison of ESD, EFT, and Surge Transients

Figure 8-6 shows the test setup used to validate THVD14x9 surge performance according to the IEC 61000-4-5 1.2/50-µs surge pulse.

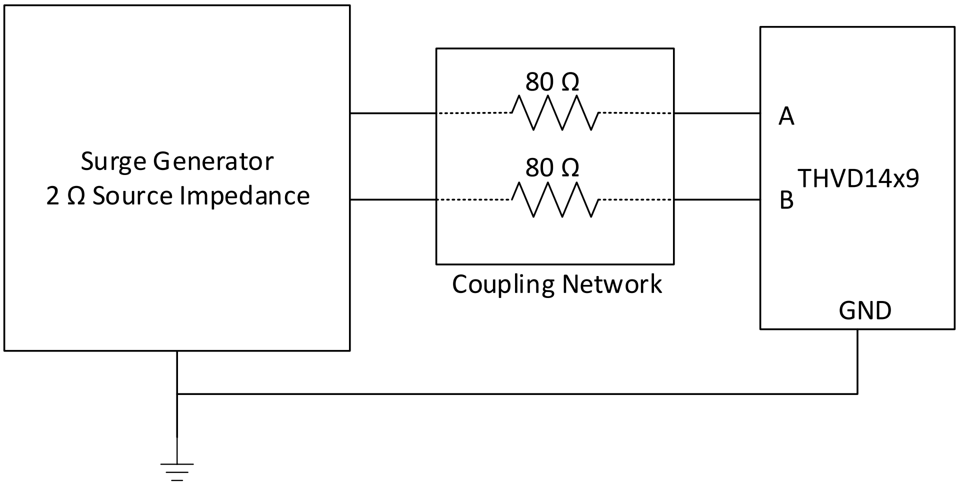

Figure 8-6. THVD14x9(V) Surge Test Setup

THVD14x9(V) product family is robust to ±4-kV surge transients without the need for any external components.

8.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD14x9(V) family feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) hysteresis guarantees excellent noise immunity.

8.3.5 Failsafe Receiver

The differential receivers of the THVD14x9(V) family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver will output a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\_FSH}|$.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

THVD14x9(V) are half-duplex RS-485 transceivers with integrated system-level surge protection. Standard 8-pin SOIC (D) package allows drop-in replacement into existing systems and eliminate system-level protection components.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, with a value that matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

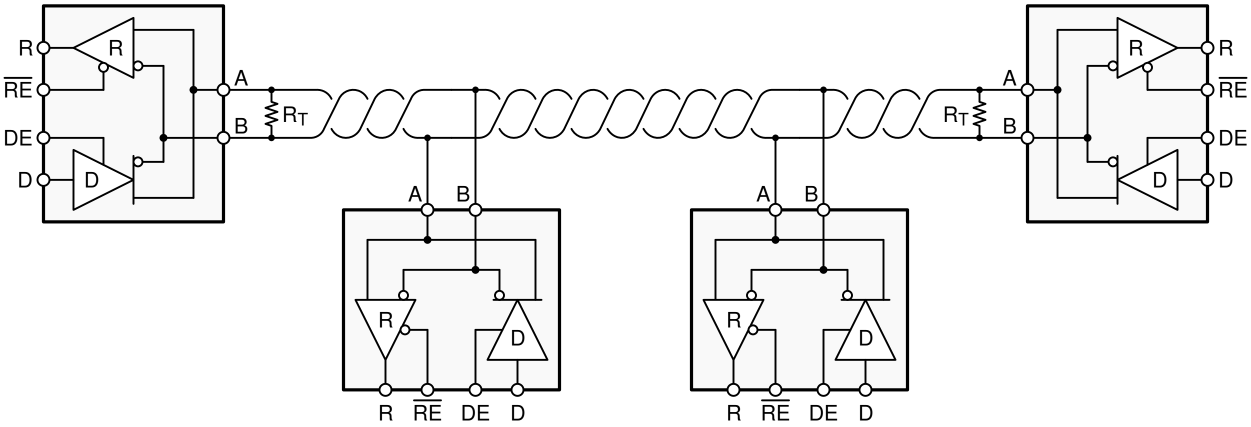

Figure 9-1. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

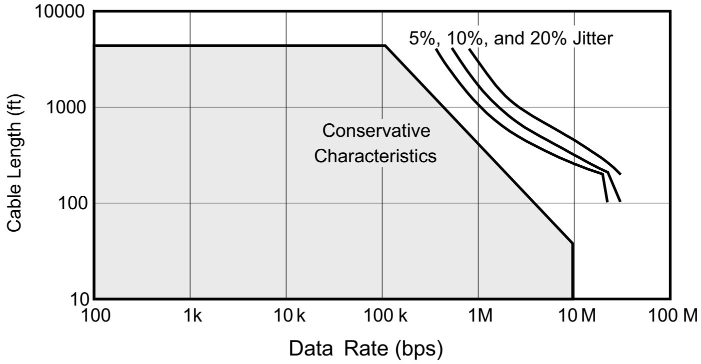

Figure 9-2. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 12 Mbps for the THVD1449(V)) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \tag{1}$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD14x9(V) devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.2 Detailed Design Procedure

RS-485 transceivers operate in noisy industrial environments typically require surge protection at the bus pins. Figure 9-3 compares 4-kV surge protection implementation with a regular RS-485 transceiver (such as THVD14x0) against with the THVD14x9(V). The internal TVS protection of the THVD14x9(V) achieves ±4-kV IEC 61000-4-5 surge protection without any additional external components, reducing system level bill of materials.

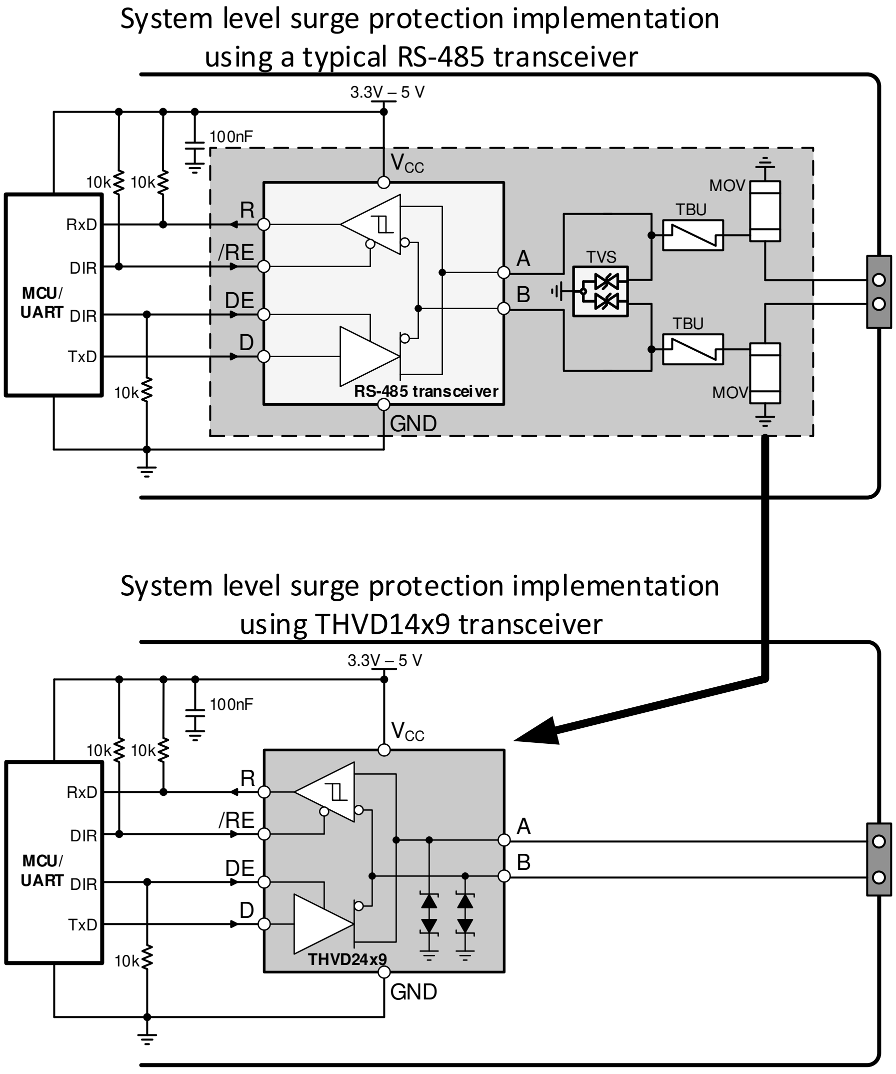

Figure 9-3. Implementation of System-Level Surge Protection Using THVD14x9(V)

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

Additional external protection components generally are not needed when using THVD14x9(V) transceivers.

1. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
2. Use at least two vias for V_{CC} and ground connections of decoupling capacitors to minimize effective via-inductance.
3. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.

11.2 Layout Example

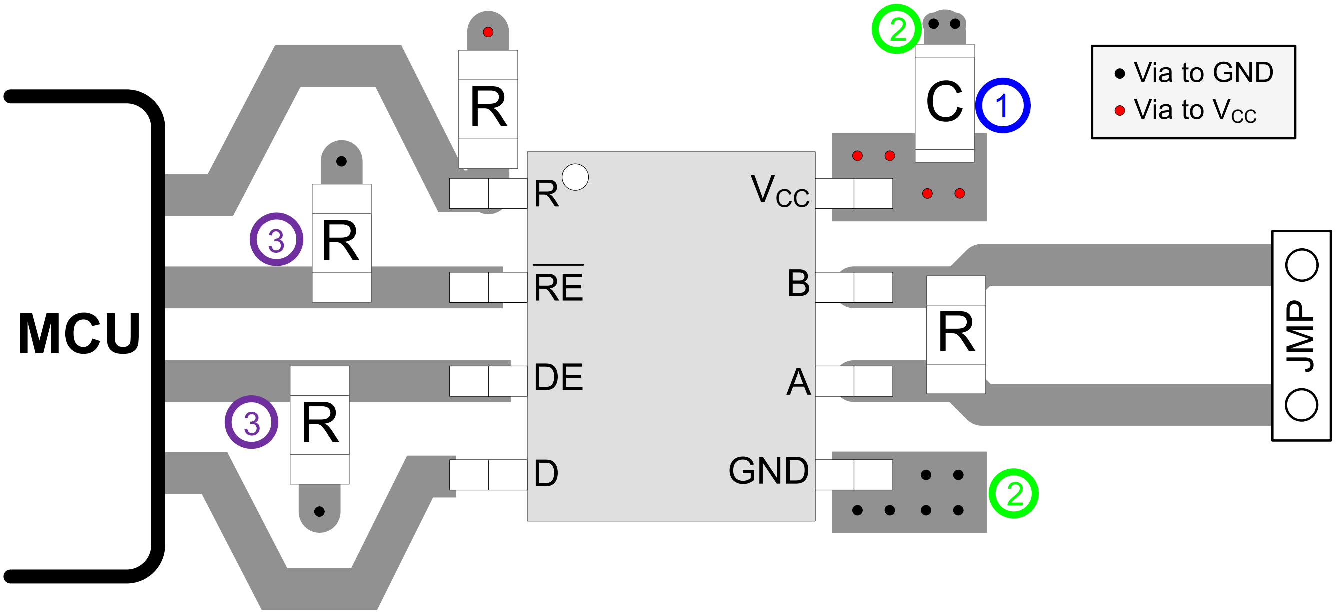

Figure 11-1. THVD1439, THVD1449 Layout Example

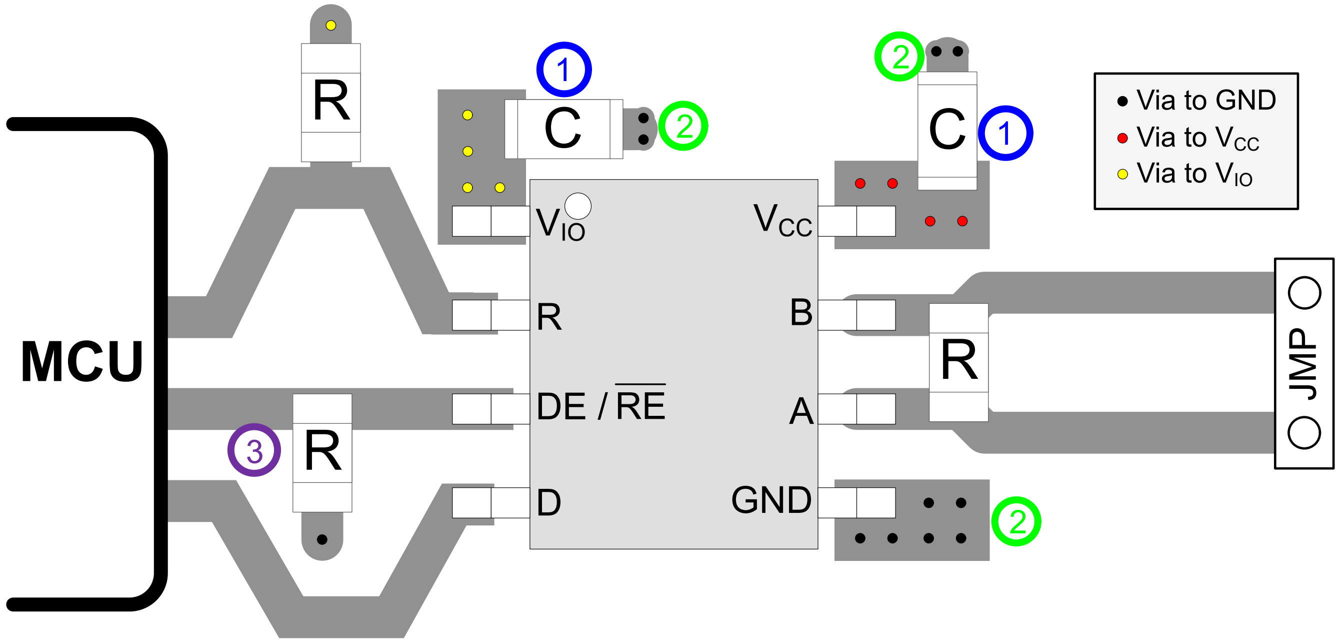

Figure 11-2. THVD1439V THVD1449V Layout Example

12 Device and Documentation Support

12.1 Device Support

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

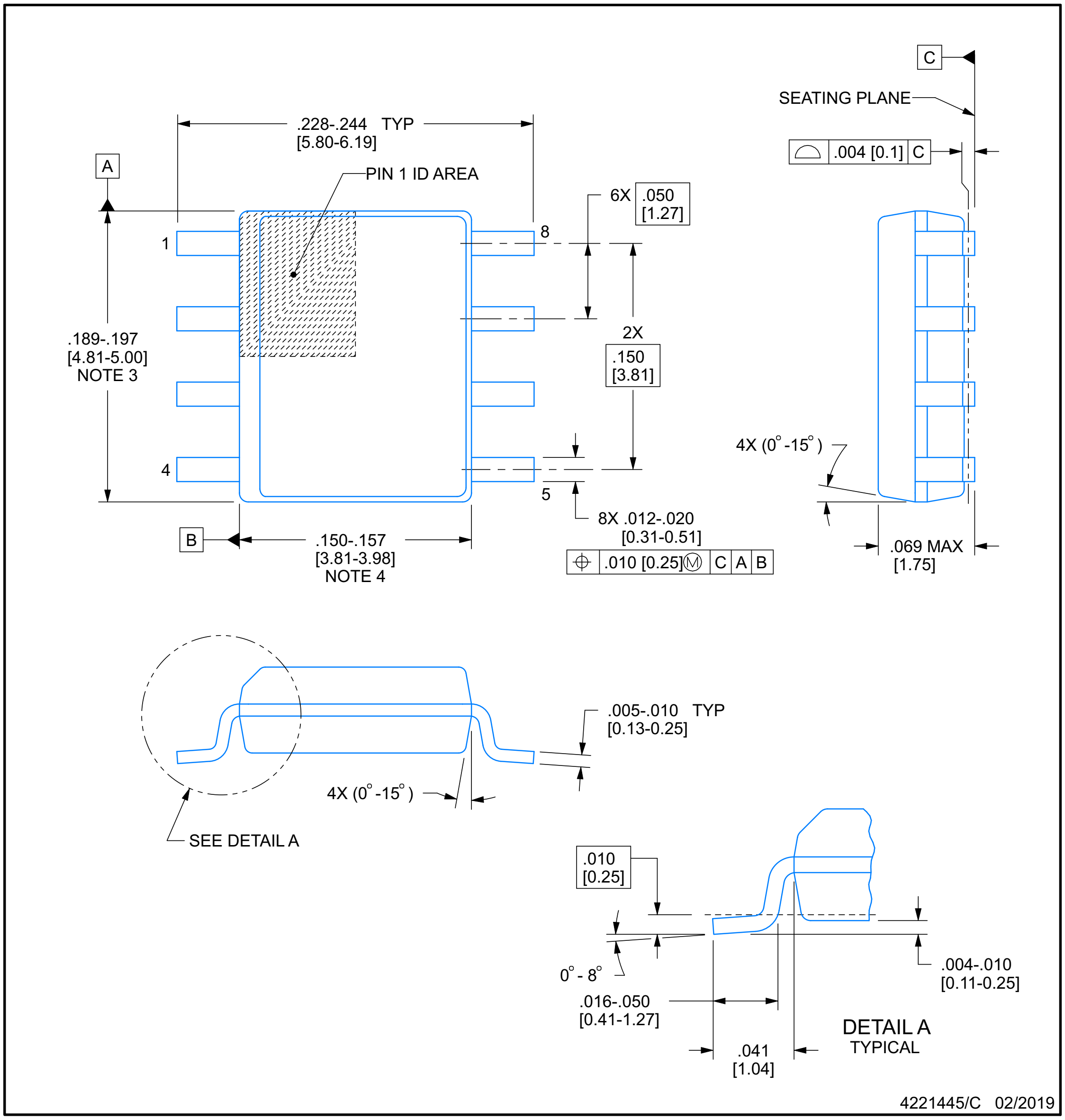
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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ADVANCE INFORMATION

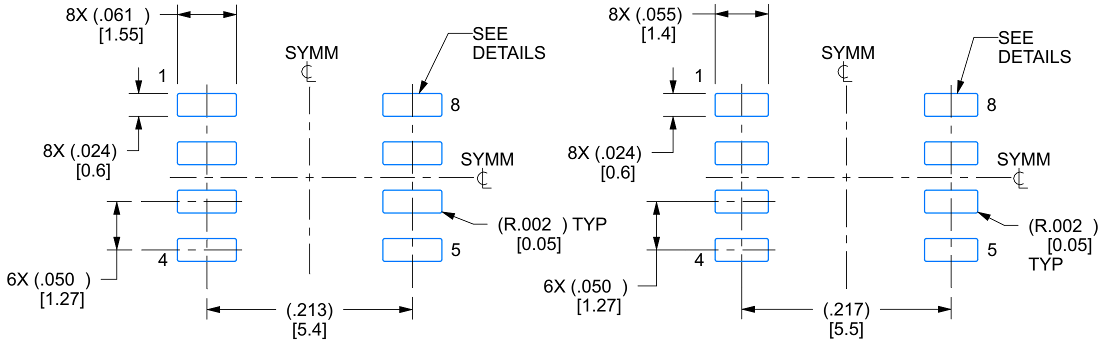
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

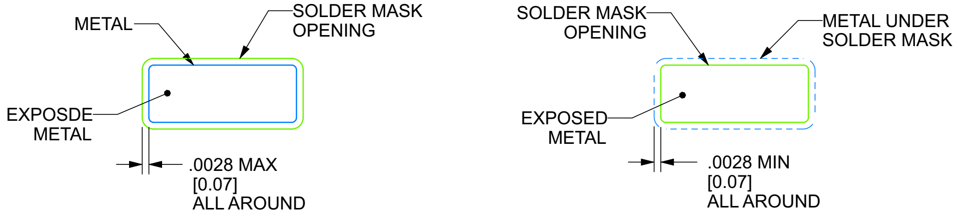
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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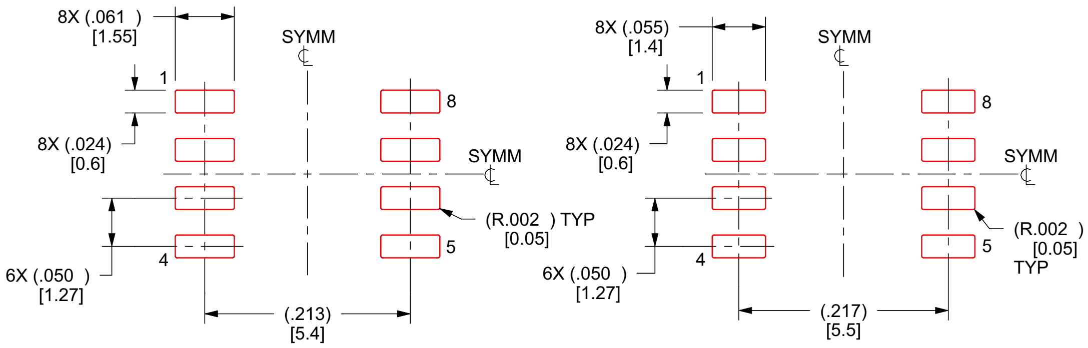
EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

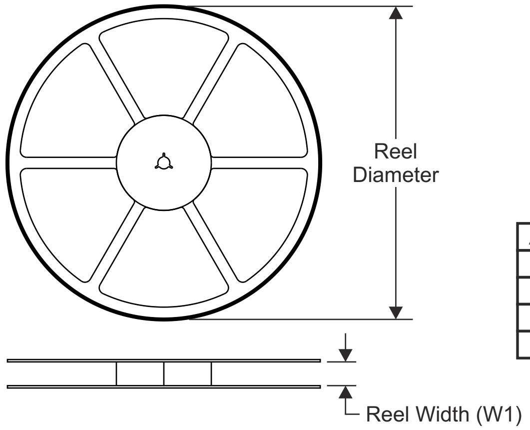
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

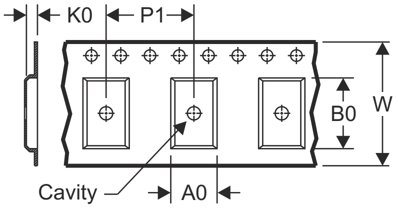
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

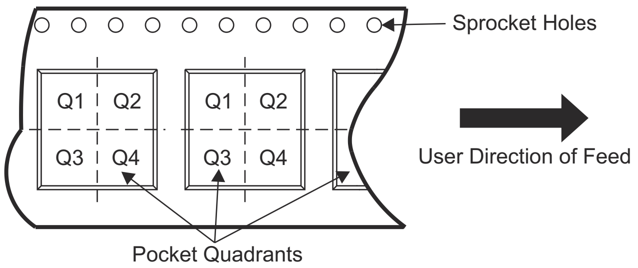


TAPE DIMENSIONS



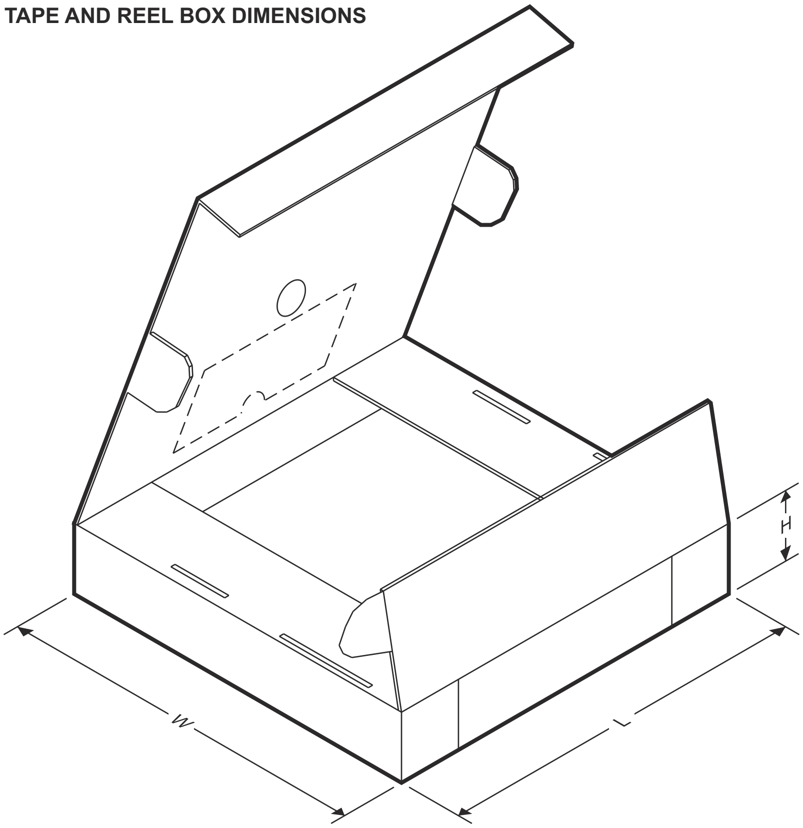
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTHVD1439DR PTHVD1439VDR PTHVD1449DR PTHVD1449VDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTHVD1439DR PTHVD1439VDR PTHVD1449DR PTHVD1449VDR	SOIC	D	8	2500	340.5	338.1	20.6

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTHVD1439VDR	ACTIVE	SOIC	D	8	2500	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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