

SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

- Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A
- Meet ITU Recommendations V.10 and V.11
- Designed to Operate Up to 20 Mbaud
- –7 V to 7 V Common-Mode Input Voltage Range With 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 k Ω Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement
35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

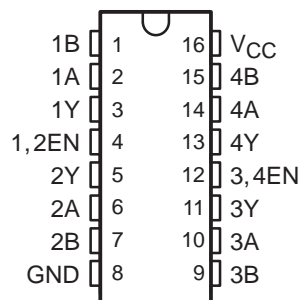
description

The SN55ALS195 and SN75ALS195 are four differential line receivers with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

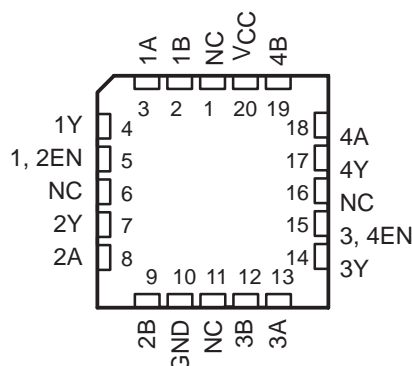
The devices are optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of ± 7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

The SN55ALS195 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75ALS195 is characterized for operation from 0°C to 70°C .

SN55ALS195 . . . J OR W PACKAGE
SN75ALS195 . . . J OR N PACKAGE†
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

† For surface-mount package, see the SN75ALS199.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

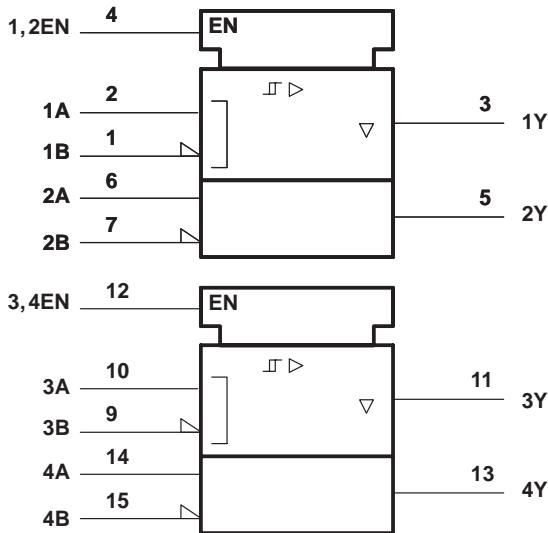
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FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2\text{ V}$	H	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	H	?
$V_{ID} \leq -0.2\text{ V}$	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

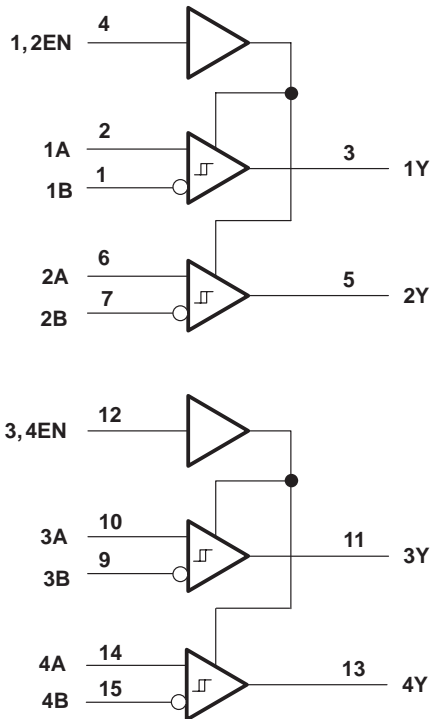
logic symbol†



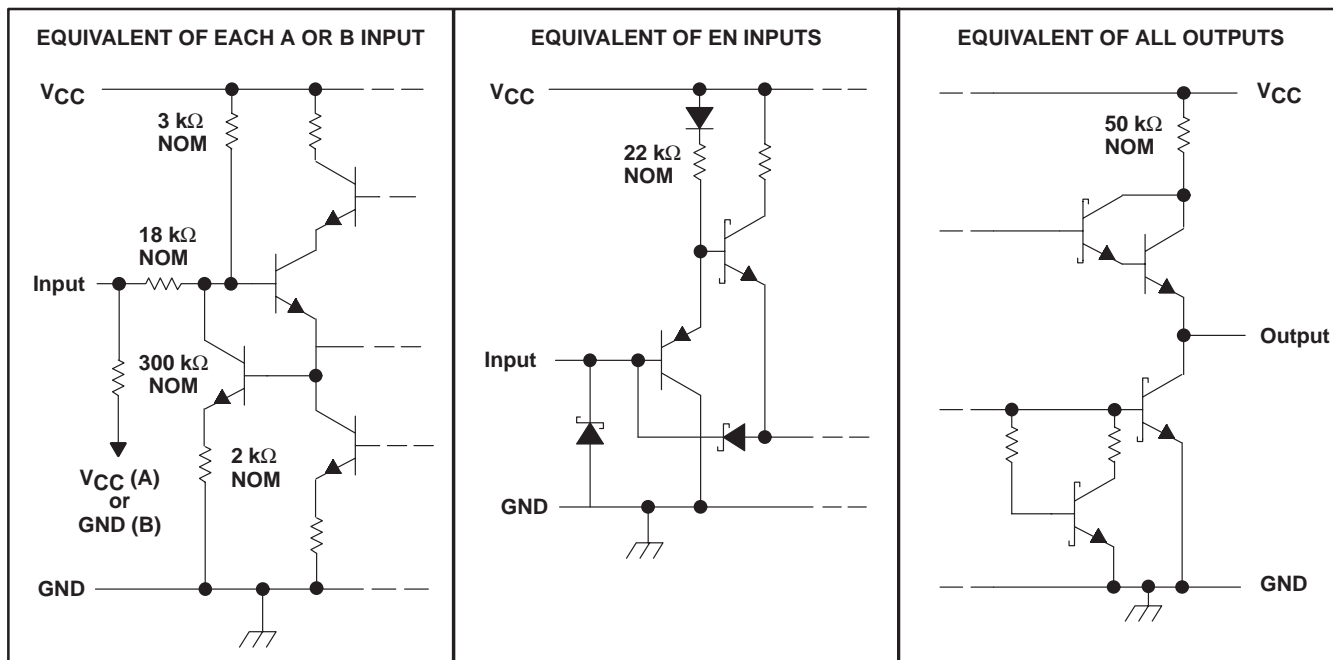
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J, N, and W packages.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, A or B inputs, V_I	± 15 V
Differential input voltage, V_{ID} (see Note 2)	± 15 V
Enable input voltage, V_I	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN55ALS195	-55°C to 125°C
SN75ALS195	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, N, or W package	300°C

[†] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/ $^\circ\text{C}$	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/ $^\circ\text{C}$	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/ $^\circ\text{C}$	656 mW	N/A
N	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW	N/A
W	1000 mW	8.0 mW/ $^\circ\text{C}$	640 mW	200 mW

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recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7			± 7	V
Differential input voltage, V_{ID}			± 12			± 12	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			-200§			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				120		mV
V_{IK}	Enable-input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, See Figure 1	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -400 \mu A$	2.5	3.6		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = -200 \text{ mV}$, See Figure 1	$I_{OL} = 8 \text{ mA}$			0.45	V
			$I_{OL} = 16 \text{ mA}$			0.5	
I_{OZ}	High-impedance-state output current	$V_{CC} = \text{MAX}$, $V_O = 2.7 \text{ V}$	$V_{IL} = 0.8 \text{ V}$, $V_{ID} = -3 \text{ V}$			20	μA
		$V_{CC} = \text{MAX}$, $V_O = 0.5 \text{ V}$	$V_{IL} = 0.8 \text{ V}$, $V_{ID} = 3 \text{ V}$			-20	
I_I	Line input current	Other input at 0 V, See Note 3	$V_{CC} = \text{MIN}$, $V_I = 15 \text{ V}$		0.7	1.2	mA
			$V_{CC} = \text{MAX}$, $V_I = -15 \text{ V}$		-1	-1.7	
I_{IH}	High-level enable-input current	$V_{CC} = \text{MAX}$	$V_{IH} = 2.7 \text{ V}$			20	μA
			$V_{IH} = 5.25 \text{ V}$			100	
I_{IL}	Low-level enable-input current	$V_{CC} = \text{MAX}$	$V_{IL} = 0.4 \text{ V}$			-100	μA
r_i	Input resistance			12	18		k Ω
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$, See Note 4	$V_{ID} = 3 \text{ V}$, $V_O = 0$	-15	-78	-130	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$	Outputs disabled		22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.

4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = 0\text{ to }3\text{ V}$, See Figure 2		15	22	ns
t_{PHL} Propagation delay time, high- to low-level output			15	22	ns
t_{PZH} Output enable time to high level	See Figure 3		13	25	ns
t_{PZL} Output enable time to low level			10	25	
t_{PHZ} Output disable time from high level	See Figure 3		19	25	ns
t_{PLZ} Output disable time from low level			17	22	

PARAMETER MEASUREMENT INFORMATION

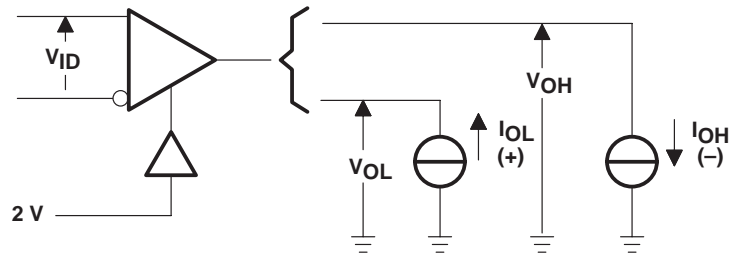
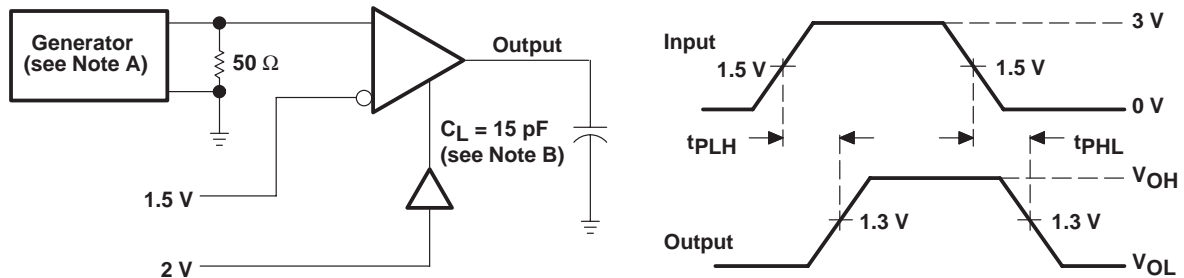


Figure 1. V_{OH} , V_{OL}



TEST CIRCUIT

VOLTAGE WAVEFORMS

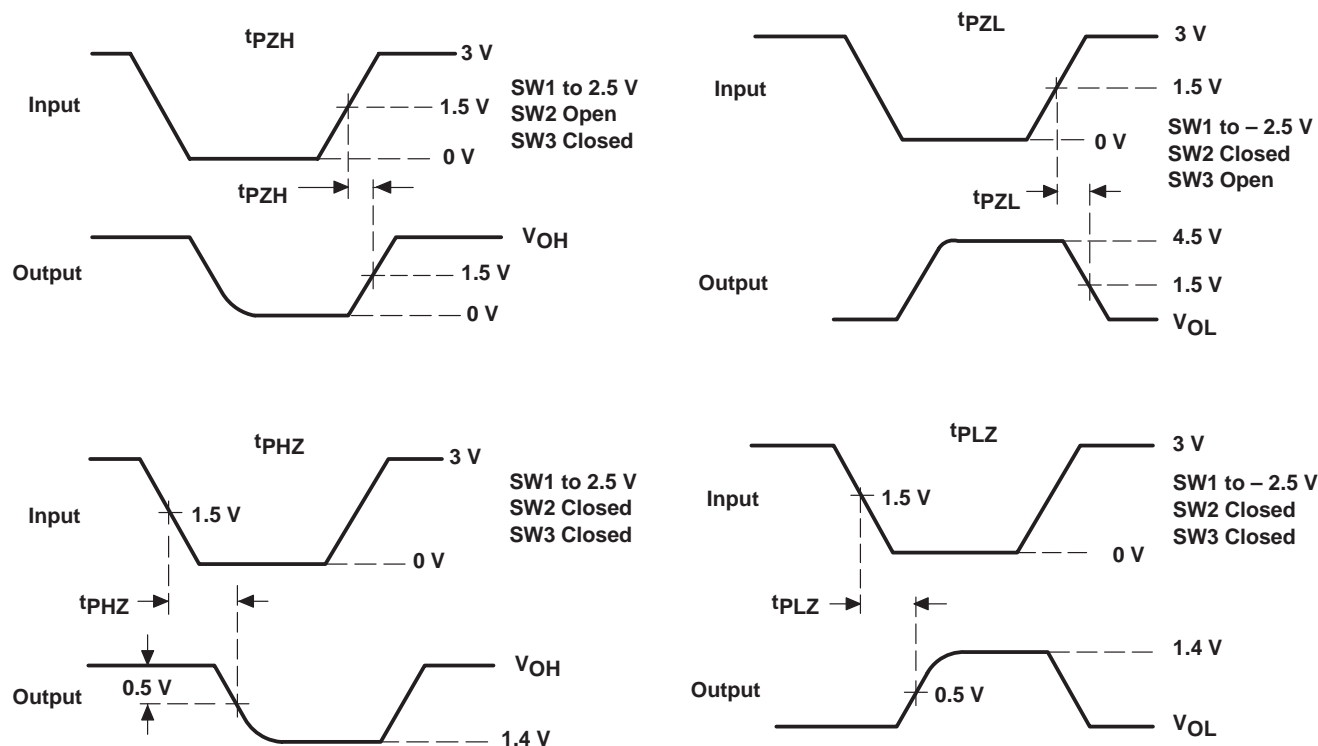
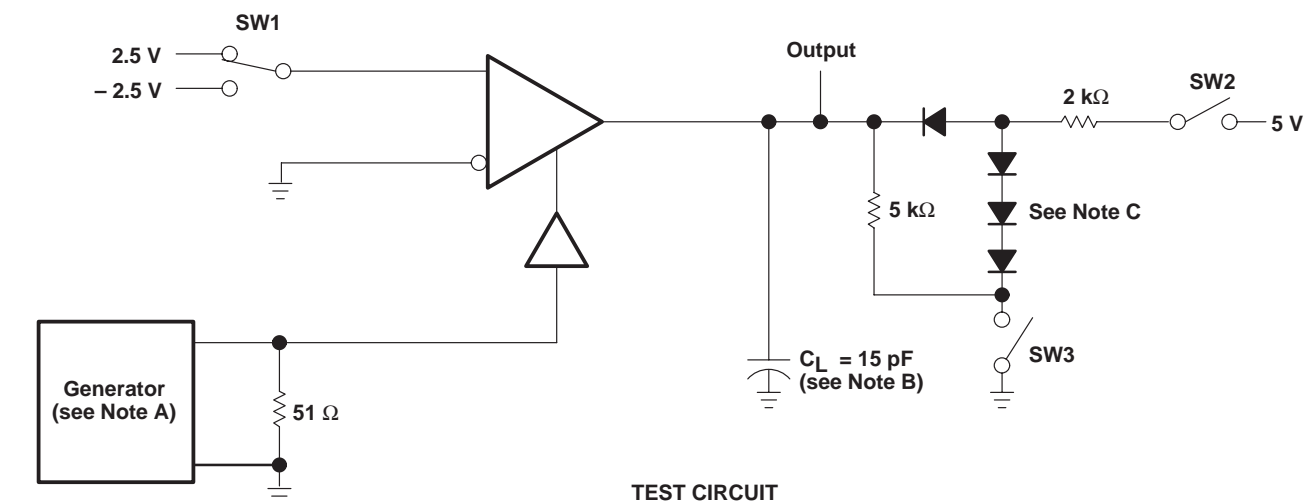
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

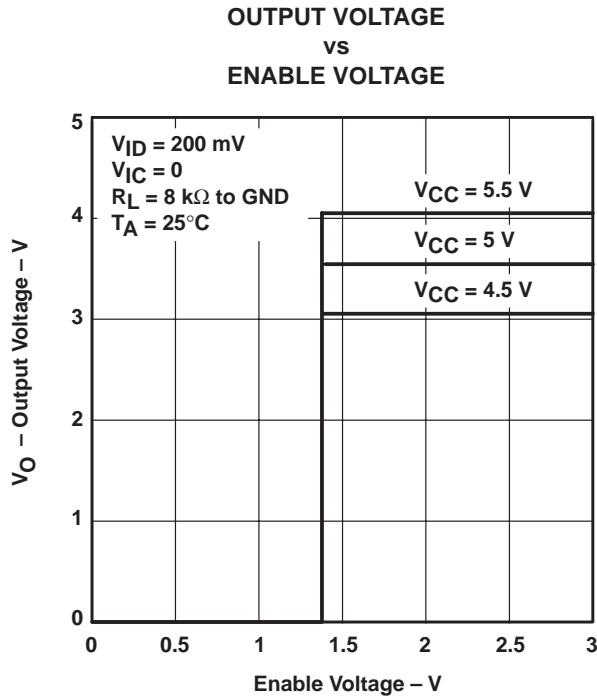


Figure 4

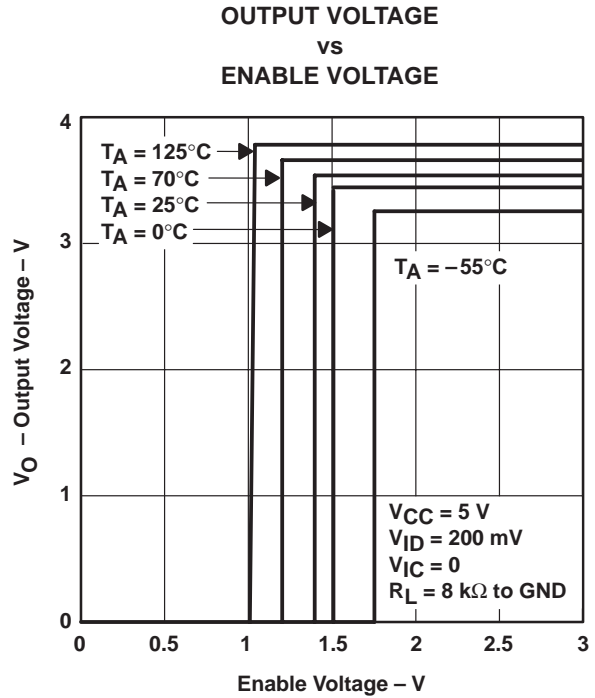


Figure 5

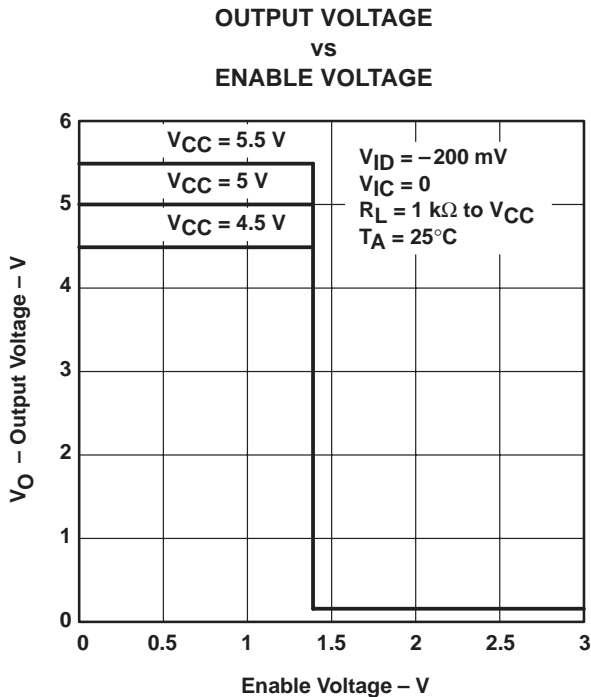


Figure 6

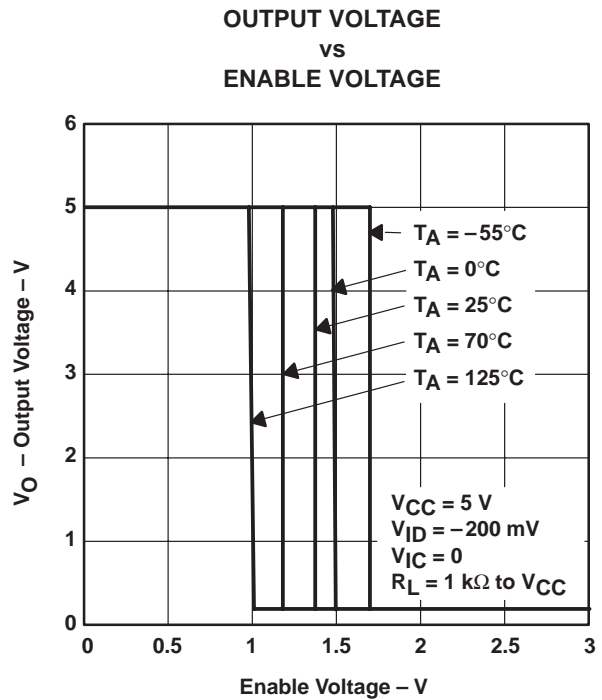


Figure 7

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

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TYPICAL CHARACTERISTICS†

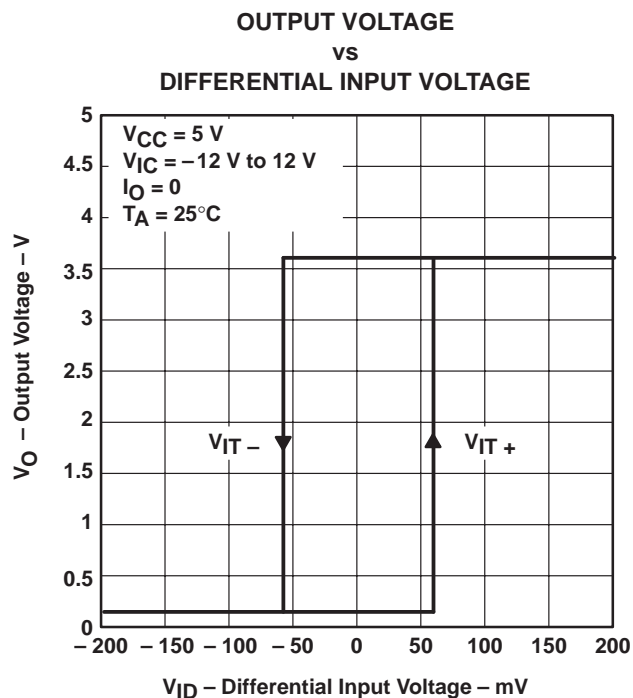


Figure 8

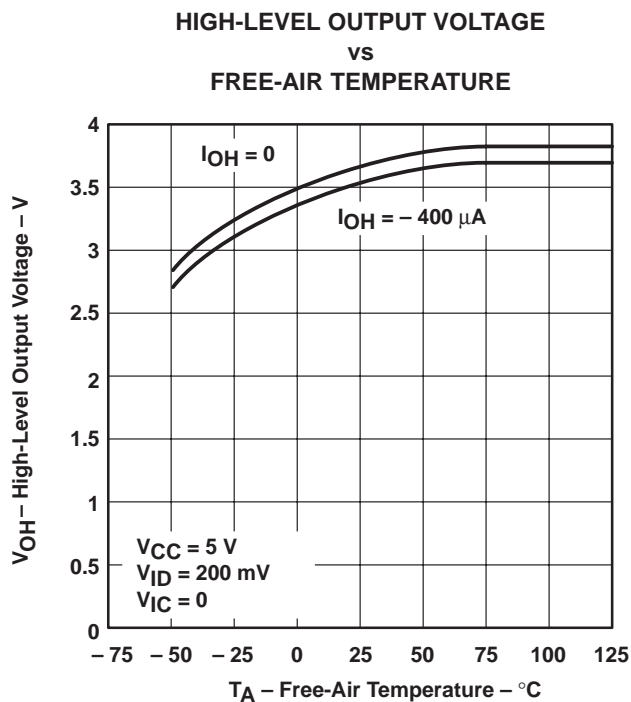


Figure 9

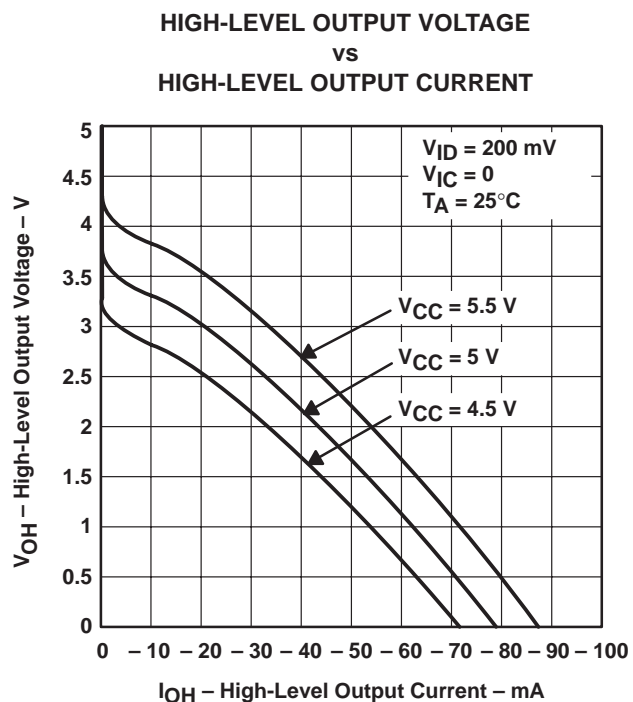


Figure 10

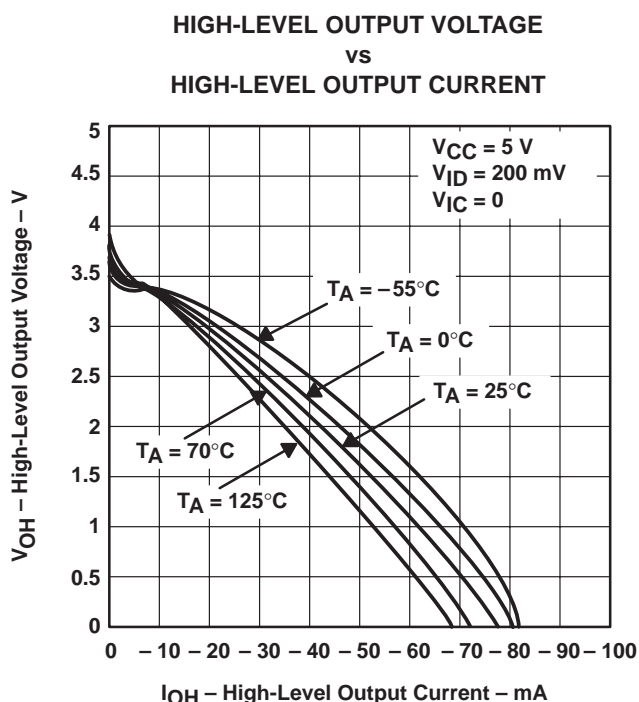


Figure 11

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

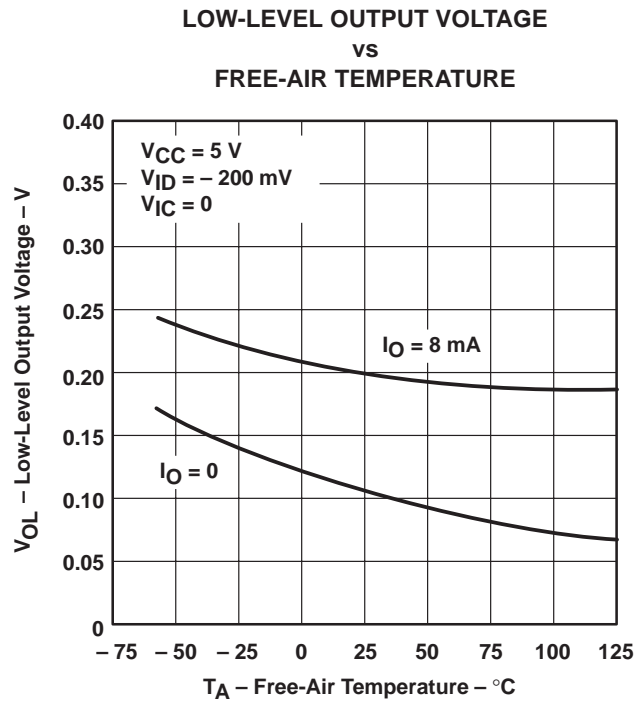


Figure 12

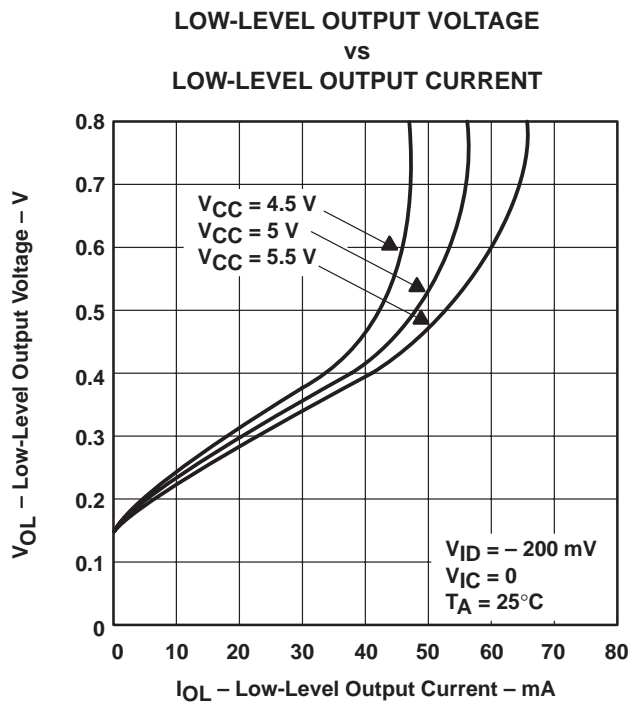


Figure 13

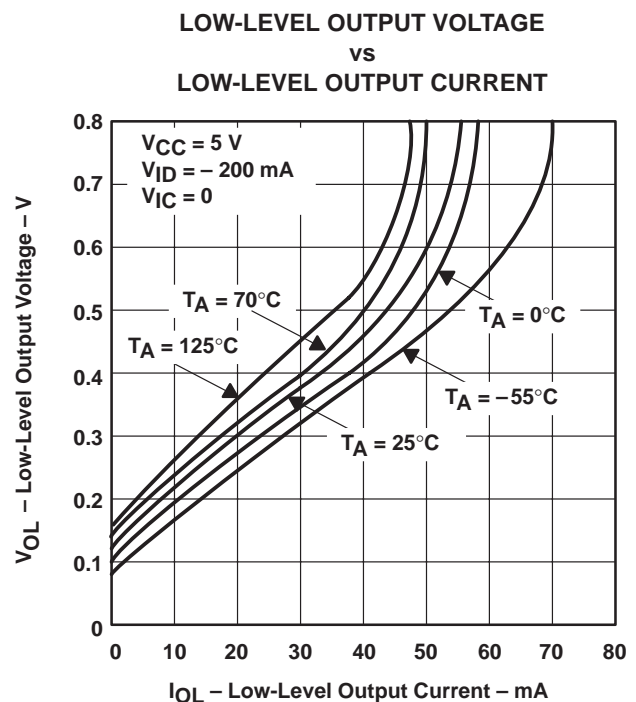


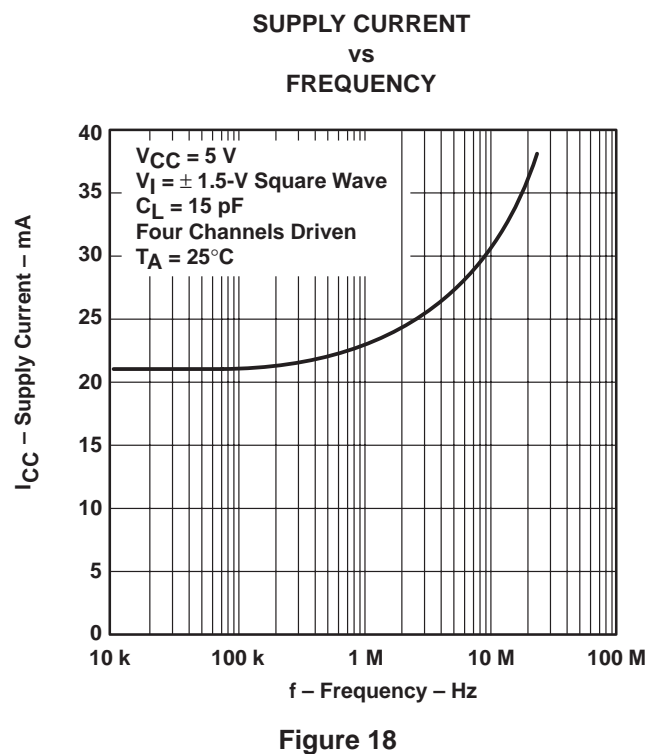
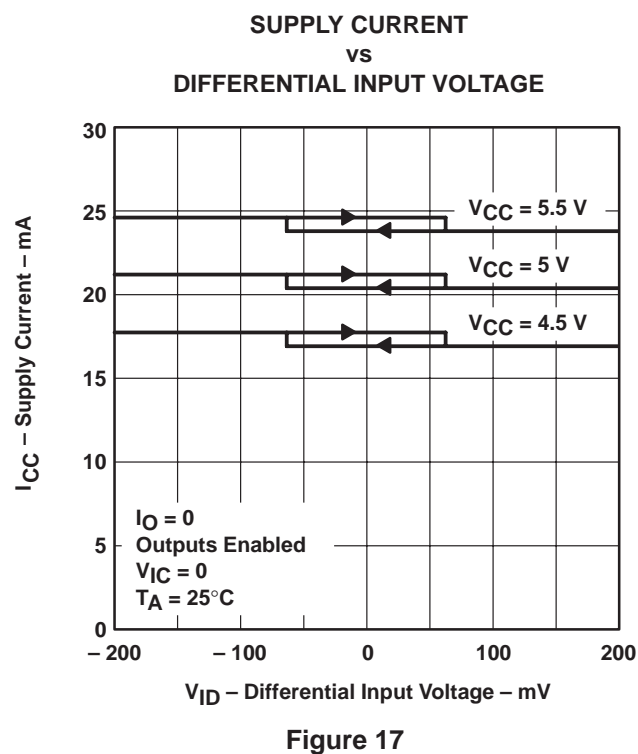
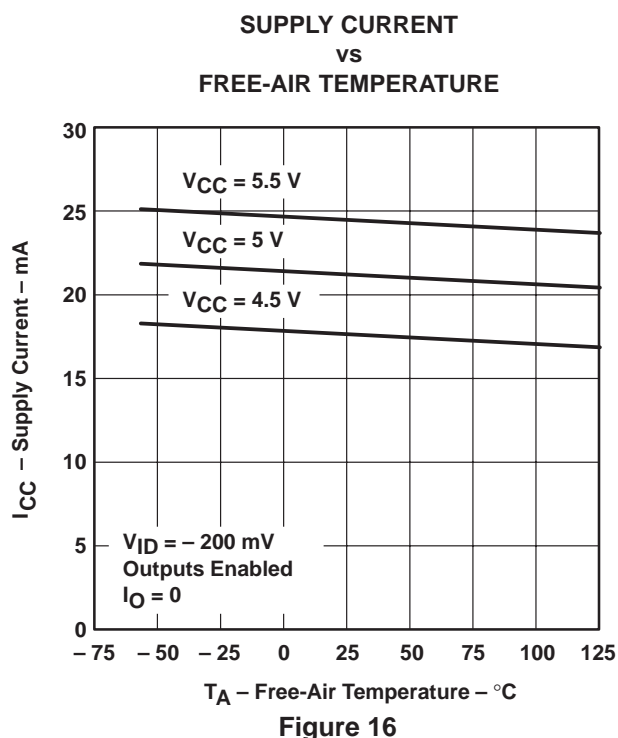
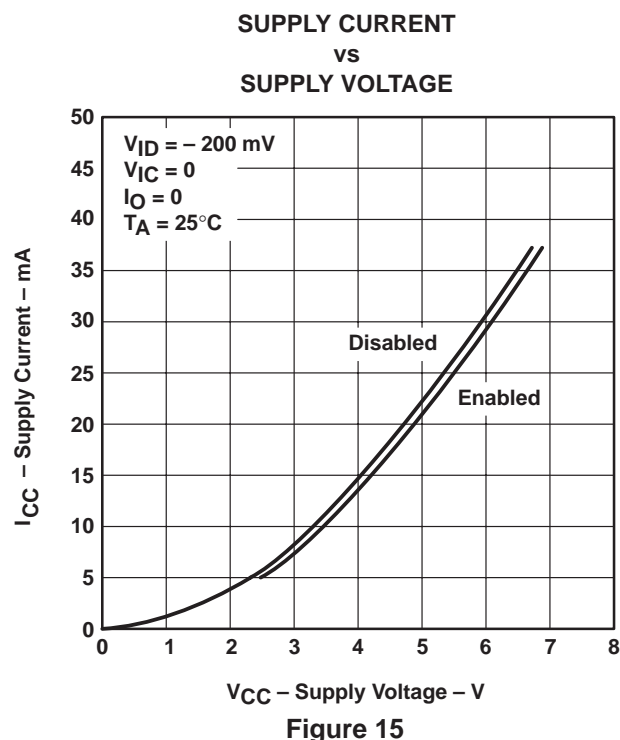
Figure 14

† Data for temperatures below 0°C and above 70°C , and below 4.75 V and above 5.25 V , are applicable to SN55ALS195 circuits only.

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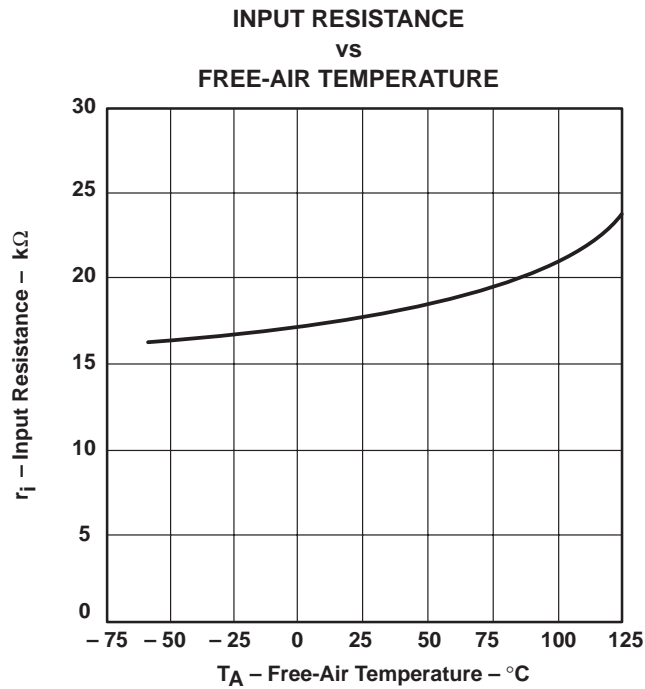


Figure 19

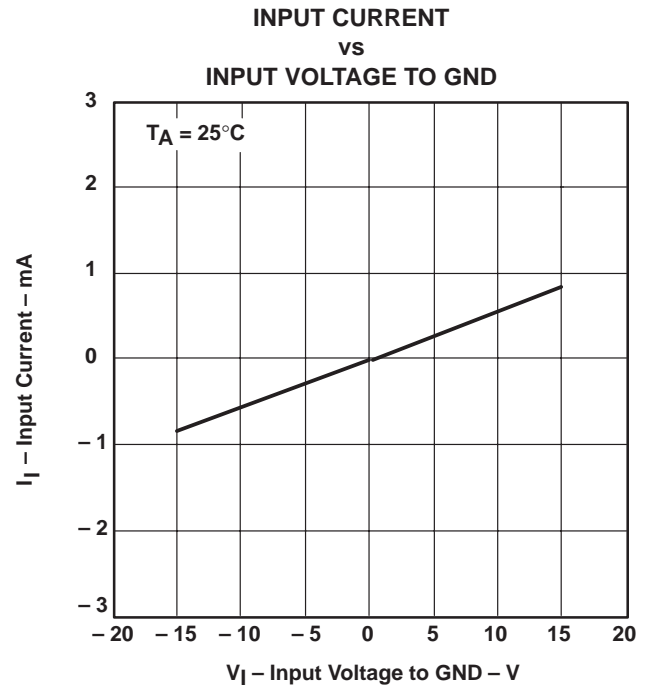


Figure 20

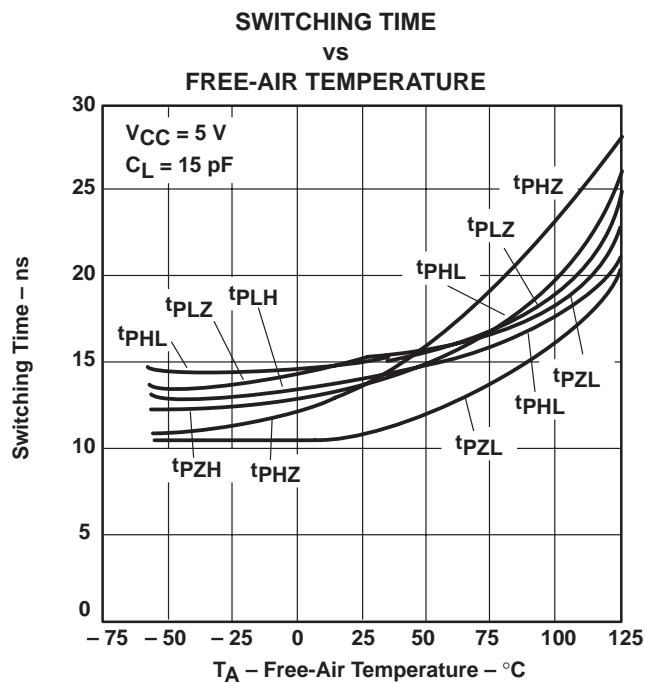


Figure 21

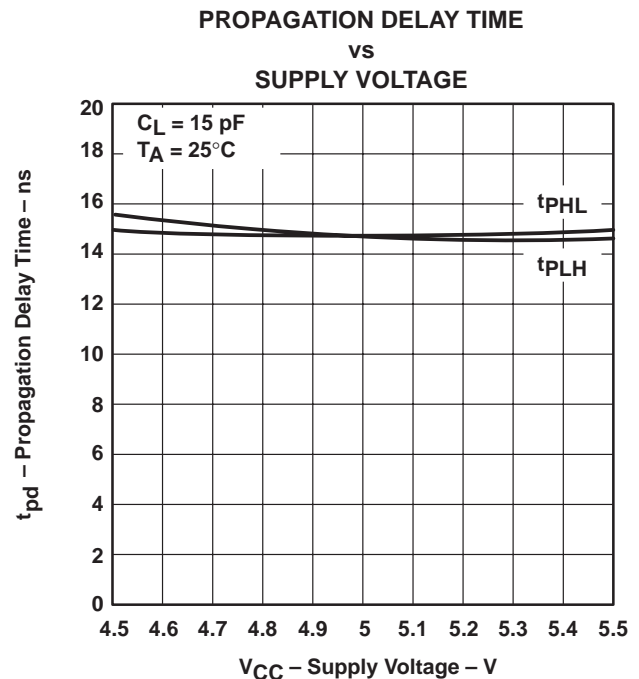


Figure 22

† Data for temperatures below $0^{\circ}C$ and above $70^{\circ}C$, and below $4.75 V$ and above $5.25 V$, are applicable to SN55ALS195 circuits only.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS195N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS195N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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