

# SN75174 QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS039B – OCTOBER 1980 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11.
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range of  $-7\text{ V}$  to  $12\text{ V}$
- Active-High Enable
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Operates From Single 5-V Supply
- Low Power Requirements
- Functionally Interchangeable With MC3487

## description

The SN75174 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately  $150^{\circ}\text{C}$ . This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

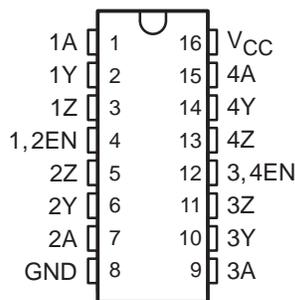
The SN75174 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE**  
(each driver)

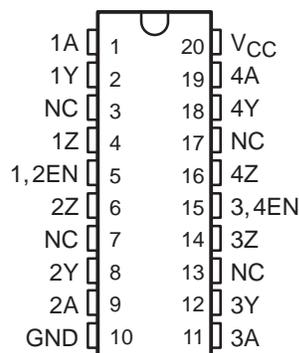
| INPUT | ENABLE | OUTPUTS |   |
|-------|--------|---------|---|
|       |        | Y       | Z |
| H     | H      | H       | L |
| L     | H      | L       | H |
| X     | L      | Z       | Z |

H = TTL high level, X = irrelevant,  
L = TTL low level, Z = high impedance (off)

**N PACKAGE**  
(TOP VIEW)



**DW PACKAGE**  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

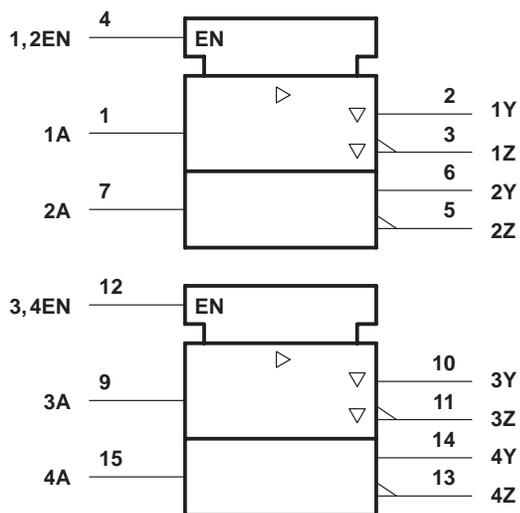
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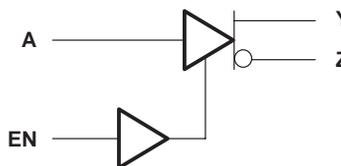
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## logic symbol†

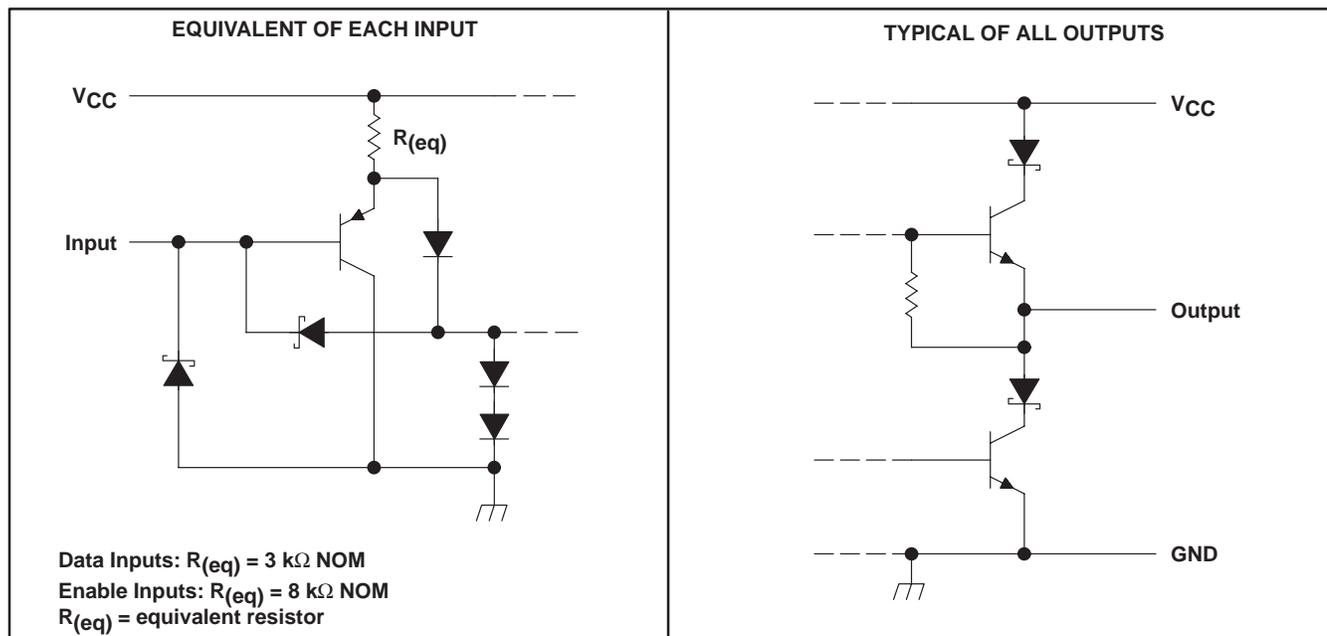


## logic diagram, each driver (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematics of inputs and outputs



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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

|  |                              |
|--|------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)                        | 7 V                          |
| Output voltage range, $V_O$                                  | –10 V to 15 V                |
| Input voltage, $V_I$   | 5.5 V                        |
| Continuous total dissipation                                 | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$                  | 0°C to 70°C                  |
| Storage temperature range, $T_{stg}$                         | –65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING |
|---------|---|---|--|
| DW      | 1125 mW                                     | 9.0 mW/°C   | 720 mW                                   |
| N       | 1150 mW                                     | 9.2 mW/°C   | 736 mW                                   |

## recommended operating conditions

|                                       | MIN  | NOM      | MAX  | UNIT |
|---------------------------------------|------|----------|------|------|
| Supply voltage, $V_{CC}$              | 4.75 | 5        | 5.25 | V    |
| High-level input voltage, $V_{IH}$    | 2    |          |      | V    |
| Low-level input voltage, $V_{IL}$     |      |          | 0.8  | V    |
| Common-mode output voltage, $V_{OC}$  |      | –7 to 12 |      | V    |
| High-level output current, $I_{OH}$   |      |          | –60  | mA   |
| Low-level output current, $I_{OL}$    |      |          | 60   | mA   |
| Operating free-air temperature, $T_A$ | 0    |          | 70   | °C   |



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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| PARAMETER         |   | TEST CONDITIONS                                    |                          | MIN                           | TYP† | MAX      | UNIT |
|-------------------|---|--|--------------------------|-------------------------------|------|----------|------|
| V <sub>IK</sub>   | Input clamp voltage                                 | I <sub>I</sub> = -18 mA                            |                          |                               |      | -1.5     | V    |
| V <sub>OH</sub>   | High-level output voltage                           | V <sub>IH</sub> = 2 V,<br>I <sub>OH</sub> = -33 mA | V <sub>IL</sub> = 0.8 V, |                               | 3.7  |          | V    |
| V <sub>OL</sub>   | Low-level output voltage                            | V <sub>IH</sub> = 2 V,<br>I <sub>OL</sub> = 33 mA  | V <sub>IL</sub> = 0.8 V, |                               | 1.1  |          | V    |
| V <sub>O</sub>    | Output voltage                                      | I <sub>O</sub> = 0                                 |                          | 0                             |      | 6        | V    |
| V <sub>OD1</sub>  | Differential output voltage                         | I <sub>O</sub> = 0                                 |                          | 1.5                           | 6    | 6        | V    |
| V <sub>OD2</sub>  | Differential output voltage                         | R <sub>L</sub> = 100 Ω,                            | See Figure 1             | 1/2 V <sub>OD1</sub><br>or 2‡ |      |          | V    |
|                   |   | R <sub>L</sub> = 54 Ω,                             | See Figure 1             | 1.5                           | 2.5  | 5        | V    |
| V <sub>OD3</sub>  | Differential output voltage                         | See Note 2   |                          | 1.5                           |      | 5        | V    |
| Δ V <sub>OD</sub> | Change in magnitude of differential output voltage§ |  |                          |                               |      | ±0.2     | V    |
| V <sub>OC</sub>   | Common-mode output voltage¶                         | R <sub>L</sub> = 54 Ω or 100 Ω, See Figure 1       |                          |                               |      | +3<br>-1 | V    |
| Δ V <sub>OC</sub> | Change in magnitude of common-mode output voltage§  |  |                          |                               |      | ±0.2     | V    |
| I <sub>O</sub>    | Output current with power off                       | V <sub>CC</sub> = 0, V <sub>O</sub> = -7 V to 12 V |                          |                               |      | ±100     | μA   |
| I <sub>OZ</sub>   | High-impedance-state output current                 | V <sub>O</sub> = -7 V to 12 V                      |                          |                               |      | ±100     | μA   |
| I <sub>IH</sub>   | High-level input current                            | V <sub>I</sub> = 2.7 V                             |                          |                               |      | 20       | μA   |
| I <sub>IL</sub>   | Low-level input current                             | V <sub>I</sub> = 0.5 V                             |                          |                               |      | -360     | μA   |
| I <sub>OS</sub>   | Short-circuit output current                        | V <sub>O</sub> = -7 V                              |                          |                               |      | -180     | mA   |
|                   |   | V <sub>O</sub> = V <sub>CC</sub>                   |                          |                               |      | 180      |      |
|                   |   | V <sub>O</sub> = 12 V                              |                          |                               |      | 500      |      |
| I <sub>CC</sub>   | Supply current (all drivers)                        | No load  | Outputs enabled          |                               | 38   | 60       | mA   |
|                   |   |  | Outputs disabled         |                               | 18   | 40       |      |

† All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

‡ The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.

§ Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

¶ In ANSI Standard EIA/TIA-422-B, V<sub>OC</sub>, which is the average of the two output voltages with respect to ground, is called output offset voltage, V<sub>OS</sub>.

NOTE 2: See EIA Standard RS-485.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER          |                                     | TEST CONDITIONS         |              | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------|-------------------------|--------------|-----|-----|-----|------|
| t <sub>d(OD)</sub> | Differential-output delay time      | R <sub>L</sub> = 54 Ω,  | See Figure 2 |     | 45  | 65  | ns   |
| t <sub>t(OD)</sub> | Differential-output transition time |                         |              |     | 80  | 120 |      |
| t <sub>pZH</sub>   | Output enable time to high level    | R <sub>L</sub> = 110 Ω, | See Figure 3 |     | 80  | 120 | ns   |
| t <sub>pZL</sub>   | Output enable time to low level     | R <sub>L</sub> = 110 Ω, | See Figure 4 |     | 55  | 80  | ns   |
| t <sub>pHZ</sub>   | Output disable time from high level | R <sub>L</sub> = 110 Ω, | See Figure 3 |     | 75  | 115 | ns   |
| t <sub>pLZ</sub>   | Output disable time from low level  | R <sub>L</sub> = 110 Ω, | See Figure 3 |     | 18  | 30  | ns   |



### SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | EIA/TIA-422-B             | RS-485                                 |
|----------------------|---------------------------|--|
| $V_O$                | $V_{oa}, V_{ob}$          | $V_{oa}, V_{ob}$                       |
| $ V_{OD1} $          | $V_o$                     | $V_o$                                  |
| $ V_{OD2} $          | $V_t (R_L = 100 \Omega)$  | $V_t (R_L = 54 \Omega)$                |
| $ V_{OD3} $          |                           | $V_t$ (Test Termination Measurement 2) |
| $\Delta V_{OD} $     | $  V_t  -  \bar{V}_t  $   | $  V_t  -  \bar{V}_t  $                |
| $V_{OC}$             | $ V_{os} $                | $ V_{os} $                             |
| $\Delta V_{OC} $     | $ V_{os} - \bar{V}_{os} $ | $ V_{os} - \bar{V}_{os} $              |
| $I_{OS}$             | $ I_{sa} ,  I_{sb} $      |  |
| $I_O$                | $ I_{xa} ,  I_{xb} $      | $I_{ia}, I_{ib}$                       |

### PARAMETER MEASUREMENT INFORMATION

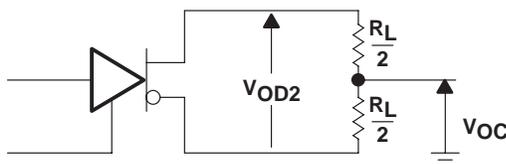
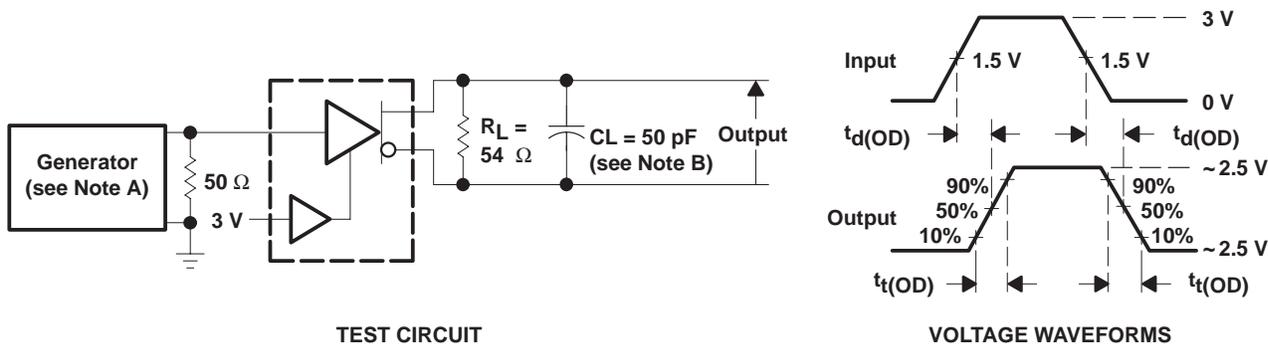


Figure 1. Differential and Common-Mode Output Voltages



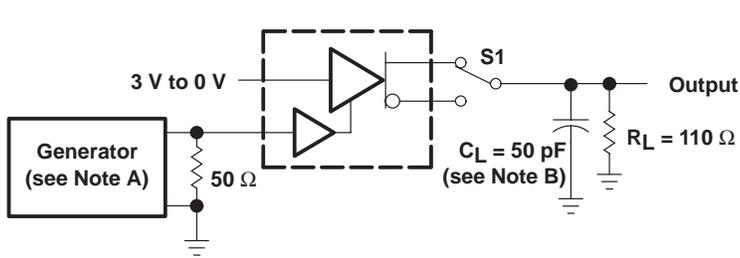
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $PRR \leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Voltage Waveforms

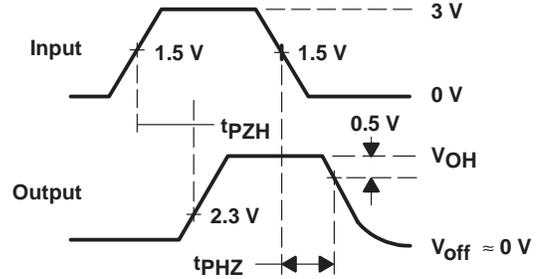
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## PARAMETER MEASUREMENT INFORMATION



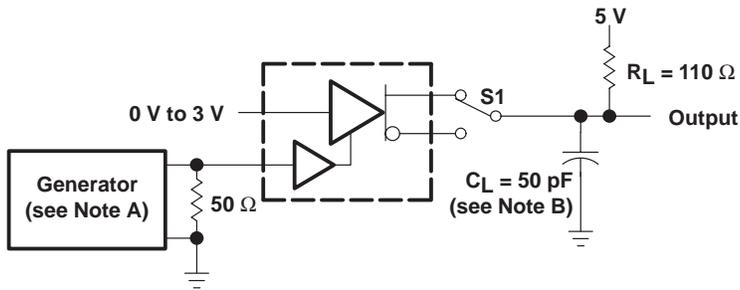
TEST CIRCUIT



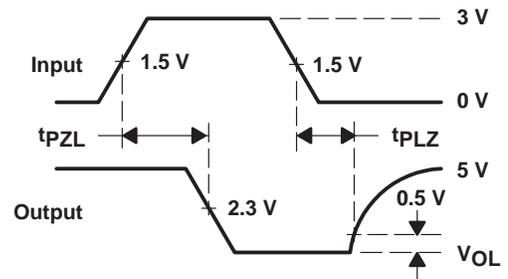
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r \leq$  5 ns,  $t_f \leq$  5 ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r \leq$  5 ns,  $t_f \leq$  5 ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

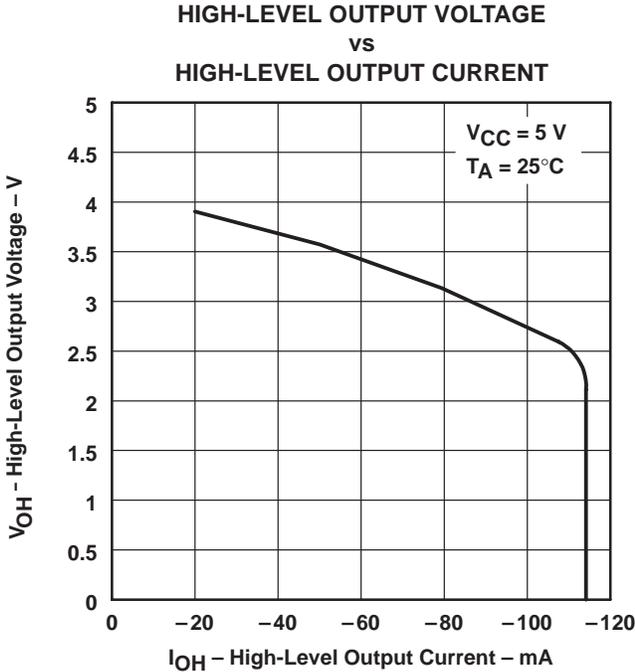


Figure 5

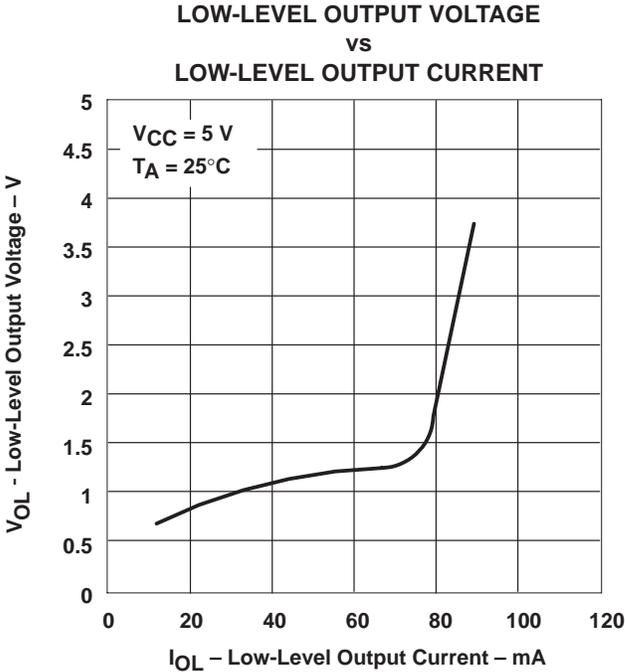


Figure 6

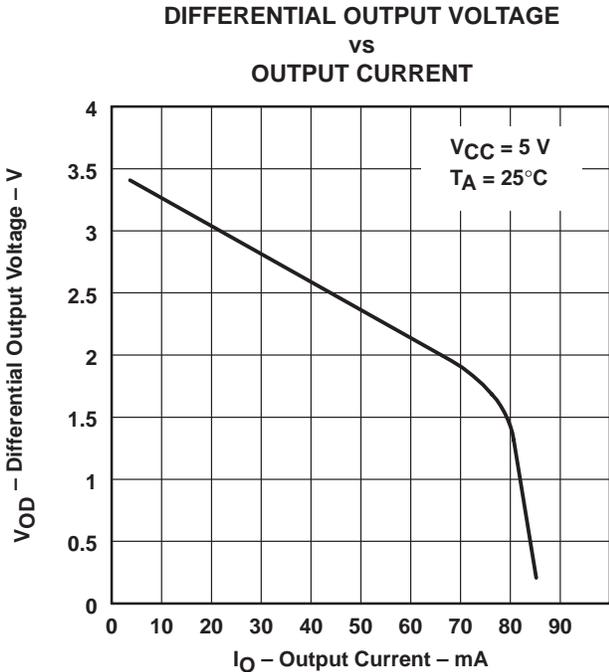


Figure 7

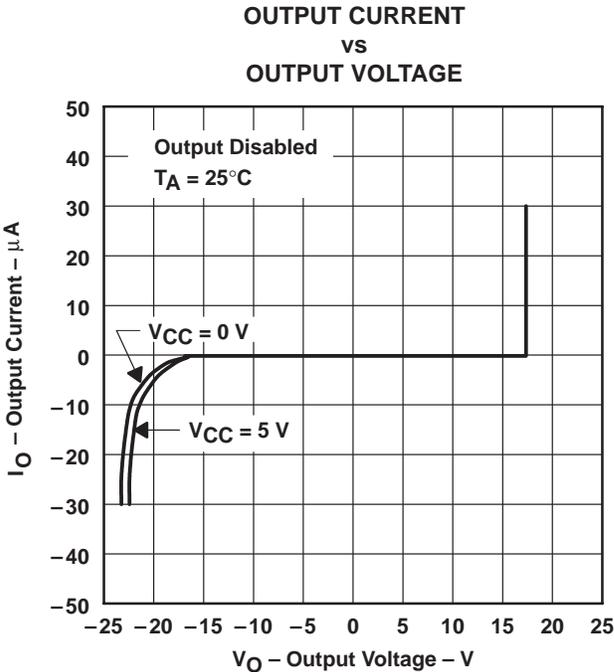


Figure 8

# SN75174 QUADRUPLE DIFFERENTIAL LINE DRIVER

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## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

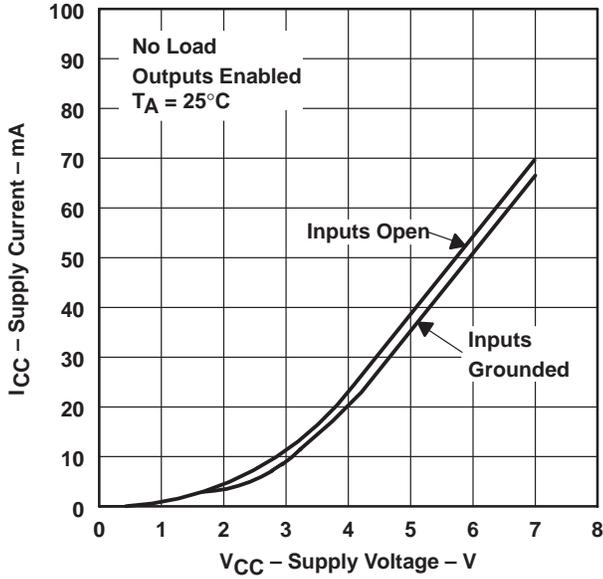


Figure 9

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

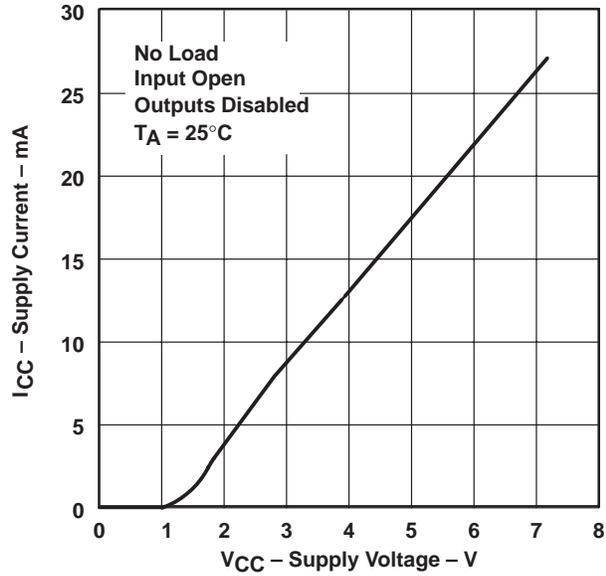
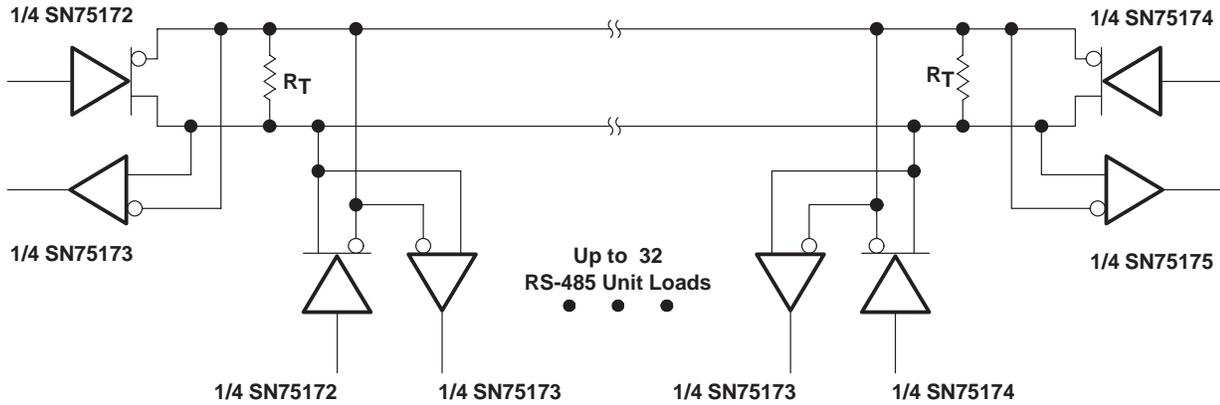


Figure 10

## APPLICATION INFORMATION



NOTE: The line length should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 11. Typical Application Circuit

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75174DW        | ACTIVE        | SOIC         | DW              | 20   | 25          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75174                 | <a href="#">Samples</a> |
| SN75174DWR       | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75174                 | <a href="#">Samples</a> |
| SN75174DWRE4     | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75174                 | <a href="#">Samples</a> |
| SN75174DWRG4     | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75174                 | <a href="#">Samples</a> |
| SN75174N         | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN75174N                | <a href="#">Samples</a> |
| SN75174NE4       | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN75174N                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



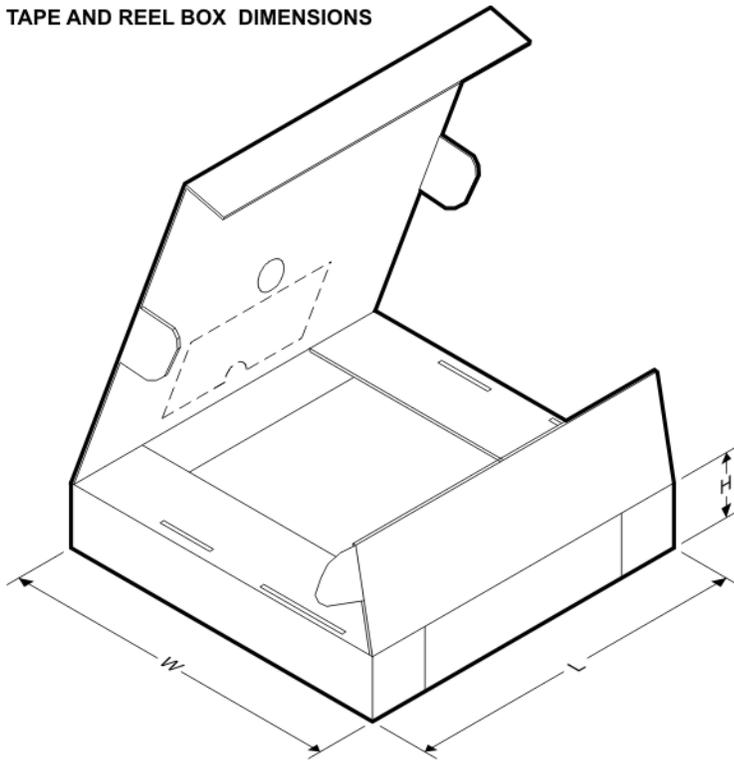
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75174DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75174DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

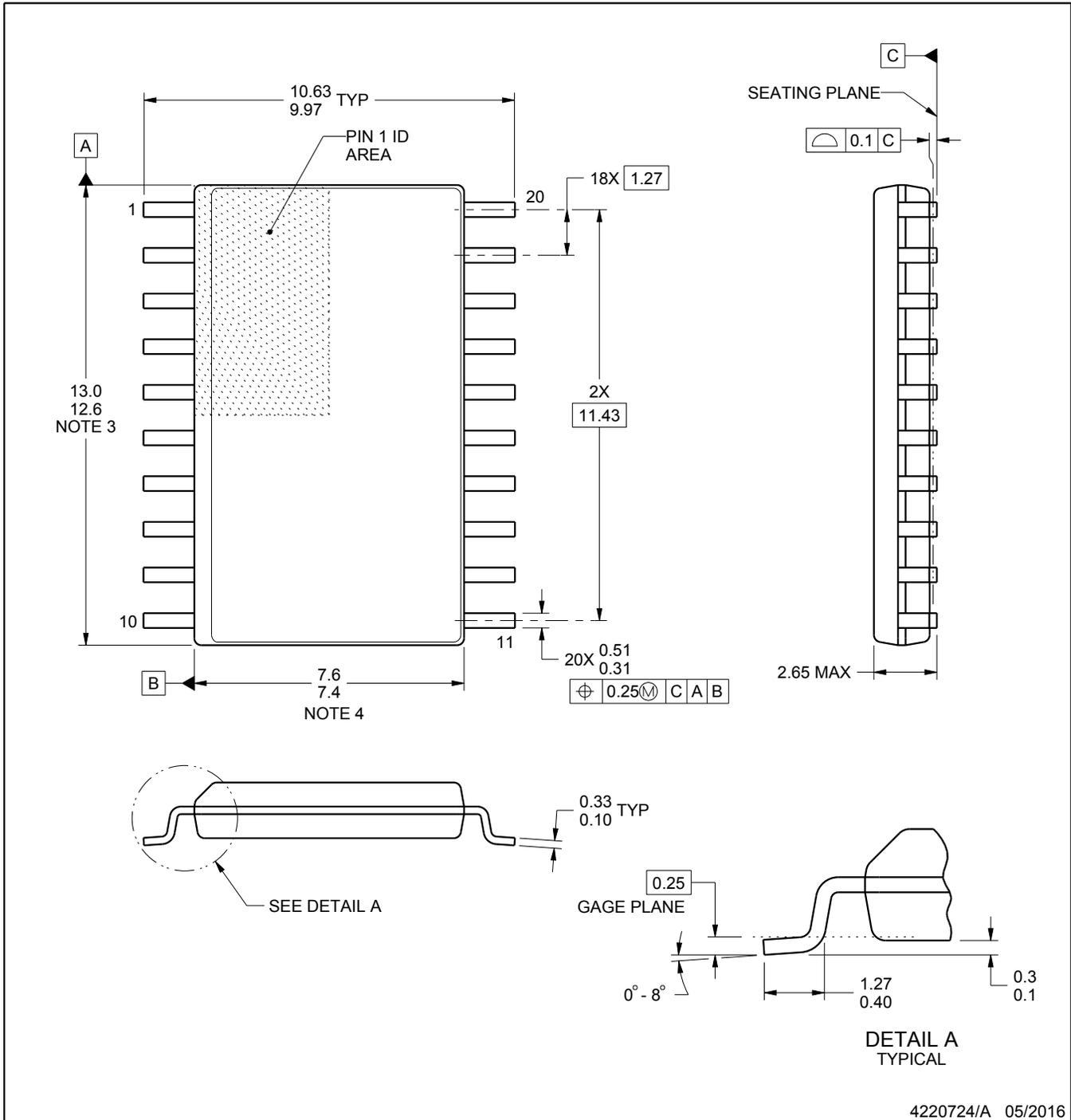
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



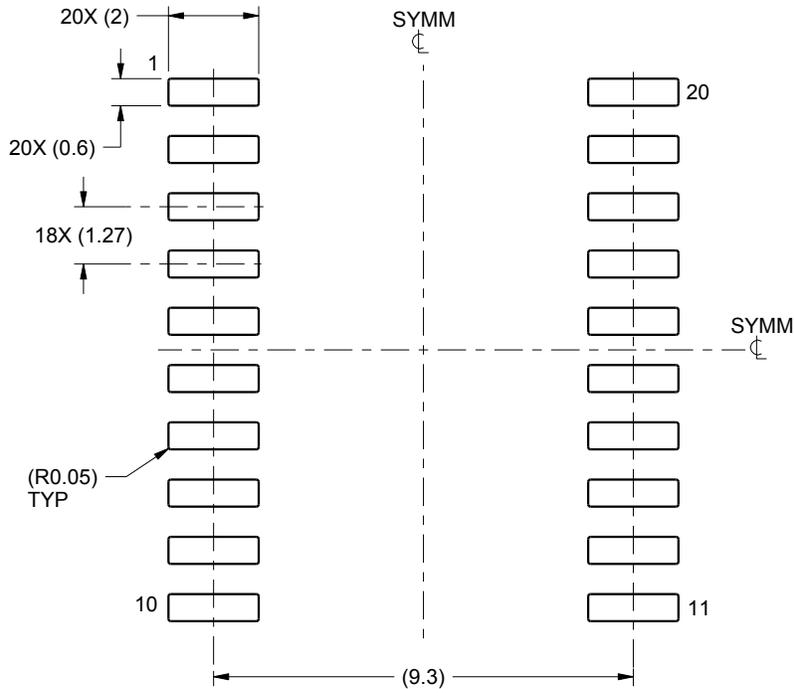
4220724/A 05/2016

# EXAMPLE BOARD LAYOUT

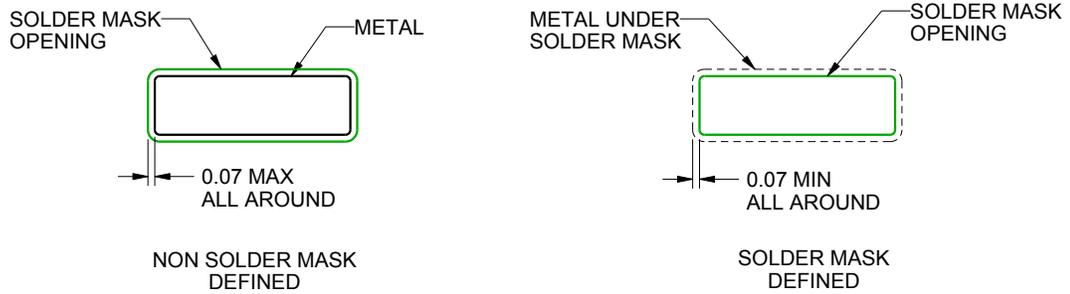
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

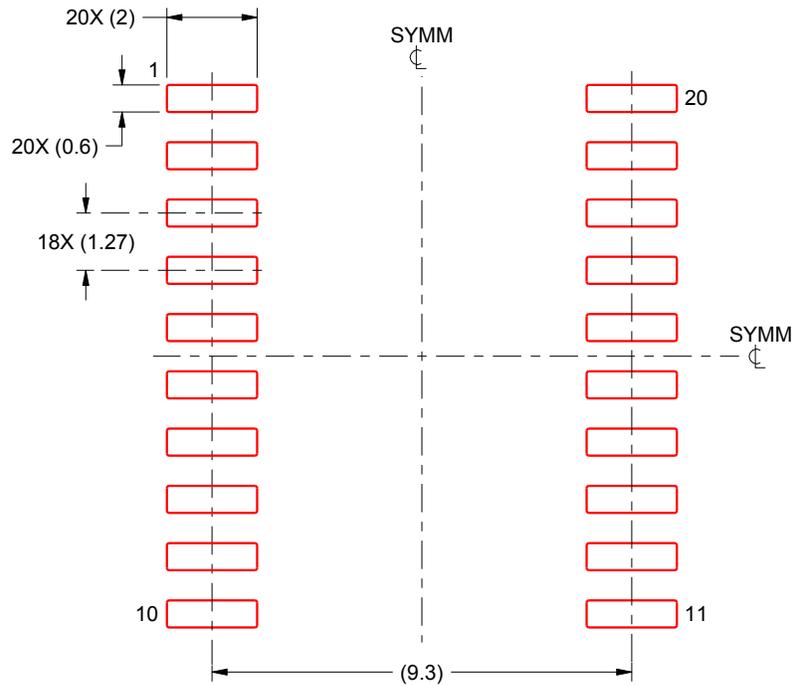
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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