TUSB1002A USB3.2 10Gbps 双通道线性转接驱动器

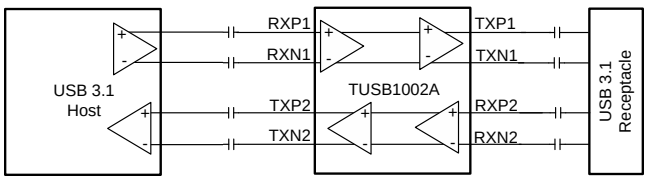
1 特性

- 支持 USB3.2 x1 SuperSpeed (5Gbps) 和 SuperSpeedPlus (10Gbps)
- 支持 PCI Express Gen3、SATA Express 和 SATA Gen3。
- 超低功耗架构
  - 活动：<300mW
  - 断开/U2/U3：< 1.9mW
  - 关断：< 700µW
- 可调节电压输出摆幅线性范围高达 1200 mVpp
- 无主机/设备端要求
- 16 种线性均衡设置，高达 16dB（10Gbps 时）
- 可调节直流均衡增益
- 支持热插拔
- 与 LVPE502A 和 LVPE512 USB 3.0 转接驱动器引脚兼容
- 与 TUSB1002 转接驱动器引脚对引脚兼容
- 温度范围：0°C 至 70°C（商业级）和 –40°C 至 85°C（工业级）
- ±5kV HBM ESD
- 由 3.3V 单电源供电。
- 采用 4mm x 4mm VQFN 封装

2 应用

- 笔记本和台式机
- 电视
- 平板电脑
- 手机
- 有源电缆
- 扩展坞

简化原理图



3 说明

TUSB1002A 是业内首款双通道 USB 3.2 x1 SuperSpeedPlus (SSP) 转接驱动器和信号调节器。该器件采用超低功耗架构，由 3.3V 电源供电，具有很低的功耗。它支持 USB3.2 低功耗模式，可进一步降低空闲状态下的功耗。

TUSB1002A 实现了一款线性均衡器，最高可容许码间串扰 (ISI) 引入 16dB 的损耗。当 USB 信号在印刷电路板 (PCB) 或电缆上传输时，其完整性会在通道损耗和码间串扰的影响下有所降低。线性均衡器可对通道损失进行补偿，进而延长通道传输距离，从而使系统符合 USB 规范。凭借双通道和小型封装，TUSB1002A 可在 USB3.2 路径中灵活放置。

TUSB1002A 采用 24 引脚 4mm x 4mm VQFN 封装。它还具有商业级 (TUSB1002A) 和工业级 (TUSB1002AI) 两个版本。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
TUSB1002A	VQFN (24)	4.00mm x 4.00mm
TUSB1002AI		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

目录

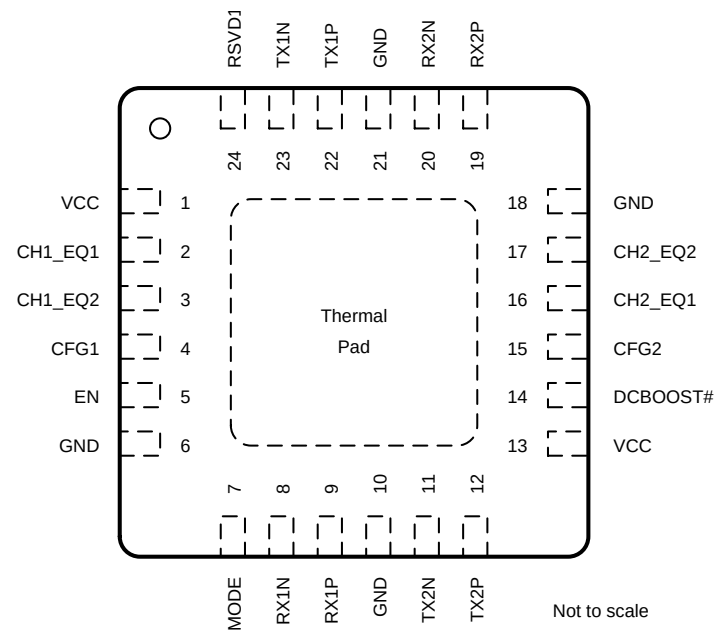
4 修订历史记录

Changes from Original (March 2018) to Revision A **Page**

- Changed text From: "Inclusion of these 330nF capacitors and 220k resistors is optional but highly recommended." To: "Inclusion of the 330 nF capacitors and 220k resistors is optional." in the *Detailed Design Procedure* ... 20
- Added ordered list of implementation options for USB connector to TUSB1002A RX pins ... 20

5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		TYPE	INTERNAL PULLUP PULLDOWN	DESCRIPTION
NAME	NO.			
RX1P	9	90Ω Differential Input		Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1
RX1N	8			Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 1
RX2P	19	90Ω Differential Input		Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2
RX2N	20			Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 2.
TX1P	22	90Ω Differential Output		Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1.
TX1N	23			Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 1.
TX2P	12	90Ω Differential Output		Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2.
TX2N	11			Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 2.
CH1_EQ1	2	I (4-level)	PU (approx 45K) PD (approx 95K)	CH1_EQ1. Configuration pin used to control Rx EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. This pin along with CH1_EQ2 allows for up to 16 equalization settings.
CH1_EQ2	3	I (4-level)		CH1_EQ2. Configuration pin used to control Rx EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. This pin along with CH1_EQ1 allows for up to 16 equalization settings.
CH2_EQ1	16	I (4-level)		CH2_EQ1. Configuration pin used to control Rx EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. This pin along with CH2_EQ2 allows for up to 16 equalization settings.
CH2_EQ2	17	I (4-level)		CH2_EQ2. Configuration pin used to control Rx EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. This pin along with CH2_EQ1 allows for up to 16 equalization settings.
EN	5	I (2-level)	PU (approx 400 K)	EN. Places TUSB1002A into shutdown mode when asserted low. Normal operation when pin is asserted high. When in shutdown, TUSB1002A's receiver terminations will be high impedance and tx/rx channels will be disabled.

Pin Functions (continued)

PIN		TYPE	INTERNAL PULLUP PULLDOWN	DESCRIPTION
NAME	NO.			
CFG1	4	I (4-level)	PU (approx 45K) PD (approx 95K)	CFG1. This pin along with CFG2 will select VOD linearity range and DC gain for both channels 1 and 2. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. Refer to 表 3 for VOD linearity range and DC gain options.
CFG2	15	I (4-level)	PU (approx 45K) PD (approx 95K)	CFG2. This pin along with CFG1 will set VOD linearity range and DC gain for both channels 1 and 2. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. Refer to 表 3 for VOD linearity range and DC gain options.
MODE	7	I (4-level)	PU (approx 45 K) PD (approx 95K)	MODE. This pin is for selecting different modes of operation. The state of this pin is sampled after the rising edge of EN. Refer to 图 2 for details of timing. 0 = Basic Redriver Mode. R = PCIe / Test Mode. PCIe Mode and TI Internal use only F = USB3.2 x1 Dual Channel Operation enabled (TUSB1002A normal mode). 1 = USB3.2 x1 Single-channel operation.
RSVD1	24	O		RSVD1. Under normal operation, this pin will be driven low by TUSB1002A. Recommend leaving this pin unconnected on PCB.
DCBOOST#	14	I (2-level)	PU (approx 400 K)	DCBOOST#. This pin when asserted low will increase the DC Gain level defined in表 3 by +1 dB unless already at +2dB. If DC Gain level defined in表 3 is already at +2 dB, then asserting this pin low will not change the DC Gain level. This pin can be left unconnected if this function is not needed. 1 = DC Gain defined by 表 3. 0 = DC Gain defined by 表 3 is increased by +1 dB.
VCC	1, 13	Power		3.3 V (±10%) Supply.
GND	6, 10, 18, 21	GND		Ground
Thermal pad				Thermal pad. Recommend connecting to a solid ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	V_{CC}	-0.3	4	V
Voltage Range on I/O pins	Differential voltage for RX1P/N and RX2P/N	-2.5	2.5	V
	Voltage at RX pins	-0.5	4	V
	Voltage on Control pins	-0.5	4	V
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{PSN}	Supply noise on V_{CC} pins			100	mV
T_A	TUSB1002A Ambient temperature	0		70	°C
	TUSB1002AI Ambient temperature	-40		85	°C
T_J	TUSB1002A Junction temperature	0		105	°C
	TUSB1002AI Junction temperature	-40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB1002A RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
$P_{U0\_SSP\_1200mV}$	Power under USB3.1 operation in U0 operating at SuperSpeedPlug datarate with linear range set to 1200mV.	At 10 Gbps; V_{CC} = 3.3 V; EN = 1; Pattern = CP9; V_{OD} = 1200mVpp		330		mW
$P_{U0\_SSP\_1000mV}$	Power under USB3.1 operation in U0 operating at SuperSpeedPlug datarate with linear range set to 1000mV.	At 10 Gbps; V_{CC} = 3.3 V; EN = 1; Pattern = CP9; V_{OD} = 1000mVpp		310		mW
$P_{U0\_SSP\_900mV}$	Power under USB3.1 operation in U0 operating at SuperSpeedPlug datarate with linear range set to 900mV.	At 10 Gbps; V_{CC} = 3.3 V; EN = 1; Pattern = CP9; V_{OD} = 900mVpp		295		mW
P_{U1}	Power in U1 with linear range set to 1200mV.	In U1; V_{CC} = 3.3 V; EN = 1; V_{OD} = 1200mVpp		330		mW
P_{U2U3}	Power when in U2/U3 state.	V_{CC} = 3.3 V; EN = 1; Both channels in U2/U3;		1.5		mW
$P_{DISCONNECT\_NONE}$	Power when no USB device detected on both TX1P/N and TX2P/N.	V_{CC} = 3.3 V; EN = 1; RX1 and RX2 termination disabled;		1.9		mW
$P_{DISCONNECT\_ONE}$	Power when a single USB device detected on either TX1P/N or TX2P/N.	V_{CC} = 3.3 V; EN = 1; Either RX1 or RX2 termination enabled but not both enabled;		1.9		mW
$P_{SHUTDOWN}$	Shutdown power when EN = 0.	VCC = 3.3 V; EN = 0;		0.7		mW
4-level Inputs (CFG[2:1], MODE, CH1_EQ[2:1], CH2_EQ[2:1])						
V_{TH}	Threshold "0" / "R"	V_{CC} = 3.3 V		0.55		V
	Threshold "R" / "F"	V_{CC} = 3.3 V		1.65		V
	Threshold "F" / "1"	V_{CC} = 3.3 V		2.8		V
I_{IH}	High-level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	20		80	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	-160		-40	µA
R_{PU}	Internal pullup resistance			45		kΩ
R_{PD}	Internal pulldown resistance			95		kΩ
EN, DCBOOST#						
V_{IH}	High-level input voltage	V_{CC} = 3.3 V	1.7		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 3.3 V	0		0.7	V
I_{IH}	High-level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	-10		10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	-15		15	µA
R_{PU_EN}	Internal pullup resistance for EN and DCBOOST#			400		kΩ
USB3.1 Receiver Interface (RX1P/N and RX2P/N)						
$R_{L\_100\ MHz}$	Rx Differential return loss at 100 MHz to 2.5 GHz	SDD11 100 MHz to 2.5 GHz at 90-ohms		-18		dB
$R_{L\_5\ GHz}$	Rx Differential return loss at 5 GHz	SDD11 5 GHz at 90-ohms		-14		dB
$R_{L\_10\ GHz}$	Rx Differential return loss from 5 to 10 GHz	SDD11 5 GHz to 10 GHz at 90-ohms		-6		dB
R_{L_CM}	Rx common mode return loss	SCC11 0.5 to 5 GHz at 90-ohms		-12		dB
X-Talk	Differential crosstalk between TX and RX signal pairs			-50		dB
$E_{ACGAIN\_5\ GHz}$	Max AC Equalization Gain	50 mVpp CP10 at 5 GHz; VCC = 3.3V;		16		dB

Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_{DC_GAIN0}	DC Gain at 0 dB setting	200 mVpp VID at 100 MHz; 1200mV Linear Range Setting;		.7		dB
E_{DC_GAIN1}	DC Gain at 1 dB setting	200 mVpp VID at 100 MHz; 1200mV Linear Range Setting;		1.6		dB
E_{DC_GAIN2}	DC Gain at 2 dB setting	200 mVpp VID at 100 MHz; 1000mV Linear Range Setting;		2.3		dB
E_{DC_GAIN-1}	DC Gain at -1 dB setting	200 mVpp VID at 100 MHz; 1200mV Linear Range Setting;		-0.25		dB
V_{DIFF_IN}	Input differential peak-peak voltage swing range			1200		mV
$V_{RX-DC-CM}$	RX DC common mode voltage			0		V
$R_{RX-DC-CM}$	RX DC common mode impedance	Measured at connector; Present when USB Device detected on TXP/N;	18		30	Ω
$R_{RX-DC-DIFF}$	RX DC differential impedance	Measured at connector; Present when USB Device detected on TXP/N;	72		120	Ω
$Z_{RX-DC-DIFF}$	DC Input CM Input Impedance V > 0 during RESET or power down.	1. Rx DC CM Impedance with Rx terminations not powered. 2. Measured over the range 0 - 500 mV with respect to GND. 3. Only DC input CM Input impedance V > 0 is specified.	35			kΩ
$V_{RX-SIGNAL-DET}$	Input differential peak-to-peak signal detect assert level	At 10 Gbps; No loss input channel and PRBS7 pattern.		85		mV
$V_{RX-IDLE-DET}$	Input differential peak-to-peak signal detect de-assert level	At 10 Gbps; No loss input channel and PRBS7 pattern.		60		mV
$V_{RX-LFPS-DET}$	LFPS detect threshold.	Below min is squelched	100		310	mV
$V_{RX-CM-AC-P}$	Peak RX AC common mode voltage	Measured at package pin.			150	mV
USB3.1 Transmitter Interface (TX1P/N and TX2P/N)						
$R_{L\_TX\_100\ MHz}$	Tx Differential return loss at 100 MHz	SDD22 100 MHz - 2.5 GHz at 90-ohms		-20		dB
$R_{L\_TX\_2.5\ GHz}$	Tx Differential return loss at 5 GHz	SDD22 5 GHz at 90-ohms		-16		dB
$R_{L\_TX\_10\ GHz}$	Tx Differential return loss from 5 to 10 GHz	SDD22 5 GHz to 10 GHz at 90-ohms		-8.5		dB
$R_{L\_TX\_CM}$	Tx common mode return loss	SCC22 0.5 to 5 GHz at 90-ohms		-6.7		dB
$V_{TX-DIFFPP-1200}$	Differential peak-to-peak TX voltage swing linear dynamic range at 100MHz	1200 mVpp setting; 100MHz; Measured at -1dB compression point = 20 log(VOD/VOD_linear)		1000		mV
	Differential peak-to-peak TX voltage swing linear dynamic range at 5GHz	1200 mVpp setting; 5GHz; Measured at -1dB compression point = 20 log(VOD/VOD_linear)		1300		mV
$V_{TX-DIFFPP-1000}$	Differential peak-to-peak TX voltage swing linear dynamic range at 100MHz	1000 mVpp setting; 100MHz; Measured at -1dB compression point = 20 log(VOD/VOD_linear)		900		mV
	Differential peak-to-peak TX voltage swing linear dynamic range at 5GHz	1000 mVpp setting; 5GHz; Measured at -1dB compression point = 20 log(VOD/VOD_linear)		1150		mV
$V_{TX-DIFFPP-900}$	Differential peak-to-peak TX voltage swing linear dynamic range at 100MHz	900 mVpp setting; 100MHz; Measured at -1dB compression point = 20 log(VOD/VOD_linear)		800		mV
	Differential peak-to-peak TX voltage swing linear dynamic range at 5GHz	900 mVpp setting; 5GHz; Measured at -1dB compression point = 20 log(VOD/VOD_linear)		1000		mV
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during Rx Detection.	Measured at package pins.			600	mV

Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common mode voltage change U2/U3 state.	Max allowed instantaneous commode-mode voltage at connector side of AC coupling capacitor. This is an absolute voltage spec referenced to the receive side termination ground.	-600		600	mV
$V_{TX-DC-CM}$	TX DC common mode voltage	1200mVpp linear range setting;	0	1.85	2.05	V
$V_{TX-CM-AC-PP-ACTIVE}$	Transmitter AC common mode peak-peak voltage in U0. Maximum mismatch from TXP+TXN for both time and amplitude.	1200mVpp linear setting; CHx_EQ setting matches input channel insertion loss;			116	mV
$V_{TX-IDLE-DIFF-AC-PP}$	AC electrical idle differential peak-to-peak output voltage		0		10	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common mode voltage between U1 and U0				200	mV
$R_{TX-DC-CM}$	TX DC common mode impedance		18		30	Ω
$R_{TX-DC-DIFF}$	TX DC differential impedance		72		120	Ω
$I_{TX-SHORT}$	Transmitter short-circuit current limit.				107	mA
$C_{AC-COUPLING}$	External AC coupling capacitor on differential pairs.		75		265	nF

6.6 Timing Requirements

over operating free-air temperature and voltage range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
t_{d_pg}	Internal power good asserted high when V_{CC} is at 2.5V			5	µs
t_{CFG_SU}	CFG(1) pins setup before internal Reset(2) high	0			µs
t_{CFG_HD}	CFG(1) pins hold after internal Reset(2) high	500			µs
t_{VCC_RAMP}	V_{CC} supply ramp requirement	0.1		50	ms

(1) Following pins comprise CFG pins: MODE, CFG[2:1], CH1_EQ[2:1], CH2_EQ[2:1]
(2) Internal reset is the logical AND of EN pin and internal power good.

6.7 Switching Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{IDLEEntry}$	Delay from U0 to electrical idle	V_{CC} = 3.0 V; EN = 1;See 图 1			150	ps
$t_{IDLEEntry\_U1}$	U1 exit time. Break in electrical idle to transmission of LFPS.	V_{CC} = 3.0 V; EN = 1; See 图 1			150	ps
$t_{IDLEEntry\_U2U3}$	U2/U3 exit time; Break in electrical idle to transmission of LFPS	V_{CC} = 3.0 V; EN = 1; See 图 1			6	µs
t_{DIFF_DLY}	Differential propagation delay	V_{CC} = 3.0 V; EN = 1;			150	ps
t_{PWRUP_ACTIVE}	Time from assertion of EN to device active and performing Rx.Detect on both ports	V_{CC} = 3.0 V; EN = 1;			8	ms
$t_{TX\_RISE\_FALL}$	Transmitter rise/fall time	V_{CC} = 3.3 V; EN = 1; 10 Gbps; 20% to 80% of differential output; 1200 mVpp linear range setting; Fast Input rise/fall time;		27		ps
$t_{RF\_MISMATCH}$	Transmitter rise/fall mismatch	V_{CC} = 3.3 V; EN = 1; 10 Gbps; 20% to 80% of differential output; 1200 mVpp linear range setting; 1000 mVpp VID		.6		ps
t_{TX_DJ}	Transmitter residual deterministic jitter	V_{CC} = 3.3 V; EN = 1; 10 Gbps; 1200 mVpp linear range setting; Input channel loss of 12 dB; Output channel loss of 1.5 dB; Optimized EQ;		0.05		UI

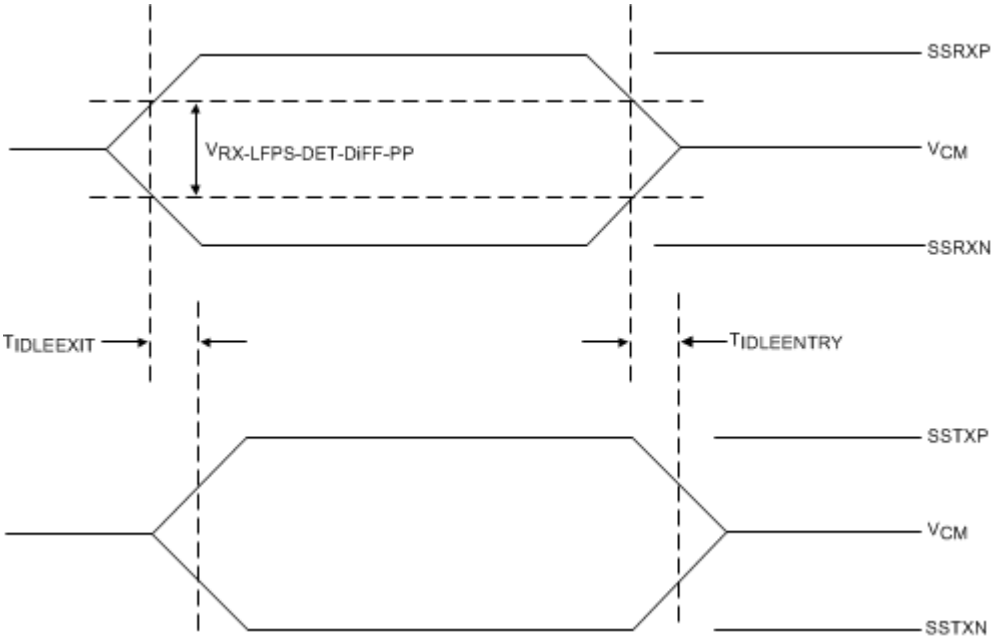


图 1. Idle Entry and Exit Latency

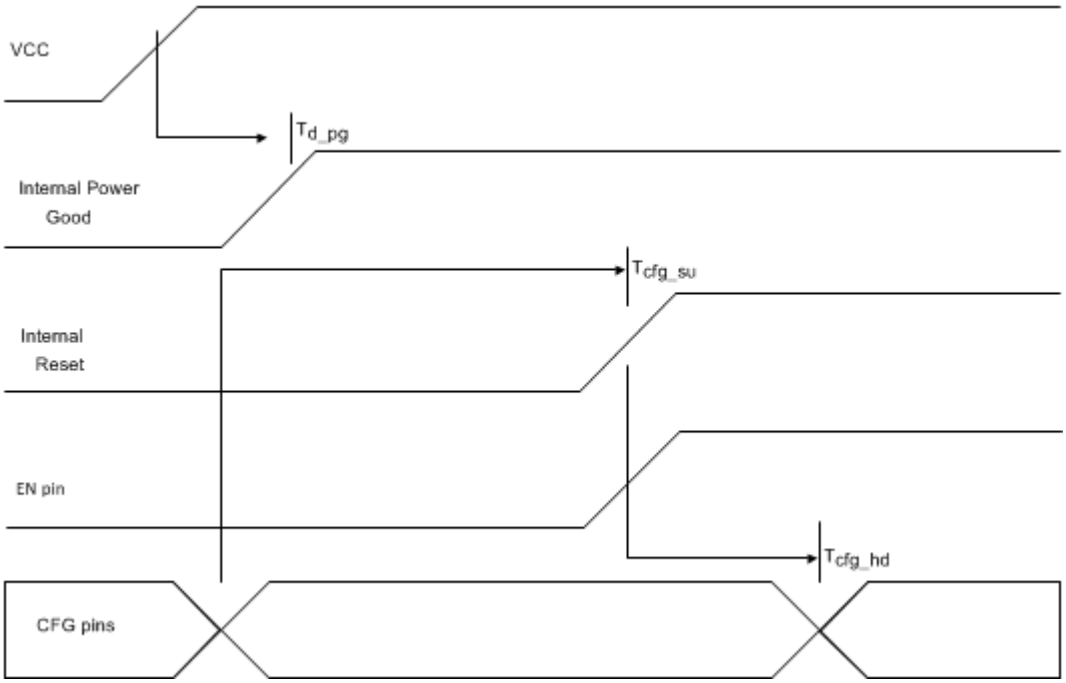


图 2. Power-Up Diagram

6.8 Typical Characteristics

V_{CC} = 3.3V , 25°C, 200 mVpp V_{ID} sine wave, Z_O = 100 Ω, RGE package

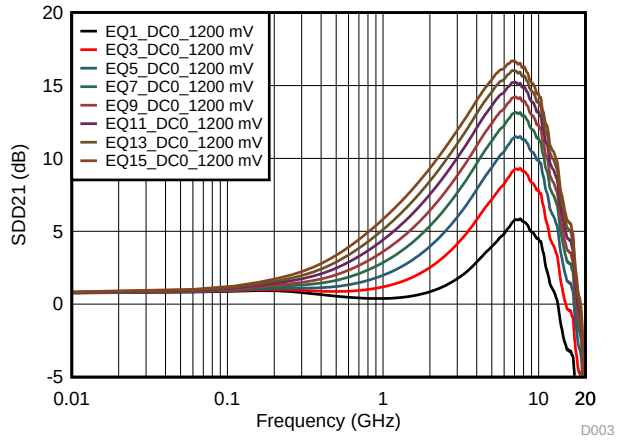


图 3. 1200 mV DC0 Gain Odd EQ Settings Curves

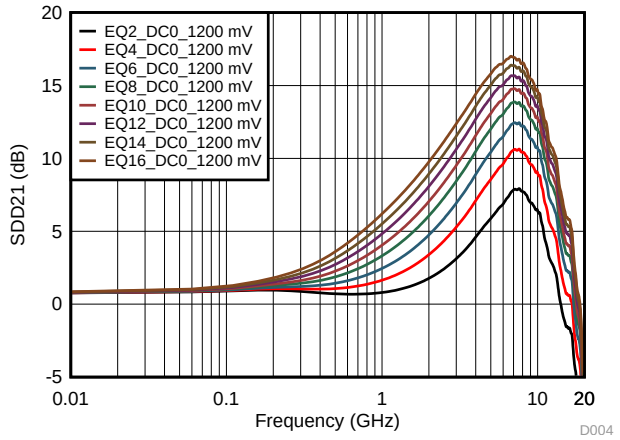


图 4. 1200 mV DC0 Even EQ Settings Curves

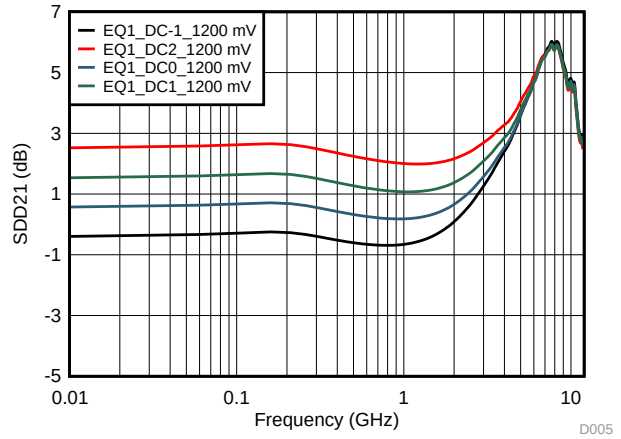


图 5. 1200 mV DC Gain Adjustments Curves

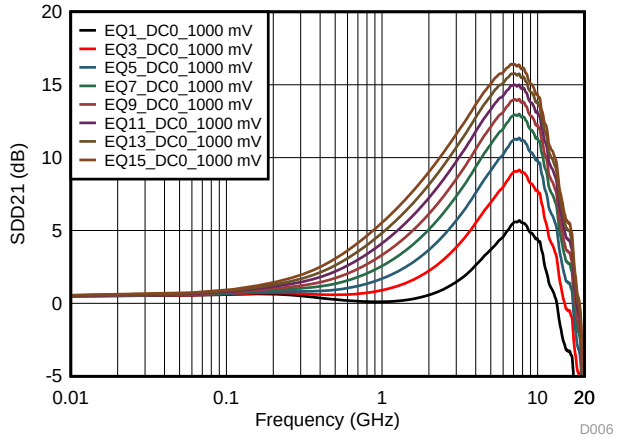


图 6. 1000 mV DC0 Gain Odd EQ Settings Curves

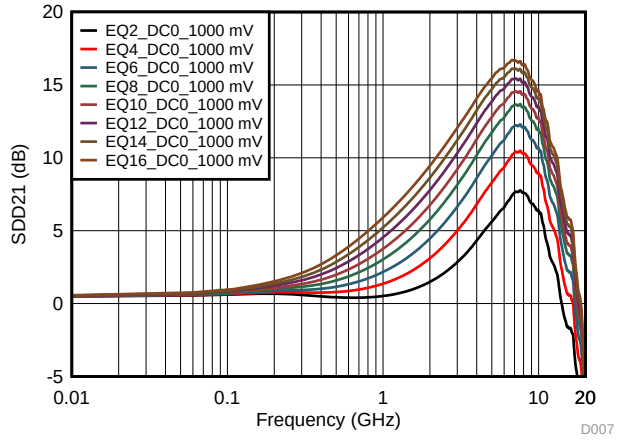


图 7. 1000 mV DC0 Gain Even EQ Settings Curves

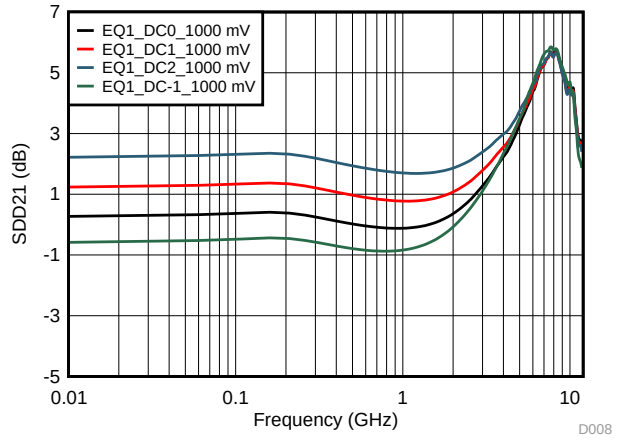


图 8. 1000 mV DC Gain Adjustments Curves

Typical Characteristics (接下页)

V_{CC} = 3.3V , 25°C, 200 mVpp V_{ID} sine wave, Z_O = 100 Ω, RGE package

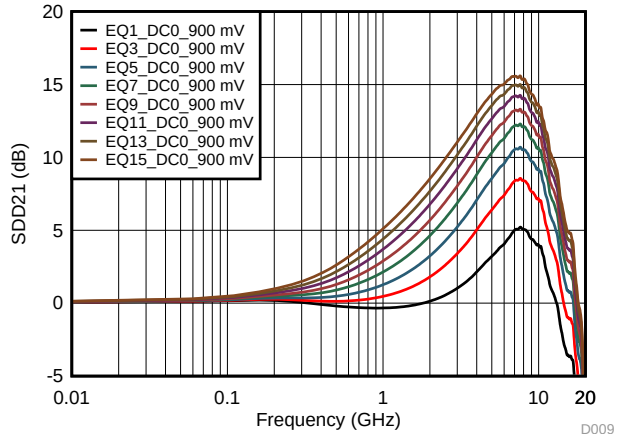


图 9. 900 mV DC0 Gain Odd EQ Settings Curves

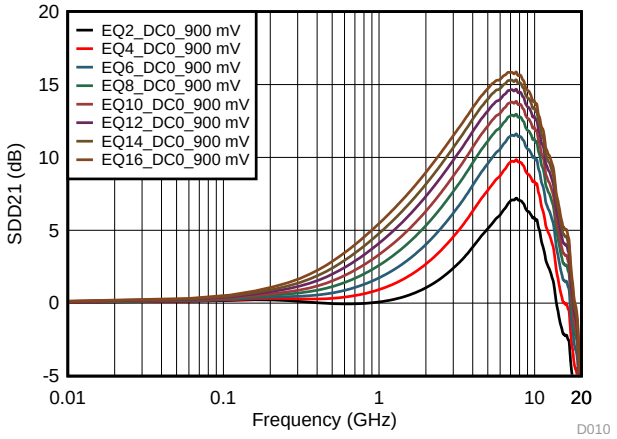


图 10. 900 mV DC0 Gain Even EQ Settings Curves

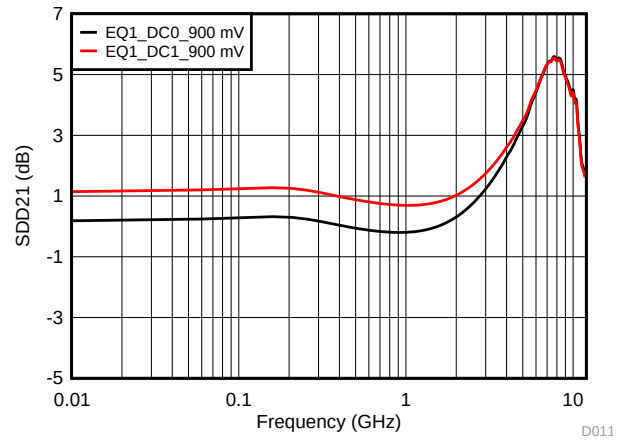


图 11. 900 mV DC Gain Adjustment Curves

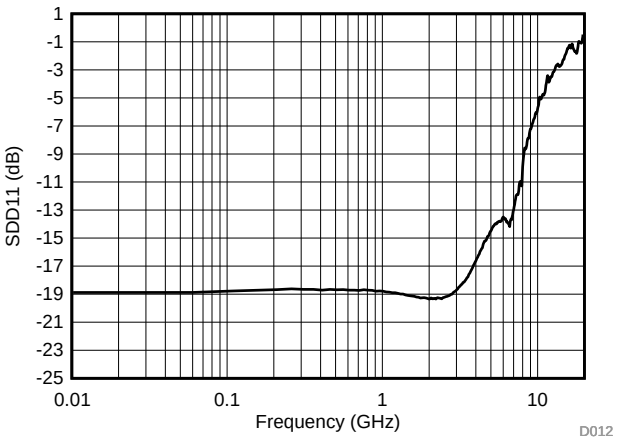


图 12. SDD11 Return Loss

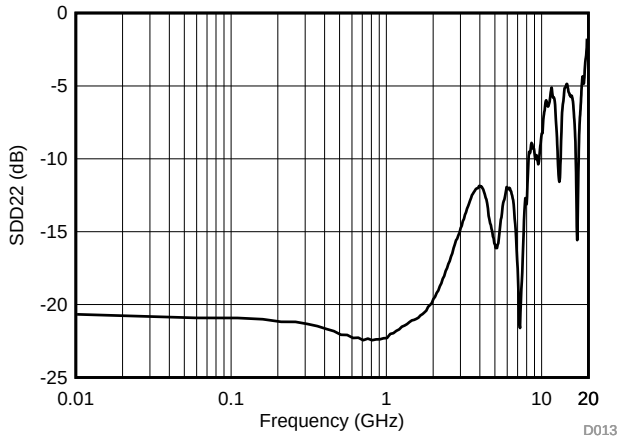


图 13. SDD22 Return Loss

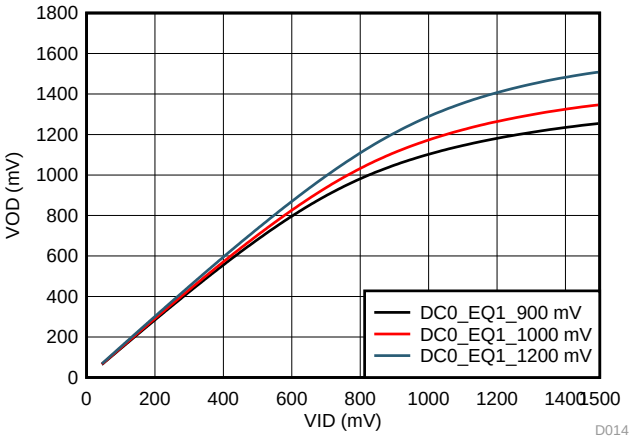


图 14. 5-GHz Sine Wave VID vs VOD Linearity Range Setting

Typical Characteristics (接下页)

V_{CC} = 3.3V , 25°C, 200 mVpp V_{ID} sine wave, Z_O = 100 Ω, RGE package

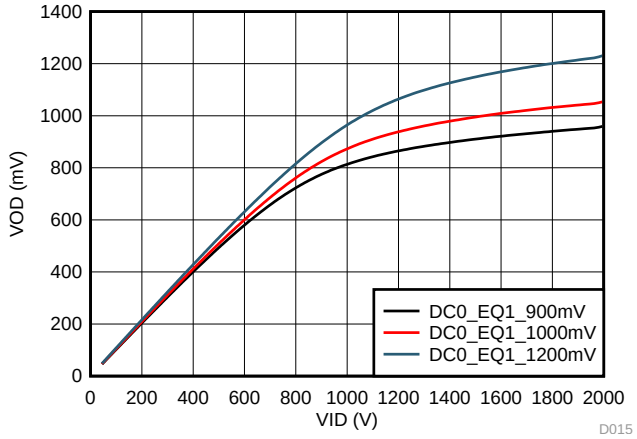


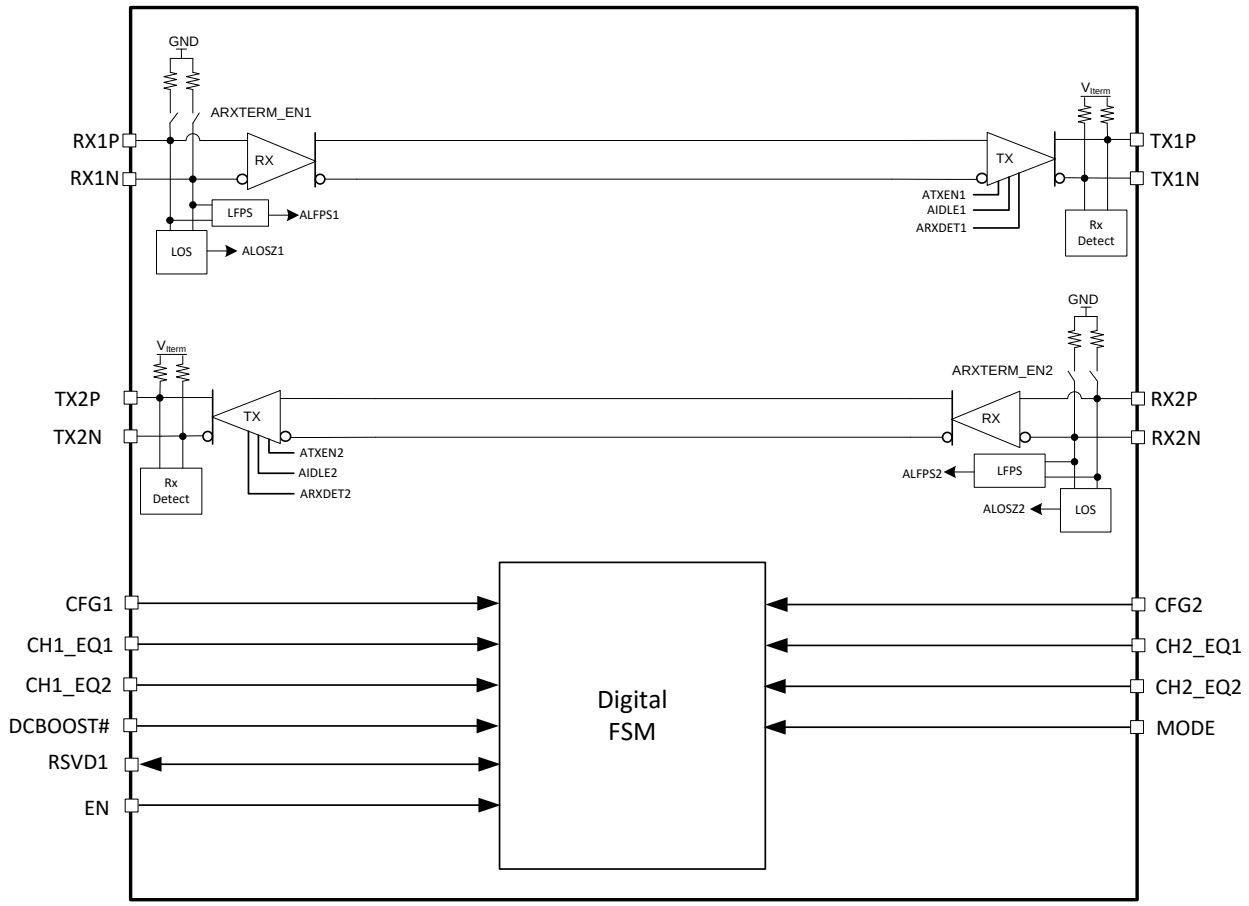
图 15. 100-MHz Sine Wave VID vs VOD Linearity Range Setting

7 Detailed Description

7.1 Overview

The TUSB1002A is the industry's first, dual lane USB 3.2 x1 SuperSpeedPlus redriver. As signals traverse through a channel (like FR4 trace) the amplitude of the signal is attenuated. The attenuation varies depending on the frequency content of the signal. Depending the length of the channel this attenuation could be large enough resulting in signal integrity issues at a USB 3.2 receiver. By placing a TUSB1002A between USB3.2 host and device the attenuation effect of the channel can eliminated or minimized. The result is a USB3.2 compatible eye at the devices receiver. With up to 16 receiver equalization settings, the TUSB1002A can support many different channel loss combinations. The TUSB1002A offers low power consumption on a single 3.3 V supply with its ultra low power architecture. It supports the USB3.2 low power modes which further reduces idle power consumption. The TUSB1002A settings are configured through pins. In addition to equalization adjustment, the TUSB1002A provides knobs for adjusting DC gain and voltage output linearity range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 4-Level Control Inputs

The TUSB1002A has (MODE, CFG1, CFG2, CH1_EQ1, CH1_EQ2, CH2_EQ1, and CH2_EQ2) 4-level inputs pins that are used to control the equalization gain and the output voltage swing dynamic range. These 4-level inputs use a resistor divider to help set the 4 valid levels and provide a wider range of control settings. These resistors together with the external resistor connection combine to achieve the desired voltage level.

表 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

注

In order to conserve power, the TUSB1002A disables 4-level input's internal pull-up/pull-down resistors after the state of 4-level pins have been sampled on rising edge of EN. A change of state for any four level input pin is not applied to TUSB1002A until after EN pin transitions from low to high.

7.3.2 Linear Equalization

With a linear equalizer, the TUSB1002A can electrically shorten a particular channel allowing for longer run lengths.

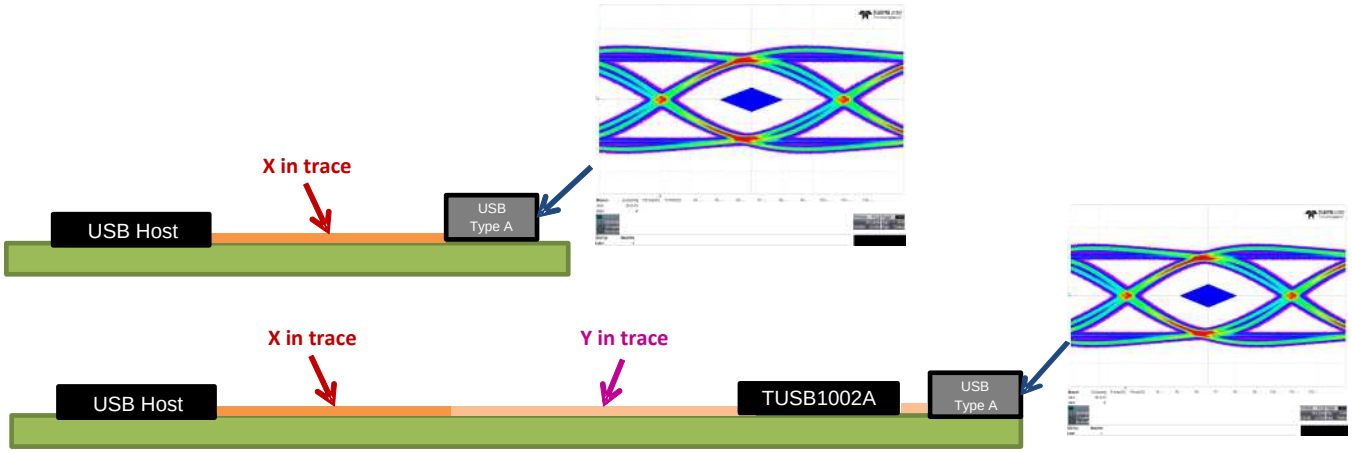


图 16. Linear Equalizer

With a TUSB1002A, a longer trace can be made to have similar insertion loss as a shorter trace. For example, a long trace of X + Y inches can be made to have similar loss characteristics of a shorter trace of X inches.

The receiver equalization level for each channel is determined by the state of the CHx_EQ1 and CHx_EQ2 pins, where x = 1 or 2.

表 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.0 / 3.6
2	0	R	2.1 / 5.5
3	0	F	3.0 / 6.8
4	0	1	4.0 / 8.1
5	R	0	4.6 / 9.0
6	R	R	5.5 / 10.0
7	R	F	6.2 / 10.8
8	R	1	6.9 / 11.6
9	F	0	7.3 / 11.9
10	F	R	7.9 / 12.6
11	F	F	8.4 / 13.1
12	F	1	9.0 / 13.7
13	1	0	9.4 / 14.1
14	1	R	9.9 / 14.6
15	1	F	10.3 / 14.9
16	1	1	10.7 / 15.3

7.3.3 Adjustable VOD Linear Range and DC Gain

The CFG1 and CFG2 pins can be used to adjust the TUSB1002A output voltage swing linear range and receiver equalization DC gain. 表 3 details the available options.

For best performance, the TUSB1002A should be operated within its defined VOD linearity range. The gain of the incoming VID should be kept to less than or equal to the TUSB1002A VOD linear range setting. The can be determined by 公式 1:

$$\text{VID at 5 GHz} = \text{VOD} \times (10^{-(Gv/20)}) \quad (1)$$

where

- Gv = TUSB1002A Gain and VOD = TUSB1002A VOD linearity setting.

For example, for a VOD linearity range setting of 1200 mV, the maximum incoming VID signal at 5 GHz with a CHx_EQ[1:0] setting of 2 (5.5 dB) is 1200 x ($10^{-(5.5/20)}$) = 637 mVpp. The TUSB1002A can be operated outside its VOD linear range but jitter will be higher.

表 3. VOD Linear Range and DC Gain

SETTING #	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 V_{OD} LINEAR RANGE (mVpp)	CH2 V_{OD} LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1200	1200
10	F	R	+2	+2	1200	1200
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	+2	0	1200	1200
14	1	R	0	+2	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200

7.3.4 USB3.2 Dual Channel Operation (MODE = “F”)

TheTUSB1002A in dual-channel operation waits for far-end terminations on both channels 1 and 2 before transitioning to fully active state (U0 mode). This mode of operation, defined as MODE pin = ‘F’, is the most common configuration for USB3.2 Source (DFP) and Sink (UFP) applications.

In a USB3.2 x2 application, two TUSB1002A redrivers are used: One on the config lane and the other on the non-config lane. The TUSB1002A on the non-config lane must be placed in basic redriver mode (MODE pin = "0"). The TUSB1002A on the config lane should be placed in USB3.2 dual channel operation (MODE pin = "F"). The expectation is the USB power delivery (PD) controller will hold both TUSB1002A in shutdown mode until a connection can be established. Upon establishing a connection, the USB PD controller will place each TUSB1002A into the appropriate mode.

7.3.5 USB3.2 Single Channel Operation (MODE = “1”)

In some applications, like Type-C USB3.2 active cables, only one of the two channels may be active. For this application, setting MODE pin = ‘1’, enables single-channel operation. In this mode of operation, the TUSB1002A attempts far-end termination on both channels 1 and 2. The channel which has a far-end termination detected is enabled while the remaining channel is disabled. If far-end termination is detected on both channels, then TUSB1002A behaves in dual channel operation (both channels enabled).

7.3.6 PCIe/SATA/SATA Express Redriver Operation (MODE = “R”; CFG1 = "0"; CFG2 = "0")

The TUSB1002A can be used as a PCI Express (PCIe) Gen3, SATA Gen3, or SATA Express redriver. When TUSB1002A's MODE pin = “R”, CFG1 pin = "0", and CFG2 pin = "0", the TUSB1002A enables both channels (upstream and downstream) receiver and transmitter paths upon detecting far-end termination on both TX1 and TX2. Both upstream and downstream paths remain enabled until EN pin is de-asserted low. All USB3.2 power management functionality is disabled in this mode. In this mode, the TUSB1002A is transparent to PCIe link power management (L0s, L1) and SATA interface power states. Once far-end termination is detected on both TX1 and TX2, the TUSB1002A power is at $P_{(U0\_SSP\_1200mV)}$ regardless of the PCIe or SATA power state. To save power during system S3/S4/S5 states it is suggested to de-assert the EN pin to conserve power.

注

In this mode the linearity range will be fixed at 1200mVpp and DC gain to 0dB.

7.3.7 Basic Redriver Operation (MODE = “0”)

The TUSB1002A can be used as a basic redriver for non-USB3.2 x1 applications. When the TUSB1002A MODE pin = “0”, the TUSB1002A enables both channels receiver and transmitter paths. The channel receiver and transmitter termination are both enabled. All USB3.2 power management functionality is disabled.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The Shutdown mode is entered when EN pin is low and VCC is active and stable. This mode is the lowest power state of the TUSB1002A. While in this mode, the TUSB1002A receiver terminations is disabled.

7.4.2 Disconnect Mode

Next to Shutdown Mode, the Disconnect mode is the lowest power state of the TUSB1002A. The TUSB1002A enters this mode when exiting Shutdown mode. In this state, the TUSB1002A periodically checks for far-end receiver termination on both SSTX1 and SSTX2. Upon detection of the far-end receiver's termination on both ports, the TUSB1002A transitions to a fully active mode called U0 mode.

7.5 U0 Mode

The U0 mode is the highest power state of the TUSB1002A. Anytime high-speed traffic (SuperSpeed or SuperSpeedPlus) is being received, the TUSB1002A remains in this mode. The TUSB1002A only exits this mode if electrical idle is detected on both SSRX1 and SSRX2. While in this mode, the TUSB1002A hs speed receivers and transmitters are powered and active.

7.6 U1 Mode

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1002A receiver termination remains enabled and the TXP/N DC common mode is maintained.

7.7 U2/U3 Mode

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB1002A periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either CH1 or CH2, the TUSB1002A leaves the U2/U3 mode and transition to the Disconnect mode. It also monitors the SSRX1 and SSRX2 for a valid LFPS. Upon detection of a valid LFPS, the TUSB1002A immediately transitions to the U0 mode.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TUSB1002A is a linear redriver designed specifically to compensation for ISI jitter caused by attenuation through a passive medium like traces and cables. Because the TUSB1002A has two independent channels, it can be optimized to correct ISI in both the upstream and downstream direction through 16 different equalization choices. Placing the TUSB1002A between a USB3.2 Host/device controller and a USB3.2 receptacle can correct signal integrity issues resulting in a more robust system.

8.2 Typical USB3.2 Application

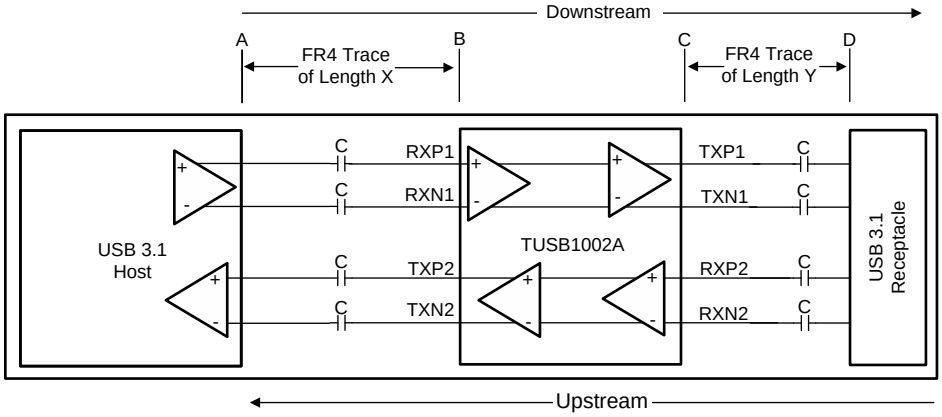


图 17. TUSB1002A in USB3.2 x1 Host Application

8.2.1 Design Requirements

For this design example, use the parameters shown in 表 4.

表 4. Design Parameters

PARAMETER	VALUE
VCC supply (3 V to 3.6 V)	3.3 V
Mode of Operation (Dual or Half Channel)	MODE = F (Floating) for USB3.2 Dual Channel
TX1, TX2, RX1 A/C coupling Capacitor (75 nF to 265 nF)	100 nF
Optional RX2 A/C coupling Capacitor (297 nF to 363 nF)	330 nF ±10%
Optional RX2 pull-down resistors on USB receptacle side of AC capacitor (200K to 242K ohms)	220 kΩ
A to B FR4 Length (inches)	8
A to B FR4 Trace Width (mils)	4
C to D FR4 length (inches)	2
C to D FR4 Trace Width (mils)	4
DC Gain (-2, -1, 0, +1, +2)	0 dB (CFG[2:1] pins floating)
Linear Range (900 mV, 1000 mV, or 1200 mV)	1200 mV (CFG[2:1] pins floating)

8.2.2 Detailed Design Procedure

The TUSB1002A differential receivers and transmitters have internal BIAS and termination. For this reason, the TUSB1002A must be connected to the USB3.2 host and receptacle through external A/C coupling capacitors. In this example, as depicted in 表 4, 100 nF capacitors are placed on TX2P and TX2N, RX1P and RX1N, and TX1P and TX1N. 330 nF A/C coupling capacitors along with 220 kΩ resistors are placed on the RX2P and RX2N. Inclusion of the 330 nF capacitors and 220k resistors is optional. The ordered list below details the three implementation options for the RX2p/n path.

Three implementation options for USB connector to TUSB1002A's RX pins:

1. DC couple TUSB1002A's RX pins to USB connector. No 330 nF capacitors and no 220 kΩ pull-down resistors.
2. 330 nF capacitors with 220 kΩ resistors as depicted in 图 18. The purpose of 220 kΩ resistors is to discharge the capacitor within 250ms after a USB device is removed from the USB connector.
3. The stub from the 220 kΩ resistor pad may create impedance discontinuities causing negative impact to performance. Assuming leakage current from external components is enough to discharge capacitor, 330 nF capacitor without the 220 kΩ resistor is a valid option.

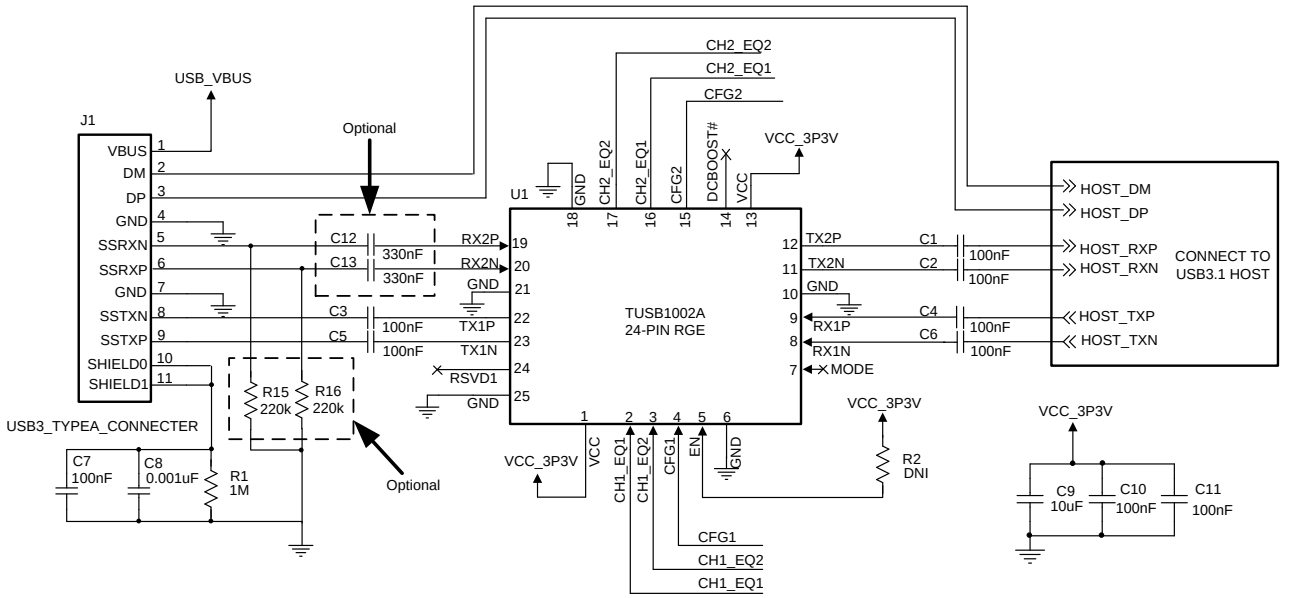


图 18. Host Implementation Schematic

The USB3.2 Dual channel operation is used in this example. Mode pin should be left floating (unconnected) when using this mode.

The TUSB1002A compensates for channel loss in both the upstream (D to C) and downstream direction (A to B). This is done by configuring the CH1_EQ[2:1] and CH2_EQ[2:1] pins to the equalization setting that matches as close possible to the channel insertion loss. In this particular example, CH1_EQ[2:1] is for path A to B which is the channel between USB3.2 host and the TUSB1002A, and CH2_EQ[2:1] is for path C to D which is the channel between TUSB1002A and the USB3.2 receptacle.

The TUSB1002A supports 5 levels of DC gain that are selected by the CFG[2:1] pins. Typically, the DC gain should be set to 0 dB but may need to be adjusted to correct any one of the following conditions:

1. Input V_{ID} too high resulting in V_{OD} being greater than USB 3.2 defined swing. For this case, a negative DC gain should be used.
2. Input V_{ID} too low resulting in V_{OD} being less than USB 3.2 defined swing. For this case, a positive DC gain should be used.
3. Low frequency discontinuities in the channel resulting in DC component of the signal clipping the vertical eye mask. For this case, a positive DC gain should be used.

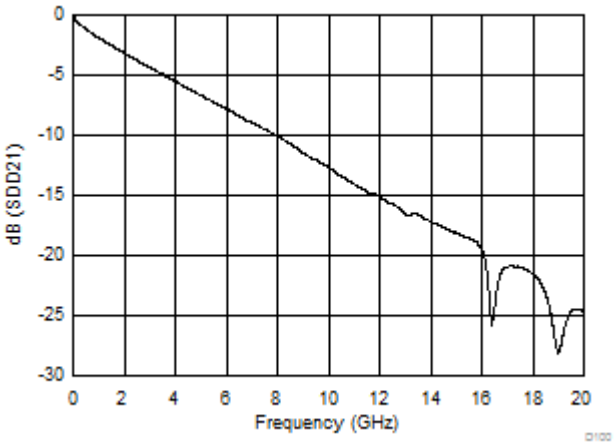
It is assumed in this example the incoming V_{ID} is at the nominal defined USB3.2 range and the channel is linear across frequency. The CFG1 and CFG2 pins can both be left floating if these assumptions are true.

In this particular example, the channel A-B has a trace length of 8 inches with a 4 mil trace width. This particular channel has about 0.83 dB per inch of insertion loss at 5 GHz. This equates to approximately 6.7 dB of loss for the entire 8 inches of trace. An additional 1.5 dB of loss is added due to package of the USB3.2 Host, TUSB1002A, and the A/C coupling capacitor. This brings the entire channel loss at 5 GHz to 6.7 dB + 1.5 dB = 8.2 dB. A typical USB 3.1 host/device will have around 3 dB of transmitter de-emphasis. Transmitter de-emphasis pre-compensates for the loss of the output channel. With 3 dB of de-emphasis, the total equalization required by the TUSB1002A is in the 5.2 dB (8.2 dB - 3 dB) range. The channel A-B for this example is connected to TUSB1002A's RX1P/N input and therefore CH1_EQ[2:1] pins are used for adjusting TUSB1002A RX1P/N equalization settings. The CH1_EQ[2:1] pins should be set such that TUSB1002A equalization is between 5dB and 8dB.

The channel C-D has a trace length of 2 inches with a 4mil trace width. Assuming 0.83 dB per inch of insertion loss, the 2 inch trace will equate to about 1.66 dB of loss at 5 GHz. An additional 2dB of loss needs to be added due to package, A/C coupling capacitor, and the USB 3.1 receptacle. The total loss is around 3.66 dB. Because channel C-D includes a USB 3.1 receptacle, the actual total loss could be much greater than 3.66dB due to the fact that devices plugged into the receptacle will also have loss. The device plugged into receptacle will have either a short or long channel. USB3.2 standard defines total loss limit of 23dB that is distributed as 8.5 dB for Host, 8.5dB for device, and 6.0dB for cable. With variable channel of devices plugged into the USB3.2 receptacle, configuring TUSB1002A's RX2P/N equalization settings is not as straight forward as Channel A-B.

Engineer can not set TUSB1002A CH2_EQ[2:1] pins to the largest equalization setting to accommodate the largest allowed USB3.2 device/cable loss of 14.5 dB. Doing so will result in TUSB1002A operating outside its linear range when a device with short channel is plugged into the receptacle. For this reason, it is recommended to configure TUSB1002A CH2_EQ[2:1] pins to equalize a shorter device channel. This will result in requiring USB3.2 host to compensate for remaining channel loss for the worse case USB3.2 channel of 14.5 dB. The definition of a short device channel is not specified in USB 3.2 specification. Therefore, an engineer must make their own loss estimate of what constitutes a short device channel. For particular example, we will assume the short channel is around 2 to 3 dB. The device's channel loss will need to be added to estimated Channel C-D loss minus the typical 3db of de-emphasis. This means CH2_EQ[2:1] pins should be configured to handle a loss of 3 to 5 db.

8.2.3 Application Curves



Freq = 5 GHz dB(SDD21) = –6.666

图 19. Insertion Loss for 8inch 4 mil FR4 Trace

8.3 Typical SATA, PCIe and SATA Express Application

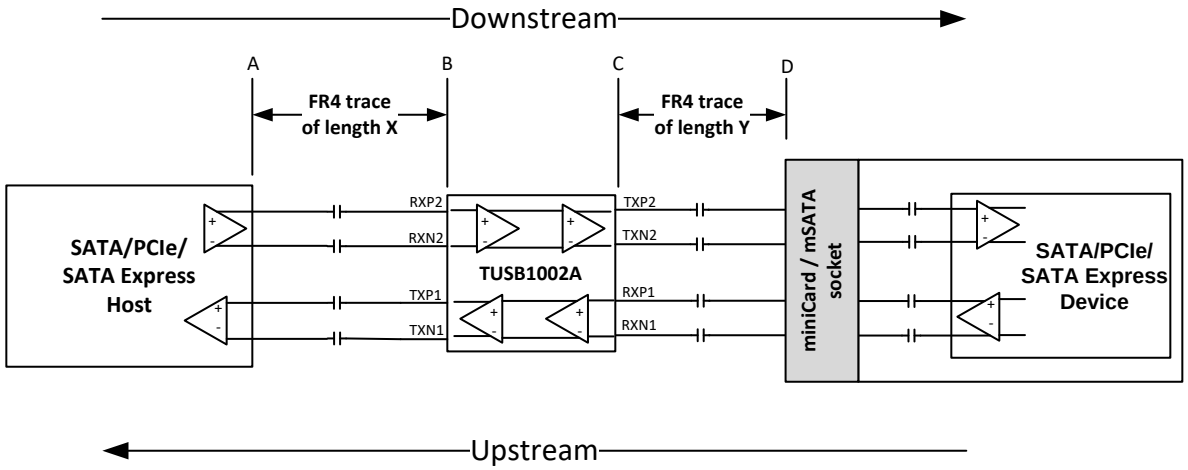


图 20. SATA/PCIe/SATA Express Typical Application

8.3.1 Design Requirements

表 5. Design Parameters

PARAMETER	VALUE
VCC supply (3 V to 3.6 V)	3.3 V
PCIe Support Required (Yes/No)	Yes
SATA Express Support Required (Yes/No)	Yes
SATA Support Required (Yes/No)	Yes, then ferrite beads (FB1 and FB2) and 49.9-ohm required. No, then ferrite bead (FB1 and FB2) and 49.9-ohm not required.
TX1, TX2, RX2 A/C coupling Capacitor (176 nF to 265 nF)	220 nF ±10%
RX1 A/C coupling Capacitor (297 nF to 363 nF)	Optional. But if implemented suggest 330 nF ±10%
A to B FR4 Length (inches)	8
A to B FR4 Trace Width (mils)	4
C to D FR4 length (inches)	2
C to D FR4 Trace Width (mils)	4
DC Gain (-2, -1, 0, +1, +2)	Not configurable when MODE = "R", CFG1 = "0", and CFG2 = "0". Will always default to 0 dB
Linear Range (900 mV, 1000 mV, or 1200 mV)	Not configurable when MODE = "R", CFG1 = "0", and CFG2 = "0". Will always default to 1200mV

8.3.2 Detailed Design Procedure

The MODE pin = "R", CFG1 = "0", and CFG2 = "0" will place the TUSB1002A into PCIe mode. In this mode, the TUSB1002A will have its DC gain fixed at 0dB and its linearity range fixed at 1200mV. The TUSB1002A will perform far-end receiver termination detection and enable both upstream and downstream paths when far-end termination is detected on both TX1 and TX2.

The AC coupling capacitor range defined for a SATA device is a lot smaller than the AC-coupling capacitor range defined for SATA Express and PCI Express (PCIe) as indicated by 图 21. The AC-coupling capacitor range defined for SATA Express and PCI Express is within the same range as the AC-coupling capacitor range defined by USB 3.1. The TUSB1002A will be able to detect PCIe and SATA Express device's receiver termination. But the SATA 12nF (max) AC-coupling capacitor prevents TUSB1002A from detecting the SATA device receiver termination. To correct this problem, a ferrite bead along with 49.9 ohm resistor must be placed between C_{TX2} and miniCard/mSATA socket. These components can be isolated from the high-speed channel when PCIe or SATA Express is active by using an NFET as shown in 图 22. The NFET should be enabled whenever a SATA

device is present. The ferrite bead chosen must present at least 600 ohms impedance at 100MHz so as to not impact high-speed signalling. It is recommended to use Murata BLM03AG601SN1 or BLM03HD601SN1D or a ferrite bead with similar characteristics from a different vendor. For applications which only require support for PCIe and SATA Express and do not need to support SATA, the ferrite beads and 49.9 ohm resistors are not needed.

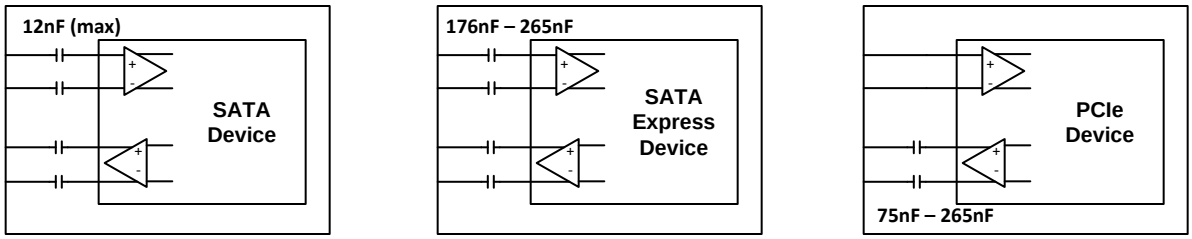


图 21. AC-Coupling capacitor Implementation for SATA, SATA Express, and PCIe Devices

The TUSB1002A power is at $P_{(U0\_SSP\_1200mV)}$ when both its upstream and downstream paths are enabled. In order to save system power in system S3/S4/S5 states, it is suggested to control the TUSB1002A EN pin. Anytime the system enters a low power state (S3, S4, or S5), it is suggested to de-assert the EN pin. While EN pin is de-asserted, the TUSB1002A will consume $P_{(SHUTDOWN)}$. Assertion of this pin is necessary anytime the system exits a lower power state.

The TUSB1002A compensates for channel loss in both the upstream (C to D) and downstream direction (A to B). This is done by configuring the CH1_EQ[2:1] and CH2_EQ[2:1] pins to the equalization setting that matches as close possible to the channel insertion loss. In this particular example, CH2_EQ[2:1] is for path A to B which is the channel between PCIe/SATA/SATA Express host and the TUSB1002A, and CH1_EQ[2:1] is for path C to D which is the channel between TUSB1002A and the miniCard/mSATA socket.

In this particular example, the channel A-B has a trace length of 8 inches with a 4 mil trace width. This particular channel has about 0.83 dB per inch of insertion loss at 5 GHz. This equates to approximately 6.7 dB of loss for the entire 8 inches of trace as depicted in 图 19. An additional 1.5 dB of loss is added due to package of the PCIe/SATA/SATA Express Host, TUSB1002A, and the A/C coupling capacitor. This brings the entire channel loss at 5 GHz to 6.7 dB + 1.5 dB = 8.2 dB. The channel A-B for this example is connected to TUSB1002A RX2P/N input and therefore CH2_EQ[2:1] pins are used for adjusting TUSB1002A RX2P/N equalization settings. The CH2_EQ[2:1] pins should be set such that TUSB1002A equalization is between 5dB and 8dB. A value closer to 5 dB maybe best if Host has transmitter de-emphasis.

A similar method should be used for the upstream path (C to D). In this particular example, C to D has a trace length of 2 inches with a 4-mil trace width. This equates to approximately 1.5 dB at 5 GHz. The SATA/SATA Express/PCIe device will have its own channel loss. This loss can be added to the C to D channel loss. For this example, we will assume a value of 5dB is acceptable to compensate for C to D channel loss as well as loss associated with the SATA/SATA Express/PCIe device. The CH1_EQ[2:1] pins should be set such that TUSB1002A equalization is 5dB.

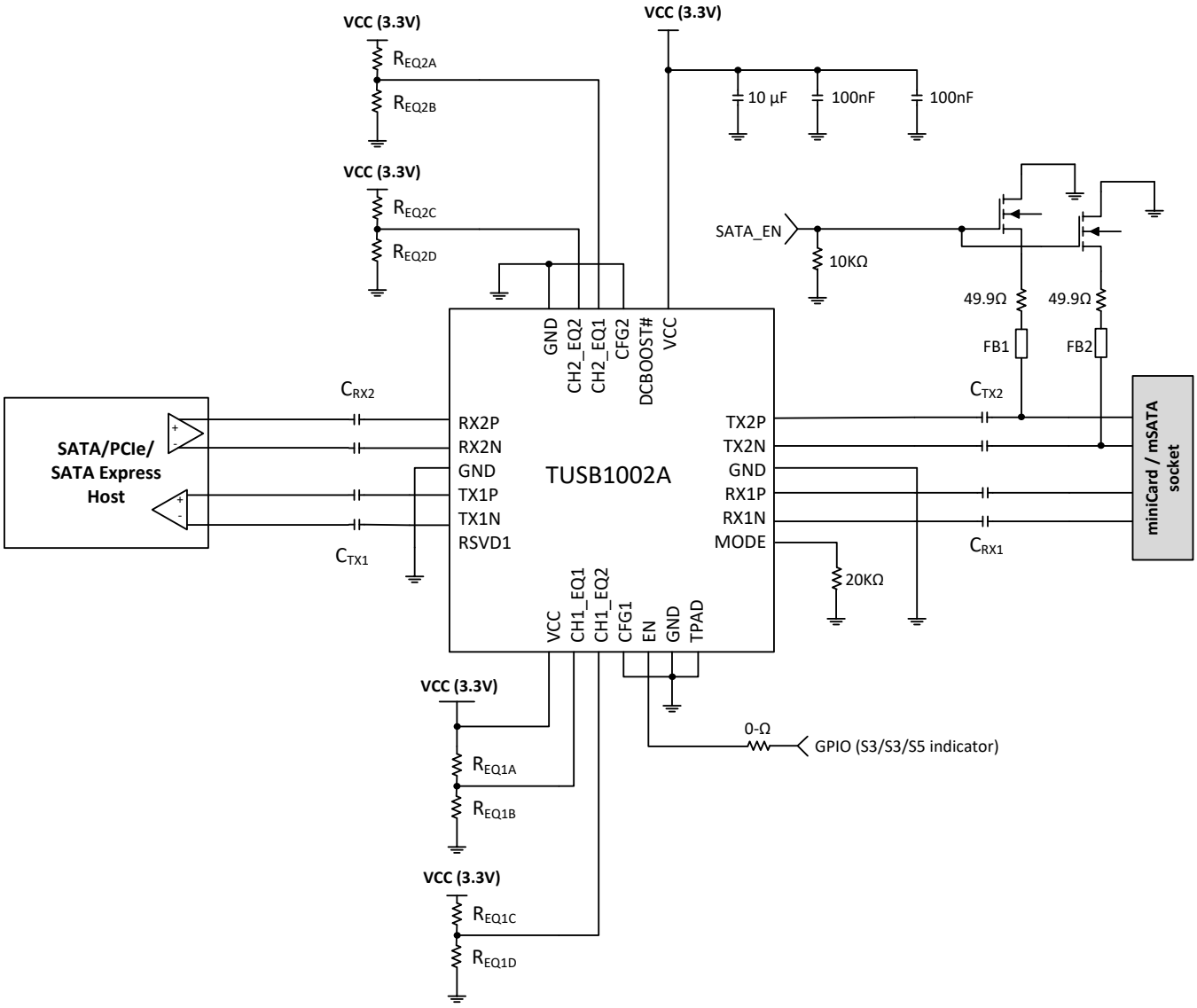


图 22. Example SATA/PCIe/SATA Express Schematic

8.3.3 Application Curves

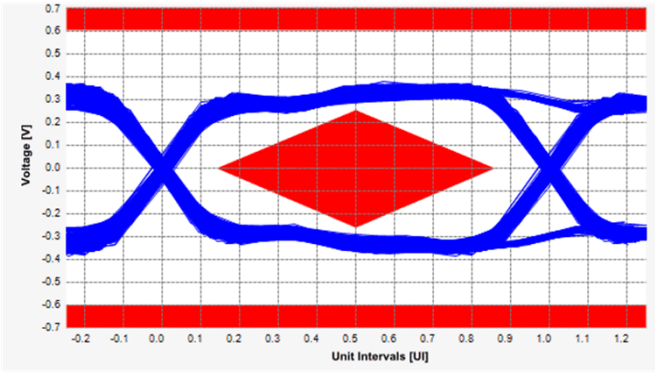


图 23. PCIe Gen1 TX Eye Diagram

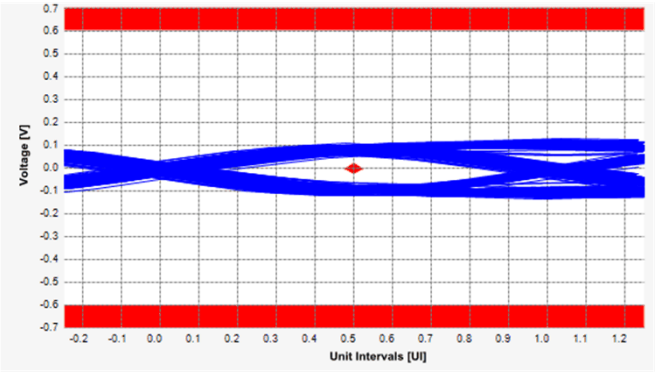


图 24. PCIe Gen 3 TX Eye Diagram

9 Power Supply Recommendations

The TUSB1002A has two V_{CC} supply pins. It is recommended to place a 100 nF de-coupling capacitor near each of the V_{CC} pins. It is also recommended to have at least one bulk capacitor of at least 10 µF on the V_{CC} plane near the TUSB1002A.

10 Layout

10.1 Layout Guidelines

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
- Keep away from other high speed signals.
- In USB3 applications maintaining polarity thru the TUSB1002A is not necessary. Therefore it is recommended to connect polarity in such a way that produces the best routing.
- Intra-pair routing should be kept to within 2 mils.
- Intra-pair length matching should be near the location of mismatch.
- Inter-pair length matching is not necessary.
- Each pair should be separated at least by 3 times the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This minimizes any length mismatch causes by the bends; ad therefore, minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- When using thru-hole USB connectors, it is recommend to route differential pairs on bottom layer in order to minimize the stub created by the thru-hole connector.
- Adding Test points causes impedance discontinuity; and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Example

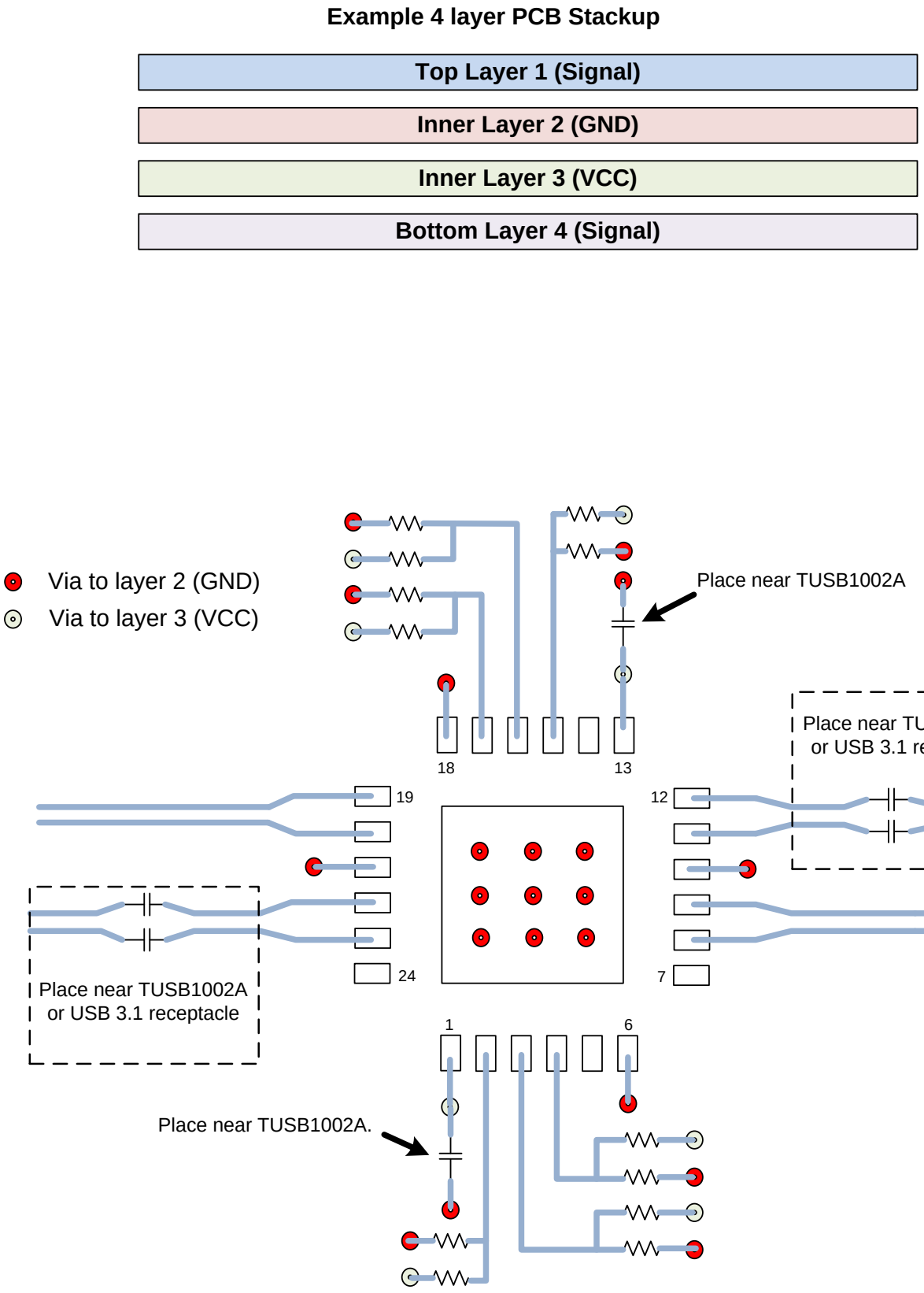


图 25. Example Layout

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1002AIRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TUSB 1002A	Samples
TUSB1002AIRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TUSB 1002A	Samples
TUSB1002ARGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TUSB 1002A	Samples
TUSB1002ARGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TUSB 1002A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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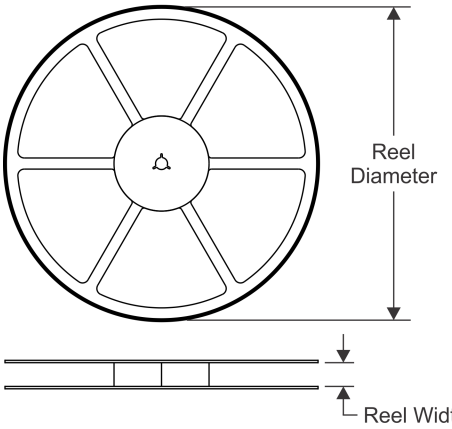
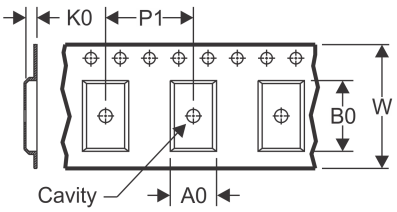
TAPE AND REEL INFORMATION

REEL DIMENSIONS

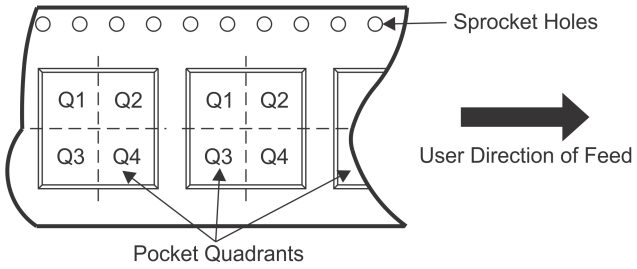


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

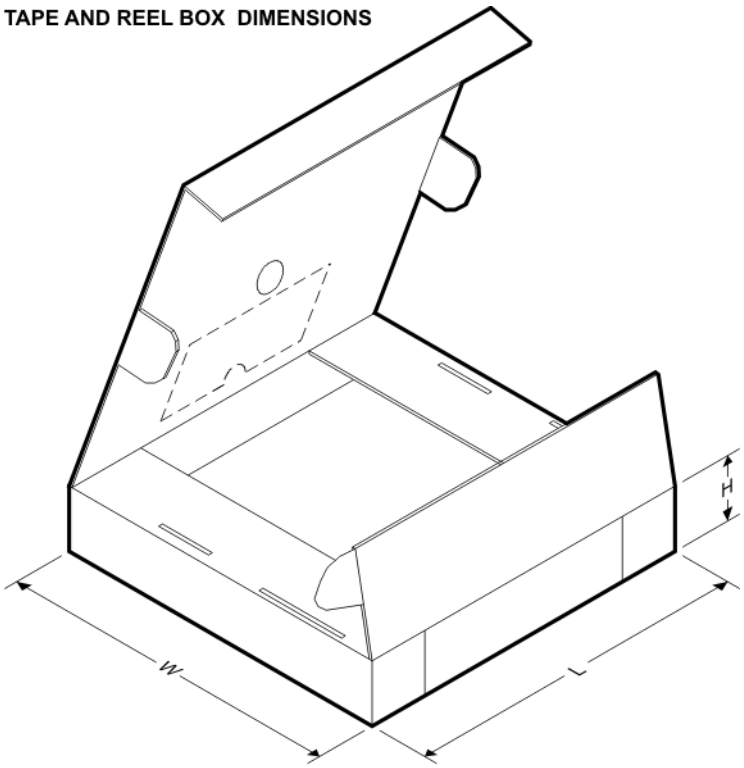
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1002AIRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSB1002AIRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSB1002ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSB1002ARGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



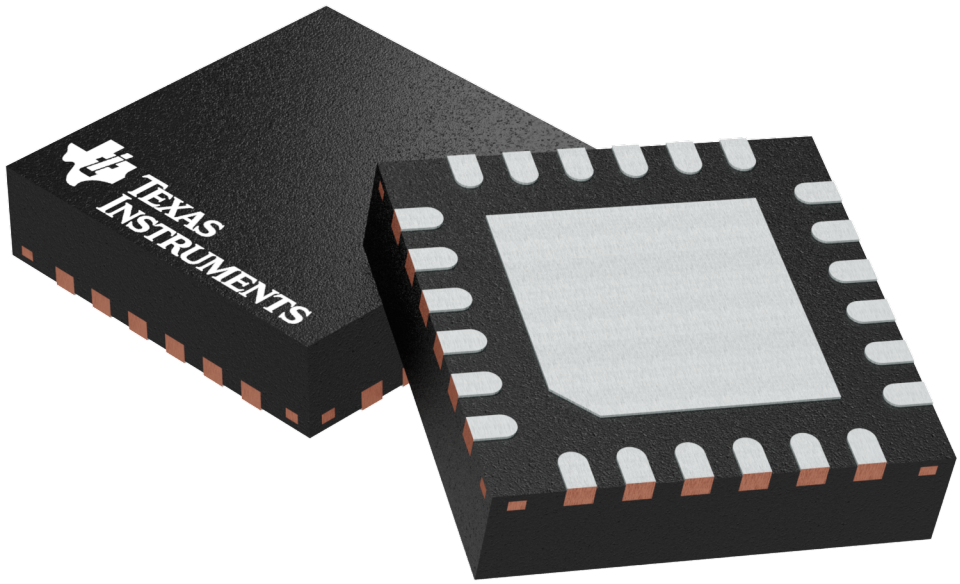
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1002AIRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TUSB1002AIRGET	VQFN	RGE	24	250	210.0	185.0	35.0
TUSB1002ARGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TUSB1002ARGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

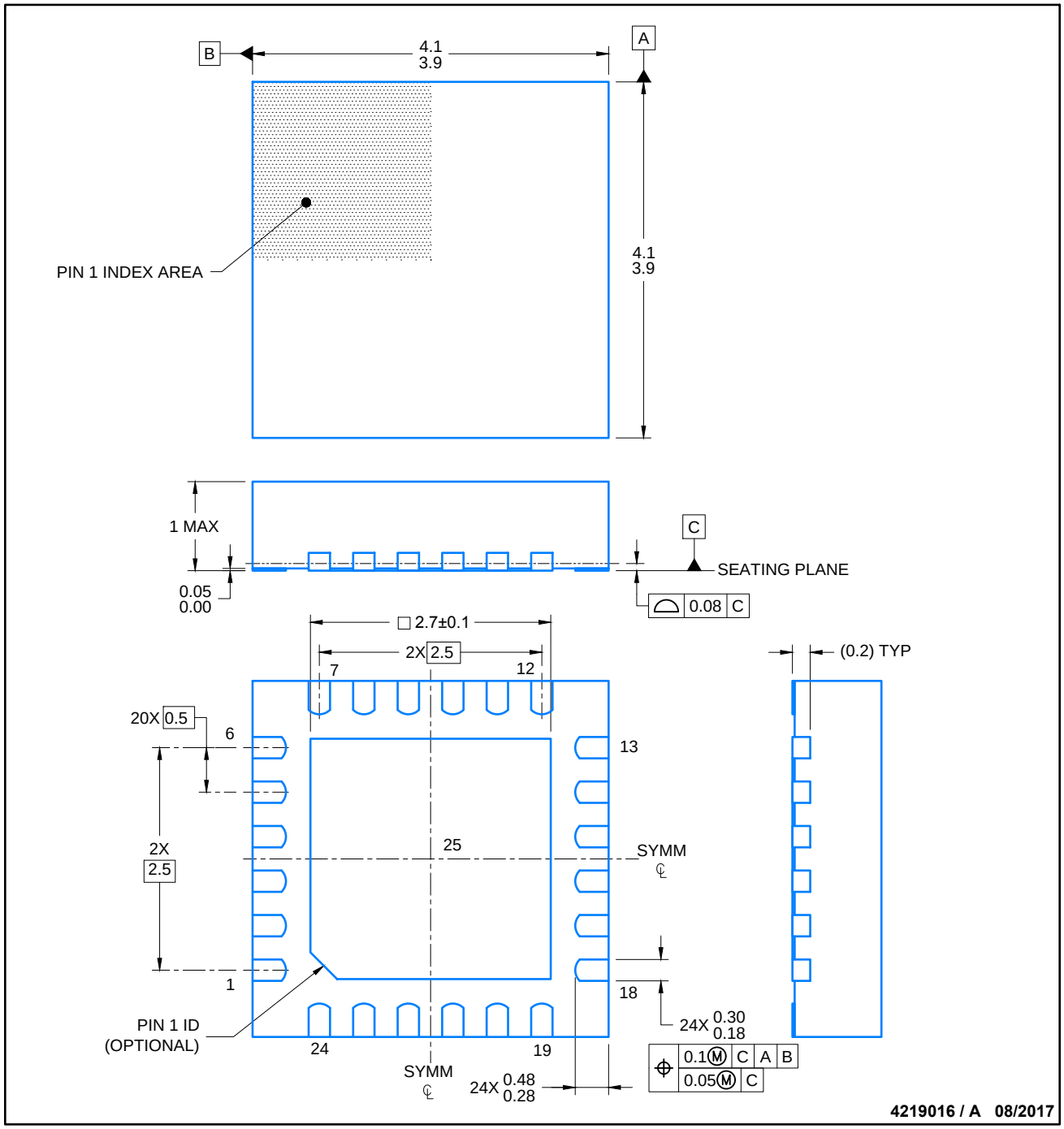
4204104/H

PACKAGE OUTLINE

RGE0024H

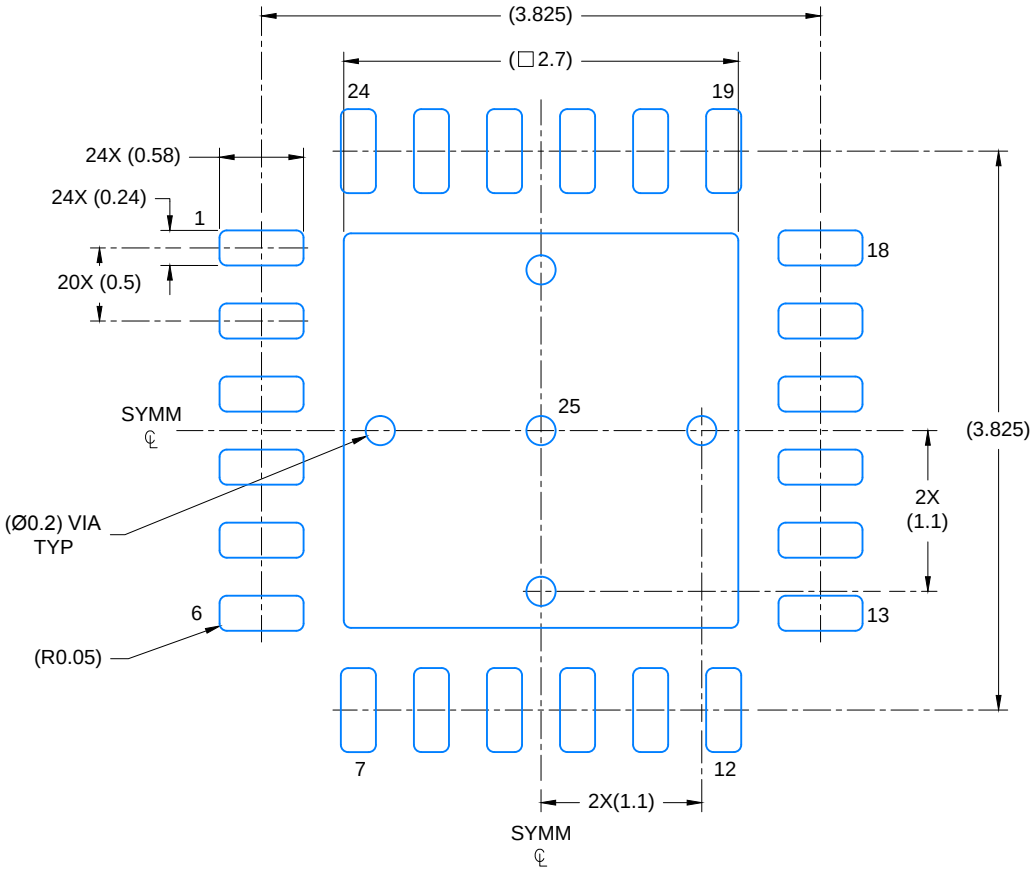
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



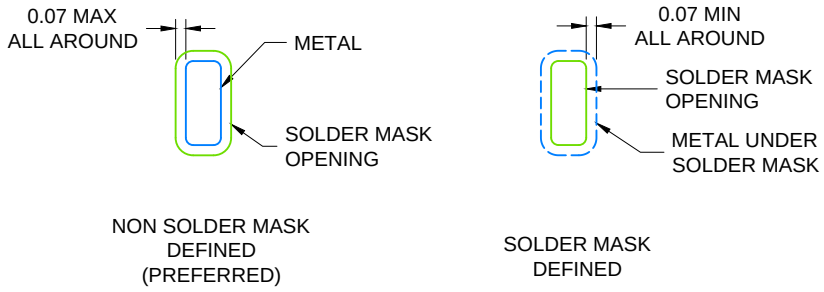
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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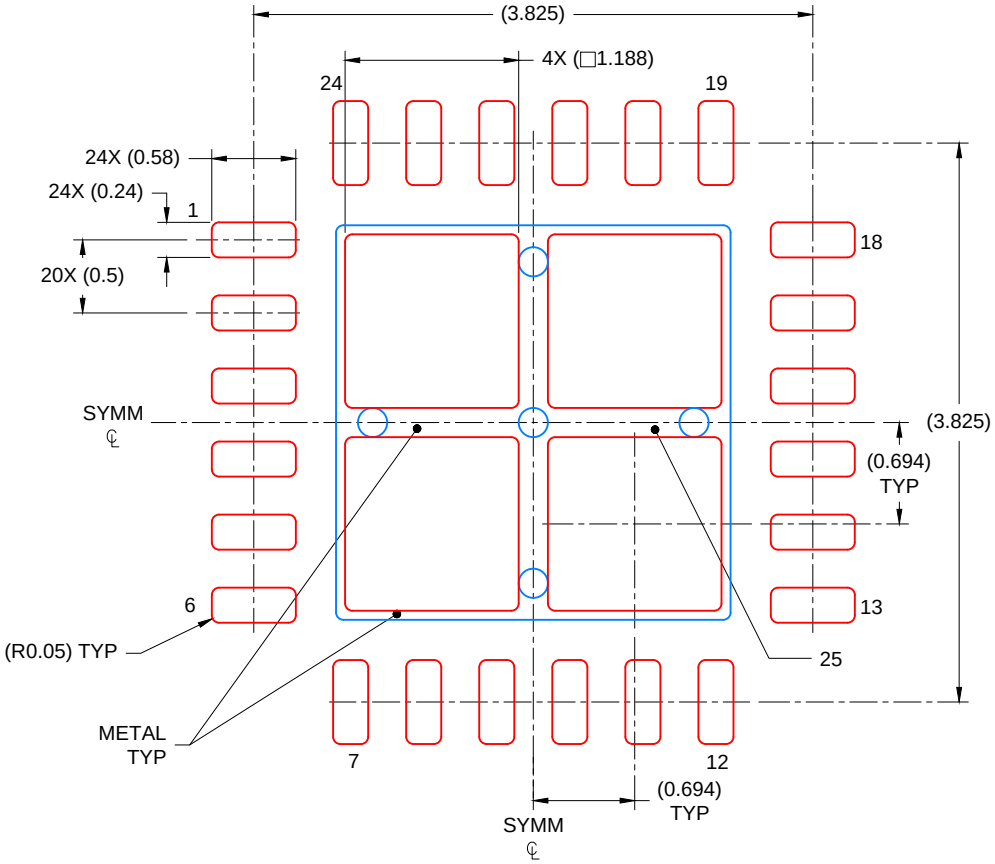
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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