DLPC7540 High Resolution Controller

1 Features

- DLPC7540 controller using DLP471TE, DLP471NE, DLP650TE or DLP651NE digital micromirror device (DMD) supports
  - Up to 4K UHD at 60 Hz
  - Up to 1080p at 240 Hz (2D) and 120 Hz (3D)
- Provides single V-by-One® HS video input port with one, two, four, or eight lanes
  - Up to 600 MHz Pixel clock support
  - Up to 3.0 Gbps input transmission rate
- Two OpenLDI (FPD-Link I) video input ports with 6-lanes (5 data) per port
- Input formats supported
  - RGB, YCbCr and ICtCp
  - 4:4:4, 4:2:2, 4:2:0
- Internal Arm Cortex-R4F processor with FPU
  - 88 configurable GPIOs
  - Programmable PWM generator
  - Programmable capture and delay timers
  - USB 2.0 high-speed OTG controller
  - SPI primary/secondary controllers
  - I^2C primary/secondary controllers
  - UART and interrupt controllers
- Warping engine
  - Improved 1D, 2D and 3D keystone correction
  - Optical distortion correction (radial and lateral color distortion e.g. for short throw)
  - Warping (multi-point manual warp and full warp map access 62x32 points)
  - Blending (manual blending and full bleding map access 63x32 points)
- Additional image processing
  - DynamicBlack
  - TI DLP® BrilliantColor™
  - HDR10 (PQ and HLG) support
  - Frame rate conversion
  - Color coordinate adjustment
  - White color temperature adjustment
  - Programmable degamma
  - Spatial-temporal multiplexing
  - Integrated support for 3-D display
- Splash screen display and capture
- Integrated 2G-bit frame memory eliminates need for external high-speed memory
- External memory support
  - Parallel flash for µP and PWM sequences
  - Secondary flash for Splash Capture, Warping
- System control
  - DMD power and reset driver control
  - DMD horizontal and vertical image flip
- JTAG boundary scan test support
- LED, RGB Laser and Laser Phosphor illuminations

2 Applications

- Enterprise projector
- Laser TV
- Smart projector
- Digital signage

3 Description

The DLPC7540 is a digital display controller for the 4K UHD and 1080p display chipsets, which comprises of DLPC7540 controller, DLP471TE, DLP471NE, DLP650TE or DLP651NE DMDs and DLPA100 Power and Motor driver. This solution targets display systems that require high resolution and high brightness in a small form factor. To ensure reliable operation, the DLPC7540 controller must always be used with the DLP471TE, DLP471NE, DLP650TE or DLP651NE DMDs and the DLPA100 power management integrated circuit in each application.

Device Information(1)(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC7540ZDC	P-HBGA (676)	31.00 mm × 31.00 mm

(1) For all available packages, see the orderable addendum.
(2) Includes embedded heat slug.

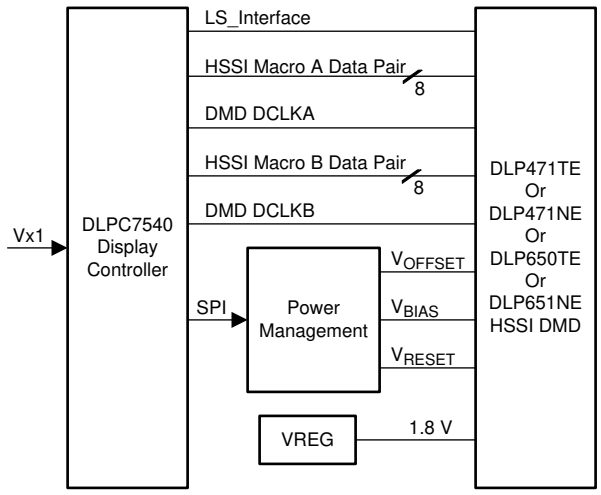

Figure 3-1. Typical Standalone System

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2021	*	Initial Release

5 Pin Configuration and Functions

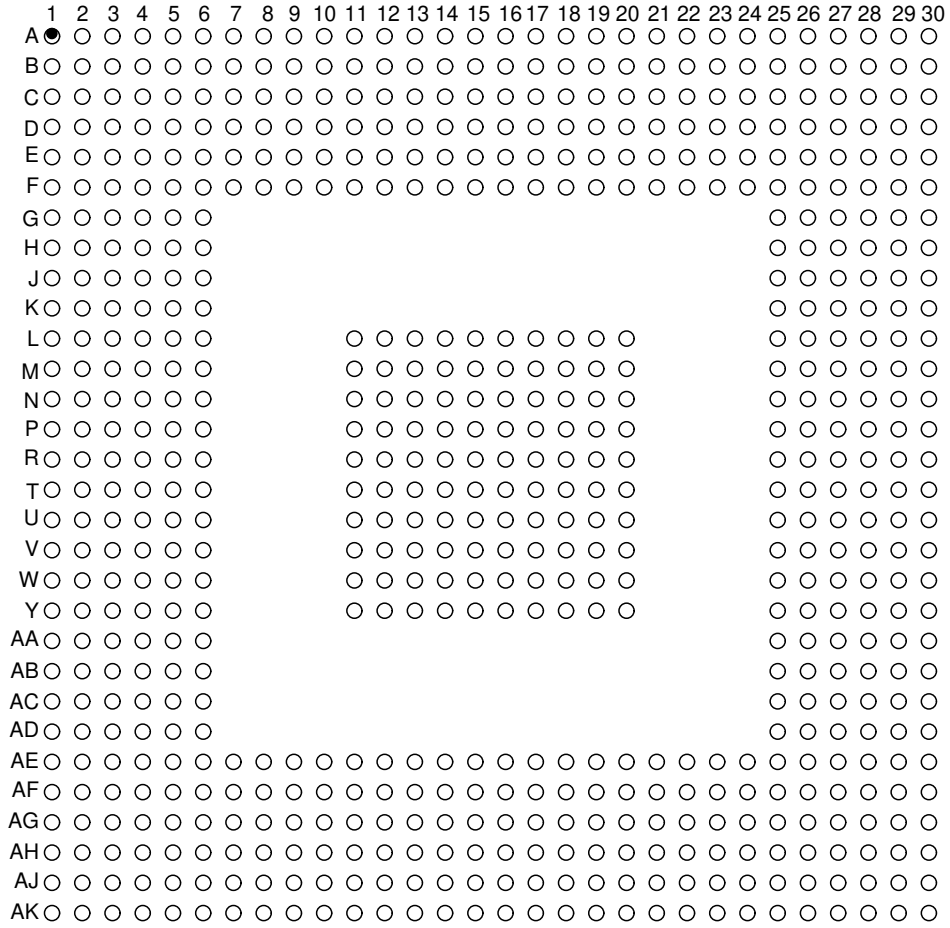


Figure 5-1. ZDC Package 676-Pin PBGA Top View

Table 5-1. Initialization, Board Level Test, and Debug

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
POSENSE	AE27	I_8	Power-On Sense: Signal provided from external voltage monitoring circuit ('0' = All Controller supply voltages not at valid level, '1' = All Controller supply voltages have reached 90% specified minimum voltage) Drive this signal to inactive (low) after the falling edge of PWRGOOD as specified. See Section 6.13 for specific timing requirements as well as the required power up and power down sequence. This pin includes hysteresis
PWRGOOD	AG30	I_8	Power Good: Signal provided from external power supply of voltage monitor A high value indicates all power is within operating voltage specifications and the system is safe to exit its reset state. A transition from high to low indicates that the Controller or DMD supply voltage drops below its rated minimum level. This transition must occur prior to the supply voltage dropping per the timing specified, as this is an early warning of an imminent power loss condition. This warning is required to enhance long term DMD reliability. When PWRGOOD goes low for the specified minimum time, a DMD park and full Controller reset are performed, protecting the DMD. Note that both Controller and DMD supply voltages must be within operating voltage levels to successfully execute the DMD park. The minimum PWRGOOD de-assertion time is used to protect the system input from glitches. When PWRGOOD is low, the Controller is held in its reset state. See Section 6.13 for specific timing requirements as well as the required power up and power down sequence. This pin includes hysteresis

Table 5-1. Initialization, Board Level Test, and Debug (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
EXT_ARSTZ	AF29	O_8	External Reset: General purpose reset output ('0' = Reset, '1' = Normal Operation) This output is asserted low immediately upon POSENSE being asserted low, and remains low while POSENSE remains low. This signal remains low after POSENSE is set high, until released by software. This signal is also asserted low approximately 5 µs after the detection of PWRGOOD going low, or any internally generated reset. In all cases, this signal remains active low for a minimum of 2ms. Note: this signal can also be independently driven via software register.
MTR_ARSTZ	AF27	O_8	Color Wheel Motor Controller Reset: Color wheel motor controller reset output ('0' = Reset, '1' = Normal Operation) This output is asserted low immediately upon POSENSE being asserted low, and remains low while POSENSE remains low. This signal remains low after POSENSE is set high, until released by software. This signal is also asserted low approximately 5 µs after the detection of PWRGOOD going low, or any internally generated reset. In all cases, this signal remains active low for a minimum of 2ms. Note: this signal can also be independently driven via software register.
TCK	AK19	I_8	JTAG, ARM-ICE, and CPU MBIST Serial Data Clock. This signal is shared between JTAG, ARM-ICE (TI test only), and CPU MBIST (Manufacturing test only) operation Includes a weak internal pulldown.
TMS1	AH20	I_8	JTAG Test Mode Select Includes weak internal pullup.
TMS2	AJ20	I_8	ARM-ICE Test Mode Select For normal operation, this pin must be left open or unconnected. Includes a weak internal pullup.
TMS3	AK20	I_8	CPU MBIST Test Mode Select For normal operation this pin must be left open or unconnected. Includes a weak internal pullup.
TRSTZ	AG21	I_8	JTAG, ARM-ICE, and CPU MBIST Reset. This signal is shared between JTAG, ARM-ICE (TI test only), and CPU MBIST (Manufacturing test only) operation. *For normal operation, this pin must be pulled to ground through an external resistor with value 8 kΩ or less. Failure to pull this pin low during normal operation causes start-up and initialization problems.* For JTAG Boundary Scan, ARM-ICE Debug operation, or CPU MBIST, this pin must be pulled-up or left disconnected. Includes a weak internal pullup and Hysteresis.
TDI	AG20	I_8	JTAG, ARM-ICE, and CPU MBIST: Serial Data In Includes weak internal pullup.
TDO1	AG19	O_8	JTAG Serial Data Out.
TDO2	AH19	O_8	ARM-ICE Serial Data Out For normal operation, this pin must be left open or unconnected.
TDO3	AJ19	O_8	CPU MBIST Serial Data Out For normal operation, this pin must be left open or unconnected.
ETM_TRACE CLK	C30	O_8	TI internal use. Must be left unconnected. (Clock for Trace debug)
ETM_TRACE CTL	D30	O_8	TI internal use. Must be left unconnected. (Control for Trace Debug)
ICTSEN	K26	I_8	IC Tristate Enable (Active high) Asserting this signal transitions all outputs into tristate (except for the JTAG interface). Includes a weak internal pulldown, however, an external pulldown is recommended for added protection. Also includes hysteresis.
ICTSE	M26	I_8	TI internal use. Includes a weak internal pulldown, however, an external pulldown is recommended for added protection. Also includes hysteresis.
TSTPT_0	E29	B_8	Test pin 0 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10 kΩ. Tri-stated while PWRGOOD is asserted low. It may be driven as an output for debug use as described in *Section 7.3.8*.

Table 5-1. Initialization, Board Level Test, and Debug (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
TSTPT_1	E30	B_8	Test pin 1 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10 kΩ. Tri-stated while PWRGOOD is asserted low. It may be driven as an output for debug use as described in *Section 7.3.8*.
TSTPT_2	F26	B_8	Test pin 2 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10 kΩ. Tri-stated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in *Section 7.3.8*.
TSTPT_3	F27	B_8	Test pin 3 This pin requires an external pulldown or pullup resistor (depending on the desired debug output as noted below) with a value of ≤ 10 kΩ. Tri-stated while PWRGOOD is asserted low. It may be driven as an output for debug use as described in *Section 7.3.8*.
TSTPT_4	F28	B_8	Test pin 4 This pin requires an external pulldown resistor (≤ 10 kΩ). Tri-stated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in *Section 7.3.8*.
TSTPT_5	F29	B_8	Test pin 5 This pin requires an external pulldown resistor (≤ 10 kΩ). Tri-stated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in *Section 7.3.8*.
TSTPT_6	G26	B_8	Test pin 6 This pin requires an external pulldown resistor (≤ 10 kΩ). Tri-stated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in *Section 7.3.8*.
TSTPT_7	G28	B_8	Test pin 7 This pin requires an external pulldown resistor (≤ 10 kΩ). Tri-stated while PWRGOOD is asserted low. It can be driven as an output for debug use as described in *Section 7.3.8*.
HWTEST_EN	L26	I_8	Manufacturing test enable signal. This signal must be connected directly to ground on the PCB for normal operation. Includes weak internal pulldown and hysteresis.

(1) See Table 5-13 for more information on I/O definitions.

Table 5-2. Analog Front End (Not Supported in DLPC7540)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
AFE_ARSTZ	K2	O_8	Reserved.
AFE_CLK	K3	O_8	Reserved.
AFE_IRQ	K4	I_8	Reserved.
ALF_VSYNC	K5	I_8	Reserved.
ALF_HSYNC	J1	I_8	Reserved.
ALF_CSYNC	J2	I_8	Reserved.

(1) See Table 5-13 for more information on I/O definitions.

Table 5-3. V-by-One Interface Input Data and Control

PIN		I/O (1)	DESCRIPTION (2) (3)
NAME	NO.		
VX1_DATA0_P VX1_DATA0_N VX1_DATA1_P VX1_DATA1_N VX1_DATA2_P VX1_DATA2_N VX1_DATA3_P VX1_DATA3_N VX1_DATA4_P VX1_DATA4_N VX1_DATA5_P VX1_DATA5_N VX1_DATA6_P VX1_DATA6_N VX1_DATA7_P VX1_DATA7_N	C18 D18 A19 B19 C20 D20 A21 B21 C22 D22 A23 B23 C24 D24 A25 B25	I_1	V-by-One interface data lanes.
VX1_HTPDN	E17	O_4	V-by-One interface hot plug detect (controller receiver pulls this signal low to indicate its presence to the transmitter) This signal is open drain at the controller output. A pullup resistor is required at the transmitter.
VX1_LOCKN	E19	O_4	V-by-One interface clock detect lock (controller receiver pulls this signal low to indicate clock extraction lock to the transmitter) This signal is open drain at the controller output. A pullup resistor is required at the transmitter.
VX1_CM_CKREF0 VX1_CM_CKREF1 VX1_CM_CKREF2 VX1_CM_CKREF3	E20 E21 E23 E24	I_1	V-by-One reserved: Tie these reserved pins to ground.
VX1_CM_AMOUT0 VX1_CM_AMOUT1 VX1_CM_AMOUT2 VX1_CM_AMOUT3	F19 F21 F22 F23	O_1	V-by-One reserved: These pins are reserved and must remain unconnected

(1) See Table 5-13 for more information on I/O definitions.
(2) The system supports 1 lane, 2 lane, 4 lane, or 8 lane operation, based on the bandwidth requirement of the input source. The inputs for any un-used data lanes must be left open.
(3) The V-by-One port supports limited lane remapping to help optimize board layout. The details are described in Section 7.3.4.

Table 5-4. OpenLDI (FPD-Link I) Ports Input Data and Control

PIN		I/O (1)	DESCRIPTION(2) (3)
NAME	NO.		
FPDA_CLK_P FPDA_CLK_N	H3 H4	I_5	FPD-Link Port A Clock Lane
FPDA_DATAA_P FPDA_DATAA_N FPDA_DATAB_P FPDA_DATAB_N FPDA_DATAC_P FPDA_DATAC_N FPDA_DATAD_P FPDA_DATAD_N FPDA_DATAE_P FPDA_DATAE_N	G1 G2 F3 F4 E1 E2 D3 D4 C1 C2	I_5	FPD-Link Port A Data Lanes
FPDB_CLK_P FPDB_CLK_N	A4 B4	I_5	FPD-Link Port B Clock Lane

Table 5-4. OpenLDI (FPD-Link I) Ports Input Data and Control (continued)

PIN		I/O (1)	DESCRIPTION(2) (3)
NAME	NO.		
FPDB_DATAA_P FPDB_DATAA_N FPDB_DATAB_P FPDB_DATAB_N FPDB_DATAC_P FPDB_DATAC_N FPDB_DATAD_P FPDB_DATAD_N FPDB_DATAE_P FPDB_DATAE_N	C5 D5 A6 B6 C7 D7 A8 B8 C9 D9	I_5	FPD-Link Port B Data Lanes
FPDC_CLK_P FPDC_CLK_N	A10 B10	I_5	FPD-Link Port C - Reserved for Parallel Port use only.
FPDC_DATAA_P FPDC_DATAA_N FPDC_DATAB_P FPDC_DATAB_N FPDC_DATAC_P FPDC_DATAC_N FPDC_DATAD_P FPDC_DATAD_N FPDC_DATAE_P FPDC_DATAE_N	C11 D11 A12 B12 C13 D13 A14 B14 C15 D15	I_5	FPD-Link Port C Data Lanes - Reserved for Parallel Port use only.

(1) See Table 5-13 for more information on I/O definitions.
(2) Throughout this document the terms FPD and FPD-Link refer to OpenLDI (FPD-Link I).
(3) Tie the inputs for any un-used port(s) to ground, or pull to ground through an external resistor.

Table 5-5. Parallel Port Input Data and Control (Not Supported in DLPC7540)

PIN		I/O (1)	DESCRIPTION PARALLEL RGB MODE
NAME	NO.		
PCLK *(FPDB_DATAB_N)*	B6	I_6	Reserved.
VSYNC *(FPDA_DATAE_P)*	C1	I_6	Reserved.
HSYNC *(FPDA_DATAE_N)*	C2	I_6	Reserved.
DATEN *(FPDB_DATAE_N)*	D9	I_6	Reserved. (2)
FIELD *(FPDC_DATAE_P)*	C15	I_6	Reserved.
3D_REF *(FPDC_DATAE_N)*	D15	I_6	Reserved.
PDATA_A0 *(FPDA_CLK_P)* PDATA_A1 *(FPDA_CLK_N)* PDATA_A2 *(FPDA_DATAA_P)* PDATA_A3 *(FPDA_DATAA_N)* PDATA_A4 *(FPDA_DATAB_P)* PDATA_A5 *(FPDA_DATAB_N)* PDATA_A6 *(FPDA_DATAC_P)* PDATA_A7 *(FPDA_DATAC_N)* PDATA_A8 *(FPDA_DATAD_P)* PDATA_A9 *(FPDA_DATAD_N)*	H3 H4 G1 G2 F3 F4 E1 E2 D3 D4	I_6	Reserved.
PDATA_B0 *(FPDB_CLK_P)* PDATA_B1 *(FPDB_CLK_N)* PDATA_B2 *(FPDB_DATAA_P)* PDATA_B3 *(FPDB_DATAA_N)* PDATA_B4 *(FPDB_DATAB_P)* PDATA_B5 *(FPDB_DATAC_P)* PDATA_B6 *(FPDB_DATAC_N)* PDATA_B7 *(FPDB_DATAD_P)* PDATA_B8 *(FPDB_DATAD_N)* PDATA_B9 *(FPDB_DATAE_P)*	A4 B4 C5 D5 A6 C7 D7 A8 B8 C9	I_6	Reserved.

Table 5-5. Parallel Port Input Data and Control (Not Supported in DLPC7540) (continued)

PIN		I/O (1)	DESCRIPTION PARALLEL RGB MODE
NAME	NO.		
PDATA_C0 *(FPDC_CLK_P)* PDATA_C1 *(FPDC_CLK_N)* PDATA_C2 *(FPDC_DATAA_P)* PDATA_C3 *(FPDC_DATAA_N)* PDATA_C4 *(FPDC_DATAB_P)* PDATA_C5 *(FPDC_DATAB_N)* PDATA_C6 *(FPDC_DATAC_P)* PDATA_C7 *(FPDC_DATAC_N)* PDATA_C8 *(FPDC_DATAD_P)* PDATA_C9 *(FPDC_DATAD_N)*	A10 B10 C11 D11 A12 B12 C13 D13 A14 B14	I_6	Reserved.

(1) See Table 5-13 for more information on I/O definitions.
(2) If the DATEN is not actively driven, then it must be pulled up to 3.3V with a weak pull up resistor (50k Ohm max).

Table 5-6. DMD Reset and Low Speed Interfaces

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
DMD_LS0_CLK_P DMD_LS0_CLK_N	AH17 AG17	O_2	DMD low speed differential interface, Port 0 Clock
DMD_LS0_WDATA_P DMD_LS0_WDATA_N	AK16 AJ16	O_2	DMD low speed differential interface, Port 0 Write Data
DMD_LS1_CLK_P DMD_LS1_CLK_N	AH15 AG15	O_2	DMD low speed differential interface, Port 1 Clock (2)
DMD_LS1_WDATA_P DMD_LS1_WDATA_N	AK14 AJ14	O_2	DMD low speed differential interface, Port 1Write Data (2)
DMD_LS0_RDATA	AH13	I_3	DMD, low speed single ended serial interface, Port 0 Read Data (3)
DMD_LS1_RDATA	AG13	I_3	DMD, low speed single ended serial interface, Port 1 Read Data (2) (3). If this port not used, this signal requires an external pullup or pulldown to keep this input from floating.
DMD_DEN_ARSTZ	AK12	O_3	DMD driver enable signal / Active Low Asynchronous Reset ('1' = Enabled, '0' = Reset) This signal is driven low after the DMD is parked and before power is removed from the DMD. *If the 1.8-V power to the DLPC7540 is independent of the 1.8-V power to the DMD, then an external pulldown resistor must be used to hold the signal low in the event the DLPC7540 power is inactive while DMD power is applied.*

(1) See Table 5-13 for more information on I/O definitions.
(2) DMD LS1 port is reserved for single controller, two DMD applications.
(3) All control interface reads make use of the single ended low speed signals. **The read data is clocked by the low speed differential write clock.**

Table 5-7. DMD HSSI (High Speed Serial Interface)

PIN (1)		I/O (2)	DESCRIPTION
NAME	NO.		
DMD_HSSI0_CLK_P DMD_HSSI0_CLK_N	AK25 AJ25	O_7	DMD high speed serial interface, Port 0 Clock Lane.

Table 5-7. DMD HSSI (High Speed Serial Interface) (continued)

PIN (1)		I/O (2)	DESCRIPTION
NAME	NO.		
DMD_HSSI0_D0_P DMD_HSSI0_D0_N DMD_HSSI0_D1_P DMD_HSSI0_D1_N DMD_HSSI0_D2_P DMD_HSSI0_D2_N DMD_HSSI0_D3_P DMD_HSSI0_D3_N DMD_HSSI0_D4_P DMD_HSSI0_D4_N DMD_HSSI0_D5_P DMD_HSSI0_D5_N DMD_HSSI0_D6_P DMD_HSSI0_D6_N DMD_HSSI0_D7_P DMD_HSSI0_D7_N	AK29 AJ29 AH28 AG28 AK27 AJ27 AH26 AG26 AH24 AG24 AK23 AJ23 AH22 AG22 AK21 AJ21	O_7	DMD high speed serial interface, Port 0 Data Lanes.
DMD_HSSI1_CLK_P DMD_HSSI1_CLK_N	AH7 AG7	O_7	DMD high speed serial interface, Port 1 Clock Lane.
DMD_HSSI1_D0_P DMD_HSSI1_D0_N DMD_HSSI1_D1_P DMD_HSSI1_D1_N DMD_HSSI1_D2_P DMD_HSSI1_D2_N DMD_HSSI1_D3_P DMD_HSSI1_D3_N DMD_HSSI1_D4_P DMD_HSSI1_D4_N DMD_HSSI1_D5_P DMD_HSSI1_D5_N DMD_HSSI1_D6_P DMD_HSSI1_D6_N DMD_HSSI1_D7_P DMD_HSSI1_D7_N	AH11 AG11 AK10 AJ10 AH9 AG9 AK8 AJ8 AK6 AJ6 AH5 AG5 AK4 AJ4 AK2 AJ2	O_7	DMD high speed serial interface, Port 1 Data Lanes.
HSSI_ATETEST	AJ12	O_7	Manufacturing Test use only - Must be left open (i.e. unconnected)

(1) A number of pin remapping options are available for the HSSI high speed channels to aid with optimizing board signal routing. See Section 7.3.5 for information on these pin remapping options.
(2) See Table 5-13 for more information on I/O definitions.

Table 5-8. Program Memory (FLASH) Interface

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
PM_CSZ_0	T27	O_8	Chip select: Boot FLASH Only (Boot FLASH must use this chip select)
PM_CSZ_1	T28	O_8	Chip select: Additional Peripheral Device
PM_CSZ_2	T29	O_8	Chip select: Additional Peripheral Device
PM_ADDR_0	T30	O_8	Address bit (LSB)
PM_ADDR_1	U26	O_8	Address bit
PM_ADDR_2	U27	O_8	Address bit
PM_ADDR_3	U29	O_8	Address bit
PM_ADDR_4	U30	O_8	Address bit
PM_ADDR_5	V29	O_8	Address bit
PM_ADDR_6	V28	O_8	Address bit
PM_ADDR_7	V27	O_8	Address bit
PM_ADDR_8	V26	O_8	Address bit
PM_ADDR_9	W30	O_8	Address bit

Table 5-8. Program Memory (FLASH) Interface (continued)

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
PM_ADDR_10	W29	O_8	Address bit
PM_ADDR_11	W28	O_8	Address bit
PM_ADDR_12	W26	O_8	Address bit
PM_ADDR_13	Y30	O_8	Address bit
PM_ADDR_14	Y29	O_8	Address bit
PM_ADDR_15	Y28	O_8	Address bit
PM_ADDR_16	Y27	O_8	Address bit
PM_ADDR_17	Y26	O_8	Address bit
PM_ADDR_18	AA30	O_8	Address bit
PM_ADDR_19	AA29	O_8	Address bit
PM_ADDR_20	AA27	O_8	Address bit
PM_ADDR_21	AA26	O_8	Address bit
PM_ADDR_22	AB29	O_8	Address bit
PM_ADDR_23 *(GPIO_47)*	AB28	B_8	Address bit (MSB) [2]
PM_WEZ	R28	O_8	Write Enable (active low)
PM_OEZ	R29	O_8	Output Enable (active low)
PM_BLSZ_0	R30	O_8	Lower Byte (7:0) Enable (active low) - only applicable to devices using PM_CSZ_1 or PM_CSZ_2
PM_BLSZ_1	T26	O_8	Upper Byte (15:8) Enable (active low) - only applicable to devices using PM_CSZ_1 or PM_CSZ_2
PM_Data_0	L29	B_8	Data bit
PM_Data_1	L30	B_8	Data bit
PM_Data_2	L28	B_8	Data bit
PM_Data_3	M27	B_8	Data bit
PM_Data_4	M28	B_8	Data bit
PM_Data_5	M29	B_8	Data bit
PM_Data_6	M30	B_8	Data bit
PM_Data_7	N26	B_8	Data bit
PM_Data_8	N27	B_8	Data bit
PM_Data_9	N29	B_8	Data bit
PM_Data_10	N30	B_8	Data bit
PM_Data_11	P26	B_8	Data bit
PM_Data_12	P27	B_8	Data bit
PM_Data_13	P28	B_8	Data bit
PM_Data_14	P29	B_8	Data bit
PM_Data_15	R26	B_8	Data bit

(1) See Table 5-13 for more information on I/O definitions.
(2) The Program Memory address bus can be extended by one bit to 24 bits by making use of GPIO_47. Add an external pulldown resistor when this GPIO is configured for this purpose.

Table 5-9. Peripheral Interfaces

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
IIC0_SCL	E27	B_{13}	I^2C Port 0 (Master-Slave), Typically slave for Host Command and Control to Controller, SCL (bidirectional, open-drain): An external pullup is required. The minimum acceptable value for this pullup is 1KΩ .

Table 5-9. Peripheral Interfaces (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
IIC0_SDA	D29	B_{13}	I^2C Port 0 (Master-Slave), Typically slave for Host Command and Control to Controller, SDA. (bidirectional, open-drain): An external pullup is required. The minimum acceptable value for this pullup is 1KΩ
SSP0_TXD	AD27	O_8	SSP/SPI Port 0 Data Out (Master): Transmit data pin
SSP0_RXD	AD29	I_8	SSP/SPI Port 0 Data In (Master): Receive data pin
SSP0_CLK	AD28	O_8	SSP/SPI Port 0 Clock (Master): Clock pin
SSP0_CSZ_2	AC28	O_8	SPI Port 0 chip select 2 (Master): Chip select (Active Low) An external pullup resistor (≤ 10 kΩ) is suggested to avoid a floating chip select input to the external device
SSP0_CSZ_1	AC26	O_8	SPI Port 0 chip select 1 (Master): Chip select (Active Low) An external pullup resistor (≤ 10 kΩ) is suggested to avoid a floating chip select input to the external device
SSP0_CSZ_0	AB27	O_8	SPI Port 0 chip select 0 (Master): Chip select (Active Low) An external pullup resistor (≤ 10 kΩ) is suggested to avoid a floating chip select input to the external device
UART0_TXD	P4	O_8	UART Port 0 (Slave): Serial Data Transmit This UART port is reserved for TI debug. An external pullup resistor (≤ 10 kΩ) is required
UART0_RXD	P5	I_8	UART Port 0 (Slave): Serial Data Receive This UART port is reserved for TI debug. An external pullup resistor (≤ 10 kΩ) is required
UART0_RTSZ	N2	O_8	UART Port 0 (Slave): Ready To Send (Hardware flow control signal (Active Low)) This UART port is reserved for TI debug. An external pullup resistor (≤ 10 kΩ) is required
UART0_CTSZ	N3	I_8	UART Port 0 (Slave): Clear to Send (Hardware flow control signal (Active Low)) This UART port is reserved for TI debug. An external pullup resistor (≤ 10 kΩ) is required
USB_DAT_P USB_DAT_N	B27 A27	B_{11}	USB OTG Data Lane (Master-Stave)
USB_VBUS	D26	B_{11}	USB OTG 5V Power Supply Detection (Master-Slave)
USB_ID	C27	I_{Other}	USB OTG Mini Receptacle Identification (Master-Slave)
USB_TXRTUNE	C26	B_{GND}	USB OTG Reference Resistor An external reference resistor must be connected as shown in Section 10.1.7
USB_XI	A29	I_{GND}	USB OTG External Oscillator XI - Not used (clock provided internally) For normal operation this pin must be connected to GND.
USB_XO	B29	B_{GND}	USB OTG External Oscillator XO - Not used (clock provided internally) For normal operation this pin must be left open (unconnected).
USB_ANALOGTEST	C28	B_{Other}	USB OTG Manufacturing Test This pin must be left open (unconnected)
PMD_INTZ	AD26	I_8	Interrupt from DLPA100 (Active Low) This signal requires an external pullup. It also has hysteresis
CW_PWM	AE30	O_8	Color Wheel Control PWM
CW_INDEX	AE29	I_8	Color Wheel Index This pin has hysteresis

(1) See Table 5-13 for more information on I/O definitions.

Table 5-10. GPIO Peripheral Interface

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_87	K1	B_8	General purpose I/O 87: Options: 1. Alt 0: Reserved 2. Alt 1: DAO_CLKIN (I) 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_86	L5	B_8	General purpose I/O 86: Options: 1. Alt 0: Reserved 2. Alt 1: DAO_DI_1 (I) 3. Optional GPIO
GPIO_85	L4	B_8	General purpose I/O 85: Options: 1. Alt 0: Reserved 2. Alt 1: DAO_DI_0 (I) 3. Optional GPIO
GPIO_84	L3	B_8	General purpose I/O 84: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_CLKIN_2 (I) 3. Optional GPIO
GPIO_83	L2	B_8	General purpose I/O 83: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_DI_2 (I) 3. Optional GPIO
GPIO_82	M5	B_8	General purpose I/O 82: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_CLKIN_1 (I) 3. Optional GPIO
GPIO_81	M4	B_8	General purpose I/O 81: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_DI_1 (I) 3. Optional GPIO
GPIO_80	M2	B_8	General purpose I/O 80: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_CLKIN_0 (I) 3. Optional GPIO
GPIO_79	M1	B_8	General purpose I/O 79: Options: 1. Alt 0: Reserved 2. Alt 1: HBT_DI_0 (I) 3. Optional GPIO
GPIO_78	N5	B_8	General purpose I/O 78: Options: 1. Alt 0: Reserved 2. Alt 1: SEQ_SYNC (B/ OpenDrain) 3. Optional GPIO
GPIO_77	N4	B_8	General purpose I/O 77: Options: 1. Alt 0: Reserved 2. Alt 1: EFSYNC (O)/ DASYNC (I) 3. Optional GPIO
GPIO_76	AD5	B_8	General purpose I/O 76: Options: 1. Alt 0: AWC1_DACD_PWMB_1 (O) 2. Alt 1: N/A 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_75	AC1	B_8	General purpose I/O 75: Options: 1. Alt 0: AWC1_DACS_PWMA_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_74	AC2	B_8	General purpose I/O 74: Options: 1. Alt 0: AWC1_DACD_PWMB_0 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_73	AC4	B_8	General purpose I/O 73: Options: 1. Alt 0: AWC1_DACS_PWMA_0 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_72	AC5	B_8	General purpose I/O 72: Options: 1. Alt 0: AWC1_DACCLK_0_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_71	AD1	B_8	General purpose I/O 71: Options: 1. Alt 0: AWC1_OUT_ENZ (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_70	AD2	B_8	General purpose I/O 70: Options: 1. Alt 0: AWC0_DACD_PWMB_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_69	AD3	B_8	General purpose I/O 69: Options: 1. Alt 0: AWC0_DACS_PWMA_1 (O) 2. Alt 1: MEMAUX_1 (O) (#2) 3. Optional GPIO
GPIO_68	AD4	B_8	General purpose I/O 68: Options: 1. Alt 0: AWC0_DACD_PWMB_0 (O) 2. Alt 1: IIC2_SDA (B) (#3) 3. Optional GPIO
GPIO_67	AF4	B_8	General purpose I/O 67: Options: 1. Alt 0: AWC0_DACS_PWMA_0 (O) 2. Alt 1: IIC2_SCL (B) (#3) 3. Optional GPIO
GPIO_66	AE2	B_8	General purpose I/O 66: Options: 1. Alt 0: AWC0_DACCLK_0_1 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_65	AE3	B_8	General purpose I/O 65: Options: 1. Alt 0: AWC0_OUT_ENZ (O) 2. Alt 1: N/A 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_64	AE4	B_8	General purpose I/O 64: Options: 1. Alt 0: OCLKB (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_63	AG2	B_8	General purpose I/O 63: Options: 1. Alt 0: PWM_OUT_UVLED (O) 2. Alt 1: OCLKD (O) (#2) 3. Optional GPIO
GPIO_62	AG3	B_8	General purpose I/O 62: Options: 1. Alt 0: PWM_OUT_IRLED (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_61	AF1	B_8	General purpose I/O 61: Options: 1. Alt 0: PWM_OUT_BLED (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_60	AF2	B_8	General purpose I/O 60: Options: 1. Alt 0: PWM_OUT_GLED (O) 2. Alt 1: UART2_RXD (I) (#2) 3. Optional GPIO
GPIO_59	AG1	B_8	General purpose I/O 59: Options: 1. Alt 0: PWM_OUT_RLED (O) 2. Alt 1: UART2_TXD (O) (#2) 3. Optional GPIO
GPIO_58	V1	B_8	General purpose I/O 58: Options: 1. Alt 0: PWM_OUT_STD_2 (O) 2. Alt 1: Reserved 3. Optional GPIO
GPIO_57	V2	B_8	General purpose I/O 57: Options: 1. Alt 0: 2. Alt 1: N/A 3. Optional GPIO
GPIO_56	W2	B_8	General purpose I/O 56: Options: 1. Alt 0: PWM_OUT_STD_0 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_55	K29	B_8	General purpose I/O 55: Options: 1. Alt 0: PWM_OUT_CW2 (O) 2. Alt 1: Reserved 3. Optional GPIO
GPIO_54	K28	B_8	General purpose I/O 54: Options: 1. Alt 0: PWM_OUT_CW1 (O) 2. Alt 1: N/A 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_53	W3	B_8	General purpose I/O 53: Options: 1. Alt 0: Reserved 2. Alt 1: LED_DRIVER_ON (O) 3. Optional GPIO
GPIO_52	W4	B_8	General purpose I/O 52: Options: 1. Alt 0: Reserved 2. Alt 1: N/A 3. Optional GPIO
GPIO_51	V5	B_8	General purpose I/O 51: Options: 1. Alt 0: Reserved 2. Alt 1: DMD_PWR_EN (O) 3. Optional GPIO
GPIO_50	AC29	B_8	General purpose I/O 50: Options: 1. Alt 0: SSP0_CSZ_3 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_49	AC30	B_8	General purpose I/O 49: Options: 1. Alt 0: SSP0_CSZ_4 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_48	AB26	B_8	General purpose I/O 48: Options: 1. Alt 0: USB OTG External USB Switch Control (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_47	AB28	B_8	General purpose I/O 47: Options: 1. Alt 0: PM_ADDR_23 (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_46	K27	B_8	General purpose I/O 46: Options: 1. Alt 0: CW_Index_2 (I) (#1) 2. Alt 1: SSP2_BC_CSZ (O-MST/I-SLV) 3. Optional GPIO
GPIO_45	J30	B_8	General purpose I/O 45: Options: 1. Alt 0: CW_Index_1 (I) (#1) 2. Alt 1: SSP2_CSZ_2 (O-MST/I-SLV) 3. Optional GPIO
GPIO_44	J29	B_8	General purpose I/O 44: Options: 1. Alt 0: OCLKC (O) (#1) 2. Alt 1: SSP2_CSZ_1 (O-MST/I-SLV) 3. Optional GPIO
GPIO_43	J27	B_8	General purpose I/O 43: Options: 1. Alt 0: OCLKD (O) (#1) 2. Alt 1: SSP2_CSZ_0 (O-MST/I-SLV) 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION(2) (3) (4)
NAME	NO.		
GPIO_42	J26	B_8	General purpose I/O 42: Options: 1. Alt 0: IIC2_SDA (B) (#1) 2. Alt 1: SSP2_DO (O) 3. Optional GPIO
GPIO_41	H30	B_8	General purpose I/O 41: Options: 1. Alt 0: IIC2_SCL (B) (#1) 2. Alt 1: SSP2_DI (I) 3. Optional GPIO
GPIO_40	H29	B_8	General purpose I/O 40: Options: 1. Alt 0: MEMAUX_1 (O) (#1) 2. Alt 1: SSP2_SCLK (O-MST/I-SLV) 3. Optional GPIO
GPIO_39	H28	B_8	General purpose I/O 39: Options: 1. Alt 0: UART2_RXD (I) (#1) 2. Alt 1: HBT_CLKOUT (O) 3. Optional GPIO
GPIO_38	H27	B_8	General purpose I/O 38: Options: 1. Alt 0: UART2_TXD (O) (#1) 2. Alt 1: HBT_DO (O) 3. Optional GPIO
GPIO_37	H26	B_8	General purpose I/O 37: Options: 1. Alt 0: CW_Index_2 (I) (#2) 2. Alt 1: DAO_CLKOUT (O) 3. Optional GPIO
GPIO_36	G30	B_8	General purpose I/O 36: Options: 1. Alt 0: CW_Index_1 (I) (#2) 2. Alt 1: DAO_DO_1 (O) 3. Optional GPIO
GPIO_35	G29	B_8	General purpose I/O 35: Options: 1. Alt 0: OCLKC (O) (#2) 2. Alt 1: DAO_DO_0 (O) 3. Optional GPIO
GPIO_34	Y1	B_8	General purpose I/O 34: Options: 1. Alt 0: WRP_CAMERA_TRIG (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_33	Y2	B_8	General purpose I/O 33: Options: 1. Alt 0: PAUX11 (O) {CW Spoke} 2. Alt 1: IIC2_SDA (B) (#2) 3. Optional GPIO
GPIO_32	Y4	B_8	General purpose I/O 32: Options: 1. Alt 0: PAUX10 (O) {CW Rev} 2. Alt 1: IIC2_SCL (B) (#2) 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_31	Y5	B_8	General purpose I/O 31: Options: 1. Alt 0: PAUX9 (O) {XPR-Y} 2. Alt 1: PAUX_INT3 (O) 3. Optional GPIO
GPIO_30	AA1	B_8	General purpose I/O 30: Options: 1. Alt 0: PAUX8 (O) {XPR-X} 2. Alt 1: PAUX_INT2 (O) 3. Optional GPIO
GPIO_29	AA2	B_8	General purpose I/O 29: Options: 1. Alt 0: PAUX7 (O) {SSI Subframe} 2. Alt 1: N/A 3. Optional GPIO
GPIO_28	AA3	B_8	General purpose I/O 28: Options: 1. Alt 0: PAUX6 (O) {UV_LED_EN} 2. Alt 1: LEDSEL_4 (O) 3. Optional GPIO
GPIO_27	AA4	B_8	General purpose I/O 27: Options: 1. Alt 0: PAUX5 (O) {IR_LED_EN} 2. Alt 1: LEDSEL_3 (O) 3. Optional GPIO
GPIO_26	AA5	B_8	General purpose I/O 26: Options: 1. Alt 0: PAUX4 (O) {B_LED_EN} 2. Alt 1: LEDSEL_2 (O) 3. Optional GPIO
GPIO_25	AB2	B_8	General purpose I/O 25: Options: 1. Alt 0: PAUX3 (O) {G_LED_EN} 2. Alt 1: LEDSEL_1 (O) 3. Optional GPIO
GPIO_24	AB3	B_8	General purpose I/O 24: Options: 1. Alt 0: PAUX2 (O) {R_LED_EN} 2. Alt 1: LEDSEL_0 (O) 3. Optional GPIO
GPIO_23	AB4	B_8	General purpose I/O 23: Options: 1. Alt 0: PAUX1 (O) {SEQ Index} 2. Alt 1: PAUX_INT1 (O) 3. Optional GPIO
GPIO_22	AB5	B_8	General purpose I/O 22: Options: 1. Alt 0: PAUX0 (O) {LED SENSE} 2. Alt 1: PAUX_INT0 (O) 3. Optional GPIO
GPIO_21	P3	B_8	General purpose I/O 21: Options: 1. Alt 0: PWM-IN1 (I) 2. Alt 1: N/A 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_20	P2	B_8	General purpose I/O 20: Options: 1. Alt 0: PWM-IN0 (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_19	P1	B_8	General purpose I/O 19: Options: 1. Alt 0: IR1 (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_18	R5	B_8	General purpose I/O 18: Options: 1. Alt 0: IR0 (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_17	R4	B_8	General purpose I/O 17: Options: 1. Alt 0: N/A 2. Alt 1: N/A 3. Optional GPIO
GPIO_16	R2	B_8	General purpose I/O 16: Options: 1. Alt 0: UART1_RTSZ (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_15	R1	B_8	General purpose I/O 15: Options: 1. Alt 0: UART1_CTSZ (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_14	T3	B_8	General purpose I/O 14: Options: 1. Alt 0: UART1_RXD (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_13	T4	B_8	General purpose I/O 13: Options: 1. Alt 0: UART1_TXD (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_12	T5	B_8	General purpose I/O 12: Options: 1. Alt 0: IIC1_SDA (B) 2. Alt 1: N/A 3. Optional GPIO
GPIO_11	T2	B_8	General purpose I/O 11: Options: 1. Alt 0: IIC1_SCL (B) 2. Alt 1: N/A 3. Optional GPIO
GPIO_10	V3	B_8	General purpose I/O 10: Options: 1. Alt 0: SAS_INTGTR_EN (O) 2. Alt 1: N/A 3. Optional GPIO

Table 5-10. GPIO Peripheral Interface (continued)

PIN		I/O (1)	DESCRIPTION (2) (3) (4)
NAME	NO.		
GPIO_09	U1	B_8	General purpose I/O 09: Options: 1. Alt 0: SAS_CSZ (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_08	U2	B_8	General purpose I/O 08: Options: 1. Alt 0: SAS_DO (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_07	U4	B_8	General purpose I/O 07: Options: 1. Alt 0: SAS_DI (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_06	V4	B_8	General purpose I/O 06: Options: 1. Alt 0: SAS_CLK (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_05	A17	B_8	General purpose I/O 05: Options: 1. Alt 0: SSP1_CSZ_2 (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO
GPIO_04	B17	B_8	General purpose I/O 04: Options: 1. Alt 0: SSP1_CSZ_1 (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO
GPIO_03	B15	B_8	General purpose I/O 03: Options: 1. Alt 0: SSP1_CSZ_0 (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO
GPIO_02	C16	B_8	General purpose I/O 02: Options: 1. Alt 0: SSP1_DO (O) 2. Alt 1: N/A 3. Optional GPIO
GPIO_01	D16	B_8	General purpose I/O 01: Options: 1. Alt 0: SSP1_DI (I) 2. Alt 1: N/A 3. Optional GPIO
GPIO_00	E16	B_8	General purpose I/O 00: Options: 1. Alt 0: SSP1_SCLK (O-MST/I-SLV) 2. Alt 1: N/A 3. Optional GPIO

(1) See Table 5-13 for more information on I/O definitions.
(2) This table defines the GPIO capabilities of the DLPC7540. Please see Section 7.3.7 for specific product configuration allocations of these GPIO.
(3) Most GPIO have at least one alternate hardware functional use in addition to being available as a general purpose I/O. Depending on the product configuration, GPIO may be reserved specifically for use as an alternate hardware function (and would therefore not be

available as a general purpose I/O). More information on GPIO allocations for specific product configurations can be found in Section 7.3.7.

(4) All GPIO that are available as a general purpose I/O must be configured as an input, a standard output, or an open-drain output. This is set in the flash configuration. Configure unused GPIO as a logic zero output and leave unconnected, otherwise an external pullup or pulldown resistor is required to avoid a floating input. The reset default for all GPIO is as an input signal. An external pullup resistor (≤ 10 kΩ) is required for each signal configured as open-drain output.

Table 5-11. Clock and Support

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
REFCLKA_I	AJ18	I_9	Crystal A Input: Reference clock crystal input. (2) (3)
REFCLKA_O	AK18	O_{10}	Crystal A Output: Reference clock crystal output. (2)
REFCLKB_I	B16	I_{14}	Crystal B Input: Reference clock crystal input. (2) (3)
REFCLKB_O	A16	O_{15}	Crystal B Output: Reference clock crystal output. (2)
OCLKA	AD30	O_8	General Purpose Output Clock A (4) Targeted for driving Color Wheel motor controller. Frequency is software programmable, with a power-up default frequency of 0.77 MHz. Note: the output frequency is not affected by non-power-up reset operations (i.e., the system holds the last programmed value until system is power cycled).

(1) See Table 5-13 for more information on I/O definitions.
(2) For more information on this signal see Section 6.12
(3) For applications where an external oscillator is used in place of a crystal, use an oscillator to drive this pin
(4) For more information on this signal see Section 6.21

Table 5-12. Power and Ground

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
VDD115_PLLMA	AE18	PWR	1.15-V digital power for MCG (Master Clock Generator A) PLL
VDD115_PLLMB	F15	PWR	1.15-V digital power for MCG (Master Clock Generator B) PLL
VAD115_PLLS	F16	PWR	1.15-V analog power for SCG doubler PLL
VAD18_PLLMA	AE19	PWR	1.8-V analog power for MCG (Master Clock Generator A) PLL
VAD18_PLLMB	F14	PWR	1.8-V analog power for MCG (Master Clock Generator B) PLL
VAD33_OSCA	Y18	PWR	3.3-V analog power for Crystal-OSC
VAD33_OSCB	L17	PWR	3.3-V analog power for Crystal-OSC
VAD115_FPD	F7,F9,F11,J6,L12	PWR	1.15-V analog power for FPD
VDD33_FPD	E6,E8,E10,E12,E14,G6,L11,L13	PWR	3.3-V digital power for FPD
VAD115_VX1	F24,L18	PWR	1.15-V analog power for VX1
VAD18_VX1	E18,L19	PWR	1.8-V analog power for VX1
VAD33_USB	D27,E26,F25	PWR	3.3-V analog power for USB
VDD18_SCS	L16,R6,T25,AE16	PWR	1.8-V digital power for SCS DRAM
VDD121_SCS	L15,N11,P20,U11,V20,Y16	PWR	1.21-V digital power for SCS SRAM
VAD115_HSSI	Y14,Y19,AF7,AF9,AF11,AF13AF21,AF23,AF25	PWR	1.15-V analog power for HSSI interface
VAD115_HSSI0_PLL	AE22	PWR	1.15-V analog power for HSSI-0 PLL
VAD115_HSSI1_PLL	AE10	PWR	1.15-V analog power for HSSI-1 PLL
VDD33_HSSI	Y12,Y20,AE8,AE12,AE20,AE24	PWR	3.3-V digital power for HSSI interface
VAD18_LSIF	Y15,AE13,AE14	PWR	1.8-V analog power for DMD low-speed interface
LVDS_VREFTEST	AF16		Manufacturing test use only - must be left open-unconnected
VDD115	L14,L20,M11,N20,P11,R20,T11,U20,V11,W20,Y11,Y13,Y17	PWR	1.15-V core power
VDD33	H25,K25,L6,M20,M25,N6,P25,R11,T20,U6,V25,W6,W11,Y25,AA6,AB25,AC6,AD25,AE6	PWR	3.3-V digital power

Table 5-12. Power and Ground (continued)

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
VSS	A1,A2,A3,A5,A7,A9,A11,A13,A15,A18,A20,A22,A24,A26,A28,A30,B1,B2,B3,B5,B7,B9,B11,B13,B18,B20,B22,B24,B26,B28,B30,C3,C4,C6,C8,C10,C12,C14,C17,C19,C21,C23,C25,C29,D1,D2,D6,D8,D10,D12,D14,D17,D19,D21,D23,D25,D28,E3,E4,E5,E7,E9,E11,E13,E15,E22,E25,E28,F1,F2,F5,F6,F8,F10,F12,F13,F17,F18,F20,F30,G3,G4,G5,G27,H1,H2,H5,H6,J3,J4,J5,J25.J28,K6,K30,L1,L25,L27,M3,M6,(M12),(M13),(M14),(M15),(M16),(M17),(M18),(M19),N1,(N12,(N13),(N14),(N15),(N16),(N17),(N18),(N19),N25,N28,P6,(P12),(P13),(P14),(P15),(P16),(P17),(P18),(P19),P30,R3,(R12),(R13),(R14),(R15),(R16),(R17),(R18),(R19),R25,R27,T1,T6,(T12),(T13),(T14),(T15),(T16),(T17),(T18),(T19),U3,U5,(U12),(U13),(U14),(U15),(U16),(U17),(U18),(U19),U25,U28,V6,(V12),(V13),(V14),(V15),(V16),(V17),(V18),(V19),V30,W1,W5,(W12),(W13),(W14),(W15),(W16),(W17),(W18),(W19),W25,W27,Y3,Y6,AA25,AA28,AB1,AB6,AB30,AC3,AC25,AC27,AD6,AE1,AE5,AE7,AE9,AE11,AE15,AE17,AE21,AE23,AE25,AE26,AE28,AF3,AF5,AF6,AF8,AF10,AF12,AF14,AF15,AF17,AF18,AF19,AF20,AF22,AF24,AF26,AF28,AF30,AG4,AG6,AG8,AG10,AG12,AG14,AG16,AG18,AG23,AG25,AG27,AG29,AH1,AH2,AH3,AH4,AH6,AH8,AH10,AH12,AH14,AH16,AH18,AH21,AH23,AH25,AH27,AH29,AH30,AJ1,AJ3,AJ5,AJ7,AJ9,AJ11,AJ13,AJ15,AJ17,AJ22,AJ24,AJ26,AJ28,AJ30,AK1,AK3,AK5,AK7,AK9,AK11,AK13,AK15,AK17,AK22,AK24,AK26,AK28,AK30	RTN	GND for all power supplies (Ball numbers in parenthesis are also used as thermal ball and are located within the package center region)
VPGM	G25		Manufacturing use only (efuse). Must be tied to ground.

(1) See Table 5-13 for more information on I/O definitions.

Table 5-13. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8 V SERDES (VX1)	VAD18_VX1	ESD diode to supply rail and GND
2	1.8-V LVDS (LS DMD)	VAD18_LSIF	ESD diode to supply rail and GND
3	1.8-V LMCMOS (LS DMD)	VAD18_LSIF	ESD diode to supply rail and GND
4	3.3-V OpenDrain (VX1)	VDD33	ESD diode to supply rail and GND
5	3.3-V LVDS (FPD)	VDD33_FPD	ESD diode to supply rail and GND
6	3.3-V LVCMOS (PP)	VDD33_FPD	ESD diode to supply rail and GND
7	1.15-V HSSI (HS DMD)	VAD115_HSSI	ESD diode to supply rail and GND
8	3.3-V LVCMOS I/O (8ma output drive - GPIO, etc.)	VDD33	ESD diode to supply rail and GND
9	3.3-V LVCMOS I/O (OSC)	VAD33_OSCA	ESD diode to GND
10	3.3-V LVCMOS I/O (OSC)	VAD33_OSCA	ESD diode to supply rail and GND
11	3.3-V USB (USB)	VAD33_USB	ESD diode and LBJT to GND
12	3.3-V LVCMOS (USB)	VAD33_USB	ESD diode to supply rail and GND
13	3.3-V OpenDrain (I2C)	VDD33	ESD diode to supply rail and GND
14	3.3-V LVCMOS I/O (OSC)	VAD33_OSCB	ESD diode to GND
15	3.3-V LVCMOS I/O (OSC)	VAD33_OSCB	ESD diode to supply rail and GND
TYPE			
I	Input	N/A	
O	Output		
B	Bidirectional		
PWR	Power		
RTN	Ground return		

Table 5-14. Internal Pullup and Pulldown Characteristics(1)

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	CONDITIONS	MIN	MAX	UNIT
Weak pullup resistance	V_{IN} = 0.8 V, VDD33 = 3.3 V	19	50	kΩ
	V_{IN} = 2.0 V, VDD33 = 3.3 V	12	39	kΩ

(1) An external 5.7-kΩ or less pullup or pulldown resistor (if needed) is sufficient for any voltage condition to correctly override any associated internal pullup or pulldown resistance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)(1)

SUPPLY VOLTAGE(2)		MIN	MAX	UNIT
$V_{(VDD115)}$ (Core)		–0.3	1.6	V
$V_{(VDD115\_PLLMA)}$ (Core)		–0.3	1.6	V
$V_{(VDD115\_PLLMB)}$ (Core)		–0.3	1.6	V
$V_{(VDD115\_PLLS)}$ (Core)		–0.3	1.6	V
$V_{(VAD115\_FPD)}$ (Core)		–0.3	1.6	V
$V_{(VAD115\_VX1)}$ (Core)		–0.5	1.5	V
$V_{(VAD115\_HSSI)}$ (Core)		–0.3	1.6	V
$V_{(VAD115\_HSSI0\_PLL)}$ (Core)		–0.3	1.6	V
$V_{(VAD115\_HSSI1\_PLL)}$ (Core)		–0.3	1.6	V
$V_{(VDD121\_SCS)}$ (Core)		–0.4	1.6	V
$V_{(VAD18\_PLLMA)}$ (Core)		–0.3	2.5	V
$V_{(VAD18\_PLLMB)}$ (Core)		–0.3	2.5	V
$V_{(VAD18\_VX1)}$ (I/O)		–0.5	2.5	V
$V_{(VDD18\_SCS)}$ (Core)		–0.4	2.3	V
$V_{(VDD18\_LVDS)}$ (I/O)		–0.3	2.5	V
$V_{(VDD33)}$ (I/O)		–0.3	3.9	V
$V_{(VAD33\_OSCA)}$ (I/O)		–0.3	3.9	V
$V_{(VAD33\_OSCB)}$ (I/O)		–0.3	3.9	V
$V_{(VDD33\_FPD)}$ (I/O)		–0.3	3.9	V
$V_{(VAD33\_USB)}$ (I/O)		–0.3	3.9	V
$V_{(VDD33\_HSSI)}$ (I/O)		–0.3	3.9	V
GENERAL				
T_J	Operating junction temperature	0	115	°C
T_C	Operating case temperature	0	108(3)	°C
I_{lat}	Latch-up	–100	100	mA
T_{stg}	Storage temperature range	-40	125	°C

(1) Stresses beyond those listed under *Section 6.1* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods ca affect device reliability.
(2) All voltage values are with respect to GND.
(3) Value calculated using package parameters defined in *Section 6.4*.

6.2 ESD Ratings

PARAMETER				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI-ESDA-JEDEC JS-001(1)	All pins (except Vx1_CM_CKREF0, 1, 2, 3)	±1000	V
			Vx1_CM_CKREF0, 1, 2, 3	±750	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	All pins (except Vx1_CM_CKREF0, 1, 2, 3)	±500	
			Vx1_CM_CKREF0, 1, 2, 3	+500	
				-200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TOLERANCE	MIN	NOM	MAX	UNIT
$V_{(VDD115)}$ (Core)	1.15-V Power	± 4.35% tolerance	1.10	1.15	1.20	V
$V_{(VDD115\_PLLMA)}$ (Core)	1.15-V Digital Power - MCG-A PLL (Master Clock Generator)	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$V_{(VDD115\_PLLMB)}$ (Core)	1.15-V Digital Power - MCG-B PLL (Master Clock Generator)	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$V_{(VDD115\_PLLS)}$ (Core)	1.15-V Analog Power - SCG Doubler PLL	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$V_{(VAD115\_FPD)}$ (Core)	1.15-V Analog Power - FPD	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$V_{(VAD115\_VX1)}$ (Core)	1.15-V Analog Power - VX1	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$V_{(VAD115\_HSSI)}$ (Core)	1.15-V Analog Power - HSSI	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$\Delta V_{(VAD115\_HSSI)}$ (Core)	pk-pkVAD115_HSSI supply noise @ 10 MHz (sine)				20	mV
$V_{(VAD115\_HSSI0\_PLL)}$ (Core)	1.15-V Analog Power - HSSI0 PLL	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$\Delta V_{(VAD115\_HSSI0\_PLL)}$ (Core)	pk-pkVAD115_HSSI0_PLL supply noise @ 10 MHz (sine)				20	mV
$V_{(VAD115\_HSSI1\_PLL)}$ (Core)	1.15-V Analog Power - HSSI1 PLL	+4.35/-9.13% tolerance	1.045	1.15	1.20	V
$\Delta V_{(VAD115\_HSSI1\_PLL)}$ (Core)	pk-pkVAD115_HSSI1_PLL supply noise @ 10 MHz (sine)				20	mV
$V_{(VDD121\_SCS)}$ (Core)	1.21V Digital Power - SCS DRAM	+7.43/-4.95% tolerance	1.15	1.21	1.30	V
$V_{(VAD18\_PLLMA)}$ (Core)	1.8-V Analog Power - MCG-A PLL (Master Clock Generator)	±5.0% tolerance	1.71	1.80	1.89	V
$V_{(VAD18\_PLLMB)}$ (Core)	1.8-V Analog Power - MCG-B PLL (Master Clock Generator)	±5.0% tolerance	1.71	1.80	1.89	V
$V_{(VAD18\_VX1)}$ (I/O)	1.8-V Analog Power - VX1 Interface	±5.0% tolerance	1.71	1.80	1.89	V
$V_{(VDD18\_SCS)}$ (Core)	1.8-V Digital Power - SCS DRAM	±5.0% tolerance	1.71	1.80	1.89	V
$V_{(VDD18\_LVDS)}$ (I/O)	1.8-V Analog Power - DMD LS Interface	±5.0% tolerance	1.71	1.80	1.89	V
$V_{(VDD33)}$ (I/O)	3.3-V Digital Power - (All 3.3-V I/O without dedicated 3.3-V supply - e.g. GPIO)	±5.0% tolerance	3.135	3.3	3.465	V

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TOLERANCE	MIN	NOM	MAX	UNIT
$V_{(VAD33\_OSCA)}$ (I/O)	3.3-V Analog Power - Crystal-OSCA Interface	±5.0% tolerance	3.135	3.3	3.465	V
$V_{(VAD33\_OSCB)}$ (I/O)	3.3-V Analog Power - Crystal-OSCB Interface	±5.0% tolerance	3.135	3.3	3.465	V
$V_{(VDD33\_FPD)}$ (I/O)	3.3-V Digital Power - FPD interface	±5.0% tolerance	3.135	3.3	3.465	V
$V_{(VAD33\_USB)}$ (I/O)	3.3-V Analog Power - USB Interface	±5.0% tolerance	3.135	3.3	3.465	V
$V_{(VDD33\_HSSI)}$ (I/O)	3.3-V Digital Power - DMD HSSI Interface	±5.0% tolerance	3.135	3.3	3.465	V
$\Delta V_{(VDD33\_HSSI)}$ (I/O)	pk-pkVDD33_HSSI supply noise @ 10 MHz (sine)				60	mV
GENERAL						
T_J	Operating junction temperature		0		115	°C
T_C	Operating case temperature		0		108	°C
T_A	Operating ambient temperature (1) (2)		0		55	°C

(1) The operating ambient temperature range values were determined based on the board design parameters described in Section 10.1.1 , rather than using a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Ambient thermal conditions, which impact $R_{\theta JA}$, vary by application. Thus, maximum operating ambient temperature varies by application.

a. $T_{a\_min} = T_{j\_min} – (P_{d\_min} \times R_{\theta JA}) = 0°C – (host\_min\_valueW \times host\_value°C/W) = –host\_calculated\_value°C$

b. $T_{a\_max} = T_{j\_max} – (P_{d\_max} \times R_{\theta JA}) = +115°C – (host\_max\_valueW \times host\_value°C/W) = +host\_calculated\_value°C$

(2) Operating ambient temperature is dependent on system thermal design. Operating case temperature cannot exceed its specified range across ambient temperature conditions.

6.4 Thermal Information

THERMAL METRIC (1)		TEST CONDITIONS (2)	ZDC P-HBGA676 676 PINS (576 Populated)	UNIT
$R_{\theta JA}$	Junction-to-air thermal resistance (3)	0 m/s of forced airflow, without heat-sink 1 m/s of forced airflow, without heat-sink 2 m/s of forced airflow, without heat-sink 1 m/s of forced airflow, with heat-sink, 7 W 2 m/s of forced airflow, with heat-sink, 7 W 1 m/s of forced airflow, with heat-sink,15 W 2 m/s of forced airflow, with heat-sink, 15 W	7.4 6.3 6.0 5.3 4.8 4.0 3.5	°C/W
R_{JC}	Junction-to-case thermal resistance (4)		2.7	°C/W
R_{JB}	Junction-to-board thermal resistance (4)		3.5	°C/W
ψ_{JT} (5)	Temperature variance from junction to package top center temperature, per unit power dissipation.	0 m/s of forced airflow, without heat-sink 1 m/s of forced airflow, without heat-sink 2 m/s of forced airflow, without heat-sink	0.6 0.6 0.6	°C/W
P_{MAX}	Package - Maximum Power(3) (6)	0 m/s of forced airflow, without heat-sink 1 m/s of forced airflow, without heat-sink 2 m/s of forced airflow, without heat-sink	8.10 9.52 10.00	W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) These test conditions also included a PCB sized at 101.3mm x 152.4mm incorporating the recommended PCB thermal enhancements specified in Section 10.1.1. In addition, airflow is parallel to the board surface directed at the device.
(3) See Table 6-1 for thermal parameters based on the example heat-sinks listed below
  a. Heatsink-7 W: S1525-7W, Size = 25 mm x 25 mm x 7 mm, Pins = 7 x7 = 49 (Vendor: Alpha, Type S Series)
  b. Heatsink-15 W: S1530-15W, Size = 30 mm x 3 0mm x 15 mm, Pins = 8 x 8 = 64 (Vendor: Alpha, Type S Series)
(4) Due to the complex internal construction of the DLPC7540 controller, the R_{JC} and R_{JB} thermal coefficients do not always produce an accurate junction temperature estimate. A limited set of comparison scenario data shows that the R_{JC} and R_{JB} modeled junction temperature can have a +9% to -2% error vs the actual temperature. The amount of this error varies with the use and size of an external heat sink as well as the amount of external air flow. Validate all thermal estimates based on R_{JC} and R_{JB} with an actual temperature measurement at the top-center of the package plus the delta-temp defined by ψ_{JT}.
(5) Example: Using the power we expect of 11.31 W
11.31 W * 0.6 °C/W = 6.786 °C = > $T_{C\text{-}max}$ = 115 °C - ~7 °C = 108 °C
(6) $P_{MAX} = (T_{J\text{-}max} - T_{A\text{-}max}) / R_{\theta JA}$

Table 6-1. Thermal Examples using Two Different Heat-sinks

THERMAL METRIC (1)		TEST CONDITIONS	ZDC P-HBGA676 676 PINS (576 Populated)	UNIT
$R_{\theta JA}$	Junction-to-air thermal resistance	1 m/s of forced airflow, with heat-sink, 7 W 2 m/s of forced airflow, with heat-sink, 7 W 1 m/s of forced airflow, with heat-sink, 15 W 2 m/s of forced airflow, with heat-sink, 15 W	5.3 4.8 4.0 3.5	°C/W
P_{MAX}	Package - Maximum Power	1 m/s of forced airflow, with heat-sink, 7 W 2 m/s of forced airflow, with heat-sink, 7 W 1 m/s of forced airflow, with heat-sink, 15 W 2 m/s of forced airflow, with heat-sink, 15 W	11.32 12.50 15.00 17.14	W

(1) This table show examples of what is achievable based on the two example heat-sinks.

6.5 Power Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX[1]	UNIT
$V_{(VDD115)}$	1.15-V Power	Maximum current at VDD115 = 1.2 V			5640	mA
$V_{(VDD115\_PLLMA)}$ (Core)	1.15-V Digital Power MCG-A PLL (Master Clock Generator)	Maximum current at VDD115_PLLMA = 1.2 V			6	mA
$V_{(VDD115\_PLLMB)}$ (Core)	1.15-V Digital Power MCG-B PLL (Master Clock Generator)	Maximum current at VDD115_PLLMB = 1.2 V			6	mA
$V_{(VDD115\_PLLS)}$ (Core)	1.15-V Analog Power SCG Doubler PLL	Maximum current at VDD115_PLLS = 1.2 V			3	mA
$V_{(VAD115\_FPD)}$ (Core) [2]	1.15-V Analog Power FPD	Maximum current at VAD115_FPD = 1.2 V Ports A and B Active, Port C inactive			99	mA
$V_{(VAD115\_VX1)}$ (Core) [2]	1.15-V Analog Power VX1	Maximum current at VAD115_VX1 = 1.2 V 8 Lanes, with total BW = 3.0Gbps)			400	mA
$V_{(VAD115\_HSSI)}$ (Core)	1.15-V Digital Power HSSI	Maximum current at VDD115_HSSI = 1.2 V Both ports active			462	mA
$V_{(VAD115\_HSSI0\_PLL)}$ (Core)	1.15-V Digital Power HSSI0 PLL	Maximum current at VDD115_HSSI0_PLL = 1.2 V Both ports active			1	mA
$V_{(VAD115\_HSSI1\_PLL)}$ (Core)	1.15-V Digital Power HSSI1 PLL	Maximum current at VDD115_HSSI1_PLL = 1.2 V Both ports active			1	mA
$V_{(VDD121\_SCS)}$ (Core)	1.21V Digital Power SCS DRAM	Maximum current at VDD121_SCS = 1.30 V			334	mA
$V_{(VAD18\_PLLMA)}$ (Core)	1.8-V Analog Power MCG-A PLL (Master Clock Generator)	Maximum current at VAD18_PLLMA = 1.89 V			10	mA
$V_{(VAD18\_PLLMB)}$ (Core)	1.8-V Analog Power MCG-B PLL (Master Clock Generator)	Maximum current at VAD18_PLLMB = 1.89 V			10	mA
$V_{(VAD18\_VX1)}$ (I/O) [2]	1.8-V Analog Power VX1 Interface	Maximum current at VAD18_VX1 = 1.89 V 8 Lanes, with total BW = 3.0Gbps			41	mA
$V_{(VDD18\_SCS)}$ (Core)	1.8-V Digital Power SCS DRAM	Maximum current at VDD18_SCS = 1.89 V			327	mA
$V_{(VDD18\_LVDS)}$ (I/O)	1.8-V Analog Power DMD LS Interface	Maximum current at VDD18_LVDS = 1.89 V			31	mA
$V_{(VDD33)}$ (I/O)	3.3-V Digital Power - (All 3.3-V I/O without dedicated 3.3-V supply - e.g. GPIO)	Maximum current at VDD33 = 1.3456 V			28	mA
$V_{(VAD33\_OSCA)}$ (I/O)	3.3-V Analog Power Crystal/OSCA Interface	Maximum current at VDD33_OSCA = 1.3456 V			5	mA
$V_{(VAD33\_OSCB)}$ (I/O)	3.3-V Analog Power Crystal-OSCB Interface	Maximum current at VDD33_OSCB = 1.3456 V			5	mA
$V_{(VDD33\_FPD)}$ (I/O) [2]	3.3-V Digital Power FPD interface	Maximum current at VDD33_FPD = 1.3456 V Ports A and B Active, Port C inactive			102	mA
$V_{(VAD33\_USB)}$ (I/O)	3.3-V Analog Power USB Interface	Maximum current at VDD33_USB = 1.3456 V			78	mA

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$V_{(VDD33\_HSSI)}$ (I/O)	3.3-V Digital Power DMD HSSI Interface	Maximum current at VDD33_HSSI = 1.3456 V Both ports active, with total BW = 3.0Gbps			194	mA

(1) Vendor estimate for worst case power PVT condition = corner process, high voltage, high temperature (115°C junction).
(2) The V-by-One interface and FPD-Link receivers are never intended to be simultaneously enabled . Always disable one of these interfaces.

6.6 Pin Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	1.8 V LVCMOS (I/O type 3 - LS DMD)		1.05			V
		3.3 V OpenDrain (I/O type 4 - VX1)		N/A			
		3.3 V LVCMOS (I/O type 6 - FPD)		0.8 × VDD33_FPD			
		3.3 V LVCMOS (I/O type 6 - PP)		2.0			
		3.3 V LVCMOS (I/O type 8 - GPIO)		2.0			
		3.3 V LVCMOS (I/O type 9 - OSCA)		2.0			
		3.3 V LVCMOS (I/O type 10 - OSCB)		2.0			
		3.3 V OpenDrain (I/O type 13 - I2C)		0.7 × VDD33			
V_{IL}	Low-level input threshold voltage	1.8 V LVCMOS (I/O type 3 - LS DMD)				0.6	V
		3.3 V OpenDrain (I/O type 4 - VX1)				N/A	
		3.3 V LVCMOS (I/O type 6 - FPD)				0.2 × VDD33_FPD	
		3.3 V LVCMOS (I/O type 6 - PP)				0.8	
		3.3 V LVCMOS (I/O type 8 - GPIO)				0.8	
		3.3 V LVCMOS (I/O type 9 - OSCA)				0.8	
		3.3 V LVCMOS (I/O type 10 - OSCB)				0.8	
		3.3 V OpenDrain (I/O type 13 - I2C)				0.3 × VDD33	
I_{IH}	High-level input current	1.8 V LVCMOS (I/O type 3 - LS DMD)	V_{IN} = VAD18_LSIF	–10		10	µA
		3.3 V OpenDrain (I/O type 4 - VX1)		N/A		N/A	
		3.3 V LVCMOS (I/O type 6 - PP)		-10		10	
		3.3 V LVCMOS (I/O type 8 - GPIO)	V_{IN} = VDD33	–10		10	
		3.3 V LVCMOS (I/O type 9 - OSCA)	V_{IN} = VDD33	–10		10	
		3.3 V LVCMOS (I/O type 10 - OSCB)	V_{IN} = VDD33	–10		10	
		3.3 V OpenDrain (I/O type 13 - I2C)		–10		10	

6.6 Pin Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current	1.8 V LVCMOS (I/O type 3 - LS DMD)	V_{IN} = VSS	–10		10	µA
		3.3 V OpenDrain (I/O type 4 - VX1)		N/A		N/A	
		3.3 V LVCMOS (I/O type 6 - PP)		-10		10	
		3.3 V LVCMOS (I/O type 8 - GPIO)	V_{IN} = VSS	–10		10	
		3.3 V LVCMOS (I/O type 9 - OSCA)	V_{IN} = VSS	–10		10	
		3.3 V LVCMOS (I/O type 10 - OSCB)	V_{IN} = VSS	–10		10	
		3.3 V OpenDrain (I/O type 13 - I2C)		–10		10	
V_{OH}	High-level output voltage	1.8 V LVCMOS (I/O type 3 - LS DMD)		VDD18 - 0.6			V
		3.3 V OpenDrain (I/O type 4 - VX1)		N/A			
		3.3 V LVCMOS (I/O type 6 - PP)		N/A			
		3.3 V LVCMOS (I/O type 8 - GPIO)	I_{OH} = 8 mA	VDD33 - 0.6			
		3.3 V LVCMOS (I/O type 9 - OSCA)		N/A			
		3.3 V LVCMOS (I/O type 10 - OSCB)		N/A			
		3.3 V OpenDrain (I/O type 13 - I2C)		N/A			
V_{OL}	Low-level output voltage	1.8 V LVCMOS (I/O type 3 - LS DMD)				0.4	V
		3.3 V OpenDrain (I/O type 4 - VX1)	I_{OL} = 8 mA			0.4	
		3.3 V LVCMOS (I/O type 6 - PP)				N/A	
		3.3 V LVCMOS (I/O type 8 - GPIO)	I_{OL} = 8 mA			0.4	
		3.3 V LVCMOS (I/O type 9 - OSCA)				N/A	
		3.3 V LVCMOS (I/O type 10 - OSCB)				N/A	
		3.3 V OpenDrain (I/O type 13 - I2C)	3-mA sink			0.4	

6.6 Pin Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current	1.8 V LVCMOS (I/O type 3 - LS DMD)		N/A			mA
		3.3 V OpenDrain (I/O type 4 - VX1)		N/A			
		3.3 V LVCMOS (I/O type 6 - PP)		N/A			
		3.3 V LVCMOS (I/O type 8 - GPIO)	V_{OH} = VDD33 - 0.6 V	8			
		3.3 V LVCMOS (I/O type 9 - OSCA)		N/A		N/A	
		3.3 V LVCMOS (I/O type 10 - OSCB)		N/A		N/A	
		3.3 V OpenDrain (I/O type 13 - I2C)		N/A			
I_{OL}	Low-level output current	1.8 V LVCMOS (I/O type 3 - LS DMD)		N/A			mA
		3.3 V OpenDrain (I/O type 4 - VX1)	V_{OL} = 0.4 V	8			
		3.3 V LVCMOS (I/O type 6 - PP)				N/A	
		3.3 V LVCMOS (I/O type 8 - GPIO)	V_{OL} = 0.4 V	8			
		3.3 V LVCMOS (I/O type 9 - OSCA)		N/A		N/A	
		3.3 V LVCMOS (I/O type 10 - OSCB)		N/A		N/A	
		3.3 V OpenDrain (I/O type 13 - I2C)	V_{OL} = 0.6 V	6		-	
I_{OZ}	High-impedance leakage current	1.8 V LVCMOS (I/O type 3 - LS DMD)		N/A			µA
		3.3 V OpenDrain (I/O type 4 - VX1)		-10		10	
		3.3 V LVCMOS (I/O type 6 - PP)		-10		10	
		3.3 V LVCMOS (I/O type 8 - GPIO)	VOUT = VDD33	–10		10	
		3.3 V LVCMOS (I/O type 9 - OSCA)		N/A		N/A	
		3.3 V LVCMOS (I/O type 10 - OSCB)		N/A		N/A	
		3.3 V OpenDrain (I/O type 13 - I2C)		N/A		N/A	

(1) The number inside each parenthesis for the I/O refers to the type defined in Table 5-13.

6.7 DMD HSSI Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{DIFF}	Output Peak-to-Peak Differential (1) (3) (into floating load R_{LOAD} = 100 Ω)	Data	400		1000	mVppd
		Clock	590		1000	mVppd
V_{CM}	Output common mode(3) (into floating load R_{LOAD} = 100 Ω)		200		700	mV
$\|V_{OD}\|$	Output differential voltage(1) (2) (into floating load R_{LOAD} = 100 Ω)	Data	200		500	mV
		Clock	295		500	mV
R_{DIFF}	Differential termination resistance		80	100	120	Ω
R_{TERM}	Single-ended termination resistance		40	50	60	Ω
SDD22	Differential output return loss (100 MHz to 0.75 × Baud)				-8	dB
SCC22	Common mode return loss (100 MHz to 0.75 × Baud)				-6	dB
N_{CM}	Transmitter common mode noise				(7.5% × V_{DIFF}) + 25 mV	mVppd
DJ_{DATA}	Deterministic jitter data (non-DCD)				0.20	UI pp
DJ_{CLOCK}	Deterministic jitter clock (non-DCD)				0.16	UI pp
DCD	Duty cycle distortion				0.05	UI pp
TJ	Total jitter (random + DJ)				0.30	UI pp

(1) $V_{DIFF-pp}$ = (Vp - Vn)cycle_N - (Vp - Vn)cycle_N+1 = 2 × $|V_{OD}|$
See Figure 6-1.
(2) See link to HSSI characteristics
(3) Measured with a interconnect with insertion loss of 3dB at 1.6 GHz.|

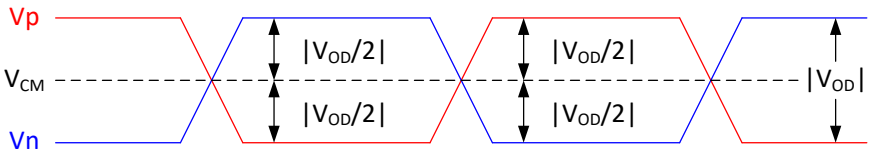


Figure 6-1. HSSI Differential Voltage Parameters

6.8 DMD Low-Speed LVDS Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{DIFF}	Output peak-to-peak differential (into R_{LOAD} = 100 Ω)	VAD18_LSIF (I/O type 2)	340		600	mVppd
V_{CM}	Steady-state common mode voltage	VAD18_LSIF (I/O type 2)	1100	1200	1300	mV
$\|V_{OD}\|$(1)	Differential output voltage (into R_{LOAD} = 100 Ω)	VAD18_LSIF (I/O type 2)	170		300	mV
$\|V_{OD}$ (Δ) $\|$(2)	V_{OD} change (between logic states)	VAD18_LSIF (I/O type 2)			25	mV
V_{CM} (Δ)	V_{CM} change (between logic states)	VAD18_LSIF (I/O type 2)			25	mV
V_{OH}	Single-ended output voltage high (3)	VAD18_LSIF (I/O type 2)			1450	mV
V_{OL}	Single-ended output voltage low (3)	VAD18_LSIF (I/O type 2)	950			mV
Tx_{term}	Internal differential termination		85	100	115	Ω

(1) V_{DIFF}-pp = (Vp - Vn)cycle_N - (Vp - Vn)cycle_N+1 = 2 × $|V_{OD}|$
See Figure 6-2
(2) $|V_{OD}$ (Δ)| = | | V_{OD}|cycle _N - $|V_{OD}|$cycle_N+1 |
(3) V_{OH} = 1300 + 300/2 = 1450; V_{OL} = 1100- 300/2 = 950

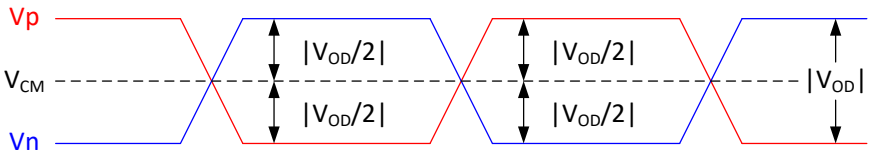


Figure 6-2. DMD Low-Speed Differential Voltage Parameters

6.9 V-by-One Interface Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)			MIN	NOM	MAX	UNIT
V_{DIFF}	Input peak-to-peak differential(2)	VAD18_VX1 (I/O type 1)	100			mVppd
$\|V_{ID}\|$	Differential input voltage(2)	VAD18_VX1 (I/O type 1)	50			mV
Rx_{term}	Internal differential termination	VAD18_VX1 (I/O type 1)	80	100	120	Ω

(1) See the V-by-One interface standard for more information
(2) See link to v-by-one timinig

6.10 FPD-Link LVDS Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			MIN	NOM	MAX	UNIT
V_{DIFF}	Input peak-to-peak differential	VDD33_FPD (I/O type 5)	200		1200	mVppd
$\|V_{ID}\|$	Differential input voltage	VDD33_FPD (I/O type 5)	100		600	mV
V_{CM}	Steady-state common mode voltage (2)	VDD33_FPD (I/O type 5)	0.25		2.4	V
Rx_{term}	Internal differential termination	VDD33_FPD (I/O type 5)	90	110	132	Ω

(1) See Figure 6-14
(2) If V_{CM} falls below $V_{CM(min)}$ at the inputs to the receiver, an open input detection circuit is automatically enabled. This detection circuit disables the receiver until the input V_{CM} rises above $V_{CM(min)}$.

6.11 USB Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER(1) (2)			MIN	NOM	MAX	UNIT
Low-Speed and Full Speed (Input Level)						
V_{IH}	Single-ended input voltage high (driven)		2.0			V
V_{IHZ}	Single-ended input voltage high (floating)		2.7		3.6	V
V_{IL}	Single-ended input voltage low				0.8	V
V_{DI}	Differential input sensitivity	|(DP) - (DM)|	0.2			V
V_{CM}	Differential common mode voltage	Includes V_{DI} range	0.8		2.5	V
Low-Speed and Full Speed (Output Level)						
V_{OL}	Low-level output voltage	with 1.425KΩ pullup to 3.6V	0.0		0.3	V
V_{OH}	High-level output voltage	with 14.25KΩ pulldown	2.8		3.6	V
V_{CRS}	Output signal crossover voltage		1.3		2.0	V
High-Speed (Input Level)						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)		525		626	mV
V_{HSCM}	High-speed data signal common mode voltage		-50		500	mV

Over operating free-air temperature range (unless otherwise noted)

PARAMETER(1) (2)			MIN	NOM	MAX	UNIT
High-Speed (Output Level)						
V_{HSOI}	High-speed idle level		–10.0		10.0	mV
V_{HSOH}	High-speed data signal - high		360		440	mV
V_{HSOL}	High-speed data signal - low		–10.0		10.0	mV
V_{CHIRPJ}	High-speed chirp J level (differential voltage)		700		1100	mV
V_{CHIRPK}	High-speed chirp K level (differential voltage)		-900		-500	mV
Termination						
R_{PU}	Bus pullup resistor		1.425		1.575	KΩ
R_{PD}	Bus pulldown resistor		14.25		15.75	KΩ
Z_{HSDRV}	High-speed driver output impedance		40.5		49.5	Ω

(1) Referenced to VAD33_USB (I/O type 11)
(2) When used as a master as part of USB OTG, the DLPC7540 requires an External USB Switch to provide the USB 5-V power. The example shown in Figure 6-3 makes use of a TI TPS2500/2501 device. The example figure does not describe the required ancillary components (such as, resistors and capacitors). For this information please refer to the USB Switch logic datasheet for the selected device. The External USB Switch is not required for product configurations that are supporting USB slave mode only.

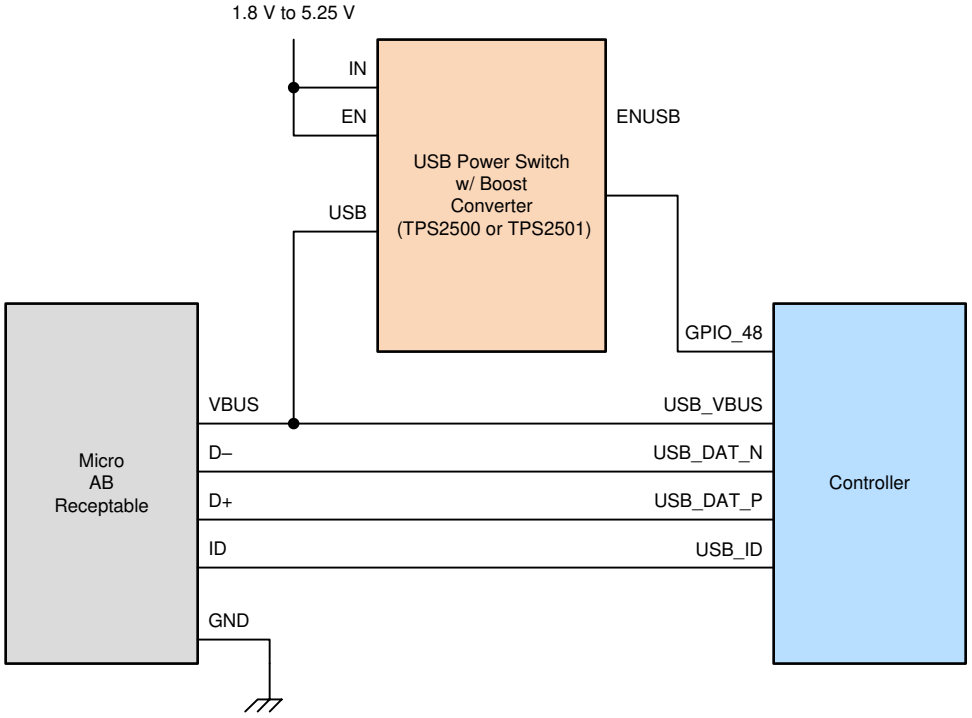


Figure 6-3. External USB Switch Example for DLPC7540 Controller as USB OTG Master

6.12 System Oscillator Timing Requirements

PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, REFCLKA(1) (2)	PLLA: 40 MHz	39.9960	40.000	40.0040	MHz
t_c	Cycle time, REFCLKA(1)	PLLA: 40 MHz	24.9975	25.000	25.0025	ns
$t_{w(H)}$	Pulse duration(3), REFCLKA, high	PLLA: 40 MHz 50% to 50% reference points (signal)	11.25			ns
$t_{w(L)}$	Pulse duration(3), REFCLKA, low	PLLA: 40 MHz 50% to 50% reference points (signal)	11.25			ns
t_t	Transition time(3), REFCLKA, $t_t = t_f / t_r$	PLLA: 40 MHz 20% to 80% reference points (signal)			2.5	ns
t_{jp}	Long term periodic jitter(3), REFCLKA (that is the deviation in period from ideal period due solely to high frequency jitter)	PLLA: 40 MHz			18	ps
f_{clock}	Clock frequency, REFCLKB(1)	PLLB: 38 MHz	37.9962	38.000	38.0038	MHz
t_c	Cycle time, REFCLKB(1)	PLLB: 38 MHz	26.3132	26.3157	26.3184	ns
$t_{w(H)}$	Pulse duration(3), REFCLKB, high	PLLB: 38 MHz 50% to 50% reference points (signal)	11.84			ns
$t_{w(L)}$	Pulse duration(3), REFCLKB, low	PLLB: 38 MHz 50% to 50% reference points (signal)	11.84			ns
t_t	Transition time(3), REFCLKB, $t_t = t_f / t_r$	PLLB: 38 MHz 20% to 80% reference points (signal)			2.63	ns
t_{jp}	Long term periodic jitter(3), REFCLKB (that is the deviation in period from ideal period due solely to high frequency jitter)	PLLB: 38 MHz			18	ps

(1) The REFCLK inputs do not support spread spectrum clock spreading.
(2) Multi-Controller systems require that a single oscillator be used to drive the REFCLKA input for all controllers in the system.
(3) Applies only when driven through an external digital oscillator. This is a 1 sigma RMS value.

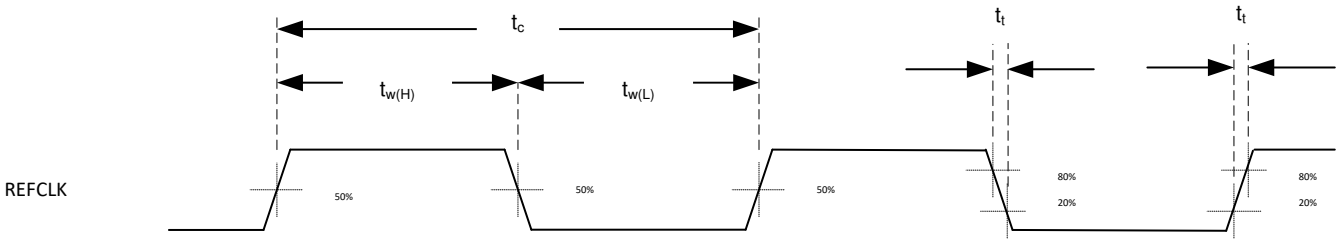


Figure 6-4. System Oscillators

6.13 Power Supply and Reset Timing Requirements

PARAMETER			MIN	MAX	UNIT
$t_{RAMP-UP}$	Power supply ramp-up time. (1) Figure 6-5	Power supply ramp for *each* supply Ramp-up time: TOV × 10% to TOV × 90% TOV = Typical Operational Voltage	0.01	10	ms
$t_{RAMP-UP-TOTAL}$	Total power supply ramp-up time.(1)	Total time within which the 1.15-V, 1.8-V, 1.21-V, and 3.3-V supplies must complete their ramp-up from the start of the 1.15-V ramp-up. Ramp-up time: TOV × 10% to TOV × 90% TOV = Typical Operational Voltage		100	ms
$t_{RAMP-DOWN}$	Power supply ramp-down time. (1) Figure 6-5 Figure 6-6	Power supply ramp for *each* supply Ramp-down time: TOV × 90% to TOV × 10% TOV = Typical Operational Voltage	0	100	ms
$t_{RAMP-DOWN-TOTAL}$	Total power supply ramp-down time.(1)	Total time within which the 1.15-V, 1.8-V, 1.21-V, and 3.3-V supplies must complete their ramp-down from the start of the 3.3-V ramp-up. Ramp-down time: TOV × 90% to TOV × 10% TOV = Typical Operational Voltage		100	ms
t_{RUSD18}	1.8-V Supply Ramp-up Start Delay (2) Figure 6-6	Delay from 1.15-V supply ramp start to 1.8-V supply ramp start.	See (3)		ms
t_{RUSD33}	3.3-V Supply Ramp-up Start Delay (2) Figure 6-6	Delay from 1.15-V supply ramp start to 3.3-V supply ramp start	10	50	ms
t_{RUSD12}	1.21-V Supply Ramp-up Start Delay (2) Figure 6-6	Delay from 1.8-V supply ramp start to 1.21-V supply ramp start.	See (4)		ms
t_{RDSD18}	1.8-V Supply Ramp-down Start Delay (2) Figure 6-6	Delay from 1.21-V supply ramp start to 1.8-V supply ramp start.	See (5)		ms
$t_{RDSD115}$	1.15-V Supply Ramp-down Start Delay (2) Figure 6-6	Delay from 3.3-V supply ramp start to 1.15-V supply ramp start.	See(8)		
t_{EW}	Early Warning Time Figure 6-8	PWRGOOD goes inactive low (as an early warning) prior to any power supply voltage going below the controller specification	500		µs
t_{PH}	Power Hold Time Figure 6-8	POSENSE remains active after PWRGOOD is disabled	500(9)		µs
t_{w1}	Pulse duration, in-active low, PWRGOOD Figure 6-7	PWRGOOD inactive time while POSENSE is active 50% to 50% reference points (signal)	4	1000 (6)	µs
t_{t1}	Transition time, PWRGOOD $t_{t1} = t_{f1}$ and t_{r1} Figure 6-7	Rise and Fall time for PWRGOOD 20% to 80% reference points (signal)		625	µs
t_{w2}	Pulse duration, in-active low, POSENSE Figure 6-8	POSENCE inactive time while PWRGOOD is inactive 50% to 50% reference points (signal)	100		ms
t_{t2}	Transition time, POSENSE $t_{t1} = t_{f1}$ and t_{r1} Figure 6-8	Rise and Fall time for POSENSE (7) 20% to 80% reference points (signal)		25	µs
t_{PSD}	PWRGOOD Start Delay Figure 6-7	Time after rising edge of POSENSE before PWRGOOD effects DLPC7540 operation	51.5	60	ms
t_{PROJ_ON}	PROJ_ON fall time delay to PWRGOOD Figure 6-8	Fall Delay PROJ_ON 80% to PWRGOOD 80% fall time start	10		ms
$t_{REFCLKA}$	Time to stable REFCLKA Figure 6-7	Time to stable REFLCKA before POSENSE	See (10)		

(1) It is assumed that all 1.15-V supplies come from the same source, although some can have additional filtering before entering the DLPC7540. As such, it is expected these supplies to ramp together (aside from differences caused by filtering). This same expectation is true for the 1.21-V, 1.8-V, and 3.3-V supplies.

(2) The DLPC7540 has specific power supply sequencing requirements which are listed below, and which also include the timings specified in this table.

a. Power Up Order:

i. 1.15-V (Core, Analog) » 1.8-V (I/O, SCS) » 1.21-V (SCS)
ii. 1.15-V (Core, Analog) » 3.3-V (I/O

b. Power Down Order:

i. 3.3-V (I/O) » 1.15-V (Core, Analog)
ii. 1.21-V (SCS) » 1.8-V (I/O, SCS) » 1.15-V (Core, Analog)

(3) This delay requirement parameter is defined as the time between two events. The first event is the point where the 1.15-V power supply ramp-up is started, and the second event is when the 1.15-V supply ramp-up reaches 80% of TOV (at which point the 1.8-V supply can start its ramp-up). Because the occurrence of the second event depends on the specific design of the 1.15-V power supply, the designer must determine the specific delay time.
(4) This delay requirement parameter is defined as the time between two events. The first event is the point where the 1.8-V power supply ramp-up is started, and the second event is when the 1.8-V supply ramp-up reaches 80% of TOV (at which point the 1.21-V supply can start its ramp-up). Because the occurrence of the second event depends on the specific design of the 1.8-V power supply, the designer must determine the specific delay time.
(5) This delay requirement parameter is defined as the time between two events. The first event is the point where the 1.21-V power supply ramp-down is started, and the second event is when the 1.21-V supply ramp-down reaches 20% of TOV (at which point the 1.8-V supply can start its ramp-down). Because the occurrence of the second event depends on the specific design of the 1.21-V power supply, the designer must determine the specific delay time.
(6) This max value is only applicable if the 1.8-V power remains ON while PWRGOOD is inactive. Otherwise, there is no maximum limit.
(7) As long as noise on this signal is below the hysteresis threshold
(8) This delay requirement parameter is defined as the time between two events. The first event is the point where the 3.3-V power supply ramp-down is started, and the second event is when the 3.3-V supply ramp-down and 1.8-V supply ramp down reaches 10% of TOV (at which point the 1.15-V supply can start its ramp-down). Because the occurrence of the second event depends on the specific design of the 3.3V and 1.8-V power supply, the designer must determine the specific delay time.
(9) If PROJ_ON is used for power down then Power Hold Time (t_{PH}) is not required.
(10) This delay requirement parameter is defined by design of RECLKA oscillator. Stable clock must be provided before releasing POSENSE.

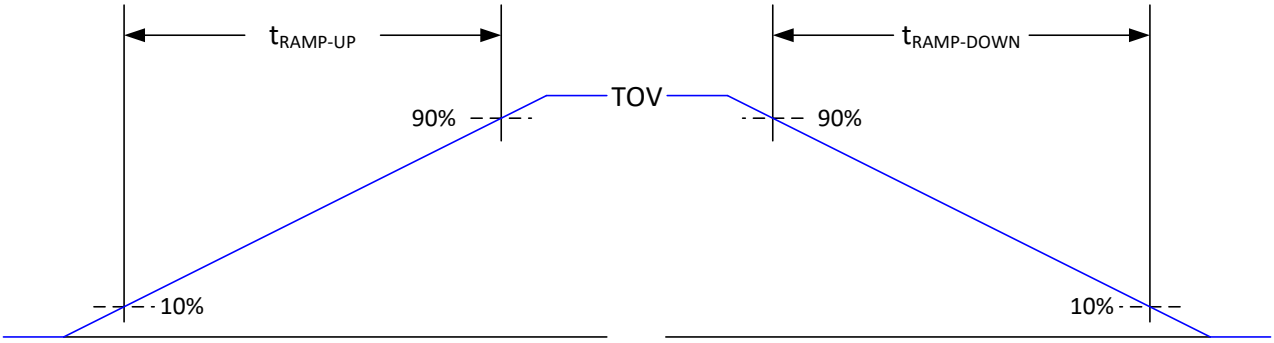
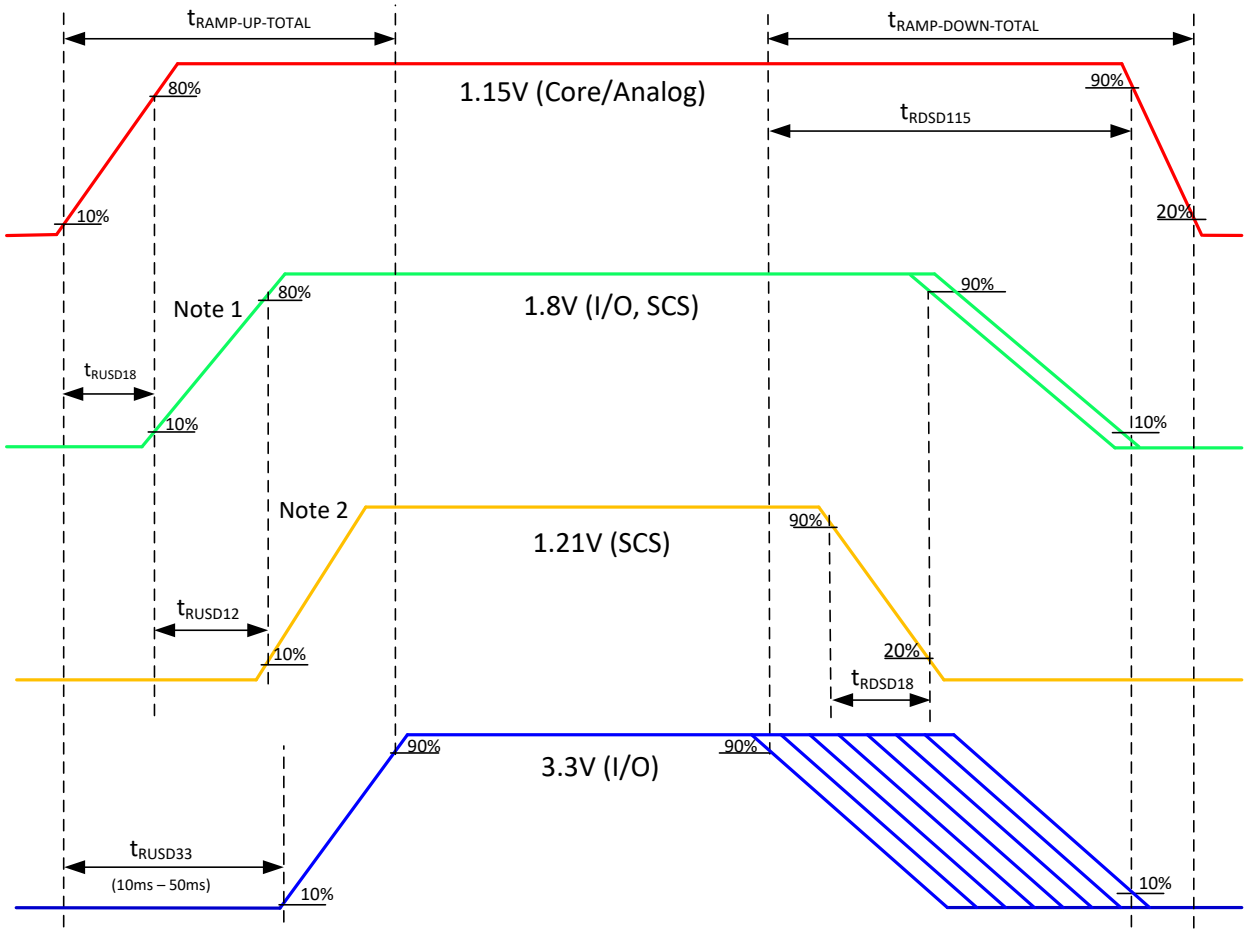


Figure 6-5. Power Supply Ramp Time



Note 1: No power up or power down timing dependency between 1.8V and 3.3V
Note 2: No power up or power down timing dependency between 1.21V and 3.3V

Figure 6-6. Power Supply Ramp Sequencing Profiles

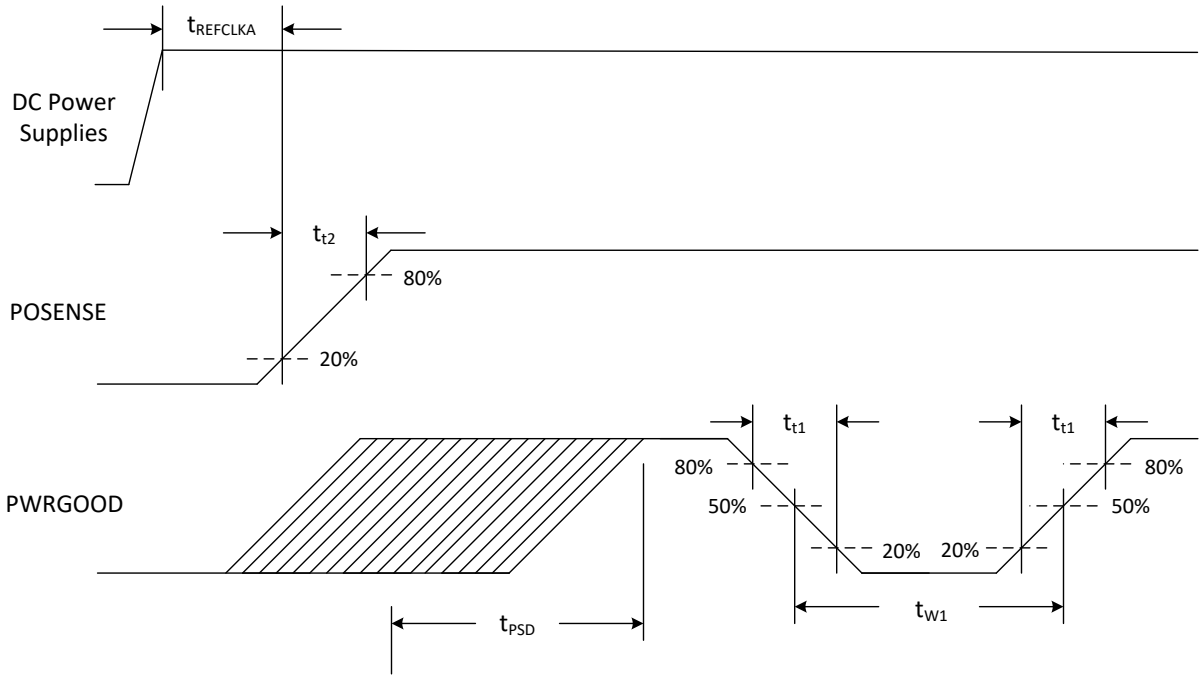


Figure 6-7. Power Up Timing

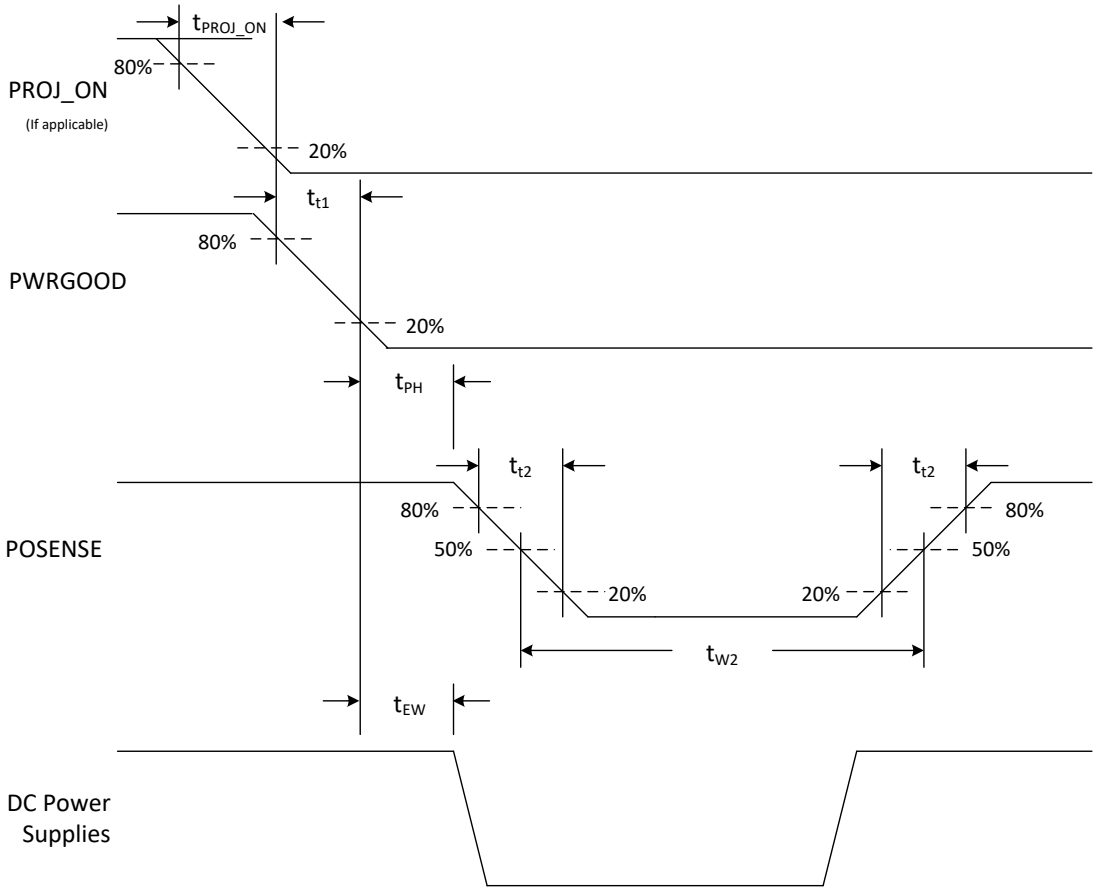


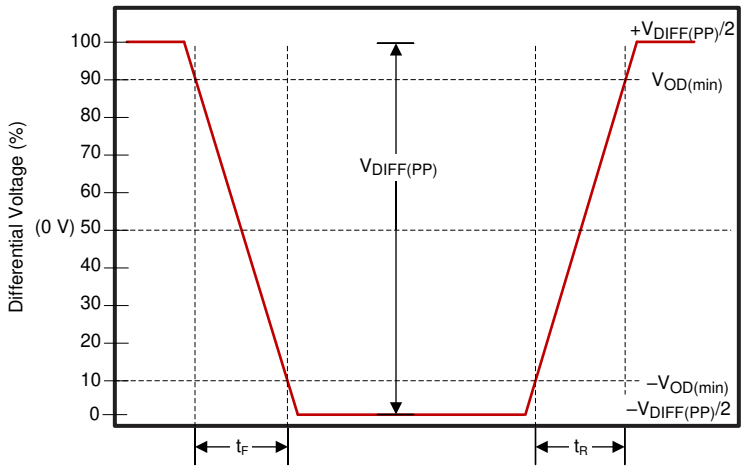
Figure 6-8. Power Down Timing

6.14 DMD HSSI Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
Baud	Baud Rate		2.4		3.2	Gbps
UI	Unit Interval, 1/Baud		312.5		416.7	ps
t_R	Differential output rise time (1) (2) (0% to 100% of minimum eye mask height)	Data	50		115	ps
		Clock	50		135	ps
t_F	Differential output fall time(1) (2) (0% to 100% of minimum eye mask height)	Data	50		115	ps
		Clock	50		135	ps
t_{X1}	maximum eye closure(3)	at zero crossing			0.15	UI
t_{X2}	maximum eye closure(3)	at minimum eye height			0.375	UI
t_{EYE}	Differential Data Eye(3)		0.7			UI
$t_{skIn2In}$	Lane to lane skew within a macro(2)				|200|	ps
t_{skM2M}	Lane to lane skew macro to macro(2)				|4UI+200|	ps
f_{SSCD}	Spread Spectrum (Down Spreading Only) (4)	When SSCD Enabled			1	%
f_{MOD}	Modulation Frequency (4)	When SSCD Enabled		78.125		KHz

(1) Rise and Fall times are associated with V_{DIFF}-pp as shown in Figure 6-9
(2) Measured with an interconnect with an insertion loss of 3dB at 1.6 GHz
(3) See Figure 6-10
(4) When SSCD is enabled, the available modulation waveform is: Triangular



V_{CM} is removed when signals are viewed differentially

Figure 6-9. HSSI Differential Timing Parameters

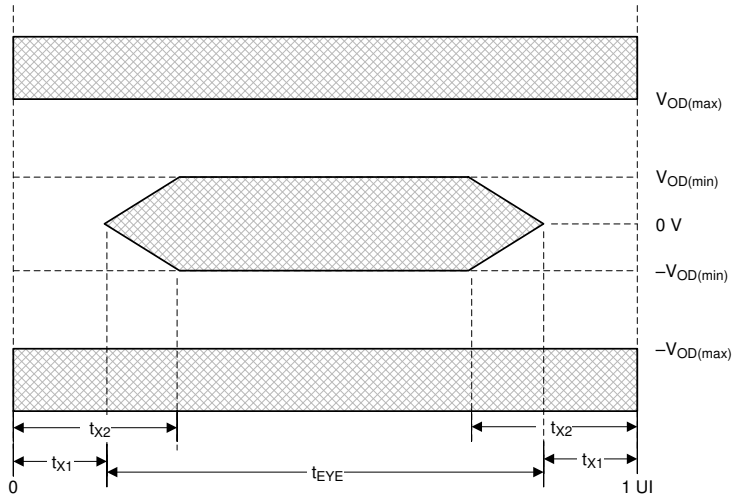


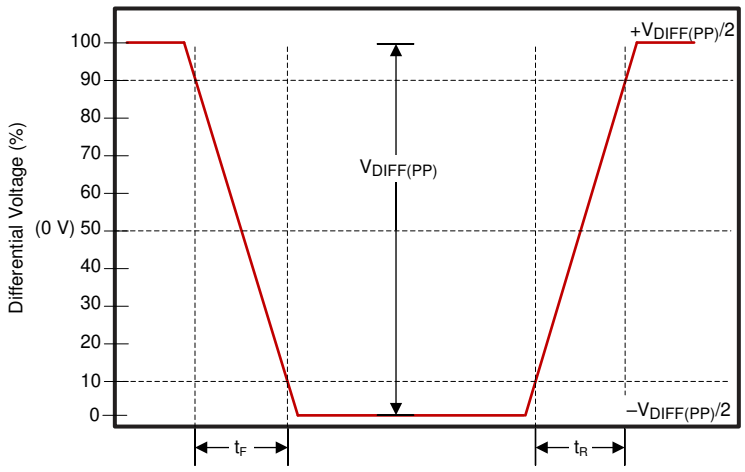
Figure 6-10. HSSI Eye Characteristics

6.15 DMD Low-Speed LVDS Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
fclock			119.966	120	120.034	MHz
t_R (1)	Differential output rise time (10% to 90%)				250	ps
t_F (1)	Differential output fall time (10% to 90%)				250	ps
DCD	Duty Cycle Distortion		45		55	%

(1) Rise and Fall times are associated with V_{DIFF}-pp as shown in Figure 6-11



V_{CM} is removed when signals are viewed differentially

Figure 6-11. DMD Low-Speed Differential Timing Parameters

6.16 V-by-One Interface General Timing Requirements

PARAMETER(1)		MIN	MAX	UNIT
f_{clock}	Source clock frequency	40 (1 lane) 20 (1 lane with Pixel Repeat) (2)	600 (8 lanes)	MHz

PARAMETER(1)			MIN	MAX	UNIT
$f_{link-ck}$	Link clock frequency per lane (3)	8 lanes 4 lanes 2 lanes 1 lane	43 43 43 43 (21.5 with Pixel Repeat)	75 85 85 85	MHz
f_{link}	Link transfer rate (3)	3-Byte Mode 4-Byte Mode 5-Byte Mode	2 2 2.15	2.55 3.0 3.0	Gbps
t_{RBIT}	Unit interval	3-Byte Mode 4-Byte Mode 5-Byte Mode	392 294 294	500 500 500	ps ps ps
t_A	Jitter Margin		0.25		UI
t_B	Rise / Fall Time		0.05		UI
t_{EYE}	Differential Data Eye		0.5		UI
t_{skew_intra}	Allowable intra-pair skew		0.3	5-	UI
t_{skew_inter}	Allowable Inter-pair Skew			5	UI
fo_{skew_inter}	Allowable Inter-pair frequency offset		–300	300	ppm
T_j	Total jitter		-	0.5	UI
R_j	Random jitter	10^12 UI	-	0.2	UI
D_j_ISI	Deterministic jitter (ISI)		-	0.2	UI
S_j	Sinusoidal jitter		-	0.1	UI

(1) V-by-One high-speed technology supports 1, 2, 4 or 8 lane operation, in addition to 3-Byte, 4-Byte, and 5-Byte transfer modes
(2) Pixel repeat is a method used to support slower clock rate sources, whereby, the source come at twice the original clock rate, with each data pixel being repeated once, and blanking being doubled as well. This method must operate external to DLPC7540. Once received, the DLPC7540 discards each duplicate data pixel and blanking clock. Pixel repeat is supported only during 1- lane operation.
(3) For V-by-One high-speed technology, both link clock rate and link transfer rate limits must be met for any source.

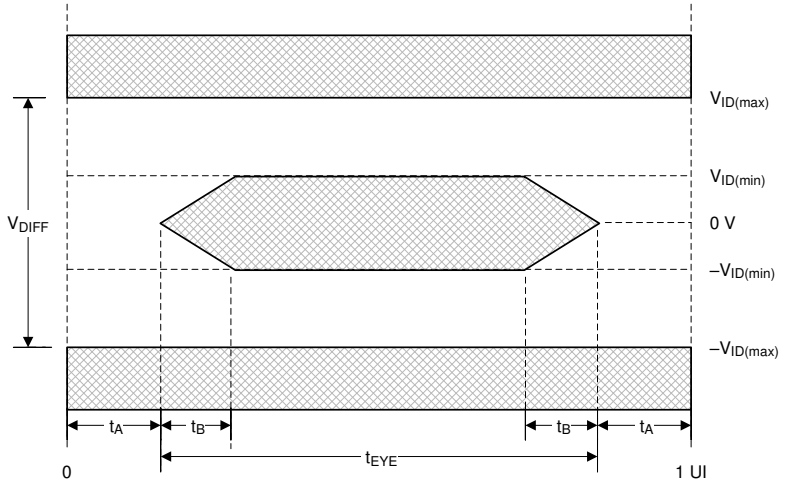


Figure 6-12. V-by-One Timing

6.17 FPD-Link Interface General Timing Requirements

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, FPDA_CLK_P/N, FPDB_CLK_P/N		20.0 (1 port) 10 (1 port with pixel repeat) (1)	330 (165 per port)	MHz
t_{clock}	Clock period, FPDA_CLK_P/N, FPDB_CLK_P/N		3.03 (6.06 per port)	50 (1 port) 100 (1 port with pixel repeat) (1)	ns
t_{RBIT}	Unit Interval (Figure 6-13)		0.865 (per port)	7.143 (1 port)	ns
t_{skew_ports}	Clock to clock skew margin between ports on same Controller, and between ports on different Controllers			1	clocks
t_A	Jitter Margin and Skew Margin between clock and data (on the same port). See Figure 6-14	f_{clock} ≤ 90 MHz		0.25	UI
		f_{clock} > 90 MHz		0.23	UI
t_B	Rise/Fall Time. See Figure 6-14	f_{clock} ≤ 90 MHz		333	ps
		f_{clock} > 90 MHz		200	ps
t_{EYE}	Differential Data Eye (Figure 6-14)	f_{clock} ≤ 90 MHz		0.50	UI
		f_{clock} > 90 MHz		0.54	UI

(1) Pixel repeat is a method used to support slower clock rate sources, whereby, the source come at twice the "original" clock rate, with each data pixel being repeated once, and blanking being doubled. Both the pixel doubling and double blanking must be done external to DLPC7540. The DLPC7540 discards each duplicate data pixel and blanking clock. The device supports pixel repeat only when using 1 port.

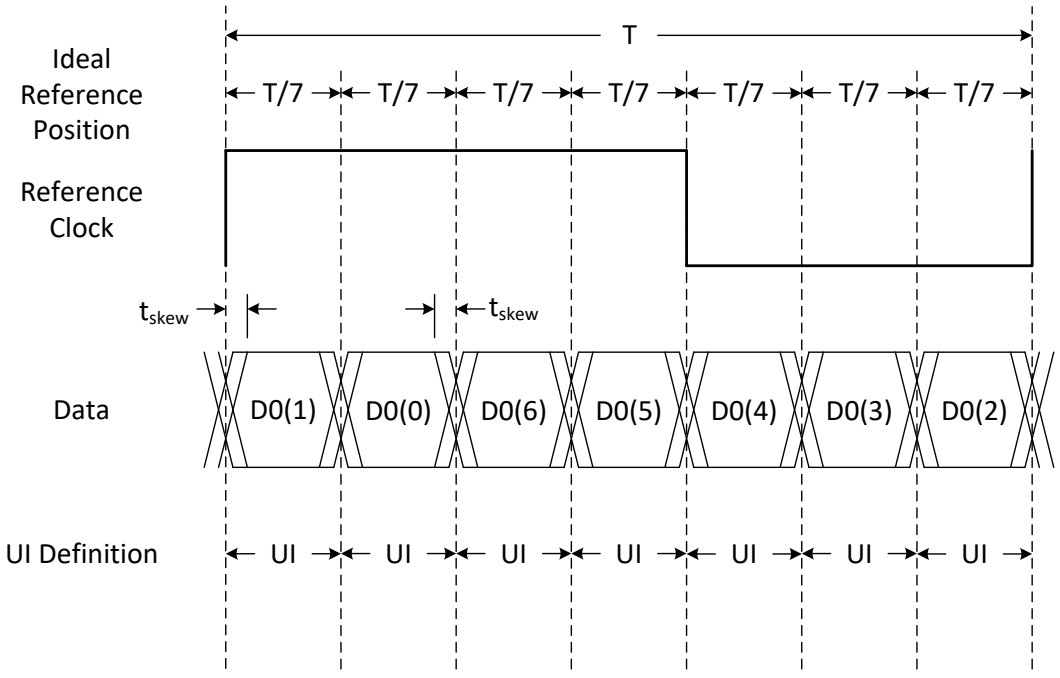


Figure 6-13. FPD-Link Data Skew

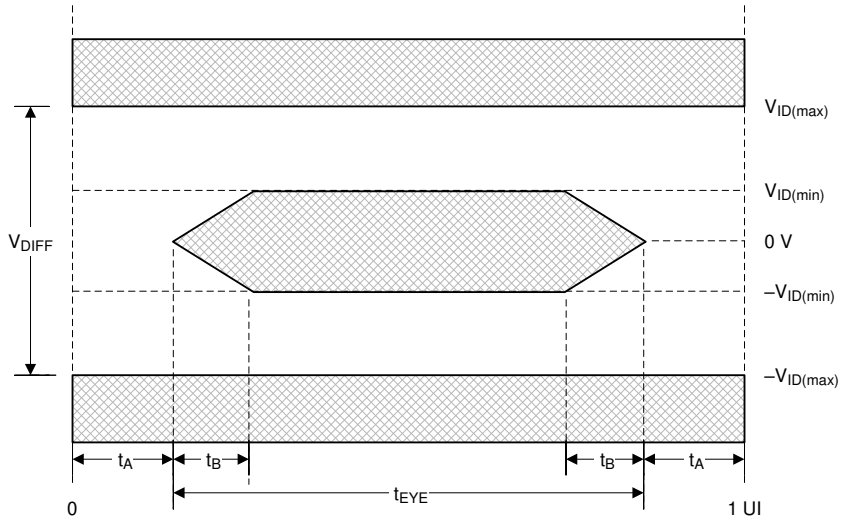


Figure 6-14. FPD-Link Timing

6.18 Source Frame Timing Requirements

See Figure 6-15

PARAMETER (1)			MIN	MAX	UNIT
t_{p_vsw}	VSYNC Active Pulse Width	50% reference points	1	127	lines
t_{p_vbp}	Vertical back porch (VBP) (2)	50% reference points	2 (3)		lines
t_{p_vfp}	Vertical front porch (VFP) (2)	50% reference points	MAX[(TVB_{MIN} - 65), 1] (3)		lines
t_{p_tvb}	Total vertical blanking (TVB) (2)	50% reference points	See (4)		lines
t_{p_hsw}	HSYNC Active Pulse Width	50% reference points	16		PCLKs
t_{p_hbp}	Horizontal back porch (HBP) (5)	50% reference points	5 (Digital Video Sources) 65 (Analog Video Sources)		PCLKs
t_{p_hfp}	Horizontal front porch (HFP) (5)	50% reference points	2		PCLKs
t_{p_thb}	Total horizontal blanking (THB) (5)	50% reference points	20 (Digital Video Sources) 80 (Analog Video Sources) (6)		PCLKs
f_{line}	Horizontal line rate		37.354		K Hz
APPL	Active Pixels per Line		640	4096	Pixels
ALPF	Active Lines per Frame		480	2400 (Low latency) 2160 (Normal)	Lines

(1) The requirements in the table apply to all external sources
(2) Vertical Blanking Parameter Definitions:
  a. Vertical Back Porch: Time from the leading edge of VSYNC to the leading edge of HSYNC for the first active line, and includes the VSYNC pulse width t_{p_vsw}.
  b. Vertical Front Porch: Time from the leading edge of HSYNC following the last active line in a frame to the leading edge of VSYNC
  c. Total Vertical Blanking: The sum of VBP + VFP = TVB.
(3) The vertical blanking required (per TVB) can be allocated as desired as long as the VFP and VBP minimum values are met.
(4) The minimum TVB can be calculated using the following:
TVBmin = 11 + ROUNDUP(LLS_VFP_MIN × (Source_ALPF/VPS_ALPF)), where:
  a. LLS_VFP_MIN (Normal Mode) = 22
  b. Source_ALPF = Active Lines Per Frame of the incoming source
  c. VPS_ALPF = 1080 (for 1920x1080 Native products and 3840x2160 4-way XPR products)
  d. Less TVBmin blanking can be required depending on the video processing being done. The configurations that drive the worst case minimum value are those configurations that combine the maximum (or near maximum) capabilities of functions such as scaling, warping, and keystone correction.
  e. This is applicable to all sources (Section 7.4). Other sources require directed testing in the end application.
  f. The minimum recommended TVB with CVT 1.2 sources is 23.
(5) Horizontal Blanking Parameter Definitions:
  a. Horizontal Back Porch: Time from the leading edge of HSYNC to the rising edge of DATEN, and includes the HSYNC pulse width t_{p_hsw}.
  b. Horizontal Front Porch: Time from the falling edge of DATEN to the leading edge of HSYNC.
  c. Total Horizontal Blanking: The sum of HBP + HFP = THB.
(6) The horizontal blanking required (per THB) can be allocated as desired as long as the HFP and HBP minimum values are met.

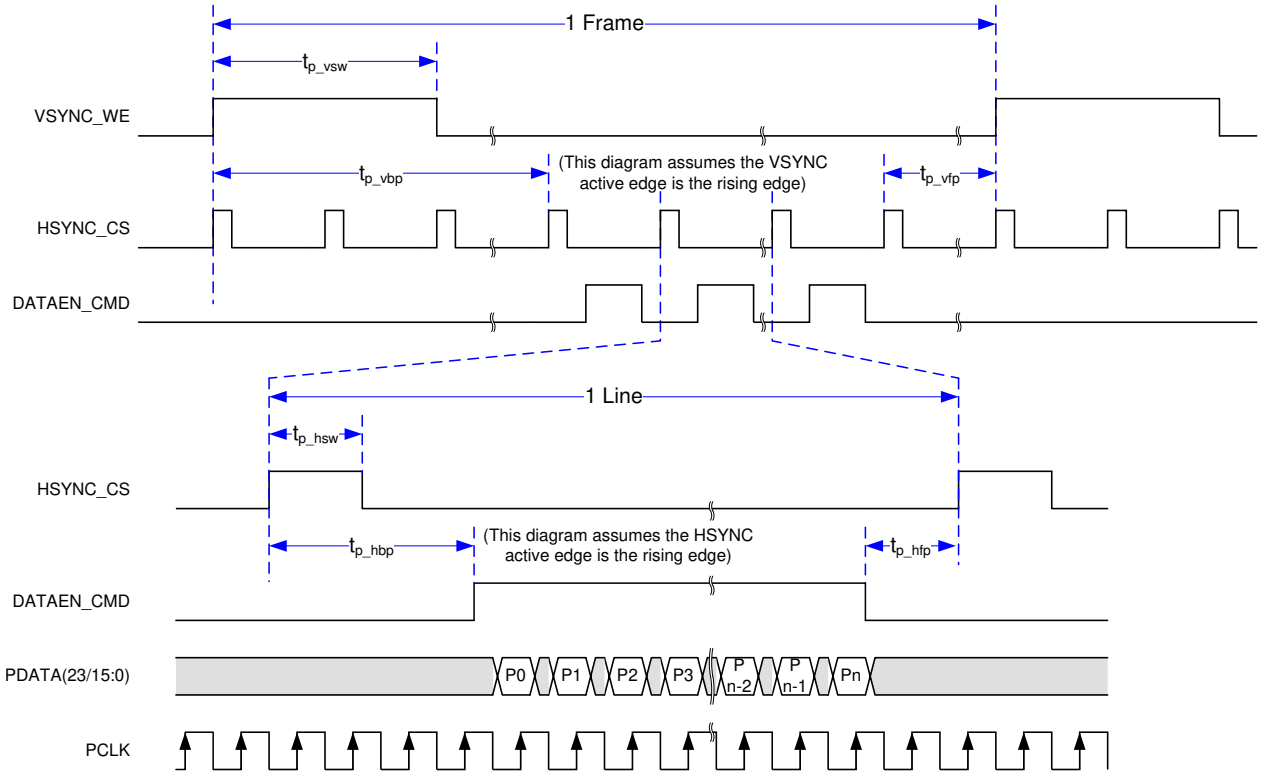


Figure 6-15. Source Frame Timing

6.19 Synchronous Serial Port Interface Timing Requirements

For SSP0, SSP1 and SSP2[1][2]

PARAMETER			MIN	MAX	UNIT
SSP Master					
f_{clock}	Clock frequency, SSPx_CLK	50% to 50% reference points	0.38	39.0	MHz
t_{clock}	Clock Period, SSPx_CLK	50% to 50% reference points	25.6	3632	ns
$t_{w(L)}$	Pulse duration low, SSPx_CLK	50% to 50% reference points	12.0		ns
$t_{w(H)}$	Pulse duration high, SSPx_CLK	50% to 50% reference points	12.0		ns
t_{delay}	Output Delay – SSPx_TXD (MOSI)		-2.5	2.5	ns
t_{su}	Setup time – SSPx_RXD (MISO)	50% to 50% reference points	15.0		ns
t_h	hold time – SSPx_RXD (MISO)	50% to 50% reference points	0		ns
t_t	Transition time (t_r and t_f- SSPx_RXD	20% to 80% reference points		1.5	ns
t_{clkjit}	Clock Jitter, SSPx_CLK			300	ps
$t_{delay\Delta}$	Clock output delay Δ { | $t_{w(H)}$ - $t_{w(L)}$ | }			500	ps
SSP Slave					
t_{delay}	Output Delay – SSPx_TXD (MOSI)		0	15	ns
t_{su}	Setup time – SSPx_RXD (MISO)	50% to 50% reference points	2.5		ns
t_h	hold time – SSPx_RXD (MISO)	50% to 50% reference points	2.5		ns

(1) The DLPC7540 SPI interfaces support SPI Modes 0, 1, 2, and 3 (that is, both clock polarities and both clock phases) as shown in Table 6-2 and Figure 6-16. As such, each SPI interface configuration must be setup to match the SPI mode being used.

(2) In most SPI applications, one clock edge is used by both master and slave devices for transmitting data while the other edge is use by both for sampling received data. This is referred to as *Standard SPI Protocol*. To maximize the SPI_CLK frequency potential, SPI masters can alternatively be designed to sample the data in (MISO) bit on the same clock edge used to transmit the next data out (MOSI) bit. This is referred to as *Enhanced SPI Protocol*. The DLPC7540 SPI master implementation supports both protocols (part of SPI interface configuration), however, to be able to use the "Enhanced SPI Protocol", the slave device must meet the requirement shown in Figure 6-17.

Table 6-2. SPI Clocking Modes

SPI Clocking Mode	SPI Clock Polarity	SPI Clock Phase
0	0	0
1	0	1
2	1	0
3	1	1

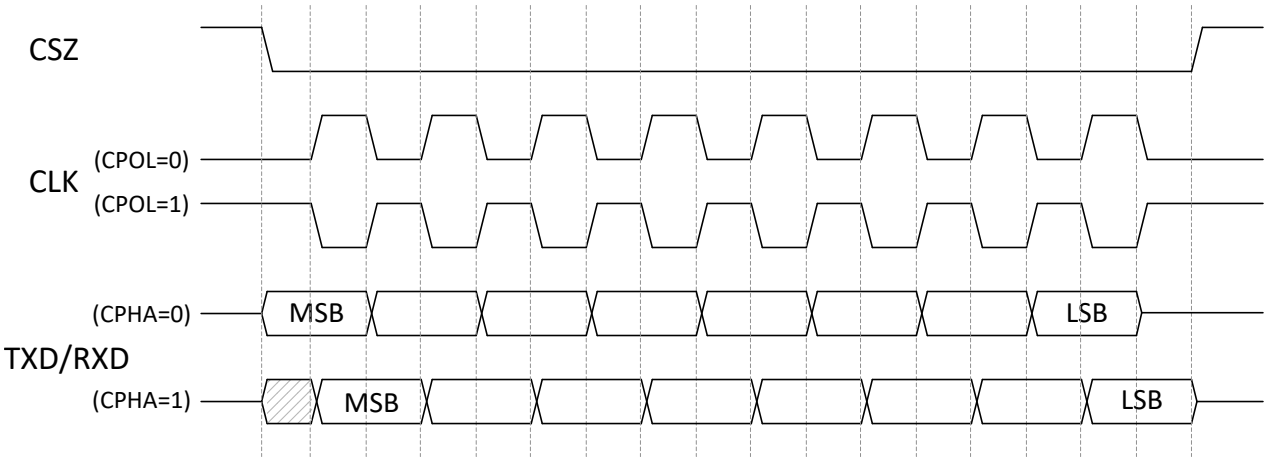


Figure 6-16. Timing Diagram for SPI Clocking Modes

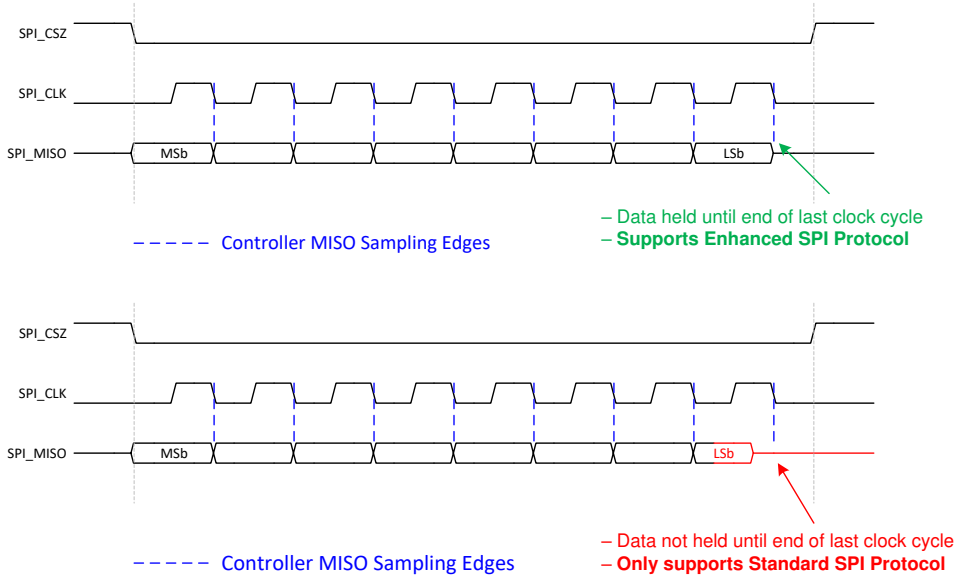


Figure 6-17. Requirement for Enhanced SPI Protocol

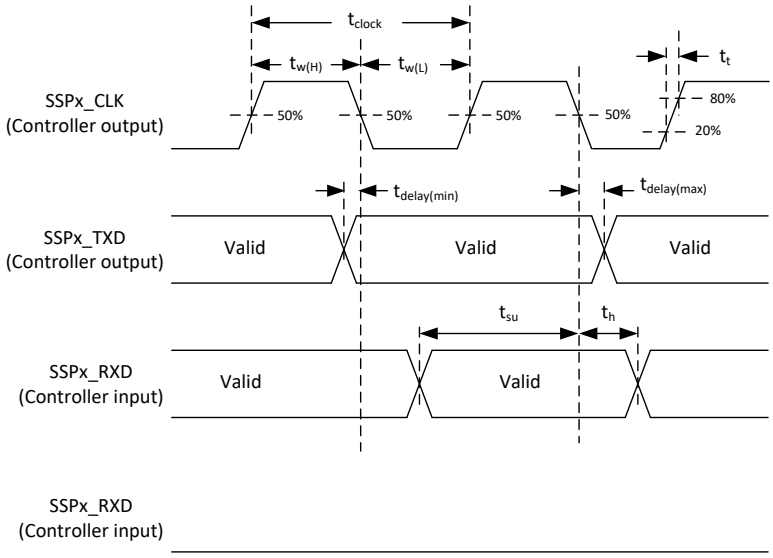


Figure 6-18. Timing Diagram for SSP Master (Modes 0/3)

6.20 Master and Slave I²C Interface Timing Requirements

For IIC0, IIC1 and IIC2

PARAMETER(1)			MIN	MAX	UNIT
f_{clock}	Clock frequency, IICx_SCL (2) (50% reference points)	Full speed		400	kHz
		Standard mode		100	kHz
C_L	Capacitive Load (for each bus line)			200	pF

(1) Meets all I²C timing per the I²C Bus Specification (except for capacitive loading as specified). For reference see Version 2.1 of the Phillips-NXP specification.
(2) By definition, I²C transactions operate at the speed of the slowest device on the bus. Full Speed operation requires all other I²C devices on the bus support Full Speed operation. The length of the line (due to its capacitance), as well as the value of the I²C pullup resistors can reduce the obtainable clock rate.

6.21 Programmable Output Clock Timing Requirements

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKA (1)	0.19	48.75	MHz
t_{clock}	Clock period, OCLKA	20.52	5263.15	ns
$t_{w(H)}$	Pulse duration high, OCLKA (50% reference points)	(t_{clock}/2) - 2		ns
$t_{w(L)}$	Pulse duration low, OCLKA (50% reference points)	(t_{clock}/2) - 2		ns
$t_{cclkjit}$	Jitter, OCLKA		200	ps
f_{clock}	Clock frequency, OCLKB (1)	0.19	48.75	MHz
t_{clock}	Clock period, OCLKB	20.52	5263.15	ns
$t_{w(H)}$	Pulse duration high, OCLKB (50% reference points)	(t_{clock}/2) - 2		ns
$t_{w(L)}$	Pulse duration low, OCLKB (50% reference points)	(t_{clock}/2) - 2		ns
$t_{cclkjit}$	Jitter, OCLKB		200	ps
f_{clock}	Clock frequency, OCLKC (1)	0.19	48.75	MHz
t_{clock}	Clock period, OCLKC	20.52	5263.15	ns
$t_{w(H)}$	Pulse duration high, OCLKC (50% reference points)	(t_{clock}/2) - 2		ns
$t_{w(L)}$	Pulse duration low, OCLKC (50% reference points)	(t_{clock}/2) - 2		ns
$t_{cclkjit}$	Jitter, OCLKC		200	ps
f_{clock}	Clock frequency, OCLKD (1)	0.19	48.75	MHz
t_{clock}	Clock period, OCLKD	20.52	5263.15	ns
$t_{w(H)}$	Pulse duration high, OCLKD (50% reference points)	(t_{clock}/2) - 2		ns
$t_{w(L)}$	Pulse duration low, OCLKD (50% reference points)	(t_{clock}/2) - 2		ns
$t_{cclkjit}$	Jitter, OCLKD		200	ps

(1) a. OCLKA is a dedicated pin, while OCLKB thru OCLKD are available via GPIO as alternate functions.
b. The frequency of OCLKA thru OCLKD is programmable, with each having a power-up default frequency of 0.77 MHz. This default frequency is not that meaningful for OCLKB thru OCLKD since they must be configured to their alternate GPIO function before they can be used as a clock output.

6.22 JTAG Boundary Scan Interface Timing Requirements (Debug Only)

See Figure 6-19

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			20	MHz
t_{clock}	Clock period, TCK		50		ns
$t_{w(H)}$	Pulse duration low, TCK	50% reference points	23		ns
$t_{w(L)}$	Pulse duration high, TCK	50% reference points		27	ns
t_s	Setup time – TDI valid before TCK↑	50% reference points	10		ns
t_h	Hold time – TDI valid after TCK↑	50% reference points	10		ns
t_s	Setup time – TMS1 valid before TCK↑	50% reference points	10		ns
t_h	Hold time – TMS1 valid after TCK↑	50% reference points	10		ns
t_t	Transition time (t_r and t_f	20% to 80% reference points		3	ns
t_{delay}	Output delay, TCK↓ to TDO1	60pF load	0	15	ns

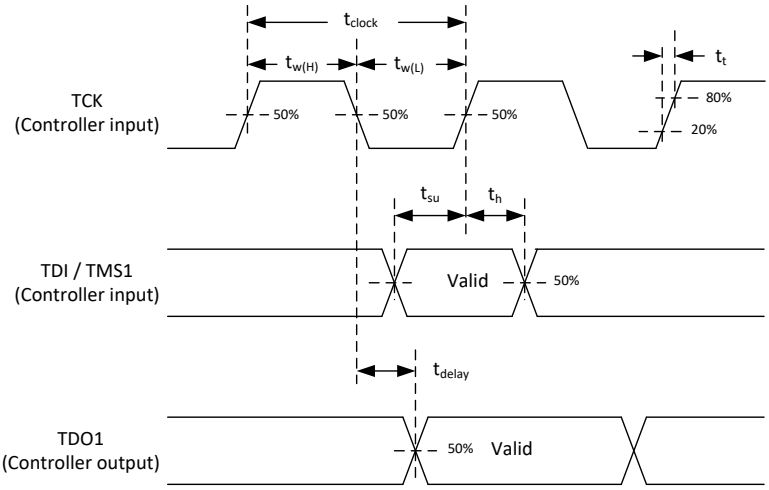


Figure 6-19. Timing Diagram for JTAG Boundary Scan

6.23 JTAG ARM Multi-Ice Interface Timing Requirements (Debug Only)

See Figure 6-20

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			8.33	MHz
t_{clock}	Clock period, TCK		120		ns
$t_{w(H)}$	Pulse duration low, TCK	50% reference points	50		ns
$t_{w(L)}$	Pulse duration high, TCK	50% reference points	50		ns
t_s	Setup time – TDI valid before TCK↑	50% reference points	15		ns
t_h	Hold time – TDI valid after TCK↑	50% reference points	15		ns
t_s	Setup time – TMS2 valid before TCK↑	50% reference points	15		ns
t_h	Hold time – TMS2 valid after TCK↑	50% reference points	15		ns
t_t	Transition time (t_r and t_f	20% to 80% reference points		5	ns
t_{delay}	Output delay, TCK↓ to TDO2		0	15	ps

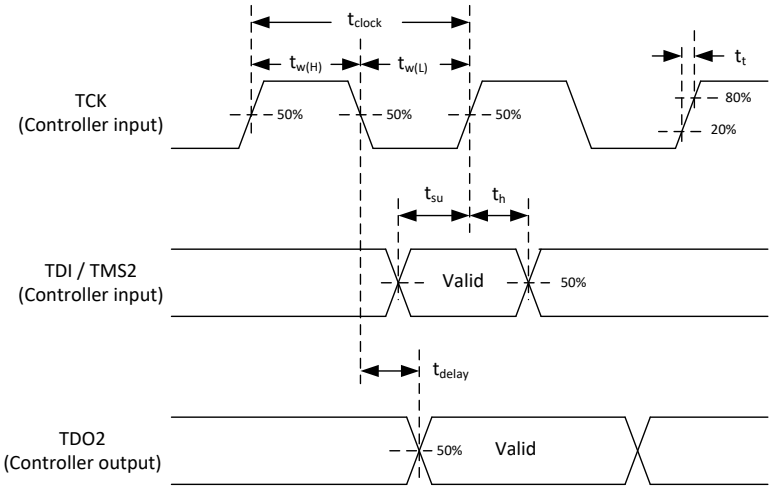


Figure 6-20. Timing Diagram for JTAG ARM Multi-Ice

6.24 Multi-Trace ETM Interface Timing Requirements

See Figure 6-21

PARAMETER(1)			MIN	MAX	UNIT
f_{clock}	Clock frequency, ETM_TRACECLK			41.56	MHz
t_{clock}	Clock period, ETM_TRACECLK		24.1		ns
$t_{w(H)}$	Pulse duration low, ETM_TRACECLK	50% reference points	11.2		ns
$t_{w(L)}$	Pulse duration high, ETM_TRACECLK	50% reference points	11.2		ns
t_{delay}	Output delay, ETM_TRACECLK↑ to "ETM_OUTPUTS" (2)		3.0	9.0	ps
t_{delay}	Output delay, ETM_TRACECLK↓ to "ETM_OUTPUTS" (2)		3.0	9.0	ps

(1) The trace interface is a source synchronous DDR interface. TRACE_CLK has a programmable delay to provide for centering its edges in the center of the trace data to optimize performance.
(2) "ETM_OUTPUTS" are: TSTPT_(7:0) and ETM_TRACECTL

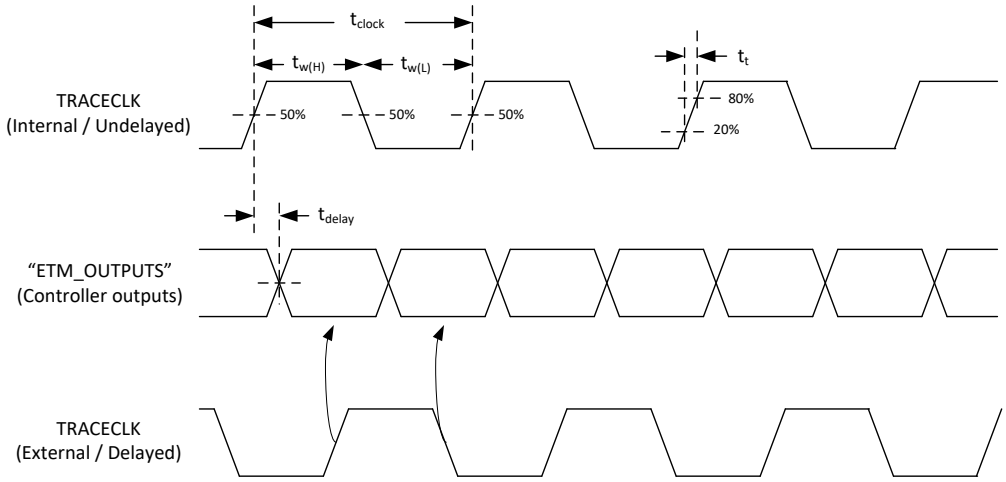


Figure 6-21. Timing Diagram for Multi-Trace ETM

7 Detailed Description

7.1 Overview

The DLPC7540 is DLP Products high resolution DMD controller. When coupled with the DLP471TE DMD or the DLP650TE DMD and DLPA100 power and motor controller, it enables low cost, high brightness 4K UHD displays. The DLPC7540 supports 4K UHD video up to 60Hz, as well as 1080p video up to 240Hz and 3D at 120Hz. Input formats include RBG, YCbCr and ICtCp (HDR10). Advanced video and color processing includes HDR10, improved linear light space processing, DynamicBlack, frame rate conversion, and a full parametric surface warping engine. It accepts 10-bit VbyOne, FPD-link. The DLPA100 has full illumination controls for LED, laser phosphor, RGB laser and hybrid illumination. Also, includes the memory bus for Flash storage. Control interfaces include SPI, I2C, UART, JTAG and USB2.0 OTG.

7.2 Functional Block Diagram

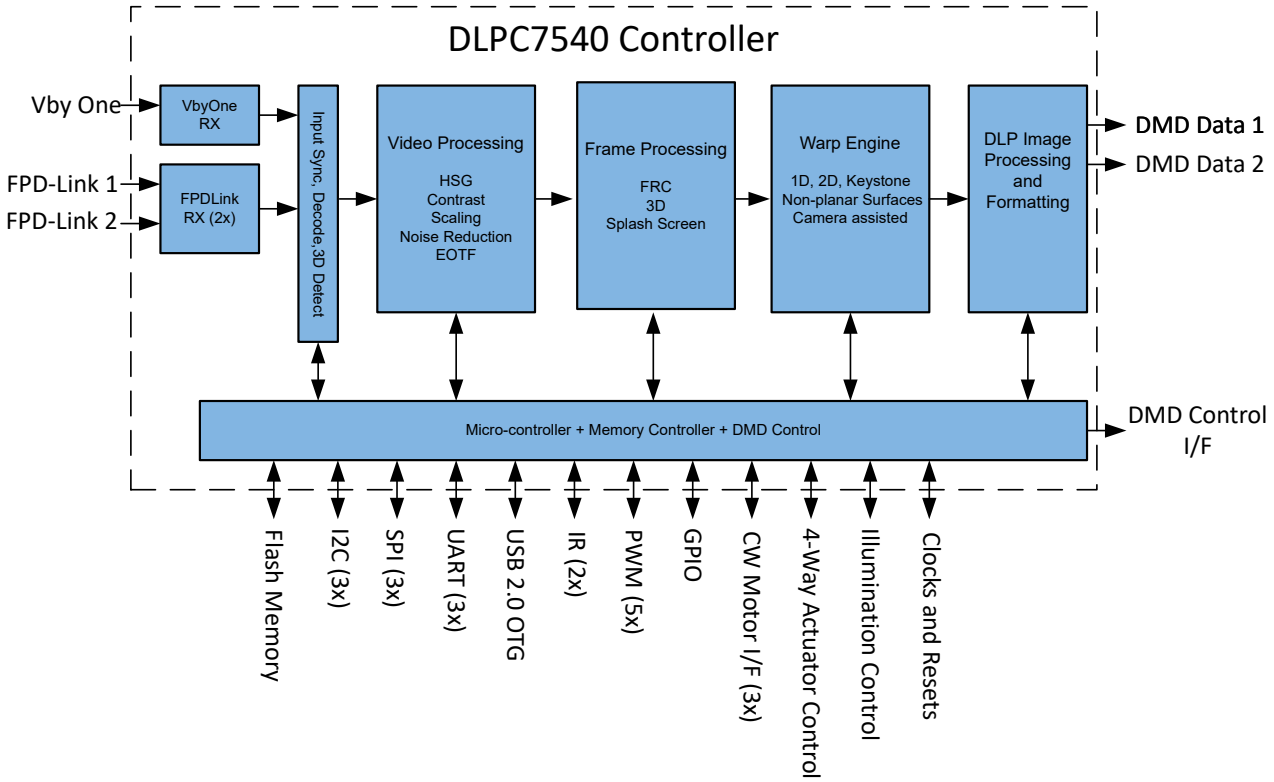


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Input Sources

Table 7-1. Supported Input Source Parameters (1)

INTERFACE	Bits/Pixel Accepted (Max)	Bits/Pixel Processed (Max)	Source Resolution: 2D		Source Resolution: 3D (per Eye) (2) (3)
			Min	Max	Max
FPD-Link	10	10	See (4)	3840 × 2160	3840 × 2160 (FS) 3840 × 2160 (VP) 1024x1200(HPH)
V-by-One	12	10	See (5)	3840 × 2160	3840 × 2160 (FS) 3840 × 2160 (VP) 1024x1200(HPH)

(1) The user must ensure that the resolution desired for a specific interface (e.g. FPD-Link) is within the bandwidth limits for that interface. Some resolutions at standard vertical rates (e.g. 60 Hz) may not be viable for all interfaces.
(2) FS = Frame Sequential (Full Resolution), VP = Vertically Packed (Full Resolution), HPH = Horizontally Packed (Half Resolution).
(3) Using the Low Latency configuration, only frame sequential 3D sources are supported, which can be supported in only one of two ways (since the Warp block is disabled when using the Low latency configuration). These are:
- For low frame rate 3D sources (e.g. 48 Hz, 60 Hz per eye), the sequence must be used to increase the display rate up to a appropriate value (e.g. 144 Hz, 120 Hz per eye).
- For high frame rate 3D sources (e.g. 120 Hz per eye), the source is treated like a 2D source and just passed through, since the source is providing the appropriate display rate.

(4) The minimum clock rate for the FPD-Link interface limits the smallest resolution that can be supported by this interface.
(5) The minimum clock rate and link rate for the V-by-One interface, as well as Byte Mode, limits the smallest resolution that can be supported by this interface. This interface supports 3-Byte, 4-Byte, and 5-Byte modes.

7.3.2 Processing Delays

The DLPC7540 introduces a variable number of field/frame delays dependent on the source type and selected processing steps performed on the source. For optimum audio/video synchronization this delay must be matched in the audio path. The following tables define the various video delay scenarios to aid in audio matching.

Because the input and output rates are different when frame rate conversion (FRC) is employed, the delay through the FRC is variable.

7.3.3 FPD-Link Interface

The DLPC7540 supports two FPD-Link 5 lane ports which can be configured for single port use (Port A or Port B), or for dual port use (Port A and Port B). The third FPD port (Port C) is reserved for parallel port use only. FPD ports A and B support a limited set of remapping options within each port, but there is no remapping between ports. When utilizing this feature, each unique lane pair can only be mapped to one unique destination lane pair, and Intra-lane remapping (i.e. swapping P with N) is not supported. In addition, the A and B ports can be swapped. Lane and port remapping (specified in flash) can help with board layout as needed. The typical lane mapping is shown in Figure 7-2. An example of an alternate lane mapping is shown in Figure 7-3. The specific intra port remapping options available are shown in Table 7-2.

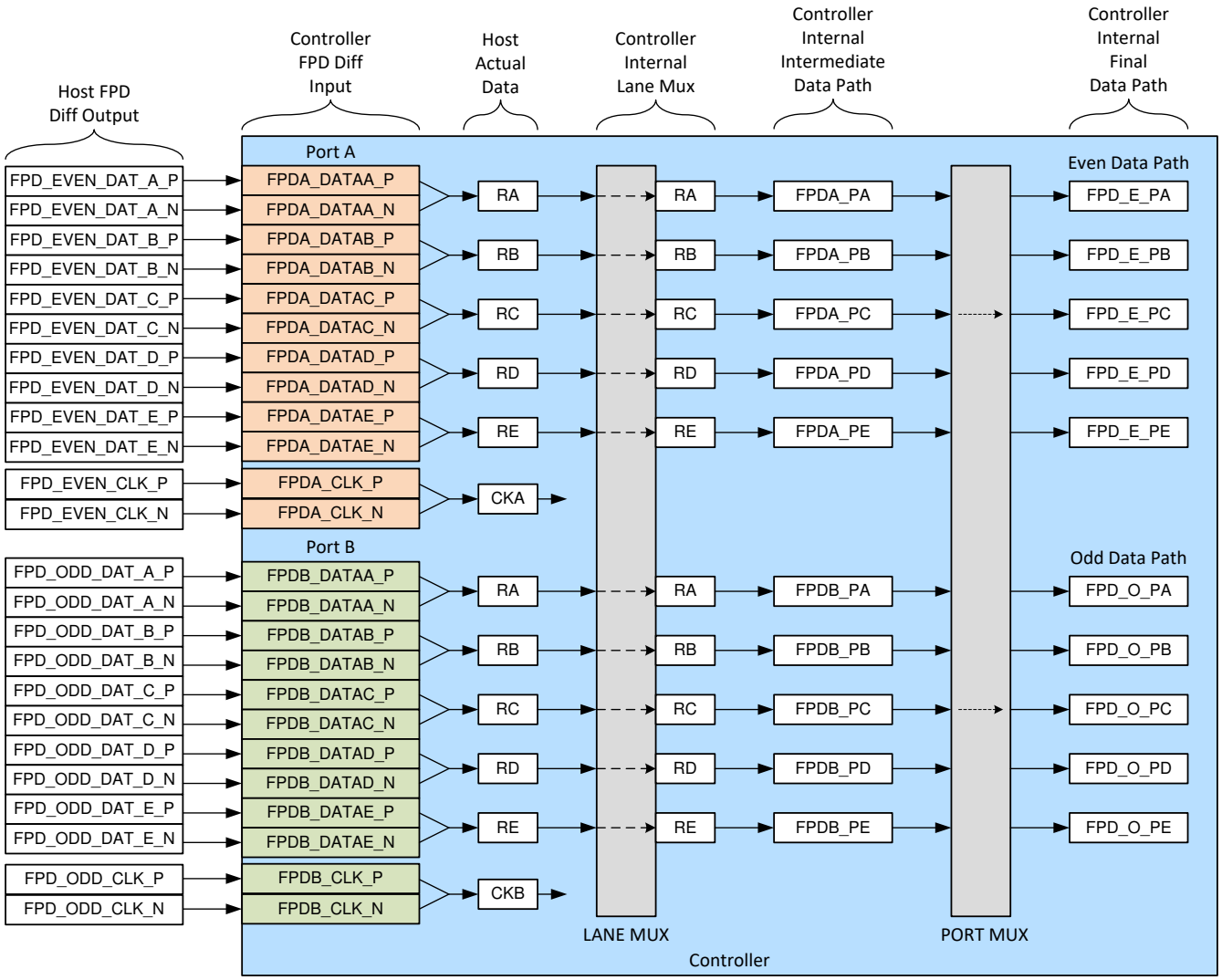


Figure 7-2. Example of Typical FPD-Link Port Lane Mapping

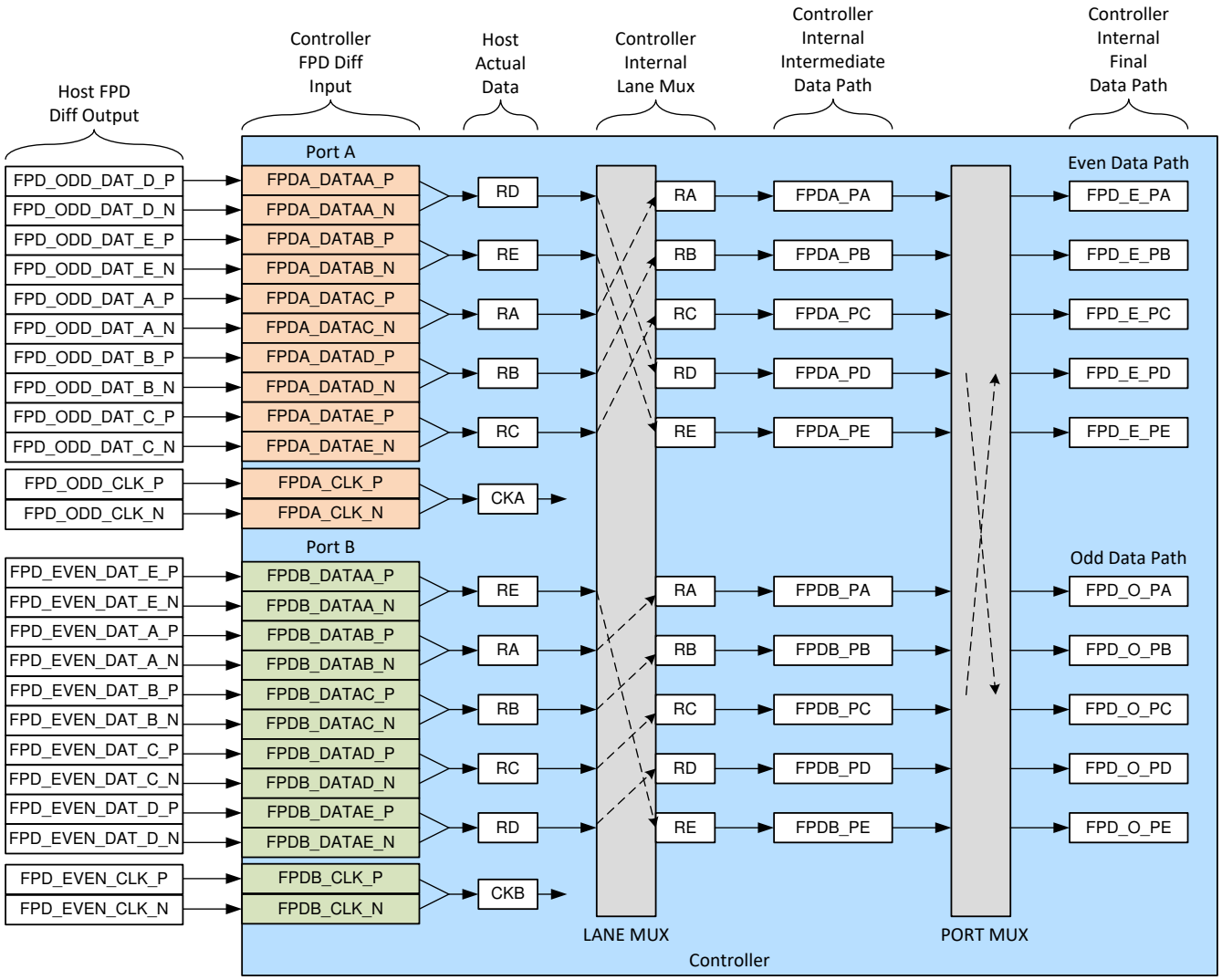


Figure 7-3. Example of Alternate FPD-Link Port Lane Mapping

Table 7-2. FPD-Link Intra Port Data Mapping Options

Mapping Options for Ports A & B	Input Data Port	Internal Final Data Path
0	FPDx_DATAA_P/N	FPD_x_PA
1	FPDx_DATAB_P/N	FPD_x_PA
2	FPDx_DATAC_P/N	FPD_x_PA
3	FPDx_DATAD_P/N	FPD_x_PA
4	FPDx_DATAE_P/N	FPD_x_PA
4	FPDx_DATAA_P/N	FPD_x_PB
0	FPDx_DATAB_P/N	FPD_x_PB
1	FPDx_DATAC_P/N	FPD_x_PB
2	FPDx_DATAD_P/N	FPD_x_PB
3	FPDx_DATAE_P/N	FPD_x_PB
3	FPDx_DATAA_P/N	FPD_x_PC
4	FPDx_DATAB_P/N	FPD_x_PC
0	FPDx_DATAC_P/N	FPD_x_PC
1	FPDx_DATAD_P/N	FPD_x_PC
2	FPDx_DATAE_P/N	FPD_x_PC
2	FPDx_DATAA_P/N	FPD_x_PD
3	FPDx_DATAB_P/N	FPD_x_PD
4	FPDx_DATAC_P/N	FPD_x_PD
0	FPDx_DATAD_P/N	FPD_x_PD
1	FPDx_DATAE_P/N	FPD_x_PD
1	FPDx_DATAA_P/N	FPD_x_PE
2	FPDx_DATAB_P/N	FPD_x_PE
3	FPDx_DATAC_P/N	FPD_x_PE
4	FPDx_DATAD_P/N	FPD_x_PE
0	FPDx_DATAE_P/N	FPD_x_PE

Independent from the remapping of the physical FPD interface, the DLPC7540 supports a number of data mappings onto the actual physical interface. There are three different 30-bit data mappings, and two different 24-bit data mappings supported. FPD sources must match at least one of these mappings These are shown in Table 7-3, Table 7-4, Table 7-5, Table 7-6, and Table 7-7.

Table 7-3. FPD-Link Data Mapping onto Physical Interface (30-bit Mode 0)

Bit Mapping - 30-bit Mode 0 (1) (30-bits per pixel)				
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**YCbCr 4:2:0**	**Mapper Output**
PA-6	G/Y[4]	Y[4]	Y00[4]	A(4)
PA-5	R/Cr[9]	Cb/Cr[9]	Cb/C00r[9]	B(9)
PA-4	R/Cr[8]	Cb/Cr[8]	Cb/Cr00[8]	B(8)
PA-3	R/Cr[7]	Cb/Cr[7]	Cb/Cr00[7]	B(7)
PA-2	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(6)
PA-1	R/Cr[5]	Cb/Cr[5]	Cb/Cr00[5]	B(5)
PA-0	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(4)
PB-6	B/Cb[5]	Unused	Y01[5]	C(5)
PB-5	B/Cb[4]	Unused	Y01[4]	C(4)
PB-4	G/Y[9]	Y[9]	Y00[9]	A(9)
PB-3	G/Y[8]	Y[8]	Y00[8]	A(8)
PB-2	G/Y[7]	Y[7]	Y00[7]	A(7)
PB-1	G/Y[6]	Y[6]	Y00[6]	A(6)
PB-0	G/Y[5]	Y[5]	Y00[5]	A(5)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[9]	Unused	Y01[9]	C(9)
PC-2	B/Cb[8]	Unused	Y01[8]	C(8)
PC-1	B/Cb[7]	Unused	Y01[7]	C(7)
PC-0	B/Cb[6]	Unused	Y01[6]	C(6)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[3]	Unused	Y01[3]	C(3)
PD-4	B/Cb[2]	Unused	Y01[2]	C(2)
PD-3	G/Y[3]	Y[3]	Y00[3]	A(3)
PD-2	G/Y[2]	Y[2]	Y00[2]	A(2)
PD-1	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(3)
PD-0	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(2)
PE-6	Field	Field	Field	Field
PE-5	B/Cb[1]	Unused	Y01[1]	C(1)
PE-4	B/Cb[0]	Unused	Y01[0]	C(0)
PE-3	G/Y[1]	Y[1]	Y00[1]	A(1)
PE-2	G/Y[0]	Y[0]	Y00[0]	A(0)
PE-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(1)
PE-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(0)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

Table 7-4. FPD-Link Data Mapping onto Physical Interface (30-bit Mode 1)

Bit Mapping - 30-bit Mode 1 (1) (30-bits per pixel)				
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**YCbCr 4:2:0**	**Mapper Output**
PA-6	G/Y[2]	Y[2]	Y00[2]	A(2)
PA-5	R/Cr[7]	Cb/Cr[7]	Cb/C00r[7]	B(7)
PA-4	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(6)
PA-3	R/Cr(5]	Cb/Cr[5]	Cb/Cr00[5]	B(5)
PA-2	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(4)
PA-1	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(3)
PA-0	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(2)
PB-6	B/Cb[3]	Unused	Y01[3]	C(3)
PB-5	B/Cb[2]	Unused	Y01[2]	C(2)
PB-4	G/Y[7]	Y[7]	Y00[7]	A(7)
PB-3	G/Y[6]	Y[6]	Y00[6]	A(6)
PB-2	G/Y[5]	Y[5]	Y00[5]	A(5)
PB-1	G/Y[4]	Y[4]	Y00[4]	A(4)
PB-0	G/Y[3]	Y[3]	Y00[3]	A(3)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[7]	Unused	Y01[7]	C(7)
PC-2	B/Cb[6]	Unused	Y01[6]	C(6)
PC-1	B/Cb[5]	Unused	Y01[5]	C(5)
PC-0	B/Cb[4]	Unused	Y01[4]	C(4)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[9]	Unused	Y01[9]	C(9)
PD-4	B/Cb[8]	Unused	Y01[8]	C(8)
PD-3	G/Y[9]	Y[9]	Y00[9]	A(9)
PD-2	G/Y[8]	Y[8]	Y00[8]	A(8)
PD-1	R/Cr[9]	Cb/Cr[9]	Cb/Cr00[9]	B(9)
PD-0	R/Cr[8]	Cb/Cr[8]	Cb/Cr00[8]	B(8)
PE-6	Field	Field	Field	Field
PE-5	B/Cb[1]	Unused	Y01[1]	C(1)
PE-4	B/Cb[0]	Unused	Y01[0]	C(0)
PE-3	G/Y[1]	Y[1]	Y00[1]	A(1)
PE-2	G/Y[0]	Y[0]	Y00[0]	A(0)
PE-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(1)
PE-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(0)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

Table 7-5. FPD-Link Data Mapping onto Physical Interface (30-bit Mode 2)

Bit Mapping - 30-bit Mode 2 (1) (30-bits per pixel)				
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**YCbCr 4:2:0**	**Mapper Output**
PA-6	G/Y[0]	Y[0]	Y00[0]	A(0)
PA-5	R/Cr[5]	Cb/Cr[5]	Cb/C00r[5]	B(5)
PA-4	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(4)
PA-3	R/Cr(3]	Cb/Cr[3]	Cb/Cr00[3]	B(3)
PA-2	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(2)
PA-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(1)
PA-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(0)
PB-6	B/Cb[1]	Unused	Y01[1]	C(1)
PB-5	B/Cb[0]	Unused	Y01[0]	C(0)
PB-4	G/Y[5]	Y[5]	Y00[5]	A(5)
PB-3	G/Y[4]	Y[4]	Y00[4]	A(4)
PB-2	G/Y[3]	Y[3]	Y00[3]	A(3)
PB-1	G/Y[2]	Y[2]	Y00[2]	A(2)
PB-0	G/Y[1]	Y[1]	Y00[1]	A(1)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[5]	Unused	Y01[5]	C(5)
PC-2	B/Cb[4]	Unused	Y01[4]	C(4)
PC-1	B/Cb[3]	Unused	Y01[3]	C(3)
PC-0	B/Cb[2]	Unused	Y01[2]	C(2)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[7]	Unused	Y01[7]	C(7)
PD-4	B/Cb[6]	Unused	Y01[6]	C(6)
PD-3	G/Y[7]	Y[7]	Y00[7]	A(7)
PD-2	G/Y[6]	Y[6]	Y00[6]	A(6)
PD-1	R/Cr[7]	Cb/Cr[7]	Cb/Cr00[7]	B(7)
PD-0	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(6)
PE-6	Field	Field	Field	Field
PE-5	B/Cb[9]	Unused	Y01[9]	C(9)
PE-4	B/Cb[8]	Unused	Y01[8]	C(8)
PE-3	G/Y[9]	Y[9]	Y00[9]	A(9)
PE-2	G/Y[8]	Y[8]	Y00[8]	A(8)
PE-1	R/Cr[9]	Cb/Cr[9]	Cb/Cr00[9]	B(9)
PE-0	R/Cr[8]	Cb/Cr[8]	Cb/Cr00[8]	B(8)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

Table 7-6. FPD-Link Data Mapping onto Physical Interface (24-bit Mode 0) (1)

Bit Mapping - 24-bit Mode 0 (2) (24-bits per pixel)				
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**YCbCr 4:2:0**	**Mapper Output**
PA-6	G/Y[0]	Y[0]	Y00[0]	A(2)
PA-5	R/Cr[5]	Cb/Cr[5]	Cb/C00r[5]	B(7)
PA-4	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(6)
PA-3	R/Cr(3]	Cb/Cr[3]	Cb/Cr00[3]	B(5)
PA-2	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(4)
PA-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(3)
PA-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(2)
PB-6	B/Cb[1]	Unused	Y01[1]	C(3)
PB-5	B/Cb[0]	Unused	Y01[0]	C(2)
PB-4	G/Y[5]	Y[5]	Y00[5]	A(7)
PB-3	G/Y[4]	Y[4]	Y00[4]	A(6)
PB-2	G/Y[3]	Y[3]	Y00[3]	A(5)
PB-1	G/Y[2]	Y[2]	Y00[2]	A(4)
PB-0	G/Y[1]	Y[1]	Y00[1]	A(3)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[5]	Unused	Y01[5]	C(7)
PC-2	B/Cb[4]	Unused	Y01[4]	C(6)
PC-1	B/Cb[3]	Unused	Y01[3]	C(5)
PC-0	B/Cb[2]	Unused	Y01[2]	C(4)
PD-6	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_Ref or Field
PD-5	B/Cb[7]	Unused	Y01[7]	C(9)
PD-4	B/Cb[6]	Unused	Y01[6]	C(8)
PD-3	G/Y[7]	Y[7]	Y00[7]	A(9)
PD-2	G/Y[6]	Y[6]	Y00[6]	A(8)
PD-1	R/Cr[7]	Cb/Cr[7]	Cb/Cr00[7]	B(9)
PD-0	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(8)
PE-6	Unused	Unused	Unused	Unused
PE-5	Unused	Unused	Unused	Unused
PE-4	Unused	Unused	Unused	Unused
PE-3	Unused	Unused	Unused	Unused
PE-2	Unused	Unused	Unused	Unused
PE-1	Unused	Unused	Unused	Unused
PE-0	Unused	Unused	Unused	Unused

(1) To support 24 bit data, the mapper shifts each 8-bit color up by 2 bits, and forces output bits A[1], A[0], B[1], B[0], C[1], and C[0] to value '0'.
(2) Input data bits are defined with bit[7] as the most significant bit, and bit[0] as the least significant bit.

Table 7-7. FPD-Link Data Mapping onto Physical Interface (24-bit Mode 1) (1)

Bit Mapping - 24-bit Mode 1 (2) (24-bits per pixel)				
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**YCbCr 4:2:0**	**Mapper Output**
PA-6	G/Y[2]	Y[2]	Y00{2}	A(4)
PA-5	R/Cr[7]	Cb/Cr[7]	Cb/C00r[7]	B(9)
PA-4	R/Cr[6]	Cb/Cr[6]	Cb/Cr00[6]	B(8)
PA-3	R/Cr(5]	Cb/Cr[5]	Cb/Cr00[5]	B(7)
PA-2	R/Cr[4]	Cb/Cr[4]	Cb/Cr00[4]	B(6)
PA-1	R/Cr[3]	Cb/Cr[3]	Cb/Cr00[3]	B(5)
PA-0	R/Cr[2]	Cb/Cr[2]	Cb/Cr00[2]	B(4)
PB-6	B/Cb[3]	Unused	Y01[3]	C(5)
PB-5	B/Cb[2]	Unused	Y01[2]	C(4)
PB-4	G/Y[7]	Y[7]	Y00[7]	A(9)
PB-3	G/Y[6]	Y[6]	Y00[6]	A(8)
PB-2	G/Y[5]	Y[5]	Y00[5]	A(7)
PB-1	G/Y[4]	Y[4]	Y00[4]	A(6)
PB-0	G/Y[3]	Y[3]	Y00[3]	A(5)
PC-6	Data En	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[7]	Unused	Y01[7]	C(9)
PC-2	B/Cb[6]	Unused	Y01[6]	C(8)
PC-1	B/Cb[5]	Unused	Y01[5]	C(7)
PC-0	B/Cb[4]	Unused	Y01[4]	C(6)
PD-6	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_Ref or Field
PD-5	B/Cb[1]	Unused	Y01[1]	C(3)
PD-4	B/Cb[0]	Unused	Y01[0]	C(2)
PD-3	G/Y[1]	Y[1]	Y00[1]	A(3)
PD-2	G/Y[0]	Y[0]	Y00[0]	A(2)
PD-1	R/Cr[1]	Cb/Cr[1]	Cb/Cr00[1]	B(3)
PD-0	R/Cr[0]	Cb/Cr[0]	Cb/Cr00[0]	B(2)
PE-6	Unused	Unused	Unused	Unused
PE-5	Unused	Unused	Unused	Unused
PE-4	Unused	Unused	Unused	Unused
PE-3	Unused	Unused	Unused	Unused
PE-2	Unused	Unused	Unused	Unused
PE-1	Unused	Unused	Unused	Unused
PE-0	Unused	Unused	Unused	Unused

(1) To support 24 bit data, the mapper shifts each 8-bit color up by 2 bits, and forces output bits A[1], A[0], B[1], B[0], C[1], and C[0] to value '0'.
(2) Input data bits are defined with bit[7] as the most significant bit, and bit[0] as the least significant bit.

7.3.4 V-by-One interface

The DLPC7540 Controller supports a single 8 lane V-by-One port which can be configured for 1, 2, 4 or 8 lane use. This interface supports limited lane remapping which is shown in . Intra-lane remapping (i.e. swapping P with N) is not supported.

Independent from the remapping of the physical V-by-One interface, the DLPC7540 supports a number of data mappings onto the actual physical interface as specified by the standard. V-by-One sources must match at least one of these mappings These are shown in Table 7-8, Table 7-9, Table 7-10, Table 7-11, Table 7-12, Table 7-13, Table 7-14, Table 7-15, Table 7-16, and Table 7-17.

Table 7-8. V-by-One Data Mapping for 36bpp/30bpp RGB/YCbCr 4:4:4

V-by-One Data Map Mode 0			
V-by-One Input Data Bit	**36bpp RGB/YCbCr 4:4:4 (1)**	**30bpp RGB/YCbCr 4:4:4**	**Mapper Output**
D[0]	R/Cr[4]	R/Cr[2]	B(2)
D[1]	R/Cr[5]	R/Cr[3]	B(3)
D[2]	R/Cr[6]	R/Cr[4]	B(4)
D[3]	R/Cr[7]	R/Cr(5]	B(5)
D[4]	R/Cr[8]	R/Cr[6]	B(6)
D[5]	R/Cr[9]	R/Cr[7]	B(7)
D[6]	R/Cr[10]	R/Cr[8]	B(8)
D[7]	R/Cr[11]	R/Cr[9]	B(9)
D[8]	G/Y[4]	G/Y[2]	A(2)
D[9]	G/Y[5]	G/Y[3]	A(3)
D[10]	G/Y[6]	G/Y[4]	A(4)
D[11]	G/Y[7]	G/Y[5]	A(5)
D[12]	G/Y[8]	G/Y[6]	A(6)
D[13]	G/Y[9]	G/Y[7]	A(7)
D[14]	G/Y[10]	G/Y[8]	A(8)
D[15]	G/Y[11]	G/Y[9]	A(9)
D[16]	B/Cb[4]	B/Cb[2]	C(2)
D[17]	B/Cb[5]	B/Cb[3]	C(3)
D[18]	B/Cb[6]	B/Cb[4]	C(4)
D[19]	B/Cb[7]	B/Cb[5]	C(5)
D[20]	B/Cb[8]	B/Cb[6]	C(6)
D[21]	B/Cb[9]	B/Cb[7]	C(7)
D[22]	B/Cb[10]	B/Cb[8]	C(8)
D[23]	B/Cb[11]	B/Cb[9]	C(9)
D[24]			
D[25]			
D[26]	B/Cb[2]	B/Cb[1]	C[0]
D[27]	B/Cb[3]	B/Cb[0]	C[1]
D[28]	G/Y[2]	G/Y[1]	A[0]
D[29]	G/Y[3]	G/Y[0]	A[1]
D[30]	R/Cr[2]	R/Cr[1]	B[0]
D[31]	R/Cr[3]	R/Cr[0]	B[1]

(1) For 36-bit inputs, the 12-bits per color truncates to 10-bits per color with the two least significant-bits per color being discarded.

Table 7-9. V-by-One Data Mapping for 27bpp RGB/YCbCr 4:4:4

V-by-One Data Map Mode 1		
V-by-One Input Data Bit	**27bpp RGB/YCbCr 4:4:4** (1)	**Mapper Output**
D[0]	R/Cr[1]	B(2)
D[1]	R/Cr[2]	B(3)
D[2]	R/Cr[3]	B(4)
D[3]	R/Cr[4]	B(5)
D[4]	R/Cr[5]	B(6)
D[5]	R/Cr[6]	B(7)
D[6]	R/Cr[7]	B(8)
D[7]	R/Cr[8]	B(9)
D[8]	G/Y[1]	A(2)
D[9]	G/Y[2]	A(3)
D[10]	G/Y[3]	A(4)
D[11]	G/Y[4]	A(5)
D[12]	G/Y[5]	A(6)
D[13]	G/Y[6]	A(7)
D[14]	G/Y[7]	A(8)
D[15]	G/Y[8]	A(9)
D[16]	B/Cb[1]	C(2)
D[17]	B/Cb[2]	C(3)
D[18]	B/Cb[3]	C(4)
D[19]	B/Cb[4]	C(5)
D[20]	B/Cb[5]	C(6)
D[21]	B/Cb[6]	C(7)
D[22]	B/Cb[7]	C(8)
D[23]	B/Cb[8]	C(9)
D[24]		
D[25]		
'0'	-	C[0]
D[27]	B/Cb[0]	C[1]
'0'	-	A[0]
D[29]	G/Y[0]	A[1]
'0'	-	B[0]
D[31]	R/Cr[0]	B[1]

(1) For 27-bit inputs, the 9-bits for each color shifts up one bit, and the least significant bit of each color is set to '0'.

Table 7-10. V-by-One Data Mapping for 24bpp RGB/YCbCr 4:4:4

V-by-One Data Map Mode 2		
V-by-One Input Data Bit	**24bpp RGB/YCbCr 4:4:4 (1)**	**Mapper Output**
D[0]	R/Cr[0]	B(2)
D[1]	R/Cr[1]	B(3)
D[2]	R/Cr[2]	B(4)
D[3]	R/Cr[3]	B(5)
D[4]	R/Cr[4]	B(6)
D[5]	R/Cr[5]	B(7)
D[6]	R/Cr[6]	B(8)
D[7]	R/Cr[7]	B(9)
D[8]	G/Y[0]	A(2)
D[9]	G/Y[1]	A(3)
D[10]	G/Y[2]	A(4)
D[11]	G/Y[3]	A(5)
D[12]	G/Y[4]	A(6)
D[13]	G/Y[5]	A(7)
D[14]	G/Y[6]	A(8)
D[15]	G/Y[7]	A(9)
D[16]	B/Cb[0]	C(2)
D[17]	B/Cb[1]	C(3)
D[18]	B/Cb[2]	C(4)
D[19]	B/Cb[3]	C(5)
D[20]	B/Cb[4]	C(6)
D[21]	B/Cb[5]	C(7)
D[22]	B/Cb[6]	C(8)
D[23]	B/Cb[7]	C(9)
D[24]		
D[25]		
'0'	-	C[0]
'0'	-	C[1]
'0'	-	A[0]
'0'	-	A[1]
'0'	-	B[0]
'0'	-	B[1]

(1) For 24-bit inputs, the 8-bits for each color shifts up two bits, and the two least significant bits of each color are set to '0'.

Table 7-11. V-by-One Data Mapping for 32bpp/24bpp/20bpp YCbCr 4:2:2 (1)

V-by-One Data Map Mode 3				
V-by-One Input Data Bit	**32bpp YCbCr 4:2:2 (2)**	**24bpp YCbCr 4:2:2 (3)**	**20bpp YCbCr 4:2:2**	**Mapper Output**
D[0]	CbCr[8]	CbCr[4]	CbCr[2]	B(2)
D[1]	CbCr[9]	CbCr[5]	CbCr[3]	B(3)
D[2]	CbCr[10]	CbCr[6]	CbCr[4]	B(4)
D[3]	CbCr[11]	CbCr[7]	CbCr[5]	B(5)
D[4]	CbCr[12]	CbCr[8]	CbCr[6]	B(6)
D[5]	CbCr[13]	CbCr[8]	CbCr[7]	B(7)
D[6]	CbCr[14]	CbCr[10]	CbCr[8]	B(8)
D[7]	CbCr[15]	CbCr[11]	CbCr[9]	B(9)
D[8]	Y[8]	Y[4]	Y[2]	A(2)
D[9]	Y[9]	Y[5]	Y[3]	A(3)
D[10]	Y[10]	Y[6]	Y[4]	A(4)
D[11]	Y[11]	Y[7]	Y[5]	A(5)
D[12]	Y[12]	Y[8]	Y[6]	A(6)
D[13]	Y[13]	Y[9]	Y[7]	A(7)
D[14]	Y[14]	Y[10]	Y[8]	A(8)
D[15]	Y[15]	Y[11]	Y[9]	A(9)
'0'	-	-	-	C(2)
'0'	-	-	-	C(3)
'0'	-	-	-	C(4)
'0'	-	-	-	C(5)
'0'	-	-	-	C(6)
'0'	-	-	-	C(7)
'0'	-	-	-	C(8)
'0'	-	-	-	C(9)
D[24]				
D[25]				
'0'	-	-	-	C[0]
'0'	-	-	-	C[1]
D[28]	Y[6]	Y[2]	Y[2]	A[0]
D[29]	Y[7]	Y[3]	Y[3]	A[1]
D[30]	CbCr[6]	CbCr[2]	CbCr[2]	B[0]
D[31]	CbCr[7]	CbCr[3]	CbCr[3]	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
(2) For 32-bit inputs, the 16-bits per color truncates to 10-bit per color, with the six least significant-bits per color discarded.
(3) For 24-bit inputs, the 12-bits per color truncates to 10-bit per color, with the two least significant-bits per color discarded.

Table 7-12. V-by-One Data Mapping for 18bpp YCbCr 4:2:2(1)

V-by-One Data Map Mode 4		
V-by-One Input Data Bit	**18bpp YCbCr 4:2:2 (2)**	**Mapper Output**
D[0]	CbCr[1]	B(2)
D[1]	CbCr[2]	B(3)
D[2]	CbCr[3]	B(4)
D[3]	CbCr[4]	B(5)
D[4]	CbCr[5]	B(6)
D[5]	CbCr[6]	B(7)
D[6]	CbCr[7]	B(8)
D[7]	CbCr[8]	B(9)
D[8]	Y[1]	A(2)
D[9]	Y[2]	A(3)
D[10]	Y[3]	A(4)
D[11]	Y[4]	A(5)
D[12]	Y[5]	A(6)
D[13]	Y[6]	A(7)
D[14]	Y[7]	A(8)
D[15]	Y[8]	A(9)
'0'	-	C(2)
'0'	-	C(3)
'0'	-	C(4)
'0'	-	C(5)
'0'	-	C(6)
'0'	-	C(7)
'0'	-	C(8)
'0'	-	C(9)
D[24]		
D[25]		
'0'	-	C[0]
'0'	-	C[1]
'0'	-	A[0]
D[29]	Y[0]	A[1]
'0'	-	B[0]
D[31]	CbCr[0]	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
(2) For 18-bit inputs, the 9-bits for each color shifts up one bit, and the least significant bits of each color is set to '0'.

Table 7-13. V-by-One Data Mapping for 16bpp YCbCr 4:2:2(1)

V-by-One Data Map Mode 5		
V-by-One Input Data Bit	**16bpp YCbCr 4:2:2 (2)**	**Mapper Output**
D[0]	CbCr[0]	B(2)
D[1]	CbCr[1]	B(3)
D[2]	CbCr[2]	B(4)
D[3]	CbCr[3]	B(5)
D[4]	CbCr[4]	B(6)
D[5]	CbCr[5]	B(7)
D[6]	CbCr[6]	B(8)
D[7]	CbCr[7]	B(9)
D[8]	Y[0]	A(2)
D[9]	Y[1]	A(3)
D[10]	Y[2]	A(4)
D[11]	Y[3]	A(5)
D[12]	Y[4]	A(6)
D[13]	Y[5]	A(7)
D[14]	Y[6]	A(8)
D[15]	Y[7]	A(9)
'0'	-	C(2)
'0'	-	C(3)
'0'	-	C(4)
'0'	-	C(5)
'0'	-	C(6)
'0'	-	C(7)
'0'	-	C(8)
'0'	-	C(9)
D[24]		
D[25]		
'0'	-	C[0]
'0'	-	C[1]
'0'	-	A[0]
'0'	-	A[1]
'0'	-	B[0]
'0'	-	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
(2) For 16-bit inputs, the 8-bits for each color shifts up one bit, and the least significant bit of each color is set to '0'.

Table 7-14. V-by-One Data Mapping Example for 12bpp/10bpp YCbCr 4:2:0(1)

V-by-One Data Map Mode 6					
V-by-One Input Data Bit	**12bpp YCbCr 4:2:0 Even Line(2)**	**12bpp YCbCr 4:2:0 Odd Line (2)**	**10bpp YCbCr 4:2:0 Even Line**	**10bpp YCbCr 4:2:0 Odd Line**	**Mapper Output**
D[0]	Y01[4]	Y01[4]	Y01[2]	Y11[2]	C(2)
D[1]	Y01[5]	Y01[5]	Y01[3]	Y11[3]	C(3)
D[2]	Y01[6]	Y01[6]	Y01[4]	Y11[4]	C(4)
D[3]	Y01[7]	Y01[7]	Y01[5]	Y11[5]	C(5)
D[4]	Y01[8]	Y01[8]	Y01[6]	Y11[6]	C(6)
D[5]	Y01[9]	Y01[9]	Y01[7]	Y11[7]	C(7)
D[6]	Y01[10]	Y01[10]	Y01[8]	Y11[8]	C(8)
D[7]	Y01[11]	Y01[11]	Y01[9]	Y11[9]	C(9)
D[8]	Y00[4]	Y00[4]	Y00[2]	Y10[2]	A(2)
D[9]	Y00[5]	Y00[5]	Y00[3]	Y10[3]	A(3)
D[10]	Y00[6]	Y00[6]	Y00[4]	Y10[4]	A(4)
D[11]	Y00[7]	Y00[7]	Y00[5]	Y10[5]	A(5)
D[12]	Y00[8]	Y00[8]	Y00[6]	Y10[6]	A(6)
D[13]	Y00[9]	Y00[9]	Y00[7]	Y10[7]	A(7)
D[14]	Y00[10]	Y00[10]	Y00[8]	Y10[8]	A(8)
D[15]	Y00[11]	Y00[11]	Y00[9]	Y10[9]	A(9)
D[16]	Cb00[4]	Cr00[4]	Cb00[2]	Cr00[2]	B(2)
D[17]	Cb00[5]	Cr00[5]	Cb00[3]	Cr00[3]	B(3)
D[18]	Cb00[6]	Cr00[6]	Cb00[4]	Cr00[4]	B(4)
D[19]	Cb00[7]	Cr00[7]	Cb00[5]	Cr00[5]	B(5)
D[20]	Cb00[8]	Cr00[8]	Cb00[6]	Cr00[6]	B(6)
D[21]	Cb00[9]	Cr00[9]	Cb00[7]	Cr00[7]	B(7)
D[22]	Cb00[10]	Cr00[10]	Cb00[8]	Cr00[8]	B(8)
D[23]	Cb00[11]	Cr00[11]	Cb00[9]	Cr00[9]	B(9)
D[24]					
D[25]					
D[26]	Cb00[2]	Cr00[2]	Cb00[0]	Cr00[0]	B[0]
D[27]	Cb00[3]	Cr00[3]	Cb00[1]	Cr00[1]	B[1]
D[28]	Y00[2]	Y10[2]	Y00[0]	Y10[0]	A[0]
D[29]	Y00[3]	Y10[3]	Y00[1]	Y10[1]	A[1]
D[30]	Y01[2]	Y11[2]	Y01[0]	Y11[0]	C[0]
D[31]	Y01[3]	Y11[3]	Y01[1]	Y11[1]	C[1]

(1) For all YCbCr 4:2:0 inputs, two consecutive pixel Luma values are brought in on each clock. Even lines carry the Cb values, and odd lines carry the Cr values.
(2) For 12bpp YCbCr 4:2:0 inputs, the 12-bits per color truncates to 10-bits per color with the two least significant-bits per color discarded.

Table 7-15. V-by-One Data Mapping Example for 8bpp YCbCr 4:2:0(1)

V-by-One Data Map Mode 7			
V-by-One Input Data Bit	**8bpp YCbCr 4:2:0 Even Line (2)**	**8bpp YCbCr 4:2:0 Odd Line (2)**	**Mapper Output**
D[0]	Y01[0]	Y11[0]	C(2)
D[1]	Y01[1]	Y11[1]	C(3)
D[2]	Y01[2]	Y11[2]	C(4)
D[3]	Y01[3]	Y11[3]	C(5)
D[4]	Y01[4]	Y11[4]	C(6)
D[5]	Y01[5]	Y11[5]	C(7)
D[6]	Y01[6]	Y11[6]	C(8)
D[7]	Y01[7]	Y11[7]	C(9)
D[8]	Y00[0]	Y10[0]	A(2)
D[9]	Y00[1]	Y10[1]	A(3)
D[10]	Y00[2]	Y10[2]	A(4)
D[11]	Y00[3]	Y10[3]	A(5)
D[12]	Y00[4]	Y10[4]	A(6)
D[13]	Y00[5]	Y10[5]	A(7)
D[14]	Y00[6]	Y10[6]	A(8)
D[15]	Y00[7]	Y10[7]	A(9)
D[16]	Cb00[0]	Cr00[0]	B(2)
D[17]	Cb00[1]	Cr00[1]	B(3)
D[18]	Cb00[2]	Cr00[2]	B(4)
D[19]	Cb00[3]	Cr00[3]	B(5)
D[20]	Cb00[4]	Cr00[4]	B(6)
D[21]	Cb00[5]	Cr00[5]	B(7)
D[22]	Cb00[6]	Cr00[6]	B(8)
D[23]	Cb00[7]	Cr00[7]	B(9)
D[24]			
D[25]			
'0'	-	-	B[0]
'0'	-	-	B[1]
'0'	-	-	A[0]
'0'	-	-	A[1]
'0'	-	-	C[0]
'0'	-	-	C[1]

(1) For all YCbCr 4:2:0 inputs, two consecutive pixel Luma values are brought in on each clock. Even lines carry the Cb values, and odd lines carry the Cr values.
(2) For 8bpp YCbCr 4:2:0 inputs, the 8-bits for each color shifts up two bits, and the two least significant bits of each color are set to '0'.

Table 7-16. V-by-One Data Mapping Example for 10bpp YCbCr 4:2:0 (1)

V-by-One Data Map Mode 8			
V-by-One Input Data Bit	**10bpp YCbCr 4:2:0 Even Line**	**10bpp YCbCr 4:2:0 Odd Line**	**Mapper Output**
D[0]	Y00[2]	Y10[2]	A(2)
D[1]	Y003]	Y10[3]	A(3)
D[2]	Y00[4]	Y10[4]	A(4)
D[3]	Y00[5]	Y10[5]	A(5)
D[4]	Y00[6]	Y10[6]	A(6)
D[5]	Y00[7]	Y10[7]	A(7)
D[6]	Y00[8]	Y10[8]	A(8)
D[7]	Y00[9]	Y10[9]	A(9)
D[8]	Cb00[2]	Cr00[2]	B(2)
D[9]	Cb00[3]	Cr00[3]	B(3)
D[10]	Cb00[4]	Cr00[4]	B(4)
D[11]	Cb00[5]	Cr00[5]	B(5)
D[12]	Cb00[6]	Cr00[6]	B(6)
D[13]	Cb00[7]	Cr00[7]	B(7)
D[14]	Cb00[8]	Cr00[8]	B(8)
D[15]	Cb00[9]	Cr00[9]	B(9)
D[16]	Y01[2]	Y11[2]	C(2)
D[17]	Y01[3]	Y11[3]	C(3)
D[18]	Y01[4]	Y11[4]	C(4)
D[19]	Y01[5]	Y11[5]	C(5)
D[20]	Y01[6]	Y11[6]	C(6)
D[21]	Y01[7]	Y11[7]	C(7)
D[22]	Y01[8]	Y11[8]	C(8)
D[23]	Y01[9]	Y11[9]	C(9)
D[24]			
D[25]			
D[26]	Y01[0]	Y11[0]	C[0]
D[27]	Y01[1]	Y11[1]	C[1]
D[28]	Cb00[0]	Cr00[0]	B[0]
D[29]	Cb00[1]	Cr00[1]	B[1]
D[30]	Y00[0]	Y10[0]	A[0]
D[31]	Y00[1]	Y10[1]	A[1]

(1) For all YCbCr 4:2:0 inputs, two consecutive pixel Luma values are brought in on each clock. Even lines carry Cb values, and odd lines carry the Cr values.

Table 7-17. V-by-One Data Mapping Example for 8bpp YCbCr 4:2:0 (1)

V-by-One Data Map Mode 9			
V-by-One Input Data Bit	**8bpp YCbCr 4:2:0 Even Line (2)**	**8bpp YCbCr 4:2:0 Odd Line (2)**	**Mapper Output**
D[0]	Y00[0]	Y10[0]	A(2)
D[1]	Y00[1]	Y10[1]	A(3)
D[2]	Y00[2]	Y10[2]	A(4)
D[3]	Y003]	Y10[3]	A(5)
D[4]	Y00[4]	Y10[4]	A(6)
D[5]	Y00[5]	Y10[5]	A(7)
D[6]	Y00[6]	Y10[6]	A(8)
D[7]	Y00[7]	Y10[7]	A(9)
D[8]	Cb00[0]	Cr00[0]	B(2)
D[9]	Cb00[1]	Cr00[1]	B(3)
D[10]	Cb00[2]	Cr00[2]	B(4)
D[11]	Cb00[3]	Cr00[3]	B(5)
D[12]	Cb00[4]	Cr00[4]	B(6)
D[13]	Cb00[5]	Cr00[5]	B(7)
D[14]	Cb00[6]	Cr00[6]	B(8)
D[15]	Cb00[7]	Cr00[7]	B(9)
D[16]	Y01[0]	Y11[0]	C(2)
D[17]	Y01[1]	Y11[1]	C(3)
D[18]	Y01[2]	Y11[2]	C(4)
D[19]	Y01[3]	Y11[3]	C(5)
D[20]	Y01[4]	Y11[4]	C(6)
D[21]	Y01[5]	Y11[5]	C(7)
D[22]	Y01[6]	Y11[6]	C(8)
D[23]	Y01[7]	Y11[7]	C(9)
D[24]			
D[25]			
'0'	-	-	C[0]
'0'	-	-	C[1]
'0'	-	-	B[0]
'0'	-	-	B[1]
'0'	-	-	A[0]
'0'	-	-	A[1]

(1) For all YCbCr 4:2:0 inputs, two consecutive pixel Luma values are brought in on each clock. Even lines carry the Cb values, and odd lines carry the Cr values.
(2) For 8bpp YCbCr 4:2:0 inputs, the 8-bits for each color shifts up two bits, and the two least significant bits of each color are set to '0'.

7.3.5 DMD (HSSI) Interface

The DLPC7540 Controller DMD interface supports two High Speed Serial Interface (HSSI) output-only interfaces for data transmission, a single low speed LVDS output-only interface for command write transactions, as well as a low speed single-ended input interface used for command read transactions. Each HSSI port supports full data-only inter-lane remapping within the port, but not between ports. When utilizing this feature, each unique data lane pair can only be mapped to one unique destination data lane pair, and Intra-lane remapping (i.e. swapping P with N) is not supported. In addition, the two HSSI ports can also be swapped. Lane and port remapping (specified in flash) can help with board layout as needed. The number of HSSI ports and number of HSSI lanes/per HSSI port required are based on DMD type and DMD display resolution. Table 7-18 shows some remapping examples. When both ports are used, they do not need to have the same pin mapping.

Table 7-18. Controller to DMD Pin Mapping Examples

DLPC7540 Controller PINS - REMAPPING EXAMPLES TO DMD PINS				DMD PINS
BASELINE	**FLIP HSSI0 180 No FLIP HSSI1**	**SWAP HSSI0 PORT WITH HSSI1 PORT**	**SWAP HSSI0 PORT WITH HSSI1 PORT AND MIXED REMAPPING**	
DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N
DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N
DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N
DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N
DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N
DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N
DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N
DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N
DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI1_D0_P DMD_HSSI1_D0_N
DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI1_D1_P DMD_HSSI1_D1_N
DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI1_D2_P DMD_HSSI1_D2_N
DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI1_D3_P DMD_HSSI1_D3_N
DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N	DMD_HSSI0_D4_P DMD_HSSI0_D4_N	DMD_HSSI0_D2_P DMD_HSSI0_D2_N	DMD_HSSI1_D4_P DMD_HSSI1_D4_N
DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N	DMD_HSSI0_D5_P DMD_HSSI0_D5_N	DMD_HSSI0_D3_P DMD_HSSI0_D3_N	DMD_HSSI1_D5_P DMD_HSSI1_D5_N
DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N	DMD_HSSI0_D6_P DMD_HSSI0_D6_N	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI1_D6_P DMD_HSSI1_D6_N
DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N	DMD_HSSI0_D7_P DMD_HSSI0_D7_N	DMD_HSSI0_D1_P DMD_HSSI0_D1_N	DMD_HSSI1_D7_P DMD_HSSI1_D7_N

7.3.6 Program Memory Flash Interface

The DLPC7540 provides three external program memory chip selects for devices to access the program memory interface. These are detailed in Table 7-19.

Table 7-19. Program Memory Interface Chip Selects

CHIP SELECT NAME	CHIP SELECT USE	DATA BUS WIDTH	ACCESS TIME	MAXIMUM SIZE SUPPORTED (1)
PM_CSZ_0	Boot FLASH only - Required (2)	16 bits	< = 120ns	256Mb
PM_CSZ_1	(or additional FLASH) - Optional	16 bits	< = 120ns	256Mb
PM_CSZ_2	Additional Peripheral Device - Optional	16 bits	< = 120ns	256Mb

(1) Using GPIO_47 as additional address bit
(2) Boot FLASH type supported is *Standard NOR parallel FLASH*, single or multi-bank.

FLASH access timing is software programmable with up to 31 wait states. Additional information about read and write wait state timing is provided in Table 7-20 and Figure 7-4.

Table 7-20. Program Memory Wait State Timing

PARAMETER	EQUATION (1)
T_{WSR}: Wait State Resolution	6ns
Read Wait States (Number of Read Wait States for each CSz read access)	ROUNDUP(MAX(T_{ACC}, T_{CE},T_{OE})/T_{WSR-N}) (2) (3)
Write Wait States for $T_{CS}$and T_{AS} (Time from CS/Address activation to WRZ assertion)	ROUNDUP(MAX(T_{CS}+5ns, T_{AS}+5ns)/T_{WSR-N}) (2)
Write Wait States for T_{WP} and T_{DS} (Time from WRZ assertion to WEZ de-assertion)	ROUNDUP(MAX(T_{WP}+5ns, T_{DS}+5ns)/T_{WSR-N}) (2)
Write Wait States for $T_{CH}$and T_{DH} (Time from CS/Address activation to WRZ assertion)	ROUNDUP(MAX(T_{CH}+5ns, T_{DH}+5ns)/T_{WSR-N}) (2)

(1)
a. T_{ACC}: Read Access Time (ADDR to DATA valid) – (address valid to DATA valid)
b. T_{CE}: Read Access Time (CSZ to DATA valid) – (chip select active to DATA valid)
c. T_{OE}: Read Access Time (OEZ to DATA valid) – (output enable active to DATA valid)
d. T_{CS}: CSZ Setup Time (Writes) – (chip select active before negedge(WEZ)
e. T_{CS}: Address Setup Time (Writes) – (address valid before negedge(WEZ)
f. T_{AS}: Address Setup Time (Writes) – (address valid before negedge(WEZ)
g. T_{WP}: Write Pulse Width (Writes) – (WEZ active low time)
h. T_{DS}: Data Setup Time (Writes) – (DATA valid before posedge(WEZ)
i. T_{CH}: CSZ Hold Time (Writes) – (CSZ held active after posedge(WEZ)
j. T_{DH}: Data Hold Time (Writes) – (DATA held valid after posedge(WEZ)

(2) Requires a minimum of at least 1 wait state
(3) Assumes a maximum single direction trace length of 90 mm (3.5 inches)

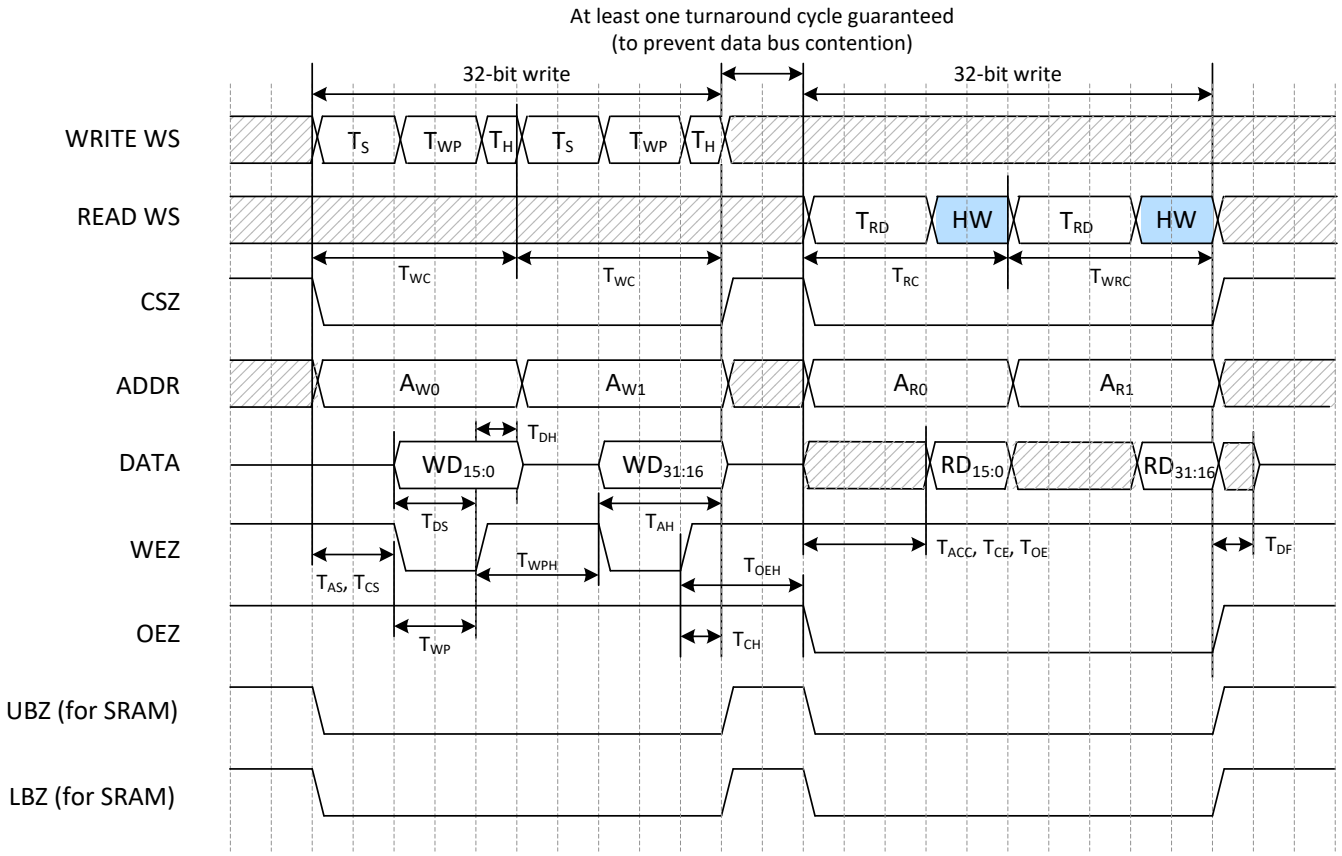


Figure 7-4. Program Memory Interface Timing Diagram

7.3.7 GPIO Supported Functionality

The DLPC7540 provides 88 general purpose I/O that are available to support a variety of functions for many different product configurations. In general, most of these I/O pins support only one specific function based on a specific product configuration, although that function can be different for a different product configuration. Most of these I/O can also be made available for TI test and debug use. Each of the following GPIO tables provide product specific details on the allocated use of each of the GPIO for a specific supported product configuration.

7.3.8 Debug Support

The DLPC7540 contains a test point output port, TSTPT_(7:0), which provides the Host with the ability to provide for Controller debug support. For initial debug operation, the four signals (TSTPT(3:0)) are sampled as inputs approximately 1.5 µs after PWRGOOD goes high (or after a system reset). Once their input state has been sampled and captured, this information is used to setup the initial test mode output state of the TSTPT_(7:0) bus. Table 7-21 defines the test mode selection for a few programmable output states for TSTPT_(7:0). Use the default state of 0000 (defined by the required external pulldown resistors) for normal operation (that is, no debug required).

To allow TI to make use of this debug capability, providing for the option of a jumper to an external pullup is recommended for TSTPT(3:0), as well as providing access to allow observation of the TSTPT bus outputs.

Table 7-21. Examples of Test Mode Selection Outputs Defined by TSTPT(3:0)(1)

TSTPT_(7:0) OUTPUT	TSTPT(3:0) CAPTURED VALUES		
	0000 (DEFAULT) (NO SWITCHING ACTIVITY)	0101 CLOCK DEBUG	1000 SYSTEM CALIBRATION
TSTPT(0)	0	HIGH	Vertical Sync
TSTPT(1)	0	166.25 MHz	Delayed CW Index

Table 7-21. Examples of Test Mode Selection Outputs Defined by TSTPT(3:0)[1] (continued)

TSTPT_(7:0) OUTPUT	TSTPT(3:0) CAPTURED VALUES		
	0000 (DEFAULT) (NO SWITCHING ACTIVITY)	0101 CLOCK DEBUG	1000 SYSTEM CALIBRATION
TSTPT(2)	0	83.13 MHz	Sequence Index
TSTPT(3)	0	41.56 MHz	CW Spoke Test Point
TSTPT(4)	0	10.39 MHz	CW Revolution Test Point
TSTPT(5)	0	25.16 MHz	Reset Sequence Aux Bit 0
TSTPT(6)	0	133.00 MHz	Reset Sequence Aux Bit 1
TSTPT(7)	0	HIGH	Reset Sequence Aux Bit 2

(1) These are only the default output selections. Software can reprogram the selection at any time.

7.4 Device Operational Modes

The DLPC7540 has two operational modes which are enabled via software command via the Host control interface. These modes are Standby and Active.

7.4.1 Standby Mode

The system is powered up and active, however, most blocks within the Controller have been shut down to conserve power. Only the µProcessor and its peripherals are active (supporting a dormant projector waiting to be woken up). In this mode the DMD is parked and no image can be displayed.

7.4.2 Active Mode

The system is powered up and fully operational, capable of projecting internal or external source images.

7.4.2.1 Normal Configuration

This configuration enables the full functionality of the DLPC7540.

7.4.2.2 Low Latency Configuration

This configuration disables some of the capabilities of the DLPC7540 to reduce the overall system latency for certain applications which are sensitive to system latency. The key function that is disabled for this configuration is the Warping block, which removes a full frame of latency from the processing path.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC7540 is the next generation high resolution display controller. It is part of the DLP471TE, DLP471NE, DLP650TE or DLP651NE chipsets. The controller integrates all system image processing and DMD control and data formatting onto a single integrated circuit (IC). It supports laser-phosphor, RGB-laser, LED and hybrid illumination systems. Standard image processing algorithms such as DynamicBlack or BrilliantColor™ are included. The DLPC7540 also includes a full featured image warping engine which can warp images on to arbitrary surfaces, as well as support image blending, and projector stacking. The warp engine gives true 3D keystone correction. Applications of interest include 4K UHD Enterprise Projectors, Laser TV, Smart Projectors, and Digital Signage.

8.2 Typical Application

The DLPC7540 controller is ideal for applications requiring high-performance, high-resolution displays. When the DLPC7540 display controller is combined with the DLP471TE, DLP471NE, DLP650TE or DLP651NE DMD, a power management and motor driver device (DLPA100), and other electrical, optical and mechanical components the chipset enables bright, affordable, full 4K UHD display solutions. A typical 4K UHD system application using the DLPC7540 controller and DLP471TE, DLP471NE, DLP650TE or DLP651NE DMD is shown in the figure below Figure 8-1

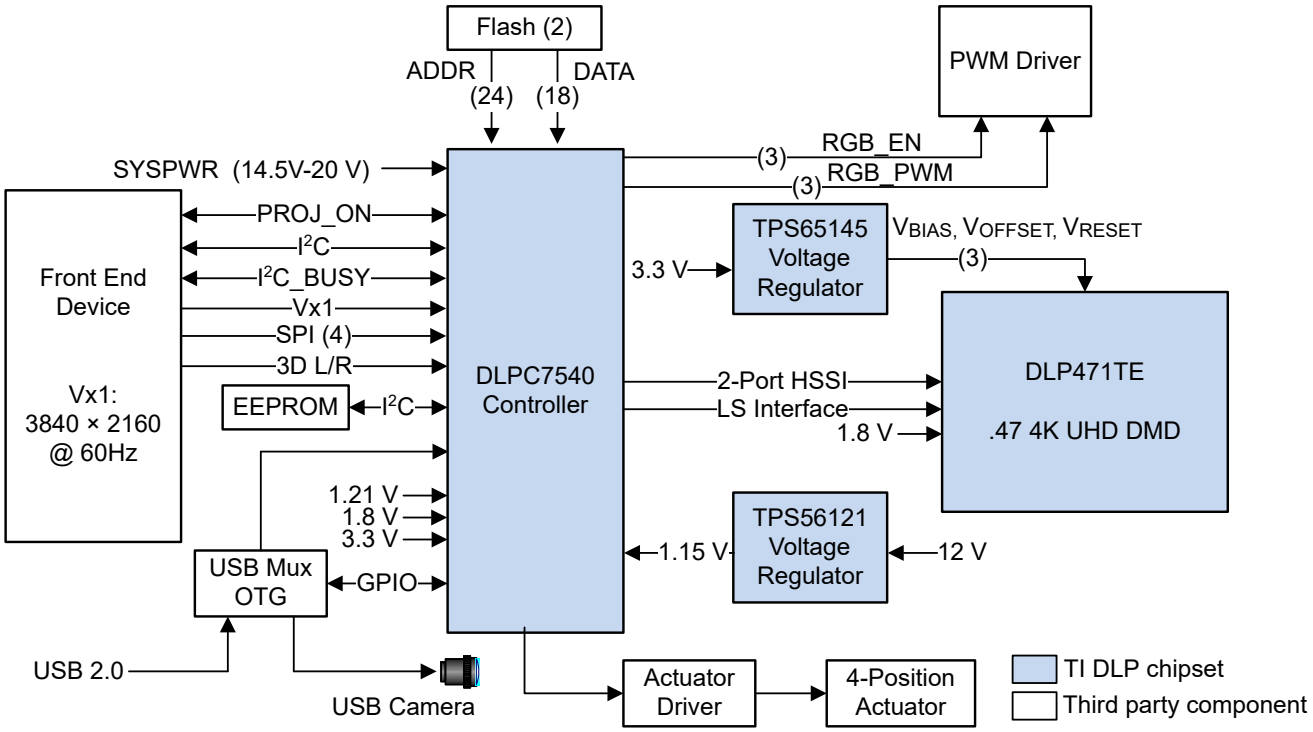


Figure 8-1. Typical 4K UHD LED System

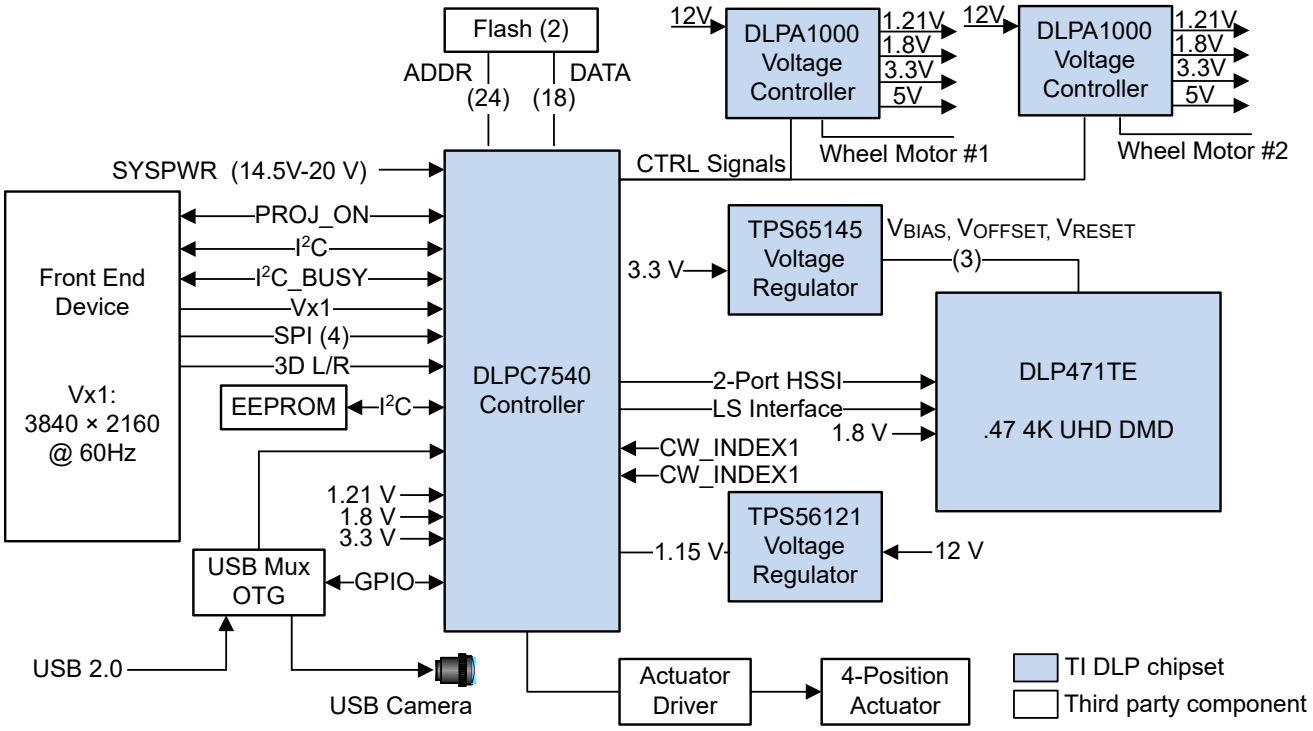


Figure 8-2. Typical 4K UHD LPCW System

8.2.1 Design Requirements

The display controller is the digital interface between the DMD and the rest of the system. The display controller takes digital V-by-One, FPD-Link input from front end receiver and drives the DMD over a high speed interface. The display controller also generates the necessary signals (data, protocols, timings) required to display images on the DMD. Reliable operation of the DMD is only ensured when the DMD and the controller are used together in a system. In addition, other devices might be needed. Typically, a Flash part is needed to store the software and firmware and power supply management part required to power the DMD and the controller.

8.2.2 Detailed Design Procedure

For connecting the DLPC7540 controller and the DLP471TE, DLP471NE, DLP650TE or DLP651NE DMD together, see the reference design schematic. It is essential to follow these layout guidelines for high-speed interfaces, V-by-One and the DMD HSSI in order to design a reliable projector. To complete the DLP system, an optical module or light engine is required that contains the DLP471TE, DLP471NE, DLP650TE or DLP651NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

9 Power Supply Recommendations

9.1 Power Supply Management

The DLPA100 manages power for the DLPC7540 and DMD. See *Section 6.13* for all power sequencing and timing requirements.

9.2 Hot Plug Usage

While the V-by-One, FPD-Link, and USB interfaces support hot plug usage (i.e. these interfaces can be connected and disconnected while the DLPC7540 is powered), the controller itself (and any DMD connected to the system) do not support Hot Plug use. As such, power down the system prior to removing the controller or DMD from any system.

9.3 Power Supplies for Unused Input Source Interfaces

While certain product configurations cannot offer or make use of all of the available input source interfaces (e.g. V-by-One, FPD-Link), *the power supplies that are associated with these unused input source interfaces must still be provided as if the interface was actually being used.* The only concession is that the ferrite based isolation filters for these supplies can be simplified down to simple de-coupling caps.

9.4 Power Supplies

9.4.1 1.15-V Power Supplies

The DLPC7540 can support a low cost power delivery system with a single 1.15-V power source derived from a switching regulator. To enable this approach, provide typical bulk (e.g. 10 µF, 22 µF) and high frequency (e.g. 0.1 µF) filtering for the core 1.15-V power rail (VDD115). Ensure that the the high-frequency capacitors are evenly distributed amongst the power balls and that they are placed as close to the power balls as possible. Additional filtering must be provided for each of the uniquely defined 1.15-V power pins (e.g. VDD115_PLLMA, VAD115VX1). Filtering for the unique power pins is discussed further in Section 10.1 of this document.

9.4.2 1.21V Power Supply

The DLPC7540 can support a low cost power delivery system with a single 1.21V power source derived from a switching regulator. To enable this approach, provide typical bulk (e.g. 10 µF, 22 µF) and high frequency (e.g. 0.1 µF) filtering for the 1.21-V power rail (VDD121_SCS). Place the high-frequency filtering capacitors as close as possible to the VDD121_SCS power balls.

9.4.3 1.8-V Power Supplies

The DLPC7540 can support a low cost power delivery system with a single 1.8-V power source derived from a switching regulator. To enable this approach, appropriate filtering must be provided for each of the uniquely defined 1.8-V power pins (e.g. VDD18_PLLMA, VAD18_VX1). See Section 10.1 for more information.

9.4.4 3.3-V Power Supplies

The DLPC7540 can support a low cost power delivery system with a single 3.3-V power source derived from a switching regulator. To enable this approach, provide typical bulk (e.g. 10 µF, 22 µF) and high frequency (e.g. 0.1 µF) filtering for the main 3.3-V I/O power rail (VDD33). Ensure that the the high-frequency capacitors are evenly distributed amongst the power balls and that they are placed as close to the power balls as possible. Additional filtering must be provided for each of the uniquely defined 3.3-V power pins (e.g. VAD33_USB, VDD33_FPD). This is discussed further in Section 10.1 of the document.

10 Layout

10.1 Layout Guidelines

10.1.1 General Layout Guidelines

In order to meet the thermal loads associated with the DLPC7540, TI recommends the following enhanced PCB design parameters.

- A minimum of 4 power and ground planes
  - Power layers: 1-oz. copper; Ground layers: 2-oz. copper
    - Copper coverage: 90%
  - Top and bottom signal layers: minimum 0.5-oz copper
  - Internal signal layers: 1-oz copper
- Thermal copper ground planes beneath the thermal ball array of package containing a via farm with the following attributes
  - Thermal via quantity to ground plane = 64 (as 8x8 array)
  - Thermal via size = 0.229mm - 0.25 mm (9mils - 10 mils)
  - Thermal via plating thickness = 0.025 mm (1 mil) wall thickness

For signal integrity reasons, FR370HR or equivalent high performance epoxy laminate and repreg is also recommended.

10.1.2 Power Supply Layout Guidelines

The following filtering circuits are recommended for the power supply inputs listed below.

- VAD115_VX1
- VAD18_VX1
- VAD115_FPD
- VDD33_FPD
- VAD33_USB
- VDD18_SCS

Since the PBC layout is critical to the performance of the interfaces associated with these power supplies, it is vital that these power supplies be treated like an analog signal. Specifically:

- Place high-frequency components (such as ferrites and capacitors) as close to the power ball(s) as possible.
- Choose high-frequency ceramic capacitors (such as those with a valua of 0.1 µF, 0.01 µF, and 100 nF) that have low ESR and ESL values. Design the leads as short as possible, and as such, it is recommended that these capacitors be placed under the package on the opposite side of the board..
- For each power pin, a single trace (as wide as possible) must be used from the controller to the capacitor and then through the series ferrite to the power source.
- For each power pin, add a 100-nF decoupling capacitor placed near the escape via. Add this decoupling capacitance to the capacitance recommended for filters. These are minimum recommendations, so different layouts could require additional capacitance.
- See Table 10-1 for the recommended series ferrite component for these supplies.

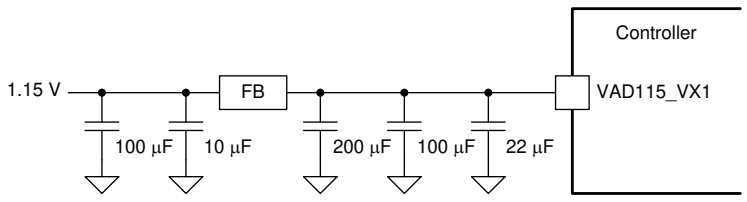


Figure 10-1. VAD115_VX1 (V-by-One) Recommended Filter

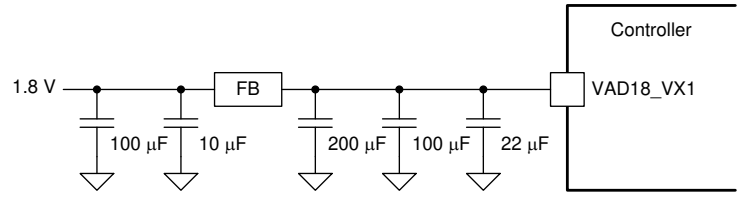


Figure 10-2. VAD18_VX1 (V-by-One) Recommended Filter

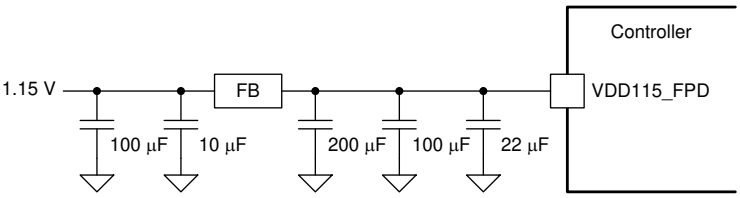


Figure 10-3. VAD115_FPD (FPD-Link) Recommended Filter

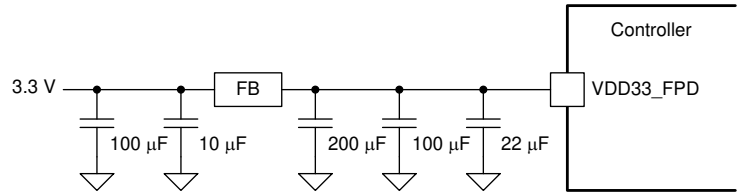


Figure 10-4. VDD33_FPD (FPD-Link) Recommended Filter

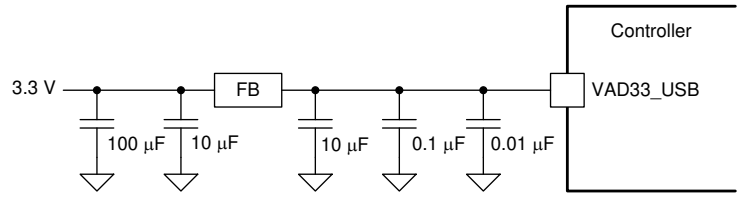


Figure 10-5. VAD33_USB (USB) Recommended Filter

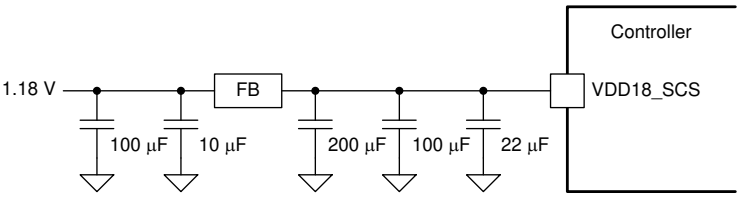


Figure 10-6. VDD18_SCS (SCS DRAM) Recommended Filter

10.1.3 Layout Guidelines for Internal Controller PLL Power

The following guidelines are recommended to achieve the desired Controller performance relative to the internal PLLs. The DLPC7540 contains multiple internal PLLs which have dedicated 1.15-V supply pins and 1.8-V supply pins which are listed below:

- VDD115_PLLMA
- VDD115_PLLMB
- VAD115_PLLS

- VAD115_HSSI0_PLL
- VAD115_HSSI1_PLL

and

- VAD18_PLLMA
- VAD18_PLLMB

It is important that each of these 1.15-V and 1.8-V supply pins have individual high frequency filtering in the form of a ferrite bead and a 0.1-µF ceramic capacitor. Ensure that the impedance of the ferrite bead is much greater than that of the capacitor at frequencies above 10 MHz. Locate these components very close to the individual PLL power supply balls. Recommended values, topology, and layout examples are shown in Table 10-1, Figure 10-7 and Figure 10-8, and Figure 10-9 respectively.

Table 10-1. Recommended PLL and Crystal Power Supply Filter Components

COMPONENT	PARAMETER	RECOMMENDED VALUE	UNIT
Shunt capacitor	Capacitance	0.1	µF
Series ferrite	Impedance at 100 MHz	> 100	Ω
	DC Resistance	< 0.40	Ω

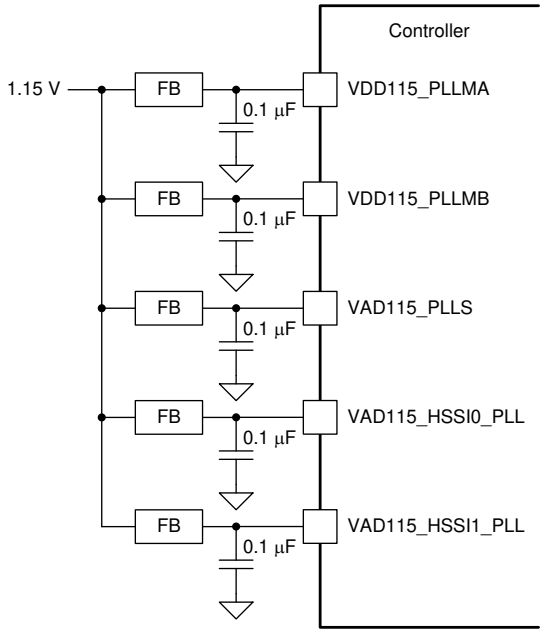


Figure 10-7. 1.15-V PLL Power Supply Filter Topology

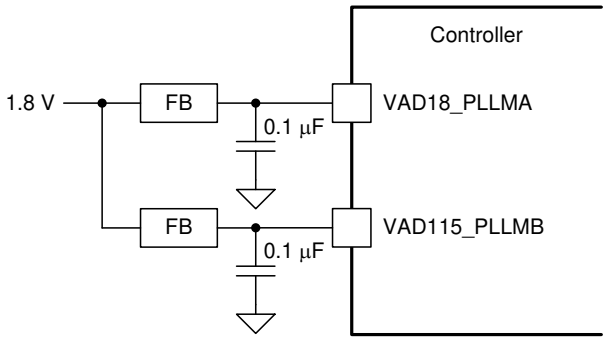


Figure 10-8. 1.8-V PLL Power Supply Filter Topology

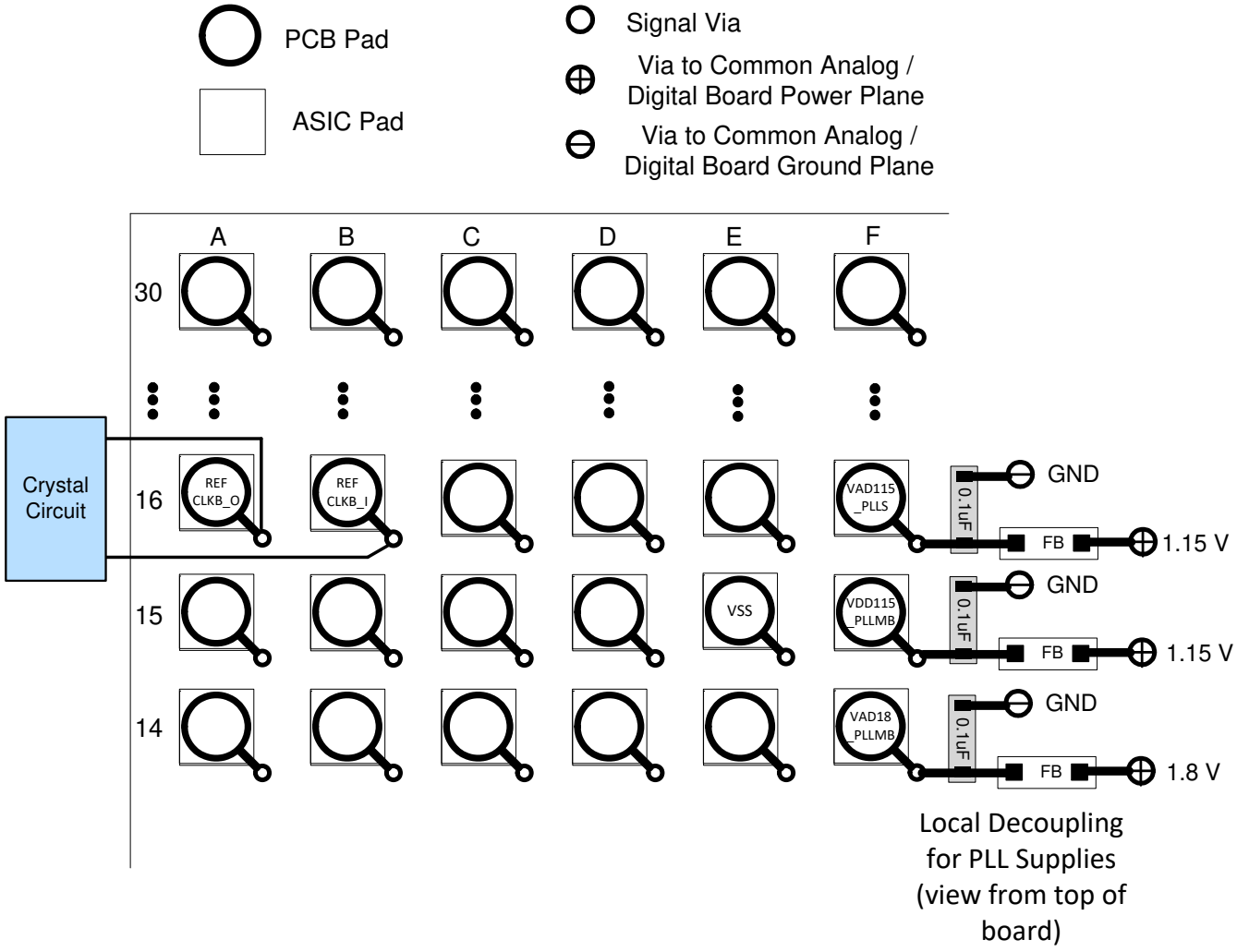


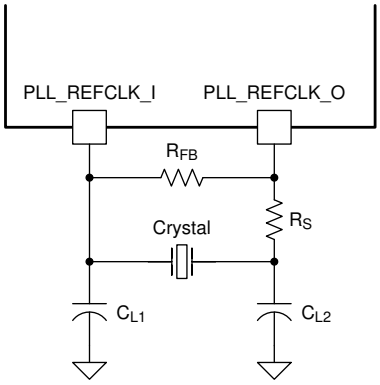
Figure 10-9. PLL Power Supply Filter Layout Examples

Since the PCB layout is critical to PLL performance, it is vital that the PLL power is treated like an analog signal. Additional design guidelines are as follows:

- Place all filter components as close to possible to each of the PLL supply package pins.
- Keep the leads of the high-frequency capacitors as short as possible, and as such, it is recommended that these capacitors be placed under the package on the opposite side of the board.
- Use a surface mount capacitor that is of high quality, low ESR, and monolithic.
- For each PLL power pin, a single trace (as wide as possible) must be used from the DLPC7540 to the capacitor and then through the series ferrite to the power source.

10.1.4 Layout Guideline for DLPC7540 Reference Clock

The DLPC7540 requires two external reference clocks to feed its internal PLLs. A crystal or oscillator can supply these references. The recommended crystal configurations and reference clock frequencies are listed in Table 10-2, with additional required discrete components shown in Figure 10-10 and defined in Table 10-2.



C_L = Crystal load capacitance
R_{FB} = Feedback Resistor

Figure 10-10. Discrete Components Required for Crystal

10.1.4.1 Recommended Crystal Oscillator Configuration

Table 10-2. Recommended Crystal Configurations

PARAMETER	CRYSTAL A	CRYSTAL B	UNIT
Crystal circuit configuration	Parallel resonant	Parallel resonant	
Crystal type	Fundamental (first harmonic)	Fundamental (first harmonic)	
Crystal nominal frequency	40	38	MHz
Crystal frequency tolerance (1)	±100 (200 p-p max)	±100 (200 p-p max)	PPM
Crystal equivalent series resistance (ESR)	60 (Max)	60 (Max)	Ω
Crystal load capacitance	20 (Max)	20 (Max)	pF
Crystal Shunt Load capacitance	7 (Max)	7 (Max)	pF
Temperature range	-40°C to +85°C	-40°C to +85°C	°C
Drive level	100 (Nominal)	100 (Nominal)	µW
R_{FB} feedback resistor (nominal)	1Meg (Nominal)	1Meg (Nominal)	Ω
C_{L1} external crystal load capacitor	See equation in (2)	See equation in (2)	pF
C_{L2} external crystal load capacitor	See equation in (3)	See equation in (3) (3)	pF
PCB layout	A ground isolation ring around the crystal is recommended	A ground isolation ring around the crystal is recommended	

(1) Crystal frequency tolerance to include accuracy, temperature, aging, and trim sensitivity. These are typically specified separately and the sum of all required to meet this requirement.
(2) CL1 = 2 × (CL – Cstray_pll_refclk_i), where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the Controller pin REFCLKx_I. See Table 10-3.
(3) CL2 = 2 × (CL – Cstray_pll_refclk_o), where: Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the Controller pin REFCLKx_O. See Table 10-3.

Table 10-3. Crystal Pin Capacitance

PARAMETER		MIN	NOM	MAX	Units
Cstray_pll_refclkA_i	Sum of package and PCB stray capacitance at REFCLKA_I		4.5		pF
Cstray_pll_refclkA_o	Sum of package and PCB stray capacitance at REFCLKA_O		4.5		pF
Cstray_pll_refclkB_i	Sum of package and PCB stray capacitance at REFCLKB_I		4.5		pF
Cstray_pll_refclkB_o	Sum of package and PCB stray capacitance at REFCLKB_O		4.5		pF

The crystal circuits in the DLPC7540 have dedicated power (VAD33_OSCA and VAD33_OSCB) pins, with the recommended filtering for each shown in Figure 10-11, and recommended values shown in Table 10-1

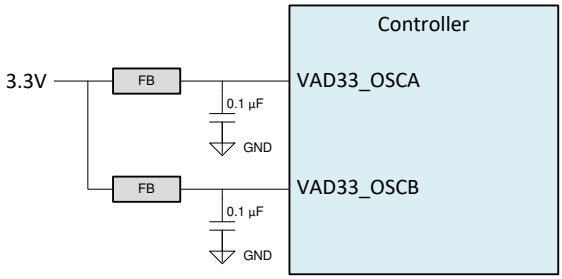


Figure 10-11. Crystal Power Supply Filtering

Table 10-4. DLPC7540 Recommended Crystal Parts

MANUFACTURER	PART NUMBER	NOMINAL FREQUENCY	FREQUENCY TOLERANCE, FREQUENCY STABILITY, AGING/YEAR	ESR	LOAD CAPACITANCE	OPERATING TEMPERATURE	Drive Level
TXC	7M38070001 (1)	38 MHz	Freq Tolerance: ±20 ppm Freq Stability: ±20 ppm Aging/Year: ±3 ppm	30Ω max	12 pF	–40°C to +85°C	100µW
TXC	7M40070041 (2)	40 MHz	Freq Tolerance: ±20 ppm Freq Stability: ±20 ppm Aging/Year: ±3 ppm	30Ω max	12 pF	–40°C to +85°C	100µW

(1) This device requires an R_S resistor with value = 0.
(2) This device requires an R_S resistor with value = 0.

10.1.5 V-by-One Interface Layout Considerations

The DLPC7540 V-by-One SERDES differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC7540 I/O timing parameters, V-by-One transmitter timing parameters, as well as Thine specific timing requirements can be found in their corresponding data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB related requirements for V-by-One are provided in Table 10-5 as a starting point for the customer.

Table 10-5. V-by-One Interface PBC Related Requirements (1)

PARAMETER	MIN	TYP	MAX	UNIT
Intra-lane cross-talk (between VX1_DATAx_P and VX1_DATAx_N)			< 1.5	mVpp
Inter-lane cross-talk (between data lane pairs)			< 1.5	mVpp
Cross-talk between data lanes and other signals			< 1.5	mVpp
Intra-lane skew			< 40	ps
Inter-lane skew			< 800	ps
Differential Impedance	90	100	110	Ω

(1) If using the minimum trace width and spacing to escape the Controller ball field, widening these out after escape is desirable if practical to achieve the target 100 Ω impedance (e.g. to reduce transmission line losses).

Additional V-by-One layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a Micro-strip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair, and between each pair, in order to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pairs are between 135º and 225º(See Figure 10-12).

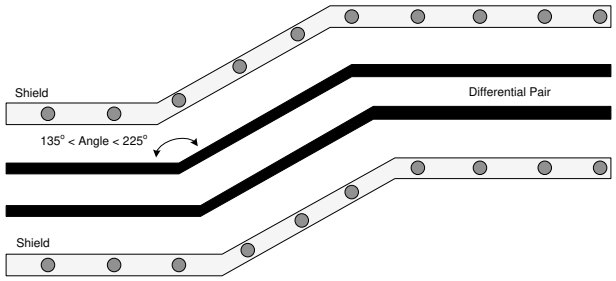


Figure 10-12. V-by-One Routing Example

10.1.6 FPD-Link Interface Layout Considerations

The DLPC7540 FPD-Link differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC7540 I/O timing parameters as well as the FPD-Link transmitter timing parameters can be found in their corresponding data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB related requirements for FPD-Link are provided in Table 10-6 as a starting point for the customer.

Table 10-6. FPD-Link Interface PBC Related Requirements

PARAMETER	MIN	TYP	MAX	UNIT
Intra-lane Cross-talk (between FPDz_DATAx_P and FPDz_DATAx_N)			< 2.0	mVpp
Inter-lane Cross-talk (between data lane pairs)			< 2.0	mVpp
Cross-talk between data lanes and other signals			< 2.0	mVpp
Intra-lane skew			< 40	ps
Inter-lane skew			± 40	ps
Differential Impedance	90	100	110	Ω

Additional FPD-Link layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a Micro-strip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair, and between each pair, in order to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pairs are between 135º and 225º (See Figure 10-13).

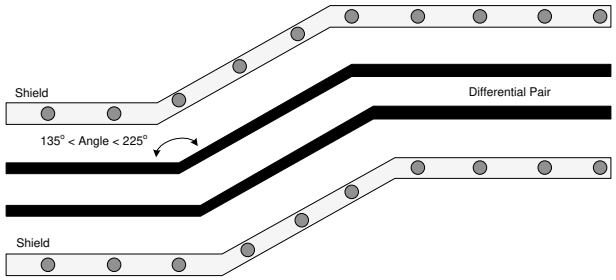


Figure 10-13. FPD-Link Routing Example

10.1.7 USB Interface Layout Considerations

The DLPC7540 USB differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC7540 I/O timing parameters, USB transmitter and receiver timing parameters, as well as USB specific timing requirements can be found in their corresponding data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB related requirements for USB are provided in Table 10-7 as a starting point for the customer.

Table 10-7. USB Interface PBC Related Requirements (1)(2)

PARAMETER	MIN	TYP	MAX	UNIT
Cross-talk between data lane (USB_DAT_P, USB_DAT_N) and other signals			< 1.5	mVpp
Intra-lane skew (USB_DAT_P, USB_DAT_N)			< 20	ps
Differential Impedance (USB_DAT_P, USB_DAT_N)	76.5	90	103.5	Ω
Single Mode impedance (USB_DAT_P, USB_DAT_N)		45		Ω
Common Mode Impedance (USB_DAT_P, USB_DAT_N)	21	30	39	Ω
Parasitic resistance (USB_DAT_P, USB_DAT_N)			≤ 0.5	Ω
Total capacitance (USB_DAT_P, USB_DAT_N)			< 4	pF
Differences of trace capacitance between USB_DAT_P, USB_DAT_N			< 1	pF
TXRTUNE resistor	172.26	174	175.74	Ω

(1) If using the minimum trace width and spacing to escape the Controller ball field, widening these out after escape is desirable if practical to achieve the target 100 Ω impedance (e.g. to reduce transmission line losses).
(2) One pcb layout example for the differential pair is shown in Figure 10-14

Additional layout guidelines for USB_DAT_P/USB_DAT_N:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a Micro-strip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair, and between each pair, in order to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pair are between 135º and 225º. (See Figure 10-15).
- Minimize the length where the differential signal pair are parallel to clocks or digital signals.
- Do not route the differential signal pair under an IC that uses a quartz crystal, oscillator, clock synchronization circuit, magnetic device, or clock.

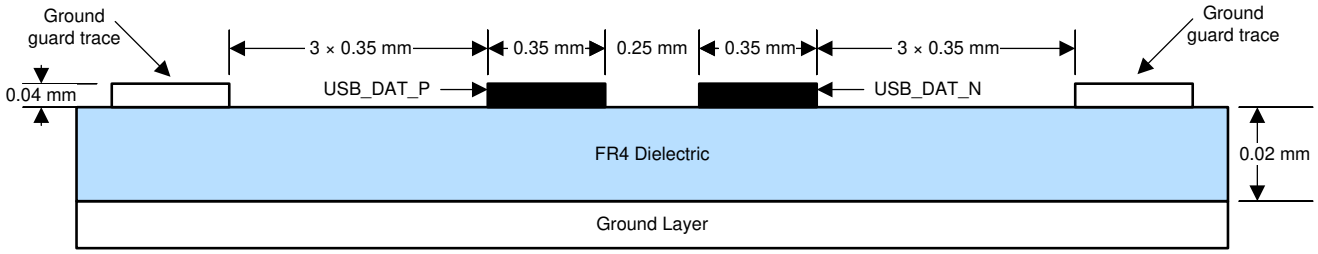


Figure 10-14. USB Layout Example

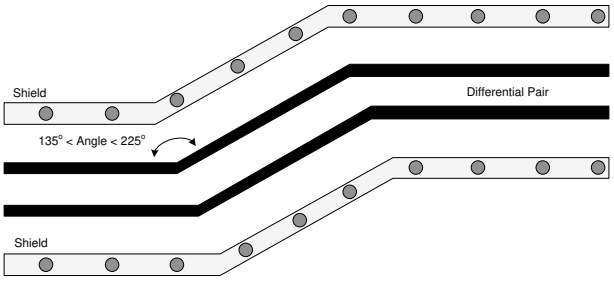


Figure 10-15. USB Routing Example

Additional USB layout guidelines for TXRTUNE

- Use the shortest possible connection lengths for the resistor between TXRTUNE and ground.
- Use ground layer and ground guard traces to shield the wires and resistor.

10.1.8 DMD Interface Layout Considerations

The DLPC7540 controller HSSI differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC7540 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB design recommendations are provided in Table 10-8 , Figure 10-16,and the paragraph below as a starting point for the customer.

Table 10-8. PCB Recommendations for DMD Interface (1)(2)

PARAMETER		MIN	MAX	UNIT
T_W	Trace Width	5.7		mils
T_S	Intra-lane Trace Spacing	5.3		mils
T_{SPP}	Inter-lane trace spacing (3)	48.3		mils

(1) Recommendations to achieve the desired nominal differential impedance as specified by R_{DIFF} in Section 6.7.
(2) These parameters show recommendations based on the micro-strip design shown in Figure 10-16. This design minimizes signal loss to support longer trace lengths at the expense of electromagnetic interference (EMI). The designer has the option to use of a stripline design for shorter trace lengths and to target minimizing EMI at the expense of signal loss.
(3) A reduced inter-lane spacing can be used to escape the Controller ball field, however, widen this spacing to at least the stated minimum after escape.

Figure 10-16. DMD Differential Layout Recommendations

Additional DMD interface layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two. If two are required, place one at each end of the line (one at the controller and one at the DMD).
- Route the differential signal pairs over a single ground or power plane using a Micro-strip line configuration.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Ensure the bend angles associated with the differential signal pairs are between 135° and 225°.
- Route the single-ended signal in a way that to minimizes the number of vias required. Limit the number of necessary vias to two. If two are required, place one at each end of the line (one at the controller and one at the DMD).
- Avoid stubs.
- No external termination resistors are required on the DMD_HSSI or DMD_LS differential signals.

- Include a series termination resistor (with a value of 30.1 Ω, for example) to the DMD_LS0_RDATA and DMD_LS1_RDATA single-ended signal paths. Place the resistor as close as possible to the corresponding DMD pin.
- The DMD_DEN_ARSTZ does not typically require a series resistor, however, for a long trace, one might be needed to reduce undershoot or overshoot.

10.1.9 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potential damage to unused video source inputs and unused GPIO, the instructions specifically noted in the associated *Section 5* must be followed. For those unused inputs without specific instructions, TI recommends that these input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. Unused output-only pins can remain open. Never tie unused output-only pins directly to power or ground. For controller inputs with an internal pullup or pulldown resistor, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Internal pullup and pulldown resistors are weak and cannot be expected to drive the external line. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value specified in Table 5-14.

There are also power supply considerations that must be followed for any unused video sources. These are detailed in Section 9.3.

10.1.10 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 10-9. Max Pin-to-Pin PCB Interconnect Recommendations - DMD

Controller INTERFACE	SIGNAL INTERCONNECT TOPOLOGY (1) (2) (3)		UNIT
DMD	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HSSI0_CLK_P DMD_HSSI0_CLK_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI0_D0_P DMD_HSSI0_D0_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI0_D1_P DMD_HSSI0_D1_N			
DMD_HSSI0_D2_P DMD_HSSI0_D2_N			
DMD_HSSI0_D3_P DMD_HSSI0_D3_N			
DMD_HSSI0_D4_P DMD_HSSI0_D4_N			
DMD_HSSI0_D5_P DMD_HSSI0_D5_N			
DMD_HSSI0_D6_P DMD_HSSI0_D6_N			
DMD_HSSI0_D7_P DMD_HSSI0_D7_N			
DMD_HSSI1_CLK_P DMD_HSSI1_CLK_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI1_D0_P DMD_HSSI1_D0_N	10 (254)	Controller PCB: 2 (50.8) DMD PCB: 4 (101.6) Flex: 10 (254)	inch (mm)
DMD_HSSI1_D1_P DMD_HSSI1_D1_N			
DMD_HSSI1_D2_P DMD_HSSI1_D2_N			
DMD_HSSI1_D3_P DMD_HSSI1_D3_N			
DMD_HSSI1_D4_P DMD_HSSI1_D4_N			
DMD_HSSI1_D5_P DMD_HSSI1_D5_N			
DMD_HSSI1_D6_P DMD_HSSI1_D6_N			
DMD_HSSI1_D7_P DMD_HSSI1_D7_N			
DMD_LS0_CLK_P DMD_LS0_CLK_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS0_WDATA_P DMD_LS0_WDATA_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS1_CLK_P DMD_LS1_CLK_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS1_WDATA_P DMD_LS1_WDATA_N	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS0_RDATA	18 (457.2)	18 (457.2)	inch (mm)
DMD_LS1_RDATA	18 (457.2)	18 (457.2)	inch (mm)

Table 10-9. Max Pin-to-Pin PCB Interconnect Recommendations - DMD (continued)

Controller INTERFACE	SIGNAL INTERCONNECT TOPOLOGY (1) (2) (3)		UNIT
DMD	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing lengths shown are the combination that was analyzed by TI.
(3) Due to board variations, create a SPICE simulation for all board designs with the Controller IBIS models to ensure signal routing lengths do not exceed signal requirements.

Table 10-10. High Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING (1) (2)				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH (3)	UNIT
DMD (4)	DMD_HSSI0_D0_P DMD_HSSI0_D0_N	DMD_HSSI0_CLK_P DMD_HSSI0_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HSSI0_D1_P DMD_HSSI0_D1_N			
	DMD_HSSI0_D2_P DMD_HSSI0_D2_N			
	DMD_HSSI0_D3_P DMD_HSSI0_D3_N			
	DMD_HSSI0_D4_P DMD_HSSI0_D4_N			
	DMD_HSSI0_D5_P DMD_HSSI0_D5_N			
	DMD_HSSI0_D6_P DMD_HSSI0_D6_N			
	DMD_HSSI0_D7_P DMD_HSSI0_D7_N			
DMD (5)	DMD_HSSI0_x_P	DMD_HSSI0_x_N	±0.01 (±0.254)	inch (mm)
DMD (4)	DMD_HSSI1_D0_P DMD_HSSI1_D0_N	DMD_HSSI1_CLK_P DMD_HSSI1_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HSSI1_D1_P DMD_HSSI1_D1_N			
	DMD_HSSI1_D2_P DMD_HSSI1_D2_N			
	DMD_HSSI1_D3_P DMD_HSSI1_D3_N			
	DMD_HSSI1_D4_P DMD_HSSI1_D4_N			
	DMD_HSSI1_D5_P DMD_HSSI1_D5_N			
	DMD_HSSI1_D6_P DMD_HSSI1_D6_N			
	DMD_HSSI1_D7_P DMD_HSSI1_D7_N			
DMD (5)	DMD_HSSI1_x_P	DMD_HSSI1_x_N	±0.01 (±0.254)	inch (mm)
DMD (6)	DMD_HSSI0_CLK_P	DMD_HSSI1_CLK_P	±0.05 (±1.27)	inch (mm)
DMD (6)	DMD_HSSI0_CLK_N	DMD_HSSI1_CLK_N	±0.05 (±1.27)	inch (mm)
DMD (4)	DMD_LS0_WDATA_P DMD_LS0_WDATA_N	DMD_LS0_CLK_P DMD_LS0_CLK_N	±1.0 (±25.4)	inch (mm)

Table 10-10. High Speed PCB Signal Routing Matching Requirements (continued)

SIGNAL GROUP LENGTH MATCHING (1) (2)				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH (3)**	**UNIT**
DMD (5)	DMD_LS0_x_P	DMD_LS0_x_N	±0.025 (±0.635)	inch (mm)
DMD (4)	DMD_LS1_WDATA_P DMD_LS1_WDATA_N	DMD_LS1_CLK_P DMD_LS1_CLK_N	±1.0 (±25.4)	inch (mm)
DMD (5)	DMD_LS1_x_P	DMD_LS1_x_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS0_RDATA DMD_LS1_RDATA	N/A	N/A (7)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These routing requirements are specific to the PCB routing. Internal package routing mismatches in the DLPC7540 and DLP471TE, DLP471NE, DLP650TE or DLP651NE have already been accounted for in these requirements.
(2) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(3) This requirement must be maintained from the Controller to the DMD, even if the signals traverse multiple boards.
(4) This is an inter-pair specification (that is, differential pair to differential pair within the group).
(5) This is an intra-pair specification (that is, length mismatch between P and N for the same pair). This is applicable to both clock and data.
(6) This is a channel to channel skew specification.
(7) The low speed read control interface from the DMD is single ended, and makes use of the differential write clock. As such, a routing mismatch between these is not applicable.

10.2 Thermal Considerations

The underlying thermal requirement for the DLPC7540 is that the maximum operating junction temperature (T_J) not be exceeded (defined in the *Section 6.3*). This temperature is dependent on operating ambient temperature, heatsink, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC7540, and power dissipation of surrounding components. The DLPC7540's package is designed to extract heat via the package heat slug to the heatsink, via the thermal balls, and through the power and ground planes of the PCB. Thus, heatsink, copper content, and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC7540 power dissipation and $R_{\theta JA}$ at 0 m/s,1 m/s, and 2 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using the test board described in Section 10.1.1. This test PCB is not necessarily representative of the customers PCB and thus the reported thermal resistance can differ from the actual product application. Although the actual thermal resistance can be different, it is the best information available during the design phase to estimate thermal performance. TI highly recommends that once the host PCB is designed and built that the thermal performance be measured and validated.

To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validate that the maximum recommended case temperature (T_C) is not exceeded. This specification is based on the measured φ_{JT} for the DLPC7540 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. Ensure that the bead and thermocouple wire contact the top of the package. Cover the bead and thermocouple wire with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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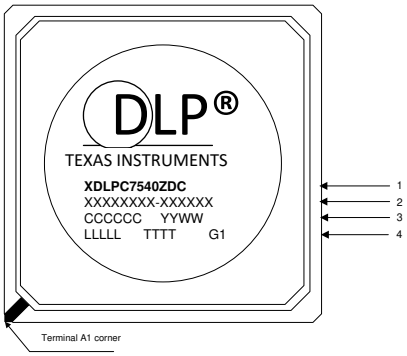
11.1.2 Device Nomenclature

11.1.2.1 Device Markings



Marking Definitions:

Line 1:	TI Part Number: Engineering Samples	X = Engineering Samples DLPC7540 = Device ID blank or A, B, C ... = Part Revision ZDC = Package designator
	TI Part Number: Production	DLPC7540 = Device ID blank or A, B, C ... = Part Revision ZDC = Package designator
Line 2:	Vendor Information	XXXXXXX-XXXXXX
Line 3:	Vendor Country Year and Week code	CCCCCC = Country YY = Year WW = Week May also include 3 character Site Code after WW ZZZ=Site Code
Line 4:	Vendor Lot and Trace Code	LLLLL = Lot code TTTT = Trace code (may be blank)

11.1.2.2 Package Data

Table 11-1. Package Information

PARAMETER	VALUE	UNITS
Number of balls (signal/thermal)	612 / 64	
Ball pitch	1.00	mm
UBM (under bump metallurgy)	0.48 (See Figure 11-1)	mm
BPD (ball pad diameter)	0.58 (See Figure 11-1)	mm
Body dimension	See Mechanical Drawing	mm
Mold compound dimensions	See Mechanical Drawing	mm
Package volume class	350 - 2000 (J-STD-20D)	mm^3
Approximate weight	5.64	g
Substrate circuit	Pb-free	
Package balls	Pb-free	

Table 11-1. Package Information (continued)

PARAMETER	VALUE	UNITS
Solder paste	Pb-free	
Solder profile	T_C =250°C, T_P = 253°C (J-STD-20D)	
Moisture sensitivity level	MSL Level 3 (J-STD-20D)	
Solder ball composition	SAC305	
WIrebond	Cu	
Mounting technique	a) Hot air reflow (including the combination of long and/or medium infrared ray reflow) b) Long or medium infrared ray reflow	

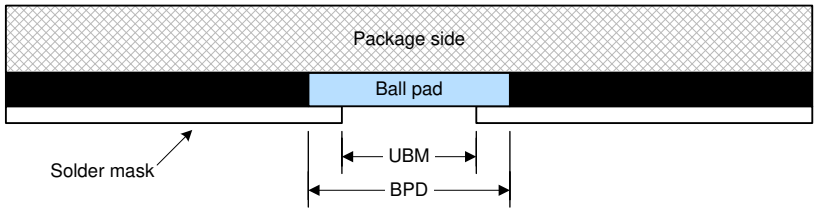


Figure 11-1. Package Ball Parameters

11.2 Trademarks

BrilliantColor™ is a trademark of Texas Instruments Inc.
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11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

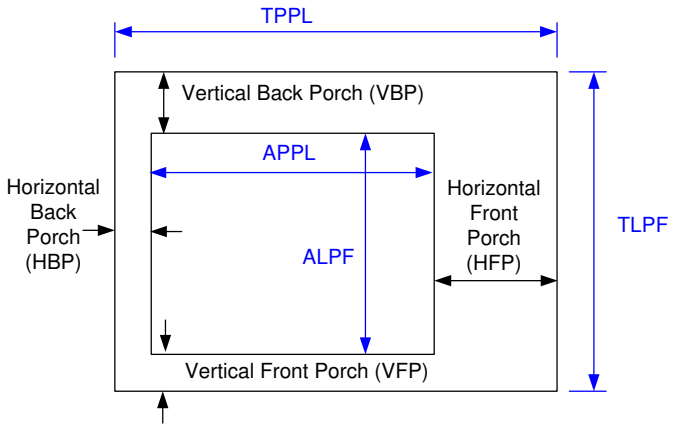
11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11.4.1 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF)	Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.
Active Pixels Per Line (APPL)	Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.
Horizontal Back Porch (HBP) Blanking	Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.
Horizontal Front Porch (HFP) Blanking	Number of blank pixel clocks after the last active pixel but before Horizontal Sync.
Horizontal Sync (HS)	Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.
Total Lines Per Frame (TLPF)	Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

Total Pixel Per Line (TPPL)	Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
Vertical Sync (VS)	Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.
Vertical Back Porch (VBP) Blanking	Number of blank lines after vertical sync but before the first active line.
Vertical Front Porch (VFP) Blanking	Number of blank lines after the last active line but before vertical sync.



12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC7540ZDC	ACTIVE	BGA	ZDC	676	40	TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

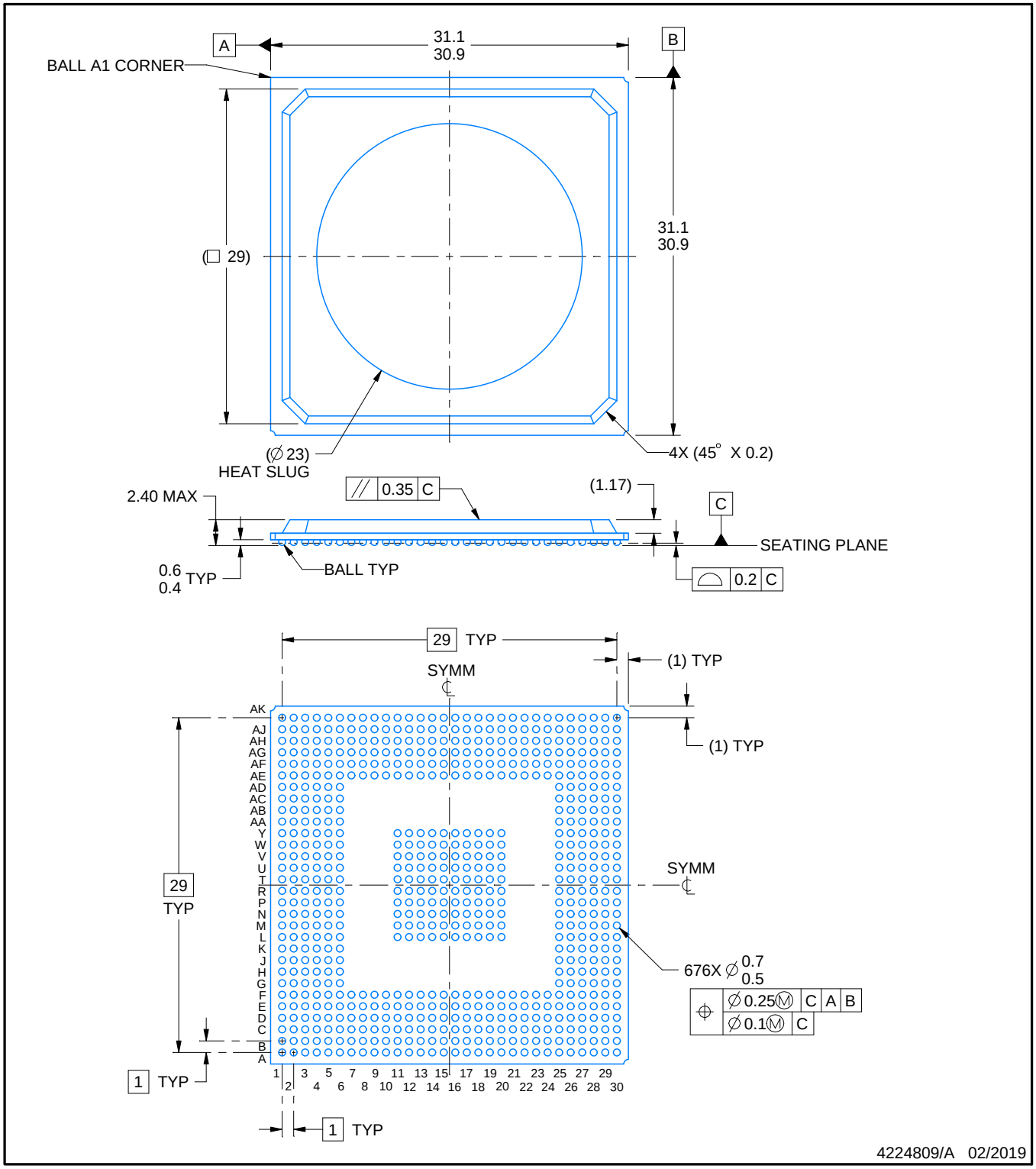
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

ZDC0676A

PBGA - 2.4 mm max height

PLASTIC BALL GRID ARRAY



4224809/A 02/2019

NOTES:

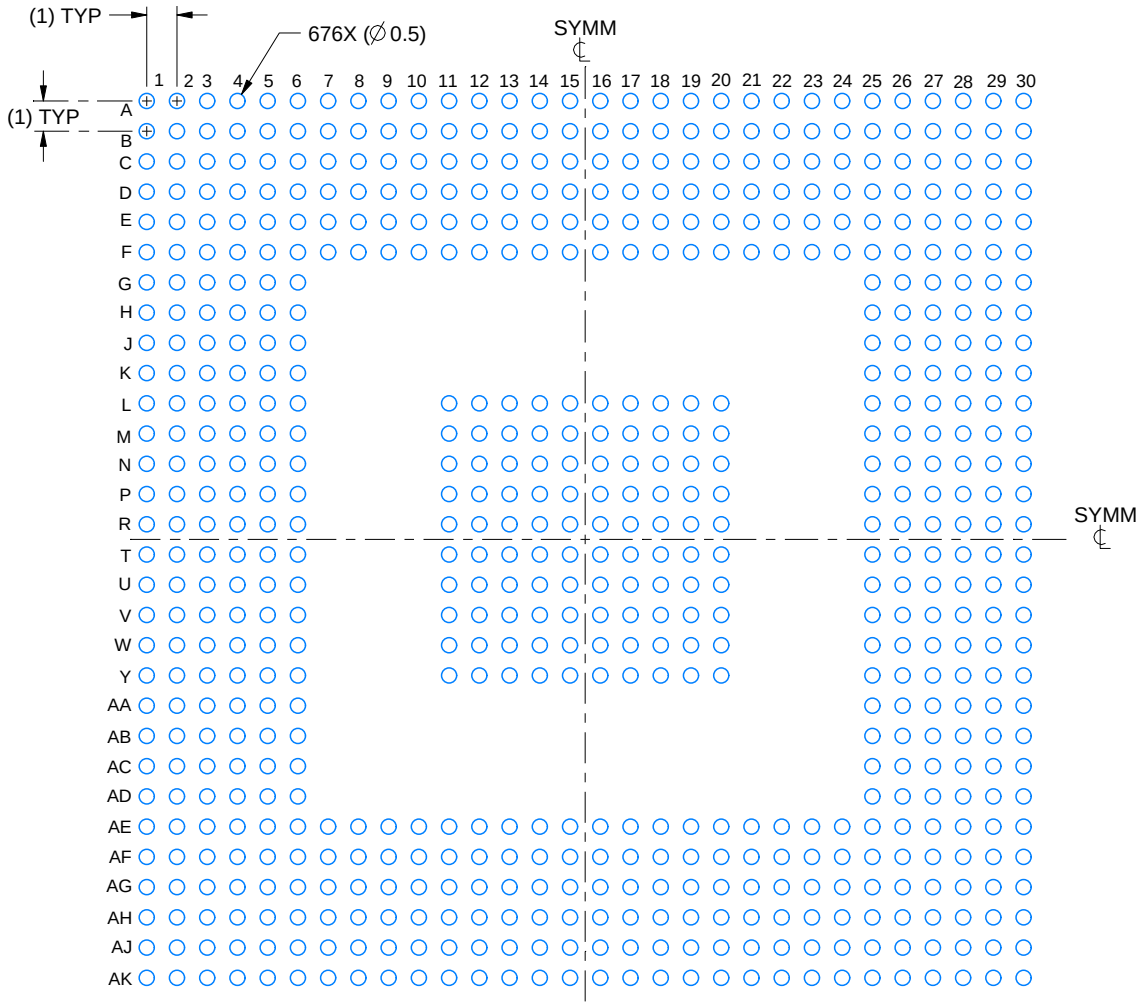
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

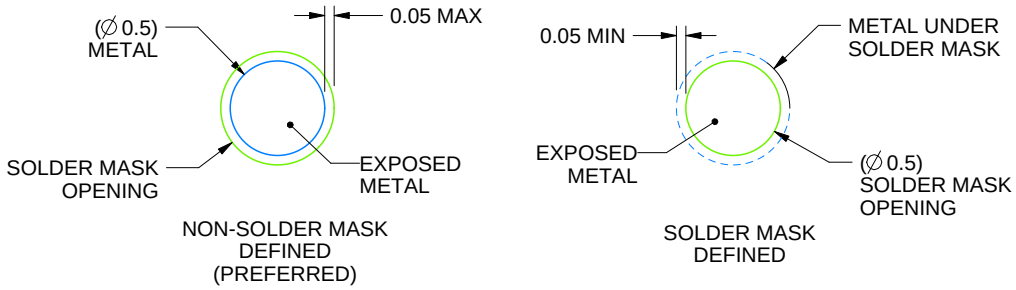
ZDC0676A

PBGA - 2.4 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X

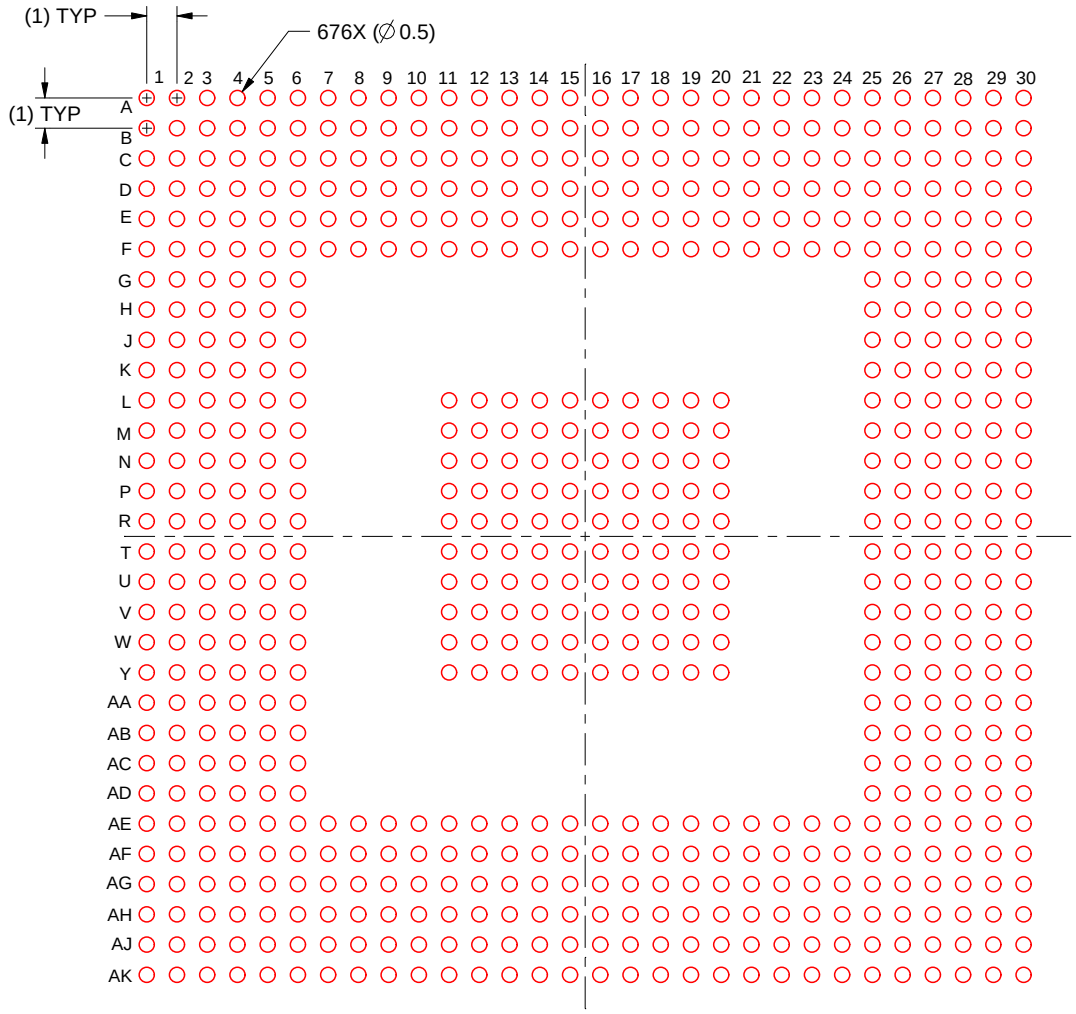


SOLDER MASK DETAILS
NOT TO SCALE

4224809/A 02/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 4X

4224809/A 02/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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